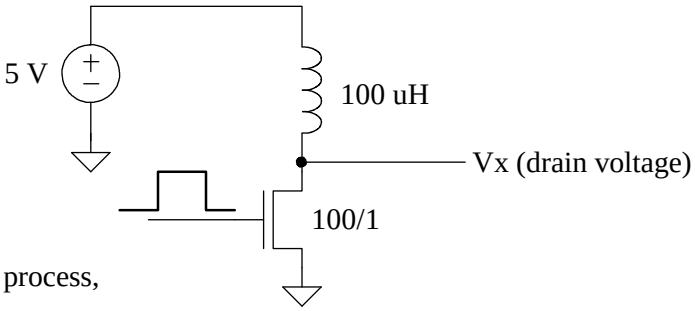
Example 32.3

Examine the circuit seen in Fig. 32.11. Assume that zero current initially flows in the inductor. At t = 10 ns the gate voltage is pulsed to 5 V and the MOSFET turns on. At t = 50 ns the gate voltage goes back to zero. In other words the MOSFET is on between 10 and 50 ns. Determine the voltages and currents in the circuit. Verify your answers using simulations.



Book's long channel process, see Table 6.2.

Figure 32.11 Current flow in an inductor.

This is a common circuit found in circuits that turn on relays, drive stepper motors, and boost switching power supplies (more on this later). With this circuit ***it's easy to destroy*** the MOSFET.

To describe the operation of the circuit note, from Ch. 10, that the effective switching resistance of the NMOS device in the long channel process used in this book is 15k·(1/100) or 150 Ω (remember this is an overestimate as discussed earlier in the chapter). The time constant, L/R, is then 667 ns or much longer than the time that the MOSFET is on. Because of this the voltage on the drain of the MOSFET never moves much beyond 0V when the MOSFET is on. Knowing this, the voltage across the inductor is 5 V when the MOSFET is on and therefore the current through the MOSFET is determined using

$$5\ V = 100\mu H \cdot \frac{di_L}{dt} \tag{32.21}$$

or

$$i_L(t) = 50k \cdot (t - 10ns) \text{ for } 10ns \le t \le 50ns \tag{32.22}$$

The current through the inductor is sketched in Fig. 32.12. It's important to note that the current through the inductor, at 50 ns, wants to continue flowing. In other

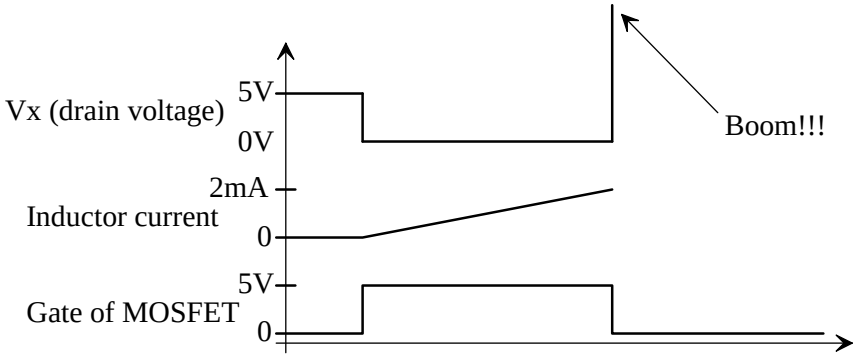


Figure 32.12 Waveforms for the circuit in Fig. 32.11.

words, it's not possible to change the current through an inductor instantaneously (and it's not possible to change the voltage across a capacitor instantaneously). However, with the MOSFET off there is no place for the current flow. The result is that the drain voltage will grow until the MOSFET breaks down providing a path for inductor's current so that the energy stored in the inductor can be released, and the current can go to zero. Simulation results are seen in Fig. 32.13. Note how in these simulation results the current, after the MOSFET breaks down (goes from having a drain voltage of roughly 150V to a having a drain voltage of 0V, the current goes negative. If we were to simulate longer we would see the current, and the drain voltage, actually start to oscillate. In other words, the energy in the circuit is moving back-and-forth between the inductor and the capacitances of the MOSFET. Adding a small resistance to dissipate this energy is a common design practice. We'll talk about this more in a moment.

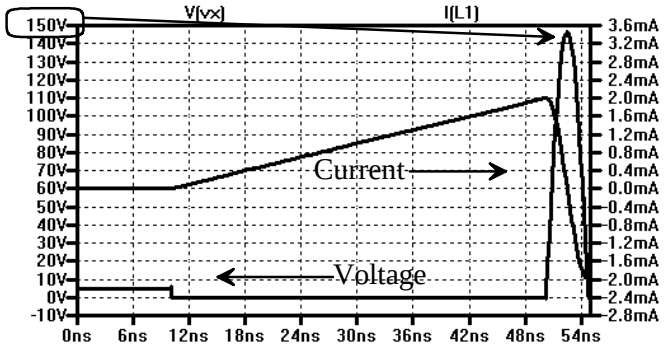


Figure 32.13 Simulation results for the circuit in Fig. 32.11.

Since this is obviously a big problem, and this circuit is widely used, how do we fix this issue? The answer is that we add a diode, as seen in Fig. 32.14. This diode is called a *commutating, snubber, suppressor, catch, or freewheeling diode*. When the drain voltage exceeds 5.6 V (diode turn on of 600 mV), the diode turns on and clamps the drain to 5.6 V. The current flowing in the inductor is diverted back to the power supply and thus the energy stored in the inductor is returned to the power supply. This is an *important circuit in power electronics*.

One last important point, as we discussed in Ch. 2, a forward biased diode has a diffusion capacitance and thus a diffusion (storage) charge that must be removed before the diode can shut off. This current flow is backwards through the diode and will result in ringing because of the inductor, see following example. ■

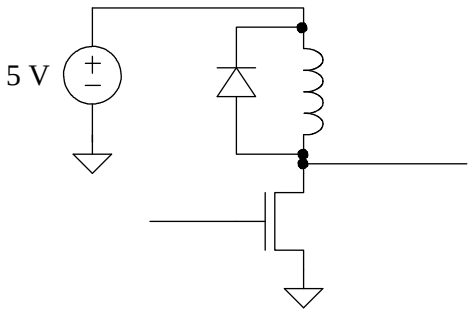


Figure 32.14 Adding a freewheeling diode to the circuit.

Example 32.4

Suppose a snubber diode is used in the circuit seen in Fig. 32.11. Estimate the time it takes for the current in the inductor to go back to zero. Comment on the operation of the circuit. Verify your answers with simulations.

We calculated that when the MOSFET shuts off in Fig. 32.11 the current flowing in the inductor is 2 mA. At this time the voltage on the drain of the MOSFET goes towards a high voltage as shown in the previous example. By adding the freewheeling (snubber) diode seen in Fig. 32.14 the drain voltage is clamped to 5.6 V and the voltage across the inductor is 0.6 V. The current flowing in the inductor is then

$$-0.6\ V = 100\mu H \cdot \frac{di_L}{dt}$$

and thus the current in the diode is

$$i_L(t) = 2mA - 6k \cdot (t - 50ns) \text{ for } 50ns \le t \le 383ns$$

where at roughly 383 ns (assuming diode voltage is always 600 mV, see simulation results in Fig. 32.15) the inductor current has gone from 2 mA down to 0. Notice, in Fig. 32.15, the ringing in both the inductor current and the MOSFET drain voltage.

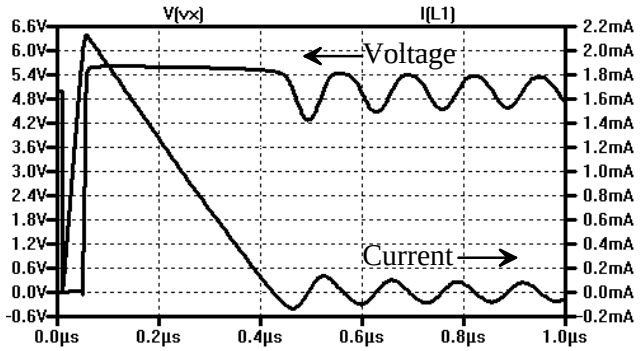
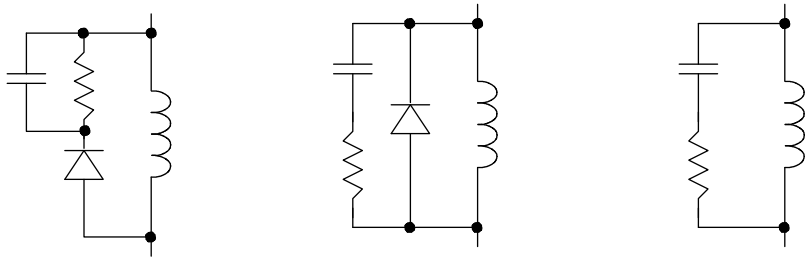


Figure 32.15 Simulating Fig. 32.11 including a snubber diode.

Towards reducing these oscillations consider the *RC* snubber circuits seen in Fig. 32.16 (see simulation examples for LTspice at CMOSedu.com). In 32.16a a resistance is added in series with the diode so that when the diode turns on the energy from the inductor can be used and dissipated as heat (power) in the resistor reducing the energy transferred back to the inductor from the diode's capacitance.



(a) (b) (c)

Figure 32.16 Adding a snubber circuit to reduce oscillations.

In other words, the resistor reduces the *Q* of the *LC* circuit (*L* is the inductor's value and *C* is the capacitance of the diode when it's forward biased, which can be significant, see Ch. 2). The added capacitor shunting the resistor is used to ensure that the circuit responds quickly so that the voltage on the drain of the MOSFET doesn't become too large. In 32.16b a resistor and capacitor are placed in parallel with the diode. The benefit of this topology over the one in Fig. 32.16a is better clamping of the drain voltage. The drawback is that the capacitance shunting the inductor goes up and thus so does the natural frequency of the *LC* circuit. The topology in Fig. 32.16c has the obvious benefit of not having a diode; however, this circuit tends to oscillate for a longer time than the others (for similar values of *R*, *L*, and *C*). Further, without the diode the drain voltage can move considerably higher than the power supply voltage. However, the frequency of the oscillations ($f = 1/(2\pi\sqrt{LC})$) can be controlled as can the length of the oscillations (the extent of the oscillations can be shortened by increasing *R*, that is, by lower the *Q* of the *LC* tank circuit.) By using a smaller *C* and a larger *R*, however, the maximum voltage on the drain of the MOSFET goes up. As with any engineering design, trade-offs must be made (again note that there are additional LTspice simulations for this example downloadable at CMOSedu.com). ■

32.2 Switching Power Supplies: Some Examples

In this section we'll cover the design of three commonly-used switching power supplies (SPSs) used for DC-to-DC conversion (changing from one DC supply voltage to a different DC supply voltage such as going from 5V to 2.5V). The benefit of using a SPS over a linear regulator is the increased efficiency. The first section covers the buck SPS. Buck converters are useful for stepping down a voltage. The second section covers the boost SPS, a converter useful for stepping up a voltage. The third section covers the design of flyback converters. Flyback converters are used in many consumer devices to supply power. These include external power supplies to supply energy to laptops (the "brick" used to power a laptop), cell phones, rechargeable shavers (or most rechargeable devices), USB AC to DC converters, etc. Flyback converters are often connected to the AC line (e.g., 120 V RMS or a sinewave with a peak voltage of 169.7V and a frequency of 50 or 60 Hz). This AC input voltage is rectified to a DC voltage of approximately, for this example, 169V. The DC voltage is then connected to the primary side of a transformer and a switch. The switch is turned on and off (modulated) at, for example, 100 kHz. This is done because a transformer that operates at a frequency of 100 kHz is considerably smaller, and less expensive, than a transformer operating at 50 or 60 Hz. The transformer in a flyback converter also provides isolation form the AC input to ensure the safety of the consumer using the power supply. Finally, in the last section, an example of a control loop using pulse width modulation (PWM) to control these SPS is provided.

32.2.1 The Buck SPS

We talked about the buck, or *step-down*, SPS back in Sec. 32.1.3. In that section we saw that the average of an input pulse waveform was used to generate a DC voltage, see Fig. 32.6. The relationship between the input and output was given by Eq. (32.19) or $V_{out} = D \cdot V_S$ where V_{out} is the DC output voltage and V_S is the input DC voltage. Figure 32.17 shows the output stage of a buck SPS. This topology is referred to as a *synchronous* SPS because the pull-down uses a transistor, MD, instead of a diode (more on this later in the section). Note, in Fig. 32.17, associated waveforms (see Fig. 32.19 for more detail).

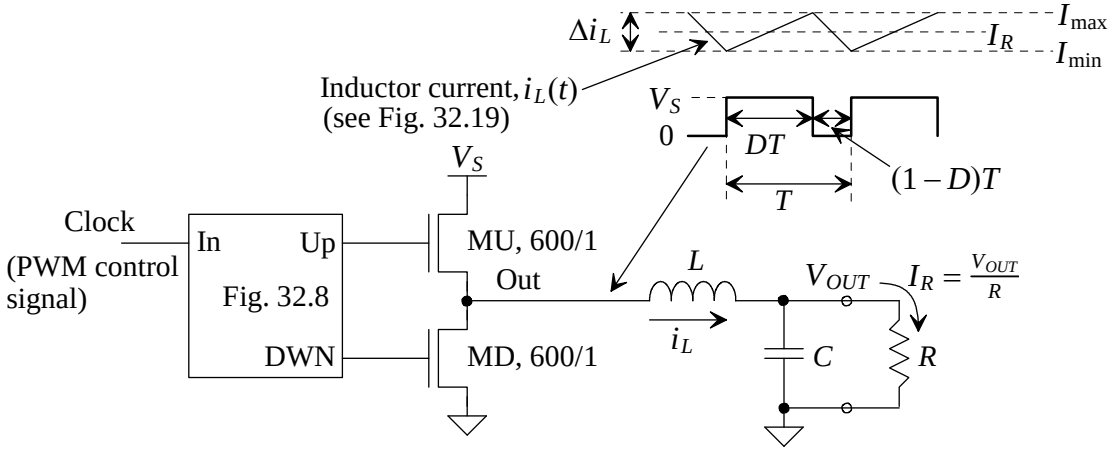


Figure 32.17 Output stage of a Buck SPS.

To analyze the buck SPS let's assume steady-state operation where the output voltage is a DC value of V_{OUT} (right-side of L) and the left-side of L is either 0 or V_S. We won't include the switches "on" resistance in the following derivations. Note, above, that the average value of i_L $(= (I_{max} + I_{min})/2)$ is the load current (modeled above with a resistor) of I_R $(= V_{OUT}/R)$. Also note that if the load current is small, and the change in the inductor Δi_L is large, then the current flowing in MD can actually flow from the source to the drain (the drain current of MD can go negative, this doesn't happen when MD is replaced with a diode). We'll discuss this (MD's drain current going negative) more in a moment and demonstrate this happening using simulations.

To begin let's assume that the left side of L is at V_S (MU is on). The change in the current through L is then

$$v_L = L \cdot \frac{di_L}{dt} = L \cdot \frac{\Delta i_{L,up}}{DT} = V_S - V_{OUT} \tag{32.23}$$

where we note that the frequency of the input signal is f which is $1/T$. When the left side of L is ground (MD is on)

$$0 - V_{OUT} = L \cdot \frac{-\Delta i_{L,dwn}}{(1-D)T} \tag{32.24}$$

Further, we know that (for constant load current I_R)

$$\Delta i_{L,up} - \Delta i_{L,dwn} = 0 = \frac{DT}{L}(V_S - V_{OUT}) - \frac{(1-D)T}{L}V_{OUT} \tag{32.25}$$

or once again the input of the buck SPS, V_S, is related to the output, V_{OUT}, using

$$V_{OUT} = D \cdot V_S \tag{32.26}$$

The maximum current through L is calculated, knowing $\Delta i_L = \Delta i_{L,up} = \Delta i_{L,dwn}$, using

$$I_{max} = I_R + \frac{\Delta i_L}{2} = V_{OUT}\left(\frac{1}{R} + \frac{1-D}{2Lf}\right) \tag{32.27}$$

and the minimum current

$$I_{min} = I_R - \frac{\Delta i_L}{2} = V_{OUT}\left(\frac{1}{R} - \frac{1-D}{2Lf}\right) \tag{32.28}$$

Selecting the Inductor

By setting this last equation to zero we can determine the minimum value of an inductor, $L_{\min}$, needed for a given load to ensure that the current in the inductor doesn't go negative

$$L_{\min} = \frac{R(1-D)}{2f} \tag{32.29}$$

In a practical design as the load current gets small, that is R becomes large, it's impossible to avoid a negative inductor current (current flowing from source to drain of MD). While this current doesn't result in any direct energy use from the input source V_S, it does cause some power dissipation because of the finite on resistance of MD.

In a traditional buck SPS a diode is used in place of MD, Fig. 32.18. The drawback of this topology is that when MU shuts off the diode turns on to continue supplying the current pulled by L which clamps Out to – 0.7 V instead of near 0V as when we used MD. Thus this conventional design topology dissipates more power than a synchronous design. For this reason this topology has fallen out of favor in many modern designs that use lower voltages. The benefit of this topology, however, is that when the inductor current goes to zero the diode shuts off (neglecting reverse recovery time which can be obviated by using a Schottky diode which has the benefit of having a forward voltage drop less than – 0.7 V) and Out goes to V_{OUT}. When the inductor current goes to zero for a part of T (in a traditional buck SPS) the operation is labeled *discontinuous current operation*.

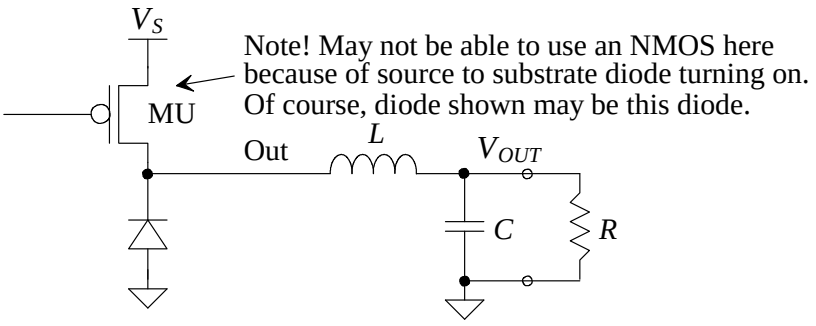


Figure 32.18 Traditional (not a synchronous) buck switching power supply.

Using Eqs. (32.27) and (32.28) we can determine the value of L in terms of the change in the inductor, Δi_L, or

$$\Delta i_L = I_{\max} - I_{\min} = V_{OUT} \cdot \frac{1-D}{Lf} \tag{32.30}$$

and

$$L = V_{OUT} \cdot \frac{1-D}{\Delta i_L \cdot f} \tag{32.31}$$

Selecting the Capacitor

Reviewing Fig. 32.17 note that the current supplied to/from capacitor is the difference between the inductor current and the load current or

$$i_C(t) = i_L(t) - I_R \tag{32.32}$$

The charge going to the capacitor is the area in the bisected triangle, Fig. 32.19, or

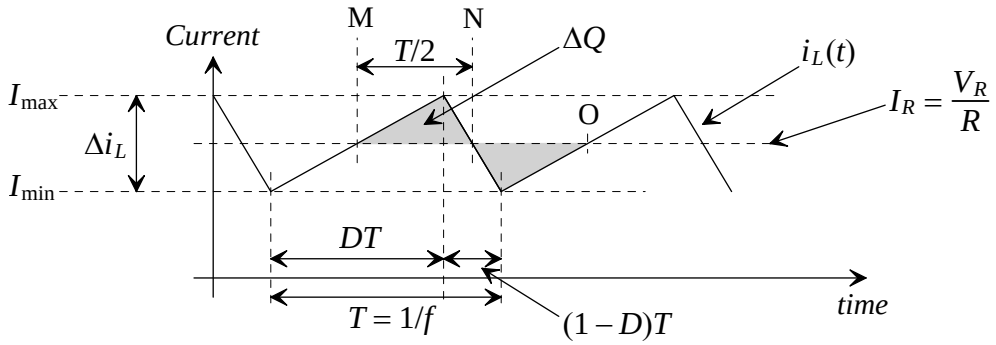


Figure 32.19 Inductor and load currents, difference is capacitor current.

$$\Delta Q = \frac{1}{2} \cdot \frac{T}{2} \cdot \frac{\Delta i_L}{2} = \frac{\Delta i_L \cdot T}{8} \tag{32.33}$$

and the change in the output voltage is

$$\Delta V_{OUT} = \frac{\Delta Q}{C} = \frac{\Delta i_L \cdot T}{C \cdot 8} \tag{32.34}$$

Finally using Eq. (32.31) we can write the minimum value of capacitance required to ensure that $\Delta V_{OUT}/V_{OUT}$ is at no more than some maximum value

$$C_{\min} = \frac{1-D}{8 \cdot L \cdot (\Delta V_{OUT}/V_{OUT}) \cdot f^2} \tag{32.35}$$

Note that for a 0.1% variation in the output voltage $\Delta V_{OUT}/V_{OUT}$ = 0.001. In other words the variation (ripple) in the output is 1 mV for every 1 V in supply voltage.

One last comment; note that between the points M and N, in Fig. 32.19, that *C* is being charged and the voltage across *C* is growing. At point N, where we go from charging the capacitor to discharging the capacitor, the output voltage is at a maximum. Between points N and O the capacitor *C* is being discharged. So at points M and O the output voltage is at a minimum while, again, at point N the output voltage is at a maximum. To calculate the output voltage change over time we can use

$$\Delta v_{OUT}(t) = \frac{1}{C} \cdot \int_0^T (i_L(t) - I_R) \cdot dt \tag{32.36}$$

or, for example when MU is on,

$$\Delta v_{OUT,up}(t) = \frac{1}{C} \cdot \int_0^t \left(\frac{\Delta i_L}{DT} \cdot t - \frac{\Delta i_L}{2}\right) \cdot dt \text{ for } 0 \le t \le DT \tag{32.37}$$

and when MD is on (keeping the equation simpler by redefining $t = 0$)

$$\Delta v_{OUT,dwn}(t) = \frac{1}{C} \cdot \int_0^t \left(\frac{-\Delta i_L}{(1-D)T} \cdot t + \frac{\Delta i_L}{2}\right) \cdot dt \text{ for } 0 \le t \le (1-D)T \tag{32.38}$$

or

$$v_{OUT}(t) = V_{OUT} + \Delta v_{OUT,up}(t) \text{ for } 0 \le t \le DT \tag{32.39}$$

and

$$v_{OUT}(t) = V_{OUT} + \Delta v_{OUT,dwn}(t - DT) \text{ for } DT \le t \le T \tag{32.40}$$

Noting that $v_{OUT}(t) = V_{OUT}$ when $i_L(t) = I_{max}$ and I_{min}.

Example 32.5

Using the buck SPS topology seen in Fig. 32.17 design a power supply that can supply 2V (= V_{OUT}) and up to 50 mA. Assume V_S = 5 V and f = 10 MHz. Comment on your design choices and simulate the operation of your design.

First thing we'll comment on is that the switches in Fig. 32.17 have an on resistance of, as discussed earlier, roughly 5 Ω. This means that if we don't increase the widths of MU and MD we'll drop a voltage across each and won't reach 2 V (with a duty cycle, *D*, of 2/5 or 0.4). In a practical circuit, one that employs a feedback loop (see Secs. 32.2.4 and 32.3), this will be much less of a problem because the feedback loop adjusts the PWM control signal (the *D*) to regulate the output voltage to the correct value. Putting this aside for the moment let's proceed with the example.

Under full load the value of *R* used to model the load is 2/50mA or 40 Ω. Of course the value of *R* used to model the load is larger when the load pulls less current. Using Eq. (32.29) we can calculate the minimum value of *L* to ensure that the inductor current doesn't go negative

$$L = \frac{R(1-D)}{2f} = \frac{40(1-0.4)}{20\times 10^6} = 1.2\ \mu H$$

This result is a bit misleading. It indicates that under full-load, 50 mA, the current in the inductor won't go negative using this value. Looking at Fig. 32.19 we see this means that I_{max} is 100 mA and I_{min} is 0. Such a large variation in the inductor current is almost always undesirable. Here we'll set *L* to 100 μH (*R* roughly 4k or for a load current of 500 μA). According to these calculations below a 500 μA load current the current in the inductor will go negative. At full-load the current in the inductor varies from 51 to 49 mA.

Next we'll select the value of the capacitor, *C*, using Eq. (32.35). Let's assume that the output variation is 1% at full-load

$$C = \frac{1-0.4}{8\cdot 100\mu\cdot 0.001\cdot (10\times 10^6)^2} = 7,500\ pF$$

Of course using a larger capacitor, if possible, is desirable (the larger capacitor doesn't cost too much, can fit in the circuit, etc.). Figure 32.20 shows the simulation results where the power supply is driving a 40 Ω load (zoom in to see the roughly 2 mV ripple [0.1%] in the output voltage). As expected the output

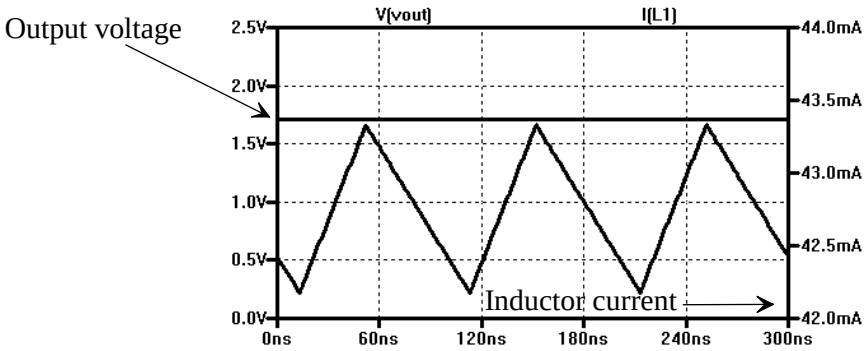


Figure 32.20 Simulating the buck SPS in Ex. 32.5 with a 40 ohm load.

voltage doesn't reach 2V because of the MOSFET's on-resistance. Note that, in this example, we simply don't increase the widths of the MOSFETs or specify a lower maximum supply current so that the output does go to 2V so that we can show, later, how the feedback loop adjusts the output voltage to the correct value by changing the duty cycle, *D*. The feedback operation is also important to regulate the output voltage when V_S varies. Of course using "weaker" MOSFETs results in the devices dissipating power which would have to be removed via a heat sink.

Figure 32.21 shows the simulation results if the load is increased to 10kΩ (load current of 200 μA). Note that the output voltage is considerably closer to the value (2 V) calculated using Eq. (32.26) but the effects of finite MOSFET switch resistance are still noticeable (output voltage slightly below 2 V). Also note that I_{MAX} is 800 μA and I_{MIN} is −400 μA (which flows from source to drain [backwards] of MD) which average to I_R of 200 μA. ■

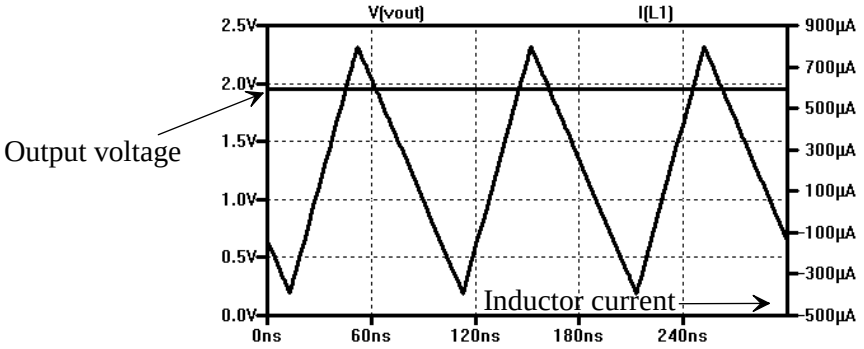


Figure 32.21 Simulating the buck SPS in Ex. 32.5 with a 10k load.

Example 32.6

Repeat Ex. 32.5 for the traditional buck SPS seen in Fig. 32.18.

To do this example we simply replace MD with a diode and replace MU with a PMOS device (1800/1 in the simulation). Again, as discussed earlier, the drawback of using the diode is the increased power dissipation. When we derived the equations in this section we assumed that the MOSFET on resistance was small so that the left side of the inductor was driven to precisely V_S and ground. By using the diode the voltage drop across the pull-down goes from the assumed 0V to, say, −0.7 V. Having a larger swing on the left side of *L* (here the swing is from 5V down to −0.7 V) with $D = 0.4$ should result in an output voltage of $5.7 \cdot 0.4 = 2.28$ *V*, which is good (neglecting the diode power dissipation), right? Simulation results, using a 40Ω load, are seen in Fig. 32.22 and show a considerably lower output voltage. Why? Even though we are using a fast switching diode the reverse recovery time of the diode is an issue (see Ch. 2). Again, when the PMOS turns on, ideally, the left side of *L* is pulled to V_S; however, because the stored charge in the diode must be removed, the diode clamps this left side of *L* at −0.7 V for a considerable amount of time. This effectively reduces *D* and causes excessive power dissipation in the PMOS device (a transistor dissipates little power when it's either fully on [small voltage across it] or fully off [no appreciable current flowing through it]). Figure 32.23 shows simulation results if the load is increased to 10k, lower currents so it's easier to shut off the diode and thus the output voltage is higher. ■

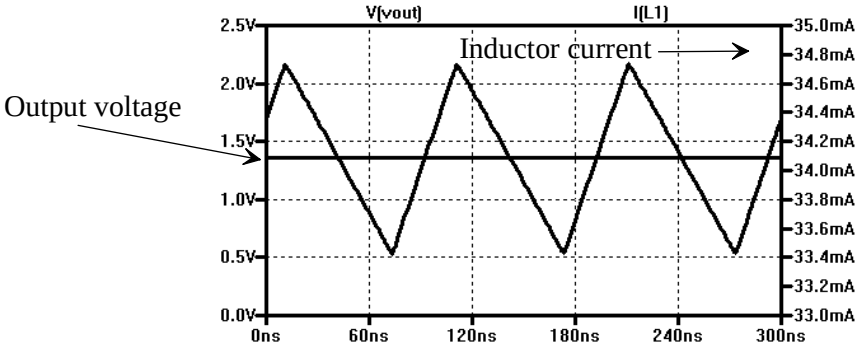


Figure 32.22 Simulating the buck SPS in Ex. 32.5 replacing MD with a diode, 40 ohm load.

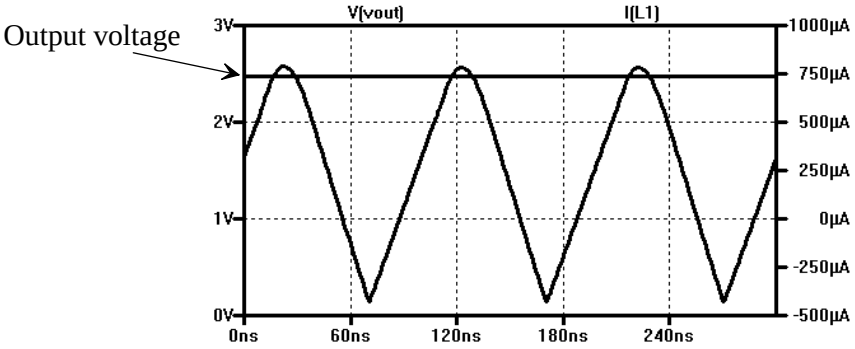


Figure 32.23 Simulating the buck SPS in Ex. 32.5 replacing MD with a diode and 10k load.

Power Supply Efficiency

Before leaving this section let's comment on the efficiency of a power supply. The efficiency is the average power supplied to the load (see Eq. (32.3)) divided by the average power supplied to the power supply (load and power supply circuitry) or

$$Efficiency = \frac{P_L}{P_S} \tag{32.41}$$

Noting that efficiency drops in a power supply as it supplies less current (supplying no current corresponds to 0% efficiency). Efficiency is generally measured under full-load conditions (conditions which, for example, drain a battery faster). Figure 32.24 shows the simulated power supplied to the buck SPS in Ex. 32.5 and the power supplied to the load (note longer simulation time). To get average power we ctrl-left click the mouse button on the trace labels at the top of the display. Here the efficiency is the power supplied to the load (73 mW, not shown below) divided by 88 mW (shown below) or 83% efficiency.

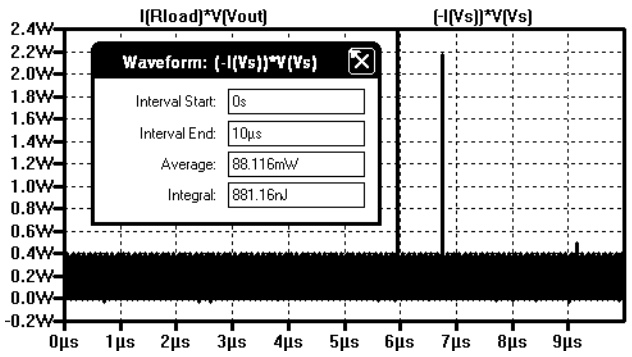


Figure 32.24 Simulating efficiency in the buck SPS from Ex. 32.5.