At this point the design consists of selecting the duty cycle, D, and the filter capacitor, C. Setting V_{OUT} to 5V in Eq. (32.62) results in D of roughly 0.3. The minimum value of R that models the load is calculated as R = 5V/1A or 5 Ω. Assuming we want no more than 10 mV of variation on the 5 V DC output we can determine C using Eq. (32.53)

$$C = \frac{0.3}{5 \cdot 100k \cdot (0.01/5)} = 300\ \mu F$$

Figure 32.32 shows the simulation results for the flyback converter driving a 5 Ω load. In this figure we show the start-up transient, just to be a bit different than the previous simulations which only showed a portion of the simulation. Note that if we increase the load the output voltage will go up a bit. In other words we aren't regulating the output. The next section provides a brief introduction to design of SPS control loops, which are used with the output stages we've covered in this, and the previous two, sections for regulating the output voltage of a power supply. ■

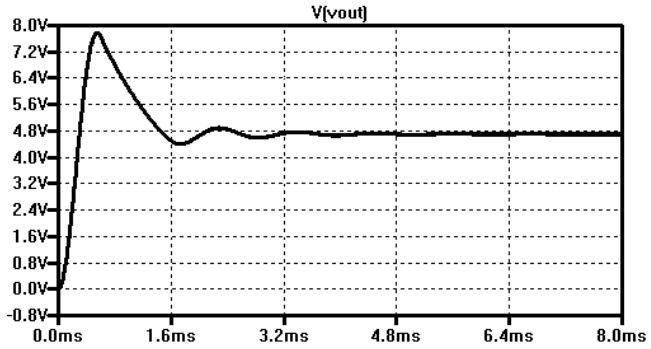

Figure 32.32 Simulating the flyback converter in Ex. 32.9 supplying energy to a 5 ohm load.

32.2.4 Pulse Width Modulation: A Control Loop Example

A pulse-width modulation (PWM) control circuit is seen below in Fig. 32.33. The goal of this circuit is to supply a PWM control signal at a frequency f (= 1/T) with a duty cycle, D, that ensures that the output voltage of the SPS is regulated to the right value with changes in the load, V_S, temperature, etc. Before getting into the design procedures let's give an example. Let's assume that the output, V_{OUT}, of the SPS is to be regulated to 2.5V.

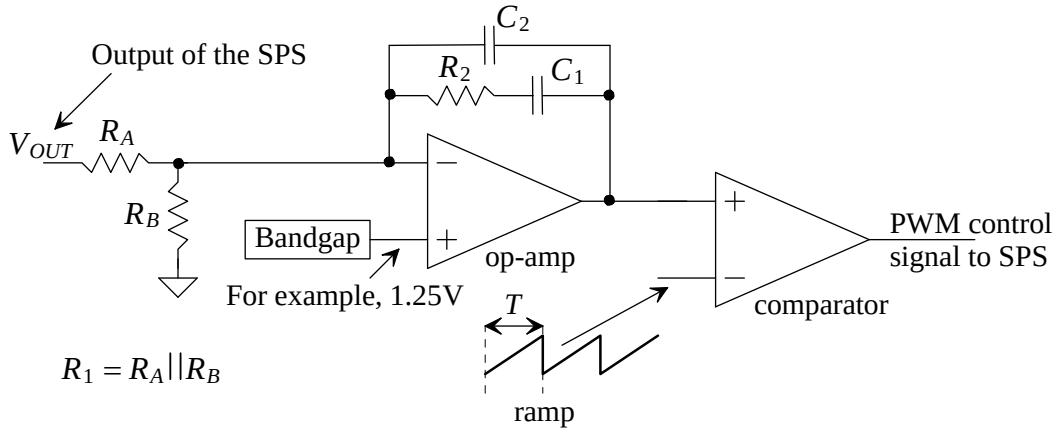

Figure 32.33 Pulse-Width Modulation (PWM) control circuit.

Since we are using a standard bandgap, see Ch. 23, the voltage on the non-inverting input of the op-amp is 1.25V. We set $R_A = R_B$ so that when $V_{OUT} = 2.5V$ the non-inverting terminal of the op-amp is 1.25V and no current flows into the feedback network of the op-amp. Note that V_{OUT}, R_A, and R_B can be Thevenized into a voltage source and a resistor with values

$$V_{OUT} \cdot \frac{R_B}{R_A + R_B} \text{ and } R_A || R_B = R_1 \tag{32.63}$$

These components are adjusted to regulate V_{OUT} to the desired value (set the Thevenized voltage source equal to the bandgap voltage and solve for R_A and R_B for a particular output voltage). In Fig. 32.33 we simplify the notation and by setting $R_1 = R_A || R_B$.

Next suppose V_{OUT} is too low. This causes the output of the op-amp to go up. When the op-amp output voltage is compared to the ramp voltage the result is that the output of the comparator will be high more often, that is, D, goes up. This will cause V_{OUT} to move back up to the correct value.

The reader may recognize the op-amp portion of the circuit in Fig. 32.33 as the active-PI (proportional plus integral) error amplifier seen back in Fig. 19.30. This "error amplifier" is also referred to as a "type-II" error amplifier because two resistors (a pole and a zero) are used. A "type-I" error amplifier is a simple integrator, that is, a resistor and a feedback capacitor. The C_2 capacitor is small, generally in the ballpark of $C_1/10$ so it won't be included in the following analysis (it's used to introduce a high-frequency pole to further roll-off the gain and smooth out the effects of switching in the loop). The transfer function of this error amplifier is, again (see Ch. 19),

$$-\frac{1 + sC_1R_2}{sR_1C_1} = \underbrace{-\frac{R_2}{R_1}}_{\text{Proportional}} \underbrace{-\frac{1}{sR_1C_1}}_{\text{Integral}} \tag{32.64}$$

where the minus sign indicates the fed back signal is subtracted (negative feedback) and

$$f_{un} \approx \frac{1}{2\pi R_1 C_1} \text{ (assuming } f_z >> f_{un}) \text{ and } f_z = \frac{1}{2\pi R_2 C_1} \tag{32.65}$$

These frequencies are the unity-gain frequency and location of the zero in the error amplifier's transfer function, Eq. (32.64). Note that at low frequencies the error amplifier's phase shift is –90 degrees. We've spent a lot of time discussing stability in this book and how it relates to these two terms so we won't repeat that discussion below. Rather, we'll provide examples of PWM control loops for the 3 SPSs we developed in this chapter.

The resonant frequency of the inductor and capacitor used in the SPS is

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{32.66}$$

This LC circuit is in the forward path of the feedback system. The phase response of the LC circuit will start rolling-off before f_0 so we have to ensure that the other components in the forward path don't contribute too much more additional phase shift. Note that instead of using the active-PI error amplifier seen in Fig. 32.33 we could use a simple integrator (remove C_2 and short across R_2) with a unity-gain frequency (aka crossover frequency, the frequency when the gain goes from being greater than one to being less than one) of $1/2\pi R_1 C_1$ (same as above). Then just set the unity-gain frequency to less than $f_0/10$. Again, as discussed above, the added zero using the type-II error amplifier helps with stability so larger pole/zero frequencies can be used (the loop will respond faster).

For the buck SPS in Ex. 32.5 f_0 = 184 kHz (f = 10 MHz), for the boost SPS in Ex. 32.7 f_0 = 5 kHz (f = 1 MHz), and for the flyback SPS in Ex. 32.9 f_0 = 1.3 kHz (f = 100 kHz). Note that the switching frequency, f , is much greater than f_0. Without getting into the details of control-loop analysis and design we'll write the following as guidelines for designing a PWM feedback control loop

*Guideline #*1 $$f_z \le f_0 \tag{32.67}$$

This zero adds to the phase shift through the forward path (which is good and why we don't use the simple integrator, type-I, error amplifier) so we want it less than, or equal to f_0 but greater than the crossover frequency (unity-gain) frequency f_{un}.

Guideline #2 $$f_{un} \le \frac{f_z}{10} \tag{32.68}$$

By using this guideline we help ensure the forward gain of the feedback system is low, and thus the feedback system is stable, when the phase shift through the forward path reaches 180 degrees. We'll use these equations to illustrate examples using the three SPS we designed in this chapter.

Buck SPS Control Loop

For the buck SPS in Ex. 32.5 with, again, f = 10 MHz and f_0 = 184 kHz, we will set f_z to 100 kHz and f_{un} to 5 kHz. Note, again, that the larger the values the faster the loop will respond but the more likely it can become unstable.

We'll assume a standard, that is not low-voltage, bandgap (V_{REF} = 1.25V) is used as the voltage reference. Again, V_{OUT} = 2V in this example. We can then write

$$1.25 = 2 \cdot \frac{R_B}{R_A + R_B} \tag{32.69}$$

One solution is R_A = 6k and R_B = 10k. Using these values, see Fig. 32.33, R_1 = 4.125k. Using Eq. (32.65) C_1 = 7.7 nF (C_2 = 0.77 nF) and R_2 = 206 Ω. (Of course standard values near these would be selected in an actual design). Figure 32.34 shows the simulation results (using these values in the control loop) when the buck SPS power supply is driving a 40 Ω load (constant DC load of 50 mA). Figure 32.35 is a simulation with varying load current. Initially there is no load current. At 200 μs the load current ramps up to a maximum of 50 mA, where it stays for a bit, then decreases back down to zero. Note that the variation in the output voltage, in this simulation, may be more than desirable in some applications. For very fast transients the loop can't respond fast enough. With f_{un} set to 5 kHz we expect response times in the 100 μs time frame. When the loop can't respond fast enough all of the charge for a fast transient would have to be supplied

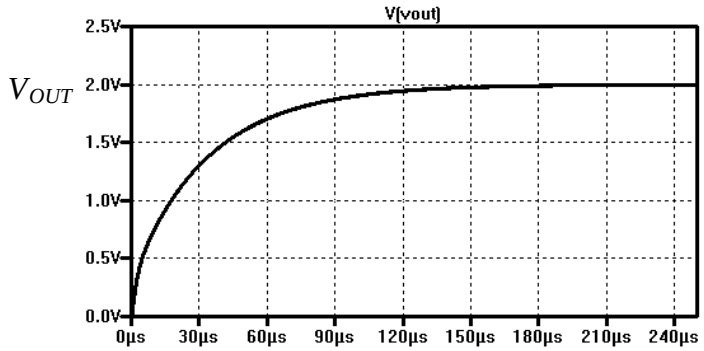

Figure 32.34 Buck SPS from Ex. 3.5 with PWM control driving 40 ohms.

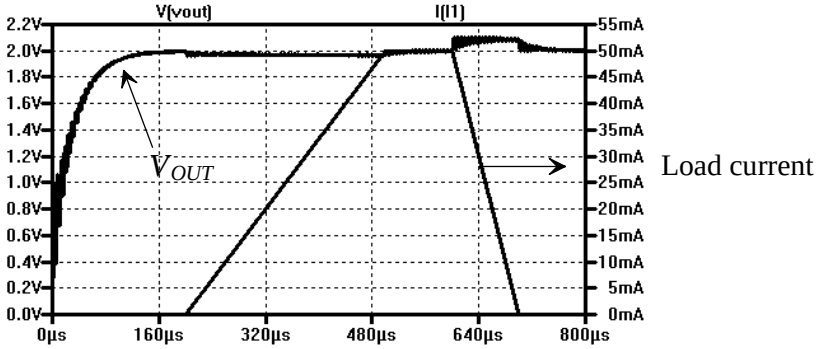

Figure 32.35 Buck SPS from Ex. 3.5 with pulsed current load.

by the filter C (understanding this is important). So, for example, if we were to step the load current from 0 to 50 mA abruptly it would take ($\Delta V/\Delta t = I/C$) only 2·(7,500pF)/0.05 = 300ns for V_{OUT} to go to zero. The feedback loop is too slow to do anything to stop this. The take-away is that if one needs to supply this much current in a very short time the filter C needs to be much, much larger (this shifts f_0 and the other parameters of the control loop).

Boost SPS Control Loop

For the boost SPS in Ex. 32.7 f_0 = 5 kHz (f = 1 MHz) so we'll set f_z to 5 kHz and f_{un} to 100Hz. We want to design the SPS so that its output is 15V

$$15 \cdot \frac{R_B}{R_A + R_B} = 1.25$$

One solution is R_A = 110k and R_B = 10k (larger values, than the 3k maximum load, so that they don't take too much of the boost's output current). Using these values R_1 = 917 Ω. Using Eq. (32.65) C_1 = 0.174 µF (C_2 = 17.4 nF) and R_2 = 183 Ω. Again, in a real design these would be rounded to standard component values. Figure 32.36 shows the simulation results showing start-up and supplying energy to max-load (5 mA, 3kΩ). An interesting thing to do at this point is to vary V_S, or temperature, in the simulation and look at how little V_{OUT} changes. Figure 32.37 shows how the output voltage varies with changing load current. Since our crossover frequency is only 100Hz we expect it will take tens of milliseconds for the loop to respond and regulate the output voltage. Here, again, we are using a relatively fast current waveform to show the output trying to keep up. Again, for fast transients a larger filter capacitor, C, is required. This, as already discussed, shifts f_0 and thus the locations (for a stable loop) of f_{un} and f_z.

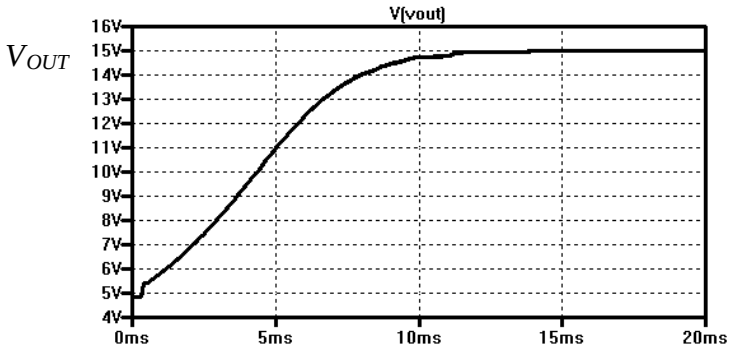

Figure 32.36 Boost SPS from Ex. 3.7 with PWM control driving 3k ohms.

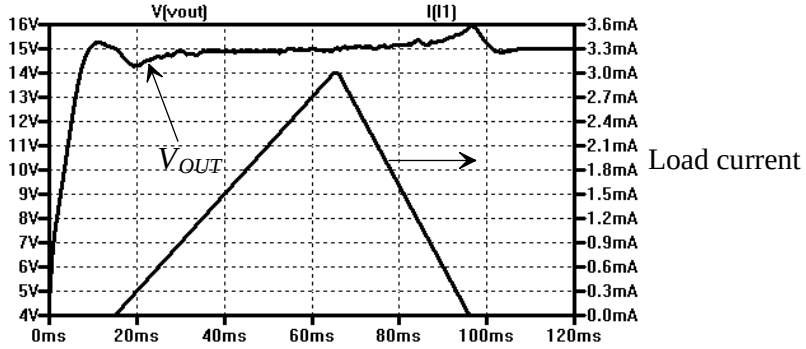

Figure 32.37 Boost SPS from Ex. 3.7 have PWM control and with pulsed current load.

Flyback SPS Control Loop

The flyback SPS topology was seen back in Fig. 32.29. Recall that one of the benefits of using this topology in consumer applications was the safety provided by the transformer, that is, the source and load grounds were isolated. Keeping this isolation is important but presents a design challenge when implementing the PWM control feedback loop. How do we sense an output voltage referenced to one ground and send the information back to modulate the MOSFET (MD) on the primary side of the transformer referenced to a different ground potential? What's commonly done is to use an opto-isolator to generate a light signal corresponding to the output voltage and then use the light signal with a photo-transistor to feed the output voltage information back to the primary for regulation, Fig. 32.38. We need a lower-voltage source to power the control block and the photo-transistor so an extra winding is added around the magnetic core as seen in Fig. 32.38. We've drawn this extra winding on the right side of the transformer symbol but it could have been drawn on the left side of the symbol as well to make the isolation of the source and load grounds clearer. We draw it like this because the left side of the transformer symbol has considerably more turns (a higher voltage is applied across the left side of the transformer) than the lower voltage windings on the right side of the symbol. We won't use an opto-isolator in the following example but rather we will focus on the design of the control loop for a flyback SPS. Note that the delay through the opto-isolator and associated circuitry is an important design concern in a practical SPS.

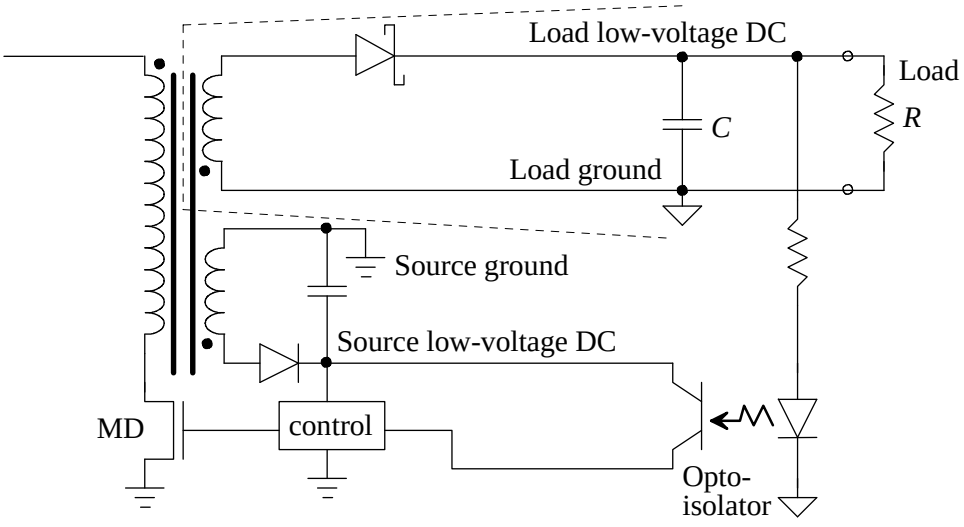

Figure 32.38 Using an opto-isolator in a flyback SPS.

For the flyback SPS in Ex. 32.9 f_0 = 1.3 kHz (f = 100 kHz) so we'll set f_z to 500 Hz and f_{un} to 20Hz. We want to design the SPS so that its output is 5V so we'll set R_A = 3k and R_B = 1k resulting in R_1 = 750 Ω. Again using Eq. (32.65) C_1 = 10.6 μF (C_2 = 1.06 μF) and R_2 = 30 Ω. Figure 32.39 shows the output of the flyback SPS driving a 5 Ω load (1A). Figure 32.40 shows the output of the SPS with a, relatively fast, pulsed current to show the speed limitations of the feedback loop.

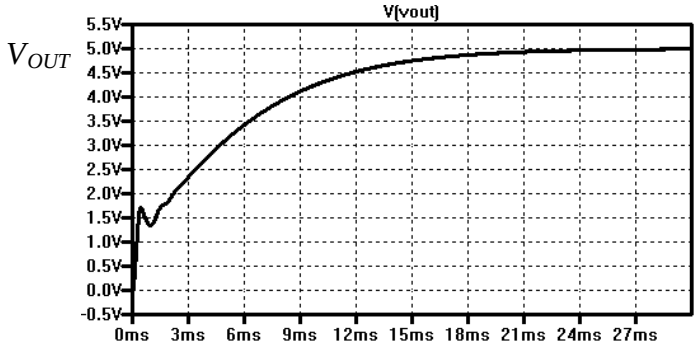

Figure 32.39 Flyback SPS from Ex. 3.9 with PWM control driving 5 ohms (1A).

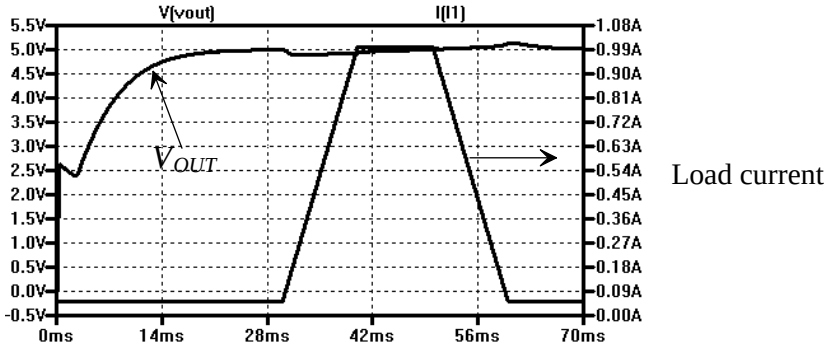

Figure 32.40 Flyback SPS from Ex. 3.9 have PWM control and with pulsed current load.

Effective Series Resistance

As discussed earlier both the inductor and capacitor will have an effective series resistance (ESR). The effects of the ESR of the capacitor can be reduced by paralleling smaller capacitors with the larger capacitor where these smaller capacitors are constructed with different dielectric materials (they have a small ESR at the higher frequencies and this smaller ESR is in parallel with large ESR of the bigger capacitor). The techniques we've developed in this section to design stable PWM control loops are robust and will work if either, or both, the inductor or capacitor has a reasonable ESR. Having said this we should point out that if a capacitor is used with an ESR that is, for the particular design, too large there will be other issues with regulating the output voltage that are unrelated to control loop stability. For example, suppose the 300 μF capacitor used in the flyback SPS designed in Ex. 32.9 has an ESR of 0.1Ω. When the diode shuts off, under full-load conditions, the capacitor has to supply 1A of current to the load. This current being supplied through the 0.1Ω results in a 100 mV drop in voltage across the capacitor (if the output voltage was at 5V it would drop to 4.9). We have the same problem, but in the opposite direction, when the diode turns on and C is charged. In this example there is more than 100 mV variation in V_{OUT} due to the effective series resistance of the capacitor which will result in an inherent hysteresis in the feedback loop.

*Some Comment*s

When we developed our guidelines for the design of a PWM control loop we didn't use switching frequency, *f*, as a design parameter. Why? The answer is that the SPS output filter, the *LC*, decouples the switching frequency from the forward path of the SPS. By increasing *C*, which we may do to reduce output ripple or provide charge for transients as discussed earlier, we move the associated resonant frequency, f_0, of the *LC* circuit downwards. The bigger *C* the lower f_0 and thus the lower the crossover frequency, f_{un}, has to be. All of this is *independent* of the switching frequency *f*.

The phase shift through the forward path (error amplifier) of the feedback system, minus the *LC* circuit, is –90 degrees. We know from numerous other places in the book covering the stability of feedback systems that we want the forward gain of the feedback system to be much less than 1 when the phase shift through the forward path reaches –180 degrees. If we just focus on the *LC* circuit it's phase shift may start rolling off a decade before f_0 (the phase may start to roll-off at $f_0/10$) and go to –90 degrees at f_0. This added to the phase shift from the forward path gets to that –180 degree point. So, we need to kill the gain way before we get to f_0. Here our guidelines specifies that at, or below, f_0 /10 the gain of the error amplifier will crossover and go from an amplifier (gain > 1) to an attenuator (gain < 1). In other words, $f_{un} < f_0/10$. We're done right? Well, we are treating the system as if it's linear, but it's not. To further increase the stability we added R_2 to the error amplifier to introduce a zero (f_z) into the error amplifier's transfer function. The question is where to put this zero? If we place it near, or below, the crossover frequency, f_{un}, it helps with the phase shift but the gain of the error-amp goes up, which is undesirable. By placing f_z at, or below, f_0 we get the increase in phase shift but the increase in gain, because we require $f_{un} \leq f_z/10$, doesn't occur until well after f_{un}.

Lastly, why do we need C_2? This capacitor is used to further smooth the switching waveforms so that the system behaves more linearly. This last point is important. Using frequency response plots that treat the SPS as a linear system to look at stability is a little useful but better stability tests involve transient waveforms, such as changes in load current (as we used in this section).

32.3 Hysteretic Control

Using PWM control in an SPS results in a known switching frequency. One issue with this approach is that it can result in significant, because of the power involved, radiated electromagnetic energy at this switching frequency and its harmonics. This radiation can interfere with the operation of other electronic devices, especially those that are controlled via a wireless connection and is referred to as "electromagnetic interference" (EMI) or "radio frequency interference" (RFI). An example where this is common is found in LED light bulbs. These light sources usually include an SPS. If one were to put one of these LED lights in, for example, a garage door opener it wouldn't be surprising that the remote control could no longer open/close the garage door because of the *radiated EMI* introduced by the SPS in the LED light. In an off-line (one powered by the AC line, the flyback converter discussed earlier is an example) SPS an input ac line filter, Fig. 32.41, is used to reduce EMI. The line filter ensures that switching noise from the SPS doesn't get radiated out on to the wires powering the supply (this is called *conducted EMI*) and prevents EMI on the wires from getting into the SPS from other sources. The Y-capacitors remove common-mode noise on line/neutral by providing a low impedance path for this higher frequency noise to ground. The X-capacitor removes the differential-mode higher frequency noise. One of the benefits of the benefits of hysteretic control is