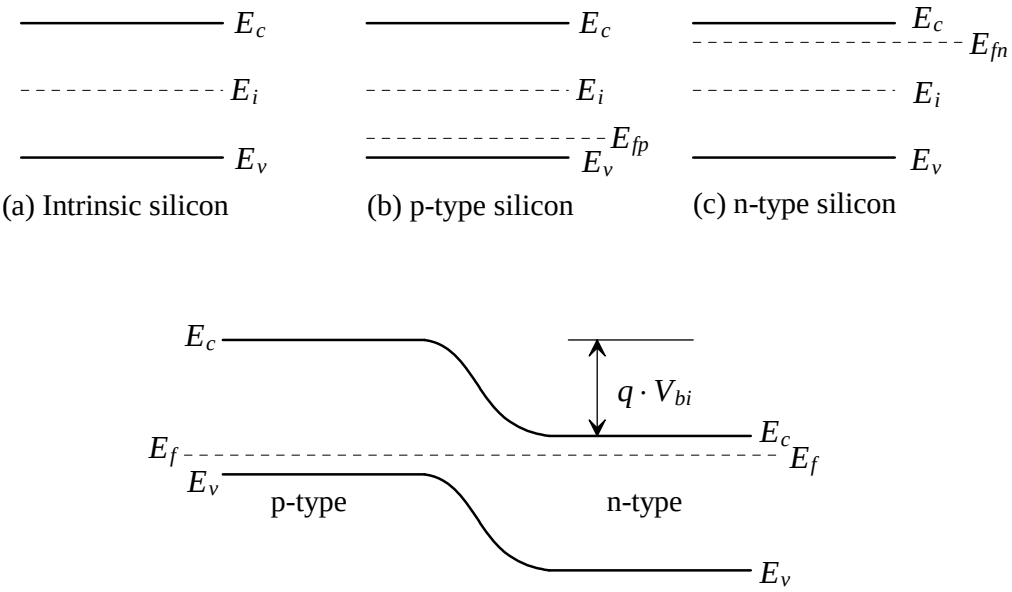

Figure 2.12 The Fermi energy levels in various structures.

The energy difference between the E_i and E_f is given, for a p-type semiconductor, by

$$E_i - E_{fp} = kT \cdot \ln \frac{N_A}{n_i} \tag{2.11}$$

and for an n-type semiconductor by

$$E_{fn} - E_i = kT \cdot \ln \frac{N_D}{n_i} \tag{2.12}$$

The band diagram of a pn junction (a diode) is seen in Fig. 2.12d. Note how the Fermi energy level is constant throughout the diode. A variation in E_f would indicate a nonequilibrium situation (the diode has an external voltage applied across it). To get current to flow in a diode, we must apply an external potential that approaches the diode's contact potential (its built-in potential, V_{bi}). By applying a potential to forward bias the diode, the conduction energy levels in each side of the diode move closer to the same level. The voltage applied to the diode when the conduction energy levels are exactly at the same level is given by

$$V_{bi} = \frac{E_{fn} - E_{fp}}{q} = \frac{kT}{q} \cdot \ln \frac{N_A N_D}{n_i^2} \tag{2.13}$$

noting that $kT/q = V_T$ is the thermal voltage.

2.4.2 Depletion Layer Capacitance

We know that n-type silicon has a number of mobile electrons, while p-type silicon has a number of mobile holes (a vacancy of electrons in the valence band). Formation of a pn junction results in a depleted region at the p-n interface (Fig. 2.13). A depletion region is an area depleted of mobile holes or electrons. The mobile electrons move across the junction, leaving behind fixed donor atoms and thus a positive charge. The movement of holes across the junction, to the right in Fig. 2.13, occurs for the p-type semiconductor as

well with a resulting negative charge. The fixed atoms on each side of the junction within the depleted region exert a force on the electrons or holes that have crossed the junction. This equalizes the charge distribution in the diode, preventing further charges from crossing the diode junction and also gives rise to a parasitic capacitance. This parasitic capacitance is called a *depletion* or *junction* capacitance.

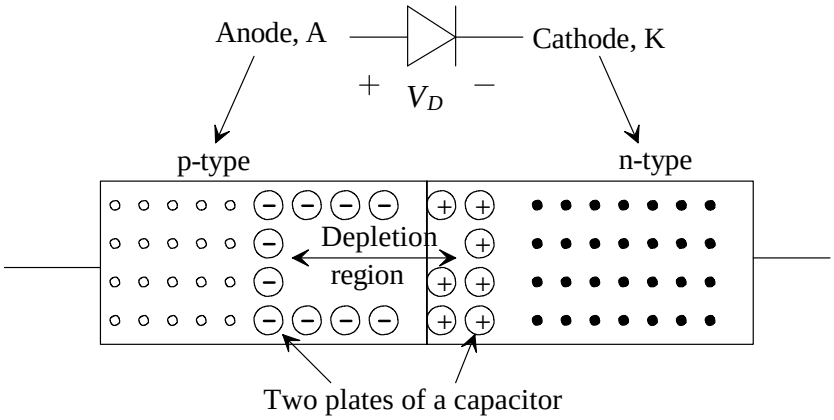

Figure 2.13 Depletion region formation in a pn junction.

The depletion capacitance, C_j, of a pn junction is modeled using

$$C_j = \frac{C_{j0}}{\left[1 - \left(\frac{V_D}{V_{bi}}\right)\right]^m} \qquad (2.14)$$

C_{j0} is the zero-bias capacitance of the pn junction, that is, the capacitance when the voltage across the diode is zero. V_D is the voltage across the diode, m is the grading coefficient (showing how the silicon changes from n- to p-type), and V_{bi} is the built-in potential given by Eq. (2.13).

Example 2.3

Schematically sketch the depletion capacitance of an n-well/p-substrate diode 100 × 100 square (with a scale factor of 1 μm), given that the substrate doping is 10^{16} atoms/cm^3 and the well doping is 10^{17} atoms/cm^3. The measured zero-bias depletion capacitance of the junction is 100 aF/μm^2 (= $100 \times 10^{-18}\ F/\mu m^2$), and the grading coefficient is 0.333. Assume the depth of the n-well is 3 μm.

The n-well doping (n-type side of the diode) has $N_D = 10^{17}$, while the substrate doping has $N_A = 10^{16}$. We can calculate the built-in potential using Eq. (2.13)

$$V_{bi} = 26\,mV \cdot \ln \frac{10^{16} \cdot 10^{17}}{(14.5 \times 10^9)^2} = 759\,mV$$

The depletion capacitance is made up of a *bottom* component and a *sidewall* component, as shown in Fig. 2.14 (see Eq. (5.17) for the more general form of Eq. (2.14)).

The bottom zero-bias depletion capacitance, C_{j0b}, is given by

$$C_{j0b} = (capacitance/area) \cdot (scale)^2 \cdot (bottom\ area) \qquad (2.15)$$

which, for this example, is

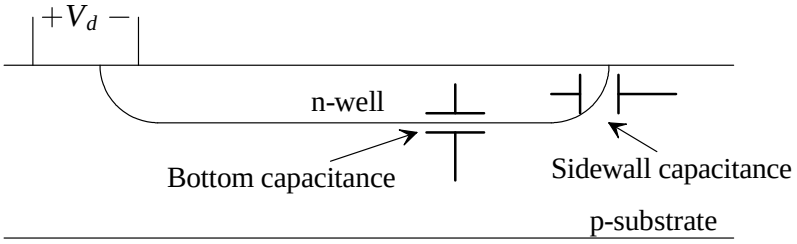

Figure 2.14 A pn junction on the bottom and sides of the junction.

$$C_{j0b} = (100\ aF/\mu m^2) \cdot (1\ \mu m)^2 \cdot (100)^2 = 1\ pF$$

The sidewall zero-bias depletion capacitance, C_{j0s}, is given by

$$C_{j0s} = (capacitance/area) \cdot (depth\ of\ the\ well) \cdot (perimeter\ of\ the\ well) \cdot (scale)^2$$

or (2.16)

$$C_{j0s} = (100\ aF/\mu m^2) \cdot (3) \cdot (400) \cdot (1\ \mu m)^2 = 120\ fF$$

The total diode depletion capacitance between the n-well and the p-substrate is the parallel combination of the bottom and sidewall capacitances, or

$$C_j = \frac{C_{j0b}}{\left[1 - \left(\frac{V_D}{V_{bi}}\right)\right]^m} + \frac{C_{j0s}}{\left[1 - \left(\frac{V_D}{V_{bi}}\right)\right]^m} = \frac{C_{j0b} + C_{j0s}}{\left[1 - \left(\frac{V_D}{V_{bi}}\right)\right]^m} \qquad (2.17)$$

Substituting in the numbers, we get

$$C_j = \frac{1\ pF + 0.120\ pF}{\left(1 - \left(\frac{V_D}{0.759}\right)\right)^{0.33}} = \frac{1.120\ pF}{\left(1 - \left(\frac{V_D}{0.759}\right)\right)^{0.33}}$$

A sketch of how this capacitance changes with reverse potential is given in Fig. 2.15. Notice that when we discuss the depletion capacitance of a diode, it is usually with regard to a reverse bias (V_D is negative). When the diode becomes forward-biased minority carriers, electrons in the p material and holes in the n material, injected across the junction, form a *stored* or *diffusion* charge in and around the junction and give rise to a storage or diffusion capacitance. This capacitance is usually much larger than the depletion capacitance. Furthermore, the time it takes to remove this stored charge can be significant. ■

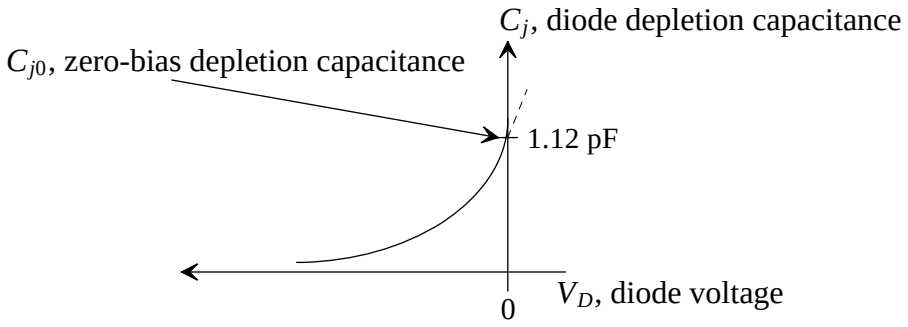

Figure 2.15 Diode depletion capacitance against diode reverse voltage.

2.4.3 Storage or Diffusion Capacitance

Consider the charge distribution of the forward-biased diode shown in Fig. 2.16. When the diode becomes forward biased, electrons from the n-type side of the junction are attracted to the p-type side (and vice versa for the holes). After an electron drifts across the junction, it starts to diffuse toward the metal contact. If the electron recombines, that is, falls into a hole, before it hits the metal contact, the diode is called a *long base diode*. The time it takes an electron to diffuse from the junction to the point where it recombines is called the carrier lifetime, τ_T (see Sec. 2.4.1). For silicon this lifetime is on the order of 10 μs. If the distance between the junction and the metal contact is short, such that the electrons make it to the metal contact before recombining, the diode is said to be a *short base diode*. In either case, the time between crossing the junction and recombining will be labeled τ_T (transit time). A capacitance is formed between the electrons diffusing into the p-side and the holes diffusing into the n-side, that is, formed between the minority carriers. (Electrons are the minority carriers in the p-type semiconductor.) This capacitance is called a **diffusion** capacitance or **storage** capacitance due to the presence of the stored, or diffusing, minority carriers around the forward-biased pn junction.

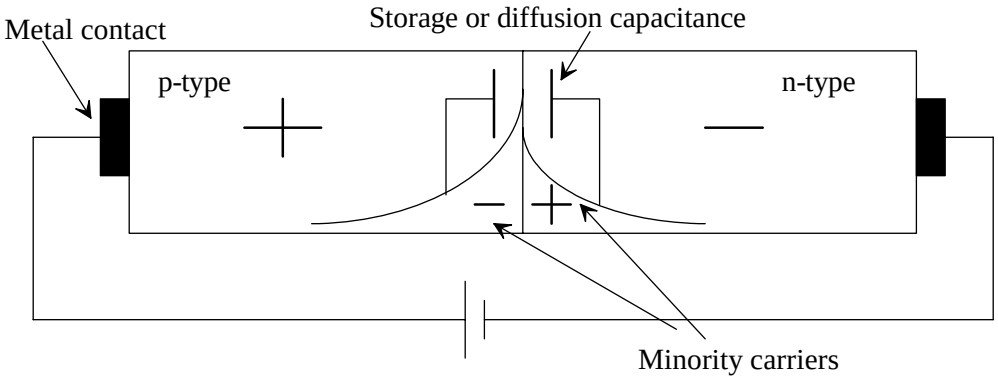

Figure 2.16 Charge distribution in a forward-biased diode.

We can characterize the storage capacitance, C_S, in terms of the minority carrier lifetime. Under DC operating conditions, the storage capacitance is given by

$$C_S = \frac{I_D}{nV_T} \cdot \tau_T \qquad (2.18)$$

I_D is the DC current flowing through the forward-biased junction given by Eq. (2.4). Looking at the diode capacitance in this way is very useful for analog AC small-signal analysis. However, for digital applications, we are more interested in the large-signal switching behavior of the diode. It should be pointed out that, in general, for a CMOS process, it is undesirable to have a forward-biased pn junction. If we do have a forward-biased junction, it usually means that there is a problem. For example, electrostatic protection diodes are turning on (Fig. 4.17), capacitive feedthrough is possibly causing latch-up, or such. These topics appear in more detail later in the book.

Consider Fig. 2.17. In the following diode switching analysis, we assume that $V_F >> 0.7$, $V_R < 0$ and that the voltage source has been at V_F long enough to reach steady-state condition; that is, the minority carriers have diffused out to an equilibrium condition. At the time t_1, the input voltage source makes an abrupt transition from a

forward voltage of V_F to a reverse voltage of V_R, causing the current to change from $\frac{V_F - 0.7}{R}$ to $\frac{V_R - 0.7}{R}$. The diode voltage remains at 0.7 V, because the diode contains a stored charge that must be removed. At time t_2, the stored charge is removed. At this point, the diode basically looks like a voltage-dependent capacitor that follows Eq. (2.14). In other words for $t > t_2$, the diode-depletion capacitance is charged through R until the current in the circuit goes to zero and the voltage across the diode is V_R. This accounts for the exponential decay of the current and voltage shown in Fig. 2.17.

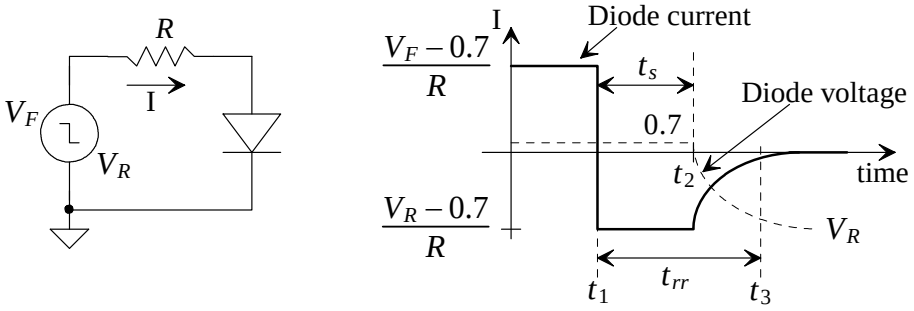

Figure 2.17 Diode reverse recovery test circuit.

The diode storage time, the time it takes to remove the stored charge, t_s, is simply the difference in t_2 and t_1, or

$$t_s = t_2 - t_1 \tag{2.19}$$

This time is also given by

$$t_s = \tau_T \cdot \ln \frac{i_F - i_R}{-i_R} \tag{2.20}$$

where $\frac{V_F - 0.7}{R} = i_F$ and $\frac{V_R - 0.7}{R} = i_R$ = a negative number in this discussion. Note that it is quite easy to determine the minority carrier lifetime using this test setup.

Defining a time t_3, where $t_3 > t_2$, when the current in the diode becomes 10% of $\frac{V_R - 0.7}{R}$, we can define the diode reverse recovery time, or

$$t_{rr} = t_3 - t_1 \tag{2.21}$$

Note that the reverse recovery time (the time it takes to shut off a forward-biased diode) is one of the big reasons that digital circuits made using silicon bipolar transistors don't perform as well, in general, as their CMOS counterparts.

2.4.4 SPICE Modeling

The SPICE diode model parameters are listed in Table 2.1. The series resistance, R_s, results from the finite resistance of the semiconductor used in making the diode and the contact resistance, the resistance resulting from a metal contact to the semiconductor. At this point, we are only concerned with the resistance of the semiconductor. For a reverse-biased diode, the depletion layer width changes, increasing for larger reverse voltages (decreasing both the capacitance and series resistance, of the diode). However, when we model the series resistance, we use a constant value. In other words, SPICE will not show us the effects of a varying R_S.

Table 2.1 SPICE parameters related to diode.

Name	SPICE	
I_S	IS	Saturation current
R_S	RS	Series resistance
n	N	Emission coefficient
V_{bd}	BV	Breakdown voltage
I_{bd}	IBV	Current which flows during V_{bd}
C_{j0}	CJ0	Zero-bias pn junction capacitance
V_{bi}	VJ	Built-in potential
m	M	Grading coefficient
τ_T	TT	Carrier transit time

Example 2.4

Using SPICE, explain what happens when a diode with a carrier lifetime of 10 ns is taken from the forward-biased region to the reverse-biased region. Use the circuit shown in Fig. 2.18 to illustrate your understanding.

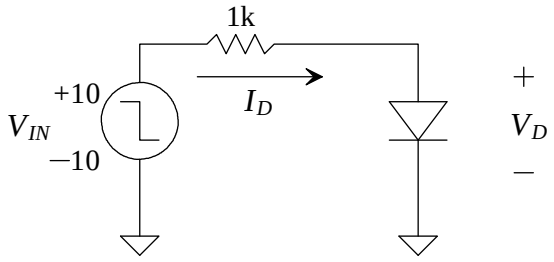

Figure 2.18 Circuit used in Ex. 2.4 to demonstrate simulation of a diode's reverse recovery time.

We assume a zero-bias depletion capacitance of 1 pF. The SPICE netlist used to simulate the circuit in Fig. 2.18 is shown below.

```
*** Figure 2.19 CMOS: Circuit Design, Layout, and Simulation ***

.control
destroy all
run
let id=-i(vin)*1k
plot vd vin id
.endc

D1      vd      0       Dtrr
R1      vin     vd      1k
Vin     vin     0       DC      0       pulse 10 -10 10n .1n .1n 20n 40n

.Model Dtrr  D   is=1.0E-15 tt=10E-9 cj0=1E-12 vj=.7 m=0.33
.tran 100p 25n
.end
```

Figure 2.19 shows the current through the diode (I_D), the input voltage step (V_{IN}), and the voltage across the diode (V_D).

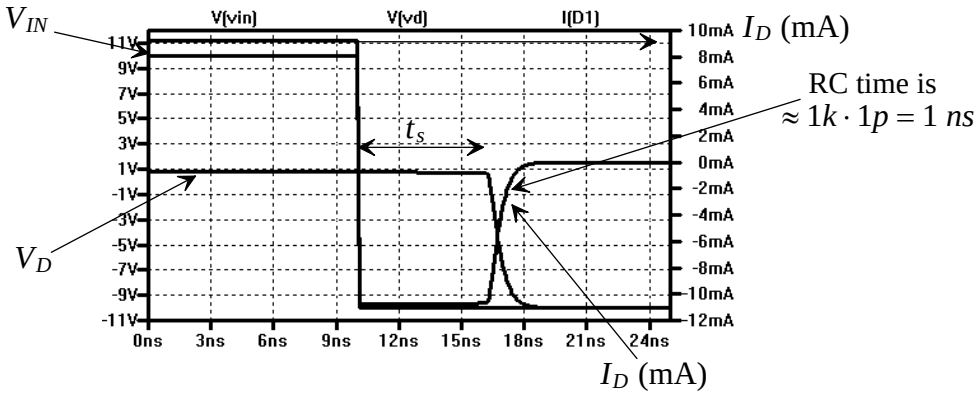

Figure 2.19 The simulation results for Ex. 2.4.

What's interesting to notice about this circuit is that current actually flows through the diode in the negative direction (cathode to anode), even though the diode is forward biased (has a forward voltage drop of 0.7 V). During this time, the stored minority carrier charge (the diffusion charge) is removed from the junction. The storage time is estimated using Eq. (2.20)

$$t_s = 10ns \cdot \ln \frac{9.3 + 10.7}{10.7} = 6.25\ ns$$

which is close to the simulation results. Note that the input pulse doesn't change until 10 ns after the simulation starts. This ensures a steady-state condition when the input changes from 10 to –10 V. ■

2.5 The RC Delay through an N-well

At this point, we know that the n-well can function as a resistor and as a diode when used with the substrate. Figure 2.20a shows the parasitic capacitance and resistance associated with the n-well. Since there is a depletion capacitance from the n-well to the substrate, we could sketch the equivalent symbol for the n-well resistor, as shown in Fig. 2.20b. This is the basic form of an RC transmission line. If we put a voltage pulse into one side of the n-well resistor, then a finite time later, called the delay time and measured at the 50% points of the pulses, the pulse will appear.

RC Circuit Review

Figure 2.21 shows a simple RC circuit driven from a voltage pulse. If the input pulse transitions from 0 to V_{pulse} at a time which we'll call zero, then the voltage across the capacitor (the output voltage) is given by

$$V_{out}(t) = V_{pulse}(1 - e^{-t/RC}) \qquad (2.22)$$

The time it takes the output of the RC circuit to reach 50% of V_{pulse} (defined as the circuit's delay time) is determined using

$$\frac{V_{pulse}}{2} = V_{pulse}(1 - e^{-t_d/RC}) \rightarrow t_d \approx 0.7RC \qquad (2.23)$$