Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 9,606,907

Issued: March 28, 2017

Filed: August 20, 2013

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

Inter Partes Review No. IPR2018-00362

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,606,907 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

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I. PETITIONER'S MANDATORY NOTICES

A. Real Party-in-Interest (37 CFR § 42.8(b)(1))

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

B. Related Matters (37 CFR § 42.8(b)(2))

U.S Patent No. 9,606,907 B2 ("the 907 Patent") issued on March 28, 2017, and is now involved in the following proceedings:

- *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017)
- *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Cal. filed June 14, 2017)

The 907 Patent is a continuation of U.S. Patent 8,516,185 B2, which issued on August 20, 2013, and is involved in the following proceedings:

- IPR2017-00577 (instituted July 7, 2017 "as to claims 1–3, 7, 8, and 10–12 of the '185 Patent as being unpatentable under 35 U.S.C. 103(a) as obvious over Halbert and Amidi")
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016)
- *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016)

This petition is one of four related petitions against all claims of the 907 Patent. There are four petitions given the length of the claim language and the word limits in 37 C.F.R. § 42.24(a)(1)(i). The four petitions are generally divided as follows:

- IPR petition against claims 1–29 and 58–65 of the 907 Patent based primarily on the Ellsberry reference (Ex.1005)
- IPR petition against claims 30–57 of the 907 Patent based primarily on the Ellsberry reference (Ex.1005)
- IPR petition against claims 1–29 and 58–65 of the 907 Patent based primarily on the Halbert reference (Ex.1006)
- IPR petition against claims 30–57 of the 907 Patent based primarily on the Halbert reference (Ex.1006)

C. Lead and Back-up Counsel (37 CFR § 42.8(b)(3))

Lead Counsel is: Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492.

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- Theodore W. Chandler (Reg. No. 50,319), Sidley-SKH-IPR@sidley.com, (213) 896-5830
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- Ferenc Pazmandi (Reg. No. 66,216), Sidley-SKH-IPR@sidley.com, (415) 772-7410.

D. Service Information (37 CFR § 42.8(b)(4))

Service on Petitioners may be made by e-mail (Sidley-SKH-IPR@sidley.com), mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

II. INTRODUCTION

Petitioners respectfully request institution of trial on all claims of the 907 Patent (Ex.1001), with this Petition addressing claims 1-29 and 58-65, and a companion Petition addressing 30-57. All of the claims in the 907 Patent fundamentally cover the same invention disclosed and claimed in the parent patent, the 185 Patent (Ex.1017), and were only allowed after a terminal disclaimer was filed. Trial was instituted on the parent patent, *see* Ex.1031, and should be instituted here as well based on Ellsberry (Ex.1005), which was not considered during prosecution and matches the 907 Patent even more closely than the art before the Board for the trial on the parent patent.

Ellsberry is remarkably similar to the 907 Patent: Both identify the same problem, which is that increasing the number of memory devices on a memory module increases the electrical load, thus slowing down the system. And both disclose the same solution: adding data buffers along the bottom edge of the memory module, which reduce the load and selectively connect only the memory devices in use, while disconnecting the memory devices not in use. Even the figures in Ellsberry (e.g., Figs.5,13,11) are remarkably similar to the figures in the 907 Patent (e.g., Figs.3C,4A,4B).

Although Ellsberry likely anticipates, this Petition focuses on obviousness to avoid unnecessary disputes. The claims of the 907 Patent are much longer than the

claims in the parent patent, but the extra words do not actually add anything beyond what would have already been employed in conventional memory modules (such as a printed circuit board). Nor do the extra words create any claim construction disputes material to this Petition, given that Ellsberry's disclosure is so similar to the 907 Patent's disclosure that Ellsberry satisfies the claim requirements under any reasonable construction.

Trial should be instituted on all claims based on this Petition and the companion Petition.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the 907 Patent May Be Contested by Petitioner (§42.104(a))

Petitioner certifies it is not barred or estopped from requesting *inter partes* review ("IPR") of the 907 Patent (Ex.1001). Neither Petitioner, nor any party in privity with Petitioner, has filed a civil action challenging the validity of any claim of the 907 Patent. Neither Petitioner, nor any party in privity with Petitioner, has filed a prior IPR challenging the validity of any claim of the 907 Patent. Petitioner also certifies this IPR petition is filed within one year of the date of service of a complaint alleging infringement of a patent. Petitioner therefore certifies this patent is available for *inter partes* review. 37 C.F.R. §§42.101-.102.

B. Fee for Inter Partes Review (§42.15(a))

The Director is authorized to charge the fee specified by 37 CFR §42.15(a) to Deposit Account No. 50-1597.

C. Proof of Service (§§42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

IV. Identification of Claims Being Challenged (§42.104(b))

Claims 1-29 and 58-65 of the 907 Patent are unpatentable under pre-AIA 35 U.S.C. §103(a) as follows:

(i) Claims 1-29 and 58-65 are unpatentable as being obvious over U.S. Pat. Appl. Pub. No. 2006/0277355 by Ellsberry et al. ("Ellsberry") (Ex.1005);

(ii) Claims 1-29 and 58-65 are unpatentable as being obvious over Ellsberry (Ex.1005) in view of JEDEC Standard No.21-C ("JESD21-C") (Ex.1010);

(iii) Claims 7, 19, and 24 are unpatentable as being obvious over Ellsberry (Ex.1005) in view of U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (Ex.1006);

(iv) Claims 9 and 28 are unpatentable as being obvious over Ellsberry (Ex.1005) in view of U.S. Patent No. 7,334,150 to Ruckerbauer et al. ("Ruckerbauer") (Ex.1038); and

(v) Claims 14, 17-23, and 60-65 are unpatentable as being obvious over Ellsberry (Ex.1005) in view of Stone (Ex.1035).

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§**V-VII**. The evidence relied upon in this petition is listed in **Attachment B**. **Attachment C** includes a listing of the challenged claims with each limitation designated with a number and

letter (*e.g.*, [1.a]). These designations are referenced in the claim-by-claim analysis in §**VII** below.

V. Relevant Information Concerning the Contested Patent

A. Effective Filing Date of the 907 Patent

The application that resulted in the 907 Patent is a continuation of an application filed on April 15, 2010, now Patent No. 8,516,185 ("the 185 Patent") (Ex.1017), which is a "continuation-in-part" of an application filed on July 16, 2009, now Patent No. 8,417,870 (Ex.1015). Because each of the prior art references identified in this Petition predates July 16, 2009, Petitioner assumes for this Petition only that the claims of the 907 Patent are entitled to a priority date of July 16, 2009. Ex.1003¶¶43-46.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA" or "Skilled Artisan") in the field of the 907 Patent in 2009 would have had an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. Ex.1003¶47. Such a person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id*. (citing Ex.1041). A POSITA would also have been familiar with the structure and operation of

circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs, and more low level circuits such as tri-state buffers. *Id*. (citing Ex.1035).

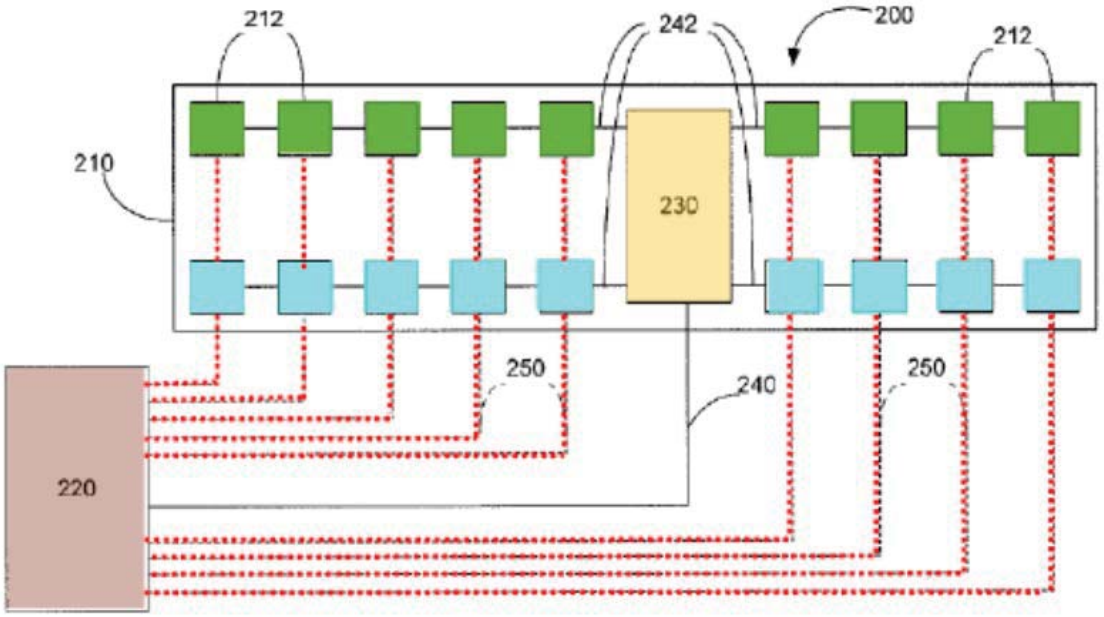
C. The 907 Patent

1. Technical Overview

The 907 Patent is directed to a memory module comprising memory devices, such as dynamic random-access memory (DRAM) or synchronous dynamic random-access memory (SDRAM) devices. Ex.1001 at 1:17-:26; Ex.1003¶¶53-54.

The memory devices on the memory module can be organized into rows or "ranks" (shown in green and blue below). Ex.1001 at 1:36-:42. Such prior-art memory modules were well known, and specific designs were standardized by a consortium called JEDEC. *Id.* at 1:64-:67,4:39-5:13,5:35-6:7,15:12-:14; Ex.1003¶55.

Figure 2A: (Prior Art)

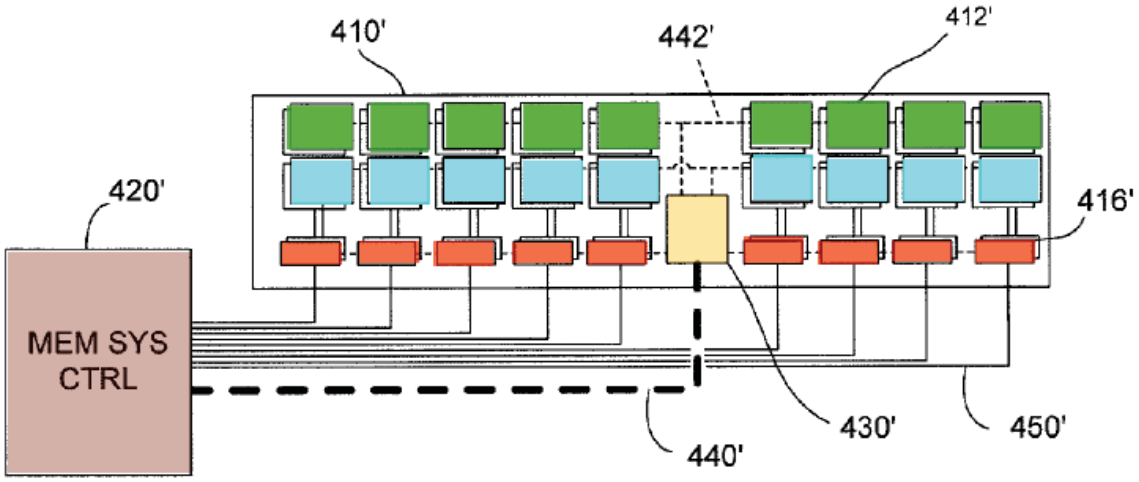


The 907 Patent explains that, in such prior-art systems, increasing memory space can raise problems, such as presenting heavier loads within the system "resulting in a slower system." Ex.1001 at 4:7-4:35,6:54-:55; Ex.1003¶57.

To address this problem, the 907 Patent discloses a "Memory Module with ***Distributed*** Data Buffers." Ex.1001 at Title. An exemplary embodiment of a memory module with such distributed data buffers is shown in Fig.3C (reproduced below with coloring added). *Id.* at 7:35-8:6. The memory module 410' includes multiple ranks of memory devices 412' (green and blue), a control circuit 430' (orange), and multiple data transmission circuits 416' (red) that are "distributed at

corresponding positions relative to the at least one printed circuit board … 410′." *Id.* at 8:20-:22; Ex.1003¶¶60-62.

Figure 3C:



The 907 Patent's "Fig. 5 schematically illustrates an example data transmission circuit 416." Ex.1001 at 15:17-:18. Reproduced below are two copies of Figure 5. The copy labeled Figure 5-1 is annotated along with Figure 4A to show the data transmission circuit 416 (red box) selectively allowing data transmission along "path A" to the memory devices in ranks A and C (while selectively isolating the other memory devices in ranks B and D). The version labeled Figure 5-2 is annotated to show the data transmission circuit 416 (red box) selectively allowing data transmission along "path B" to the memory devices in ranks B and D (while selectively isolating the other memory devices in ranks A and C). Ex.1001 at 15:35-:39,15:65-16:16,16:17-:29,17:63-18:2 (path A),18:10-

:16 (path B); Ex.1003¶¶63-65. In this way, the data transmission circuit 416 disclosed in the 907 Patent creates what the parties have called a "fork in the road" for switching between data paths A and B, thereby selectively allowing transmission of data with only the ranks of memory on one "fork" of the road while reducing the load seen by the system memory controller. Ex.1003¶63,66.

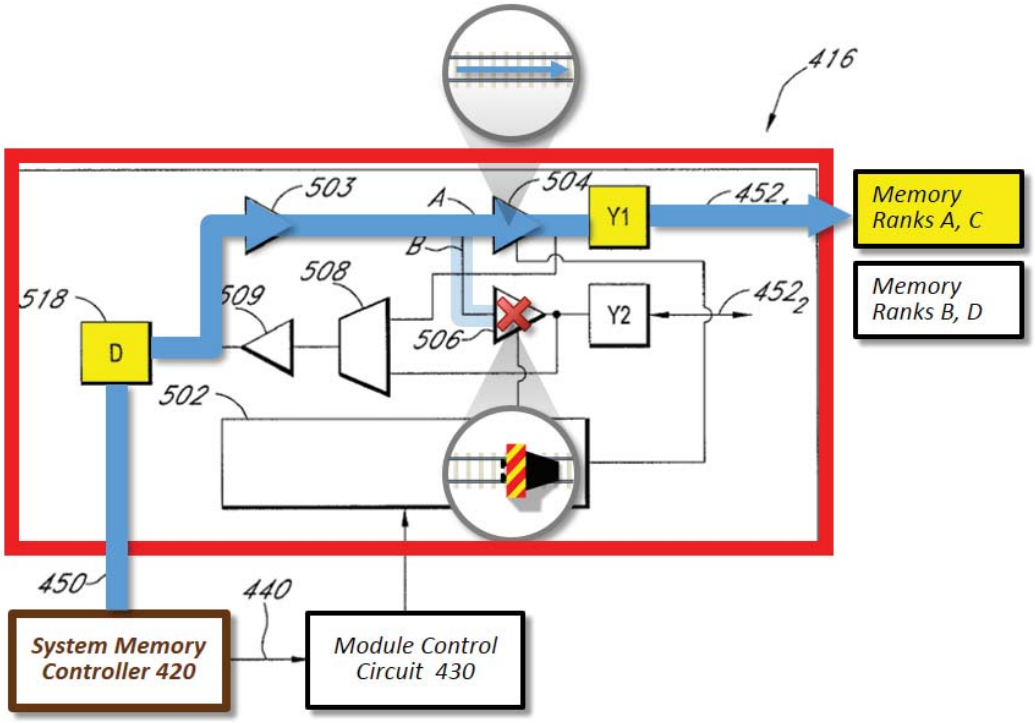


Figure 5-1

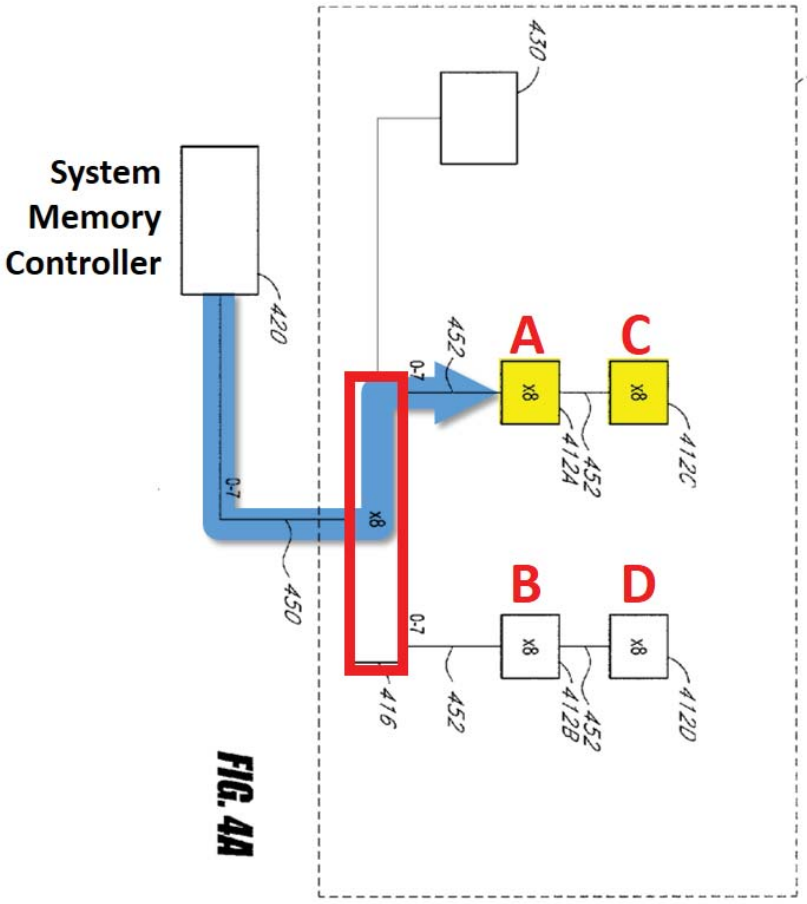

System
Memory
Controller
420
430
450
452
0-7
x8
A
C
B
D
412A
412C
412B
412D
416
FIG. 4A

Figure 4A

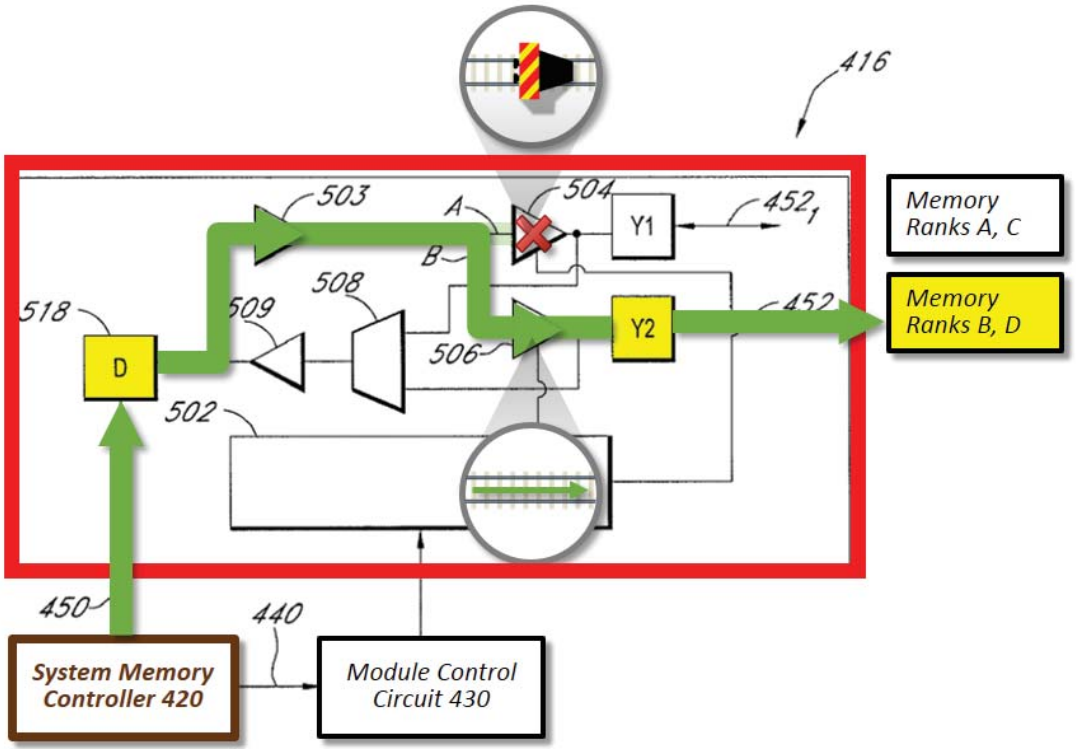


Figure 5-2

2. Summary of the Prosecution History

On November 23, 2015, the examiner rejected all claims for nonstatutory double patenting, citing the claims in the earlier patents in the family (the 870 Patent and the 185 Patent, Exs.1015&1017), either alone or in view of U.S. Patent Application Publication No. 2009/0248969 to Wu et al. ("Wu") (Ex.1021). Ex.1002 at 117-29. In addition, all pending claims were rejected in light of Wu. Ex.1002 at 130-40; Ex.1003¶¶100-101.

In response, the applicants filed a terminal disclaimer, *see* Ex.1002 at 173,310, and declarations by the inventors asserting conception "prior to March 31, 2008" to swear behind Wu, *id*. at 173-309. Ex.1003¶102.

On June 27, 2016, the examiner issued a notice of allowance for several claims. Ex.1002 at 312-20; Ex.1003¶103. After allowance, however, the applicants continued presenting new claims and amendments. Ex.1002 at 338-50,353,358-59,360-83; Ex.1003¶¶104-106.

On October 6, 2016, the examiner allowed some claims, but rejected several of the new claims. Ex.1002 at 389-397. For example, claim 36 was rejected under §112,¶1 for lack of written description. The examiner was concerned that claim 36 could be interpreted to eliminate the "fork in the road" concept discussed above (*see* §V.C.1), which the examiner concluded would be an unsupported interpretation and thus new matter lacking written description. Ex.1003¶107.

After further amendments, cancellation of claims, and addition of new claims (Ex.1002 at 402-35), the examiner allowed all the pending claims on January 13, 2017 (*id*. at 436-41), noting that Halbert (Ex.1006) was the "closest prior art," but allowing the claims because in "the instant invention … different buffers are enabled and disabled," a reference to the "fork in the road" concept. Ex.1003¶¶109-110. On February 23, 2017, the examiner issued supplemental reasons for allowance (Ex.1002 at 455-59), which noted that the claims also require that the non-selected memory devices "aren't even enabled." Ex.1003¶¶111-112.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction *in light* of the specification, 37 CFR §42.100(b), not the broadest *possible* interpretation, *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382-83 (Fed. Cir. 2017). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. §112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48,764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. "*isolate memory device load*"

The broadest reasonable construction of the phrase "*isolate memory device load,*" which appears in independent claims 1, 16, 43, 53, and 58, and dependent claim 32 (depending from independent claim 30), is "electrically separate memory device load." Ex.1003¶¶118-125.

The Board has previously interpreted the phrase "selectively isolate" in the 185 Patent (parent to the 907 Patent) to mean "electrically separate one component from another." Ex.1023 at 8. Further, during recent ITC litigation involving the 185 Patent, Patent Owner's expert agreed that "isolation always requires electrical separation." Ex.1024 at 1015:21-23; Ex.1026 at 12; Ex.1029 at 4; Ex.1003¶¶86,89,119.

2. "*the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command*"

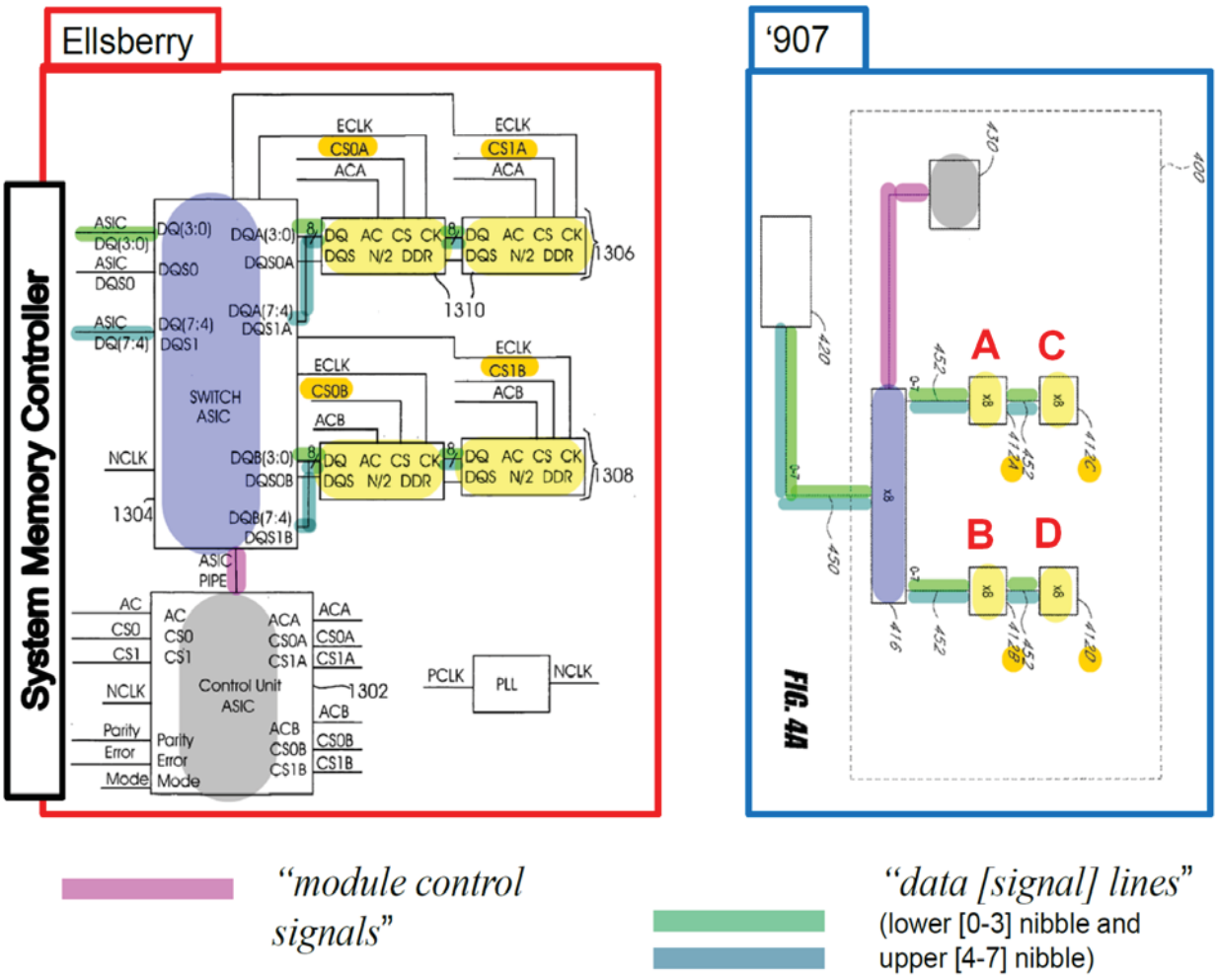
The phrase "*the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command*" appears in independent claims 1, 16, and 53. Independent claim 30 has a similar phrase: "*first memory devices … receiving each N-bit wide data signal associated with the first write command, and second memory devices … receiving each N-bit wide data signal associated with the second write command*." The broadest reasonable construction of these phrases is not limited to a single rank outputting or receiving data associated with a read or write command. Ex.1003¶¶135-136.

The claim language above does not require that the "*memory devices*" be in a single rank. It only requires that the "*memory devices*" together "*output or receive each N-bit wide data signal associated with the memory read or write command*." The 907 Patent specification does not limit the targets of a memory access to a single rank either. Ex.1001 at 14:62-15:12,17:67-18:2. Therefore, "*memory devices*" in the claim language above should not be limited to a single rank. Ex.1003¶136.

3. "Fork-in-the-road" vs. "Straight-line" Interpretation

As discussed above, the 907 Patent discloses a "fork-in-the-road" arrangement where, for a given memory access, memory device(s) on one data

path (e.g., path A) are coupled to a common data bus leading to the system memory controller, and other memory device(s) on a different data path (or different "fork" of the road) (e.g., path B) are isolated from that common data bus. Ex.1003¶126. In parallel litigation, however, Patent Owner alleges that the claimed "first" and "second" memory devices are on the ***same*** data path. Ex.1003¶127; *see also* Ex.1034 at 36; Ex.1003¶¶88,91-94,110,112. As depicted in the annotated figure below, under this "straight-line" arrangement, if A is the "first" memory device, then the "second" memory device would be C, rather than B. *Id.* Petitioner believes that interpretation is incorrect, *see* Ex.1003¶¶128-134, but the Board need not resolve this potential claim construction dispute because this Petition shows that the 907 Patent claims are unpatentable over Ellsberry under either the "fork-in-the-road" or "straight-line" interpretation, *id.* ¶128.



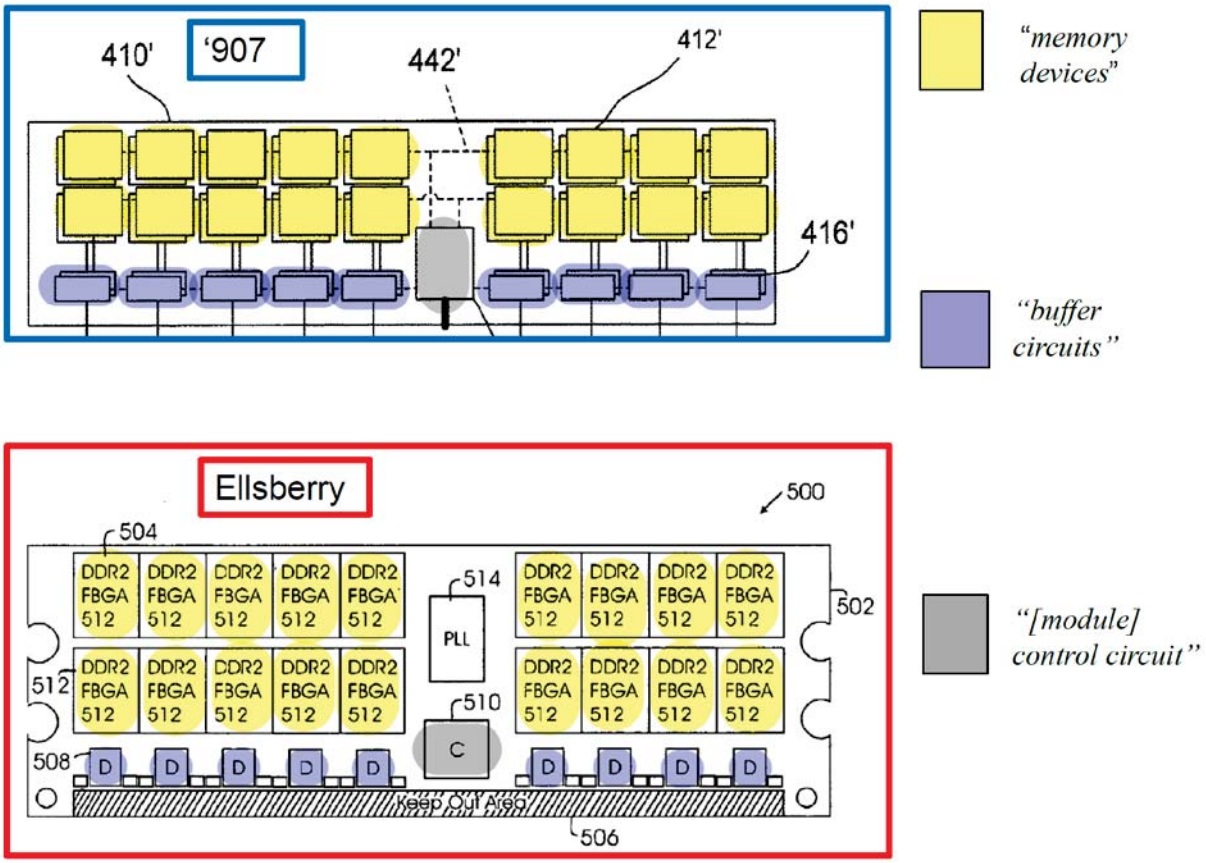
VI. Overview of the Prior Art

A. U.S. Pat. Appl. Pub. No. 2006/0277355 by Ellsberry et al. ("Ellsberry") (Ex.1005)

Ellsberry was published on December 7, 2006. Ex.1005, Cover. Ellsberry is prior art to the 907 Patent pursuant to at least 35 U.S.C. §§102(a)&(b).

Like the 907 Patent, Ellsberry is directed to the problem of "expanding the total memory capacity of a system beyond the limits of the data bus used." Ex.1005¶[0006]. And like the 907 Patent, Ellsberry discloses that the solution is to

distribute data buffers (what Ellsberry calls "memory bank switches") along the bottom edge of the memory module. Ex.1001 Fig.3C; Ex.1005 Fig.5; Ex.1003¶155-156.



Like the 907 Patent, Ellsberry explains that "the ***load on the bus is not increased*** because the memory bank switches ***present a single load*** to the bus, ***not the load of the individual memory devices*** coupled thereto." Ex.1005¶[0012]; Ex.1003¶164.

Like the 907 Patent, each data buffer circuit in Ellsberry (i.e., "memory bank switch") is configured to switch between two data paths, with one data path

connected to one group of memory devices and the other data path connected to a different group of memory devices. Ex.1001 Fig.5; Ex.1005 Fig.4; Ex.1003¶161.

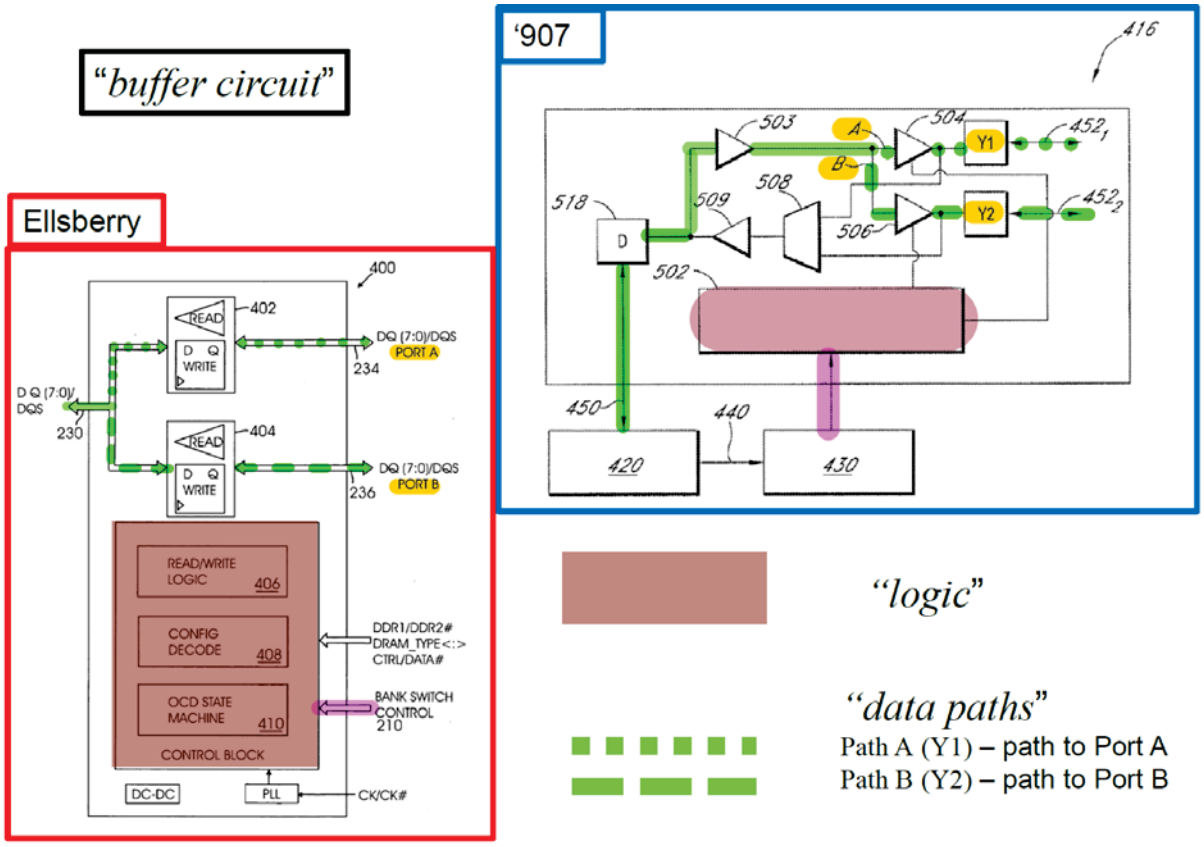


Figure 2 of Ellsberry summarizes the overall invention. Ex.1003¶163; *id.* ¶¶156-162. Each byte of data from the system memory controller is sent via data signal lines (230/232 in green) to a switch (206/208 in navy blue) which corresponds to the "buffer circuit" shown above. In response to signals (purple) from the module controller (204 in grey), the switches route the data through either port A along module data lines (e.g., 234 in green, shown below) to one group of memory devices (yellow), or through port B along module data lines (e.g., 236, not highlighted) to a different group of memory devices (yellow). *Id.* Thus, Ellsberry

discloses a "fork in the road" via its selection between the memory devices coupled to Port A versus Port B.

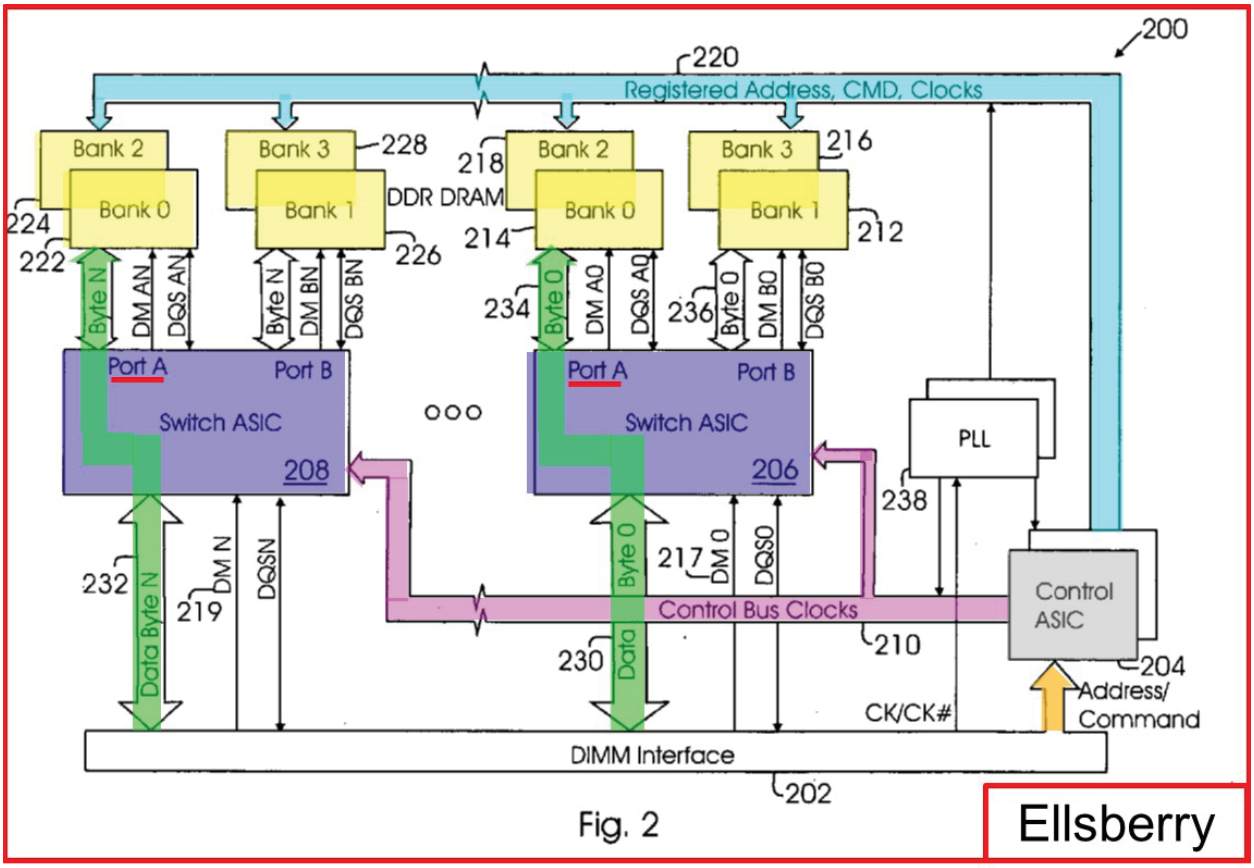


Figure 13 of Ellsberry (which corresponds to Figure 4A of the 907 Patent) provides a more detailed illustration of how the switch (navy blue) and memory devices (yellow) in Figures 2 and 5 could be arranged. Ex.1003¶¶143-148,157. In this "dual chip-select memory configuration" of FIG.13, the control unit 1302 (grey) receives two chip select signals CS0 and CS1 (orange) from the system controller, and generates four chip select signals (light blue), including chip select signals CS0A, CS1A for two respective memory devices 1306, and chip select

signals CS0B, CS1B for two other respective memory devices 1308. Ex.1005 ¶[0056], Fig.13; Ex.1003¶140. "This effectively expands the number of addressable banks per memory module without the need for additional chip select lines on the main memory bus." Ex.1005¶[0026]; Ex.1003¶138. Thus, Ellsberry also discloses the "straight line" interpretation of the 907 Patent where there are multiple memory devices on the same data path, with one enabled by a chip select signal and the other not.

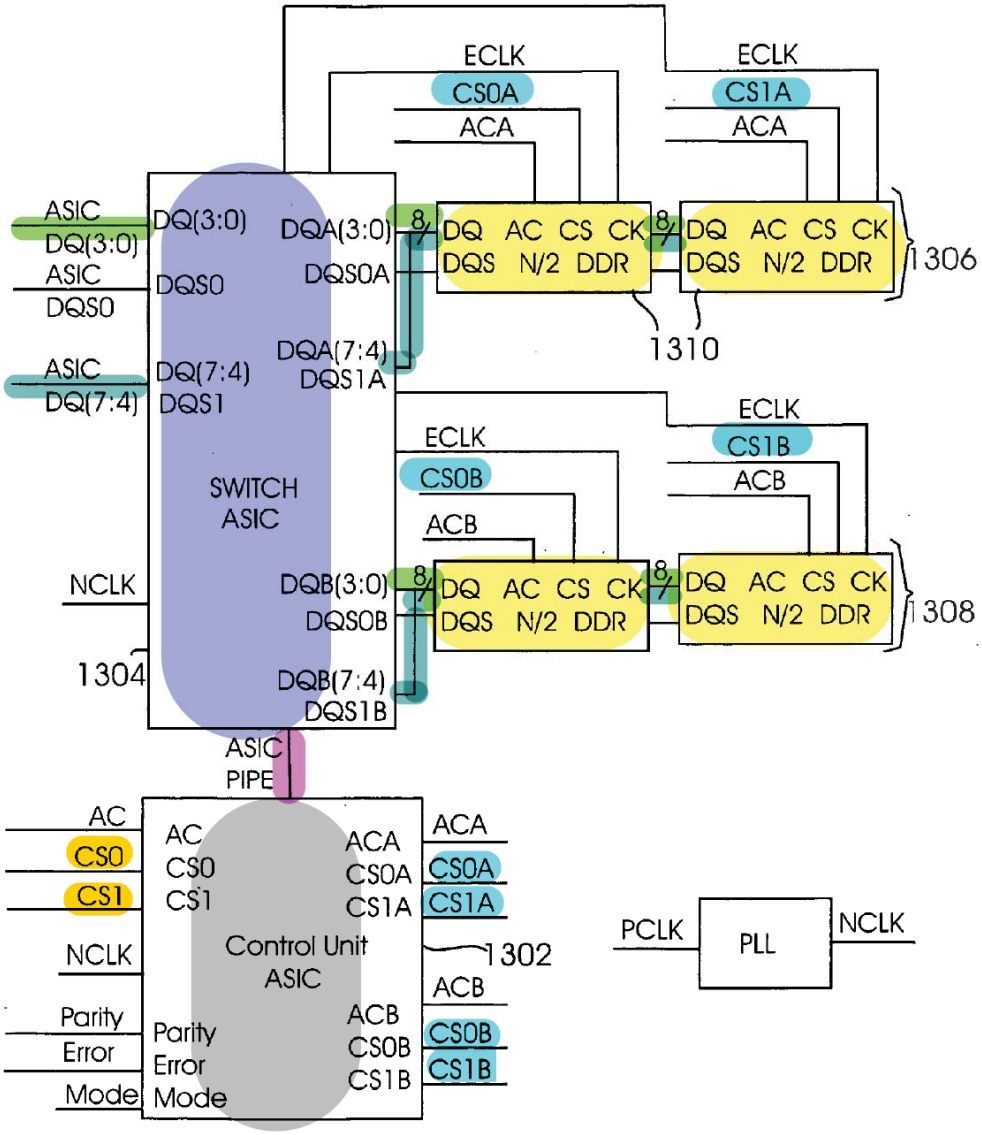
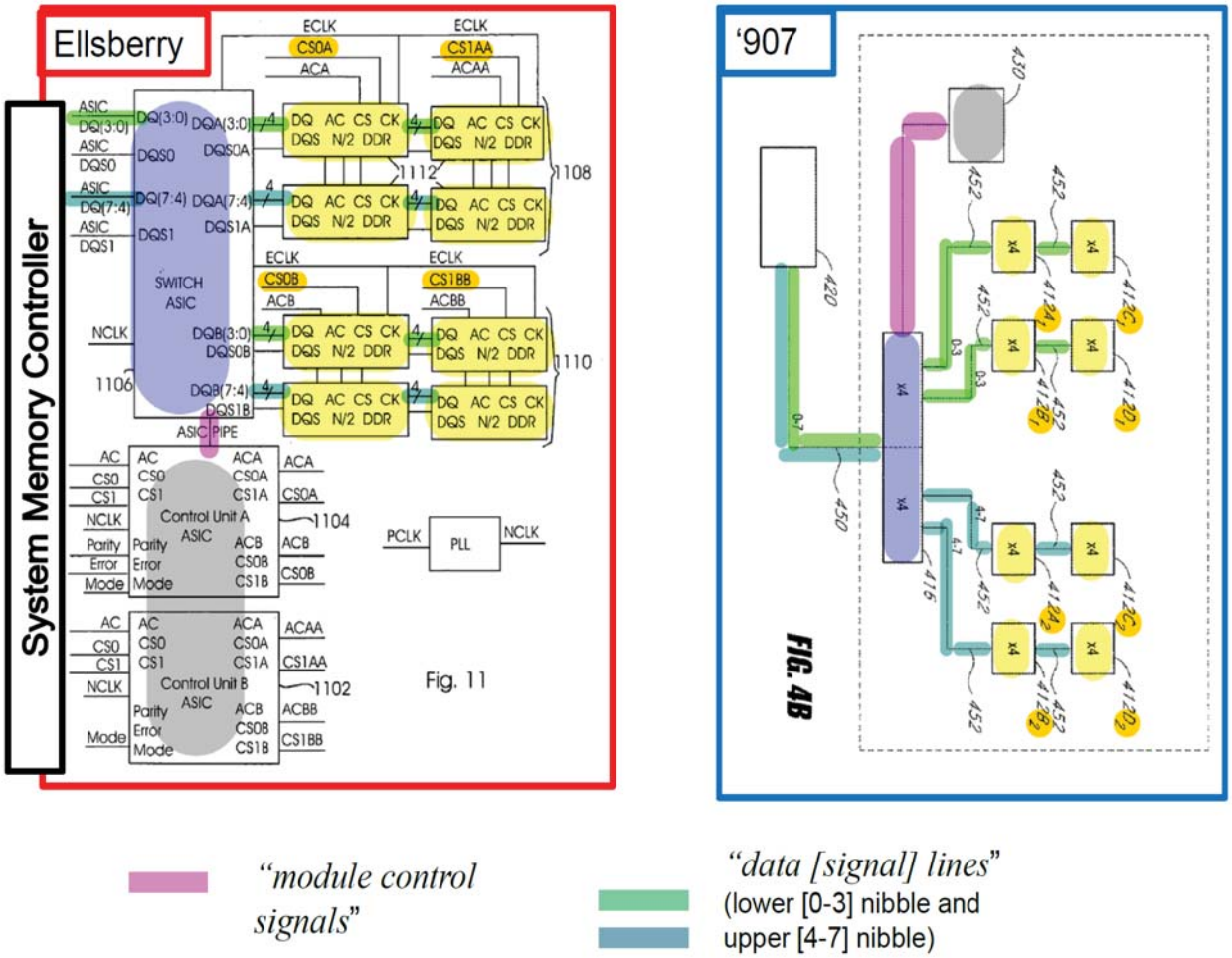


Fig. 13

Similarly, Figure 11 of Ellsberry (which corresponds to Figure 4B of the 907 Patent) provides a more detailed illustration of how the switch (navy blue) and memory devices (yellow) in Figures 2 and 6 could be arranged. Ex.1003¶¶149-152. Figure 11 is like Figure 13 except it replaces each 8-bit memory device with a pair of 4-bit memory devices, in the same way that Figure 4B of the 907 Patent

replaces each 8-bit memory device in Figure 4A with a pair of 4-bit memory devices. Ex.1003¶160.



B. JEDEC Standard No. 21-C ("JESD21-C") (Ex.1010)

JESD21-C is an industry standard for DDR SDRAM Dual In-Line Memory Modules (DIMMs). Ex.1010 at 5. JESD21-C was published in January 2002, *see* Ex.1012¶7, making it prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b).

C. U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (Ex.1006)

Halbert issued as a patent on April 4, 2006. Ex.1006, Cover. Halbert is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b).

Halbert discloses "a new memory module architecture" which can be used in "a typical memory system configuration," such as that shown in FIG.1 of Halbert. Ex.1006 at Abstract, 1:31-39; Ex.1003¶¶166-169. Halbert's modules improve on the prior art by "provid[ing] twice the data rate of the registered DIMM" and "also allow[ing] the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." *Id.*; Ex.1003¶170. Halbert's module 100 can be implemented to be "transparent to the memory system and to the memory devices… [which] allows for an embodiment that is compatible with an existing memory controller/bus and with existing memory devices." Ex.1006 at 3:42-4:35,7:31-61, Figs.7-8; Ex.1003¶¶171-177.

D. U.S. Patent No. 7,334,150 to Ruckerbauer et al. ("Ruckerbauer") (Ex.1038)

Ruckerbauer issued as a patent on February 19, 2008. Ex.1038, Cover. Ruckerbauer is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b). Ruckerbauer discloses a memory module that includes a plurality of memory chips, bus signal lines, and a clock signal regeneration circuit and a register circuit connected to the bus signal lines. Ex.1038, Abstract. Ruckerbauer discloses that its

register circuit is mounted in the middle of a memory module such that, from the register, "command and address signals run via … signal lines … on the … memory module to the … memory chips … to the left and the right of the … memory module." Ex.1038 at 4:57-62, Figs.1-2.

E. Microcomputer Interfacing by H. Stone ("Stone") (Ex.1035)

Stone is a book published in 1982. Stone is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b). Stone describes, among other things, various techniques and issues related to interfacing different components of a computer system. Chapter 4 of Stone is specifically directed to such issues as they relate to accessing computer memories, including the use of bidirectional buffers. Ex.1035 at 133, Fig.4.7.

VII. Precise Reasons for Relief Requested

A. Claims 1-29 and 58-65 are obvious over Ellsberry (Ex.1005)

The numbering of the claim limitations below corresponds to that set forth in **Attachment C**.

As explained above in §VI.A, Figures 2, 5, and 13 of Ellsberry disclose a single embodiment (corresponding to Figure 4A of the 907 Patent) which uses 8-bit memory devices, while Figures 2, 6, and 11 of Ellsberry disclose another embodiment (corresponding to Figure 4B of the 907 Patent) which instead uses pairs of 4-bit memory devices. Ex.1003¶¶144-152. As demonstrated below, all claims of the 907 Patent are unpatentable over either of these embodiments, except

the dependent claims directed to 8-bit memory devices (claims 11,26,64) are obvious in light of the first embodiment (corresponding to Figure 4A of the 907 Patent), and the dependent claims directed to pairs of 4-bit memory devices (claims 6,12,15,27,29,63,65) are obvious in light of the second embodiment (corresponding to Figure 4B of the 907 Patent).

To the extent one might argue that the disclosure relating to either of these sets of claims do not relate to the same embodiment, it would have been obvious to combine those disclosures because their inclusion in the same patent application would have motivated a Skilled Artisan to consider them together and also because Ellsberry specifically relates them to each other. Ex.1005¶[0049] ("a memory controller 510 is a control unit 204 and the memory bank switches 508 are memory bank switches 206 as described above."), ¶[0052] ("FIGS. 10, 11, 12 and 13 illustrate different configurations …[which] employ the control unit and bank switch previously described."). Furthermore, using this correspondence between the different figures to implement the modules of Ellsberry would have been a combination of known elements where each element operates as it would in the prior art, providing predictable and reliable results. Ex.1003¶¶151-152.

1. Claim 1

*a) **[1.a]:** "A memory module …"*

Ellsberry discloses a "*memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n.*" Ex.1003¶¶186-196. Ellsberry discloses a computing system 100 including a "processing unit 102" and "memory module 106," as shown in Figure 1. Ex.1005¶[0027], Fig.1.

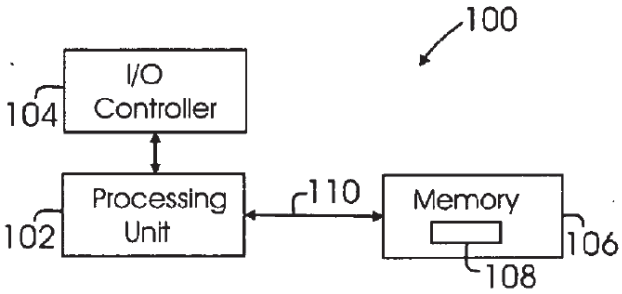


Fig. 1

Ellsberry explains that the "term 'memory module' refers to any package in which one or more memory devices are mounted (e.g., DIMM, SIMM, etc.)." *Id*. ¶[0023]. Ellsberry therefore discloses a "*memory module.*" Ex.1003¶188.

Ellsberry also discloses a "*memory controller*," such as the "processing unit 102." Ex.1003¶189; Ex.1005¶¶[0011],[0027],[0026].

Ellsberry further discloses that the "*memory module*" is "*configured to communicate with a memory controller"* through the communication path 110. Ex.1005¶[0027] (describing "communication path 110 to and/or from the memory

module 106"); Ex.1003¶¶190-192. A block diagram of Ellsberry's "capacity-expanding memory device" is disclosed in Figure 2 set forth below, showing a DIMM interface "coupled to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." Ex.1005¶¶[0028],[0011]. Such communication was well known standardized technique at the time. Ex.1010 at 6.

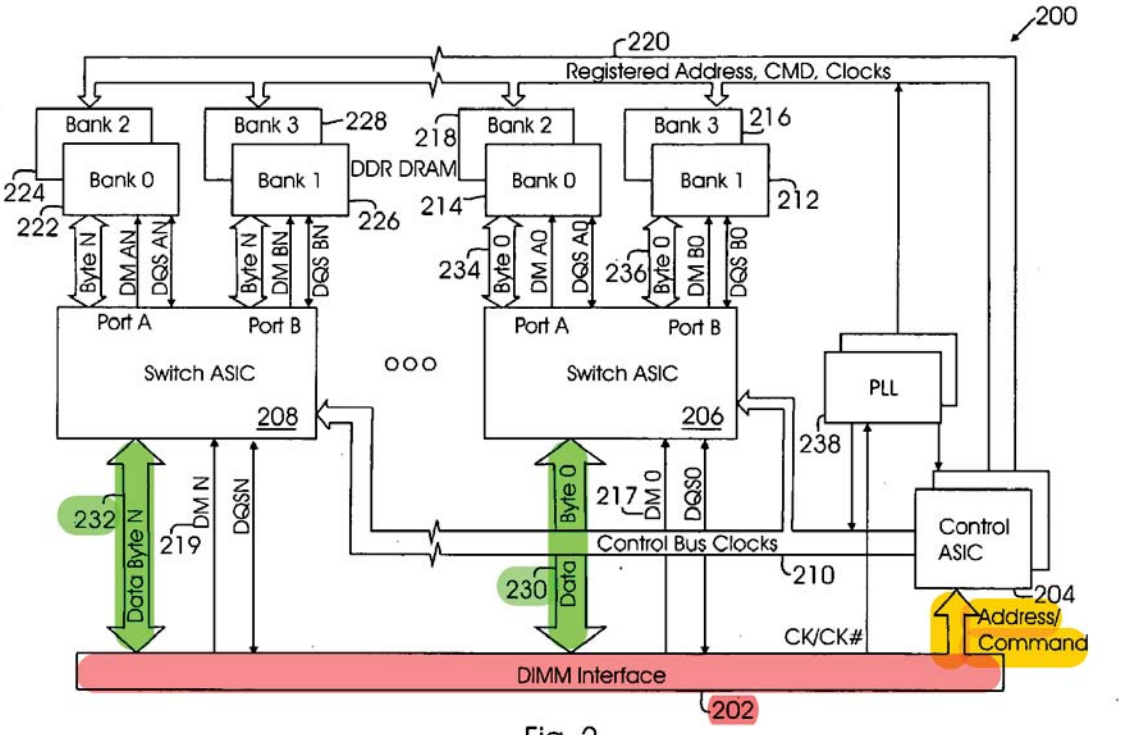


Fig. 2

Ellsberry further discloses that the memory module communicates with the memory controller "*via a set of control signal lines.*" Ex.1003¶193. Ellsberry's Address/Command signals are communicated through "*control signal lines*" in the DIMM interface 202. Ex.1005¶¶[0028],[0029] and Fig.2 (reproduced above, with

annotations showing DIMM interface in red and "*control signal lines*" in orange). Ellsberry also discloses that its memory module has "a data width" (disclosing "*a width of N bits").* Ex.1003¶194, Ex.1005¶[0034].

In Fig.2, Ellsberry also discloses "*M sets of data lines*" in the DIMM interface 202 which has "two sets of data bits" in the data buses 230-232 (annotated green) and those data bits are used together to provide "a range of data bits simultaneously." Ex.1005¶¶[0029]-[0030] and annotated Fig.2 above; Ex.1003¶195. Each of the data buses 230 and 232 includes respective data lines to transmit an entire data byte (Data Byte 0; Data Byte N). Thus, Ellsberry discloses that each group of data bits is carried on a "*set of n data lines*" where "*n*" is eight. In Ellsberry, each of the multiple data groups provides a corresponding byte, *i.e.*, eight bits ('*n*'), of data (thereby disclosing *"M sets of n data lines, where M is greater than one and N=M×n*"). Ex.1005 at Fig.2. Figures 5 and 6 of Ellsberry (like Figure 3C of the 907 Patent) show that M can be 9, as discussed below, in which case N would be 72 (i.e., 9x8).

b) [1.b]: *"a module control circuit …"*

Ellsberry discloses a "*module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to*

produce first module control signals and second module control signals in response to the set of input address and control signals." Ex.1003¶¶197-211.

Ellsberry discloses in Fig.2 a control unit 204 ("*module control circuit*") implemented as an Application Specific Integrated Circuit (ASIC), which "receives memory addresses and commands over the DIMM interface 202." Ex.1003¶198, Ex.1005¶[0029] and Fig.2 reproduced below with annotations showing the control unit 204 (grey), which receives the claimed input address and control signals (orange) through the DIMM interface 202 (red)).

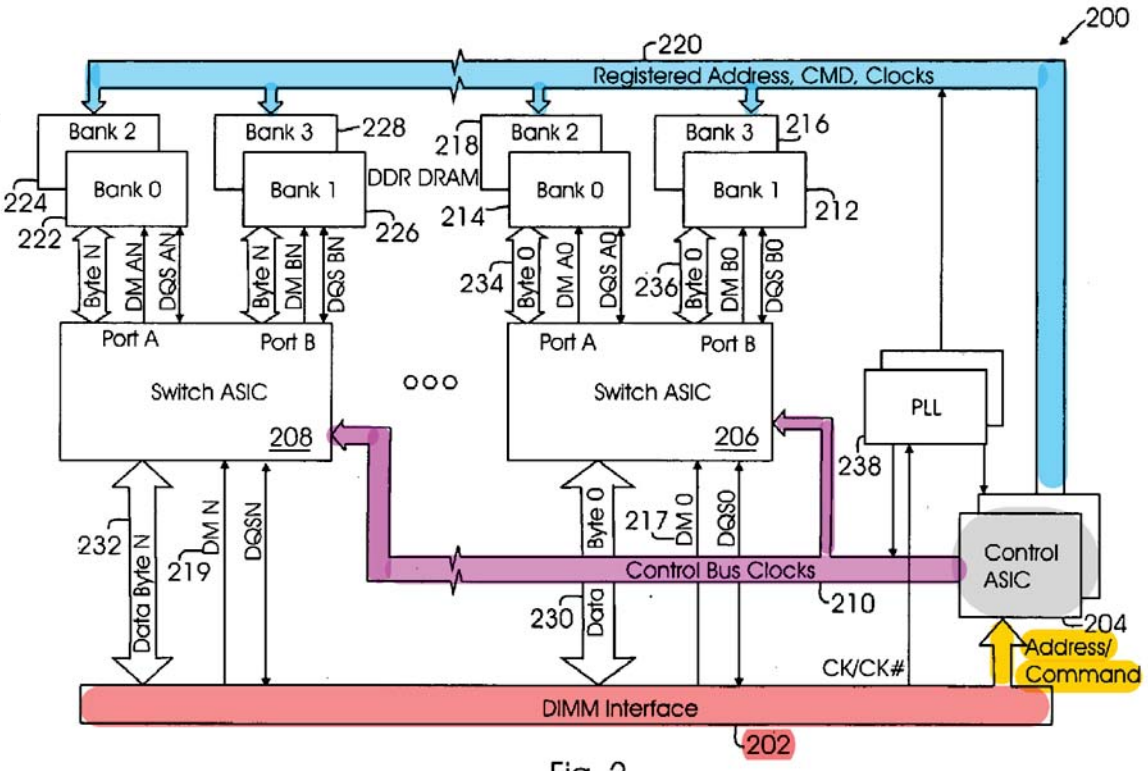


Fig. 2

A Skilled Artisan would have understood that the "Address/Command" signals received by control unit 204 can correspond to memory read or write

commands and are the claimed "*input address and control signals"* received "*via the set of control signal lines*" of limitation [1.a] in the DIMM interface, together forming the claimed "*set of input address and control signals*." Ex.1003¶199*;* Ex.1005 at Abstract, ¶[0045],Fig.8A. The DIMM interface is coupled to a "*memory controller*," such as a processor, which sends the addresses and commands to the control unit through that interface. Ex.1005¶¶[0029],[0036],Fig.2. Thus, Ellsberry discloses that the control unit 204 is "*configured to receive a set of input address and control signals … from the memory controller via the set of control signal lines*." *Id*.; Ex.1003¶¶199-201.

In response to those "Address/Command" signals, the control unit 204 controls elements of the memory module, and is therefore the claimed "*module control circuit*." Ex.1003¶200. The control unit 204 in Ellsberry "indicates to the memory bank switches 206 & 208 how data … should be received and/or stored," and "directs data to a particular memory bank based on … the address received." Ex.1005¶¶[0029],[0036].

Ellsberry further discloses that the "*input … signals*" correspond to "*a memory read or write command.*" Ex.1003¶¶202-205. Ellsberry states that the "control unit …[is] mounted on a memory module … to selectively control *write and read operations* to/from memory devices … A state machine is used to send *Read/Write commands* to the intended memory bank while sending no-operation

commands to the other memory bank." Ex.1005¶[0010], Fig.8A reproduced below with annotations; Ex.1003¶¶202,203; Ex.1005¶¶[0003],[0011]; Ex.1010 at 6, Ex.1009 at 17, 26. Ellsberry also discloses that the input commands include RAS_n, CAS_n, CS (chip select), WE_n, and A(10) signals, Ex.1005 at Fig.8B, which were known, standardized signals corresponding to read and write commands. Ex.1009 at 13.

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

ⓐ ⓑ ⓒ ⓓ ⓔ ⓕ ⓖ ⓗ ⓘ

Fig. 8A

Ellsberry also discloses that the "*module control circuit*" produces "*first*" and "*second module control signals*" in response to the "*input … signals.*" Ex.1003¶¶206-211. Ellsberry's Fig.2 is reproduced above with annotations to show the bus 220 (light blue) for transmitting the "*first module control signals*" to the memory devices and the control bus 210 (purple) for transmitting the "*second module control signals*" to the bank switches 206-208. Ex.1003¶206.

The bus 220 (light blue) carries address and command (CMD) signals (the claimed "*first module control signals*") which control the memory devices of the memory module. Ex.1003¶207. Ellsberry also discloses more detailed examples of the control unit 204 producing command and address signals for the memories in Figures 3&10-13. *Id.*; Ex.1005¶¶[0039],[0052]; *see also* Ex.1003¶¶138-152; Ex.1005 Fig.13 (control unit 1302 outputting chip select signals CS0A, CS1A, CS0B, and CS1B (light blue) and address and command signals ACA and ACB (dark blue) that are transmitted to the memory devices in banks 1306 and 1308); *id.* Figs.3,10-12,¶[0039].

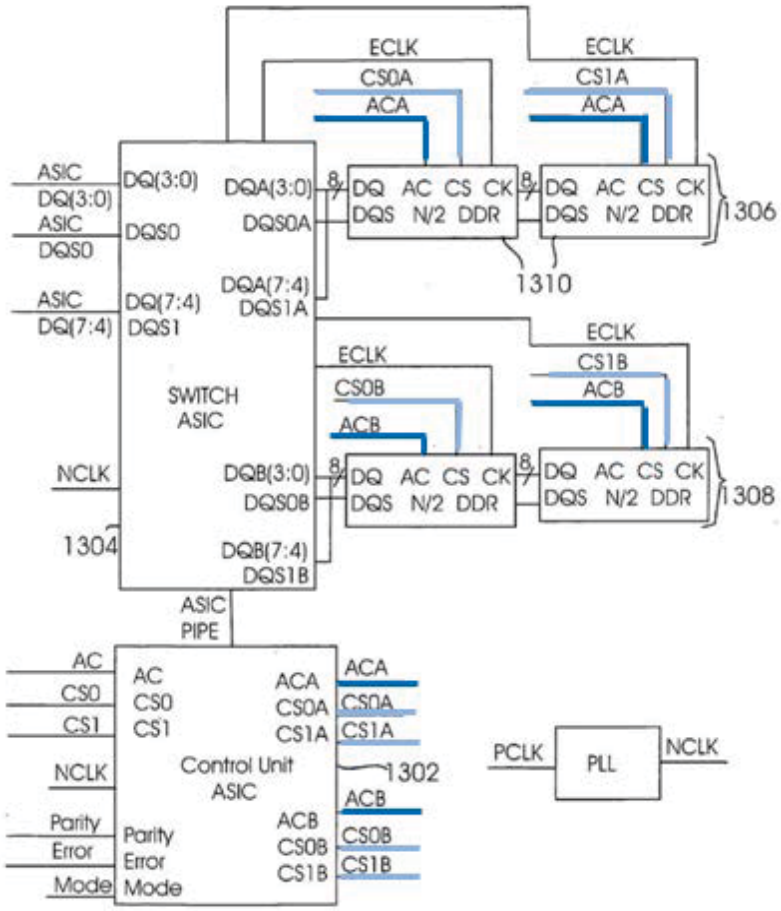


Fig. 13

Ellsberry explains that its "invention expands the addressable memory capacity on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device." Ex.1005¶[0010]; Ex.1003¶208. The "control unit maps a received logical address to a physical address …[and] directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)." Ex.1005¶¶[0011],[0033],[0041]. Such commands to the memory banks are

indicated by light blue in the annotated Fig.8A above, which also shows that these commands were produced in response to the received read or write command (annotated orange). Ex.1005¶[0042], Fig.13. Accordingly, Ellsberry's control unit (the claimed "*module control circuit*") is "*configured … to produce first module control signals … in response to the set of input address and control signals."* Ex.1003¶¶206-209.

Ellsberry also discloses that the control unit is "*configured … to produce …second module control signals in response to the set of input address and control signals.*" Ex.1003¶210. Ellsberry explains that "the control unit 204 decodes a memory address received over the DIMM interface 202, … *and causes the memory bank switch 206 and 208 to activate the correct memory bank*." Ex.1005¶[0031]; *see also id*.¶¶[0029],[0039],Fig.13; Ex.1003¶¶138-152. Thus, the control unit produces "*second module control signals*" in response to the received address and command signals (the claimed "*input address and control signals*") and provides them to the bank switches. *Id*.; Ex.1003¶210.

***c) [1.c]:** "a plurality of memory devices …"*

Ellsberry discloses "*a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated*

with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command." Ex.1003¶¶212-224.

Ellsberry discloses "*a plurality memory devices coupled to the module control circuit*." Ex.1003¶¶212-214. Ellsberry's memory module includes banks of "memory devices," such as DRAM and SDRAM devices, mounted on the circuit board of the memory module. Ex.1005¶¶[0003],[0026],[0032],Fig.2; Ex.1003¶213. Ellsberry also discloses that the address and command bus 220 couples the "*plurality of memory devices … to the module control circuit,"* which is the control unit (ASIC 204). Ex.1003¶214; Ex.1005 at Figs.3,10-13.

Ellsberry further discloses that the coupled "*memory devices*" include "*first memory devices*" which receive or output data in response to a memory write or read command, while other memory devices ("*second memory devices*") do not. Ex.1003¶¶215-223. In Ellsberry's invention, the "control unit … directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)." Ex.1005¶¶[0011],[0031],Fig.2 (activating Bank 1 out of Banks 0-3). The control unit also causes the bank switches to activate the port to which the targeted memory device is coupled and not activate the other port. Ex.1003¶¶216-217. In "row/bank" mode, read and write commands are sent only to the targeted memory device which outputs or

receives data in response to that read or write command. Ex.1005¶[0033]. Accordingly, Ellsberry discloses "*first memory devices …, wherein, in response to the first module control signals, the first memory devices output or receive … data signal associated with the memory read or write command*." Ex.1003¶218.

Ellsberry also discloses that each of the multiple (M) "Data Group 0 through Data Group N" outputs or receives one byte (n=8 bits) simultaneously to provide the full bit width (M×n) of the module. Ex.1005¶¶[0029]-[0030], and annotated Fig.2 above. Thus, Ellsberry discloses that "*the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command*." Ex.1003¶219.

A Skilled Artisan would also have understood that the memory devices receiving a "NOP (no-operation)" command do not access any data associated with the read or write command because those commands are not registered in those memory devices. *See, e.g.*, Ex.1009 at p. 14 ("The NO OPERATION (NOP) command … prevents unwanted commands from being registered."); Ex.1003¶220. Therefore, Ellsberry discloses "*memory devices [which] do not …[access] any data associated with the memory read or write command."* Ex.1003¶220.

Ellsberry's FIG.2 discloses Banks 1 and 3 on a data bus 236 and Banks 0 and 2 on another data bus 234, where a write operation can write data into Bank 1

("*first memory devices*") on enabled data bus 236, while the other data bus 234 is disabled. Ex.1005¶¶[0030],[0031],Fig.2, Fig.13; Ex.1003¶¶138-152. Thus, whether the "*second memory devices*" are those (in Bank 3) which share a data bus with the "*first memory devices*" (in Bank 1) as Patent Owner apparently contends, or the "*second memory devices*" are coupled to a disabled bus (Banks 0 and 2) as the proper construction requires, Ellsberry discloses the claimed "*second memory devices.*" Ex.1003¶222.

d) [1.d]: *"M buffer circuits …"*

Ellsberry discloses "*M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines.*" Ex.1003¶¶225-239.

Ellsberry discloses "*M buffer circuits*" that receive "*second module control signals*." Ex.1003¶¶226-229. Ellsberry discloses a memory module with multiple memory bank switches ("*M buffer circuits*"), one bank switch for each data byte of the DIMM interface. Ex.1005¶¶[0028]-[0030],[0047]-[0056], Figs.2,5,6,10-13; Ex.1003¶226. As demonstrated in Section b) with reference to the "*second module control signals*," *see* Ex.1003¶210, Ellsberry discloses that each of the bank

switches is "*configured to receive the second module control signals from the module control circuit"* (control unit 204) through the control bus 210. Ex.1003¶227.

Ellsberry further discloses a "data processing system 400 … [which] may be implemented as part of the memory bank switch 206." Ex.1005¶[0045], Fig.4 (reproduced below with annotations). Here, the bank switch has a control block configured to receive the bank switch control signals 210 (purple) from the control unit of the module. *Id*.; *see also id*. at Fig.3 (showing the module control unit outputting bank switch control signals 210); Ex.1003¶228.

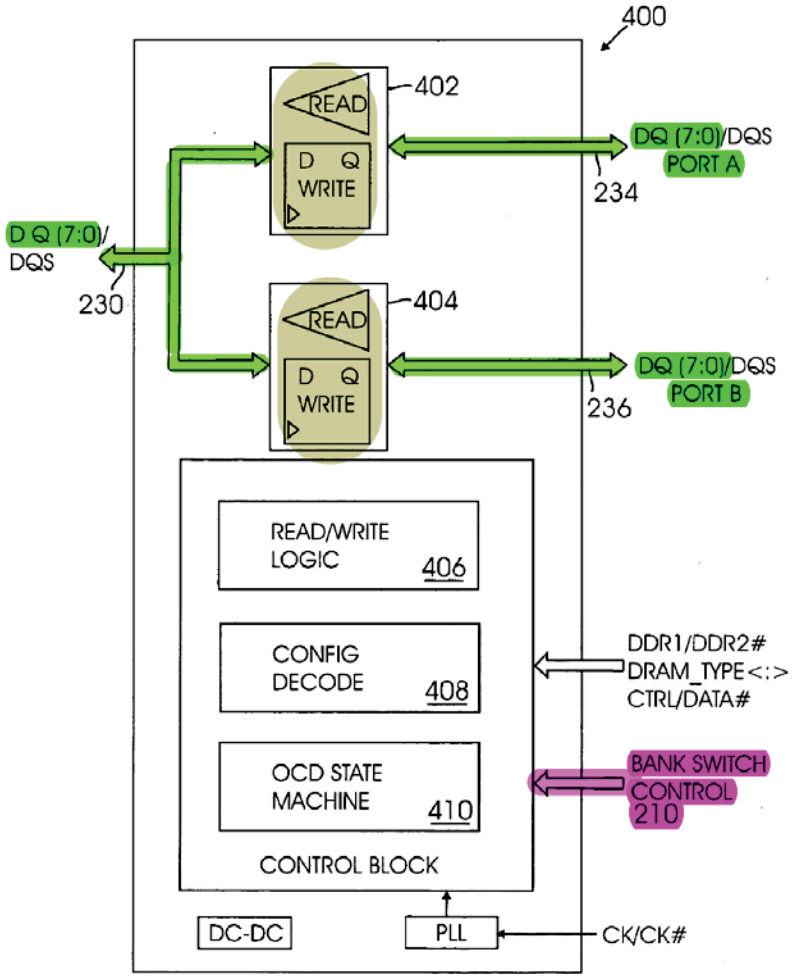
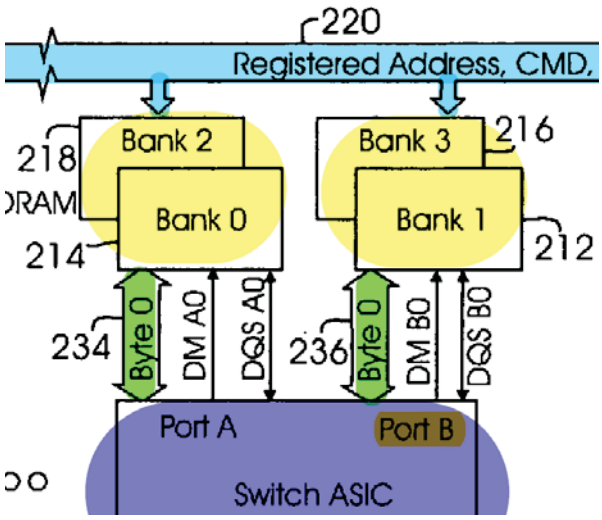


Fig. 4

Ellsberry further discloses that each of its "*buffer circuits*" is coupled to a set of "*n data lines*." Ex.1003¶¶230-231. In Fig.2, the data connection on the system side of the "memory bank switches 206 & 208" is through "the DIMM interface 202 via data buses 230 & 232, respectively." Ex.1005¶[0029]. Each of the data buses 230 and 232 includes "*a respective set of the M sets of n data lines*," where *n* is eight (carrying one byte of data). Ex.1005¶[0030]; Ex.1003¶230.

Ellsberry also discloses that each of its "*buffer circuits*" is coupled to a "*first memory device*" and a "*second memory device*" via the "*module data lines*." Ex.1003¶¶232-238. On the memory side in Ellsberry, each memory bank switch is coupled to two data buses 234 and 236, each leading to two banks, namely Banks 0 and 2 on bus 234 and Banks 1 and 3 on bus 236. Ex.1003¶232; Ex.1005¶[0030], Figs.2,4. As demonstrated in Section c), Ellsberry also discloses that the coupled memory devices include memory devices that output or receive data ("*first memory devices*") with respect to a read or write operation, and memory devices that do not access that data ("*second memory devices*"). Ex.1003¶¶215-223,233.

In Fig.2, each bank switch is coupled to four banks of memory devices, but only one of those banks, say Bank 1 ("*respective one or more of the first memory devices*") coupled to Port B of the bank switch through data bus 236 ("*n module data lines*"), participates in the data transfer associated with a write or read operation. Ex.1003¶234, Ex.1005¶¶[0030],[0031]. Here, the memory devices in Banks 0 and 2 coupled to the disabled Port A do not receive any data associated with the write command, and the memory devices in Bank 3 do not access the data targeted to Bank 1. Ex.1003¶¶235-237; Ex.1005 at Fig.2 (reproduced below in part).



e) [1.e]: *"… buffer circuit including logic …"*

Ellsberry discloses "*the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines*." Ex.1003¶¶240-246.

Ellsberry discloses a data processing system 400 that may be implemented as part of the memory bank switch 206 ("*each respective buffer circuit*"), and includes a Control Block ("*logic*") that responds to Bank Switch Control signals 210 (purple) (the claimed "*second module control signals*"). Ex.1005¶[0045], Figs.2,4 (below).

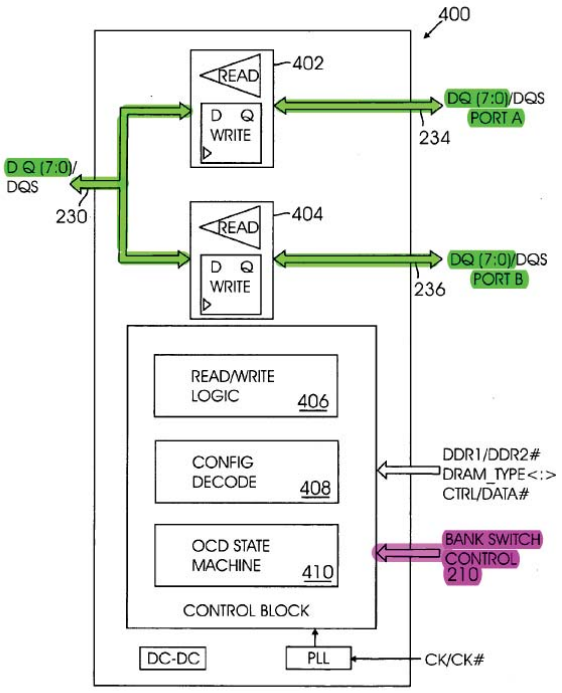


Fig. 4

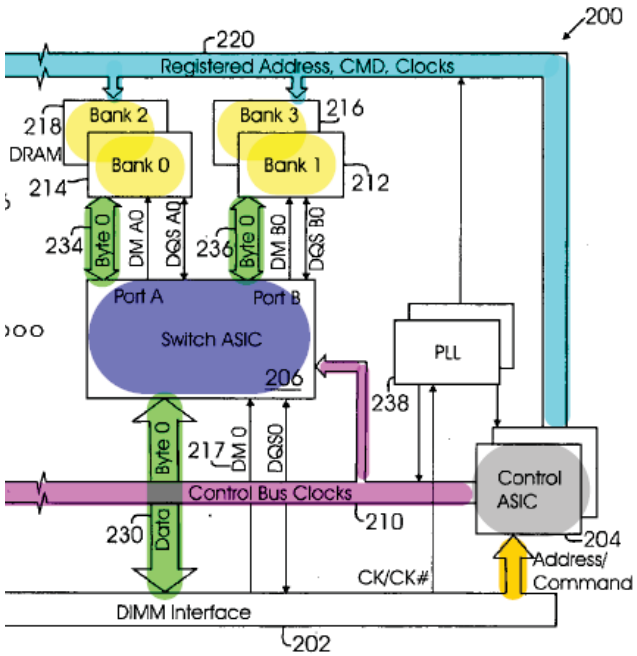


Fig. 2

Ellsberry further discloses that each bank switch allows "*communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines*." *Id*. (the data lines being annotated by green); Ex.1003¶242. In Ellsberry, "[d]ata is transmitted from the DIMM interface 202 via the data bus 230 to bidirectional signal drivers 402 & 404 that transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks." Ex.1005¶[0045]. Here, the data bus 230 carries an 8-bit section of the full bit width of the module ("*a respective n-bit section of the each N-bit wide data signal*") which is communicated through the DIMM interface including the data bus 230 ("*the*

respective set of the M sets of n data lines") between the system "*memory controller*" and the targeted memory devices ("*respective one or more of the first memory devices*"). Ex.1003¶242.

Further, Ellsberry discloses that the bank switch "*responds to the second module control signals by allowing communication*" through those data lines. Ellsberry states that the "memory bank switch is designed to receive data information … and direct the data information to a plurality of physical memory banks according to control signals from the control unit." Ex.1005¶¶[0011],[0030],[0039]; Ex.1003¶¶207,243. Ellsberry also states that the bank switch transmits that data through the data bus (in "*the set of n module data lines*") coupled to the targeted memory device. Ex.1003¶244; Ex.1005 [0031]. Thus, the bank switch is "selectively enabling or activating one of the two physical memory banks (e.g., either Port A or Port B) while disabling or deactivating the other." Ex.1005¶¶[0040],[0037], Figs.7A-F.

As discussed in Section d), Ellsberry discloses that this data communication happens "*via the set of n module data lines*" because the data bus to the targeted memory device is in the "*the set of n module data lines*" disclosed by Ellsberry. Ex.1003¶237. The bank switch is coupled to the respective Data Group carrying an eight ("*n*") bit wide data signal (DQ[7:0]), and allows the corresponding eight bits of data ("*n*"=*8*) to be communicated to or from one or more memory devices

in the selected bank (e.g., Bank 1) through the corresponding port (e.g., Port B), which is also eight ("*n*") bits wide. Ex.1005¶¶[0030-31],[0045], Figs.2,4; Ex.1003¶245.

f) [1.f]: *"… buffer circuits … configured to isolate memory device load …"*

Ellsberry discloses that each of its "*buffer circuits is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller*." Ex.1003¶¶247-250. Ellsberry explains that its memory module "presents a single load to the bus …, ***not the load of the individual memory devices*** coupled thereto." Ex.1005¶[0027]; *see also id*. [0012]. The load of the memory devices is not "presented" to the system bus because that load is electrically separated from the system bus. Ex.1003¶248. The memory device load is isolated in Ellsberry because bidirectional drivers electrically separate the load of the memory devices from the system bus. Ex.1003¶249; Ex.1005¶[0031],[0045]; Ex.1035 at 68,74-75,133, Figs.2.28,4.7. Because the memory devices coupled to the bank switch include both "first" and "second" memory devices, the "*load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices [is isolated] from the memory controller*." Ex.1003¶249.

g) [1.g]: *"a printed circuit board (PCB) …"*

Ellsberry renders obvious "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines*." Ex.1003¶¶252-263.

Ellsberry discloses a "*PCB*" having an "*edge connector*." Ex.1003¶¶252-255. Ellsberry discloses a module on a PCB with an edge interface 506 ("*edge connector*") in Figure 5 which corresponds to the module shown in Figure 2. Ex.1005¶[0047]; Ex.1003¶¶252-253 (explaining the correspondence between the circuit elements in Figs.2 & 5).

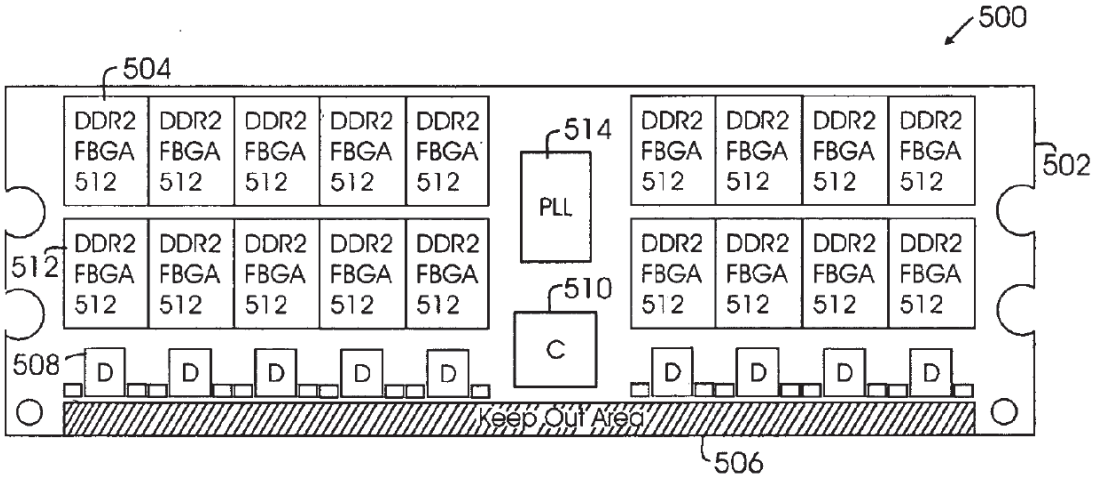


Fig. 5

The memory module of Figure 5 "includes a substrate 502 on which a plurality of memory devices 504 are mounted," Ex.1005¶[0047], from which a Skilled Artisan would have understood that the substrate as depicted in Figure 5 is *"a printed circuit board (PCB)*" because various circuits are mounted on it and because Figure 5 depicts the typical shape of a printed circuit board used as a SIMM or DIMM. Ex.1005¶[0002]; Ex.1010 at 29, 66. That PCB substrate 502 "includes an edge interface 506 that serves to communicatively couple the memory module 500 to a memory slot or to a communication bus (e.g., memory bus, etc.)." Ex.1005¶[0047]. The "edge interface" 506 is therefore *"an edge connector positioned on an edge of the PCB.*" Ex.1003¶¶254-255.

Ellsberry further discloses that its "*edge connector*" is configured to be "*releasably coupled*" to the "*contacts of a computer system socket*." Ex.1003¶¶256-260. Ellsberry explains that the edge interface 506 "serves to

communicatively couple the memory module 500 to a memory slot" through electric signals thereby disclosing that that interface is *"releasably coupled to corresponding contacts of a computer system socket*" and has "*electrical contacts configured … to provide electrical conductivity."* Ex.1003¶¶256-257, Ex.1005¶[0047].

Indeed, a Skilled Artisan would have been familiar with the existing standards for DIMM modules and corresponding sockets and electrical contacts (e.g., JESD21-C (Ex.1010)), and used that standardized technology in Ellsberry's module. Ex.1005¶¶[0050],[0002]; Ex.1010 at 6, 73; Ex.1006 at 2:3-14, Fig.1 (reproduced below), Fig.8. Therefore, a Skilled Artisan would have understood that Ellsberry's "*edge connector [is] comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity*." Ex1003¶¶258-260.

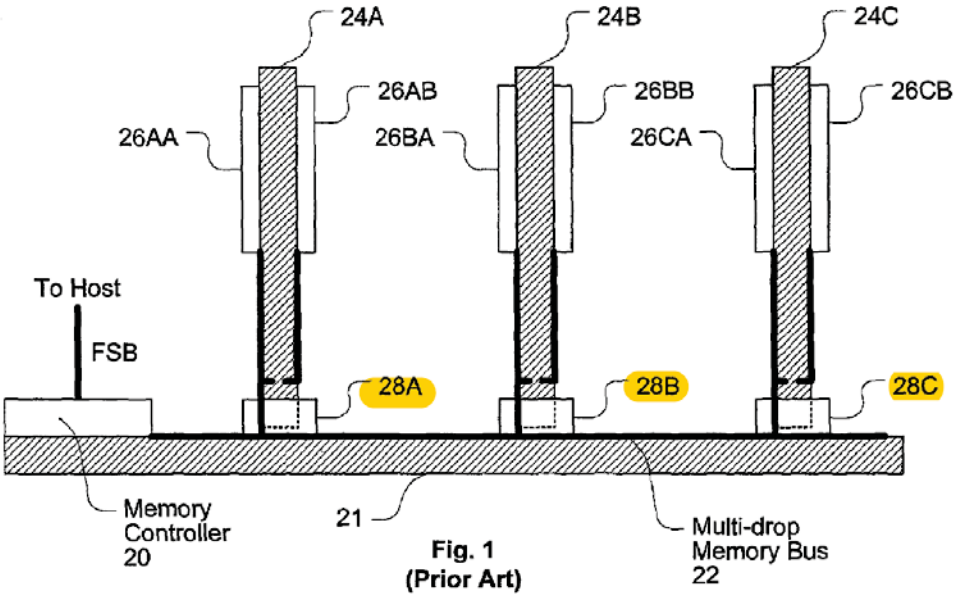


Fig. 1 (Prior Art)

Ellsberry further discloses that its "*edge connector*" provides "*electrical conductivity*" between the "*buffer circuits*" and the "*data lines*." Ex.1003¶¶261-263. Ellsberry explains that its module has nine memory bank switches 508 ("*buffer circuits*") that are "communicatively coupled to the edge interface 506 to pass signals between the edge interface 506 and the memory devices 504 &512," and each switch is coupled to a set of n data lines. Ex.1005¶¶[0047],[0050]; Ex.1003¶¶194-195, 230. Thus, Ellsberry discloses "*the edge connector comprising a plurality of electrical contacts configured … to provide electrical conductivity … between the M buffer circuits and the M sets of n data lines*." Ex.1003¶¶261-263.

h) [1.h]: *"… buffer circuits are mounted … at corresponding positions …"*

Ellsberry discloses that its "*M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices*." Ex.1003¶¶271-279. The module of Figure 5 (shown below) has nine bank switches 508 ("*M buffer circuits*"; purple) mounted on a PCB between the memory devices of memory banks 504 and 512 (yellow), on the one hand, and edge interface 506 (red), on the other. The bank switches 508 are distributed along the edge interface horizontally at uniformly spaced positions separate from one another, directly below the corresponding memory devices. Ex.1005 at Fig.5; Ex.1003¶272.

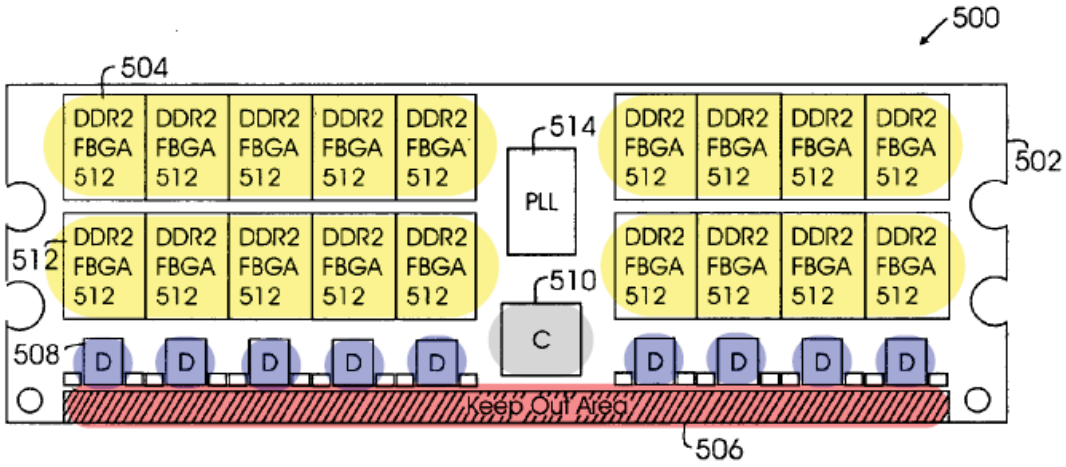


Fig. 5

Ellsberry therefore discloses "*wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other.*" Ex.1003¶¶272-273.

In Figure 5, the bank switches 508 may route data to and from the memory devices 504 and 512. Ex.1005¶¶[0047-48], Fig.5. A Skilled Artisan would have understood that, according to Fig.2, the bank switch 508 is also coupled to two more memory devices at corresponding positions on the other side of the module. Ex.1003¶274. Because the memory devices coupled to each bank switch 508 include both "*first*" and "*second*" memory devices, each bank switch 508 is at a position which corresponds to "*the respective one or more of the first memory devices and the respective one or more of the second memory devices.*" Ex.1003¶275.

2. Claims 2, 4, 10, 21 and 22

Claims 2 and 22 require that the "*the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the [module] control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal*."

Ellsberry's Figures 11 and 13 disclose chip select signals that are also relevant to the embodiments of Figures 2 and 5. Ex.1005¶¶[0028],[0030],[0033],[0042],[0036]-[0039],[0047],[0052] (relating FIGS. 11 and 13 to control units and bank switches "previously described," like those in FIGS. 2 and 5), Fig.8B (disclosing that command signals include chip select signals); Ex.1003¶¶281-283. Thus, this limitation would have been at least obvious in view of Ellsberry.

In Figure 13 (below), Ellsberry "illustrates a dual chip-select memory configuration." Ex.1005¶[0056]; Ex.1003¶284. Here, the control unit 1302 receives two chip select signals CS0 and CS1 (orange, "*at least one first chip-select signal*") and outputs four chip select signals CS0A, CS1A, CS0B and CS1B (light blue, "*second chip-select signals*"). Ex.1003¶¶285-287;

Ex.1005¶¶[0011],[0029],[0031]-[0033],[0056],Fig.13; Ex.1011 at 6 (showing the label CS refers to chip select).

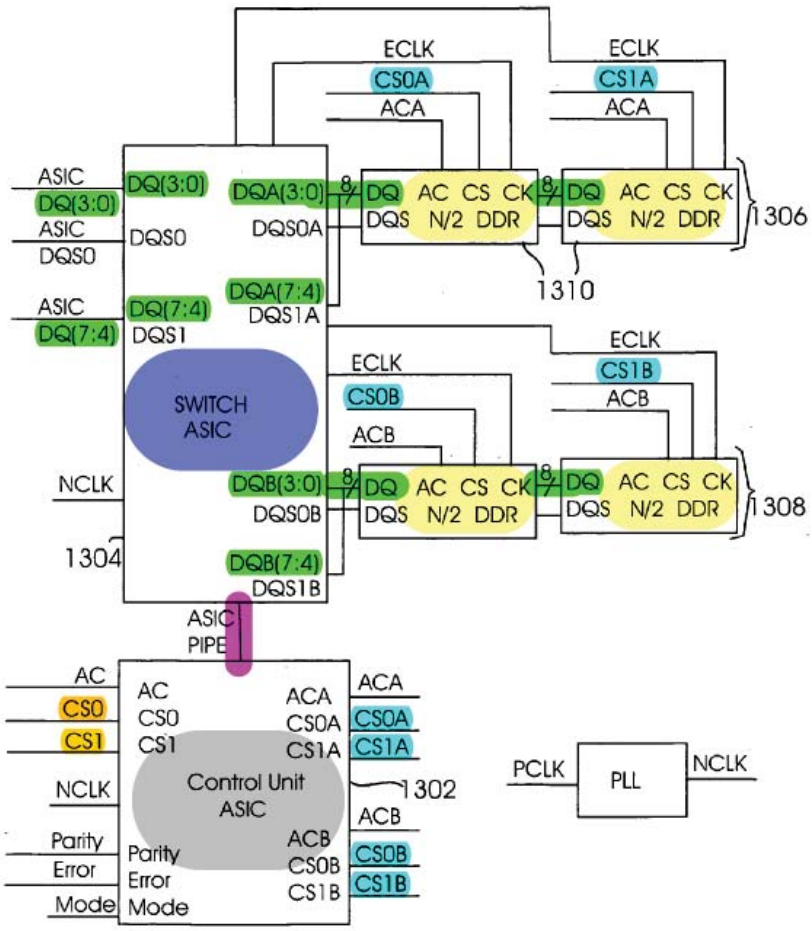


Fig. 13

When the chip-select functionality in Ellsberry's Figure 13 is combined with the bank selection functionality of Figures 2 and 5, the control unit of Figure 5 would include address translation functionality and chip-select multiplication functionality to provide an advantageous solution according to the needs of using existing memory buses and cheaper memory devices.

Ex.1005¶¶[0035],[0052],[0042], Fig.8B; Ex.1003¶¶288-290; Ex.1007 at Fig.5, [0043]. Ellsberry therefore renders claims 2 and 22 obvious.

Ellsberry also renders claims 4, 10 and 21 obvious for the reasons provided above with respect to claims 2 and 22, and because Ellsberry discloses that the "*first*" and "*second memory devices*" receive "*different chip select signals*." Ex.1003¶¶299-301,370-370,428-429. As discussed above with reference to Figures 2, 5, and 13, Ellsberry's module control unit generates four chip select signals, but only asserts one of those to activate the "*first memory devices.*" Ex.1005¶[0031], Fig.13. The memory devices not activated by a chip select include the "*second memory devices.*" *See* §1.c); Ex.1003¶¶222. Therefore, the "*first memory devices*" would receive an asserted chip select signal(s) and the "*second memory devices*" would receive other, non-asserted chip select signal(s). Ex.1003¶300.

3. Claims 3 and 61

Claims 3 and 61 require that "*the each respective buffer circuit is configured to present one memory device load on each [data line] of the respective set of … data lines [to the memory controller]*."

Ellsberry discloses that the load on data lines is a single load rather than that of several memory devices. Ex.1005 at [0027]; Ex. 1003¶293. Setting that device load to "*one memory device load*" would have been obvious because the bank switch of Ellsberry is intended to *emulate* a single higher-capacity logical memory

device and that choice would reduce the load and support known SDRAM specifications. Ex.1003¶¶294-297; Ex.1005¶¶[0010],[0031],[0046]; Ex.1011 at 65. Ellsberry explains that "each memory bank switch 206 and 208 includes ***signal drivers*** to drive data signals to and from the memory banks and to and from the DIMM interface 202. This ***reduces resistive and/or capacitive loading of the data bus*** … ***while emulating a standard memory device interface***." Ex.1005¶[0031]; Ex.1003¶295. A Skilled Artisan would have understood from this disclosure that, by emulating a standard memory device interface, the bank switch would also emulate the load of that standard memory device interface. Such a configuration would reduce the load on the bus because it presents a single memory device load that corresponds to the logical memory device it is emulating, instead of the two (or more) memory loads of the smaller capacity memory devices. Ex.1003¶295.

Ellsberry therefore renders claims 3 and 61 obvious. Ex.1003¶¶292-298,618-619.

4. Claims 5

Claim 5 requires that "*buffer circuit is configured to present a load to the respective one or more of the first memory devices that is the same as a load the memory controller would present*." Ex.1003¶¶302-310. As discussed above in Section 1.f), Ellsberry's bank switch presents the load of the bidirectional drivers 402&404 to the memory devices. Ex.1003¶304; Ex.1005¶[0045], Fig.4. It would

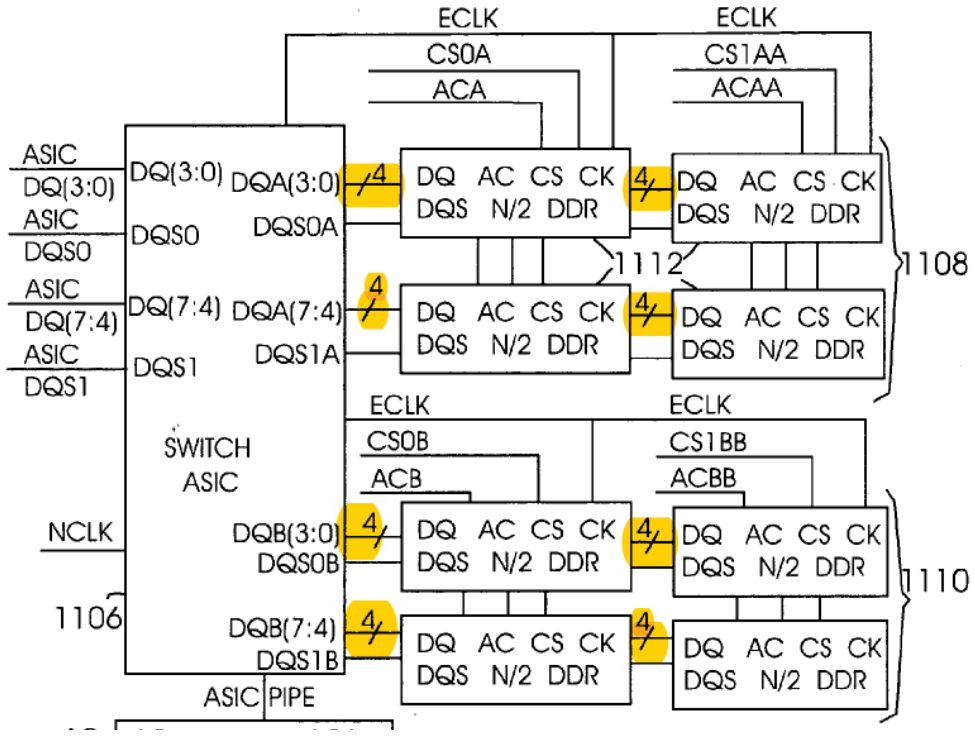
have been obvious to a Skilled Artisan to set that single load to be the same load which would be presented by the external memory controller in order to assure that the bank switch can properly interoperate with the memory devices and the signals would not be distorted. Ex.1003¶305; Ex.1005¶[0044]. In particular, Ellsberry's control unit has a "squelch function" which sets drivers in the memory devices to a "default" value, which corresponds to driving a predefined load, such as the load "*that is the same as a load the memory controller would present*," because such drivers are designed to ensure that the signals are properly received by the controller. Ex.1003¶¶306-308; Ex.1005¶[0044],Fig.9; Ex.1011 at 14-15. Configuring Ellsberry's control unit in this manner would have used well known elements that provide predictable results, since driving characteristics and corresponding loading were already standardized. Ex.1003¶308; Ex.1011 at pp. 14-15 (defining off-chip driver (OCD) "Default" values).

5. Claims 6, 15, 29 and 63

Claim 6 requires that the "*buffer circuit has a first data width of n bits, and wherein each of the plurality of memory devices has a second data width different from the first data width*."

As discussed above in Section 1.d), *see* Ex.1003¶¶226,230,232-235, Ellsberry discloses that "*each respective buffer circuit has a first data width of n bits*," such as eight bits (one byte). Ex.1003¶312; Ex.1005¶[0030],Fig.2.

Ellsberry's Figure 11, annotated below, illustrates such a "*buffer circuit*" in a configuration that includes memory devices having a data width of 4 bits ("*wherein each of the plurality of memory devices has a second data width different from the first data width.*"). Ex.1003¶313; *see also* Ex.1003¶¶314,315 (discussing Ellsberry's Fig.2 having the configuration of Fig.11); Ex.1005¶¶[0039],[0052]; Ex.1010 at 12, 15.



Ellsberry therefore discloses the requirements of claim 6. Ex.1003¶¶311-316.

Ellsberry discloses the requirements of claims 15, 29 and 63 for the reasons provided above with respect to claim 6 and because Ellsberry discloses that includes "*byte-wise buffer circuits*" and "*each set of … data signal lines is eight*

bits wide." Ex.1003¶¶391-392,444-445,622-623. In particular, each bank switch of Ellsberry transfers one byte at a time, and therefore each is a "*byte-wise buffer circuit.*" Ex.1005 at Fig.2; Ex.1003¶392.

6. Claims 7, 19 and 24

Claims 7, 19 and 24 require that the "*second module control signals indicate a direction of data flow through the buffer circuits*." The data flow through Ellsberry's bidirectional drivers 402 and 404 is controlled by a "read/write logic unit 406 [which] determines whether data is being read from or written to the memory devices." Ex.1003¶¶318; Ex.1005¶¶[0045],[0047],Fig.4 (reproduced below).

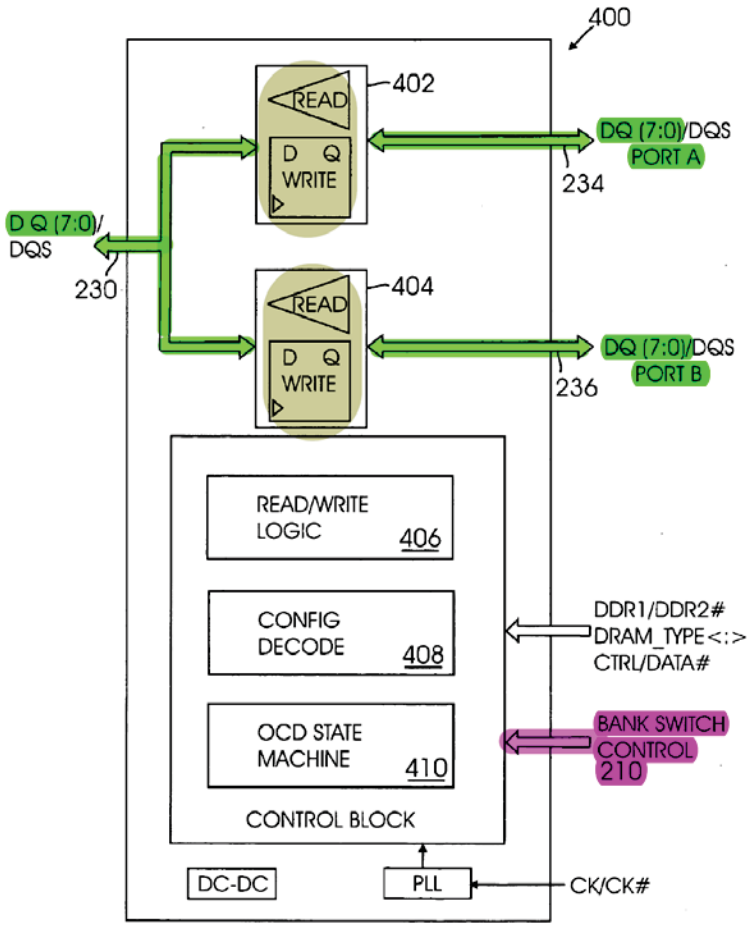


Fig. 4

Ellsberry's control unit 204 can include an "address and command processing system 300" which controls the direction of data flow in the bank switches. Ex.1003¶319, Ex.1005¶[0039],Fig.3. To implement that control from the control unit, "*the second module control signals*" would include a signal indicating the bank switching direction for the Read/Write logic in the bank switch. Ex.1005¶[0045],Fig.4. Thus, Ellsberry discloses using "*module control signals indicat[ing] a direction of data flow through the buffer circuits,*" a technique,

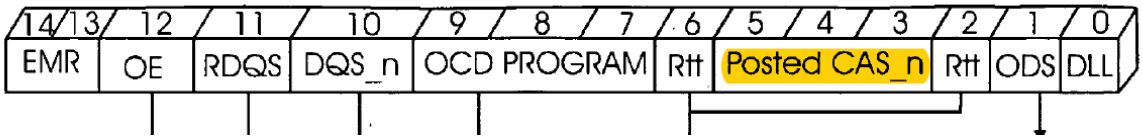
which was well known at the time. Ex.1003¶320; Ex.1035 at Fig.4.7; Ex.1006 at 5:23-39,Fig.4.

Ellsberry therefore discloses the limitations of claims 7, 19 and 24. Ex.1003 Ex.1003¶¶317-326,424-425,434-435.

7. Claims 8, 20 and 25

Claims 8, 20 and 25 require that the "[*module] control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the [second] module control signals in accordance with a latency parameter*."

Ellsberry's "*module control circuit*" is configured to control the bank switches via the control bus 210 ("*using the second module control signals*") to receive or output data at the DIMM interface 202 for a write or read command ("*N-bit wide data signal associated with the memory read or write command*"). Ex.1003¶328; Ex.1005¶¶[0010],[0029]. Ellsberry's control unit intercepts extended mode register commands including "*a latency parameter*," such as a "Posted CAS_n" parameter, also known as an "Additive latency" parameter, and uses such parameters for controlling the bank switches during read and write operations according to the timing of known standards. Ex.1003¶¶329-336; Ex.1005¶¶[0029],[0042],[0044],[0046],[0050],Fig.8A (listing MRS and EMRS),Fig.9 (below in part); Ex.1011 at p. 12, 22, 23.



To the extent one might argue that Ellsberry does not disclose this claim element, it would have been obvious to include the use of a "*latency parameter*" as claimed in the system of Ellsberry to emulate standard memory devices and assure the correct timing of the memory module in accordance with known standards, thereby avoiding transmission errors. Ex.1003¶¶338-341; Ex.1005¶¶[0029],[0031],[0046], Figs.3,4; Ex.1011 at 22; Ex.1009 at 8-10. As detailed above, Ellsberry's control unit ("*module control circuit*") intercepts mode register commands that include latency information that could be used to control the timing of memory accesses, and sends the intercepted commands to the bank switches. Ex.1003¶338. A Skilled Artisan would have been motivated to design the control unit to use that latency information to control the timing of memory accesses in order to comply with existing standards. Ex.1003¶335-336,338.

Ellsberry therefore renders claims 8, 20 and 25 obvious. Ex.1003¶¶327-342,426-427,436-437.

8. Claims 9, 13, 23, 28 and 59

Claims 9 and 28 require that the "[*module] control circuit comprises one or more integrated circuits having first input/output connections, second input/output*

connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections." Claims 13, 23 and 59 require "*module signal lines … coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets … of memory devices.*"

Ellsberry discloses that its "*module control circuit*" includes one or more "*integrated circuits having [multiple] connections*," such as application specific integrated circuits (ASICs). Ex.1003¶¶344-345; Ex.1005¶[0046],Fig.2. Ellsberry's control unit 204 provides both address and command signals, including RAS, CAS, WE and A(10) signals, to the memory devices through corresponding connections ("*module signal lines*"). Ex.1003¶345; Ex.1005¶¶[0030],[0042]-[0044], Figs.2,8A-B; *see also* Ex.1037 at 4:34-38; Ex.1011 at 1, 6, 46; Ex.1010 at 6, 19.

Ellsberry further renders obvious that its "*module control circuit*" includes "*first*" through "*fourth input/output connections*." Ex.1003¶¶346-349. When the architecture of Figure 13 is configured with the disclosures of Figures 2 and 5,

there are connections from the control unit carrying address (*e.g.*, A0-A15 in "ACA"), control (*e.g.*, RAS_n, CAS_n and WE_n in "ACA") and chip select (*e.g.*, CS0A) signals to Port A and B memory devices. Ex.1003¶347. That is, any subset of the connections carrying such signals to memory devices on Port A (*e.g.*, the address signals A0-A7 in "ACA") constitutes the claimed "*first input/output connections,*" while a different subset (*e.g.*, command signal RAS_n in "ACA" and chip select signal CS0A) constitutes the claimed *second input/output connections.*" Ex.1003¶348. The same analysis applies to the connections from the control unit to the memory devices on Port B (which would correspond to the "*third*" and "*fourth*" set of "*connections*"). Ex.1003¶349 .

Ellsberry also discloses that its "*first memory devices*" include a subset coupled to the "*first … connections*," and a subset coupled the "*second … connections*," and that its "*second memory devices*" include a subset coupled to the "*third … connections*," and a subset coupled the "*fourth … connections*." Ex.1003¶¶350-353. As demonstrated above in Section 1.c), Ellsberry's system can access a subset of the attached memory devices, such as the nine memory devices 504 disclosed in Figure 5 ("*first memory devices*") while not accessing the other memory devices (including "*second memory devices*"). Ex.1003¶¶215-223,350; Ex.1005¶¶[0031]-[0036],[0042],[0047]-[0050], Figs.5,8A. Thus, any "*subset"* of

the "*first*" or "*second*" memory devices can be assigned to any subset of the connections to satisfy the claim limitations. Ex.1003¶¶351,352.

To the extent one might argue that Ellsberry does not disclose that the "*connections*" of its control unit include "*input/output connections*" because such connections require both input and output, *see, e.g.*, Ex.1011 at 6, it would have been obvious to use a control unit with "*input/output connections*" in order to control well known memory devices at the time, including Direct DRAM devices, which can be controlled through control registers requiring both input and output access. Ex.1003¶¶365,366; Ex.1005¶¶[0003],[0023]; Ex.1042 at 3-5,72. A Skilled Artisan would have understood that the module controller can use the information in the register communication to set parameters in the memory devices. Ex.1003¶¶367,368; Ex.1005¶¶[0003],[0023],[0039],[0044],Fig.3; Ex.1042 at 3. In fact, Ellsberry specifically discloses that its module control unit uses "memory configuration information 306 (e.g., DRAM type, etc.)." Ex.1005¶[0039],Fig. 3. A Skilled Artisan would have understood and been motivated to utilize "*input/output connections*" in conjunction with Ellsberry's control unit in order provide the predictable result of receiving "memory configuration information" from the memory devices. Ex.1003¶368.

Ellsberry therefore renders claims 9, 13, 23, 28 and 59 obvious. Ex.1003¶¶344-369,380-381,432-433,442-443,614-615.

9. Claims 11, 26, and 64

Claims 11, 26 and 64 require that "[…] *one or more of the first memory devices include a single memory device outputting or receiving the [respective n-bit section of the each N-bit wide data signal]/[portion of the data] associated with the memory read or write command*." When the configuration of Ellsberry's Figure 13 is used in its module of Figures 2 and 5, each "*n-bit section of the each N-bit wide data signal"* is equal to eight bits (one byte) and each of the memory devices has a bit width of eight. Ex.1003¶¶244,280-291,373; Ex.1005 at Fig.13. Thus, whichever of the memory devices is the "*first memory device*" activated by its chip select signal in response to a read or write command, it outputs or receives eight bits (i.e., one byte). Ex.1003¶373.

Ellsberry therefore discloses the requirements of claims 11, 26 and 64. Ex.1003¶¶372-374,438-439,624-625.

10. Claims 12, 27, and 65

Claims 12, 27 and 65 require that "[…] *one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective [n-bit section of the each N-bit wide data signal]/[portion of the data] associated with the memory read or write command*." When the configuration of Ellsberry's Figure 11 is used in its module of Figures 2 and 6, each "*n-bit section of the each N-bit wide data signal"* is equal to eight bits (one byte), each of the

memory devices has a bit width of four, thus a pair of memory devices provides the same bit width as the bank switch. Ex.1003¶¶376-378; Ex.1005 at Fig.11.

Ellsberry therefore discloses the requirements of claims 12, 27 and 65. Ex.1003¶¶375-379,440-441,626-627.

11. Claim 14

Claim 14 requires that "*the first memory read or write command is a memory write command, and wherein the each respective buffer circuit includes tristate buffers controlled by the logic to transmit the respective n-bit section of the each N-bit wide data signal associated with the memory write command to the respective one or more of the first memory devices*."

As discussed above in Section 1.e), Ellsberry discloses a "*memory write command*" and transmitting the "*n-bit section*" through bidirectional drivers 402&404 to the "*memory devices*" on Ellsberry's module. Ex.1003¶¶240-246,383,384; Ex.1005¶¶[0031],[0045], Figs.4,8A. Both such drivers are "*controlled by logic*." *Id*. Although Ellsberry does not expressly describe the detailed circuit elements of bidirectional drivers 402&404, it would have been obvious to implement bidirectional memory bus drivers using "*tristate buffers*." Ex.1003¶385. The use of such buffers for that purpose was well-known as of the priority date of the 907 Patent. Ex.1003¶386; Ex.1035 (Stone) at 117 ("microprocessors are designed with tri-state drivers on the address and data

lines"). Further, a Skilled Artisan would have been motivated to use them in the configuration of Ellsberry to achieve the predictable result of a reliable and efficient interface circuit to drive data to and from the memory devices. Ex.1003¶¶386-388.

12. Claim 16

a) [16.a]: *"A memory module …"*

For the same reasons as claim [1.a], Ellsberry discloses a "*memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n*." *See* §1.a); Ex.1003¶¶186-196,393-394.

b) [16.b]: *"a control circuit …"*

For the same reasons as claim [1.b], Ellsberry discloses "*a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals*". *See* §1.b); Ex.1003¶¶198-211,395-396.

c) [16.c]: *"a plurality of memory devices …"*

For the same reasons as claim [1.c], Ellsberry discloses "*a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response*

to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command." *See* §1.c); Ex.1003¶¶212-223,397-398.

d) [16.d]: *"a plurality of buffer circuits …"*

As discussed above with reference to limitation [1.d], Ellsberry discloses, under both the fork-in-the-road and straight-line interpretations, "*a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being … coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines.*" *See* §1.d); Ex.1003¶¶225-239,399-400. Ellsberry further discloses that the coupling "*via a respective set of the M sets of n data lines*" is "*operative*." Ex.1003¶¶186-196,401-402; Ex.1005¶¶[0011],[0028].

e) [16.e]: *"… buffer circuit including data paths and logic …"*

Ellsberry discloses that "*each respective buffer circuit include[s] data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be*

communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits." *See* §1.e); Ex.1003¶¶240-246,403-408.

As discussed above with reference to limitation [1.e], Ellsberry discloses, that its "*buffer circuit*" includes "*logic*" that "*[responds] to the second module control signals … [by allowing communication of] a respective n-bit section of the each N-bit wide data signal … between the … data lines and the … module data lines ….*" *See* §1.e); Ex.1003¶¶240-246,403-404.

Ellsberry also discloses that its "*buffer circuit*" includes "*data paths and logic that configures the data paths in response to the second module control signals*." Ex.1003¶¶405-408. As shown in the annotated version of Ellsberry's Figure 4 below, the memory bank switch has one data path from bus 230 (on the left, green) through bidirectional driver 402 to port A leading to bus 234 (green), and another data path through bidirectional driver 404 to port B leading to bus 236 (green). Thus, Ellsberry discloses that the bank switch ("*buffer circuit*") has multiple "*data paths*" as required by the claim. Ex.1003¶405. The control block ("*logic*") configures those data paths to the bank switch control signals 210 (purple, "*second module control signals*"), e.g., by allowing communication through the data path to Port B, and disabling the communication through the data path to Port A. Ex.1003¶406; Ex.1005¶¶[0031],[0045].

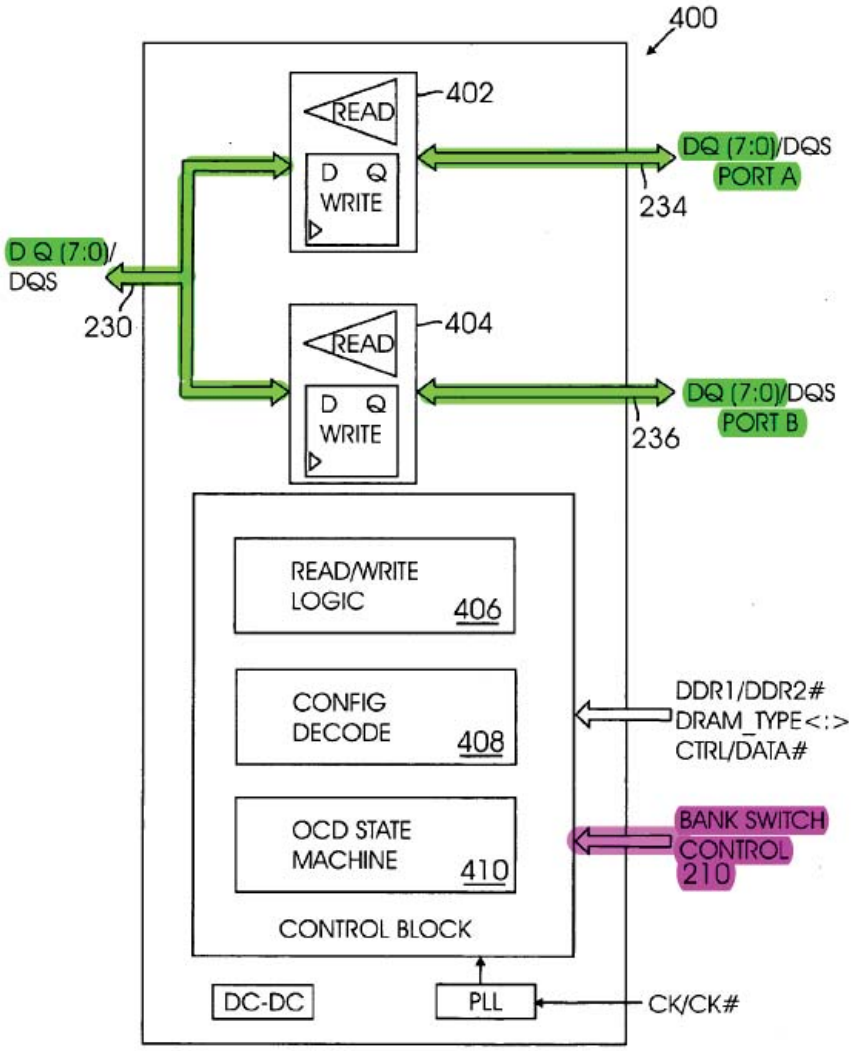


Fig. 4

By configuring the data paths to port A and port B properly, Ellsberry's bank switch "*logic*" is "*causing a respective n-bit section (DQ[7:0]) of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits*." Ex.1003¶¶237,407; Ex.1005¶[0030],Fig.4.

f) [16.f]: *"… buffer circuit … configured to isolate memory device load …"*

For the same reasons as claim [1.f], Ellsberry discloses "*each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller*." *See* §1.f); Ex.1003¶¶247-250,409-410.

g) [16.g]: *"a printed circuit board (PCB) …"*

For the same reasons as claim [1.g], Ellsberry renders obvious "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines*." *See* §1.g); Ex.1003¶¶251-270,411-412.

h) [16.h]: *"… buffer circuits are mounted … at corresponding positions …"*

For the same reasons as claim [1.h], Ellsberry renders obvious that "*the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding*

to the respective one or more of the first memory devices and the respective one or more of the second memory devices." *See* §1.h); Ex.1003¶¶271-279,413-414.

13. Claims 17-18, 60, and 62

Claims 17-18, 60 and 62 require that the "*data paths*" in its "*buffer circuit*" include "*write data paths*" and "*read data paths*" having "*at least one tristate buffer controlled by the logic*." Ex.1003¶¶415-423.

As discussed above in Section 12.e) with reference to claim element [16.e], in Ellsberry's bank switch ("buffer circuit"), one bidirectional data path passes through bidirectional driver 402 and another passes through bidirectional driver 404, both drivers being "*controlled by logic*." Ex.1003¶¶403-408,416; Ex.1005 at Fig.4. Further, as discussed above in Section 11 with reference to claim 14, it would have been obvious to a Skilled Artisan to implement bidirectional drivers 402&404 using "*tristate buffer[s]*."

14. Claim 58

a) [58.a]: *"A memory module …"*

For the same reasons as claim [1.a], Ellsberry discloses a "*memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines*." *See* §1.a); Ex.1003¶¶186-196,593-594.

b) [58.b]: *"memory devices …"*

For the same reasons as claim [1.c], Ellsberry discloses "*memory devices including first memory devices and second memory devices*." §1.c); Ex.1003¶¶212-224,595-596.

c) [58.c]: *"a module control circuit …"*

Ellsberry discloses "*a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data*

associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals."

As shown above with reference to limitation [1.b], Ellsberry discloses "*a module control circuit*" that receives "*via control signal lines*" a "*first … and second set of input address and control signals*" that correspond to separate "*memory read or write command[s]*." *See* §1.b); Ex.1003¶¶198-201,598.

As shown above with reference to limitation [1.c], Ellsberry further discloses that "*in response to the first output … signals, the first memory devices output or receive data …while the second memory devices do not …*," and "*in response to the first output … signals, the first memory devices output or receive data …while the second memory devices do not ….*" *See* §1.c); Ex.1003¶¶212-224,600-601. That is, Ellsberry discloses that a memory access may be directed to a subset of the memory devices coupled to Port A (or Port B) which will output or receive data in response, and non-targeted memory devices coupled to Port B (or Port A) will not output or receive data. Ex.1003¶601.

Ellsberry also discloses that its "*module control circuit" is "configured ... to produce a first [and second] set of module control signals in response to the first [and second] set of input … signals,*" where the first and second sets of module control signals are "*different.*" *See* Ex.1003¶¶452-458,602. In response to the first and second memory accesses ("*first" and "second" "input address and control signals*") the control unit will produce corresponding address and command signals on the address and command bus 220 to the memory banks ("*first" and "second" "output address and control signals*"), and bank control signals for the bank switches on control bus 210 ("*first" and "second" "module control signals"*). Ex.1003¶¶453,454. Ellsberry also discloses that different memory banks can be activated in response to the first and second memory accesses, which would cause the control unit to send different "*module control signals*" to the bank switches in order to activate a different Port (A or B). Ex.1003¶455; Ex.1005¶[0031],[0039].

Ellsberry also discloses that the "*first module control signals*" are different from the "*second module control signals.*" Ex.1003¶¶457. Ellsberry discloses that the "control unit 204 … indicates to the memory bank switches 206 &208 ***how*** data from the DIMM interface 202 should be received and/or stored." Ex.1005¶[0029]. Ellsberry also discloses Mode Register Set (MRS), Extended Mode Register Set (EMRS), and Burst related commands and corresponding parameters that can be set and reset by those commands anytime. Ex.1005 at

Figs.8A,8B,9; Ex.1011 at 10. After such a change, the "*second module control signals*" for the bank switches would be different from the "*first module control signals*" due to different timing parameters such as latency and burst length parameters even if the same Port of the bank switch is activated. Ex.1003¶¶327-336.

To the extent one might argue that Ellsberry does not disclose such use of timing parameters, it would have been obvious for the reasons discussed above with reference to claim 8. *See* §7; Ex.1003¶¶338-341.

d) [58.d]: *"a plurality of buffer circuits …"*

For the same reasons as claim [1.d], Ellsberry discloses "*a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices*." *See* §1.d); Ex.1003¶¶225-239,604-605.

e) [58.e]: *"… buffer circuit including data paths and logic …"*

Ellsberry discloses that "*each respective buffer circuit includ[es] data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals*."

As discussed above with respect to limitation [16.e], Ellsberry discloses that its "*buffer circuit*" includes "*data paths and logic that configures the data paths in response to the first set of module control signals*." *See* §12.e); Ex.1003¶¶403-408,465.

As discussed above with respect to limitation [1.e], Ellsberry discloses that its "*buffer circuit*" causes "*a respective portion of the data associated with the first*

memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit." *See* §1.e); Ex.1003¶¶240-246,466-467. Ellsberry discloses that a memory access (such as a write) to a subset of the memory devices (such as those coupled to Port B) will cause 8 bits per bank switch ("*a respective portion of the data associated with the first memory read or write command*") to be received by each bank switch ("*buffer circuit*") and transmitted to memory devices coupled to (in this example) Port B ("*respective one or more of the first memory devices"*). Ex.1003¶¶240-246,466.

In the same way, Ellsberry discloses that, "in response to the second module control signals" its "buffer circuit" causes "*a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit*." Ex.1003¶¶468-469. For the same reasons, a subsequent write of data ("*the second write command*") to memory devices coupled to Port A ("*one or more of the second memory devices*") would cause the Ellsberry banks switches to produce the same functionality, albeit with the data transferred to the Port A memory devices. Ex.1003¶¶240-246,468.

Ellsberry also discloses that the "*data paths*" are "*configured differently when the logic is responding to the second module control signals*" versus "*the*

first module control signals." Ex.1003¶470. In response to the first (or second) write command and the module control signals produced in response thereto, the bank switches configure the write data path through bidirectional driver 404 (or 402) so that data would be transmitted to memory devices coupled to Port B (or Port A). *Id*.; Ex.1005¶[0045],Fig.4; Ex.1003¶¶240-246. Moreover, Ellsberry discloses this limitation even under Patent Owner's apparent interpretation where the "*second memory devices*" are coupled to Port B, like the "*first memory devices*," and the data paths can be configured with different timing and duration for the second write command. Ex.1003¶¶452-458,470.

f) [58.f]: *"… buffer circuit … configured to isolate memory device load …"*

For the same reasons as claim [1.f], Ellsberry discloses "*each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller*." *See* §1.f); Ex.1003¶¶247-250,608-609.

g) [58.g]: *"a printed circuit board (PCB) …"*

For the same reasons as claim [1.g], Ellsberry renders obvious "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be*

releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines." *See* §1.g); Ex.1003¶¶251-270,610-611.

h) [58.h]: *"… buffer circuits are mounted … at corresponding positions …"*

For the same reasons as claim [1.h], Ellsberry renders obvious that "*the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices*." *See* §1.h); Ex.1003¶¶271-279,612-613.

B. Claims 1-29 and 58-65 are obvious over Ellsberry (Ex.1005) in view of JESD21-C (Ex.1010)

To the extent one might argue that Ellsberry does not sufficiently disclose claim elements [1.g], [16.g] and [58.g], it would have been obvious to include the claimed configuration in the system of Ellsberry at least in view of JESD21-C (Ex.1010). Ex.1003¶¶264-270; Ex.1010 at 6, 66, 73. In the combination with Ellsberry, the edge connector of JESD21-C would "*provide electrical conductivity between the module control circuit and the set of control signal lines, and between*

the M buffer circuits and the M sets of n data lines." Indeed, the edge connector of JESD21-C, just like in Ellsberry, includes "address bus," "memory data bus," and RAS, CAS, WE and chip select control signal lines to provide electrical conductivity for the corresponding signals. Ex.1010 at 6. JESD21-C therefore discloses this claim element.

Ellsberry and JESD21-C are analogous art to the 907 Patent because each is in the same field of endeavor (memory module design) (*see* Ex.1005 at Abstract; Ex.1010 at 5; Ex.1001 at Abstract), and also because Ellsberry and JESD21-C are reasonably pertinent to the problem addressed by the 907 Patent (efficient support of multi-rank memory modules) (*see* Ex.1001 at 1:35-2:51, Ex.1010 at 12; Ex.1005¶[0010]). The combination of Ellsberry and JESD21-C would have been simply the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement in the context of DIMM modules. Ex.1005¶¶[0002],[0023],[0027], Figs.5-6; Ex.1003¶¶266-267. A Skilled Artisan would have been motivated to make the combination in order to use the standard PCB form factor at that time with the novel capacity-expanding technology of Ellsberry (*see* Ex.1003¶268, Ex.1005¶¶[0026],[0027],[0050]), and to expand the possible market for any product embodying Ellsberry's technology (*see* Ex.1003¶269), and to ensure the ability to incorporate JESD21-C compatible

memory devices for a variety of design applications (*see* Ex.1003¶270, Ex.1036 at 1:65-2:3).

C. Claims 7, 19, and 24 are obvious over Ellsberry (Ex.1005) in view of Halbert (Ex.1006)

To the extent one argues that Ellsberry does not disclose the requirements of claims 7, 19, and 24, it would have been also obvious from Ellsberry's disclosure for the control unit to indicate "*a direction of data flow*" to the bank switches so that Ellsberry's Read/Write logic can properly control the drivers. Ex.1003¶321; Ex.1005 at claim 6 ("the memory bank switch … transfer[s] data information *to and from t*wo or more physical memory banks in real time *according to control signals from the controller*"). This functionality would have been obvious in view of Halbert's DIR (direction) signal which could be advantageously used by Ellsberry's Read/Write logic to synchronize the operation of the bank switch by configuring the bidirectional signal drivers. Ex.1003¶¶322-325; Ex.1005¶¶[0045],[0058],Claim 6; Ex.1006 at Fig.4. Indeed, Ellsberry and Halbert are analogous art to the 907 Patent, use similar "snooping" techniques to determine the direction of the flow, and control bidirectional drivers accordingly. Ex.1003¶¶323-325; Ex.1001 at 1:17-22, 10:55-62; Ex.1005¶¶[0010],[0012],[0039]; Ex.1006 at 3:58-4:8, 5:23-30,Fig.4. A Skilled Artisan would have readily understood that Ellsberry's command decoder 304 can be implemented to "snoop" read and write commands in order to generate a DIR

signal and provide a predictable result (i.e., setting the direction of data flow). Ex.1003¶325.

D. Claims 9 and 28 of the 907 Patent are obvious over Ellsberry (Ex.1005) in view of Ruckerbauer (Ex.1038)

To the extent one might argue that, in claims 9 and 28, the term "*first memory devices include a subset of memory devices coupled to the first input/output connections*" requires that the "*first input/output connections*" be coupled to fewer than all of the "*first memory devices*," Ellsberry renders this claim obvious in view of Ruckerbauer even under such a narrow interpretation. Ex.1003¶¶354-364. For example, both Ellsberry and Ruckerbauer disclose mounting a control circuit in the middle of the circuit board such that some of the memory devices are mounted to the left of the control circuit and some of the memory devices are mounted to the right of the control circuit, and Ruckerbauer discloses separate connections to the left and to the right. Ex.1003¶¶355-357; Ex.1005¶¶[0030],[0049], Fig.5; Ex.1038 at 4:57-62, 5:62-6:16, Figs.1-2.

Ellsberry and Ruckerbauer are analogous art to the 907 Patent because they are directed to "improving the performance and the memory capacity of memory subsystems … [including] dual in-line memory modules (DIMMs)." Ex.1001 at 1:17-22; Ex.1005 at [0010]; Ex.1038 at 1:20-2:36; Ex.1003¶358. Further, a Skilled Artisan would have been motivated to implement Ellsberry's module with separate control lines to the left and right according to Ruckerbauer because it

would simplify the connections and reduce the capacitive loading to reach the required signal speeds. Ex.1003¶¶358-362; Ex.1005¶¶[0010],[0027],Fig.5 (below),Fig.13; Ex.1038 at 4:46-5:3.

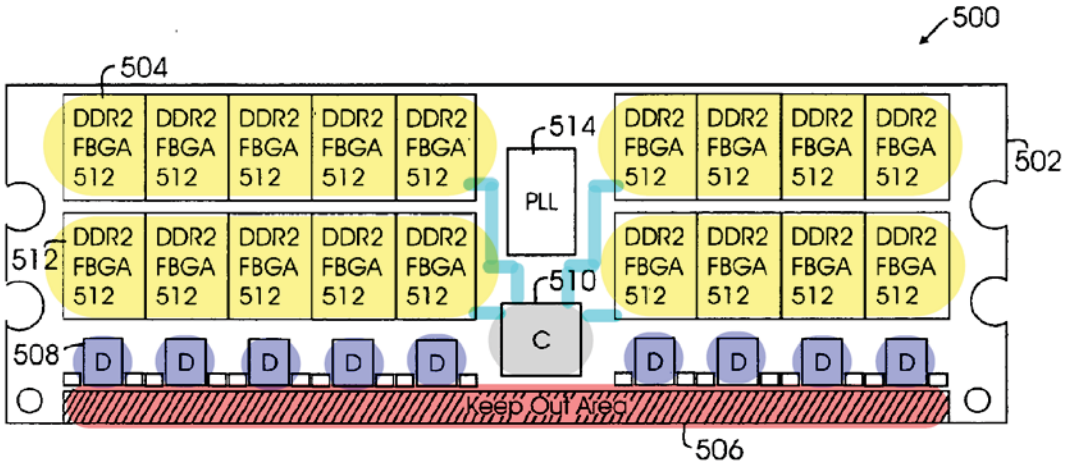


Fig. 5

Such an implementation would have been well within the level of skill at the time, and would use well known, standardized techniques that would work as in the prior art provide predictable results. Ex.1003¶¶363-364; Ex.1010 at 18; Ex.1038 at Fig.1, 2:31-:32.

E. Claims 14, 17-23 and 60-65 are obvious over Ellsberry (Ex.1005) in view of Stone (Ex.1035)

To the extent one argues that claims 14, 17-18, 60 and 62 (and the claims that depend from them) are not obvious because Ellsberry does not expressly disclose the use of "*tristate buffers*," it would have been obvious to implement Ellsberry's bidirectional drivers using "*tristate buffers*" to drive data to and from

the memory devices efficiently and reliably, as explained by Stone. Ex.1003¶¶385-388; Ex.1005 at Figs.11,13; Ex.1035 at 68,74 (Fig.2.28),117.

As shown in the configurations of Figs. 11 and 13 of Ellsberry, each of the data buses on Ports A and B of the bank switch has multiple taps, one for each memory device. Ex.1003¶388. A Skilled Artisan would have been motivated to use "*tristate buffers*" because Stone states that "tri-state drivers … [are] ***suitable for driving several taps on a transmission line***." Ex.1035 at 74; Ex.1003¶388. Thus, it would have been obvious to a Skilled Artisan to implement bidirectional drivers 402&404 in Ellsberry's multi-tap configuration using Stone's tristate buffers, such as those disclosed in Stone. Ex.1003¶¶388-389.

Further, with respect to claims 17-18, 60 and 62, Stone discloses separate write and read data paths, each of which includes a tristate buffer, as depicted below in Stone's Fig.4.7. Ex.1003¶417. The tristate buffers of Stone would be controlled by the bank switch logic of Ellsberry. Ex.1003¶¶418,419,421-423; Ex.1035 at 133.

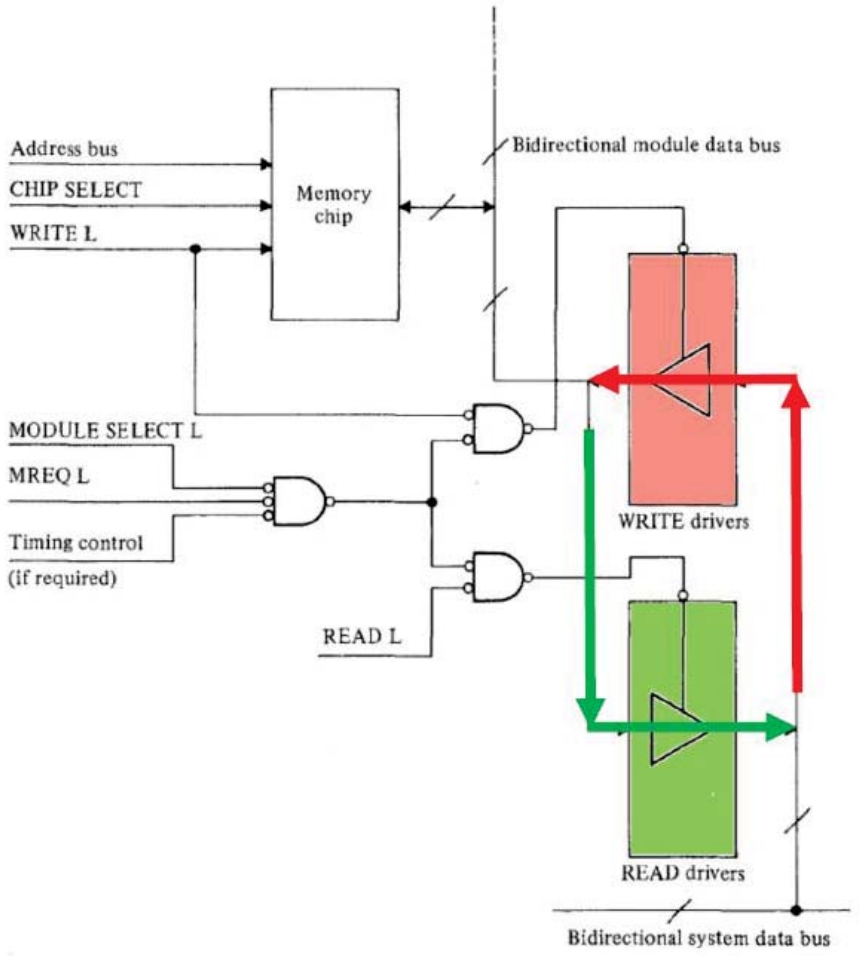


FIGURE 4.7 Tri-state driver control for interfacing memory chips to bidirectional data lines.

Ellsberry in view of Stone therefore renders claims 17, 18, 60 and 62 (and the claims that depend from them) obvious. Ex.1003¶¶415-423,616-617,620-621.

VIII. CONCLUSION

Because this Petition demonstrates that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the challenged claims, the Petitioner respectfully requests that a Trial be instituted and Claims 1-29 and 58-65 of the 907 Patent be canceled as unpatentable.

Dated: December 22, 2017

Respectfully Submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,987 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment A:

Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on this 22nd day of December, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by Federal Express on the following counsel of record for patent owner:

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 9,606,907
1002	File History of U.S. Patent No. 9,606,907
1003	Declaration of Dr. Harold Stone
1004	Curriculum Vitae of Dr. Harold Stone
1005	US Patent App. Publication No. 2006/0277355 by Ellsberry et al.
1006	US Patent No. 7,024,518 to Halbert et al.
1007	U.S. Patent Application Publication No. 2006/0117152 to Amidi et al.
1008	U.S. Patent Application Publication No. 2006/0262586 by Solomon et al.
1009	JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000)
1010	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1011	JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005)
1012	Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC)
1013	U.S. Patent No. 7,289,386 to Bhakta et al.
1014	U.S. Patent No. 7,532,537 to Solomon et al.
1015	U.S. Patent No. 8,417,870 to Lee et al.
1016	File History of U.S. Patent No. 8,417,870
1017	U.S. Patent No. 8,516,185 to Lee et al.
1018	File History of U.S. Patent No. 8,516,185

Exhibit #	Reference Name
1019	U.S. Patent No. 8,130,560 to Rajan et al.
1020	U.S. Patent No. 5,784,705 to Leung
1021	US Patent App. Publication No. 2009/0248969 by Wu et al.
1022	Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *SanDisk Corp. v. Netlist, Inc.*, IPR2014-01029, Paper No. 11 (Dec. 16, 2014)
1023	Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01369, Paper No. 12 (Mar. 9, 2015)
1024	Excerpts from the Hearing in *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 8–11, 2017)
1025	Complainant Netlist, Inc.'s Initial Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 30, 2017) (excerpts relevant to '185 patent)
1026	Respondents' Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 30, 2017) (excerpts relevant to '185 patent)
1027	High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex.1026)
1028	Complainant Netlist Inc.'s Reply Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent)
1029	Respondents' Reply Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent)

Exhibit #	Reference Name
1030	High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029)
1031	Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00577, Paper No. 8 (July 7, 2017)
1032	Final Written Decision, *Diablo Techs., Inc. v. Netlist, Inc.*, IPR2014-00882, Paper No. 33 (Dec. 14, 2015)
1033	*Netlist, Inc. v. Diablo Techs., Inc.*, No. 2016-1742 (Fed. Cir. July 25, 2017)
1034	Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 (June 14, 2017)
1035	Stone, H.S. *Microcomputer Interfacing*, Reading, MA: Addison Wesley, 1982
1036	U.S. Patent No. 5,630,096 to Zuravleff et al.
1037	U.S. Patent No. 6,683,372 to Wong et al.
1038	U.S. Patent No. 7,334,150 to Ruckerbauer et al.
1039	Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004)
1040	Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts)
1041	Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts)
1042	Direct RDRAM datasheet (2000)

PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment C:

Claim Listing

Ref. #	Listing of Challenged Claims
[1.a]	**1.** A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
[1.b]	a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
[1.c]	a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
[1.d]	M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,
[1.e]	the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines,
[1.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

Ref. #	Listing of Challenged Claims
[1.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines,
[1.h]	wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[2]	**2.** The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.
[3]	**3.** The memory module of claim 1, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the M sets of n data lines to the memory controller.
[4]	**4.** The memory module of claim 3, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.
[5]	**5.** The memory module of claim 1, wherein the each respective buffer circuit is configured to present a load to the respective one or more of the first memory devices that is the same as a load the memory controller would present.

Ref. #	Listing of Challenged Claims
[6]	**6.** The memory module of claim 1, wherein the each respective buffer circuit has a first data width of n bits, and wherein each of the plurality of memory devices has a second data width different from the first data width.
[7]	**7.** The memory module of claim 1, wherein the second module control signals indicate a direction of data flow through the buffer circuits.
[8]	**8.** The memory module of claim 1, wherein the module control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter.
[9]	**9.** The memory module of claim 1, wherein the module control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[10]	**10.** The memory module of claim 1, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.
[11]	**11.** The memory module of claim 1, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[12]	**12.** The memory module of claim 1, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.

Ref. #	Listing of Challenged Claims
[13]	**13.** The memory module of claim 1, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the plurality of memory devices.
[14]	**14.** The memory module of claim 1, wherein the first memory read or write command is a memory write command, and wherein the each respective buffer circuit includes tristate buffers controlled by the logic to transmit the respective n-bit section of the each N-bit wide data signal associated with the memory write command to the respective one or more of the first memory devices.
[15]	**15.** The memory module of claim 1, wherein the M buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide.
[16.a]	**16.** A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
[16.b]	a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
[16.c]	a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

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[16.d]	a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,
[16.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits,
[16.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and
[16.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines,
[16.h]	wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

Ref. #	Listing of Challenged Claims
[17]	**17.** The memory module of claim 16, wherein the data paths include write data paths, each write data path including at least one tristate buffer controlled by the logic.
[18]	**18.** The memory module of claim 17, wherein the data paths further include read data paths, each read data path including a tristate buffer controlled by the logic.
[19]	**19.** The memory module of claim 18, wherein the second module control signals indicate a direction of data flow through the buffer circuits.
[20]	**20.** The set of circuits in claim 18, wherein the control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the module control signals in accordance with a latency parameter.
[21]	**21.** The memory module of claim 18, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the control circuit.
[22]	**22.** The memory module of claim 18, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.
[23]	**23.** The memory module of claim 18, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the plurality of memory devices.
[24]	**24.** The memory module of claim 16, wherein the second module control signals indicate a direction of data flow through the buffer circuits.

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[25]	**25.** The memory module of claim 16, wherein the control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter.
[26]	**26.** The memory module of claim 16, wherein each of the plurality of memory devices is n-bit wide, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[27]	**27.** The memory module of claim 16, wherein each of the memory devices is n/2-bit wide, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[28]	**28.** The memory module of claim 16, wherein the control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[29]	**29.** The memory module of claim 16, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide.
[30.a]	**30.** A memory module having a data width of N bits and configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

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[30.b]	a module control circuit configured to receive from the memory controller via the set of control signal lines first input address and control signals corresponding to a first write command and subsequently second input address and control signals corresponding to a second write command, the module control circuit producing first output address and control signals and first module control signals in response to the first input address and control signals, the module control circuit producing second output address and control signals and second module control signals in response to the second input address and control signals, the second module control signals being different from the first module control signals;
[30.c]	memory devices coupled to the module control circuit, the memory devices including first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command, and second memory devices responding to the second output address and control signals by receiving each N-bit wide data signal associated with the second write command; and
[30.d]	a plurality of buffer circuits operatively coupled to respective sets of the plurality of sets of data signal lines and configured to receive the first module control signals from the module control circuit and subsequently the second module control signals from the module control circuit,

Ref. #	Listing of Challenged Claims
[30.e]	each respective buffer circuit in the plurality of buffer circuits including data paths and logic that configures the data paths in response to the first module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the first write command received by the each respective buffer circuit from the memory controller via a respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the first memory devices, where n is equal to a bit width of the each respective buffer circuit, wherein the logic in the each respective buffer circuit subsequently configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the second write command received by the each respective buffer circuit from the memory controller via the respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the second memory devices, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein each of the respective one or more of the first memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein each of the respective one or more of the second memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the second write command; and
[30.f]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality sets of data signal lines,

Ref. #	Listing of Challenged Claims
[30.g]	wherein the plurality of buffer circuits are mounted on the PCB between memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[31]	**31.** The memory module of claim 30, wherein the data paths in the each respective buffer circuit are configured in accordance with a latency parameter when the logic is responding to the first module control signals and when the logic is responding to the second module control signals.
[32]	**32.** The memory module of claim 30, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the respective one or more of the second memory devices from the memory controller.
[33]	**33.** The memory module of claim 32, wherein the each respective buffer circuit is configured to present to the memory controller one memory device load on each data signal line of the respective set of the plurality of sets of data signal lines.
[34]	**34.** The memory module of claim 32, wherein the each respective buffer circuit is configured to present a load that is the same as a load the memory controller would present to the respective one or more of the first memory devices and subsequently to the respective one or more of the second memory devices.
[35]	**35.** The memory module of claim 30, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the plurality of sets of data signal lines is eight bits wide.

Ref. #	Listing of Challenged Claims
[36]	**36.** The memory module of claim 30, wherein the module control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[37]	**37.** The memory module of claim 30, wherein each of the memory devices is n-bit wide, wherein the respective one or more of the first memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the second write command.
[38]	**38.** The memory module of claim 30, wherein each of the memory devices is n/2-bit wide, wherein the respective one or more of the first memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the second write command.
[39]	**39.** The memory module of claim 30, wherein the each respective buffer circuit includes input buffers to receive the respective n-bit section of the each N-bit wide data signal associated with the first write command from the memory controller, wherein each of the input buffers is comparable in loading to an input buffer on one of the memory devices.

Ref. #	Listing of Challenged Claims
[40]	**40.** The memory module of claim 39, wherein the each respective buffer circuit further includes output buffers to drive the respective n-bit section of the each N-bit wide data signal associated with the first write command to the respective one or more of the first memory devices, wherein each of the output buffers is comparable in loading to an output buffer on the memory controller.
[41]	**41.** The memory module of claim 40, wherein the output buffers regenerate the respective n-bit section of the each N-bit wide data signal associated with the first write command to restore desired signal waveform shapes in the respective n-bit section of the each N-bit wide data signal associated with the first write command.
[42]	**42.** The memory module of claim 39, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the plurality of sets of data signal lines is eight bits wide.
[43.a]	**43.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:
[43.b]	memory devices;

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[43.c]	a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command;
[43.d]	a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices,
[43.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit,
[43.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller; and

Ref. #	Listing of Challenged Claims
[43.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines,
[43.h]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.
[44]	**44.** The memory module of claim 43, wherein the set of module control signals are further dependent on whether the memory read or write command is a memory read command or a memory write command, and wherein the logic configures the data paths differently depending on whether the memory read or write command is a memory read command or a memory write command.
[45]	**45.** The memory module of claim 43, wherein the data paths include write data paths, and wherein the write data paths include tristate buffers controlled by the logic.
[46]	**46.** The memory module of claim 45, wherein the memory read or write command is a memory write command, and wherein the tn state buffers regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal waveform shapes, and transmit regenerated signals to the respective one or more of the subset of the memory devices.

Ref. #	Listing of Challenged Claims
[47]	**47.** The memory module of claim 45, wherein the each respective buffer circuit is configured to present one memory device load on each data line of the respective set of the plurality of sets of data lines to the memory controller.
[48]	**48.** The memory module of claim 45, wherein the data paths include read data paths, and wherein the read data paths include tristate buffers controlled by the logic.
[49]	**49.** The memory module of claim 48, wherein the memory read or write command is a memory read command, and wherein the tn state buffers in the read data paths regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the respective one or more of the subset of the memory devices to restore signal waveform shapes, and transmit regenerated signals to the memory controller via the respective set of the plurality sets of data lines.
[50]	**50.** The memory module of claim 48, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.
[51]	**51.** The memory module of claim 50, wherein each of the memory devices is eight bits wide, wherein the one or more memory devices in the subset of the memory devices include a single memory device outputting or receiving the respective portion of the data associated with the memory read or write command.
[52]	**52.** The memory module of claim 50, wherein each of the memory devices is four bits wide, wherein the one or more memory devices in the subset of the memory devices include a pair of memory devices each outputting or receiving half of the respective portion of the data associated with the memory read or write command.
[53.a]	**53.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

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[53.b]	a module control circuit coupled to the set of control signal lines and configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce output address and control signals and a set of module control signals in response to the input address and control signals, the module control circuit having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections;
[53.c]	memory devices including first memory devices and second memory devices, the first memory devices including a first number of memory devices coupled to the first input/output connections and a second number of memory devices coupled to the second input/output connections, the second memory devices including a third number of memory devices coupled to the third input/output connections and a fourth number of memory devices coupled to the fourth input/output connections, wherein, in response to the output address and control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
[53.d]	a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit is coupled between respective one or more of the first memory devices and a respective set of the plurality of sets of data lines, and between respective one or more of the second memory devices and the respective set of the plurality of sets of data lines,
[53.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective section of the each N-bit wide data signal to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit,

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[53.f]	wherein the data paths include write data paths and read data paths, the write data paths including tristate buffers controlled by the logic and the read data paths including tristate buffers controlled by the logic,
[53.g]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and the respective one or more of the second memory devices from the memory controller; and
[53.h]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data signal lines,
[53.i]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[54]	**54.** The memory module of claim 53, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the plurality of sets of data lines to the memory controller.
[55]	**55.** The memory module of claim 54, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.

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[56]	**56.** The memory module of claim 55, wherein each of the memory devices is eight bits wide, wherein the one or more of the first memory devices include a single memory device outputting or receiving the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command.
[57]	**57.** The memory module of claim 55, wherein each of the memory devices is four bits wide, wherein the one or more of the first memory devices include a pair of memory devices each outputting or receiving 4 bits of the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command.
[58.a]	**58.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:
[58.b]	memory devices including first memory devices and second memory devices;

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[58.c]	a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;
[58.d]	a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices,

Ref. #	Listing of Challenged Claims
[58.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals,
[58.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and
[58.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines,
[58.h]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

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[59]	**59.** The memory module of claim 58, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the memory devices.
[60]	**60.** The memory module of claim 59, wherein the data paths include write data paths, and wherein the write data paths include tristate buffers controlled by the logic.
[61]	**61.** The memory module of claim 60, wherein the each respective buffer circuit is configured to present one memory device load on each data line of the respective set of the plurality of sets of data lines.
[62]	**62.** The memory module of claim 60, wherein the data paths include read data paths, and wherein the read data paths including tristate buffers controlled by the logic.
[63]	**63.** The memory module of claim 62, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.
[64]	**64.** The memory module of claim 63, wherein each of the memory devices is eight bits wide, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective portion of the data associated with the first memory read or write command.
[65]	**65.** The memory module of claim 63, wherein each of the memory devices is four bits wide, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective portion of the data associated with the first memory read or write command.