Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 9,606,907

Issued: March 28, 2017

Filed: August 20, 2013

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH DISTRIBUTED DATA BUFFERS AND METHOD OF OPERATION

Inter Partes Review No. IPR2018-00365

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,606,907 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

TABLE OF CONTENTS

I. INTRODUCTION

Petitioners respectfully request institution of trial on all claims of the 907 Patent based on the obvious combination of the prior art Halbert (Ex.1006) and Amidi (Ex.1007) references, with this Petition addressing claims 30-57, and a companion Petition addressing claims 1-29 and 58-65. All claims in the 907 Patent fundamentally cover the same invention disclosed and claimed in the parent, 185 Patent (Ex.1017), and were only allowed after a terminal disclaimer was filed. Trial was instituted on the parent patent based on the combination of Halbert and Amidi, *see* Ex.1031, and should be instituted here as well for similar reasons.

The 907 Patent essentially claims distributed data buffers on a memory module, but Halbert disclosed such a memory module years earlier. And Amidi makes it obvious that Halbert could have been used with multiple selectively enabled ranks of memory, just as the 907 Patent does.

During prosecution of the 907 Patent, Halbert was not disclosed to the examiner until after the claims had been allowed, and the examiner's new reasons for allowance addressed only Halbert alone, not the combination of Halbert and Amidi that is the basis of this petition and the Board's previous institution of trial against the parent patent. Although the claims of the 907 Patent are much longer than the claims in the parent patent, the extra words do not actually add anything beyond what would have already been employed in conventional memory modules

(such as a printed circuit board). Nor do the extra words create any claim construction disputes material to this Petition, given that the combination of Halbert and Amidi satisfies the claim requirements under any reasonable construction. Trial should therefore be instituted on all claims based on this Petition and its companion Petition.

II. PETITIONER'S MANDATORY NOTICES

A. Real Party-in-Interest (37 CFR § 42.8(b)(1))

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

B. Related Matters (37 CFR § 42.8(b)(2))

U.S Patent No. 9,606,907 B2 ("the 907 Patent") issued on March 28, 2017, and is now involved in the following proceedings:

- *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017)
- *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Cal. filed June 14, 2017)

The 907 Patent is a continuation of U.S. Patent 8,516,185 B2, which issued on August 20, 2013, and is involved in the following proceedings:

- IPR2017-00577 (instituted July 7, 2017 "as to claims 1–3, 7, 8, and 10–12 of the '185 Patent as being unpatentable under 35 U.S.C. 103(a) as obvious over Halbert and Amidi")

- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016)
- *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016)

This petition is one of four related petitions against all claims of the 907 Patent. There are four petitions given the length of the claim language and the word limits in 37 C.F.R. § 42.24(a)(1)(i). The four petitions are generally divided as follows:

- IPR petition against claims 1–29 and 58–65 of the 907 Patent based primarily on the Ellsberry reference (Ex.1005)
- IPR petition against claims 30–57 of the 907 Patent based primarily on the Ellsberry reference (Ex.1005)
- IPR petition against claims 1–29 and 58–65 of the 907 Patent based primarily on the Halbert/Amidi references (Ex.1006,7)
- IPR petition against claims 30–57 of the 907 Patent based primarily on the Halbert/Amidi references (Ex.1006,7)

The Ellsberry-based petitions are not redundant to the Halbert/Amidi-based petitions because Patent Owner has previously argued that Halbert and Amidi may not properly be combined. Moreover, the Halbert/Amidi-based petitions are not redundant of the Ellsberry petitions because the Board has previously instituted trial against the parent of the 907 Patent based on the Halbert/Amidi combination.

C. Lead and Back-up Counsel (37 CFR § 42.8(b)(3))

Lead Counsel is: Joseph A. Micallef (Reg. No. 39,772), Sidley-SKH-IPR@sidley.com, (202) 736-8492.

Back-up Counsel are:

- Theodore W. Chandler (Reg. No. 50,319), Sidley-SKH-IPR@sidley.com, (213) 896-5830
- Wonjoo Suh (Reg. No. 64,124), Sidley-SKH-IPR@sidley.com, (202) 736-8831
- Ferenc Pazmandi (Reg. No. 66,216), Sidley-SKH-IPR@sidley.com, (415) 772-7410.

D. Service Information (37 CFR § 42.8(b)(4))

Service on Petitioners may be made by e-mail (Sidley-SKH-IPR@sidley.com), mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the 907 Patent May Be Contested by Petitioner (§42.104(a))

Petitioner certifies it is not barred or estopped from requesting *inter partes* review ("IPR") of the 907 Patent (Ex.1001). Neither Petitioner, nor any party in

privity with Petitioner, has filed a civil action challenging the validity of any claim of the 907 Patent. Neither Petitioner, nor any party in privity with Petitioner, has filed a prior IPR challenging the validity of any claim of the 907 Patent, other than those identified above in Section II.B. Petitioner also certifies this IPR petition is filed within one year of the date of service of a complaint alleging infringement of a patent. Petitioner therefore certifies this patent is available for *inter partes* review. 37 C.F.R. §§42.101-.102.

B. Fee for Inter Partes Review (§42.15(a))

The Director is authorized to charge the fee specified by 37 CFR §42.15(a) to Deposit Account No. 50-1597.

C. Proof of Service (§§42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

IV. Identification of Claims Being Challenged (§42.104(b))

Claims 30-57 of the 907 Patent are unpatentable under pre-AIA 35 U.S.C. §103(a) as follows:

(i) Claims 30-57 are unpatentable as being obvious over U.S. Patent No. 7,024,518 to Halbert et al. ("Halbert") (Ex.1006) in view of U.S. Pat. App. Pub. No. 2006/0117152 to Amidi et al. ("Amidi") (Ex.1007);

(ii) Claims 36 and 53-57 are unpatentable as being obvious over Halbert (Ex.1006) and Amidi (Ex.1007) in view of U.S. Patent No. 7,334,150 to Ruckerbauer et al. ("Ruckerbauer") (Ex.1038);

(iii) Claims 45-57 are unpatentable as being obvious over Halbert (Ex.1006) and Amidi (Ex.1007) in view of Stone (Ex.1035); and

(iv) Claims 31 is unpatentable as being obvious over Halbert (Ex.1006) and Amidi (Ex.1007) in view of U.S. Pat. App. Pub. No. 2006/0262586 to Solomon et al. ("Solomon") (Ex.1008).

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§**V-VII**. The evidence relied upon in this petition is listed in **Attachment B**. **Attachment C** includes a listing of the challenged claims with each limitation designated with a number and letter (*e.g.*, [1.a]). These designations are referenced in the claim-by-claim analysis in §**VII** below.

V. Relevant Information Concerning the Contested Patent

A. Effective Filing Date of the 907 Patent

The application that resulted in the 907 Patent is a continuation of an application filed on April 15, 2010, now Patent No. 8,516,185 ("the 185 Patent") (Ex.1017), which is a "continuation-in-part" of an application filed on July 16, 2009, now Patent No. 8,417,870 (Ex.1015). Because each of the prior art references identified in this Petition predates July 16, 2009, Petitioner assumes for this Petition only that the claims of the 907 Patent are entitled to a priority date of July 16, 2009. Ex.1003¶¶43-46.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA" or "Skilled Artisan") in the field of the 907 Patent in 2009 would have had an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in

such engineering disciplines and at least three years working the field. Ex.1003¶47. Such a person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id*. (citing Ex.1041). A POSITA would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs, and more low level circuits such as tri-state buffers. *Id*. (citing Ex.1035).

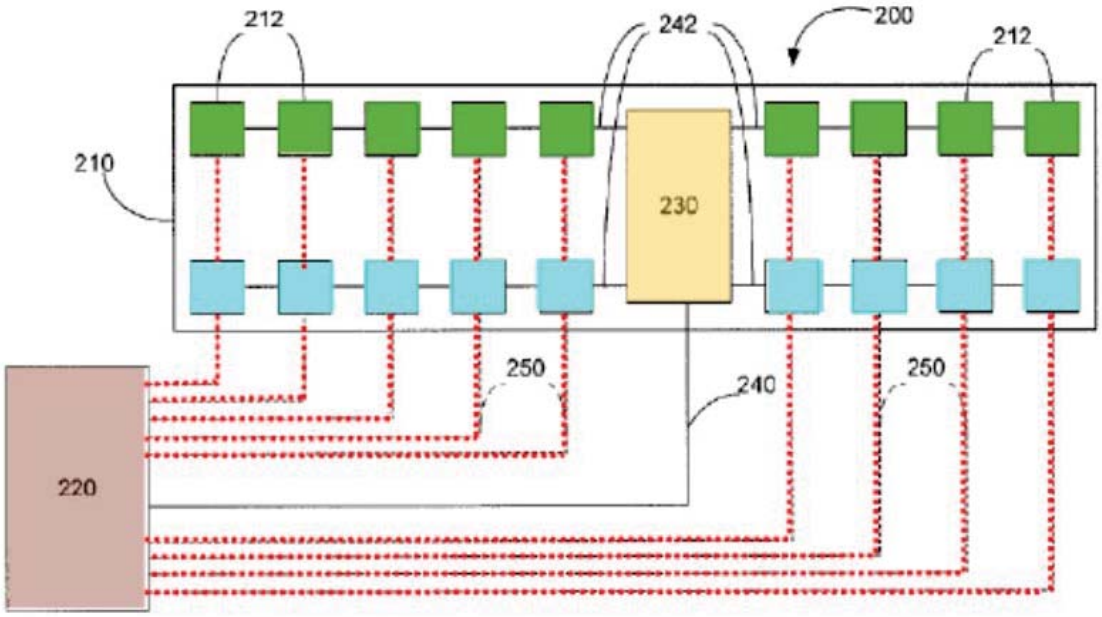
C. The 907 Patent

1. Technical Overview

The 907 Patent is directed to a memory module comprising memory devices, such as dynamic random-access memory (DRAM) or synchronous dynamic random-access memory (SDRAM) devices. Ex.1001 at 1:17-:26; Ex.1003¶¶53-54.

The memory devices on the memory module can be organized into rows or "ranks" (shown in green and blue below). Ex.1001 at 1:36-:42. Such prior-art memory modules were well known, and specific designs were standardized by a consortium called JEDEC. *Id.* at 1:64-:67,4:39-5:13,5:35-6:7,15:12-:14; Ex.1003¶¶55-56.

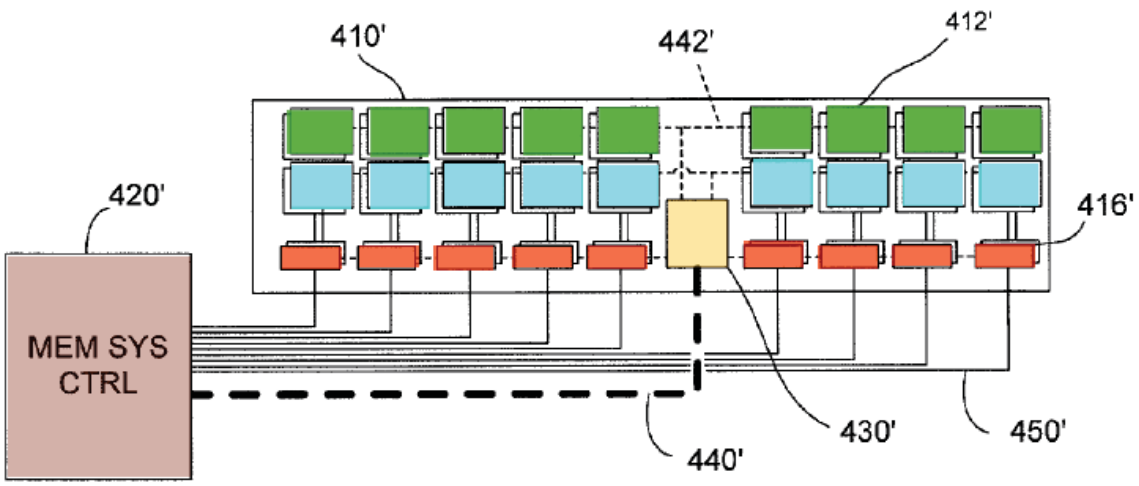
Figure 2A: (Prior Art)



The 907 Patent explains that, in such prior-art systems, increasing memory capacity increases loads within the system "resulting in a slower system." Ex.1001 at 4:7-4:35,6:52-:55; Ex.1003¶¶57-59.

To address this problem, the 907 Patent discloses a "Memory Module with ***Distributed*** Data Buffers." Ex.1001 at Title, Fig.3C (annotated below), 7:35-8:6. The memory module 410' includes multiple ranks of memory devices 412' (green and blue), a control circuit 430' (orange), and multiple data transmission circuits 416' (red) that are "distributed at corresponding positions relative to the at least one printed circuit board … 410′." *Id.* at 8:17-:22; Ex.1003¶¶60-62.

Figure 3C:



The 907 Patent's "Fig. 5 schematically illustrates an example data transmission circuit 416." Ex.1001 at 15:17-:19. Reproduced below are two copies of Figure 5. The copy labeled Figure 5-1 is annotated along with Figure 4A to show the data transmission circuit 416 (red box) selectively allowing data transmission along "path A" to the memory devices in ranks A and C (while selectively isolating the other memory devices in ranks B and D). The version labeled Figure 5-2 is annotated to show the data transmission circuit 416 (red box) selectively allowing data transmission along "path B" to the memory devices in ranks B and D (while selectively isolating the other memory devices in ranks A and C). Ex.1001 at 15:35-:39,15:65-16:16,16:17-:29,17:63-18:2 (path A),18:10-:16 (path B); Ex.1003¶¶63-65. In this way, the data transmission circuit 416 disclosed in the 907 Patent creates what the parties have called a "fork in the road"

for switching between data paths A and B, thereby selectively allowing transmission of data with only the ranks of memory on one "fork" of the road while reducing the load seen by the system memory controller. Ex.1003¶63,66.

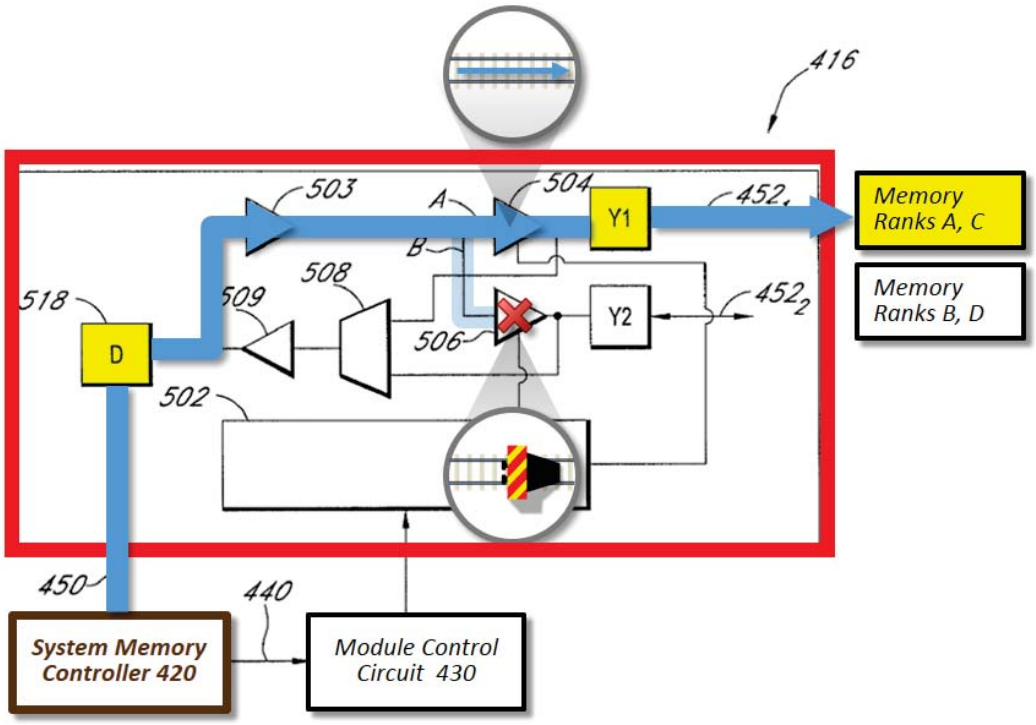


Figure 5-1

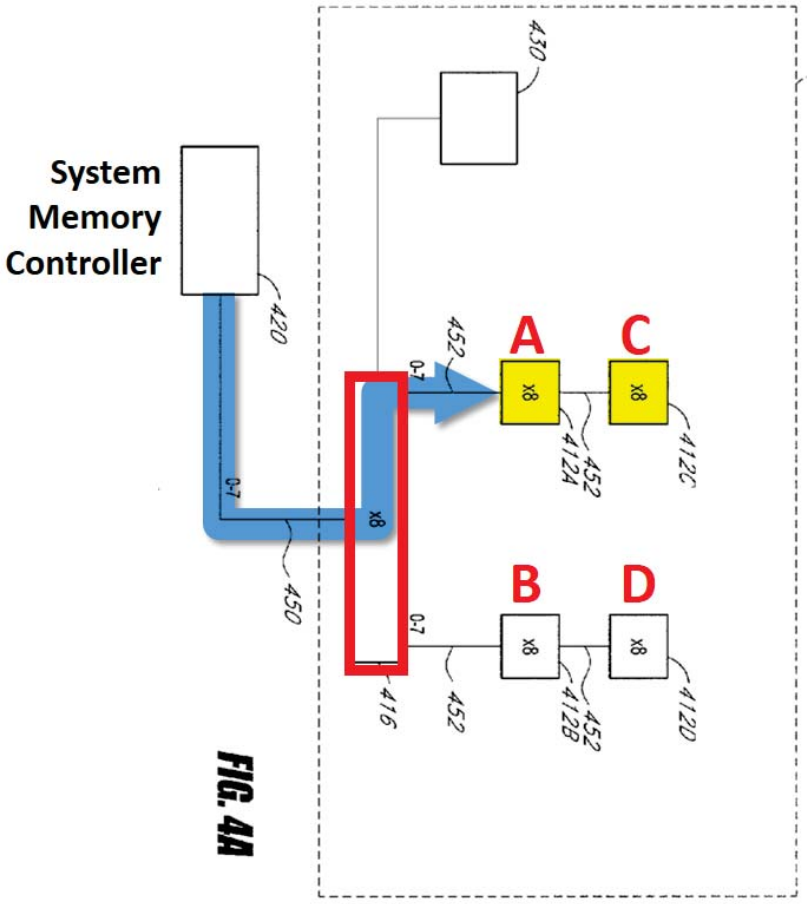

System
Memory
Controller
420
450
430
452
0-7
x8
A
C
B
D
412A
412C
412B
412D
416
FIG. 4A

Figure 4A

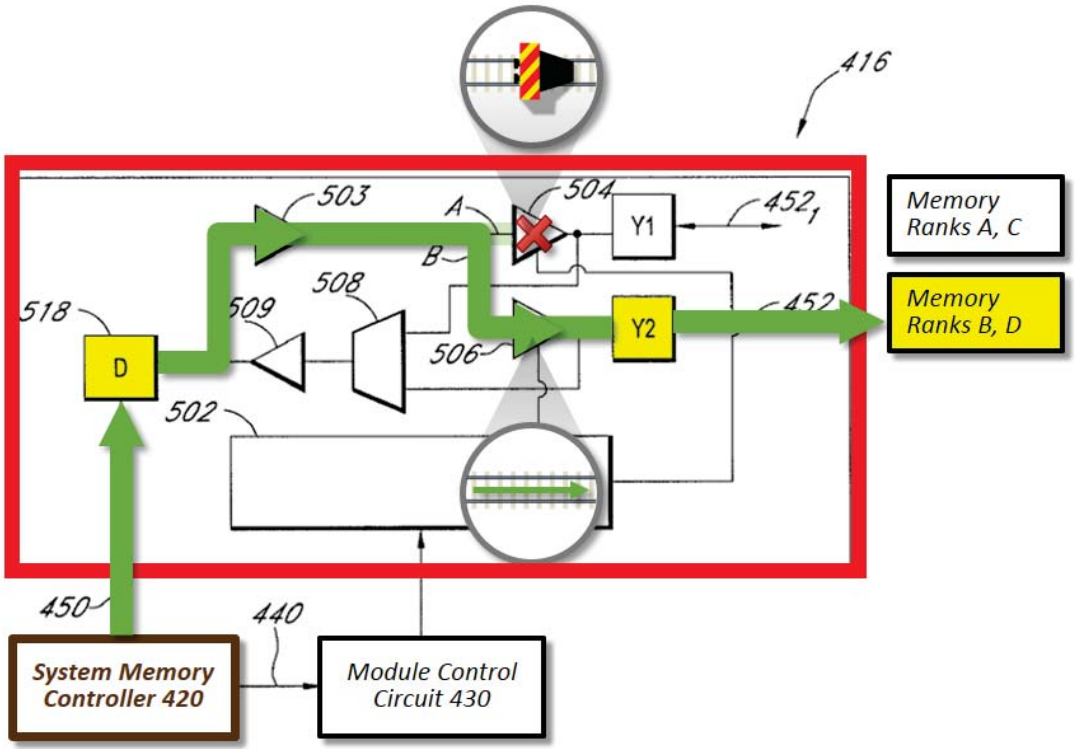


Figure 5-2

2. Summary of the Prosecution History

After the Examiner rejected all claims, including for double patenting over earlier patents in the family (the 870 Patent and the 185 Patent, Exs.1015&1017) and in view of U.S. Patent Application Publication No. 2009/0248969 to Wu et al. ("Wu") (Ex.1021), the applicants filed a terminal disclaimer and also declarations by the inventors asserting conception "prior to March 31, 2008" to swear behind Wu. Ex.1002 at 117-40, 173-310; Ex.1003¶¶100-102.

On June 27, 2016, the examiner issued a notice of allowance for several claims. Ex.1002 at 312-20; Ex.1003¶103. After allowance, however, the

applicants disclosed Halbert (Ex.1006) for the first time, and presented new claims and amendments. Ex.1002 at 338-50,353,358-59,360-88; Ex.1003¶¶104-106.

On October 6, 2016, the examiner allowed some claims, but rejected several of the new claims. Ex.1002 at 389-397. For example, claim 36 was rejected under §112,¶1 for lack of written description. The examiner was concerned that claim 36 could be interpreted to eliminate the "fork in the road" concept discussed above (*see* §V.C.1), which the examiner concluded would be an unsupported interpretation and thus new matter lacking written description. Ex.1003¶107.

After further amendments, cancellation of claims, and addition of new claims (Ex.1002 at 402-35), the examiner allowed all the pending claims on January 13, 2017 (*id*. at 436-41), noting that Halbert was the "closest prior art," but allowing the claims because in "the instant invention … different buffers are enabled and disabled," a reference to the "fork in the road" concept. Ex.1003¶¶109-110. On February 23, 2017, the examiner issued supplemental reasons for allowance (Ex.1002 at 455-59), which noted that the claims also require that the non-selected memory devices "aren't even enabled." Ex.1003¶¶111-112.

The examiner did not address the combination of Halbert and Amidi (Ex.1007) that is the subject of this Petition and was the basis for the institution decision involving the parent patent (Ex.1031).

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction *in light* of the specification, 37 CFR §42.100(b), not the broadest *possible* interpretation, *In re Smith Int'l, Inc.*, 871 F.3d 1375, 1382-83 (Fed. Cir. 2017). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. §112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48,764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. "*isolate memory device load*"

The broadest reasonable construction of the phrase "*isolate memory device load,*" which appears in independent claims 1, 16, 43, 53, and 58, and dependent claim 32 (depending from independent claim 30), is "electrically separate memory device load." Ex.1003¶¶118-125.

The Board has previously interpreted the phrase "selectively isolate" in the 185 Patent (parent to the 907 Patent) to mean "electrically separate one component from another." Ex.1023 at 8. Further, during recent ITC litigation involving the 185 Patent, Patent Owner's expert agreed that "isolation always requires electrical separation." Ex.1024 at 1015:21-23; Ex.1026 at 12; Ex.1029 at 4; Ex.1003¶¶86,89,119.

2. "*the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command*"

The phrase "*the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command*" appears in independent claims 1, 16, and 53. Independent claim 30 has a similar phrase: "*first memory devices … receiving each N-bit wide data signal associated with the first write command, and second memory devices … receiving each N-bit wide data signal associated with the second write command*." The broadest reasonable construction of these phrases is not limited to a single rank outputting or receiving data associated with a read or write command. Ex.1003¶¶135-136.

The claim language above does not require that the "*memory devices*" be in a single rank. It only requires that the "*memory devices*" together "*output or receive each N-bit wide data signal associated with the memory read or write command*." The 907 Patent specification does not limit the targets of a memory access to a single rank either. Ex.1001 at 14:62-15:12,17:67-18:2. Therefore, "*memory devices*" in the claim language above should not be limited to a single rank. Ex.1003¶136.

3. "Fork-in-the-road" vs. "Straight-line" Interpretation

As discussed above, the 907 Patent discloses a "fork-in-the-road" arrangement where, for a given memory access, memory device(s) on one data

path (e.g., path A) are coupled to a common data bus leading to the system memory controller, and other memory device(s) on a different data path (or different "fork" of the road) (e.g., path B) are isolated from that common data bus. Ex.1003¶126. In parallel litigation, however, Patent Owner alleges that the claimed "first" and "second" memory devices are on the ***same*** data path. Ex.1003¶127; *see also* Ex.1034 at 36; Ex.1003¶¶88,91-94,110,112. As depicted in the annotated figure below, under this "straight-line" arrangement, if A is the "first" memory device, then the "second" memory device would be C, rather than B. *Id.* Petitioner believes that interpretation is incorrect, *see* Ex.1003¶¶128-134, but the Board need not resolve this potential claim construction dispute because this Petition shows that the 907 Patent claims are unpatentable over Halbert and Amidi under either the "fork-in-the-road" or "straight-line" interpretation, *id.* ¶128.

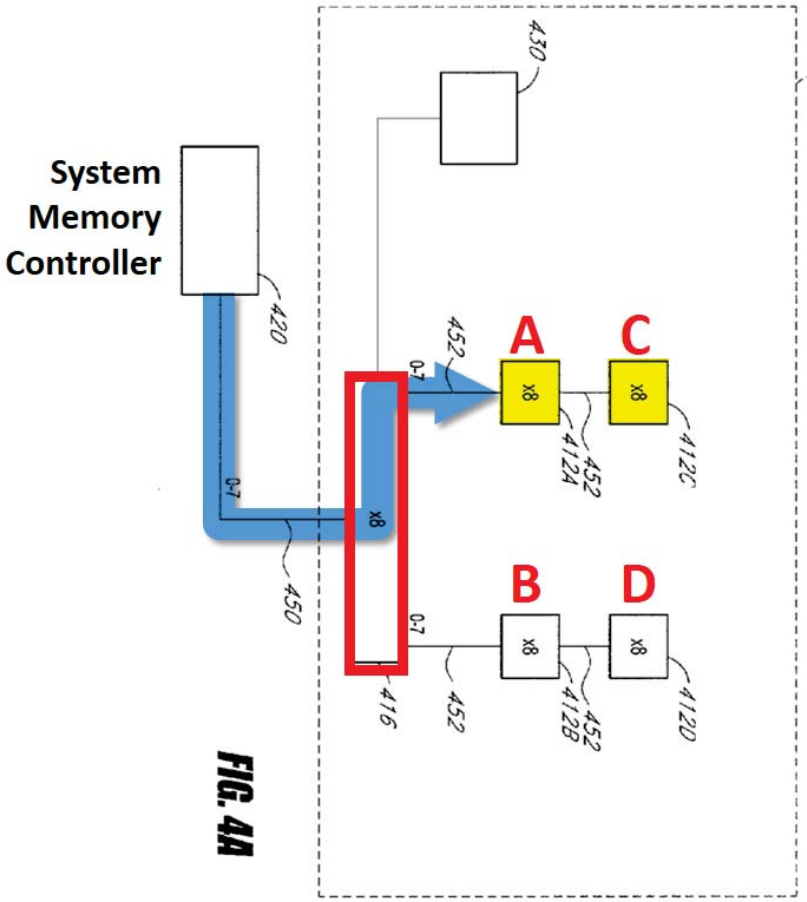


FIG. 4A

VI. Overview of the Prior Art

A. US Patent No. 7,024,518 to Halbert et al. ("Halbert") (Ex.1006)

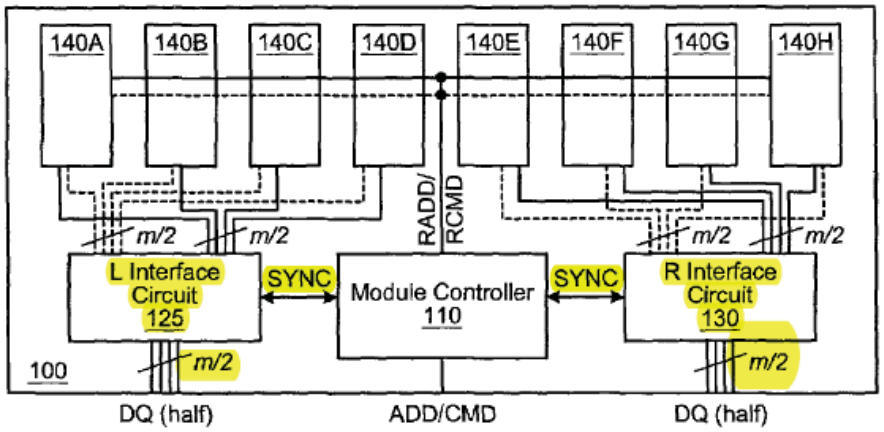
Halbert issued as a patent on April 4, 2006. Ex.1006, Cover. Halbert is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b).

Halbert recognized that a "dual-bank" memory module was cheaper than two "single-bank" memory modules. Ex.1006 at 3:32-:41. But increasing the number of memory devices would increase the load "that a memory device (or the

controller) sees when it drives the bus …, this capacitance may make it infeasible to drive signals reliably on the bus." *Id.* at 4:20-:22.

To solve this problem, Halbert discloses an improved memory module that "allow[s] the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." *Id.* at 3:67-4:2; Ex.1003¶170. Like the 907 Patent, Halbert discloses distributing buffers (what Halbert calls "interface circuits") along the bottom edge of the memory module:

Fig. 7



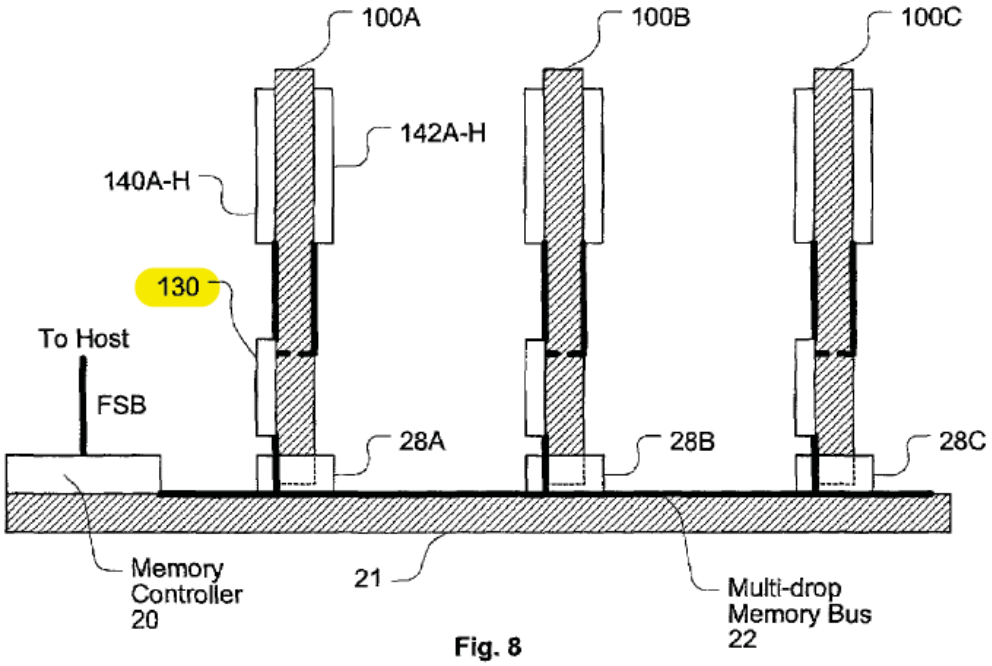
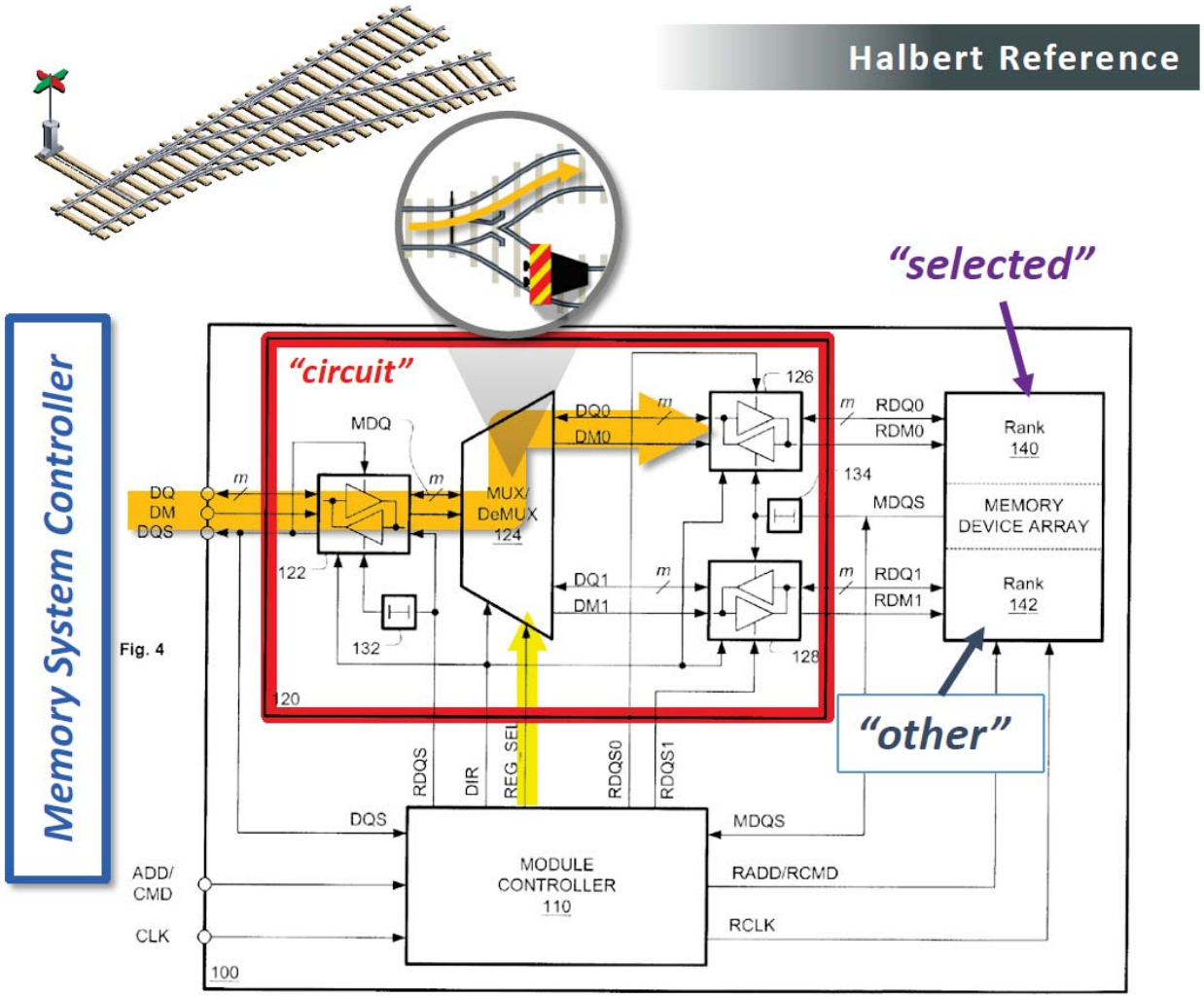


Fig. 8

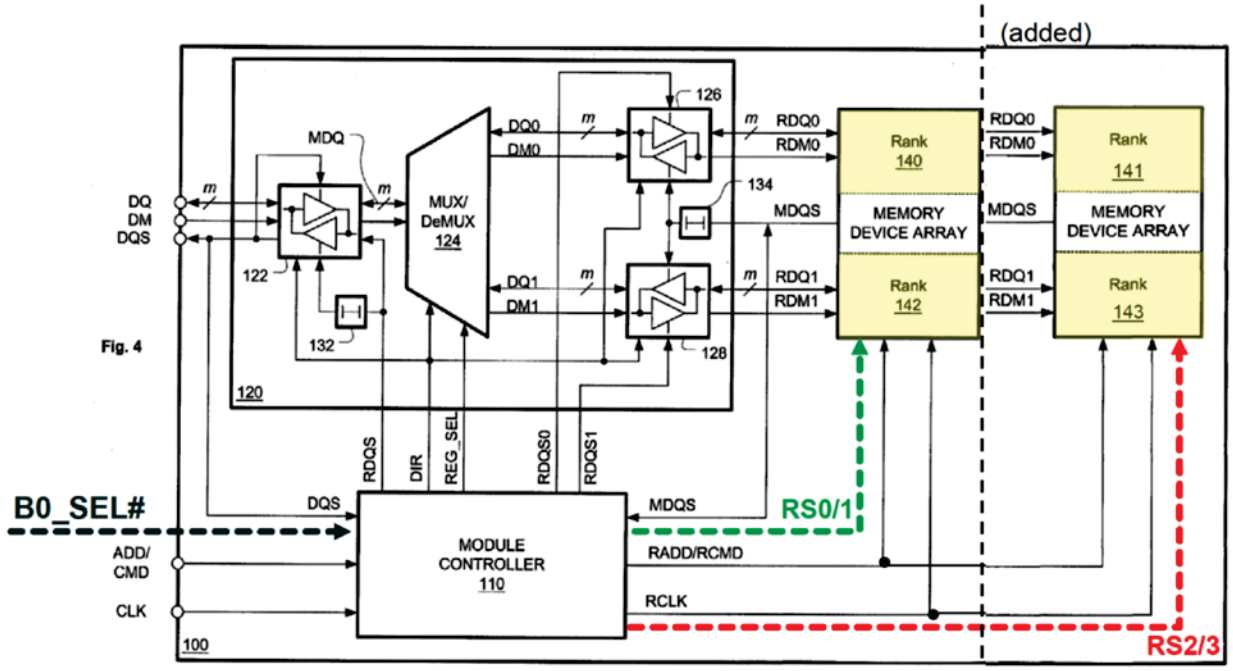
Each of the interface circuits 125 and 130 (shown in Fig.7 above) can be implemented as a circuit which is almost identical to the data interface circuit 120 of Halbert's Fig.4 (reproduced below with annotations) except that the number of data signal lines is split in half, i.e., interface circuit 120 in Fig.4 has 'm' DQ lines connecting to the data bus, while each of the Left and Right Interface Circuits 125 and 130 in Fig.7 has only half of those data signal lines, 'm/2'. Ex.1006 at 7:37-40; Ex.1003¶173. As shown below, Fig.4 of Halbert discloses that MUX/DeMUX 124 creates a "fork in the road" that routes data to a selected rank of memory while isolating the other (not selected) rank of memory:



Ex.1006 at 5:51-:65, Fig.4; Ex.1030 at 12; *see also* Ex.1029 at 11-16; Ex.1003¶175.

Halbert also discloses alternative implementations. For example, Halbert explains that its "illustrated examples … show two ranks of memory, but other numbers of ranks are also possible, e.g., a 4:1 multiplexer and four ranks of memory." Ex.1006 at 9:20-:35; Ex.1003¶177.

As discussed below, the combination of Halbert and Amidi renders obvious the arrangement shown below, where there are four ranks of memory (yellow) rather than just two. This arrangement satisfies the "straight line" interpretation of the 907 Patent because there are multiple memory devices on the same data path, with one enabled by a chip select signal and the other not.



B. U.S. Pat. App. Pub. No. 2006/0117152 to Amidi et al. ("Amidi") (Ex.1007)

Amidi was published on June 1, 2006. Ex.1007, Cover. Amidi is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b).

Amidi discloses a ***four*** rank memory module that appears to the system memory controller to only have ***two*** ranks (and thus only needs ***two*** chip select signals). Amidi explains that "[b]ecause memory devices with lower densities are

cheaper and more readily available, it may be advantageous to build … memory module using lower densities devices." Ex.1007¶[0008]. "A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed." *Id.* ¶[0011]; Ex.1003¶180.

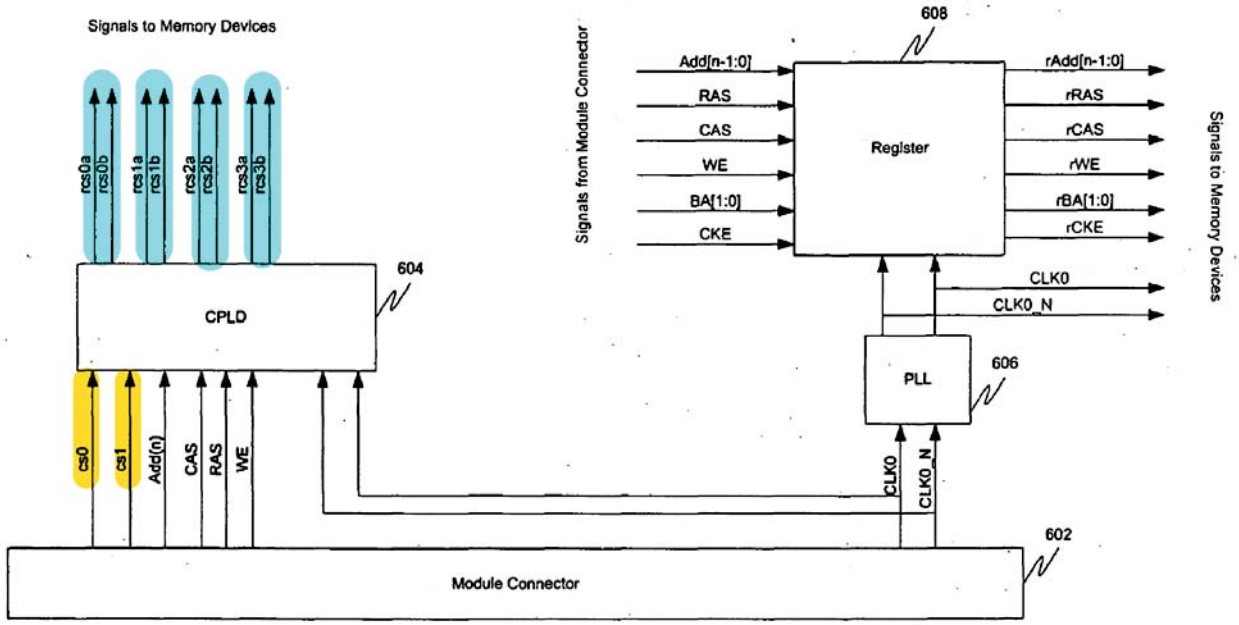
Amidi's memory module includes a "[Complex Programmable Logic Device] CPLD 410 [which] emulates a two rank memory module on the four rank memory module 400. . . . The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410." Ex.1007¶[0041], Fig.4A; Ex.1003¶182.

For a read or write operation, Amidi's CPLD determines which of the four ranks is active based on the first and second chip select signals CS0 and CS1, and the highest row address bit Add(n), as depicted in the table of FIG. 5 (below). Ex.1007¶[0043], Fig.5; Ex.1003¶183.

Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

Amidi's CPLD "ensures that all commands for a two rank memory module conveyed by the module connector 602 are also performed on the four rank

memory modules." Ex.1007¶[0052]. Amidi's CPLD uses command signals such as CAS, RAS, and WE in addition to the chip select signals cs0 and cs1 and the row address, and generates four chip select signals rcs0, rcs1, rcs2, and rcs3 (one for each rank) as shown in the detailed block diagrams of Amidi's FIG. 8 and FIG. 6A (reproduced below with annotations highlighting the two received chip selects in orange and the generated four chip selects in light blue). Ex.1003¶184.



Row Address Decoding
FIG.6A

C. U.S. Patent No. 7,334,150 to Ruckerbauer et al. ("Ruckerbauer") (Ex.1038)

Ruckerbauer issued as a patent on February 19, 2008. Ex.1038, Cover. Ruckerbauer is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b). Ruckerbauer discloses a memory module that includes a plurality of memory

chips, bus signal lines, and a register circuit connected to the bus signal lines. Ex.1038, Abstract. Ruckerbauer discloses that its register circuit is mounted in the middle of a memory module such that, from the register, "command and address signals run via … signal lines … on the … memory module to the … memory chips … to the left and the right of the … memory module." Ex.1038 at 4:57-62, Figs.1-2.

D. Microcomputer Interfacing by H. Stone ("Stone") (Ex.1035)

Stone is a book published in 1982. Stone is prior art to the 907 Patent pursuant to 35 U.S.C. §§102(a)&(b). Stone describes various techniques and issues related to interfacing different components of a computer system. Chapter 4 of Stone is specifically directed to accessing computer memories, including the use of bidirectional buffers. Ex.1035 at 133, Fig.4.7.

E. U.S. Pat. App. Pub. No. 2006/0262586 to Solomon et al. ("Solomon") (Ex.1008)

Solomon is titled "Memory Module with a Circuit Providing Load Isolation and Memory Domain Translation" and published on November 23, 2006. Solomon is prior art to the 907 Patent under 35 U.S.C. §§102(a),(b). One of the named inventors on Solomon is also a named inventor on the 907 Patent, and many concepts in the 907 Patent came from Solomon. Ex.1003¶¶49-52. Solomon discloses a memory module that includes memory devices coupled to a circuit that

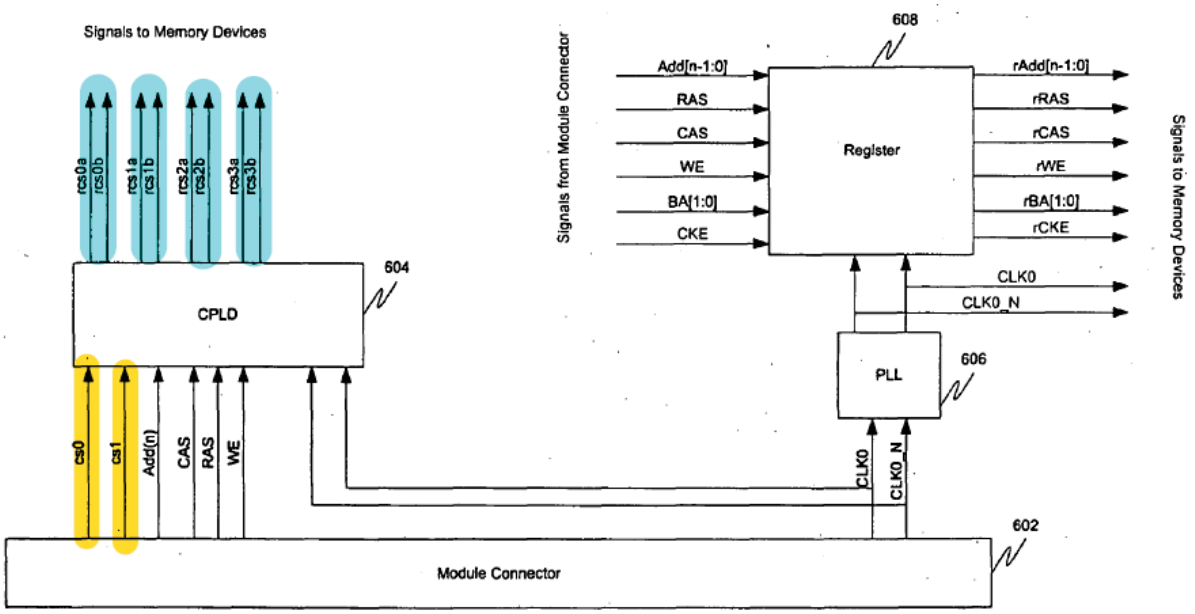
"selectively isolates one or more of the loads of the memory devices from the computer system." Ex.1008¶[0040],Fig.1.

VII. Precise Reasons for Relief Requested

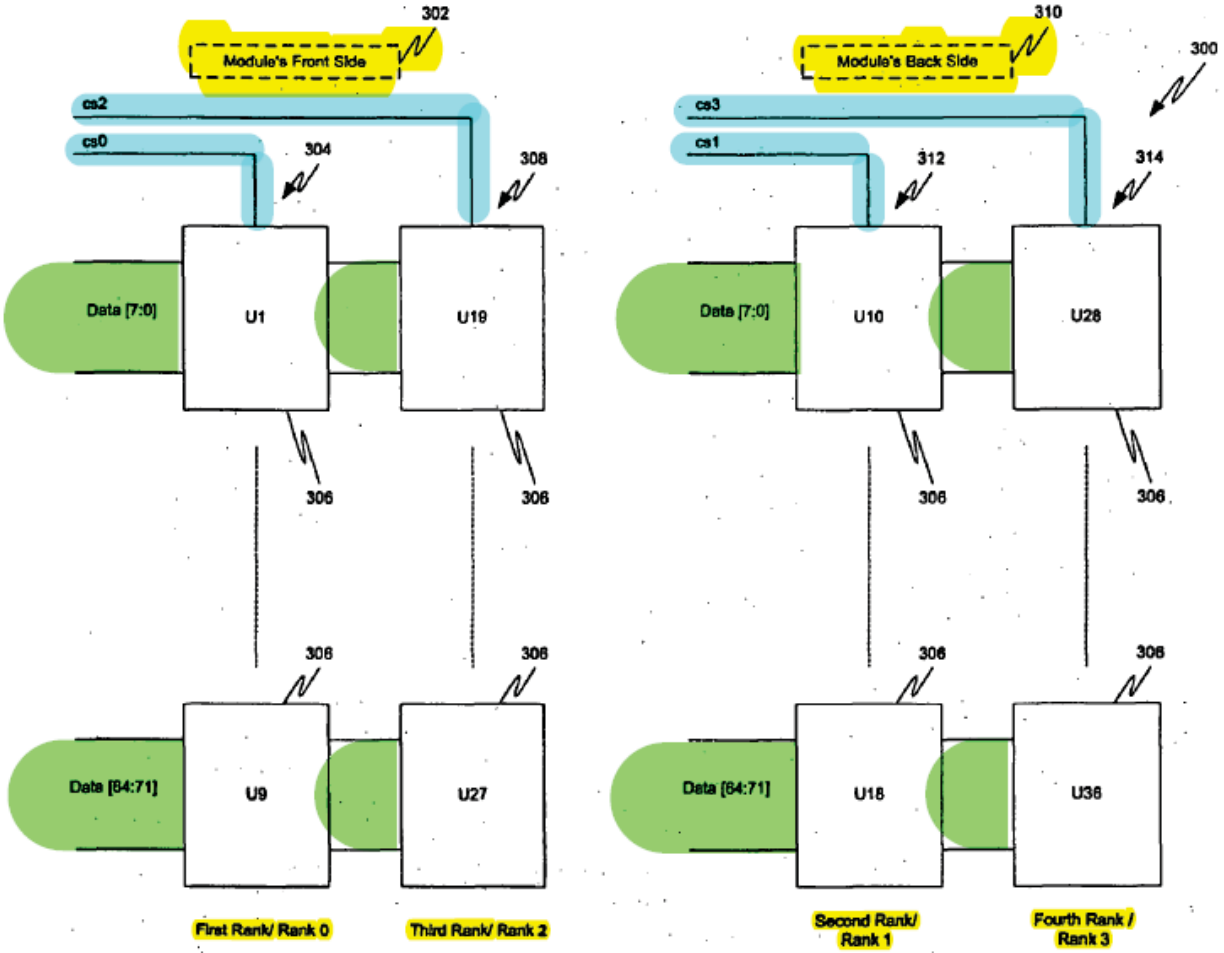
A. It was obvious to increase the capacity of Halbert's (Ex.1006) module by adding two more ranks as disclosed in Amidi (Ex.1007)

Memory modules at the time, like Halbert's, were designed to have one or more "ranks" of memories such that they were compatible with the existing memory buses and memory controllers. Ex.1006 at 3:55-57; Ex.1003¶¶205-206. Thus, Halbert's statement that "other numbers of ranks are also possible, e.g., … four ranks of memory," Ex.1006 at 9:20-27, would have motivated Skilled Artisans to find known, reliable designs, including Amidi's, for adding such ranks. Ex.1007; Ex.1008; Ex.1005; and Ex.1010 (standardized RDIMMs with one and two ranks). Combining Amidi's techniques with Halbert's would have doubled the capacity of Halbert's module at a low cost and maintained compatibility with the existing memory buses and controllers, which would have further motivated such a combination. Ex.1003¶¶207-208; Ex.1006 at 3:32-52; Ex.1007¶[0008]. This obvious combination of Halbert in view of Amidi is referred to as the "Halbert-Amidi combination" throughout this Petition. As discussed below, the Halbert-Amidi combination can be operated with or without rate doubling (*see* Sections 1&2 below).

Amidi and Halbert are analogous art directed to the problem of efficient support of multi-rank memory modules, like the 907 Patent. Ex.1001 at 1:17-2:21; Ex.1006 at 1:16-2:60,3:32-4:35; Ex.1007¶¶[0001-11]; Ex.1003¶209. Amidi's four-rank memory module receives control signals, including two chip selects (cs0, cs1), from which a CPLD generates four chip selects, one for each rank. Ex.1007¶¶[0034-36,'41,'44,'60,'61], FIGS. 6A&3 (annotated below); Ex.1003¶¶210-211.



Row Address Decoding
FIG.6A



Transparent Four Rank DDR Module Block Diagram
FIG. 3

Here, the "*data lines*" (green) are shared by ranks receiving separate chip select signals—which was a well-known, reliable way to add ranks. Ex.1007 at Fig.3, ¶[0034]; Ex.1010 at 12; Ex.1003¶212. Thus, it was obvious to employ the additional memory ranks and chip-select functionality of Amidi in Halbert in a combination where Amidi's chip select functionality is implemented in Halbert's module controller 110 and the chip select signals are directly coupled to individual

ranks, where the additional ranks share the data lines with Halbert's original ranks similar to the design in Amidi. Ex.1003¶¶213,218; Ex.1007 at Fig.3.

The additional ranks 141 and 143 could be stacked on the respective ranks 140 and 142 to "solve the placement problem." Ex.1007 at Abstract, ¶[0010], Figs.4A-4B; Ex.1006 at Fig.8 (annotated below); Ex.1003¶219. This was a well-known, predictable technique with efficient use of real estate on the module. Ex.1010 at 15,20,21,29,35; Ex.1003¶220.

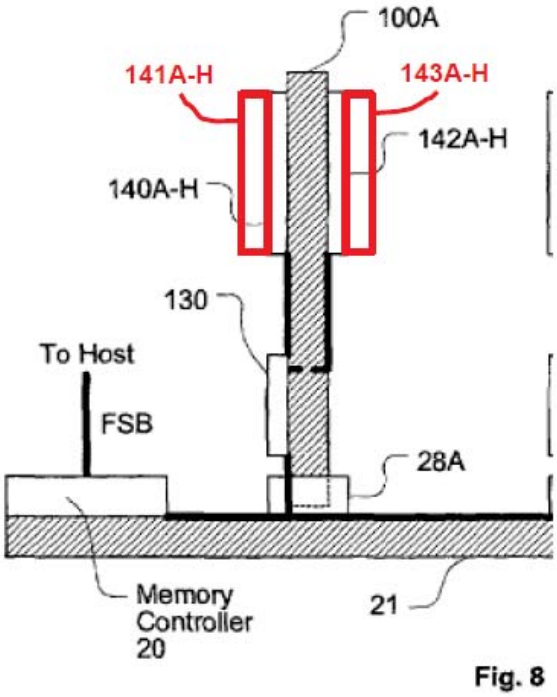
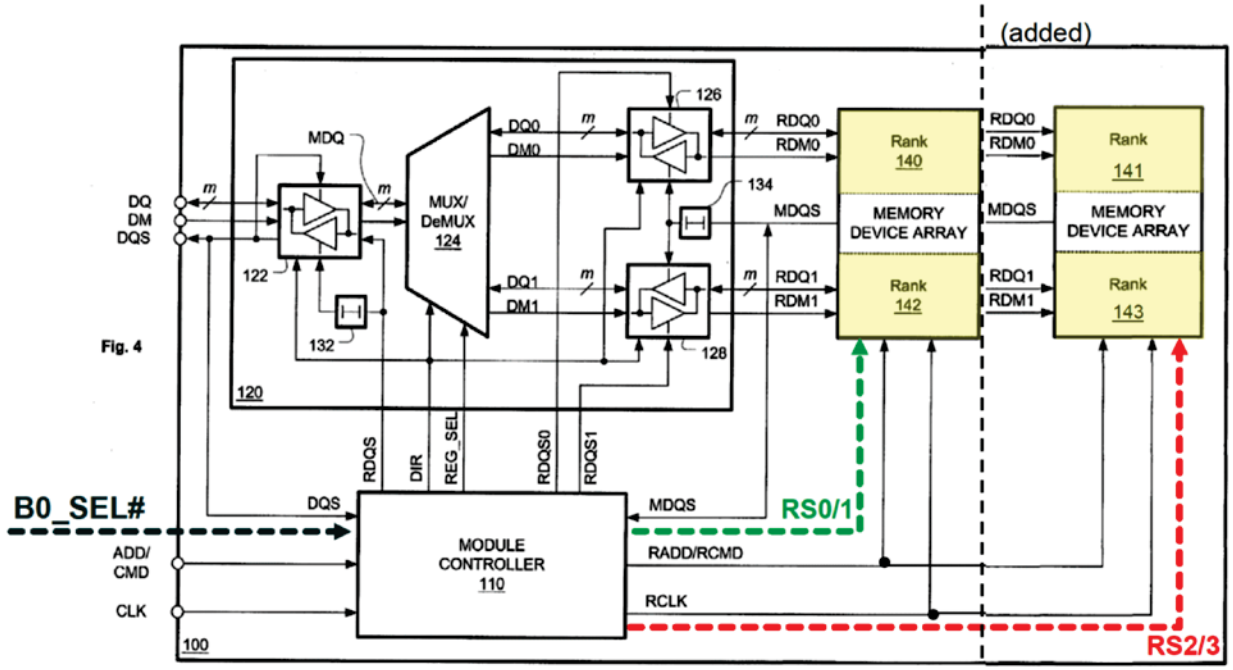


Fig. 8

1. Halbert-Amidi combination with rate doubling

Halbert's module 100 can be advantageously expanded with two additional ranks 141 and 143 using Amidi's technique in a way that is "compatible" with how the chip select signal B0_SEL# is used in Halbert's system, as shown in the

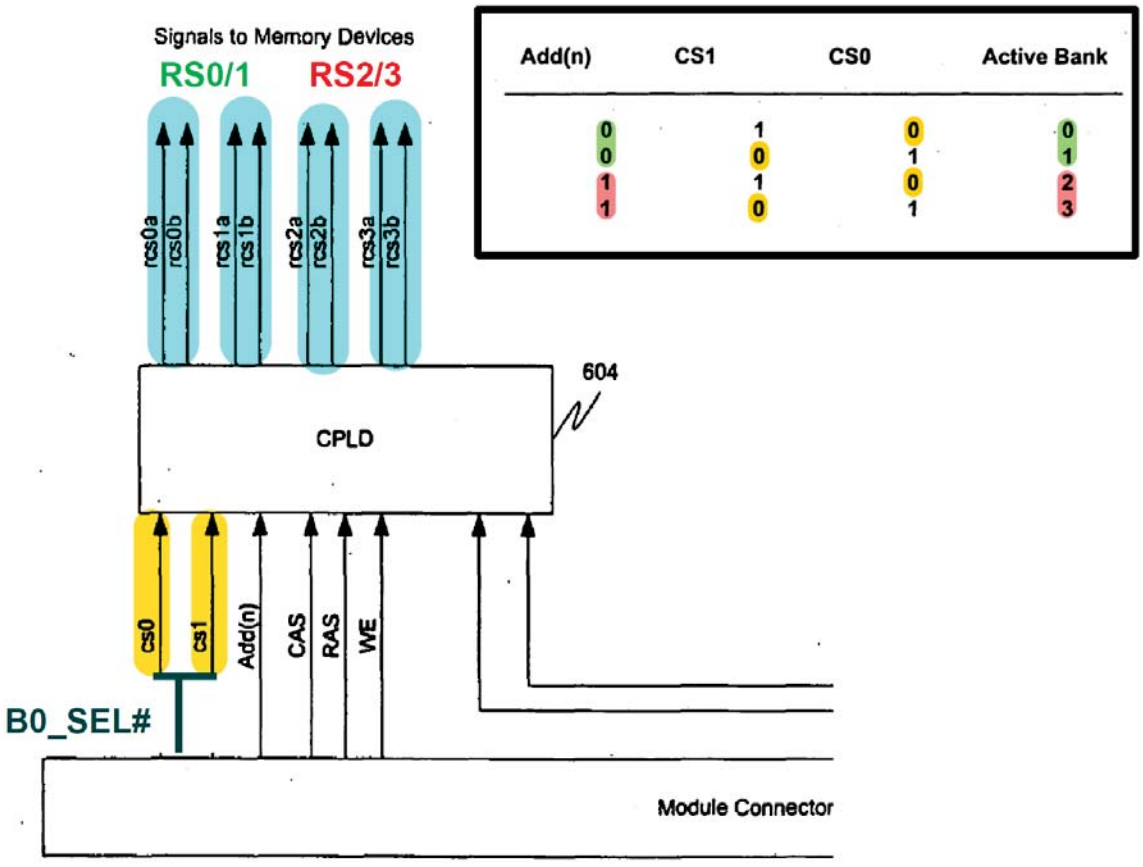
modified Fig.4 of Halbert below. Ex.1006 at Fig.3, 3:55-57,6:1-4; Ex.1008¶[0011]; Ex.1003¶¶214,215.



As shown above, Halbert's module controller 110 is modified to generate four chip select signals, RS0, RS1, RS2, and RS3 from the chip select B0_SEL# and address signals of the existing memory bus as explained by Amidi. Ex.1003¶216. The chip selects RS0 and RS1 select ranks 140 and 142 the same way as in Halbert's preferred embodiment, which doubles the memory devices' data rate. Ex.1006 at Figs.5,6. Additional ranks 141 and 143 are selected by chip selects RS2 and RS3, share the RDQ0 and RDQ1 (and MDQS) buses with ranks 140 and 142, and operate substantially the same way as those ranks.

In the cited combination, Halbert's module controller 110 includes Amidi's CPLD functionality which receives B0_SEL# on two of its inputs, cs0 and cs1, and

generates chip selects RS0-RS3 (corresponding to Amidi's rcs0-rcs3). Ex.1007, Figs.5,6A (annotated below); Ex.1006 at 5:63-65,6:21-37; Ex.1003¶¶216,217,221. When B0_SEL# is asserted ("logic 0"), both cs0 and cs1 are asserted ("logic 0") and row address bit Add(n) selects whether ranks 0 and 1 (RS0/1) or ranks 2 and 3 (RS2/3) are activated. *Id.*; Ex.1007 FIG.8 (block diagram of the CPLD); Ex.1003¶222. Amidi's Load Mode Register, Auto Refresh, and Auto Pre-Charge functionalities in the CPLD would also operate the same way as disclosed in Amidi. Ex.1007 at FIG.8, ¶¶[0052],[0064-68]; Ex.1003¶224.



The Halbert-Amidi combination would advantageously double the capacity of Halbert's module and remain "compatible with an existing memory controller/bus" which uses only B0_SEL# to activate the module, like in Halbert. Ex.1006 at 3:55-57,6:1-4; Ex.1007 at FIGS.3,6A; Ex.1003¶¶223,226. The combination would have been only the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than one would expect from such an arrangement, i.e., the predictable result of operating each rank at desired times. Ex.1003¶225. Here, the module controller 110, the data interface circuit 120 (and 125 and 130), the ranks 140 and 142, and the additional ranks 141 and 143 when activated, operate to double the data rate of Halbert. Ex.1006 at 3:60-64,5:66-7:30, Figs.5,6; Ex.1003¶¶227,232. The module controller 110 generates the chip select signals in accordance with the operation of Amidi's CPLD with a slight modification of inputting the B0_SEL# signal to both of the cs0 and cs1 inputs. Ex.1003¶¶228,233. This is a straightforward application of Halbert's rate doubling and Amidi's selection rules allowing the additional ranks to be controlled using the existing bus. Ex.1003¶¶229-230. The combination uses only known technology that would work as in the prior art. *See* Ex.1007, Ex.1008, Ex.1005, Ex.1010 (disclosing techniques for adding ranks), Ex.1003¶231. A Skilled Artisan therefore had reasons, and would have been

motivated, to make the combination, and doing so would have been well within the level of ordinary skill.

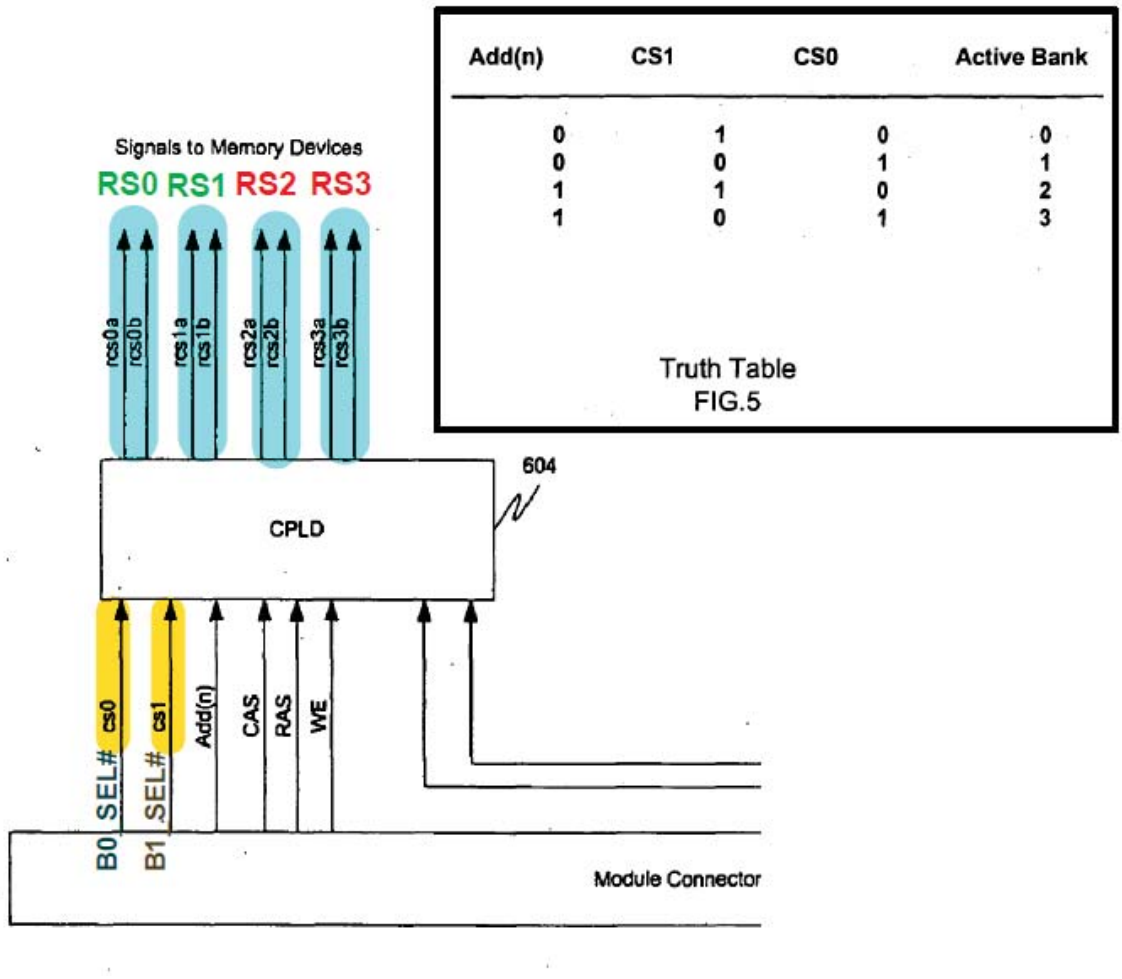
Although the combination could be further simplified in some respects, the Skilled Artisan would have been motivated to keep the separate chip select lines for each rank as disclosed by Amidi even when two ranks are activated "concurrently." Ex.1006 at 4:57-59. This avoids extra load of the additional ranks on the chip select lines so that "it is possible to reach the speeds required for transferring the [command and address] … signals." Ex.1038 at 2:24-2:36; Ex.1003¶234.

Therefore, the Halbert-Amidi combination configured with rate doubling functionality would have been obvious and would perform as in the prior art to provide nothing more than what was expected from it. Ex.1003¶235.

2. Halbert-Amidi combination without rate doubling

It would also have been obvious to implement the Halbert-Amidi combination in a manner that permitted operation ***without*** doubling the data rate of the memory devices. Ex.1006 at 3:42-64,4:57-59 (concurrent operation happens "generally"), 9:66-10:1; Ex.1007¶[0072]; Ex.1003¶¶236,237. To provide such functionality, Amidi's CPLD functionality would operate in Halbert's module controller 110 as described above, but use *both* chip select signals B0_SEL# and

B1_SEL# as the respective inputs cs0 and cs1 to activate only one of the ranks 140-143 for a read or write operation. *Id.*; Ex.1007 at FIGS.5,6 (annotated below).



Here, Halbert's module controller 110 would be additionally modified to include the ability to enable only the data path of the activated rank. Ex.1003¶241. This modification was well within the level of skill, since Halbert explains how to activate those data paths and the additional ranks 141 and 143 are connected to the same data paths. Ex.1006 at Fig.4, 5:23-65. Making the path selection to be the same for an entire data access, i.e., without alternating each clock cycle, was

straightforward as it required only to maintain an already known configuration for a longer time. Ex.1003¶242. Halbert also discloses counters which may be used to determine the duration of the control. Ex.1006 at 6:11-:14; Ex.1003¶242. Techniques for implementing such a system were also disclosed by Ellsberry. *See* Ex.1005. Therefore, this would be a combination of known elements performing as in the prior art and providing reliable results, and within the level of ordinary skill in the art.

Skilled Artisans would have been motivated to implement the Halbert-Amidi combination with this additional functionality (*i.e.*, the ability to operate without rate doubling) because Halbert's module can be implemented using "double-data-rate" or "quad-data-rate" SDRAM devices which could match the "full speed of the memory system data bus" so that no further data rate doubling would be required in an "existing" system employing such memory devices. Ex.1006 at 3:42-57, 9:55-62. Halbert's load isolation, however, would still help "to drive signals reliably on the bus" at those "double-data-rate" and "quad-data-rate" speeds. Ex.1006 at 4:9-26; Ex.1003¶239. It would also "improve upon the multi-drop memory bus architecture by isolating the memory devices on each module from the bus." Ex.1006 at 4:23-27; Ex.1003¶238. These advantages for such a design were also described by Ellsberry. Ex.1005¶¶[0012],[0027],[0031]. Thus,

the Halbert-Amidi combination can also be advantageously configured without rate doubling.

B. Claims 30-57 of the 907 Patent are unpatentable as being obvious over Halbert (Ex.1006) in view of Amidi (Ex.1007)

The numbering of the claim limitations below corresponds to that set forth in **Attachment C**.

1. Claim 30

a) [30.a] – "A memory module …"

Claim 30 requires a "*memory module having a data width of N bits and configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines*." Ex.1003¶¶187-204,455-456.

Halbert discloses a "*memory module*" 100, such as a Dual Inline Memory Module (DIMM). Ex.1006 at Figs.7-8(annotated below),2:8-14,3:11-14,7:31-61,11:26-29(claim 9). Halbert's memory module, like a DIMM in general, is "*configured to communicate with a memory controller*" through an edge connector with electrical contacts along an edge of a circuit board which, when inserted in a memory socket 28A-C, form electrical connections to a memory bus 22 coupled to the system memory controller 20. Ex.1003¶187.

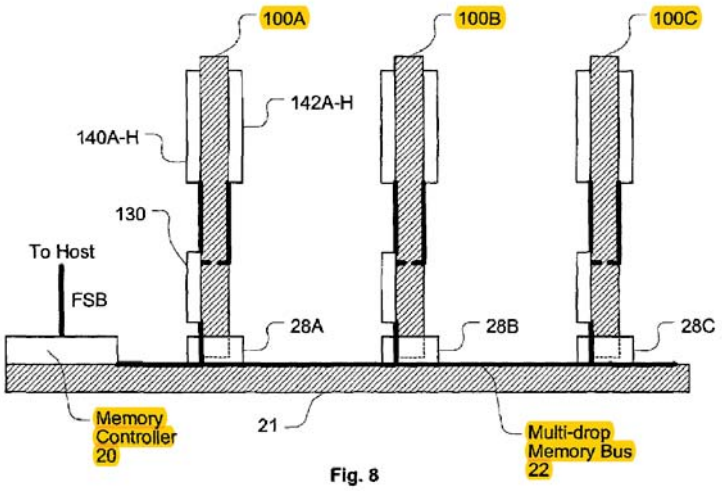
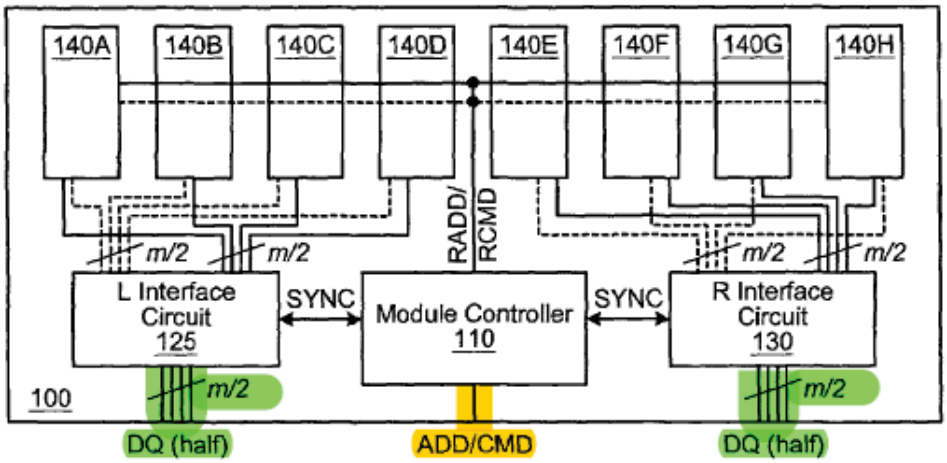


Fig. 8

Memory controller 20 and multi-drop memory bus 22 include "an existing memory controller/bus" which Halbert's memory module 100 is "compatible" with. Ex.1006 at 1:31-2:60,3:55-57,6:1-4,Figs.1-3. Ex.1003¶¶190,191.

The memory module 100 includes an "[i]nterface circuit 120 of FIG. 4 [which] is split into two identical interface circuits (left circuit 125 and right circuit 130) in FIG. 7, each handling half of the data lines." Ex.1006 at 4:36-39, 7:37-40. Thus, Halbert's module has two ("*plurality of*") sets of "*data signal lines*" ("DQ(half)", green), handled by respective left and right circuits 125 and 30. Ex.1003¶¶188,189,198; Ex.1006 at 7:37-40, Fig.7(annotated below).

Fig. 7



The module's edge interface also includes a set of address and command lines ("ADD/CMD", orange; "*a set of control signal lines")* consistent with, and directly corresponding to those in well known, standardized registered DIMMs. Ex.1006 at 1:40-60,2:23-60,Figs.2-3,7(annotated above); Ex.1009 at 7; Ex.1011 at 6; Ex.1010 at 7-8,12; Ex.1003¶¶192-197.

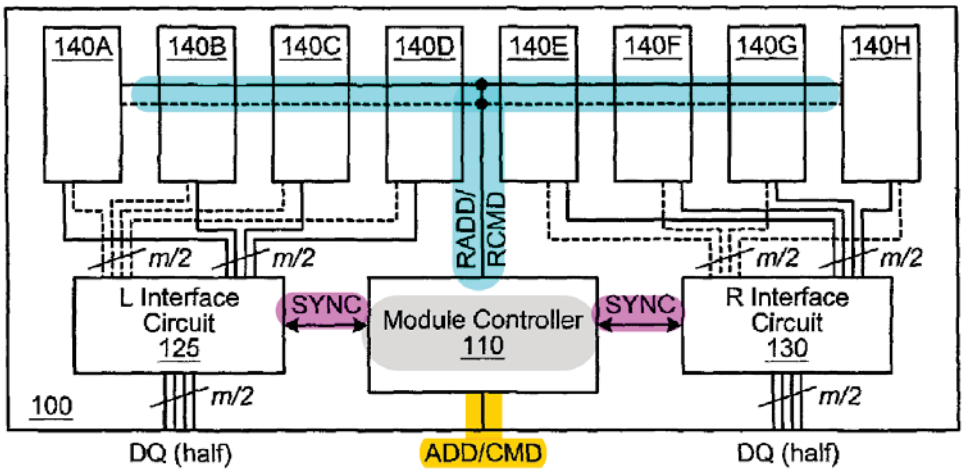
b) [30.b] – *"a module control circuit …"*

Claim 30 further requires "*a module control circuit configured to receive from the memory controller via the set of control signal lines first input address and control signals corresponding to a first write command and subsequently second input address and control signals corresponding to a second write command, the module control circuit producing first output address and control signals and first module control signals in response to the first input address and control signals, the module control circuit producing second output address and*

control signals and second module control signals in response to the second input address and control signals, the second module control signals being different from the first module control signals."

Halbert discloses a memory module including "*a module control circuit configured to receive from the memory controller via the set of control signal lines first input address and control signals.*" Ex.1003¶¶245-247,458-461. Halbert's module includes a module controller 110 ("*a module control circuit*") receiving address and control signals on the ADD/CMD input control signal lines from the memory controller ("*configured to receive from the memory controller via the set of control signal lines first input address and control signals*"). Ex.1006 at 3:11-14,5:28-30 6:1-4,6:66-7:2,7:31-61, Figs.4-6,7(annotated below); Ex.1003¶¶245,192-193. Module controller 110 can receive a second set of control signals for a second a memory access. *Id*.

Fig. 7



In response, module controller 110 provides "*first"* and *"second" "output address and control signals*" on the RADD/RCMD bus (light blue) and "*first"* and *"second" "module control signals*" on the SYNC bus (purple). *Id*.

Halbert (as well as Amidi) discloses that the input address and control signals can correspond to one or more write commands. Ex.1003¶¶248-251,459; Ex.1006 at 6:4-8, Fig.6. In the Halbert-Amidi combination, Ex.1003¶¶205-243, different write commands can be directed to the original ranks (140, 142) or to the additional ranks (141, 143). Ex.1006, at 6:1-4; Ex.1003¶¶214-216,221-223,236-242,460.

In the Halbert-Amidi combination, the "*module control circuit*" produces "*first*" and "*second" "output address and control signals*" and "*module control signals*" in the manner required by limitation [30.b]. *See* Ex.1003¶¶462-472. In response to the "*first"* and *"second" "input address and control signals*," Halbert's modified module controller 110 provides address and command signals, including respective chip select signals, to memory ranks 140-143 ("*first"* and *"second" "output address and control signals*"), and control signals (SYNC) for the interface circuits 125 and 130 ("*first"* and *"second" "module control signals"*). Ex.1003¶¶253-262,463,464.

The Halbert-Amidi combination also includes "*second module control signals*" that are "*different from the first module control signals*" under the fork-in-

the-road interpretation. Halbert's controller 20 can use masking signals to write a single first data word into rank 140 with the first write command and a second data word into rank 142 with the second write command. Ex.1003¶¶270,271,465; Ex.1006 5:51-65,9:46-54, Fig.4. As the two data words pass through different paths, the corresponding module control signals (SYNC) are different. Similarly, in the Halbert-Amidi combination without rate doubling, the first write command targets rank 140 while the second write command targets rank 142, and the data paths are configured differently, and the corresponding module control signals are also different. *Id.* Ex.1003¶¶236-242.

In the Halbert-Amidi combination, the "*first module control signals*" are different from the "*second module control signals*" even under Patent Owner's straight-line interpretation where the first and second memory devices are coupled to the same data bus. Ex.1003¶¶126-134,467. In Halbert's "burst mode access," Ex.1006 6:10-14, controller 20 can set and alter the length of the data burst. Ex.1011 at 9,10. Thus, Halbert's module with the additional ranks can receive two write commands, one with a burst length directed to rank 140 and another one with a changed burst length directed to rank 141. Because of the difference in burst lengths, the "timing and synchronization signals" ("*module control signals*") would be different for the first and second write operations. Ex.1003¶¶468-469; Ex.1006 at 4:45-47,5:51-58,6:11-14. Similarly, the CAS and Additional latency

values may also change, leading to different timing for the first and second memory accesses. *See* §2 below; Ex.1003¶¶342-355,470; Ex.1011 at 10,22. Skilled Artisans would have been motivated to make such changes in the length and timing of Halbert's data bursts because those can be optimized for different operations and the corresponding standards specifically allow these changes. Ex.1003¶471, Ex.1011 at 10.

***c) [30.c]** – "memory devices …"*

Claim 30 further requires "*memory devices coupled to the module control circuit, the memory devices including first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command, and second memory devices responding to the second output address and control signals by receiving each N-bit wide data signal associated with the second write command*." Ex.1003¶¶264-278,473-474.

Halbert's ranks 140 and 142 include "*memory devices coupled to the module control circuit*" through the RADD/RCMD bus carrying the "*first"* and *"second" "output address and control signals.*" Ex.1006 at 7:31-53,9:55-65, Figs.4,7,8; Ex.1003¶¶265-266. In the Halbert-Amidi combination, the additional ranks 141 and 143 are also coupled to the module controller and receive the "*first"* and *"second" "output address and control signals*" on the RADD/RCMD bus. Ex.1003¶¶205-243.

Halbert further discloses concurrent memory operation of ranks 140 and 142 ("*first memory devices*") which "*respond[] to the first output address and control signals*" by each accessing m bits of data ("*each N-bit wide data signal associated with the first write command"*) on the RDQ0 and RDQ1 buses. Ex.1006 at 4:57-59, Figs.4-6. In response to a WRITE command (e.g., at T4 in Fig.6), the memory devices in rank 140 receive m bits ("DI_a1") on RDQ0, and those in rank 142 receive m bits ("DI_a2") on RDQ1. *Id*. at Figs.4,6, 6:66-7:30. Thus, ranks 140 and 142 receive each m bit-wide data associated with a write command. Ex.1003¶267. Subsequently, the system memory controller can write data to additional memory ranks 141 and 143 ("*second memory devices*") on the respective RDQ0 and RDQ1 buses the same way. Ex.1003¶¶126-134,267-278.

To the extent one might argue that this limitation requires a *single rank* to output or receive all of the data "*associated with the memory … write command*," the Halbert-Amidi combination also includes this requirement under such an interpretation. Ex.1003¶¶269-272. Halbert's controller can use "masking bits" to write a single m-bit wide data word ("*N-bit wide data signal associated with the … write command"*) into one of Halbert's ranks 140 and 142. Ex.1006 at 9:46-54; Ex.1003¶¶270-271. When the masking bit is asserted, the data lines do not carry "*data signal associated with the … write command.*" Ex.1011 at 29-30.

In the Halbert-Amidi combination without rate doubling (under the "fork-in-the-road" interpretation), Ex.1003¶¶236-242, a read or write operation would access only one rank on one of Halbert's module data buses ("*first memory devices,*" e.g., on RDQ0) and the subsequent operation could access memory devices on the other module data bus ("*second memory devices,*" e.g., on RDQ1). *Id*. As discussed above (*see* §b)), different memory write operations can target different memory devices, e.g., in the different ranks under both the fork-in-the-road and straight-line interpretations. Ex.1003¶¶463-471,475.

d) [30.d] – "a plurality of buffer circuits …"

Claim 30 further requires "*a plurality of buffer circuits operatively coupled to respective sets of the plurality of sets of data signal lines and configured to receive the first module control signals from the module control circuit and subsequently the second module control signals from the module control circuit*." Ex.1003¶¶280-290,476-477.

Halbert discloses a left interface circuit 125 and a right interface circuit 130 as "*a plurality of buffer circuits,*" each including a buffer 122 and configured to receive SYNC signals ("*first*" and "*second*" "*module control signals*") from the module controller 110 ("*the module control circuit*"). Ex.1006 at 4:60-5:5,7:31-53, Fig.4,7 (annotated above); Ex.1003¶¶261-262,280-282. Each "*buffer circuit*" is operatively coupled to the system memory controller through a respective set of

"m/2" data lines ("*data signal lines*") carrying m/2 bits each ("DQ (half)"). Ex.1006 at 7:37-40, Fig.7; Ex.1003¶¶283-284.

***e) [30.e]** – "… buffer circuit … including data paths and logic …"*

Claim 30 further requires "*each respective buffer circuit in the plurality of buffer circuits including data paths and logic that configures the data paths in response to the first module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the first write command received by the each respective buffer circuit from the memory controller via a respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the first memory devices, where n is equal to a bit width of the each respective buffer circuit, wherein the logic in the each respective buffer circuit subsequently configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the second write command received by the each respective buffer circuit from the memory controller via the respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the second memory devices, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein each of the respective one or more of the first*

memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein each of the respective one or more of the second memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the second write command."

Halbert discloses that its "*buffer circuit*" includes "*data paths and logic that configures the data paths in response to the first module control signals*." Ex.1003¶¶412-417,479. Halbert's data interface circuit includes bidirectional buffer 122 and registers 126, 128, and Mux/DeMux 124 that include "*logic that configures the data paths in response to the … module control signals*" including DIR and REG_SEL signals. Ex.1006 Fig.4 (annotated below), 5:23-65. In response to DIR, this logic configures the buffers and registers as drivers or receivers and as DeMux or Mux and, in response to REG_SEL, the logic determines which data path (through 126 or 128) should be active and which should be disabled. *Id*.; Ex.1003¶¶292-294,416; Ex.1006 at 7:37-40

Halbert's data interface circuit has one "*data path*" from the system data bus DQ (on the left, green) ("*a respective set of the plurality of sets of data signal lines")* through MUX/DeMUX 124, register 126, and data bus RDQ0 (green) to rank 140, and another "*data path*" through MUX/DeMUX 124, register 128, and data bus RDQ1 (green) to rank 142. Ex.1006 at Fig.4(annotated below), 5:16-22.

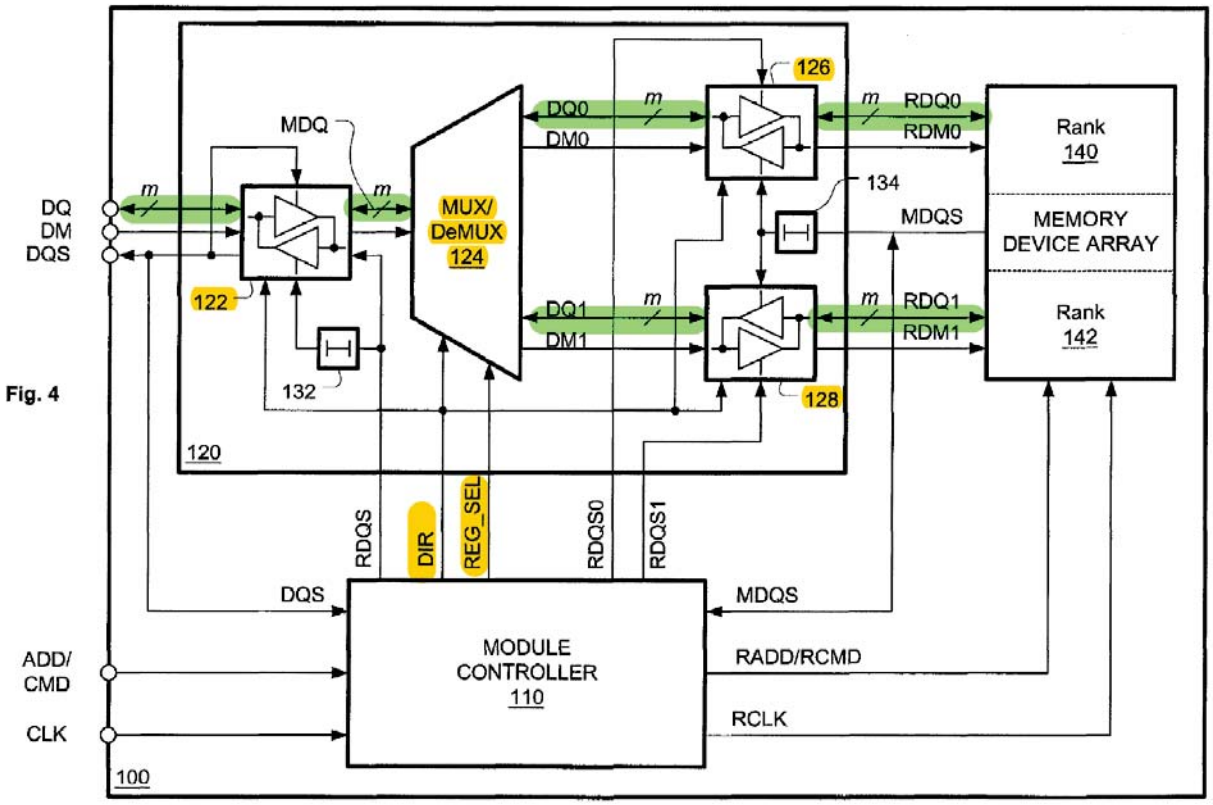


Fig. 4

Halbert's memory access (such as a write) to a subset of the memory devices (such as those in Ranks 140 and 142) will cause m/2 bits ("*a respective n-bit section of the each N-bit wide data signal*") to be received by each data interface circuit 125 and 130 ("*buffer circuit*") and transmitted to memory devices coupled to it ("*respective one or more of the first memory devices*"), where m/2 bits is the data width of each of the interface circuits 125 and 130 ("*where n is equal to a bit width of the each respective buffer circuit*"). Ex.1003¶¶291-299,480. Similarly, "*in response to the second module control signals,*" Halbert's "*buffer circuit*" causes an "*n-bit section of the each N-bit wide data signal*" to be transmitted to the "*second memory devices.*" Ex.1003¶482.

In the Halbert-Amidi combination, when using masking bits or when configured without rate doubling, a write to rank 140 on one data path can be followed by a write ("*the second write command*") to ranks 142 or 143 on the other data path in accordance with the fork-in-the-road interpretation; alternatively, the second write can target additional memory devices in rank 141 using the same data bus (RDQ0) in accordance with the straight-line interpretation. Ex.1003¶¶126-134,205-243,270-271,480,483.

The Halbert-Amidi combination also includes "*data paths*" that are "*configured differently when the logic is responding to the second module control signals*" versus "*the first module control signals*." Ex.1003¶¶484-485. The data paths are configured differently under the fork-in-the-road interpretation when different paths to different module data buses are activated for the first and second write commands. Ex.1003¶¶463-471,485. Under the straight-line interpretation, Halbert discloses that the control signals have different length and timing for the second write operation because of changed burst length and latency, and these control signals configure the data paths differently. Ex.1003¶¶413-416; Ex.1006 at 5:51-54; *see also* §b) above.

The Halbert-Amidi combination also includes "*first memory devices*" that receive data in response to the "*first memory command*" and the "*second memory devices*" that receive data in response to the "*second memory command*." *See*

Ex.1003¶486. Also as demonstrated above in §c), each memory device (140A-D) coupled to left circuit 125 in Halbert, and each memory device (140E-H) coupled to right circuit 130 will receive (during a write) m/8 bits (e.g., 4 bits) of the N-bit wide data signal (e.g., 32 bits). Ex.1003¶¶264-268. Thus, in response to the "*first write command*" each of the "*first memory devices*" (140A-H) "*receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the first write command*." Similar logic applies to the "*second write command*" directed to rank 142 or 143 on the other bus of the Halbert-Amidi combination in accordance with the fork-in-the-road interpretation, or to the additional rank 141 on the same bus in accordance with the straight-line interpretation. Ex.1003¶¶205-243. Either way, each of the corresponding "*second*" memory devices "*receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the second write command*."

f) [30.f] – "a printed circuit board (PCB) …"

Claim 30 further requires "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines,*

and between the plurality of buffer circuits and the plurality sets of data signal lines." Ex.1003¶¶304-307,488-489.

Halbert's "*memory module*" can be a DIMM "comprising a printed circuit board" that "has electrical contact points arranged on both sides along one long edge… [to] form electrical connections to the main board's memory bus when the DIMM is inserted into a DIMM memory socket." Ex.1006 at 2:8-14,3:11-14,7:31-61,11:26-30(claim 9), Figs.7,8; Ex.1003¶¶189-191,305-306. As discussed above in Section a), the socket includes a "*set of control signal lines*" coupled to the module controller 110 ("*module control circuit*") and two "*sets of data signal lines"* coupled to the left and right interface circuits 125 and 130 ("*M buffer circuits*"). Ex.1003¶¶187-199,306.

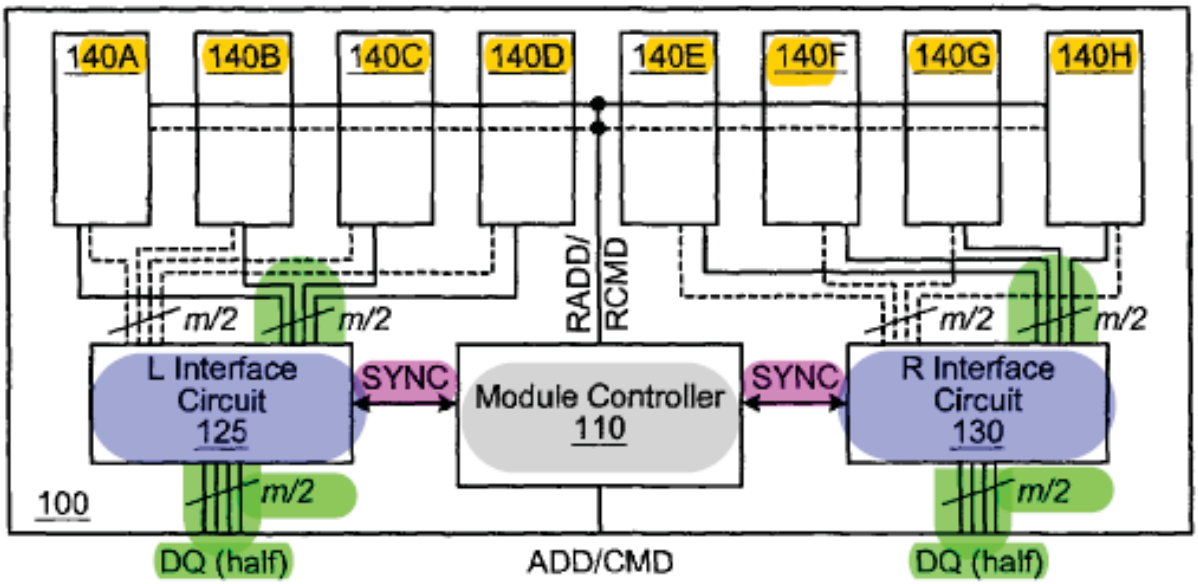
***g) [30.g]** – "… buffer circuits are mounted … at corresponding positions …"*

Claim 30 further requires that the "*the plurality of buffer circuits are mounted on the PCB between memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices*."

The left and right interface circuits 125 and 130 in Halbert are mounted on the PCB on the left and right side and between the edge connector and the memory

devices 140A-140D and 140E-140H, respectively. Ex.1006 at FIG. 7(annotated below); Ex.1003¶¶308-314. The module controller is centered between the left and right interface circuits that "*are distributed along the edge connector at corresponding positions separate from each other.*" Ex.1006 at 7:40-:49; Ex.1003¶¶309-311.

Fig. 7



The left and right interface circuits 125 and 130 are disposed on the left and right side, respectively, at a position corresponding to their coupled memory devices which include both "*first*" and "*second*" memory devices. Ex.1003¶¶264-278,312-314; *see also* §c). That is, in the Halbert-Amidi combination, the memory devices coupled to each interface circuit include "*first*" and "*second*" memory devices because rank 142 has memories on the other side on the module at

positions corresponding to those in rank 140 and the additional ranks 141 and 143 are stacked on ranks 140 and 142. Ex.1003¶314.

2. Claim 31

Claim 31 requires that "*the data paths in the each respective buffer circuit are configured in accordance with a latency parameter when the logic is responding to the first module control signals and when the logic is responding to the second module control signals*." Ex.1003¶¶492-495.

As discussed above, see §1.e), Halbert discloses that, in each of the interface circuits 125 and 130 ("*buffer circuit*"), "*the data paths …[are] configured … when the logic is responding to the first module control signals and when the logic is responding to the second module control signals.*" Ex.1003¶¶413-417,493.

Halbert discloses use of a "*latency parameter*," such as read latency, write latency, CAS latency, and additional latency, which are used to control the interface circuits and the respective timing for memory accesses, and this timing would have been understood by a Skilled Artisan to be part of the process by which data paths are configured. Ex.1003¶¶343-355,463-471,494.

Halbert's module controller 110 provides timing and synchronization signals (SYNC) to data interface circuit 120. Ex.1003¶¶261-262,343; Ex.1006 at 4:40-48,5:23-39,7:31-53, Figs.4,7. Halbert also discloses the timing of the corresponding data ("*each N-bit wide data signal*") associated with a read or write

command. *Id*. at 5:66-7:30, Figs.5-6. Therefore, Halbert discloses that "*the data paths in the each respective buffer circuit are configured in accordance with*" the timing required by a read or write command.

Halbert's module controller asserts the DIR signal at the time "when [memory] device array 140/142 is expected to begin driving buses RDQ0 and RDQ1," which was recognized by a Skilled Artisan as "a known CAS (column address strobe) latency" after which "the memory bank places data … onto bus lines." Ex.1006 at 2:55-60; Ex.1003¶344. Further, the "controller 110 counts … each operation's burst length … to track how long to stay in the READ state," Ex.1006 at 6:10-19, which the Skilled Artisan would have understood to use the CAS latency parameter to define the time between the read commands and the respective data bursts. *Id*. Fig.5. A Skilled Artisan would have understood that similar timing requirements apply to write commands. Ex.1011 at 22, Fig.22. Therefore, Halbert discloses that "*the data paths in the each respective buffer circuit are configured in accordance with a latency parameter*."

The Halbert-Amidi combination therefore renders claim 31 obvious. *See* Ex.1003¶¶342-356,435-436,445-446.

3. Claim 32

Claim 32 requires that "*the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or*

more of the first memory devices and memory device load associated with the respective one or more of the second memory devices from the memory controller."

Halbert's memory modules "allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus" from the memory controller in order "to drive signals reliably on the bus." Ex.1006 3:67-4:27,4:60-62. In Halbert's data interface circuits, the bi-directional buffers 122 isolate the load of *all* of the memory devices, including the "*first*" and "*second*" memory devices. Ex.1003¶¶301-302; Ex.1035 at 68,74-75,133, Figs.2.28,4.7.

The Halbert-Amidi combination therefore renders claim 32 obvious. *See* Ex.1003¶¶300-303,496-497.

4. Claims 33, 47 and 54

Claims 33, 47 and 54 require that the "*buffer circuit is configured to present … one memory device load on each data signal line of the respective set of the plurality of sets of data signal lines [to the memory controller]*."

As discussed above in Section 3, Halbert's bidirectional buffer 122 presents a device load on each of the data lines (DQ). Ex.1003¶301; Ex.1006 at 3:67-4:2,4:60-62,Fig.4. It would have been obvious to have that load as "*one memory device load*" to be "compatible with an existing memory controller/bus and with existing memory devices." Ex.1006 at 3:42-57,4:8-22. Skilled Artisans would have understood that the "memory devices that operate at the full speed of the

memory system data bus" have a corresponding device load, and Halbert's interface circuit should present that memory device load on the system data bus in order to "appear" to the system memory controller as such a memory device. *Id*., Ex.1003¶¶322-323. Skilled Artisans would also have understood that memory system specifications provide limitations on the load presented by the memory device. Ex.1011 at 65; Ex.1003¶¶324-325. Halbert therefore renders claims 33, 47, 54 obvious. *See* Ex.1003¶¶498-499,564-565,602-603.

5. Claim 34

Claim 34 requires that the "*buffer circuit is configured to present a load that is the same as a load the memory controller would present to the respective one or more of the first memory devices and subsequently to the respective one or more of the second memory device*."

As discussed above in §3, Halbert's memory devices are "isolated from the full capacitive loading effects of the system memory data bus" (Ex.1003¶301; Ex.1006 at 3:67-4:5), and its interface circuit "*is configured to present a load to the respective one or more of the first memory devices that is*" the load of the registers 126 and 128. Ex.1003¶332; Ex.1006 at 5:6-39, Fig.4. It would have been obvious to have that "*load*" be "*the same as a load the memory controller would present*" to be "compatible with an existing memory controller/bus and with existing memory devices" so that, "to the memory devices, it appears that each is

connected to a controller," including "the capacitance[, i.e., a load,] that a memory device (or the controller) sees when it drives the bus." Ex.1006 at 3:42-57,4:9-22; Ex.1003¶333. Thus, Skilled Artisans would have looked for and matched the relevant specifications for the load of a memory controller when designing the buffer devices coupled to the memory devices. Ex.1003¶334; Ex.1039 at 13,52,209-210,255. Halbert therefore renders claim 34 obvious. Ex.1003¶500-501.

6. Claims 35, 42, 50 and 55

Claims 35, 42, 50 and 55 require that the "*buffer circuits [are] byte-wise buffer circuits, and wherein each set of the plurality of sets of data [signal] lines is eight bits wide*." As discussed above in §1.d), each of Halbert's *"buffer circuits"* (left and right circuits 125 and 130) has a data width equal to m/2 bits. Ex.1003¶283; Ex.1006 at Fig. 7. In Halbert's module, the data width m, the memory type, or the number of memory devices in one rank "is not critical," so that m can be 16 providing m/2=8 bit (one byte) wide interface circuits. Ex.1006 at 2:37-42,9:38-39,9:55-56,Fig.2. Halbert therefore renders claims 35, 42, 50 and 55 obvious. *See* Ex.1003¶¶502-503,528-529,573-574,604-605.

7. Claim 36

Claim 36 requires that the "*module control circuit comprises one or more integrated circuits having first input/output connections, second input/output*

connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections."

Halbert's module controller 110 ("*module control circuit*") is a "*circuit*" which can be "integrated in a single device" ("*one or more integrated circuits*"). Ex.1006 at 4:40-48,7:47-49,10:1-6; Ex.1003¶358. To the extent one might argue that Halbert does not disclose this limitation, it would have been obvious because module controller 110 is a discrete, separate unit, and using integrated circuits on a PCB was a well-known, efficient way to implement it. Ex.1003¶¶359-362; Ex.1006 at 7:47-49,10:1-6; Ex.1007¶[0028]; Ex.1010 at 22,23,35.

As discussed above with reference to the Halbert-Amidi combination and claim element [30.b] (*see* §§A&1.b)), module controller 110 is coupled to ranks (including "*subsets*") of memory devices by "*address and control signals*" on the RADD/RCMD bus, chip select signals RS0-RS3, and strobe signals MDQS. Ex.1006 Fig.4; Ex.1007 Figs.3,6A; Ex.1003¶¶245-263. Amidi further discloses that, for each rank (e.g., Rank0), the CPLD has two "*input/output connections*"

(e.g., rcs0a and rcs0b) each carrying a chip select signal to a subset of the memory devices in that rank. Ex.1007¶¶[0069-70], Figs.3,6A; Ex.1003¶¶368. Skilled Artisans would have understood that the "*address and control signals*" can also be carried on two or more "*input/output connections*" between the module controller and the memory devices, which was a predictable, standardized technique at the time. Ex.1010 at 18 (showing two connections for each registered address and command signal); Ex.1003¶¶368. Thus, each rank in the Halbert-Amidi combination includes subsets of memory devices with respective "*input/output connections*," as required by these claims.

8. Claims 37, 51 and 56

Claims 37, 51 and 56 require that "… *wherein the [respective] one or more [of the first] memory devices [in the subset of the memory devices] include a single memory device [outputting or] receiving the respective [n-bit]/[8-bit] [section]/[portion] of [the] [each N-bit wide] data [signal] associated with the [first] [memory] [read or] write command, [and wherein the respective one or more of the second memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the second write command]*."

Halbert discloses memory devices having data width of four, eight, or sixteen bits, which is not a "critical" characteristic. Ex.1006 at 2:37-43,9:55-56;

Ex.1003¶378. In a memory module having a width (m) of 32 bits, each of the left and right interface circuits handles 16 bits. Ex.1006 at 2:19-22,3:55-57. With 16-bit wide memory devices, "*a single memory device [is] outputting or receiving the respective n[=16]-bit section of the each N[=32]-bit wide data signal associated with the memory read or write command*." Ex.1006 at 2:40-43; Ex.1003¶379. The width (m) of Halbert's module can also be 16, Ex.1006 at 9:38-39, so each of the left and right circuits transfers m/2=8 bits (one byte) at a time, and therefore each is a byte-wise buffer circuit, and the respective data section is eight bits wide. *See id*.; Ex.1006 at Fig.2.

To the extent one might argue that Halbert does not disclose using such arrangements of 16 or 8 bit wide memory devices in a memory module, such arrangements would have been obvious, because Halbert explains that the specific number of memory devices and bit width shown in the drawing is "not critical." Ex.1006 at 9:55-56; Ex.1003¶381. Halbert therefore renders claims 37, 51 and 56 obvious. *See* Ex.1003¶¶506-507,575-576,606-607.

9. Claims 38, 52 and 57

Claims 38, 52 and 57 require "*[wherein each of the memory devices is four bits wide], wherein the respective one or more of the first memory devices [in the subset of memory devices] include a pair of memory devices each [outputting or] receiving [half]/[[4 bits] of the respective n-bit section of the each [N-bit]/[8-bit]*

wide data signal associated with the [first] [read or] write command, [and wherein the respective one or more of the second memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the second write command]."

Halbert discloses memory devices having data width of four, eight, or sixteen bits, which is not a "critical" characteristic. Ex.1006 at 2:37-43,9:55-56; Ex.1003¶¶336-338,378-381. When Halbert's module is 32 bits wide and uses 8-bit wide memory devices, each memory device in the "*pair of memory devices"* is *"outputting or receiving [8 bits which is] half of the respective [16]-bit section of the each [32]-bit wide data signal associated with the memory read or write command."* Ex.1003¶385. Halbert therefore renders claims 38, 52 and 57 obvious. *See* Ex.1003¶¶508-509,577-578,608-609.

10. Claim 39

Claim 39 requires that "*each respective buffer circuit includes input buffers to receive the respective n-bit section of the each N-bit wide data signal associated with the first write command from the memory controller, wherein each of the input buffers is comparable in loading to an input buffer on one of the memory devices*."

As demonstrated above in §3, Halbert's bidirectional buffer 122 presents a device load on each of the data lines (DQ). Ex.1003¶301; Ex.1006 Fig.4, 3:67-

4:2,4:60-62. It would have been obvious to set that load to be "*comparable in loading to an input buffer on one of the memory devices*" because that would make Halbert's module "compatible with an existing memory controller/bus and with existing memory devices." Ex.1006 at 3:42-57,4:8-22; Ex.1011 at 65; Ex.1003¶¶322-326; *see also* §4. Halbert therefore renders claims 39 obvious. Ex.1003¶¶634-635.

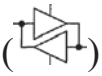
11. Claim 40

Claim 40 requires that "*each respective buffer circuit further includes output buffers to drive the respective n-bit section of the each N-bit wide data signal associated with the first write command to the respective one or more of the first memory devices, wherein each of the output buffers is comparable in loading to an output buffer on the memory controller*."

As explained above in Sections 1.e),5,&10, each of Halbert's interface circuits ("*buffer circuit*") includes a bidirectional buffer "*to drive the respective n-bit section of the each N-bit wide data signal associated with the first write command to the respective one or more of the first memory devices* " and present a "*load*" that "*is comparable in loading to an output buffer on the memory controller.*" Ex.1003¶¶291-299,330-335,517,518.

12. Claim 41

Claim 41 requires that the "*output buffers regenerate the … data signal associated with the first write command to restore desired signal waveform shapes …*." Halbert's bidirectional registers 126 and 128 include buffers in the WRITE direction ("*output buffers*") which were obvious to be implemented using tristate buffers as explained by Stone. Ex.1003¶¶389-398; Ex.1006, Fig.4; Ex.1035 at 74. In operation, the bidirectional register latches the value of the incoming data signal, and that latched value is re-driven, thereby regenerating the desired waveform. Ex.1003¶¶525-526; Ex.1006 at 5:54-58, Fig.4; Ex.1035 at 96.

To the extent one might argue that Halbert does not disclose this limitation, it would have been obvious. Indeed, Halbert's Fig. 4 discloses a symbol of a tristate buffer () in each of the bidirectional registers 126 and 128, thereby motivating a Skilled Artisan to use such a tristate buffer in the register, which was well within the level of skill at the time and would have led to predictable results, including restoring the desired signal waveform shape. Ex.1006 at Fig.4; Ex.1003¶526.

13. Claim 43

a) [43.a] – "A memory module …"

For the same reasons as claim [30.a], the Halbert-Amidi combination includes a "*memory module configured to communicate with a memory controller*

via a set of control signal lines and a plurality of sets of data lines." *See* §1.a); Ex.1003¶¶187-204,530-531.

***b) [43.b]** – "memory devices"*

For the same reasons as claim [30.c], the Halbert-Amidi combination includes "*memory devices*." *See* §1.c); Ex.1003¶¶264-278,532-533.

***c) [43.c]** – "a module control circuit …"*

Claim 43 further requires "*a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command*."

For the reasons explained above with respect to limitation [30.b], Halbert discloses a "*module control circuit*" that receives "*input address and control signals*" from a "*memory controller … via the set of control signal lines*." *See* §1.b); Ex.1003¶¶245-247,535.

As discussed above with respect to limitation [30.b], the "*module control circuit*" in the Halbert-Amidi combination is configured "*to produce output address and control signals in response to the set of input address and control signals.*" *See* §1.b); Ex.1003¶¶462-471,536.

In the Halbert-Amidi combination, the "*module control circuit*" is configured "*to evaluate the … input … signals to determine*" from which "*memory devices to output or receive data*." Ex.1003¶¶537-539. Halbert's module controller includes Amidi's CPLD functionality that uses input address and control signals to determine which of the ranks 140-143 is the target of a memory access. Ex.1003¶¶253-262; Ex.1006 at 6:5-8,7:54-61; Ex.1007¶[0041]; Ex.1003¶537. Thus, the Skilled Artisan would have implemented the module controller to "*evaluate*" the input address and control signals in order to produce the control signals that activate specific ranks to respond to write commands. Ex.1003¶538; Ex.1011 at 20; Ex.1010 at 6.

As discussed above with respect to limitation [30.b], the "*module control circuit*" in the Halbert-Amidi combination produces "*module control signals*" as

recited in limitation [43.c]. *See* §1.b); Ex.1003¶¶252-262,540. In response to the evaluation of input address and control signals the module controller produces various module control signals for controlling the module such that the memory access is directed to the proper memory devices. *Id*.

As discussed above with respect to limitation [30.c], the Halbert-Amidi combination is configured such that, "*in response to the output … signals*," one subset of "*memory devices output or receive data*" and "*other memory devices*" do not. *See* §1.c); Ex.1003¶¶264-278,541. In response to the module control signals, the target memory devices will output or receive data while the non-target memory devices will not under the fork-in-the-road interpretation, or the non-target memory devices will not access the data under the straight-line interpretation. Ex.1003¶¶264-278.

***d) [43.d]** – "a plurality of buffer circuits …"*

For the same reasons as claim [30.d], the Halbert-Amidi combination includes "*a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices*." *See* §1.d); Ex.1003¶¶279-290,543-544.

e) [43.e] *– "… buffer circuit including data paths and logic …"*

For the same reasons as claim [30.e], the "*buffer circuits*" in the Halbert-Amidi combination include "*data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit*." *See* §1.e); Ex.1003¶¶412-417,545-546.

f) [43.f] *– "… buffer circuit … configured to isolate memory device load …"*

For the same reasons as claim 32, each "*buffer circuit*" in the Halbert-Amidi combination "*is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller*." *See* §3; Ex.1003¶¶300-303,547-548.

g) [43.g] *– "a printed circuit board (PCB) …"*

For the same reasons as claim [30.f], the Halbert-Amidi combination includes "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module*

control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines." *See* §1.f); Ex.1003¶¶304-307,549-550.

***h) [43.h]** – "… buffer circuits are mounted … at corresponding positions …"*

For the same reasons as claim [30.g], the "*buffer circuits*" in the Halbert-Amidi combination "*are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices*." *See* §1.g); Ex.1003¶¶308-315,551-552.

14. Claim 44

Claim 44 requires that "*the set of module control signals are further dependent on whether the memory read or write command is a memory read command or a memory write command, and wherein the logic configures the data paths differently depending on whether the memory read or write command is a memory read command or a memory write command*."

The "*second module control signals*" (SYNC) in Halbert discussed above in Section 1.b) include a "direction signal DIR [which] specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)."

Ex.1003¶¶261-262; Ex.1006 at 5:23-39,7:51-53. The DIR signal controls which direction the bidirectional buffers, registers and MU/DeMUX will communicate data, "*depending on whether the memory read or write command is a memory read command or a memory write command"*. Ex.1003¶¶339-341,554; Ex.1006 at 5:23-39,5:51-65. Halbert also discloses that the logic in the interface circuit configures the data paths through MUX/DeMUX 124 and bidirectional registers 126 and 128 differently depending on the command received being a read or a write. Ex.1003¶¶339-341,555.

15. Claims 45 and 48

Claims 45 and 48 require that the "*data paths*" in its "*buffer circuit*" include "*write data paths*" and "*read data paths*" having "*tristate buffers controlled by the logic*."

As discussed above in §§1.e)&10, each data interface circuit ("*buffer circuit*") in Halbert includes one bidirectional data path through register 126 and another one through register 128, both registers being controlled by logic and using "*tristate buffer[s]*". Ex.1003¶¶390-397,414-416,425-426; Ex.1006 at 9:30-35, Fig.4 ().

Using two separate data paths, one "*read data path*" and one "*write data path"* with unidirectional components instead of a bidirectional path, as disclosed by Halbert's alternative, was a well-known technique described decades earlier in

text books, like Stone. Ex.1035 at 133, Fig.4.7. Designing such logic for Halbert's module was well within the level of skill at the time. Ex.1003¶¶426-427. The Halbert-Amidi combination therefore renders claims 45 and 48 obvious.

16. Claims 46 and 49

Claims 46 and 49 require that "*the memory read or write command is a memory write command, and wherein the tn state buffers regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal waveform shapes, and transmit regenerated signals to the respective one or more of the subset of the memory devices*."

Halbert's module can receive "*a memory write command.*" Ex.1003¶561; Ex.1006 at Fig.6. As demonstrated above in §12(claim 41), bidirectional registers 126 and 128 can be implemented using tristate buffers to "*regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal waveform shapes*" and the regenerated data would be transmitted *"to the respective one or more of the subset of the memory devices"* because that is the purpose of output buffers in this context. Ex.1003¶¶522-527,562; Ex.1006 at 5:6-14.

17. Claim 53

a) [53.a] – "A memory module …"

For the same reasons as claim [30.a], the Halbert-Amidi combination includes a "*memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines*." *See* §1.a); Ex.1003¶¶187-204,579-580.

b) [53.b] – "a module control circuit …"

Claim 53 further requires "*a module control circuit coupled to the set of control signal lines and configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce output address and control signals and a set of module control signals in response to the input address and control signals, the module control circuit having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections*." *See* Ex.1003¶¶581-584.

As shown above (limitation [30.b]), Halbert discloses "*a module control circuit coupled to the set of control signal lines and configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines.*" *See* §1.b); Ex.1003¶¶245-247. The Halbert-Amidi combination further includes *"a module control circuit ... configured ... to produce output address and control*

signals and a set of module control signals in response to the input address and control signals" for the reasons set forth above in §1.b). *See* Ex.1003¶¶462-472.

As shown above (claim 36), Halbert-Amidi combination also includes a "*module control circuit having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections.*" *See* §7; Ex.1003¶¶357-374 above.

***c) [53.c]** – "memory devices …"*

Claim 53 further requires "*memory devices including first memory devices and second memory devices, the first memory devices including a first number of memory devices coupled to the first input/output connections and a second number of memory devices coupled to the second input/output connections, the second memory devices including a third number of memory devices coupled to the third input/output connections and a fourth number of memory devices coupled to the fourth input/output connections, wherein, in response to the output address and control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command*." *See* Ex.1003¶¶585-589.

As shown above (limitation [30.c]), the Halbert-Amidi combination includes "*memory devices including first memory devices and second memory devices.*" *See* §1.c); Ex.1003¶¶264-278.

As shown above (claim 36), the Halbert-Amidi combination includes "*first memory devices including a first number of memory devices coupled to the first input/output connections and a second number of memory devices coupled to the second input/output connections, the second memory devices including a third number of memory devices coupled to the third input/output connections and a fourth number of memory devices coupled to the fourth input/output connections.*" *See* §7; Ex.1003¶¶357-374.

As shown above (limitation [43.b]), the Halbert-Amidi combination is configured such that, "*in response to the output address and control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command*" *See* §13.b); Ex.1003¶¶264-278.

***d) [53.d]** – "a plurality of buffer circuits …"*

For the same reasons as claim [30.d], the Halbert-Amidi combination includes "*a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer*

circuit is coupled between respective one or more of the first memory devices and a respective set of the plurality of sets of data lines, and between respective one or more of the second memory devices and the respective set of the plurality of sets of data lines." *See* §1.d); Ex.1003¶¶279-290,590-591.

***e) [53.e]** – "… buffer circuit including data paths and logic …"*

For the same reasons as claim [30.e], each "*buffer circuit*" in the Halbert-Amidi combination includes "*data paths and logic that configures the data paths in response to the set of module control signals to allow a respective section of the each N-bit wide data signal to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit*." *See* §1.e); Ex.1003¶¶412-417,592-593.

***f) [53.f]** – "… write … and read data paths …"*

As discussed above in §15, the "*data paths*" in the Halbert-Amidi combination include "*write data paths and read data paths, the write data paths including tristate buffers controlled by the logic and the read data paths including tristate buffers controlled by the logic*." Ex.1003¶¶424-432,594-595.

***g) [53.g]** – "… buffer circuit … configured to isolate memory device load …"*

For the same reasons as claim 32, each "*buffer circuit*" in the Halbert-Amidi combination "*is further configured to isolate memory device load associated with the respective one or more of the first memory devices and the respective one or*

more of the second memory devices from the memory controller." *See* §3; Ex.1003¶¶300-303,596-597.

h) [53.h] *– "a printed circuit board (PCB) …"*

For the same reasons as claim [30.f], the Halbert-Amidi combination includes "*a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data signal lines*." *See* §1.f); Ex.1003¶¶304-307,598-599.

i) [53.i] *– "… buffer circuits are mounted … at corresponding positions …"*

For the same reasons as claim [30.g], the "*buffer circuits*" in the Halbert-Amidi combination "*are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices*." *See* §1.g); Ex.1003¶¶308-315,600-601.

C. Claims 36 and 53-57 are obvious over Halbert (Ex.1006) and Amidi (Ex.1007) in further view of Ruckerbauer (Ex.1038)

Claims 36 and 53 (and the claims that depend from them) require the "*module control circuit … having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, … the first memory devices include[ing] [a subset/first number] of memory devices coupled to the first input/output connections and [another subset/a second number] of memory devices coupled to the second input/output connections, … the second memory devices include[ing] [a subset/third number] of memory devices coupled to the third input/output connections and [another subset/fourth number] of memory devices coupled to the fourth input/output connections.*"

The Halbert-Amidi combination (*see* §A) in view of Ruckerbauer renders obvious that the "*module control circuit*" includes "*first*" through "*fourth input/output connections*" as claimed. *See* Ex.1003¶¶253-260,360. Halbert discloses multiple "*connections*" to transmit signals to the memory devices on the RADD/RCMD bus. Ex.1003¶¶253-260. Halbert's RADD/RCMD bus is shown in Fig. 7 as a T-bus with a left-right branching point outside the module controller. Ex.1006 Fig.7. Skilled Artisans, however, would have used Ruckerbauer's separate left and right buses instead for "further increasing speeds … [where]

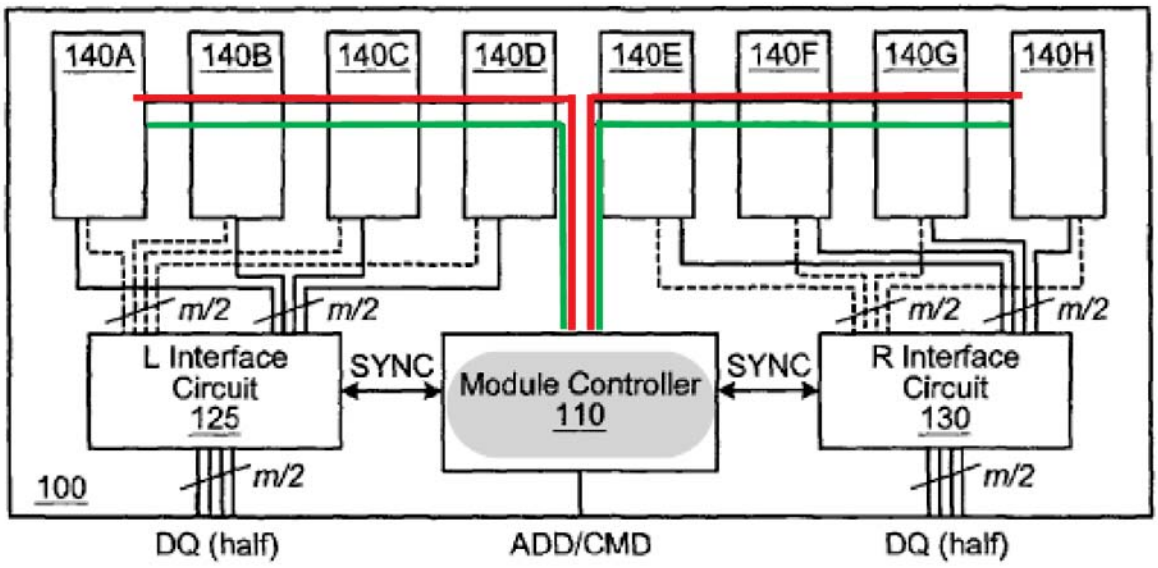
conventional transfer of command and address signals is no longer possible." Ex.1038 at 1:20-28; Ex.1006 at 4:9-22; Ex.1003¶361.

The Halbert-Amidi combination in view of Ruckerbauer also renders obvious that the "*first memory devices*" include a subset coupled to the "*first … connections*," and a subset coupled the "*second … connections*," and that its "*second memory devices*" include a subset coupled to the "*third … connections*," and a subset coupled the "*fourth … connections*." Ex.1003¶¶361-374. Although Halbert's RADD/RCMD bus is shown in FIG. 7 as a T-bus with a left-right branching point outside the module controller, it was obvious to use Ruckerbauer's separate left and right buses instead to operate at "further increasing speeds … [where] conventional transfer of command and address signals is no longer possible." Ex.1038 at 1:20-28; Ex.1006 at 4:9-22; Ex.1003¶361. To allow higher speeds, Ruckerbauer uses separate "command and address signals run … to the left and the right of the … memory module 10." Ex.1038 at 4:57-62,5:62-6:16, Figs.1,2. Thus, Ruckerbauer discloses the claimed subsets (left and right). Ex.1003¶¶361-362.

Halbert and Ruckerbauer (and Amidi) are analogous art to the 907 Patent (Ex.1003¶363) and Skilled Artisans would have implemented Halbert's module according to Ruckerbauer's separate signals to the left and right in each rank in order to reduce device loading effects, and made possible operation at higher

speeds. Ex.1003¶¶364-367; Ex.1006 at 4:9-22, Fig.7 (annotated below); Ex.1038 at 2:31-32.

Fig. 7



Such doubling of the connections would have been well within the level of skill at the time as it would use well known components which would perform as in the prior art and provide predictable results. Ex.1010 at 18; Ex.1038 Fig.1; Ex.1003¶¶368-369.

To the extent one might argue that Halbert does not disclose "*input/output connections*" requiring both input and output, *see, e.g.*, Ex.1011 at 6, Halbert also renders such an interpretation obvious. Ex.1003¶370. For example, Halbert discloses MDQS (memory data strobe) input/output connections between module controller 110 and ranks 140 and 142. Ex.1006 at 5:63-65,6:15-48, Fig.4; Ex.1011 at 6; Ex.1003¶371. The Skilled Artisan would also have been motivated to use a

module controller with "*input/output connections*" to the memory devices because Halbert's invention can use "Rambus™ DRAM devices (with an appropriate controller)" and these devices use input/output connections to "supply the RDRAM configuration information to a controller and …[to] select the operating modes of the device." Ex.1006 at 9:55-62; Ex.1042 at 3-5; Ex.1003¶¶372-373. Implementing such input/output control connections was well with the level of skill at the time as evidenced by the Direct RDRAM devices and thus would have provided predictable results.

The Halbert-Amidi combination in view of Ruckerbauer therefore renders obvious claims 36 and 53 (and the claims that depend from them). *See* Ex.1003¶¶357-374,387-388,441-442,451-452,630-631.

D. Claims 45-57 are obvious over Halbert (Ex.1006) and Amidi (Ex.1007) in view of Stone (Ex.1035)

The Halbert-Amidi combination in view of Stone meets the claim 45 and claim limitation [53.f] requirement that "*the data paths include write data paths [and read data paths], and wherein the write data paths include tristate buffers controlled by the logic [and the read data paths including tristate buffers controlled by the logic]*," and the requirement that "*the tn state buffers regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal*

waveform shapes" as set forth in claims 46 and 49 (and the claims that depend from them). Ex.1003¶¶292-298,389-398.

As discussed above in §B.12, Halbert discloses that the interface circuits include bidirectional buffers and registers. To the extent one might argue that Halbert does not disclose "*tristate*" buffers in these buffers and registers, it would have been obvious as it was a well-known technique and would have resulted in the predictable result of a reliable and efficient interface circuit to drive data to and from the memory devices on a multi-tap bus, as taught in text books, like Stone. Ex.1003¶¶393-396; Ex.1035 at 68,74-75,117.

Further, using two separate data paths, one "read data path" and one "*write data path"* with unidirectional components instead of a bidirectional path, as disclosed by Halbert's alternative, Ex.1006 at 9:30-35, was also well-known from Stone. Ex.1035 at 133, Fig.4.7. Designing such unidirectional components with tristate buffers and logic for the specific control signals shown in Halbert was also well within the level of skill at the time. Ex.1003¶¶426-427.

The Halbert-Amidi combination in view of Stone renders claims 45, 46, 49 and 53 (and the claims that depend from them) obvious.

E. Claim 31 is obvious over the combination of Halbert (Ex.1006) and Amidi (Ex.1007) in further view of Solomon (Ex.1008)

To the extent one might argue that Halbert does not disclose that "*the each respective buffer circuit are configured in accordance with a latency parameter*," it would have been obvious because prior art memory controllers and memory devices used known latency parameters for timing the data transfers, and Halbert's module "is compatible" with these devices. Ex.1003¶346; Ex.1006 at 2:46-60,3:55-57. A Skilled Artisan would have also used latency parameters (CAS, Additive, etc.) for tracking pipelined read and write operations, and for timing the control signals accordingly. Ex.1006 at 6:10-14; Ex.1011 at 22, Fig.22; Ex.1003¶347.

Such latency based timing was well known at the time. Ex.1008(Solomon), [0132]. Halbert and Solomon (and Amidi) are analogous art directed to multi-rank memory module design problems, just like the 907 patent. Ex.1001 at 1:17-2:21; Ex.1006 at 1:16-2:60,3:32-4:35; Ex.1007¶¶[0001],[0003]-[0011]; Ex.1008¶¶[0003],[0009]-[0012],[0040], Fig.1; Ex.1003¶¶348-350. Solomon's memory module uses CAS latency for timing as described in a Verilog code. Ex.1008¶¶[0119],[0132]; Ex.1003¶350. It would have been obvious to employ Solomon's latency parameter technique in the configuration of the Halbert-Amidi combination, because Halbert already uses timing parameters, like burst length,

which is set by the same Mode Register Set command, and those latency parameters and these techniques provided predictable, reliable results for timing. Ex.1003¶¶351-355; Ex.1011 at 11-12.

VIII. CONCLUSION

Because the information presented in this petition shows that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the petition, the Petitioner respectfully requests that a Trial be instituted and that Claims 30-57 of the 907 Patent be canceled as unpatentable.

Dated: December 27, 2017

Respectfully Submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,688 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment A:

Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on this 27th day of December, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by Federal Express on the following counsel of record for patent owner:

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 9,606,907
1002	File History of U.S. Patent No. 9,606,907
1003	Declaration of Dr. Harold Stone
1004	Curriculum Vitae of Dr. Harold Stone
1005	US Patent App. Publication No. 2006/0277355 by Ellsberry et al.
1006	US Patent No. 7,024,518 to Halbert et al.
1007	U.S. Patent Application Publication No. 2006/0117152 to Amidi et al.
1008	U.S. Patent Application Publication No. 2006/0262586 by Solomon et al.
1009	JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000)
1010	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1011	JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005)
1012	Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC)
1013	U.S. Patent No. 7,289,386 to Bhakta et al.
1014	U.S. Patent No. 7,532,537 to Solomon et al.
1015	U.S. Patent No. 8,417,870 to Lee et al.
1016	File History of U.S. Patent No. 8,417,870
1017	U.S. Patent No. 8,516,185 to Lee et al.
1018	File History of U.S. Patent No. 8,516,185

Exhibit #	Reference Name
1019	U.S. Patent No. 8,130,560 to Rajan et al.
1020	U.S. Patent No. 5,784,705 to Leung
1021	US Patent App. Publication No. 2009/0248969 by Wu et al.
1022	Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *SanDisk Corp. v. Netlist, Inc.*, IPR2014-01029, Paper No. 11 (Dec. 16, 2014)
1023	Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01369, Paper No. 12 (Mar. 9, 2015)
1024	Excerpts from the Hearing in *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 8–11, 2017)
1025	Complainant Netlist, Inc.'s Initial Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 30, 2017) (excerpts relevant to '185 patent)
1026	Respondents' Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (May 30, 2017) (excerpts relevant to '185 patent)
1027	High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex. 1026)
1028	Complainant Netlist Inc.'s Reply Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent)
1029	Respondents' Reply Post-Hearing Brief, *Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent)

Exhibit #	Reference Name
1030	High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex. 1029)
1031	Institution of *Inter Partes* Review of U.S. Patent No. 8,516,185, *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00577, Paper No. 8 (July 7, 2017)
1032	Final Written Decision, *Diablo Techs., Inc. v. Netlist, Inc.*, IPR2014-00882, Paper No. 33 (Dec. 14, 2015)
1033	*Netlist, Inc. v. Diablo Techs., Inc.*, No. 2016-1742 (Fed. Cir. July 25, 2017)
1034	Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 (June 14, 2017)
1035	Stone, H.S. *Microcomputer Interfacing*, Reading, MA: Addison Wesley, 1982
1036	U.S. Patent No. 5,630,096 to Zuravleff et al.
1037	U.S. Patent No. 6,683,372 to Wong et al.
1038	U.S. Patent No. 7,334,150 to Ruckerbauer et al.
1039	Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004)
1040	Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts)
1041	Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts)
1042	Direct RDRAM datasheet (2000)

PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 9,606,907

Attachment C:

Claim Listing

Ref. #	Listing of Challenged Claims
[1.a]	**1.** A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
[1.b]	a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
[1.c]	a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
[1.d]	M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,
[1.e]	the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines,
[1.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

Ref. #	Listing of Challenged Claims
[1.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines,
[1.h]	wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[2]	**2.** The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.
[3]	**3.** The memory module of claim 1, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the M sets of n data lines to the memory controller.
[4]	**4.** The memory module of claim 3, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.
[5]	**5.** The memory module of claim 1, wherein the each respective buffer circuit is configured to present a load to the respective one or more of the first memory devices that is the same as a load the memory controller would present.

Ref. #	Listing of Challenged Claims
[6]	**6.** The memory module of claim 1, wherein the each respective buffer circuit has a first data width of n bits, and wherein each of the plurality of memory devices has a second data width different from the first data width.
[7]	**7.** The memory module of claim 1, wherein the second module control signals indicate a direction of data flow through the buffer circuits.
[8]	**8.** The memory module of claim 1, wherein the module control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter.
[9]	**9.** The memory module of claim 1, wherein the module control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[10]	**10.** The memory module of claim 1, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit.
[11]	**11.** The memory module of claim 1, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[12]	**12.** The memory module of claim 1, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.

Ref. #	Listing of Challenged Claims
[13]	**13.** The memory module of claim 1, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the plurality of memory devices.
[14]	**14.** The memory module of claim 1, wherein the first memory read or write command is a memory write command, and wherein the each respective buffer circuit includes tristate buffers controlled by the logic to transmit the respective n-bit section of the each N-bit wide data signal associated with the memory write command to the respective one or more of the first memory devices.
[15]	**15.** The memory module of claim 1, wherein the M buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide.
[16.a]	**16.** A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:
[16.b]	a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
[16.c]	a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

Ref. #	Listing of Challenged Claims
[16.d]	a plurality of buffer circuits configured to receive the second module control signals from the control circuit, each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines,
[16.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits,
[16.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and
[16.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the control circuit and the set of control signal lines, and between the plurality of buffer circuits and the M sets of n data lines,
[16.h]	wherein the plurality of buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

Ref. #	Listing of Challenged Claims
[17]	**17.** The memory module of claim 16, wherein the data paths include write data paths, each write data path including at least one tristate buffer controlled by the logic.
[18]	**18.** The memory module of claim 17, wherein the data paths further include read data paths, each read data path including a tristate buffer controlled by the logic.
[19]	**19.** The memory module of claim 18, wherein the second module control signals indicate a direction of data flow through the buffer circuits.
[20]	**20.** The set of circuits in claim 18, wherein the control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the module control signals in accordance with a latency parameter.
[21]	**21.** The memory module of claim 18, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the control circuit.
[22]	**22.** The memory module of claim 18, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal.
[23]	**23.** The memory module of claim 18, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the plurality of memory devices.
[24]	**24.** The memory module of claim 16, wherein the second module control signals indicate a direction of data flow through the buffer circuits.

Ref. #	Listing of Challenged Claims
[25]	**25.** The memory module of claim 16, wherein the control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter.
[26]	**26.** The memory module of claim 16, wherein each of the plurality of memory devices is n-bit wide, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[27]	**27.** The memory module of claim 16, wherein each of the memory devices is n/2-bit wide, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command.
[28]	**28.** The memory module of claim 16, wherein the control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[29]	**29.** The memory module of claim 16, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide.
[30.a]	**30.** A memory module having a data width of N bits and configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

Ref. #	Listing of Challenged Claims
[30.b]	a module control circuit configured to receive from the memory controller via the set of control signal lines first input address and control signals corresponding to a first write command and subsequently second input address and control signals corresponding to a second write command, the module control circuit producing first output address and control signals and first module control signals in response to the first input address and control signals, the module control circuit producing second output address and control signals and second module control signals in response to the second input address and control signals, the second module control signals being different from the first module control signals;
[30.c]	memory devices coupled to the module control circuit, the memory devices including first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command, and second memory devices responding to the second output address and control signals by receiving each N-bit wide data signal associated with the second write command; and
[30.d]	a plurality of buffer circuits operatively coupled to respective sets of the plurality of sets of data signal lines and configured to receive the first module control signals from the module control circuit and subsequently the second module control signals from the module control circuit,

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[30.e]	each respective buffer circuit in the plurality of buffer circuits including data paths and logic that configures the data paths in response to the first module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the first write command received by the each respective buffer circuit from the memory controller via a respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the first memory devices, where n is equal to a bit width of the each respective buffer circuit, wherein the logic in the each respective buffer circuit subsequently configures the data paths in response to the second module control signals, causing a respective n-bit section of the each N-bit wide data signal associated with the second write command received by the each respective buffer circuit from the memory controller via the respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the second memory devices, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein each of the respective one or more of the first memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein each of the respective one or more of the second memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the second write command; and
[30.f]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality sets of data signal lines,

Ref. #	Listing of Challenged Claims
[30.g]	wherein the plurality of buffer circuits are mounted on the PCB between memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[31]	**31.** The memory module of claim 30, wherein the data paths in the each respective buffer circuit are configured in accordance with a latency parameter when the logic is responding to the first module control signals and when the logic is responding to the second module control signals.
[32]	**32.** The memory module of claim 30, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the respective one or more of the second memory devices from the memory controller.
[33]	**33.** The memory module of claim 32, wherein the each respective buffer circuit is configured to present to the memory controller one memory device load on each data signal line of the respective set of the plurality of sets of data signal lines.
[34]	**34.** The memory module of claim 32, wherein the each respective buffer circuit is configured to present a load that is the same as a load the memory controller would present to the respective one or more of the first memory devices and subsequently to the respective one or more of the second memory devices.
[35]	**35.** The memory module of claim 30, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the plurality of sets of data signal lines is eight bits wide.

Ref. #	Listing of Challenged Claims
[36]	**36.** The memory module of claim 30, wherein the module control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.
[37]	**37.** The memory module of claim 30, wherein each of the memory devices is n-bit wide, wherein the respective one or more of the first memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the second write command.
[38]	**38.** The memory module of claim 30, wherein each of the memory devices is n/2-bit wide, wherein the respective one or more of the first memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the second write command.
[39]	**39.** The memory module of claim 30, wherein the each respective buffer circuit includes input buffers to receive the respective n-bit section of the each N-bit wide data signal associated with the first write command from the memory controller, wherein each of the input buffers is comparable in loading to an input buffer on one of the memory devices.

Ref. #	Listing of Challenged Claims
[40]	**40.** The memory module of claim 39, wherein the each respective buffer circuit further includes output buffers to drive the respective n-bit section of the each N-bit wide data signal associated with the first write command to the respective one or more of the first memory devices, wherein each of the output buffers is comparable in loading to an output buffer on the memory controller.
[41]	**41.** The memory module of claim 40, wherein the output buffers regenerate the respective n-bit section of the each N-bit wide data signal associated with the first write command to restore desired signal waveform shapes in the respective n-bit section of the each N-bit wide data signal associated with the first write command.
[42]	**42.** The memory module of claim 39, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the plurality of sets of data signal lines is eight bits wide.
[43.a]	**43.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:
[43.b]	memory devices;

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[43.c]	a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce output address and control signals in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce a set of module control signals dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command;
[43.d]	a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices,
[43.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit,
[43.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller; and

Ref. #	Listing of Challenged Claims
[43.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines,
[43.h]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more memory devices in the subset of the memory devices and the one or more of the other memory devices.
[44]	**44.** The memory module of claim 43, wherein the set of module control signals are further dependent on whether the memory read or write command is a memory read command or a memory write command, and wherein the logic configures the data paths differently depending on whether the memory read or write command is a memory read command or a memory write command.
[45]	**45.** The memory module of claim 43, wherein the data paths include write data paths, and wherein the write data paths include tristate buffers controlled by the logic.
[46]	**46.** The memory module of claim 45, wherein the memory read or write command is a memory write command, and wherein the tn state buffers regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal waveform shapes, and transmit regenerated signals to the respective one or more of the subset of the memory devices.

Ref. #	Listing of Challenged Claims
[47]	**47.** The memory module of claim 45, wherein the each respective buffer circuit is configured to present one memory device load on each data line of the respective set of the plurality of sets of data lines to the memory controller.
[48]	**48.** The memory module of claim 45, wherein the data paths include read data paths, and wherein the read data paths include tristate buffers controlled by the logic.
[49]	**49.** The memory module of claim 48, wherein the memory read or write command is a memory read command, and wherein the tn state buffers in the read data paths regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the respective one or more of the subset of the memory devices to restore signal waveform shapes, and transmit regenerated signals to the memory controller via the respective set of the plurality sets of data lines.
[50]	**50.** The memory module of claim 48, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.
[51]	**51.** The memory module of claim 50, wherein each of the memory devices is eight bits wide, wherein the one or more memory devices in the subset of the memory devices include a single memory device outputting or receiving the respective portion of the data associated with the memory read or write command.
[52]	**52.** The memory module of claim 50, wherein each of the memory devices is four bits wide, wherein the one or more memory devices in the subset of the memory devices include a pair of memory devices each outputting or receiving half of the respective portion of the data associated with the memory read or write command.
[53.a]	**53.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

Ref. #	Listing of Challenged Claims
[53.b]	a module control circuit coupled to the set of control signal lines and configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce output address and control signals and a set of module control signals in response to the input address and control signals, the module control circuit having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections;
[53.c]	memory devices including first memory devices and second memory devices, the first memory devices including a first number of memory devices coupled to the first input/output connections and a second number of memory devices coupled to the second input/output connections, the second memory devices including a third number of memory devices coupled to the third input/output connections and a fourth number of memory devices coupled to the fourth input/output connections, wherein, in response to the output address and control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;
[53.d]	a plurality of buffer circuits each configured to receive the set of module control signals from the module control circuit, wherein each respective buffer circuit is coupled between respective one or more of the first memory devices and a respective set of the plurality of sets of data lines, and between respective one or more of the second memory devices and the respective set of the plurality of sets of data lines,
[53.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the set of module control signals to allow a respective section of the each N-bit wide data signal to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit,

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[53.f]	wherein the data paths include write data paths and read data paths, the write data paths including tristate buffers controlled by the logic and the read data paths including tristate buffers controlled by the logic,
[53.g]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and the respective one or more of the second memory devices from the memory controller; and
[53.h]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data signal lines,
[53.i]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.
[54]	**54.** The memory module of claim 53, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the plurality of sets of data lines to the memory controller.
[55]	**55.** The memory module of claim 54, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.

Ref. #	Listing of Challenged Claims
[56]	**56.** The memory module of claim 55, wherein each of the memory devices is eight bits wide, wherein the one or more of the first memory devices include a single memory device outputting or receiving the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command.
[57]	**57.** The memory module of claim 55, wherein each of the memory devices is four bits wide, wherein the one or more of the first memory devices include a pair of memory devices each outputting or receiving 4 bits of the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command.
[58.a]	**58.** A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:
[58.b]	memory devices including first memory devices and second memory devices;

Ref. #	Listing of Challenged Claims
[58.c]	a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce first output address and control signals in response to the first set of input address and control signals and second output address and control signals in response to the second set of input address and control signals, wherein, in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce a first set of module control signals in response to the first set of input address and control signals and a second set of module control signals in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;
[58.d]	a plurality of buffer circuits each configured to receive from the module control circuit the first set of module control signals and subsequently the second set of module control signals, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices,

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[58.e]	the each respective buffer circuit including data paths and logic that configures the data paths in response to the first set of module control signals to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to the second set of module control signals to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals,
[58.f]	wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and
[58.g]	a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data lines,
[58.h]	wherein the plurality of buffer circuits are mounted on the PCB between the memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

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[59]	**59.** The memory module of claim 58, further comprising module signal lines including a set of module signal lines coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets of the memory devices.
[60]	**60.** The memory module of claim 59, wherein the data paths include write data paths, and wherein the write data paths include tristate buffers controlled by the logic.
[61]	**61.** The memory module of claim 60, wherein the each respective buffer circuit is configured to present one memory device load on each data line of the respective set of the plurality of sets of data lines.
[62]	**62.** The memory module of claim 60, wherein the data paths include read data paths, and wherein the read data paths including tristate buffers controlled by the logic.
[63]	**63.** The memory module of claim 62, wherein each of the plurality of buffer circuits is a byte-wise buffer circuit, and wherein each set of the plurality of sets of data lines is eight bits wide.
[64]	**64.** The memory module of claim 63, wherein each of the memory devices is eight bits wide, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective portion of the data associated with the first memory read or write command.
[65]	**65.** The memory module of claim 63, wherein each of the memory devices is four bits wide, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective portion of the data associated with the first memory read or write command.