UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

NORTH STAR INNOVATIONS, INC.,
Patent Owner.

PTAB Case No.: To Be Assigned
U.S. Patent No. 6,127,875
Title: COMPLIMENTARY DOUBLE PUMPING VOLTAGE BOOST CONVERTER

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,127,875 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.123

Mail Stop **"PATENT BOARD"**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

Page

1. INTRODUCTION 1
2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW 1
2.1. Grounds for Standing (37 C.F.R. § 42.104(a)) 1
2.2. Notice of Lead and Backup Counsel and Service Information 1
2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1)) 2
2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2)) 2
2.5. Fee for *Inter Partes* Review 3
2.6. Proof of Service 3
3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B)) 3
4. BACKGROUND OF TECHNOLOGY 6
4.1. Voltage Boosting Circuits 6
4.2. Buffer 9
5. OVERVIEW OF THE 875 PATENT 11
6. 875 PATENT PROSECUTION HISTORY 17
7. CLAIM CONSTRUCTION 19
7.1. Applicable Law 19
7.2. Construction of Claim Terms 19
7.2.1. "buffer" limitations (claim 2) 20
7.2.1.1. "inverting buffer" 20
7.2.1.2. "non-inverting buffer" 21
7.3. Clarification of Other Claim Terms 22
7.3.1. "coupled" limitations (claims 1-3) 22
7.3.1.1. "coupled to" 22
7.3.1.2. "coupled between" 23
7.3.1.3. "coupled for receiving" 24
8. PERSON OF ORDINARY SKILL IN THE ART 25

9. DESCRIPTION OF THE PRIOR ART 26
9.1. U. S. Patent No. 5,267,201 ("Foss") 26
9.2. R. J. Baker et al., CMOS Circuit Design, Layout, and Simulation ("Baker").....29
9.3. S. Rabii et al., A 1.8V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6 (1997), 783-96 ("Rabii") 31
10. GROUND #1: CLAIMS 1 AND 3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING ANTICIPATED BY FOSS 33
10.1. Claim 1 is anticipated by Foss.....34
10.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:" 34
10.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;" 36
10.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;" 38
10.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and" 40
10.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal" 43
10.2. Claim 3 is anticipated by Foss.....45
10.2.1. [3.0] "The boost circuit of claim 1, further including:".....45
10.2.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and" 46
10.2.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."....47

11. GROUND #2: CLAIMS 1-3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING OBVIOUS OVER FOSS IN VIEW OF BAKER....49

11.1. Claim 1 is obvious over Foss in view of Baker....49

11.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"....49

11.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"....49

11.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"....49

11.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"....49

11.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal"....55

11.2. Claim 2 is obvious over Foss in view of Baker....57

11.2.1. [2.0] "The boost circuit of claim 1, further including:"....57

11.2.2. [2.1] "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and"....57

11.2.3. [2.2] "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor."....59

11.3. Claim 3 is obvious over Foss in view of Baker....61

11.3.1. [3.0] "The boost circuit of claim 1, further including:"....61

11.3.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and"....61

11.3.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."....61

11.4. Motivations to combine Foss and Baker....62

12. GROUND #3: CLAIMS 1-3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING OBVIOUS OVER FOSS IN VIEW OF RABII....65

12.1. Claim 1 is obvious over Foss in view of Rabii....65

12.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"....65

12.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"....65

12.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"....65

12.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"....65

12.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal"....70

12.2. Claim 2 is obvious over Foss in view of Rabii....72

12.2.1. [2.0] "The boost circuit of claim 1, further including:"....72

12.2.2. [2.1] "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and"....72

12.2.3. [2.2] "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor."....74

12.3. Claim 3 is obvious over Foss in view of Rabii....75

12.3.1. [3.0] "The boost circuit of claim 1, further including:"....75

12.3.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and" 75

12.3.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."....75

12.4. Motivations to combine Foss and Rabii.....76

13. CONCLUSION.....80

Exhibit List

Micron Exhibit #	Description
Ex. 1001	U.S. Patent No. 6,127,875 ("875 Patent")
Ex. 1002	File History for U.S. Patent No. 6,127,875 ("875 Patent FH")
Ex. 1003	Declaration of Dr. R. Jacob Baker ("Baker Decl.")
Ex. 1004	*Curriculum Vitae* of Dr. R. Jacob Baker
Ex. 1005	*Exhibit number not used*
Ex. 1006	U.S. Patent No. 5,267,201 ("Foss")
Ex. 1007[1]	Baker, R. Jacob et al., *CMOS Circuit Design, Layout, and Simulation*, IEEE Press, 1998 ("Baker")
Ex. 1008[2]	Rabii, Shahriar and Wooley, Bruce, A., *A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS*, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6 (1997), 783-96 ("Rabii")
Ex. 1009	U.S. Patent No. 4,229,667 ("Heimbigner")
Ex. 1010	IEEE Standard Dictionary of Electrical and Electronics Terms, ANSI/IEEE Std 100-1988 (4th ed. 1988) ("IEEE Standard Dictionary")
Ex. 1011	Chambers Dictionary of Science and Technology, Vol. 1, A-K (1974) ("Chambers Dictionary")
Ex. 1012	Mano, M. Morris, *Digital Logic and Computer Design*, Prentice-Hall, Inc., 1979 ("Mano")

[1] *See* Ex. 1016 for further publication information.

[2] *See* Exs. 1017 and 1018 for further publication information.

Micron Exhibit #	**Description**
Ex. 1013	Kang, Sung-Mo and Leblebici, Yusuf, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill Companies, Inc., 1996 ("Kang")
Ex. 1014	Modern Dictionary of Electronics, Revised and Updated (6th ed. 1997) ("Modern Dictionary of Electronics")
Ex. 1015	North Star's Second Amended Complaint filed in the co-pending litigation, *North Star Innovations, Inc. v. Micron Technology, Inc.*, 17-cv-506-LPS-CJB (D. Del.) ("Second Amended Complaint").
Ex. 1016	Declaration of James L. Mullins regarding R. J. Baker et al., *CMOS Circuit Design, Layout, and Simulations* ("Mullins Decl.")
Ex. 1017	Declaration of Ellen K. W. Mueller regarding S. Rabii et al., *A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS* ("Mueller Decl.")
Ex. 1018	Declaration of Rice Majors regarding S. Rabii et al., *A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS* ("Majors Decl.")

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123, Micron Technology, Inc. ("Petitioner" or "Micron") hereby petitions the Patent Trial and Appeal Board to institute an *inter partes* review of claims 1-3 of U.S. Patent No. 6,127,875, titled "Complimentary Double Pumping Voltage Boost Converter" (Ex. 1001, the "875 Patent"), and cancel those claims as unpatentable.

2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

2.1. Grounds for Standing (37 C.F.R. § 42.104(a))

Petitioner certifies that the 875 Patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review of the challenged claims of the 875 Patent on the grounds identified herein.

2.2. Notice of Lead and Backup Counsel and Service Information

Pursuant to 37 C.F.R. §§ 42.8(b)(3), 42.8(b)(4), and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

Lead Counsel	**Back-Up Counsel**
Jeremy Jason Lang Registration No. 73,604 (jason.lang@weil.com) Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3237; F: 650-802-3100	Jared Bobrow (jared.bobrow@weil.com) *Pro Hac Vice Application To Be Submitted* Postal & Hand-Delivery Address: Weil, Gotshal & Manges LLP 201 Redwood Shores Parkway Redwood Shores, CA 94065 T: 650-802-3034; F: 650-802-3100

Petitioner consents to service by electronic mail at the following addresses:

jason.lang@weil.com,
jared.bobrow@weil.com, and
Micron.Northstar.IPR@weil.com.

Pursuant to 37 C.F.R. § 42.10(b), Petitioner's Power of Attorney is attached.

2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner, Micron Technology, Inc., is the real-party-in-interest. No other parties exercised or could have exercised control over this petition; no other parties funded or directed this petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2))

North Star Innovations, Inc. ("Patent Owner" or "North Star") has asserted the 875 Patent and U.S. Patent Nos. 5,943,274 (the "274 Patent"), 7,171,526 (the "526 Patent"), and 6,465,743 (the "743 Patent") (collectively, "the asserted patents") against Micron in a co-pending litigation, *North Star Innovations, Inc. v. Micron Technology, Inc.*, 17-cv-506-LPS-CJB (D. Del.) ("Co-Pending Litigation"). North Star also has asserted the 875 Patent, the 274 Patent, U.S. Patent Nos. 6,917,555 (the "555 Patent"), and U.S. Patent No. 6,101,145 (the "145 Patent") in the following action: *North Star Innovations, Inc. v. Kingston Technology Co., Inc.*, 8:17-cv-1833 (C.D. Cal.) (complaint filed on October 20, 2017).

In addition to this Petition, Petitioner is filing an additional petition for *inter partes* review of the 875 Patent, one petition for *inter partes* review of the 274 Patent, two petitions for *inter partes* review of the 526 Patent, and one petition for *inter partes* review of the 743 Patent.[3]

The 875 Patent does not claim priority to any foreign or U.S. patent application.

2.5. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a), and any other required fees, to Deposit Account No. 601788.

2.6. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence address of record for the 875 Patent is attached.

3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

Ground #1: Claims 1 and 3 of the 875 Patent are invalid under (pre-AIA) 35 U.S.C. § 102(b) on the ground that they are anticipated by U.S. Patent No. 5,267,201 to Foss et al., entitled "High Voltage Boosted Word Line Supply Charge Pump Regulator For DRAM," filed on April 5, 1991 and issued on November 30, 1993 (Ex. 1006, "Foss").

[3] These petitions will be filed before May 3, 2018.

Ground #2: Claim 1-3 of the 875 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over Foss in view of the book entitled "CMOS Circuit Design, Layout, and Simulation," authored by R. J. Baker et al. and publicly available in 1997 (Ex. 1007, "Baker").

Ground #3: Claims 1-3 of the 875 Patent are invalid under (pre-AIA) 35 U.S.C. § 103(a) on the ground that they are obvious over Foss in view of the paper entitled "A 1.8-V Digital-Audio Sigma-Delta Modulator in 0.8-μm CMOS," authored by S. Rabii et al. and published in the IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, pp. 783-796, in June 1997 (Ex. 1008, "Rabii").

None of the prior art references on which these grounds are based was cited or considered by the Patent Office during prosecution of the 875 Patent.

These grounds are explained below and are supported by the Declaration of Dr. R. Jacob Baker (Ex. 1003, "Baker Decl.").

Statement of Non-Redundancy: The Grounds in this Petition (Petition 2) are not redundant of Ground #1 in the other petition for *inter partes* review of the 875 Patent (Petition 1) that Petitioner is filing contemporaneously herewith. The Grounds in Petition 2 are based on Foss, which is prior art under § 102(b), while Ground #1 in Petition 1 is based on Hsieh, which is prior art under § 102(e). Thus, to the extent that Patent Owner may seek to rely upon an earlier conception and reduction to practice, Foss is not cumulative of Hsieh. Also, Hsieh, unlike Foss,

has independent boost and phase signals, which completely removes the issue of whether these signals must be independent (claim elements 1.1-1.2 recite "phase signals," and claim elements 1.3-1.4 separately recite "a boost signal," creating the issue whether these must be independent and completely different signals). Moreover, Grounds #2 and #3 in Petition 2 are not redundant of Ground #1 in Petition 1 because they disclose a different implementation of a non-inverting buffer. Specifically, Foss in view of Baker or Rabii discloses a cascade of two inverters as a non-inverting buffer, while Hsieh discloses a circuit including an inverter and a NOR gate that is a non-inverting buffer when enabled.

In this petition (Petition 2), Grounds #1-3 are not redundant of one another, because Ground #1 asserts anticipation while Grounds #2 and #3 assert obviousness. Thus, issues unique to obviousness such as motivations to combine and reasonable expectation of success are relevant to Grounds #2 and #3 but not to Ground #1. Further, Ground #2 is based on Foss and Baker, and Ground #3 is based on Foss and Rabii. Baker is prior art under § 102(a), while Rabii is prior art under § 102(b). Thus, to the extent that Patent Owner may seek to rely upon an earlier conception and reduction to practice, Baker is not cumulative of Rabii. Therefore, Ground #2 is not redundant of Ground #3.

4. BACKGROUND OF TECHNOLOGY

4.1. Voltage Boosting Circuits

The evolution of integrated circuit technology has resulted in smaller devices that operate with lower supply voltages and lower power consumption. Ex. 1003, ¶33. A lower supply voltage, however, usually is unable to support complex functions such as, for example, integrated input/output circuits that practice industry standards (*e.g.*, PCIe (Peripheral Component Interconnect express) or USB (Universal Serial Bus) protocols). *Id*. To facilitate these functions, a voltage boosting circuit[4] has long been used to generate an output voltage greater than the input supply voltage. *Id.*, ¶35.

The 875 Patent does not claim to have invented voltage boosting circuits, nor could it. Ex. 1003, ¶36. Voltage boosting circuits have been known for decades before the filing of the 875 Patent. *Id.*, ¶35 (citing Ex. 1009, Abstract, 1:54-2:10 and Ex. 1007, pp. 84-88 to illustrate the well-known nature of such voltage boosting circuits). Indeed, the 875 Patent describes as admitted prior art a

[4] A voltage boosting circuit is often referred to as a "voltage boosting converter," "voltage boost circuit," "boost circuit," "voltage pump," "charge pump," "booster drive," etc. We use these terms interchangeably throughout this Petition.

basic voltage boosting circuit 10, which is depicted in FIGS. 1, 2, and 2A reproduced below.

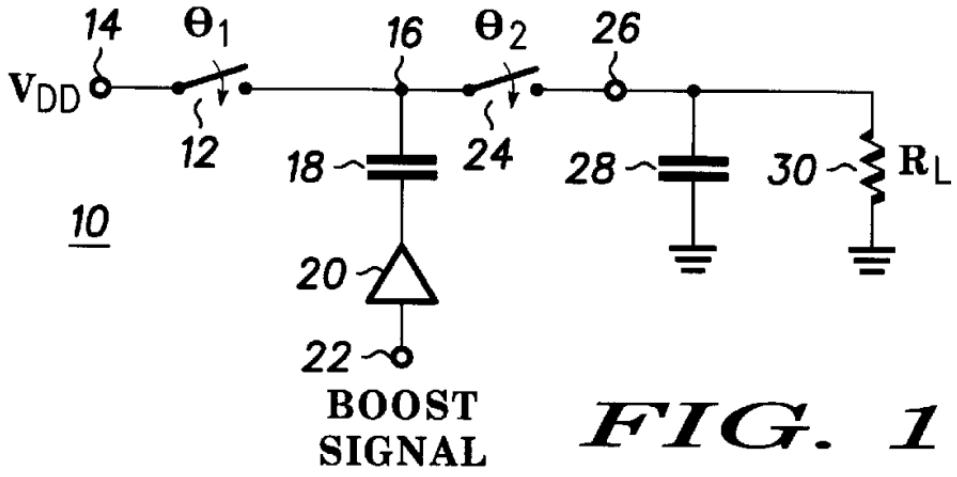


FIG. 1

- PRIOR ART -

Ex. 1001, FIG. 1

As shown in FIG. 1, an input voltage V_{DD} is supplied at terminal 14 and an output voltage is provided at terminal 26. Capacitor 18 is used to boost the output voltage, and capacitor 28 is used to store charge and to regulate the output voltage. A boost signal is provided to a terminal of capacitor 18 via buffer 20. The boost signal is used to generate a boost voltage for the voltage boosting circuit by charging capacitor 18. Ex. 1001, 1:23-43, FIG. 1. Furthermore, two switches 12 and 24 operate (*i.e.*, are turned on and off) in response to a pair of clock signals C1 and C2, which are opposite to each other and change periodically in clock cycles as shown in FIGS. 2A and 2 below. *Id.*, 1:23-50, FIGS. 2A and 2. Ex. 1003, ¶¶36-38.

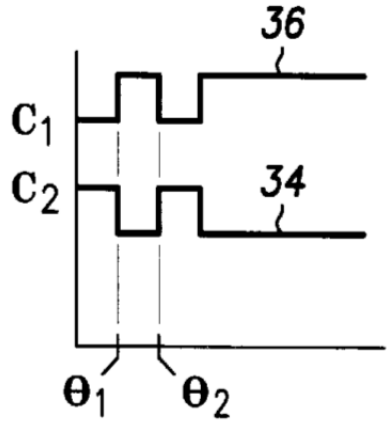


FIG. 2A

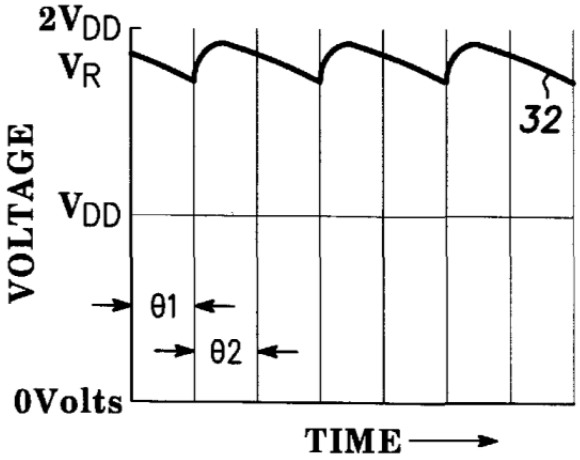


FIG. 2

Ex. 1001, FIG. 2A **Ex. 1001, FIG. 2**

This prior art voltage boosting circuit operates as follows. During the first half of a clock cycle (identified as θ_1 in FIGS. 2A and 2 above), switch 12 is closed, switch 24 is open, and the boost signal is at the ground level. As a result, the top terminal of capacitor 18 is connected to the supply voltage V_{DD}, and the output of buffer 20 is in a low voltage level state (*i.e.*, a potential at ground level), causing the bottom terminal of capacitor 18 to be at ground level. Thus, capacitor 18 is charged to the voltage V_{DD}. During the second half of the clock cycle (identified as θ_2 in FIGS. 2A and 2 above), switch 12 is open, switch 24 is closed, and the boost signal is increased to the supply voltage V_{DD}. As a result, the output of buffer 20 is in a high voltage level state (*i.e.*, a potential of V_{DD}), which causes the bottom terminal of capacitor 18 to have the potential of V_{DD}. Because capacitor 18 has been previously charged to the voltage V_{DD} in the first half of the

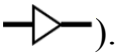
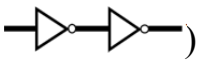
clock cycle, the potential at the top of capacitor 18 is then boosted to substantially $2V_{DD}$. Subsequently, capacitor 18 discharges to capacitor 28 and the load R_L to provide the output voltage. Consequently, the output voltage of the circuit is first boosted to substantially $2V_{DD}$ and then decays as current is delivered to the load R_L. In the first half of the next clock cycle, capacitor 18 is charged back to V_{DD} again, and the output voltage continues to decay as current is continuously delivered to the load R_L. Ex. 1001, 1:23-50, FIG. 1. Ex. 1003, ¶¶39-40.

The manner in which the output voltage (identified as V_R) changes over time is illustrated in FIG. 2, shown above. During each full clock cycle, the resulting output voltage is boosted only once (*i.e.*, at the beginning of the second half of the clock cycle, θ_2), and decays in the remaining time period, which is a large portion of the clock cycle. Ex. 1001, 1:43-52, FIG. 2; Ex. 1003, ¶41.

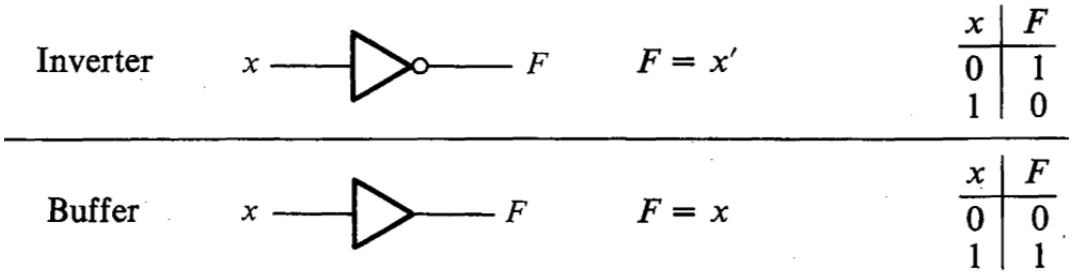
4.2. Buffer

In the context of integrated circuits, a buffer refers to an isolating circuit coupled between a driving circuit and a driven circuit that is used to prevent the driven circuit from influencing the driving circuit. Ex. 1010, pp. 6-7. In other words, a buffer decouples its output from its input, thus avoiding reaction between a driving and a driven circuit. Ex. 1011, p. 4. Ex. 1003, ¶42.

A buffer can be, for example, an inverting buffer or a non-inverting buffer. Ex. 1003, ¶¶43-44. A non-inverting buffer is often referred to simply as a buffer.

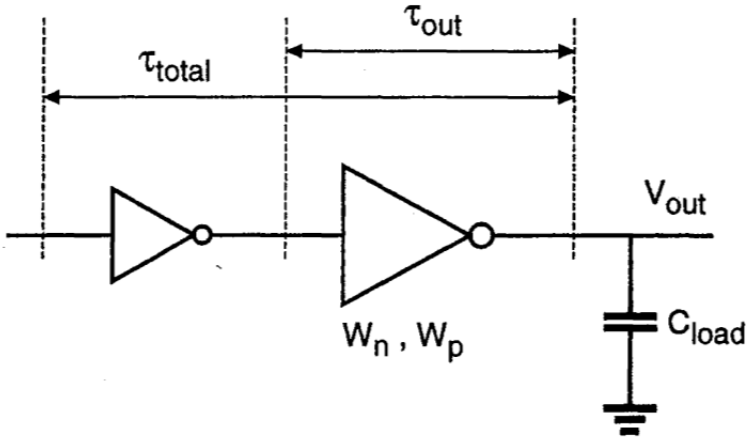
It was well known in the art to represent an inverting buffer using, for example, the schematic symbol of a NOT Gate (*i.e.*, ) and to represent a non-inverting buffer using, for example, the schematic symbol of a Buffer Gate (*i.e.*, ). *Id.* It was also well known in the art to implement a non-inverting buffer by sequentially connecting two inverting buffers into a cascade. Thus, a non-inverting buffer can also be represented by a cascade of two schematic symbols of a NOT Gate (*i.e.*, ). *Id.*, ¶45.

For example, Mano shows using the schematic symbol of a NOT Gate (*i.e.*, ) to represent an inverter (*i.e.*, inverting buffer), and using the schematic symbol of a Buffer Gate (*i.e.*, ) to represent a buffer (*i.e.*, non-inverting buffer). Ex. 1003, ¶46 (citing Ex. 1012, p. 9).



Ex. 1012, p. 9

For another example, Kang shows using a cascade of two inverters to implement a two-stage CMOS buffer (*i.e.*, non-inverting buffer). Ex. 1003, ¶47 (citing Ex. 1013, pp. 11-12).



Ex. 1013, p. 12

The terms "inverting buffer" and "non-inverting buffer" are construed in Section 7.2.1 below.

5. OVERVIEW OF THE 875 PATENT[5]

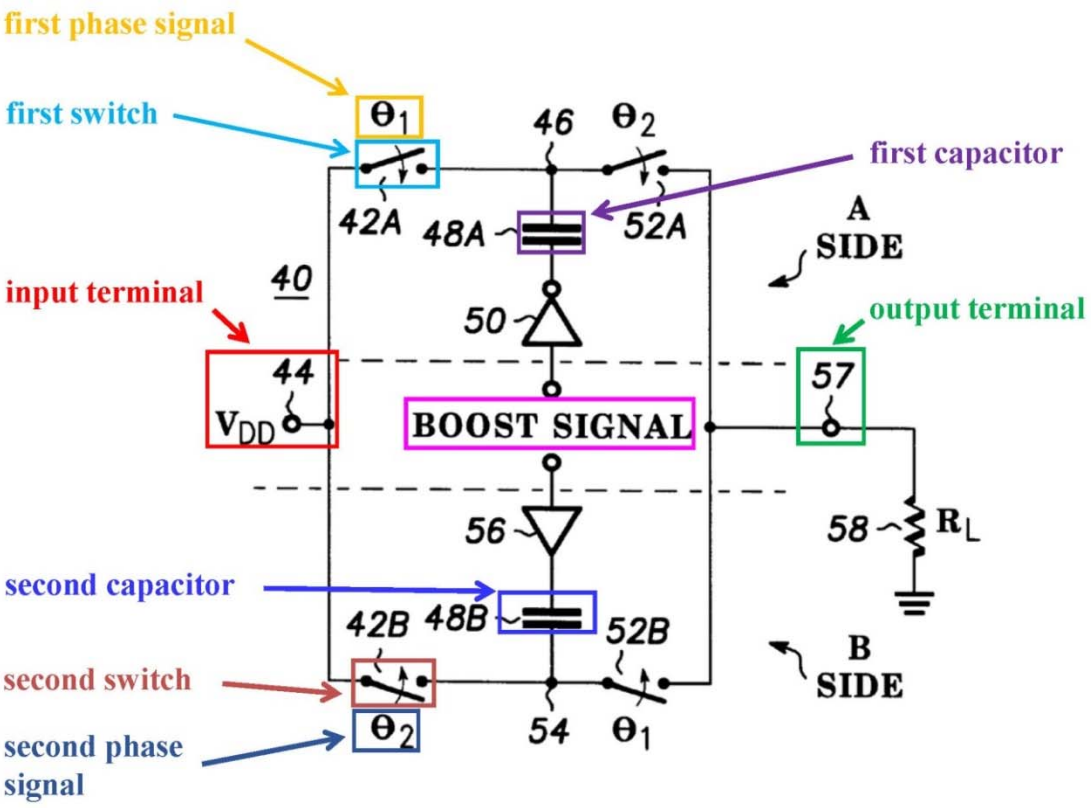
The 875 Patent relates generally to voltage boosting circuits that are suited to be manufactured in integrated circuit form. Ex. 1001, 1:5-9. The 875 Patent alleges that the prior art voltage boosting circuit shown in its FIG. 1 (reproduced and described above in Section 4.1) causes a significant amount of distortion to the output voltage. *Id.*, 1:51-52. To address this issue, the 875 Patent teaches a complementary double pumping voltage boost circuit that purportedly achieves less output voltage distortion than the prior art voltage boosting circuit described above. *Id.*, 2:66-3:3. In simple terms, the 875 Patent alleges that its voltage

[5] The 875 Patent was filed on August 13, 1998 and issued on October 3, 2000.

boosting circuit produces more of a static, level output than in the prior art. The 875 Patent alleges that the claimed boost circuit reduces the output voltage distortion because the circuit allegedly boosts the output voltage in both halves of a clock cycle, thus pumping the voltage twice as frequently as the prior art circuits and roughly halving the discharge time. *Id.*, 2:66-3:3. Ex. 1003, ¶52. Note that the claims of the 875 Patent do not require achieving less output voltage distortion or pumping the voltage at any specific frequency. Ex. 1001, 5:9-6:17. Ex. 1003, ¶53.

As illustrated below, the components and architecture of this voltage boost circuit are set forth in claims 1-3 of the 875 Patent and shown in FIG. 3 (reproduced below with colored annotations identifying the corresponding components).

> 1. A boost circuit having an input terminal and an output terminal, comprising:
> a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;
>
> a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;
>
> a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and
>
> a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal.
>
> (Ex. 1001, 5:9-6:3.)



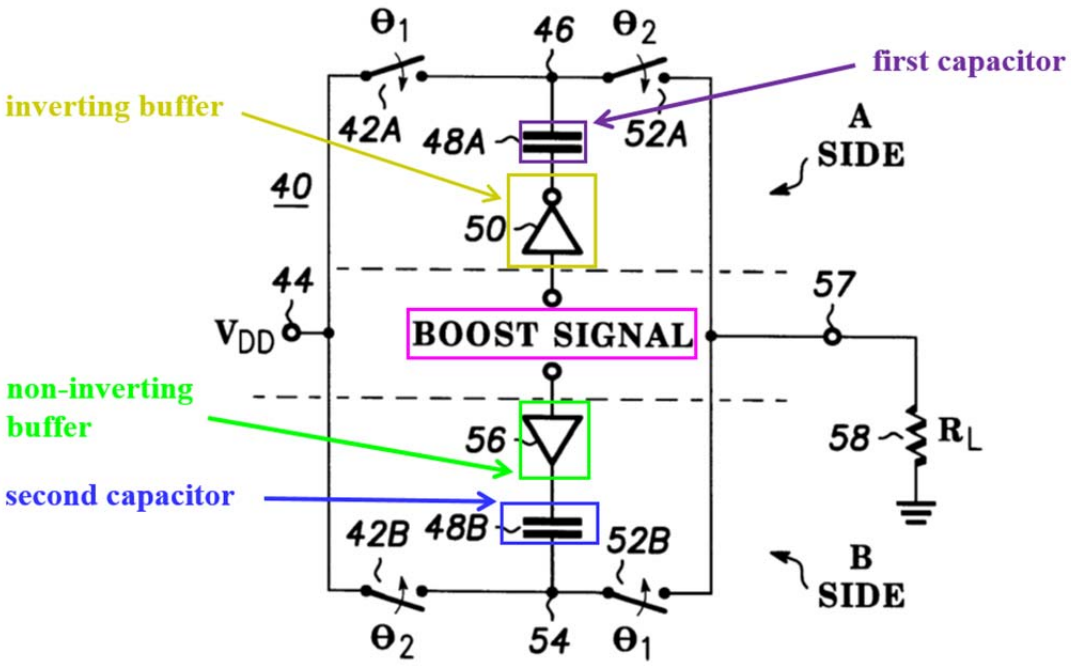
Ex. 1001, FIG. 3 (with annotations)

2. The boost circuit of claim 1, further including:

an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and

a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor.

(Ex. 1001, 6:4-10.)



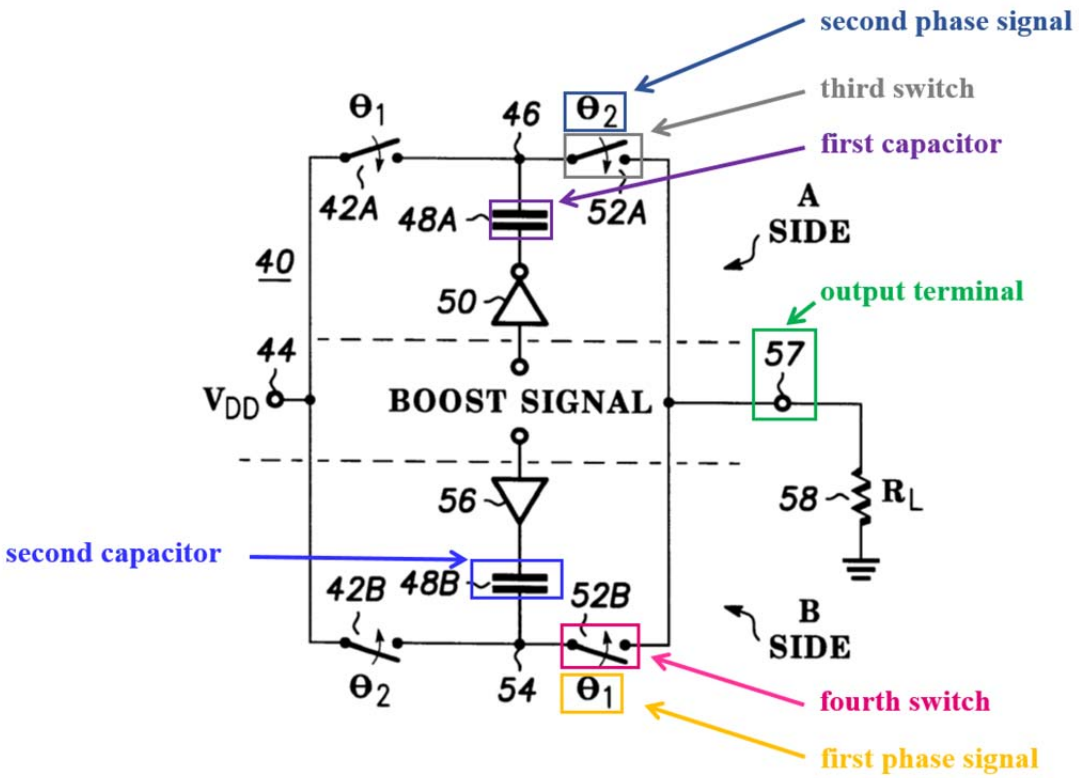
Ex. 1001, FIG. 3 (with annotations)

3. The boost circuit of claim 1, further including:

a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and

a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal.

(Ex. 1001, 6:11-17.)



Ex. 1001, FIG. 3 (with annotations)

As shown in FIG. 3, the voltage boost circuit includes two symmetric portions, an A side portion and a complementary B side portion. Each of these two portions is similar to the prior art voltage boosting circuit described above. Ex. 1001, 2:18-23. Ex. 1003, ¶55.

In operation, during the first half of a clock cycle, switches 42A and 52B are closed, switches 42B and 52A are open, and the boost signal is at the potential of V_{DD}. As a result, the A side portion operates similarly to the prior art voltage boosting circuit in the first half of a clock cycle. Specifically, the top terminal of capacitor 48A is connected to V_{DD} and the bottom terminal of capacitor 48A is

connected to the ground level (as a result of the high level boost signal being inverted by inverter 50), causing capacitor 48A to be charged to V_{DD}. In the meantime, assuming capacitor 48B has been charged to V_{DD} during a previous half cycle, then the B side portion operates similarly to the prior art voltage boosting circuit in the second half of a clock cycle. That is, the potential at the bottom terminal of capacitor 48B is boosted to substantially $2V_{DD}$. Capacitor 48B then discharges to load R_L to provide an output voltage at terminal 57. Consequently, the output voltage is first boosted to substantially $2V_{DD}$, and then decays as current is continuously delivered to load 58 (*i.e.*, resistor R_L). Ex. 1001, 2:38-56. Ex. 1003, ¶¶56-58.

Symmetrically, during the second half of the clock cycle, switches 42A and 52B are open, switches 42B and 52A are closed, and the boost signal is dropped to the ground level. The A side portion and the B side portion switch roles, where capacitor 48B is charged to V_{DD}, and capacitor 48A (which has been charged to V_{DD} in the previous half cycle) is boosted to substantially $2V_{DD}$ and then discharges to provide the output voltage. As a result, the output voltage again is first boosted to substantially $2V_{DD}$, and then decays as current is continuously delivered to load 58. Ex. 1001, 2:56-63. Ex. 1003, ¶¶59-61.

The manner in which the output voltage (identified as V_R) changes over time is illustrated in FIG. 4 shown below. The output voltage V_R is boosted in both

halves of each clock cycle, thus the voltage is pumped twice as frequently as in the admitted prior art circuit. Ex. 1003, ¶62.

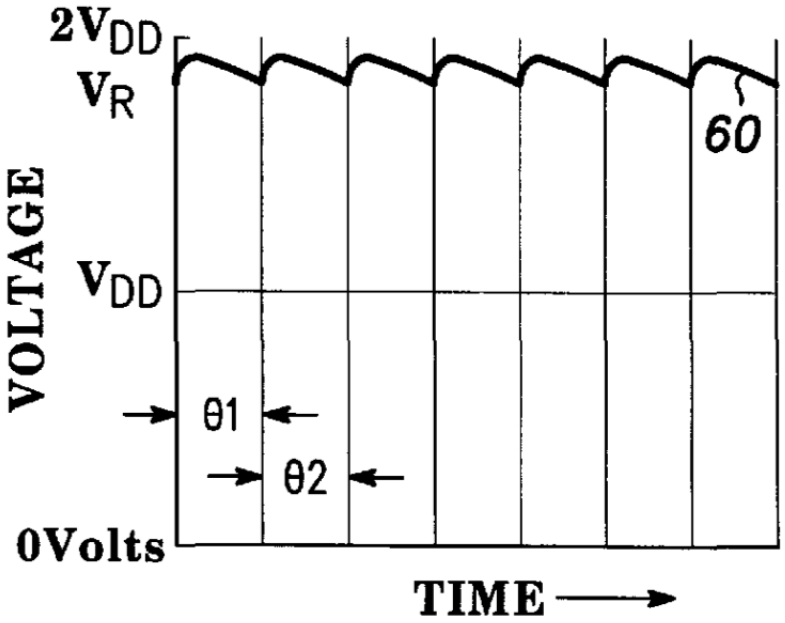


FIG. 4

Ex. 1001, FIG. 4

6. 875 PATENT PROSECUTION HISTORY

The application leading to the 875 Patent was originally filed on August 13, 1998 with 18 claims. Ex. 1002, pp. 8-24. In a Preliminary Amendment filed on February 17, 1999, Applicant added new claims 19-24. *Id.*, pp. 46-49. The added claims 19-21 were allowed in a first Office Action dated November 24, 1999, and

issued as claims 1-3 of the 875 Patent.[6] *Id.*, pp. 50-57, 75-78. During prosecution, the Examiner considered only three prior art references. Ex. 1003, ¶64.

[6] As to the prosecution of the non-issued claims, Applicant canceled original claims 10-18 in the Preliminary Amendment. In the first Office Action, claims 1 and 22 were rejected under 35 U.S.C. § 112; claim 1 was rejected as anticipated by U.S. Pat. No. 5,644,534 (Soejima); claims 2, 3, 5 and 6 were rejected as anticipated by U.S. Pat. No. 5,917,367 (Woo); and claims 23 and 24 were objected to as being dependent upon the rejected independent claim 22. Ex. 1002, pp. 50-57. In a Response dated April 7, 2000, Applicant canceled claims 1-9 and amended claims 22 and 23. *Id.*, pp. 60-64. In a second Office Action dated May 9, 2000, claim 22 was rejected under 35 U.S.C. § 112; and claims 22-24 were rejected as anticipated by U.S. Pat. No. 5,889,428 (Young). *Id.*, pp. 65-71. After Applicant canceled claims 22-24, the application was allowed and claims 19-21 issued as claims 1-3 respectively. *Id.*, pp. 73-78.

7. CLAIM CONSTRUCTION[7]

7.1. Applicable Law

The 875 Patent will expire on August 13, 2018 – a date which is before these proceedings will conclude. Accordingly, Petitioner has applied the claim construction principles of *Phillips* rather than the broadest reasonable interpretation standard applicable to non-expired patents. *See In re Rambus, Inc.*, 694 F.3d 42, 46 (Fed. Cir. 2012); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (*en banc*).

7.2. Construction of Claim Terms

All claim terms not specifically addressed in this Section have been accorded their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art (POSA) at the time of the invention and

[7] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the 875 Patent for failure to satisfy the requirements of 35 U.S.C § 112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition, or the constructions provided herein, shall be construed as a waiver of such challenge, or agreement that the requirements of 35 U.S.C. § 112 are met for any claim of the 875 Patent.

consistent with the intrinsic record. Petitioner respectfully submits that the following terms should be construed for this IPR:

7.2.1. "buffer" limitations (claim 2)

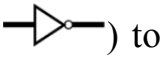
The 875 Patent does not define the term "buffer." Dictionary definitions for buffer include, for example, "an isolating circuit used to prevent a driven circuit from influencing a driving circuit," and "an electronic circuit to decouple the output of the buffer from its input, thus avoiding reaction between a driving and a driven circuit." Ex. 1010, pp. 6-7. Ex. 1011, p. 4. These definitions are consistent with the usage of "buffer" in the specification of the 875 Patent and consistent with the ordinary meaning of this term to a POSA. Ex. 1003, ¶¶77-78. Thus, under the *Phillips* standard, the term "buffer" would have been understood to mean "a circuit that isolates or decouples its output from its input." *Id.*, ¶78.

7.2.1.1. "inverting buffer"

The 875 Patent does not define the term "inverting buffer." A POSA would have understood that an inverting buffer refers to a buffer circuit that functions as an inverter. Ex. 1003, ¶¶44, 85. The Modern Dictionary of Electronics defines an inverter as "a circuit with one input and one output, and its function is to invert the input," and describes that "[w]hen the input is high, the output is low, and vice versa." Ex. 1014, p. 4. This definition is consistent with the usage of "inverting

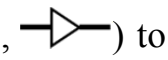
buffer" in the specification of the 875 Patent and consistent with the ordinary meaning of this term to a POSA. Ex. 1003, ¶86.

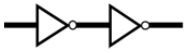
Thus, under the *Phillips* standard, the term "inverting buffer" would have been understood to mean "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is an inversion of its input (*i.e.*, when the input is high, the output is low, and vice versa)." Ex. 1003, ¶86.

The 875 Patent uses the schematic symbol of a NOT Gate (*i.e.*, ) to represent an inverting buffer (*e.g.*, inverting buffer 50 in FIG. 3). Ex. 1001, FIG. 3. The specification of the 875 Patent, however, does not describe how the inverting buffer is implemented. Ex. 1003, ¶87.

7.2.1.2. "non-inverting buffer"

The 875 Patent does not define the term "non-inverting buffer." A POSA would have understood that a non-inverting buffer refers to a buffer circuit whose output is not inverted from its input. Ex. 1003, ¶¶43, 88. Thus, under the *Phillips* standard, the term "non-inverting buffer" would have been understood to mean "a circuit that isolates or decouples its output from its input, and when enabled, generates an output that is not inverted from its input (*i.e.*, when the input is high, the output is high, and when the input is low, the output is low)." *Id.*, ¶89.

The 875 Patent uses the schematic symbol of a Buffer Gate (*i.e.*, ) to represent non-inverting buffer 56 in FIG. 3. Ex. 1001, FIG. 3. The specification of

the 875 Patent, however, does not describe how the non-inverting buffer is implemented. Furthermore, as discussed above in Section 4.2, a non-inverting buffer can be implemented by, for example, sequentially connecting two inverting buffers into a cascade. Thus, a non-inverting buffer can also be represented using, for example, a cascade of two schematic symbols of a NOT Gate (*i.e.*, ). Ex. 1003, ¶90.

7.3. Clarification of Other Claim Terms

Although the following terms need not be construed for this IPR, Petitioner provides the following clarifications.

7.3.1. "coupled" limitations (claims 1-3)

7.3.1.1. "coupled to"

A term "A 'coupled to' B"[8] would not have been understood to mean that A and B must be directly connected. For example, as shown in FIG. 3, the 875 Patent discloses terminal 46 of capacitor 48A being connected to output terminal 57 via switch 52A. The specification of the 875 Patent describes that terminal 46 is coupled to output terminal 57 via switch 52A. Ex. 1001, 2:33-35 ("Terminals 46

[8] "A" and "B" each represents a device or terminal in a circuit throughout this Petition.

and 54 are **coupled respectively via a pair of switches 52A and 52B to** output 57").[9] Ex. 1003, ¶69.

Moreover, the term "A 'coupled to' B" would not have been understood to mean that A and B are always connected. For example, the 875 Patent discloses terminal 46 of capacitor 48A being connected to output terminal 57 via switch 52A, even though switch 52A is open (thus disconnecting terminal 46 from output terminal 57) during the first half of each clock cycle. Ex. 1001, 2:38-56. Ex. 1003, ¶70.

7.3.1.2. "coupled between"

Similar to the term "coupled to," a term "A 'coupled between' B and C"[10] would not have been understood to mean that A must be directly connected to B and C. For example, as shown in FIG. 3, the 875 Patent describes that switch 42A is positioned between input terminal 44 and output terminal 57, with one end directly connected to input terminal 44 and another end connected to output terminal 57 via switch 52A. Ex. 1003, ¶72.

[9] Emphasis is added throughout unless otherwise noted.

[10] "C" represents a device or terminal in a circuit throughout this Petition.

Additionally, similar to the term "coupled to," the term "A 'coupled between' B and C" would not have been understood to mean that A is always connected to B and C. Ex. 1003, ¶73.

7.3.1.3. "coupled for receiving"

A term "A 'coupled for receiving' D"[11] would not have been understood to mean that A must receive the exact voltage signal of D. For example, as shown in FIG. 3, the 875 Patent describes that capacitor 48A is "coupled for receiving" a boost signal via inverting buffer 50, and that capacitor 48B is "coupled for receiving" the boost signal via non-inverting buffer 56. Ex. 1003, ¶74. Yet, when the boost signal goes through a buffer, the output is not the exact same signal that was input to the buffer, but instead is a signal that is pulled from a power or ground rail depending on the value of the input and the type of buffer (*e.g.*, inverting, non-inverting). *Id*.

A term "A 'coupled for receiving' D" would not have been understood to mean that A must directly receive D. For example, the 875 Patent describes that capacitor 48A is "coupled for receiving" a boost signal by indirectly receiving an inversion of the logical value of the boost signal via inverting buffer 50, and that

[11] "D" represents a signal throughout this Petition.

capacitor 48B is "coupled for receiving" the boost signal by indirectly receiving the logical value of the boost signal via non-inverting buffer 56. Ex. 1003, ¶75.

Additionally, similar to the terms "coupled to" and "coupled between," the term "A 'coupled for receiving' D" would not have been understood to mean that A always receives (directly or indirectly) the logical value of D or an inversion of the logical value of D. Ex. 1003, ¶76.

8. PERSON OF ORDINARY SKILL IN THE ART

A POSA with respect to the technology described in the 875 Patent would be a person with at least a Bachelor of Science degree in electrical engineering or a closely related field, along with at least 4-5 years of experience in the design of integrated circuits. An individual with an advanced degree in a relevant field would require less experience in the design of integrated circuits. Ex. 1003, ¶¶27-31.

9. DESCRIPTION OF THE PRIOR ART

9.1. U. S. Patent No. 5,267,201 ("Foss")[12]

Foss discloses a prior art voltage boosting circuit that is the same as the complementary double pumping voltage boost circuit described in the 875 Patent. Specifically, like the voltage boosting circuit of the 875 Patent, Foss' voltage boosting circuit has two symmetric portions that operate to alternately provide a boosted voltage. Ex. 1006, 1:48-51, FIG. 1. Ex. 1003, ¶109. Furthermore, Foss' voltage boosting circuit has the same architecture and components, and operates in the same manner, as the 875 Patent's voltage boost circuit. Ex. 1006, 1:24-54, FIG. 1. Ex. 1003, ¶110.

Foss' voltage boosting circuit is shown in FIG. 1, reproduced below with colored annotations identifying some of the corresponding components set forth in the claims and shown in FIG. 3 of the 875 Patent (*see* Section 5 above).

[12] Foss was filed on April 5, 1991 and issued on November 30, 1993, and is therefore prior art at least under § 102(b). *See* Ex. 1006. Foss was not cited to or discussed by the Examiner during prosecution of the 875 Patent. *See* Section 6 above.

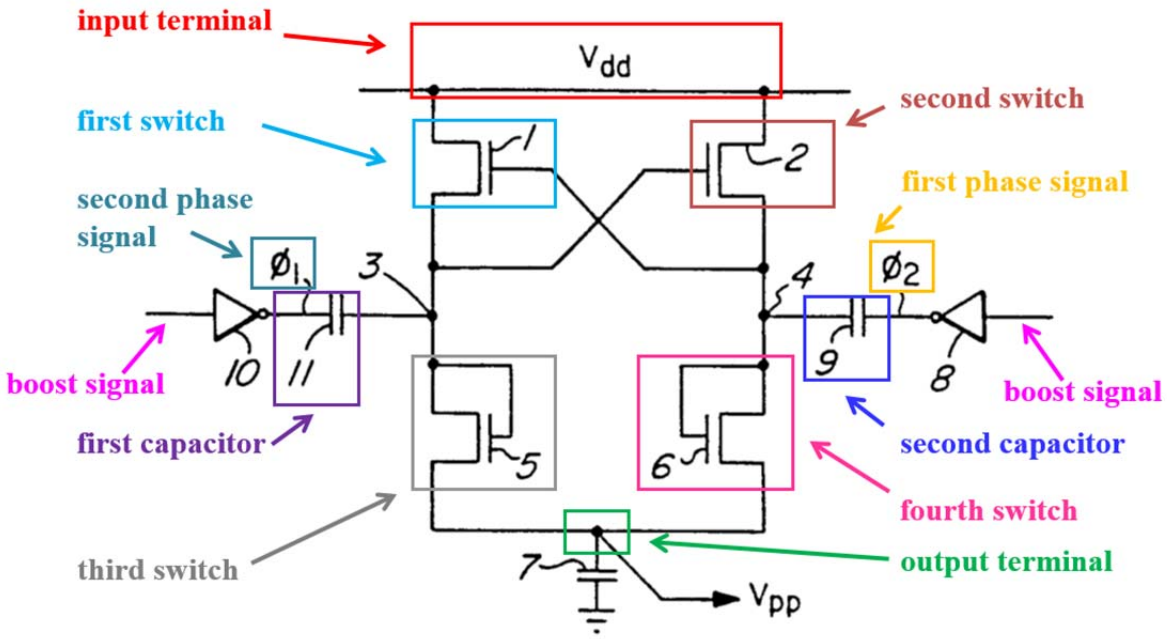


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

As shown in FIG. 1 and described in the specification, Foss' voltage boosting circuit has transistor 1 coupled between voltage rail V_{dd} and an output terminal that provides output voltage V_{pp} to load capacitor 7. Similarly, the voltage boosting circuit has transistor 2 coupled between voltage rail V_{dd} and the output terminal. Ex. 1006, 1:27-35, 45-47, FIG. 1. Transistor 1 is operated by clock signal ϕ_2 and transistor 2 is operated by another clock signal ϕ_1. As shown in FIG. 2 below, those two clock signals are opposite to each other. *Id.*, 1:40-44, 49-50, FIGS. 1 and 2. Ex. 1003, ¶¶111-112, 115.

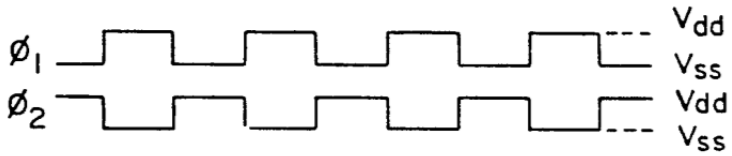


FIG. 2
PRIOR ART
Ex. 1006, FIG. 2

As shown in FIG. 1, Foss' voltage boosting circuit also has capacitor 11 with a right-side terminal coupled to the output terminal and a left-side terminal coupled for receiving clock signal ϕ1, and capacitor 9 with a left-side terminal coupled to the output terminal and a right-side terminal coupled for receiving clock signal ϕ2. Ex. 1006, 1:36-44, FIG. 1. Foss further describes that the two clock signals ϕ1 and ϕ2 are provided by the same oscillator. *Id.*, 6:27-30. Ex. 1003, ¶¶116-117.

Additionally, Foss' voltage boosting circuit has transistor 5 coupled between the right-side terminal of capacitor 11 and the output terminal, and transistor 6 coupled between the left-side terminal of capacitor 9 and the output terminal. Transistors 5 and 6 are operated by clock signals ϕ1 and ϕ2 respectively. Ex. 1006, 1:27-35, FIG. 1. Ex. 1003, ¶¶113-1114.

Foss further describes that this voltage boosting circuit operates in the same manner as the voltage boost circuit of the 875 Patent. Basically, like the voltage boost circuit of the 875 Patent, as the two clock signals ϕ1 and ϕ2 are opposite as shown in FIG. 2, the two capacitors 9 and 11 alternately charge from voltage rail

V_{dd} and discharge to load capacitor 7 to provide output voltage V_{pp}. Notably, Foss states that operation of such a circuit was "well known" at the time Foss was filed. Ex. 1006, 1:48-54, FIGS. 1 and 2. Ex. 1003, ¶¶118-119.

9.2. R. J. Baker et al., CMOS Circuit Design, Layout, and Simulation ("Baker")[13]

In Subchapter 18.3, Baker discusses the design of voltage generators and, in particular, the generation of two opposite signals to operate a voltage pump. Ex. 1007, pp. 84-92. Particularly, Baker shows a voltage pump circuit in Figure 18.17 (reproduced below). *Id.*, pp. 85-87. Ex. 1003, ¶121.

[13] Baker was published, cataloged, and publicly available in MIT Libraries at least in September 1997. *See* Ex. 1016. Thus, Baker is prior art at least under § 102(a). Baker was not cited to or discussed by the Examiner during prosecution of the 875 Patent. *See* Section 6 above.

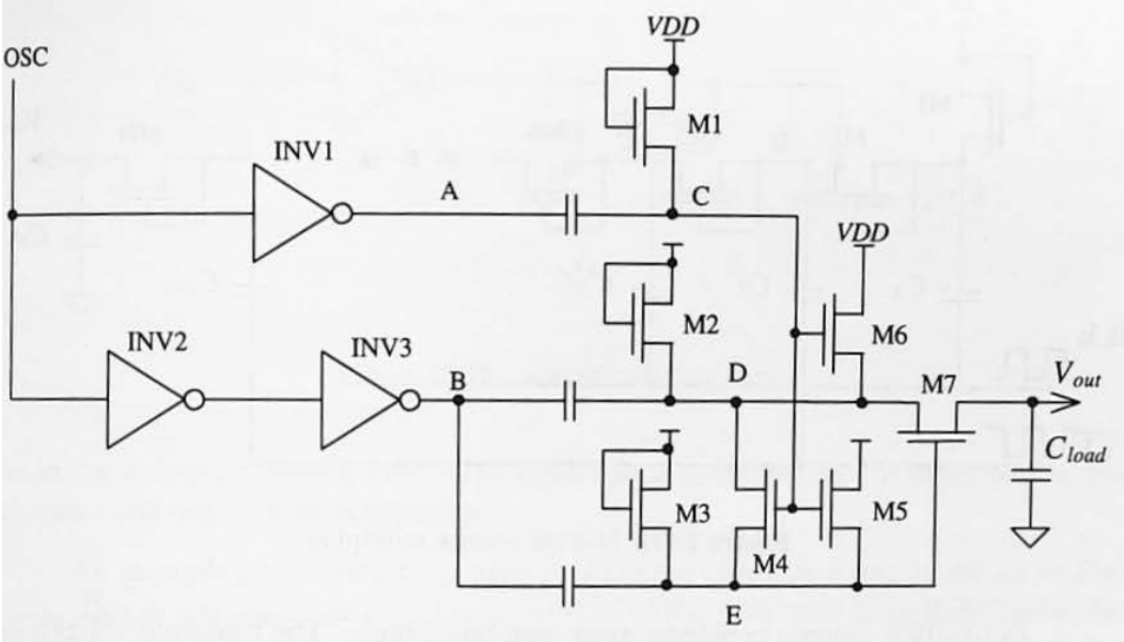


Figure 18.17 Increased efficiency voltage pump.

Ex. 1007, Figure 18.17

As shown in Figure 18.17, an oscillator OSC and three inverters INV1-INV3 collectively generate two clock signals for driving the remaining portion of the voltage pump circuit. An oscillator signal generated from oscillator OSC is inverted by inverter INV1 to generate a first clock signal at terminal A. The same oscillator signal also is inverted by inverter INV2, and then inverted again by inverter INV3, to generate a second clock signal at terminal B. Ex. 1007, p. 87. As discussed above in Sections 4.2 and 7.2.1, inverter INV1 is an inverting buffer, and the cascade of inverters INV2 and INV3 is a non-inverting buffer. Ex. 1003, ¶122.

Moreover, like clock signals C1 and C2 in the 875 Patent (Ex. 1001, FIG. 2A) and clock signals ϕ1, ϕ2 in Foss (Ex. 1006, FIG. 2), the two clock signals generated at terminals A and B are opposite to each other because they are generated by passing the same oscillator signal through an inverting buffer and a non-inverting buffer respectively. Ex. 1007, Figure 18.17. Ex. 1003, ¶123. Furthermore, like the clock signals ϕ1, ϕ2 in Foss (Ex. 1006, FIG. 1), these two clock signals are output from buffers (*e.g.*, inverting buffer INV1 and non-inverting buffer INV2-INV3) and supplied to capacitors. Ex. 1007, Figure 18.17. Ex. 1003, ¶124.

9.3. S. Rabii et al., A 1.8V Digital-Audio Sigma-Delta Modulator in 0.8-µm CMOS, IEEE Journal of Solid-State Circuits, Vol. 32, No. 6 (1997), 783-96 ("Rabii")[14]

Rabii shows a boosted clock driver circuit in Fig. 12 (reproduced below), and describes using this circuit to generate two opposite signals for operating a voltage pump. Ex. 1008, p. 791. Ex. 1003, ¶¶125-126.

[14] Rabii was published, cataloged, and publicly available at least in June 1997. *See* Ex. 1017 and Ex. 1018. Thus, Rabii is prior art at least under § 102(b). Rabii was not cited to or discussed by the Examiner during prosecution of the 875 Patent. *See* Section 6 above.

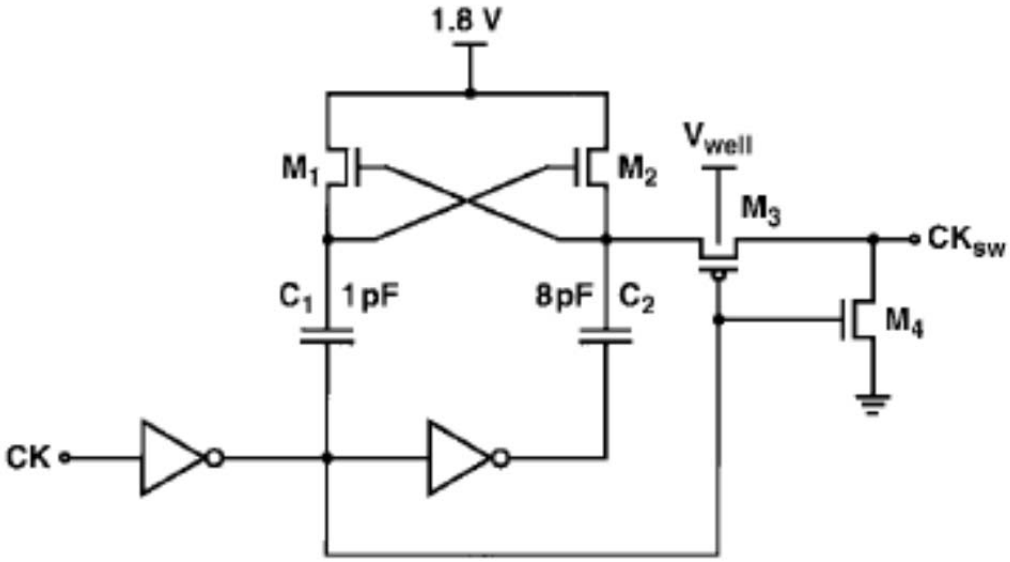


Fig. 12. Boosted clock driver.

Ex. 1008, Fig. 12

As shown in Fig. 12, a clock generation circuit including a cascade of two inverters generates two opposite clock signals from an input clock signal CK. In operation, input clock signal CK is inverted by the left inverter to generate a first clock signal, which is received by capacitor C_1. The first clock signal also is inverted by the right inverter to generate a second clock signal, which is received by capacitor C_2. Ex. 1008, p. 791. Thus, like clock signals C1 and C2 in the 875 Patent (Ex. 1001, FIG. 2A) and clock signals ϕ1, ϕ2 in Foss (Ex. 1006, FIG. 2), the two clock signals received at capacitors C_1 and C_2 are opposite to each other. Ex. 1003, ¶¶126-128. As discussed above in Sections 4.2 and 7.2.1, the left inverter is an inverting buffer, and the cascade of the two inverters is a non-inverting buffer. *Id.*, ¶126.

Moreover, Rabii describes that the boosted clock driver circuit operates essentially in the same manner as the voltage boosting circuit of the 875 Patent to provide a boosted voltage. Rabii describes a method of first charging a capacitor (*e.g.*, capacitor C_1 or C_2) to V_{DD}, then changing the voltage at the bottom terminal of that capacitor to V_{DD} by manipulating the input clock signal CK (*i.e.*, the voltage at the bottom terminal of capacitor C_1 is V_{DD} when CK is low, and the voltage at the bottom terminal of capacitor C_2 is V_{DD} when CK is high). As a result, the output voltage of that capacitor (*i.e.*, at its top terminal) is boosted to nearly $2V_{DD}$. Ex. 1008, p. 791, col. 1 ("Capacitors C_1 and C_2 are charged to V_{DD} via the cross-coupled NMOS transistors M1 and M2. When the input clock, CK, goes high, the output voltage, CK_{SW}, approaches 2 V_{DD}"). Ex. 1003, ¶¶129-130.

10. GROUND #1: CLAIMS 1 AND 3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING ANTICIPATED BY FOSS

To the extent that the phase signals of the 875 Patent need not be independent of, and may be derived from, the boost signal (*see* claims limitation [1.1]-[1.4] below), Foss discloses the "first phase signal," "second phase signal," and "boost signal." Patent Owner appears to take this position in the district court proceeding. For example, in its Second Amended Complaint, Patent Owner alleges that the claimed "phase signal" is "an inverted form of the boost signal." Ex. 1015, p. 10. Claim 1, however, separately claims a "boost signal" and a "phase signal," and FIG. 3 of the 875 Patent shows separate "boost" and "phase" signals.

Admittedly, however, the specification does not explicitly state that the boost and phase signals are independent. This assumption that the phase signals need not be independent of, and may be derived from, the boost signal applies to all the claim limitations containing the above terms in this Petition, including claim limitations [1.1]-[1.4] and [3.1]-[3.2] of Ground #1, and [1.1]-[1.4], [2.1]-[2.2] and [3.1]-[3.2] of Grounds #2 and #3.

10.1. Claim 1 is anticipated by Foss

10.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"

To the extent that the preamble is limiting, Foss discloses this limitation.

First, Foss describes a prior art voltage boosting circuit ("boost circuit") and illustrates it in FIG. 1 (reproduced below with annotations). Ex. 1006, 1:24-26 ("FIG. 1 illustrates a **voltage boosting circuit** according to the prior art"). Ex. 1003, ¶188.

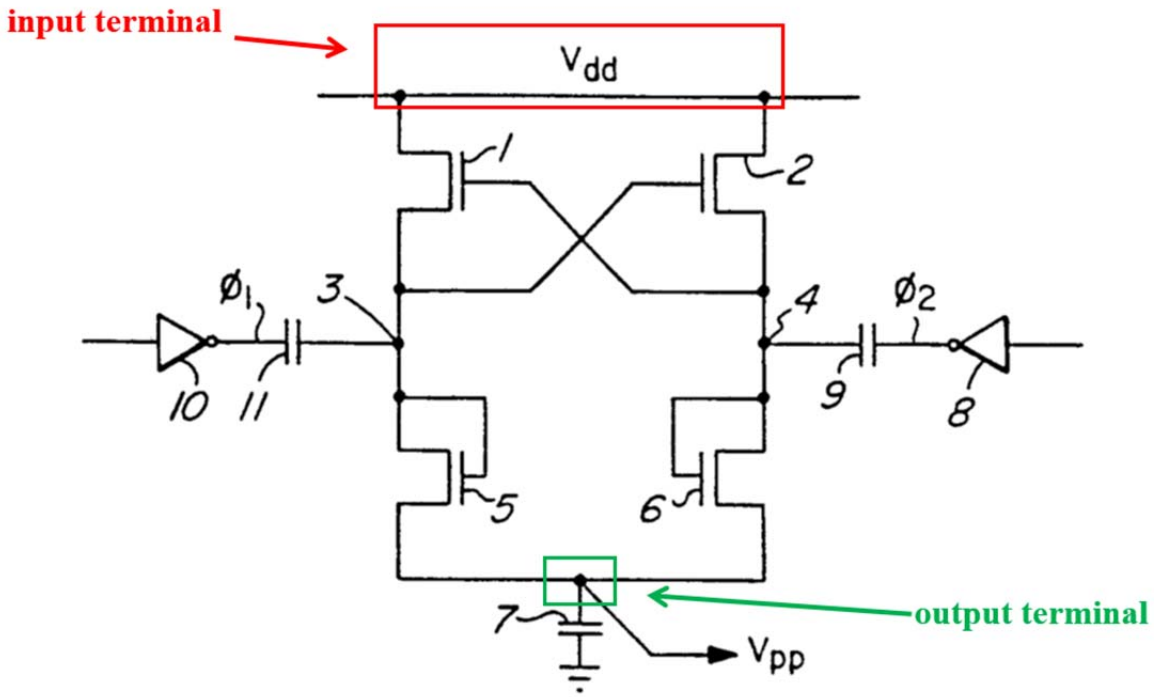


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, Foss discloses that the voltage boosting circuit ("boost circuit") has a voltage rail for receiving voltage V_{dd} ("input terminal"), and an output terminal for supplying output voltage V_{pp} ("output terminal"). Foss further discloses that sources of transistors 1 and 2 are both connected to voltage rail V_{dd} ("input terminal"). Ex. 1006, 1:27-29. Foss also discloses that the voltage boosting circuit has an output terminal V_{pp} at the junction of capacitor 7 and transistors 5 and 6. *Id.*, 1:45-47. Ex. 1003, ¶¶189-190.

10.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"

Foss discloses this limitation.

First, Foss discloses that transistor 1 ("first switch") is operated by clock signal ϕ2 ("first phase signal"). As shown in FIG. 1 (reproduced below with annotations), Foss discloses that transistor 1's gate is connected to node 4, which is connected to clock signal ϕ2 via capacitor 9. Ex. 1006, 1:36-37. A POSA would have understood that conducting of transistor 1 is controlled by clock signal ϕ2. Ex. 1003, ¶192-193. Thus, transistor 1 is a switch operated by clock signal ϕ2 ("first phase signal"). Ex. 1003, ¶193.

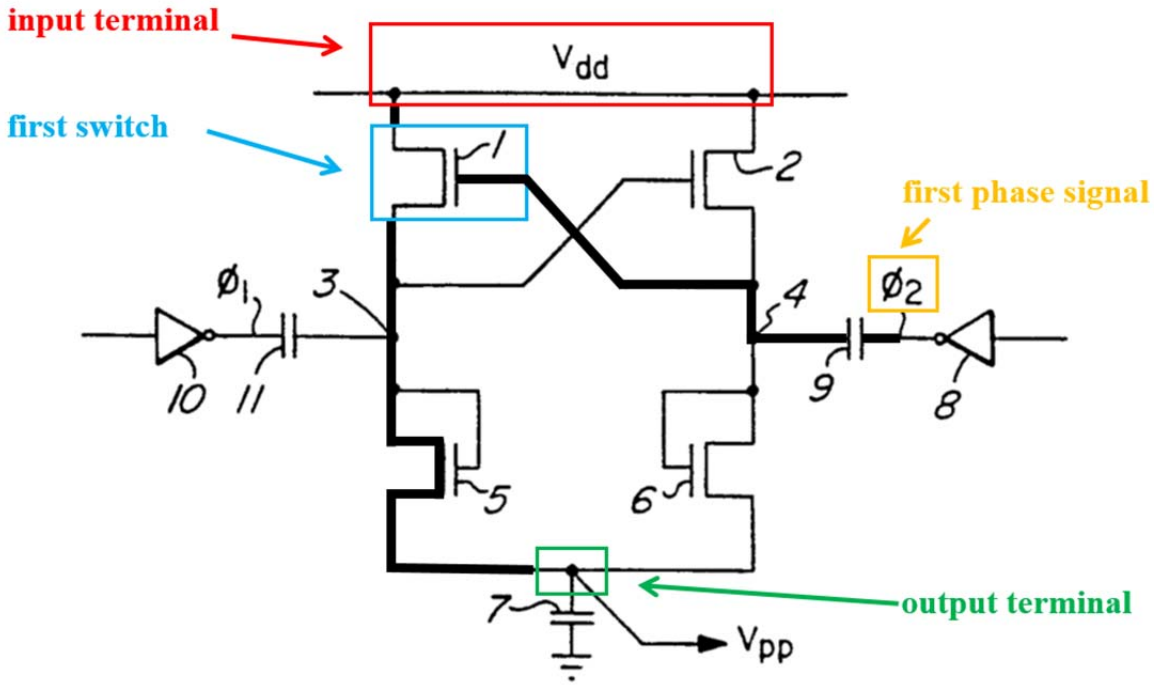


FIG. 1
PRIOR ART

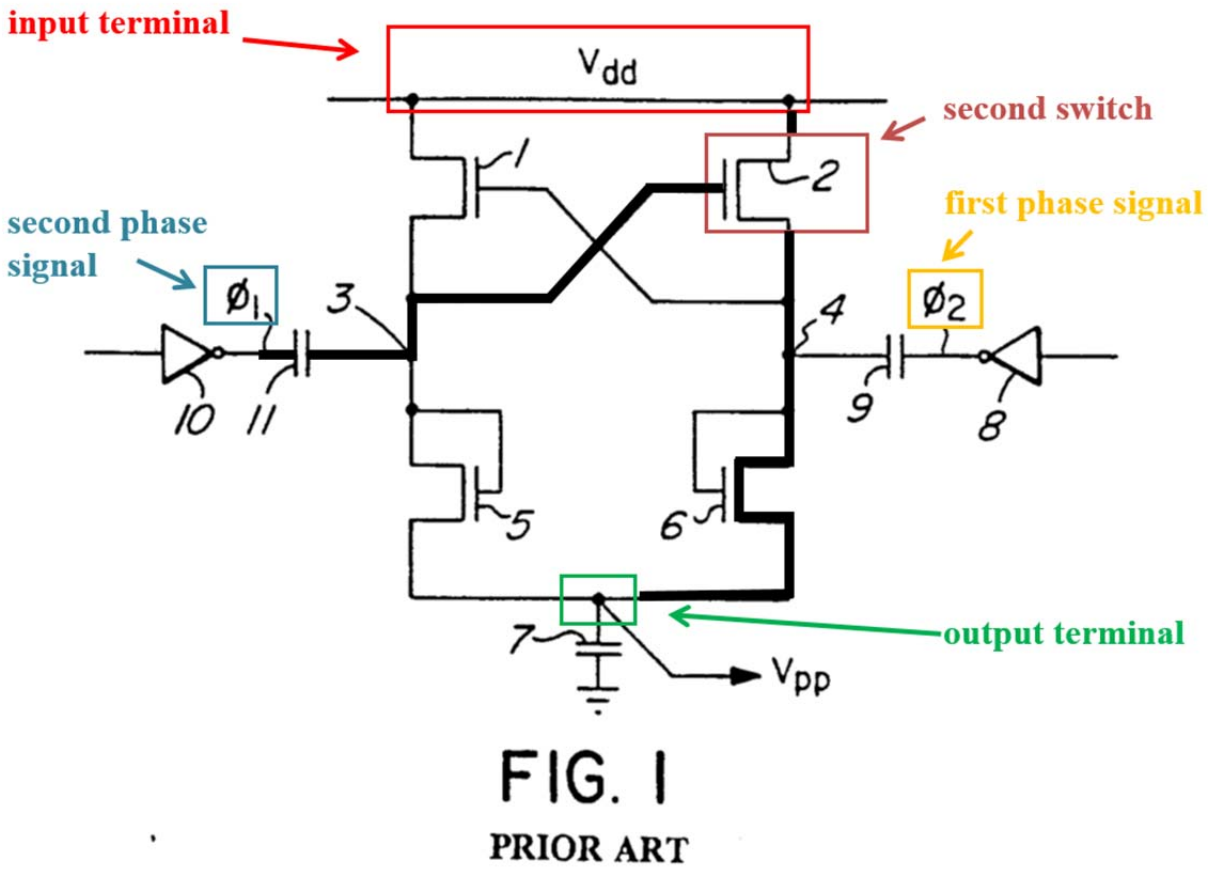
Ex. 1006, FIG. 1 (with annotations)

Second, Foss discloses that transistor 1 ("first switch") is coupled between voltage rail V_{dd} ("input terminal") and the output terminal V_{pp} ("output terminal"). Specifically, as shown in FIG. 1, the source of transistor 1 is directly connected to voltage rail V_{dd}, and the drain of transistor 1 is connected to the output terminal V_{pp} via transistor 5. Ex. 1006, 1:27-34, FIG. 1. Thus, transistor 1 is coupled between voltage rail V_{dd} and the output terminal V_{pp}. *See* Section 7.3.1.2 above. Ex. 1003, ¶¶194-195.

10.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"

Foss discloses this limitation.

First, Foss discloses that transistor 2 ("second switch") is operated by clock signal ϕ1 ("second phase signal"). As shown in FIG. 1 (reproduced below with annotations), Foss discloses that transistor 2's gate is connected to node 3, which is connected to clock signal ϕ1 via capacitor 11. Ex. 1006, 1:37-38. A POSA would have understood that conducting of transistor 2 is controlled by clock signal ϕ1. Ex. 1003, ¶196-197. Thus, transistor 2 is a switch operated by clock signal ϕ1 ("second phase signal"). *Id.*, ¶197.



Ex. 1006, FIG. 1 (with annotations)

As shown in FIG. 2, Foss also discloses that clock signal ϕ1 ("second phase signal") is opposite to clock signal ϕ2 ("first phase signal"). Ex. 1006, 1:49-50, FIG. 2 (reproduced below with annotations). Thus, transistor 2 is a switch operated by clock signal ϕ1, which is the second phase signal opposite to clock signal ϕ1 ("first phase signal"). Ex. 1003, ¶198.

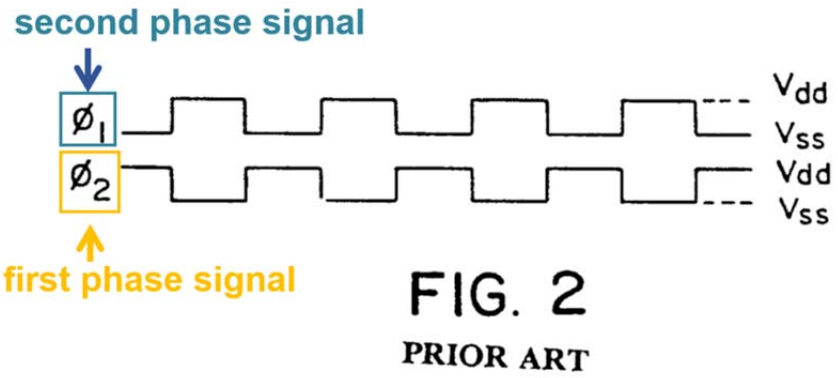


FIG. 2
PRIOR ART

Ex. 1006, FIG. 2 (with annotations)

Second, Foss discloses that transistor 2 ("second switch") is coupled between voltage rail V_{dd} ("input terminal") and output terminal V_{pp} ("output terminal"). Specifically, as shown in FIG. 1, the source of transistor 2 is directly connected to voltage rail V_{dd}, and the drain of transistor 2 is connected to output terminal V_{pp} via transistor 6. Ex. 1006, 1:27-34. Thus, transistor 2 is coupled between voltage rail V_{dd} and output terminal V_{pp}. *See* Section 7.3.1.2 above. Ex. 1003, ¶199.

10.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"

Foss discloses this limitation.

First, Foss discloses that capacitor 11 ("first capacitor") has a right-side terminal ("first terminal") coupled to output terminal V_{pp} ("output terminal"). As shown in FIG. 1 (reproduced below with annotations), Foss discloses that the right-side terminal of capacitor 11 is connected to node 3, which is connected to output

terminal V_{pp} via transistor 5. Ex. 1006, 1:27-34, 37-39, FIG. 1. Thus, the right-side terminal of capacitor 11 is coupled to output terminal V_{pp}. *See* Section 7.3.1.1 above. Ex. 1003, ¶¶201-202.

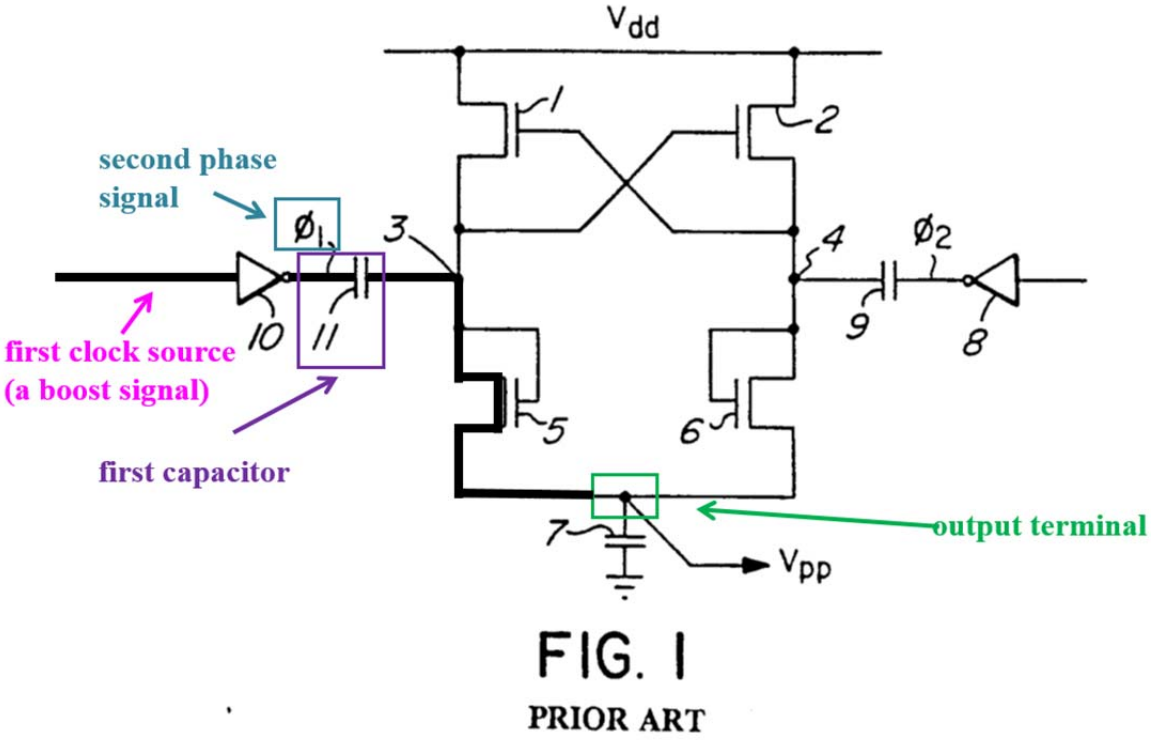


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, Foss discloses that capacitor 11 ("first capacitor") has a left-side terminal ("second terminal") coupled for receiving a first clock source ("a boost signal"). Specifically, as shown in FIG. 1, Foss discloses that the left-side terminal of capacitor 11 receives clock signal ϕ1 ("second phase signal"), which is inverted from a first clock source via inverter 10. Ex. 1006, 1:37-39 ("**another clock source is connected through an inverter 10 through capacitor 11 to node 3**"),

FIG. 1. Thus, the left-side terminal of capacitor 11 is coupled for receiving the first clock source. *See* Section 7.3.1.3 above. Ex. 1003, ¶202.

Moreover, the first clock source is a boost signal. Foss describes that the first clock source is input to the prior art voltage boosting circuit and is used to generate a boosted voltage. Ex. 1006, 1:25-51. Foss describes that an oscillator provides the first clock source, which is used to charge capacitor 11 through inverter 10. Capacitor 11 then generates a boosted voltage and outputs it by discharging to capacitor 7. *Id.*, 1:25-26, 1:42-45 ("**the clock source output at the output of inverter 10 is shown as waveform ϕ1**"), 1:49-51 ("**As the levels of ϕ1 and ϕ2 vary as shown in FIG. 2, capacitors 9 and 11 alternately charge between V_{ss} and V_{dd} and discharge to capacitor 7**"), 6:27-30, 8:63-65, FIG. 1. Thus, the first clock source is a boost signal.[15] Ex. 1003, ¶204-205.

More specifically, Foss discloses that an oscillator generates the boost signal (the first clock source) and an inversion of the boost signal (a second clock source, see next limitation). Ex. 1006, 6:27-30 ("**the prior art pump … is driven by an oscillator 40, which provides the clock signals, e.g. ϕ_1, ϕ_2**"), 8:63-65 ("**said driving means is an oscillator providing both boosted and non-boosted,**

[15]In Foss, each of clock signals ϕ2 and ϕ1 ("first phase signal" and "second phase signal") is generated from a boost signal. Ex. 1003, ¶204.

inverted and non-inverted non-overlapping clocks"). The 875 Patent describes a boost signal for a boost circuit as a signal that is used to boost the voltage of a capacitor (*e.g.*, capacitors 48A, 48B) via a buffer (*e.g.*, inverting buffer 50, non-inverting buffer 56). Like the boost signal in FIG. 3 of the 875 Patent, here the first clock source is a signal that is used to boost the voltage of a capacitor (*i.e.*, capacitor 11) via a buffer (*i.e.*, inverter 10). Ex. 1003, ¶¶206-207.

10.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal"

Foss discloses this limitation.

First, Foss discloses that capacitor 9 ("second capacitor") has a left-side terminal ("first terminal") coupled to output terminal V_{pp} ("output terminal"). Specifically, as shown in FIG. 1 (reproduced below with annotations), Foss discloses that the left-side terminal of capacitor 9 is connected to node 4, which is connected to output terminal V_{pp} via transistor 6. Ex. 1006, 1:27-34, 36-37, FIG. 1. Thus, the left-side terminal of capacitor 9 is coupled to output terminal V_{pp}. *See* Section 7.3.1.1 above. Ex. 1003, ¶209-210.

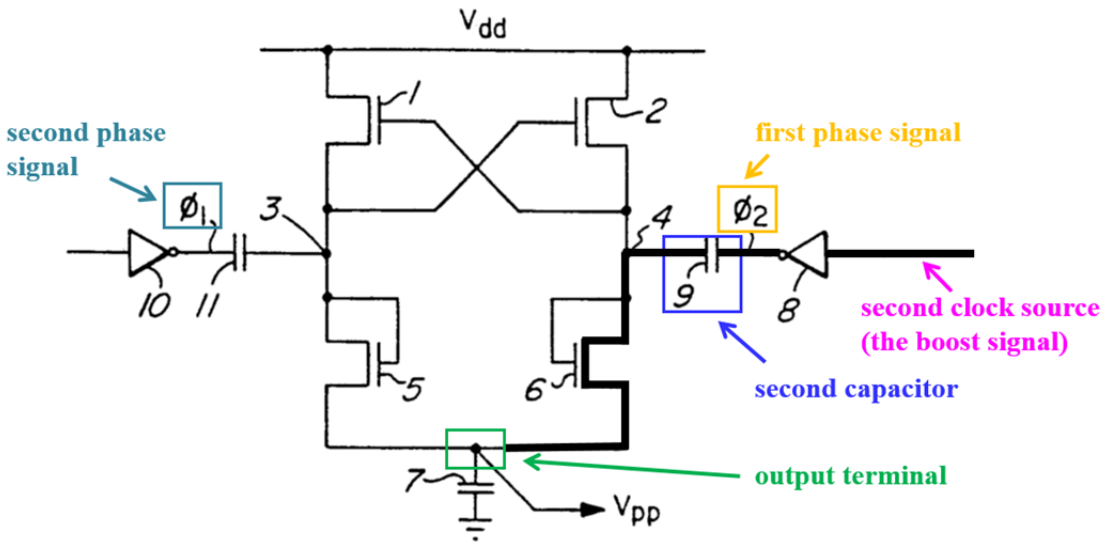


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, Foss discloses that capacitor 9 ("second capacitor") has a right-side terminal ("second terminal") coupled for receiving a second clock source (an inversion of the first clock source, which is "the boost signal"). Specifically, as shown in FIG. 1, Foss discloses that the right-side terminal of capacitor 9 receives clock signal ϕ2 ("first phase signal"), which is inverted from the second clock source via inverter 8. Ex. 1006, 1:36-37, FIG. 1. Thus, the right-side terminal of capacitor 9 is coupled for receiving the second clock source. *See* Section 7.3.1.3 above. Ex. 1003, ¶211.

Similar to above analysis for Claim [1.3] in Section 10.1.4, the second clock source is the boost signal. Ex. 1006, 1:25-26, 1:40-42, 1:49-51, 6:27-30, 8:63-65, FIG. 1. Ex. 1003, ¶212. Foss describes that both clock signals ϕ1 and ϕ2 are

provided by a common oscillator. Ex. 1006, 6:27-30 ("**the prior art pump … is driven by an oscillator 40, which provides the clock signals, e.g. ϕ_1, ϕ_2**"), 8:63-65 ("**said driving means is an oscillator providing both boosted and non-boosted, inverted and non-inverted non-overlapping clocks**"). These clock signals charge the respective capacitors to create a boosted voltage. *Id.*, 1:24-26, 1:40-42, 1:49-51, 6:27-30, 8:63-65, FIG. 1. Ex. 1003, ¶¶212-213.

Foss discloses a single oscillator that generates these clock signals. Ex. 1006, 8:63-65 ("**an oscillator providing both … inverted and non-inverted non-overlapping clocks**"). Accordingly, the disclosed first clock source is the output of the oscillator ("non-inverted" clock), and is the claimed "boost signal." Foss discloses that the output of the oscillator is "inverted" to create the "inverted … non overlapping clock[]." *Id.*; Ex. 1003, ¶¶214-215 (explaining that "inverted … non-overlapping clock" refers to inverting the clock signal, *i.e.*, output of the oscillator). Accordingly, the disclosed second clock source is the inverted output of the oscillator, and is thus the claimed "boost signal" (the 875 Patent uses "boost signal" to refer to the inversion of the "boost signal" as well), see section 7.3.1.3.

10.2. Claim 3 is anticipated by Foss

10.2.1. [3.0] "The boost circuit of claim 1, further including:"

Foss discloses this limitation. *See* above analysis for Claim 1, Section 10.1.

10.2.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and"

Foss discloses this limitation.

First, Foss discloses that transistor 5 ("third switch") is operated by clock signal ϕ1 ("second phase signal"). As shown in FIG. 1 (reproduced below with annotations), Foss discloses that transistor 5's gate is connected to node 3, which is connected to clock signal ϕ1 via capacitor 11. Ex. 1006, 1:37-38. A POSA would have understood that clock signal ϕ1 controls when transistor 5 is conducting.[16] Thus, transistor 5 is a switch operated by clock signal ϕ1 ("second phase signal"). Ex. 1003, ¶¶218-221.

[16] Transistor 5 is a diode-connected transistor, and its conducting is controlled by the potential at node 3, which is derived from clock signal ϕ1. When the potential at node 3 is higher than a threshold voltage above V_{pp}, transistor 5 is conducting; otherwise, transistor 5 is not conducting. Ex. 1003, ¶114.

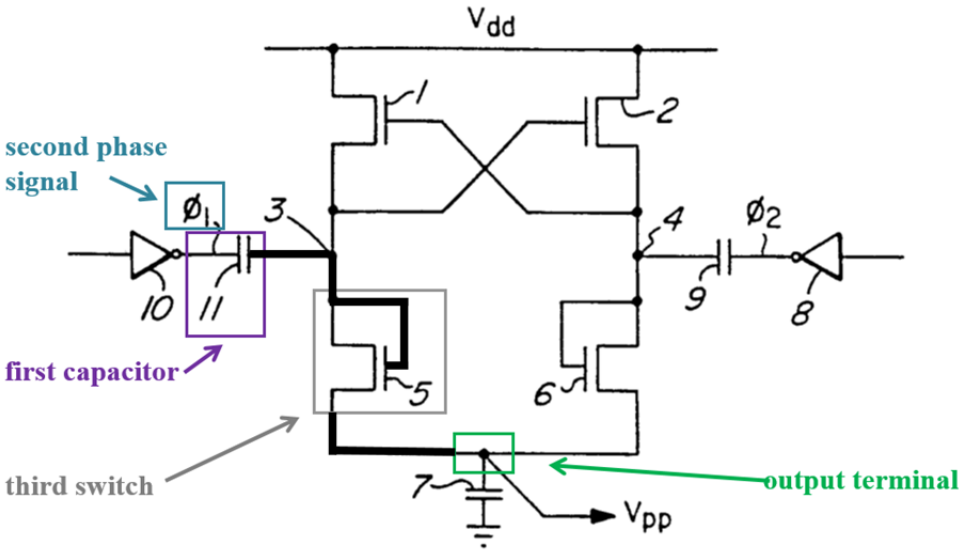


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, as shown in FIG. 1, Foss discloses that transistor 5 ("third switch") is coupled between the right-side terminal of capacitor 11 ("first terminal of the first capacitor") and output terminal V_{pp} ("output terminal"). Ex. 1006, 1:29-34, FIG. 1. Ex. 1003, ¶218-219.

10.2.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."

Foss discloses this limitation.

First, Foss discloses that transistor 6 ("fourth switch") is operated by clock signal ϕ2 ("first phase signal"). As shown in FIG. 1 (reproduced below with annotations), Foss discloses that transistor 6's gate is connected to node 4, which is connected to clock signal ϕ2 via capacitor 9. Ex. 1006, 1:36-37. A POSA would

have understood that clock signal ϕ2 controls when transistor 6 is conducting. Ex. 1003, ¶¶222-223. Thus, transistor 6 is a switch operated by clock signal ϕ2 ("first phase signal"). Ex. 1003, ¶223.

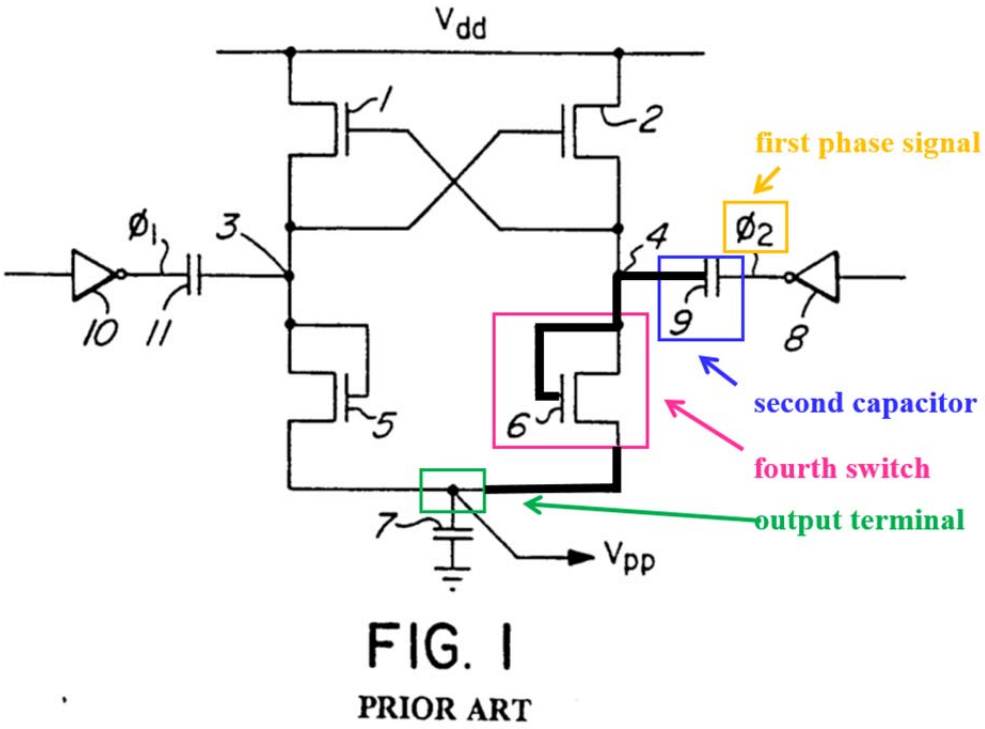


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, as shown in FIG. 1, Foss discloses that transistor 6 ("fourth switch") is coupled between the left-side terminal of capacitor 9 ("first terminal of the second capacitor") and output terminal V_{pp} ("output terminal"). Ex. 1006, 1:29-34, FIG. 1. Ex. 1003, ¶224.

11. GROUND #2: CLAIMS 1-3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING OBVIOUS OVER FOSS IN VIEW OF BAKER[17]

11.1. Claim 1 is obvious over Foss in view of Baker

11.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"

To the extent that the preamble is limiting, Foss discloses this limitation. *See* above analysis for Claim [1.0], Section 10.1.1.

11.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"

Foss discloses this limitation. *See* above analysis for Claim [1.1], Section 10.1.2.

11.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"

Foss discloses this limitation. *See* above analysis for Claim [1.2], Section 10.1.3.

11.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"

The prior art combination discloses this limitation.

---

[17] *See* Section 10 above (describing assumption that "boost" and "phase" signals need not be independent).

As illustrated above in Section 10.1.4, Foss discloses that capacitor 11 ("first capacitor") has a right-side terminal ("first terminal") coupled to output terminal V_{pp} ("output terminal"). *See* above analysis for Claim [1.3], Section 10.1.4.

To the extent that it is determined that Foss does not expressly disclose "coupled for receiving the boost signal" (*see infra*, next limitation) (*i.e.*, that the second clock source is the inverted version of the first clock source) because, for example, Foss does not illustrate in FIG. 1 the oscillator and inverter circuitry (*see* above analysis for Claim [1.3]-[1.4], Section 10.1.4-1.5), the combination of Foss in view of Baker discloses that limitation.

Adapting Foss in view of Baker also effects the current limitation as set forth below. Foss in view of Baker discloses this limitation as follows. First, Foss discloses that capacitor 11 receives clock signal ϕ1 ("second phase signal"), and capacitor 9 receives the opposite clock signal ϕ2 ("first phase signal"). As shown in FIG. 1 (reproduced below with annotations), capacitor 11 receives clock signal ϕ1 from inverter 10, and capacitor 9 receives clock signal ϕ2 from inverter 8. Ex. 1006, 1:36-44, FIG. 1. *See also* Section 10.1.4-1.5. Ex. 1003, ¶117.

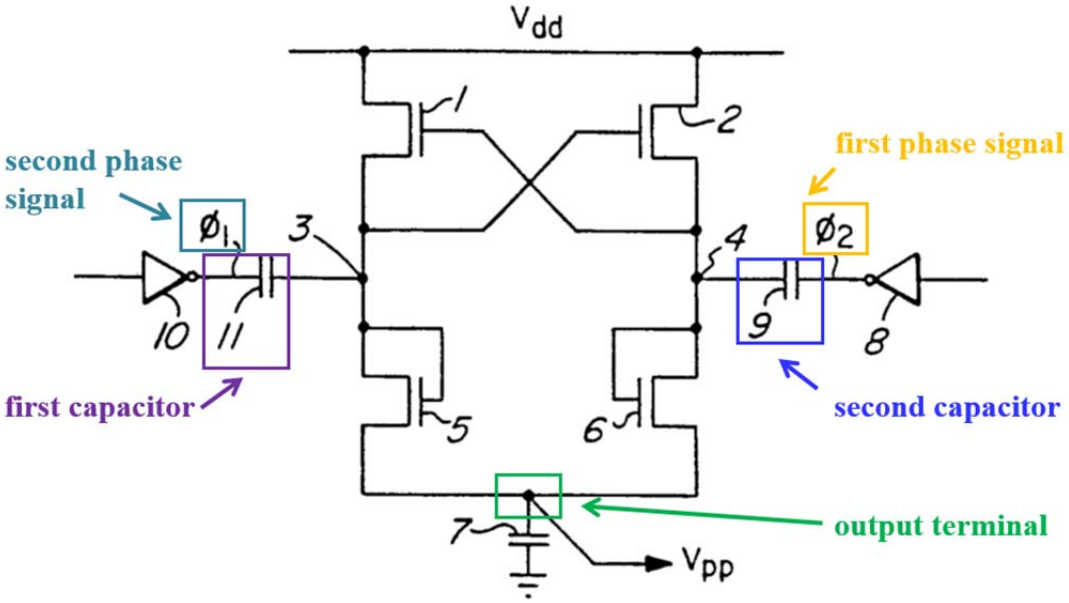


FIG. 1
PRIOR ART

Ex. 1006, FIG. 1 (with annotations)

Second, combining the teachings of Foss and Baker provides a structure for generating two opposite clock signals for Foss' voltage boosting circuit. Foss describes that both clock signals ϕ1 and ϕ2 are provided by a common oscillator. Ex. 1006, 6:27-30, 8:63-65. Ex. 1003, ¶234. Moreover, as shown in FIG. 2, the two clock signals ϕ1 and ϕ2 are opposite to each other. *See* above analysis for Claim [1.2], Section 10.1.3.

Like Foss, Baker discloses a clock generation circuit that uses an oscillator to generate two opposite clock signals from a common clock signal, but as shown

in Figure 18.17 (reproduced below with annotations), Baker details this circuitry. Ex. 1007, pp. 85-87. Ex. 1003, ¶235.

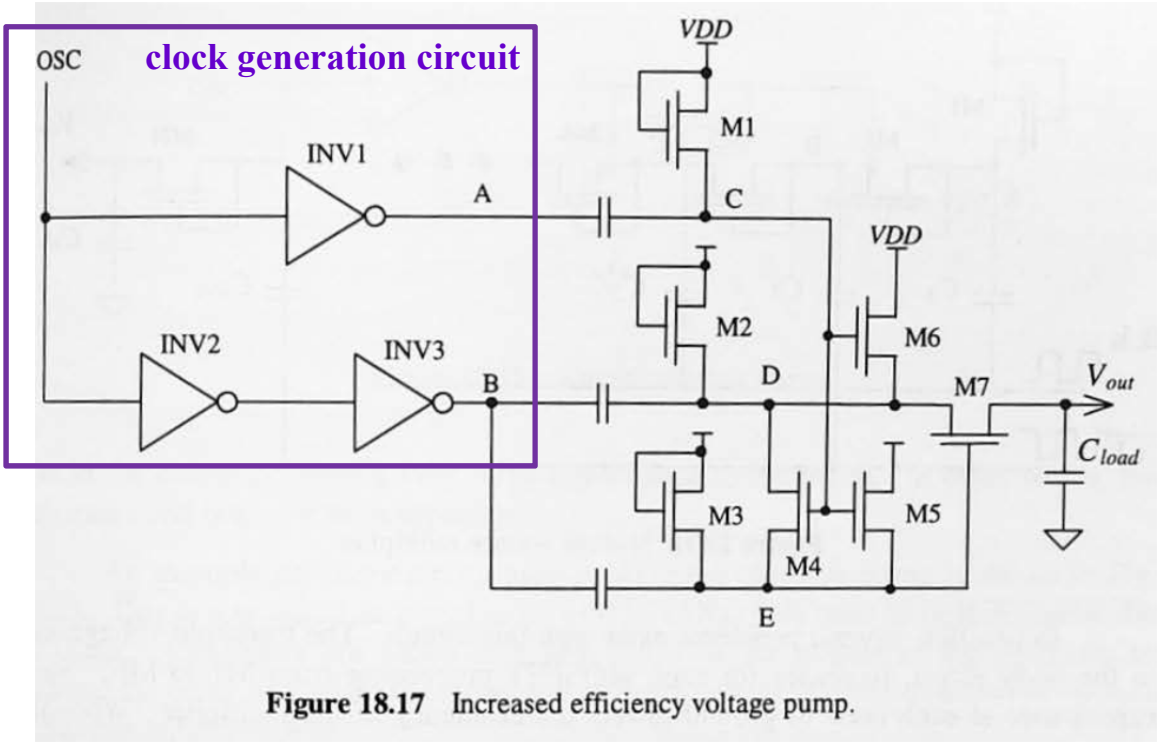


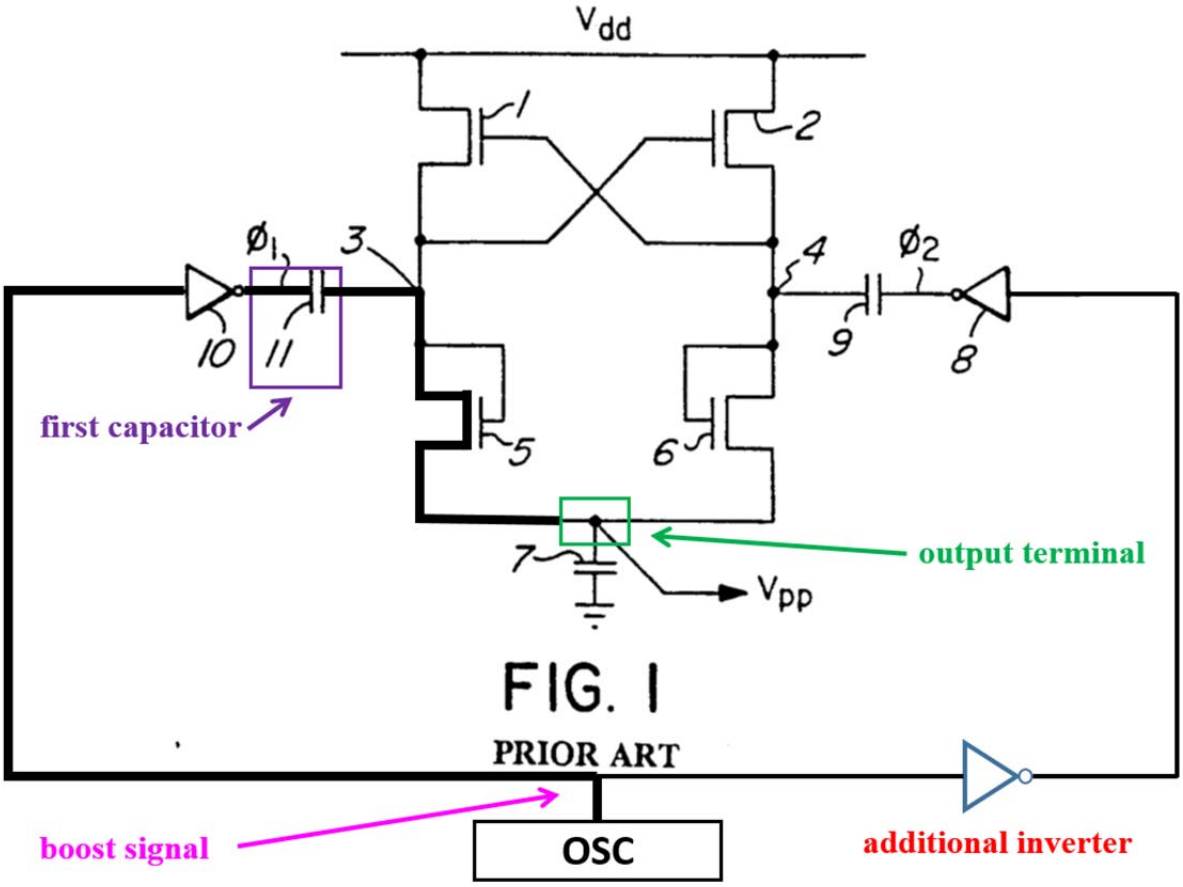
Figure 18.17 Increased efficiency voltage pump.

Ex. 1007, Figure 18.17 (with annotations)

This clock generation circuit includes oscillator OSC and three inverters INV1-INV3. Ex. 1007, pp. 85-87. An oscillator signal generated by oscillator OSC is inverted by inverter INV1 to generate a first clock signal at terminal A. The same oscillator signal is also inverted by inverter INV2, and then inverted again by inverter INV3 to generate a second clock signal at terminal B. Thus, the two clock signals are opposite to each other. Ex. 1003, ¶¶235-236.

As elaborated below in Section 11.4, it would have been obvious to a POSA to combine the teachings of Foss and Baker. An exemplary implementation of

Foss' voltage boosting circuit in light of the teachings of Baker's clock generation circuit to generate the two opposite clock signals ϕ1 and ϕ2 is illustrated below:



Ex. 1006, FIG. 1 (with annotations)

Like the arrangement in Figure 18.17 of Baker, here an oscillator signal generated by oscillator OSC is inverted by inverter 10 to generate clock signal ϕ1, and the same oscillator signal is also inverted by an additional inverter, and then inverted again by inverter 8 to generate clock signal ϕ2. As in Figure 18.17 of Baker, the resulting clock signals ϕ1 and ϕ2 are opposite to each other, just as depicted in FIG. 2 of Foss. Ex. 1003, ¶237. Particularly, a POSA would have

understood and found it obvious that using an additional inverter was a conventional technique to ensure that the two generated clock signals (ϕ1 and ϕ2) are opposite to each other. *Id.*, ¶238-239.

Third, in the circuit that adapts Foss' voltage boosting circuit in view of the teachings of Baker's clock generation circuit, the oscillator signal generated by oscillator OSC is a boost signal. Foss describes that the oscillator signal (and the clock signals generated from that oscillator signal) drives the operation of the prior art voltage boosting circuit. Ex. 1006, 1:25-26, 6:27-30, 8:63-65. The oscillator signal is an input to the circuit and is used to generate a boosted voltage by charging the capacitors (*e.g.*, capacitor 11). Thus, the oscillator signal is a boost signal. Ex. 1003, ¶240.

Furthermore, the 875 Patent describes a boost signal for a boost circuit as a signal that is used to boost the voltage of a capacitor (*e.g.*, capacitors 48A, 48B) via a buffer (*e.g.*, inverting buffer 50, non-inverting buffer 56) to generate a boosted voltage for the boost circuit. Ex. 1003, ¶241. Like the boost signal in the 875 Patent, here the oscillator signal boosts the voltage of a capacitor (*e.g.*, capacitor 11) via a buffer (*e.g.*, inverting buffer 10) to generate a boosted voltage for the circuit. *Id.*, ¶¶241-242.

Fourth, in the circuit that adapts Foss' voltage boosting circuit in view of the teachings of Baker's clock generation circuit, the left-side terminal of capacitor 11

("the second terminal of the first capacitor") is coupled for receiving the oscillator signal ("boost signal"). As shown in the above figure, the left-side terminal of capacitor 11 is connected to inverter 10 to receive an inversion of the oscillator signal. Thus, the left-side terminal of capacitor 11 is coupled for receiving the oscillator signal. *See* Section 7.3.1.3 above. Ex. 1003, ¶¶251-253.

11.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal"

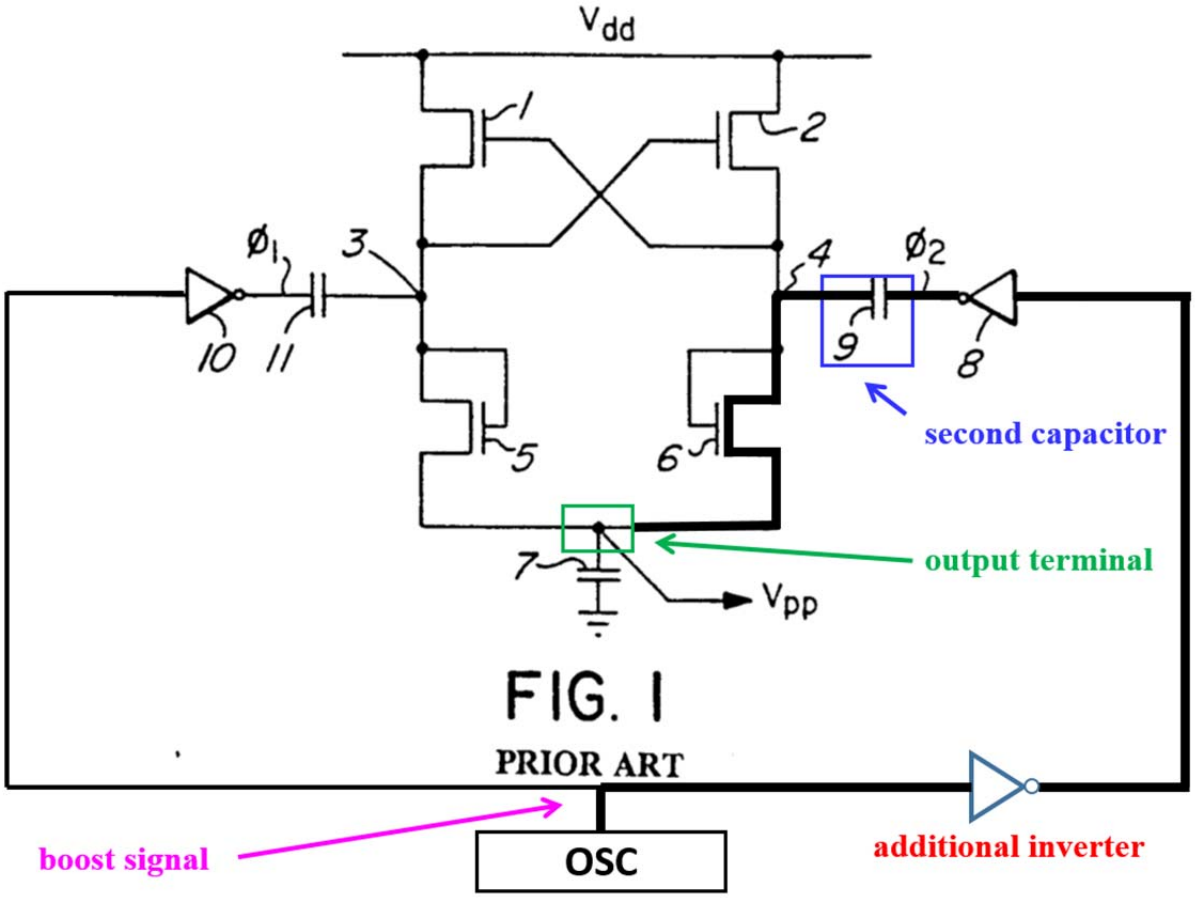
The prior art combination discloses this limitation.

As illustrated above in Section 10.1.5, Foss discloses that capacitor 9 ("second capacitor") has a left-side terminal ("first terminal") coupled to output terminal V_{pp} ("output terminal"). *See* above analysis for Claim [1.4], Section 10.1.5.

To the extent that Foss does not expressly disclose "coupled for receiving the boost signal" (*i.e.*, that the second clock source is the inverted version of the first clock source) because, for example, Foss does not illustrate in FIG. 1 the oscillator and inverter circuitry (*see* above analysis for Claim [1.3]-[1.4], Section 10.1.4-1.5), the combination of Foss in view of Baker discloses that limitation.

As discussed above for Claim [1.3] in Section 11.1.4, it would have been obvious to a POSA to combine Foss with the teachings of Baker's Figure 18.17. *See infra* Section 11.4. Ex. 1003, ¶¶262-271. An exemplary implementation of

Foss' prior art voltage boosting circuit in light of the teachings of the clock generation circuit in Figure 18.17 of Baker to generate the two opposite clock signals ϕ1 and ϕ2 is illustrated below:



Ex. 1006, FIG. 1 (with annotations)

As discussed above for Claim [1.3] in Section 11.1.4, the oscillator signal generated by oscillator OSC is a boost signal. Ex. 1003, ¶240.

Furthermore, the right-side terminal ("second terminal") of capacitor 9 ("second capacitor") is coupled for receiving the oscillator signal ("boost signal"). As shown in the above figure, the right-side terminal of capacitor 9 receives the

oscillator signal through inverter 8 and the additional inverter. Thus, the right-side terminal of capacitor 9 is coupled for receiving the oscillator signal. *See* Section 7.3.1.3 above. Ex. 1003, ¶75.

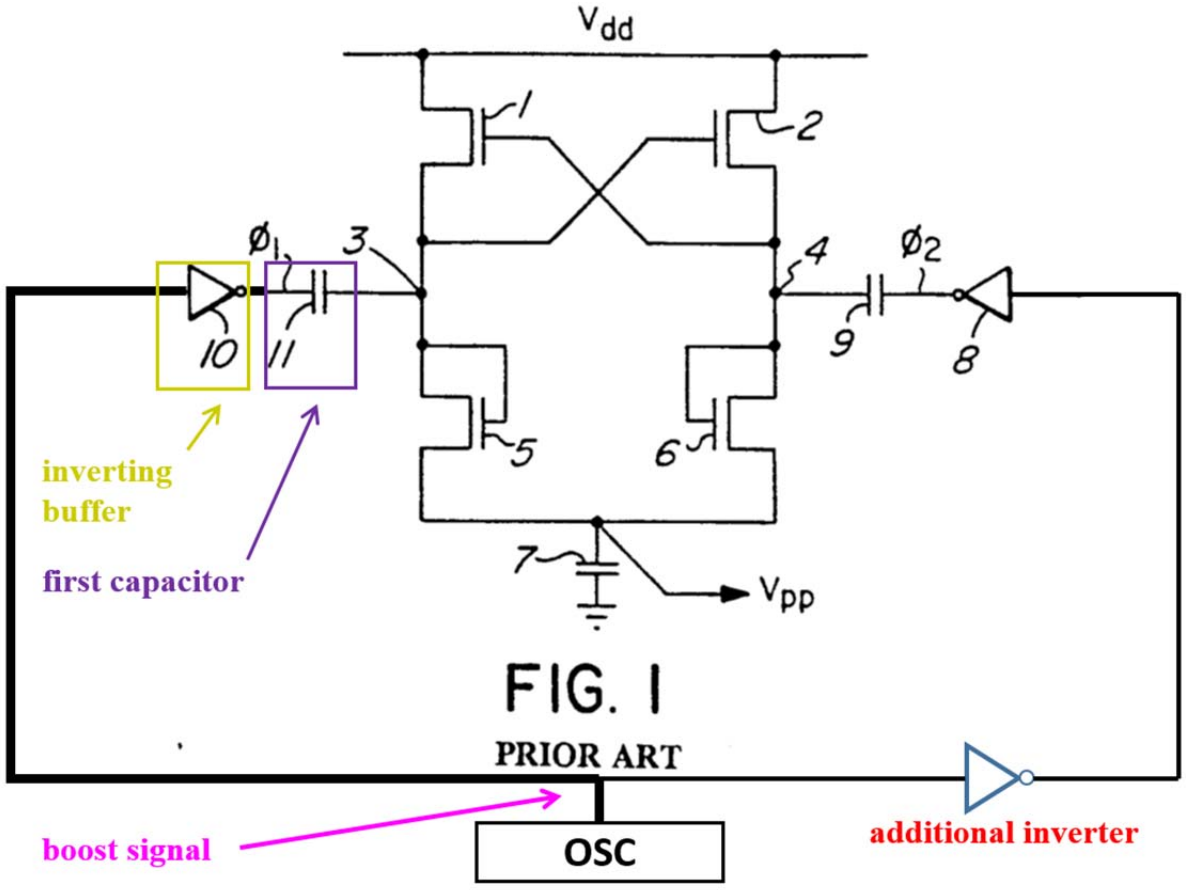
11.2. Claim 2 is obvious over Foss in view of Baker

11.2.1. [2.0] "The boost circuit of claim 1, further including:"

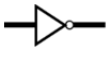
The prior art combination discloses this limitation. *See* above analysis for Claim 1, Section 11.1.

11.2.2. [2.1] "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and"

The prior art combination discloses this limitation. Specifically, in the circuit that adapts Foss' prior art voltage boosting circuit in view of the teachings of Baker's clock generation circuit (shown in the below figure), inverter 10 ("inverting buffer") has an input coupled for receiving the oscillator signal ("boost signal") generated by oscillator OSC, and has an output coupled to the left-side terminal of capacitor 11 ("the second terminal of the first capacitor").



Ex. 1006, FIG. 1 (with annotations)

First, inverter 10 is an inverting buffer. Inverter 10 isolates and decouples its output from its input (by using pull-up and pull-down transistors). Ex. 1003, ¶252. Moreover, a POSA would have understood that inverter 10 is an inverting buffer because it is an inverter, and it is represented by the schematic symbol of a NOT Gate (*i.e.*, ). *Id.*, ¶252. Furthermore, the 875 Patent uses the same symbol to represent inverting buffers (*e.g.*, inverting buffer 50 in FIG. 3, inverting

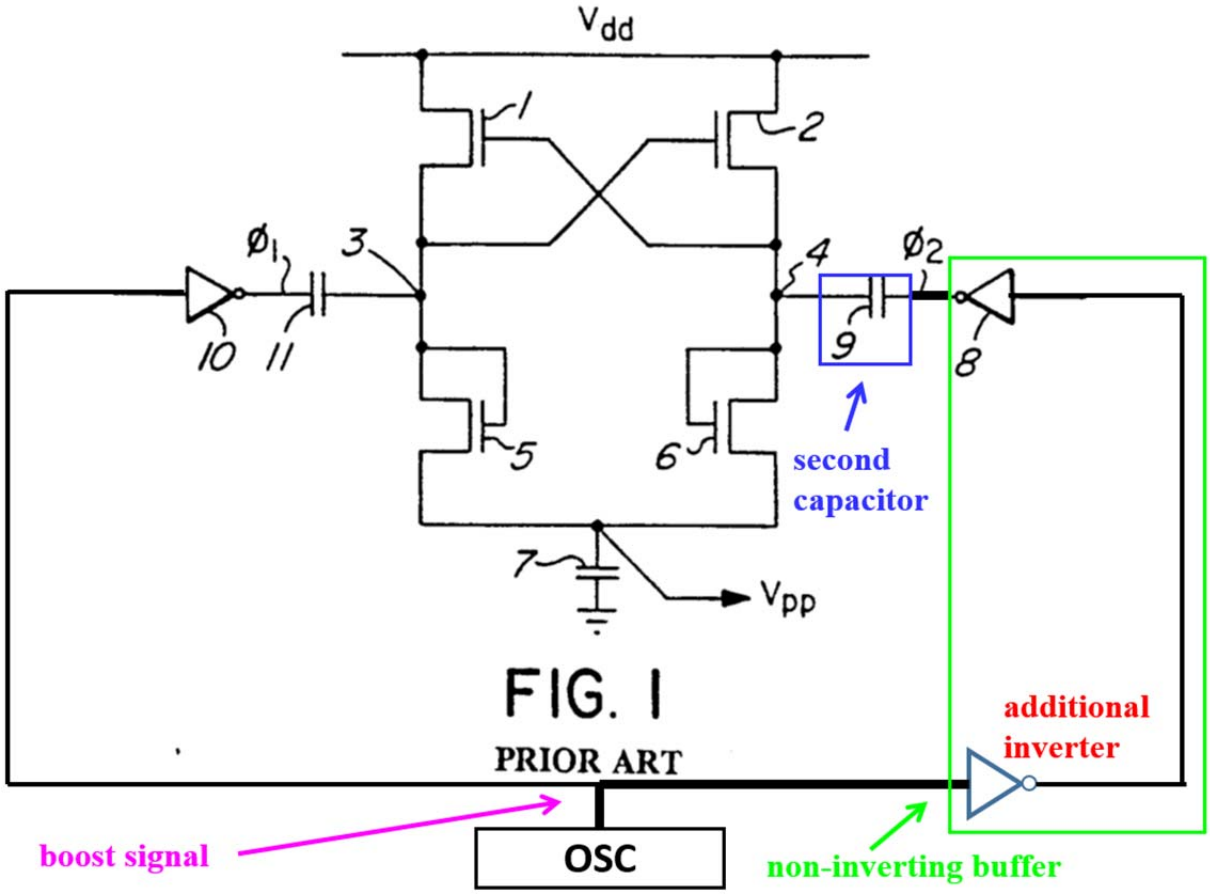
buffer 80 in FIG. 5). Ex. 1001, FIGS. 3, 5. Thus, inverter 10 is an inverting buffer. *See* Section 7.2.1.1 above. Ex. 1003, ¶252.

Second, as discussed above for Claim [1.3] in Section 11.1.4, the oscillator signal generated by oscillator OSC is a boost signal. Ex. 1003, ¶253.

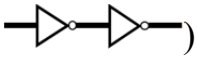
Third, as shown in the above figure, inverter 10 ("inverting buffer") has an input coupled for receiving the oscillator signal ("boost signal") and an output coupled to the left-side terminal of capacitor 11 ("the second terminal of the first capacitor"). Ex. 1003, ¶254.

11.2.3. [2.2] "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor."

The prior art combination discloses this limitation. Specifically, in the circuit that combines Foss' voltage boosting circuit and the teachings of Baker's clock generation circuit (shown in the below figure), a circuit consisting of the additional inverter and inverter 8 ("non-inverting buffer") has an input coupled for receiving the oscillator signal ("boost signal") and an output coupled to the right-side terminal of capacitor 9 ("the second terminal of the second capacitor").



Ex. 1006, FIG. 1 (with annotations)

First, the circuit consisting of the additional inverter and inverter 8 (identified in the above figure) is a non-inverting buffer. A POSA would have understood that such a circuit (*i.e.*, two inverters sequentially connected into a cascade) isolates and decouples its output from its input (by using pull-up and pull-down transistors), and its output is not inverted from its input. Ex. 1003, inverter 10 ¶255-256. Thus, this circuit is a non-inverting buffer. *Id.*, ¶256. Furthermore, as discussed above in Section 4.2, a non-inverting buffer is formed when two inverters are sequentially connected into a cascade (*i.e.*, ). Thus, this

circuit is a non-inverting buffer because it is formed by sequentially connecting two inverters (*i.e.*, the additional inverter and inverter 8) into a cascade. *See* Section 7.2.1.2 above. Ex. 1003, ¶256.

Second, as discussed above for Claim [1.3] in Section 11.1.4, the oscillator signal generated by oscillator OSC is the boost signal. Ex. 1003, ¶257.

Third, as shown in above figure, the circuit formed by the additional inverter and inverter 8 ("non-inverting buffer") has an input coupled for receiving the oscillator signal ("boost signal") and an output coupled to the right-side terminal of capacitor 9 ("the second terminal of the second capacitor"). Ex. 1003, ¶258.

11.3. Claim 3 is obvious over Foss in view of Baker

11.3.1. [3.0] "The boost circuit of claim 1, further including:"

The prior art combination discloses this limitation. *See* above analysis for Claim 1, Section 11.1.

11.3.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and"

Foss discloses this limitation. *See* above analysis for Claim [3.1], Section 10.2.2.

11.3.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."

Foss discloses this limitation. *See* above analysis for Claim [3.2], Section 10.2.3.

11.4. Motivations to combine Foss and Baker

A POSA would have been motivated to combine Foss' voltage boosting circuit with the teaching of the clock generation circuit from Baker for at least the following reasons. Ex. 1003, ¶262.

First, both references are squarely in the same field of technology (*i.e.*, voltage boost circuits). Specifically, Foss is directed to the field of voltage boost circuits (Ex. 1006, Abstract, 1:5-21). Similarly, Subchapter 18.3 of Baker teaches how to design voltage generators including voltage boost circuits (Ex. 1007, pp. 84-92). Thus, a POSA would have been motivated to consider the voltage boost circuits in both references. Ex. 1003, ¶263. Indeed, in reviewing Foss' teachings, and its reference to an oscillator without showing the internal schematics for the oscillator, a POSA would have been motivated to research clock generation circuits that provide opposite clock signals using an oscillator. Specifically, a POSA would have considered secondary resources, such as the Baker book, for further teachings in regards to such clock generation circuits that generate opposite clock signals for voltage pump circuits. *Id.*, ¶264.

Second, a POSA would have found the solution taught by Baker to be an ideal one for Foss' voltage boosting circuit. In particular, because Baker discloses a circuit that generates the first clock signal using a single inverter (*i.e.*, INV1) and generates the second clock signal using only two inverters (*i.e.*, INV2 and INV3),

the two clock signals would be opposite in phase. Ex. 1003, ¶265. This is precisely what Foss' voltage boosting circuit calls for, *e.g.*, *see* FIG. 2 of Foss. *See* Section 9.1. Thus, Baker's circuity accomplishes Foss' goal with respect to the clock circuity. Ex. 1003, ¶265.

Third, adapting Foss' prior art voltage boosting circuit with the teachings from Figure 18.17 of Baker would provide a predictable solution with a high expectation of success. This combination would simply apply a known technique (*i.e.*, using an oscillator and inverters to generate two opposite clock signals) to yield predictable results (*i.e.*, providing desired clock signals to drive Foss' voltage boosting circuit). Specifically, Foss' voltage boosting circuit calls for two opposite clock signals (*i.e.*, ϕ1 and ϕ2), which is exactly what the clock generation circuit in Figure 18.17 of Baker provides. In other words, Foss describes a requirement (*i.e.*, two opposite clock signals for a two-phase circuit operation) and discloses an oscillator to fulfill that requirement. Baker complements Foss by detailing how an oscillator generates two opposite clock signals. And adapting Foss to include an inverter in view of Baker was routine and effectively an undergraduate-level exercise. Ex. 1003, ¶266.

Fourth, the combination would have been obvious to try. Specifically, the teachings from Figure 18.17 of Baker provide an obvious and simple solution to generate the opposite clock signals in Foss' voltage boosting circuit. Notably, Foss

describes using an oscillator to generate the two opposite clock signals (Ex. 1006, 6:27-30, 8:63-65), and Figure 18.17 of Baker teaches exactly how to use an oscillator to generate two opposite clock signals (Ex. 1007, pp. 85-87). That is, Foss suggests what is disclosed in Figure 18.17 of Baker, and it certainly would have been obvious to try to adapt Foss in view of Baker. Ex. 1003, ¶268.

Finally, Foss describes that the two clock signals are used to drive the operation of the voltage boosting circuit (*i.e.*, serving as a boost signal) through an inverter (*i.e.*, inverter 10 and inverter 8 in FIG. 1) and then a capacitor (*i.e.*, capacitor 11 and capacitor 9 in FIG. 1). Figure 18.17 of Baker shows exactly the same thing, *i.e.*, the two clock signals are used to drive the operation of the voltage boost circuit through an inverter and then a capacitor. The configuration of Foss is suitable for Baker's teachings, and thus the combination would have been an obvious and easy choice. Ex. 1003, ¶269-271.

12. GROUND #3: CLAIMS 1-3 OF THE 875 PATENT ARE UNPATENTABLE AS BEING OBVIOUS OVER FOSS IN VIEW OF RABII[18]

12.1. Claim 1 is obvious over Foss in view of Rabii

12.1.1. [1.0] "A boost circuit having an input terminal and an output terminal, comprising:"

To the extent that the preamble is limiting, Foss discloses this limitation. *See* above analysis for Claim [1.0], Section 10.1.1.

12.1.2. [1.1] "a first switch coupled between the input terminal and the output terminal and operated by a first phase signal;"

Foss discloses this limitation. *See* above analysis for Claim [1.1], Section 10.1.2.

12.1.3. [1.2] "a second switch coupled between the input terminal and the output terminal and operated by a second phase signal that is opposite to the first phase signal;"

Foss discloses this limitation. *See* above analysis for Claim [1.2], Section 10.1.3.

12.1.4. [1.3] "a first capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving a boost signal; and"

The prior art combination discloses this limitation.

---

[18] *See* Section 10 above (describing assumption that "boost" and "phase" signals need not be independent).

As illustrated above in Section 10.1.4, Foss discloses that capacitor 11 ("first capacitor") has a right-side terminal ("first terminal") coupled to output terminal V_{pp} ("output terminal"). *See* above analysis for Claim [1.3], Section 10.1.4.

To the extent that it is determined that Foss does not expressly disclose "coupled for receiving the boost signal" (*see infra*, next limitation) (*i.e.*, that the second clock source is the inverted version of the first clock source) because, for example, Foss does not illustrate in FIG. 1 the oscillator and inverter circuitry (*see* above analysis for Claim [1.3]-[1.4], Section 10.1.4-1.5), the combination of Foss and Rabii discloses this limitation.

Adapting Foss in view of Rabii also effects the current limitation as set forth below. Foss in view of Rabii discloses this limitation as follows. First, as discussed above in Section 10.1.4-1.5, Foss discloses that capacitor 11 receives clock signal ϕ1 ("second phase signal"), and that capacitor 9 receives opposite clock signal ϕ2 ("first phase signal").

Second, combining the teachings of Foss and Rabii provides a structure for generating two opposite clock signals for Foss' voltage boosting circuit. Specifically, Foss describes that both clock signals ϕ1 and ϕ2 are generated from a common source (*e.g.*, an oscillator). Ex. 1006, 6:27-30, 8:63-65. Ex. 1003, ¶280 . Moreover, as shown in FIG. 2, the two clock signals ϕ1 and ϕ2 are opposite to each other. *See* above analysis for Claim [1.2], Section 10.1.3.

Like Foss, Rabii discloses a clock generation circuit that generates two opposite clock signals from a common input clock signal (*i.e.*, CK), but as shown in Fig. 12 (reproduced below with annotations), Rabii details this circuitry. Ex. 1008, p. 791. Ex. 1003, ¶281.

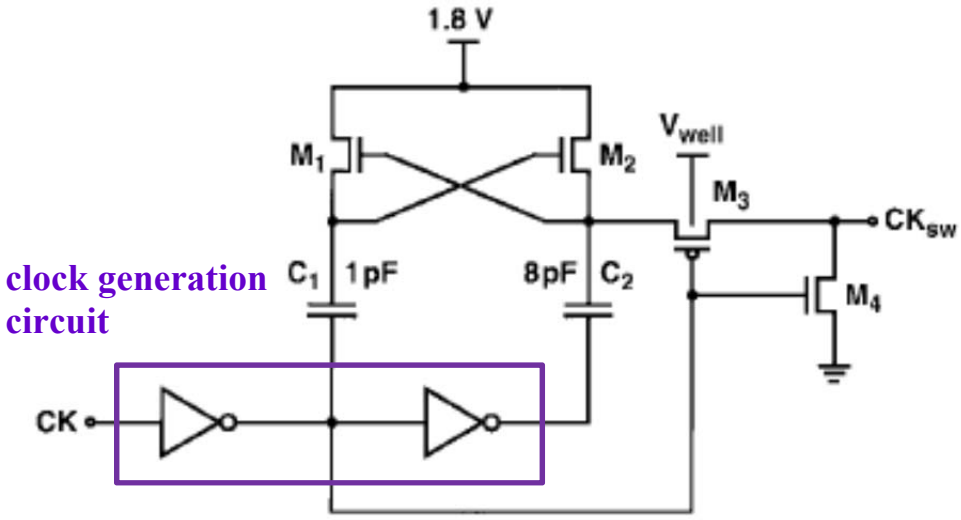
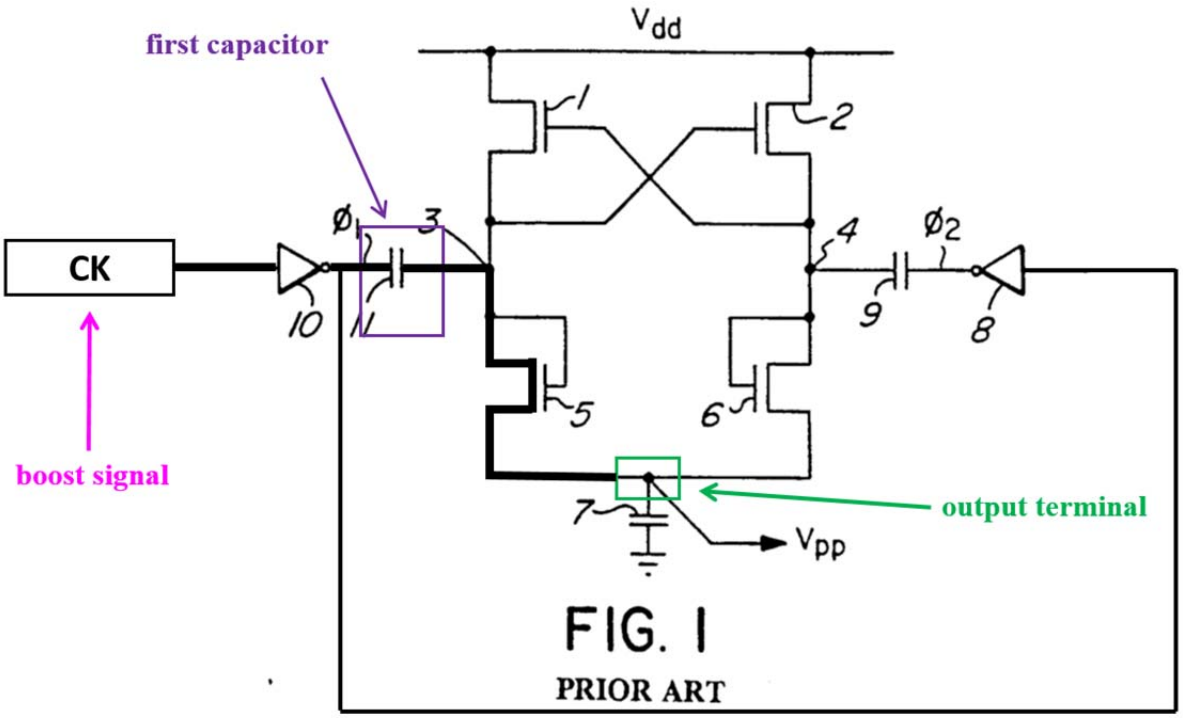


Fig. 12. Boosted clock driver.

Ex. 1008, Fig. 12 (with annotations)

The clock generation circuit includes a cascade of two inverters. An input clock signal CK is inverted by the left inverter to generate a first clock signal, which is received by capacitor C_1. The first clock signal is also inverted by the right inverter to generate a second clock signal, which is received by capacitor C_2. Thus, the two clock signals are opposite to each other. Ex. 1008, p. 791. Ex. 1003, ¶283. Additionally, a POSA would have understood that the input clock signal CK can be generated by, for example, an oscillator. *Id.*, ¶284.

As elaborated below in Section 12.4, it would have been obvious to a POSA to combine Foss with the teachings of Rabii's Fig. 12. As a result of the combination, an exemplary implementation of using the teachings of the clock generation circuit taught in Fig. 12 of Rabii to generate the two opposite clock signals ϕ1 and ϕ2 for Foss' prior art voltage boosting circuit is illustrated in the below figure:



Ex. 1006, FIG. 1 (with annotations)

As shown in the figure above, like the arrangement in Fig. 12 of Rabii, here an input clock signal CK is inverted by inverter 10 to generate clock signal ϕ1, which is then inverted again by inverter 8 to generate clock signal ϕ2. As in Fig.

12 of Rabii, the resulting clock signals ϕ1 and ϕ2 are opposite to each other. Ex. 1003, ¶¶284-285.

Third, in the circuit that combines Foss' voltage boosting circuit with the teachings of Rabii's clock generation circuit, the input clock signal CK is a boost signal. Specifically, Foss describes that an oscillator signal, which is a clock source from which the clock signals ϕ1 and ϕ2 are generated, drives the operation of the voltage boosting circuit. Ex. 1006, 1:25-26, 6:27-30, 8:63-65. A POSA would have understood that Rabii's input clock signal CK, like the oscillator signal described in Foss, is input to the circuit and is used to generate a boosted voltage by charging the capacitors (*e.g.*, capacitors C_1 and C_2). Moreover, the input clock signal CK itself can be generated from an oscillator, thus making it an oscillator signal as described in Foss. Thus, the input clock signal CK is a boost signal. Ex. 1003, ¶286.

Furthermore, the 875 Patent describes a boost signal for a boost circuit as a signal that is used to boost the voltage of a capacitor (*e.g.*, capacitors 48A, 48B) via a buffer (*e.g.*, inverting buffer 50, non-inverting buffer 56) to generate a boosted voltage for the boost circuit. Ex. 1003, ¶287. Like the boost signal in the 875 Patent, here the input clock signal CK boosts the voltage of a capacitor (*e.g.*, capacitor 11) via a buffer (*e.g.*, inverting buffer 10) to generate a boosted voltage

for the circuit. Thus, the input clock signal CK is a boost signal according to the disclosure of the 875 Patent. *Id.*, ¶287.

Fourth, in the circuit that combines Foss' voltage boosting circuit with the teachings of Rabii's clock generation circuit, the left-side terminal of capacitor 11 ("the second terminal of the first capacitor") is coupled for receiving the input clock signal CK ("boost signal"). Specifically, as shown in the above figure, the left-side terminal of capacitor 11 is connected to inverter 10 to receive an inversion of the input clock signal CK. Thus, the left-side terminal of capacitor 11 is coupled for receiving the input clock signal CK. *See* Section 7.3.1.3 above. Ex. 1003, ¶288.

12.1.5. [1.4] "a second capacitor having a first terminal coupled to the output terminal and a second terminal coupled for receiving the boost signal"

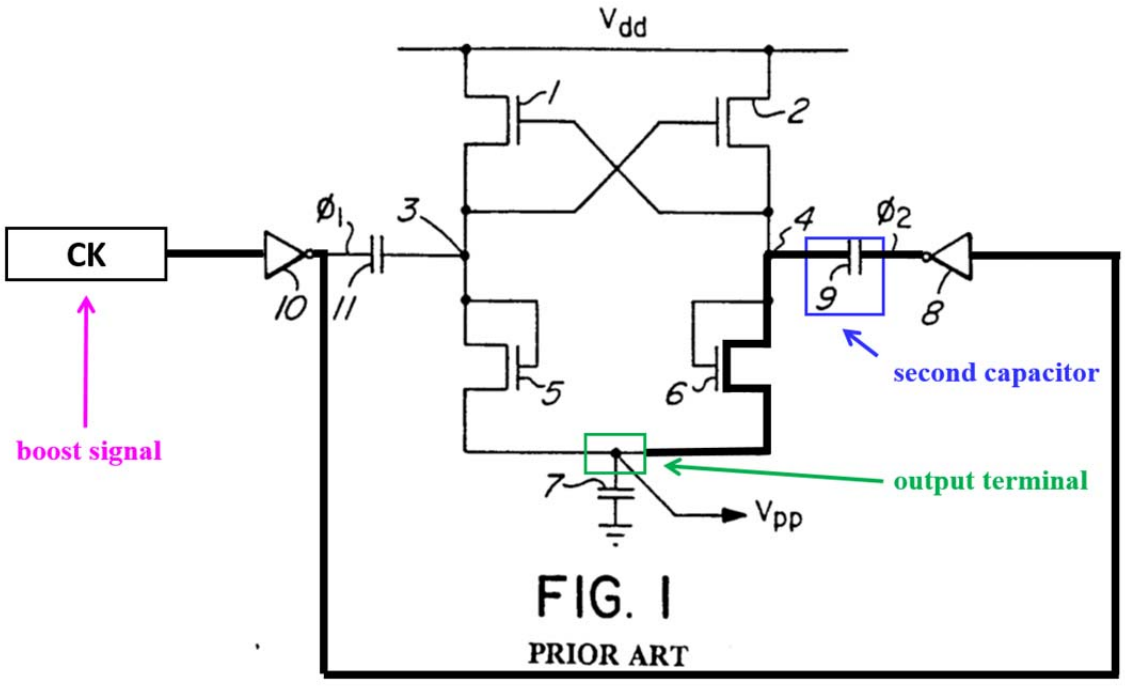
The prior art combination discloses this limitation.

As illustrated above in Section 10.1.5, Foss discloses that capacitor 9 ("second capacitor") has a left-side terminal ("first terminal") coupled to the output terminal V_{pp} ("output terminal"). *See* above analysis for Claim [1.4], Section 10.1.5.

To the extent that it is determined that Foss does not expressly disclose "coupled for receiving the boost signal" (*i.e.*, that the second clock signal is the inverted version of the first clock signal) because, for example, Foss does not

illustrate in FIG. 1 the oscillator and inverter circuitry (*see* above analysis for Claim [1.3]-[1.4], Section 10.1.4-1.5), the combination of Foss in view of Rabii discloses this limitation.

As discussed above for Claim [1.3] in Section 12.1.4, it would have been obvious to a POSA to combine Foss with the teachings of Rabii's Fig. 12. An exemplary implementation of using the teachings of the clock generation circuit taught in Rabii's Fig. 12 to generate the two opposite clock signals ϕ1 and ϕ2 for Foss' voltage boosting circuit is illustrated in the below figure:



Ex. 1006, FIG. 1 (with annotations)

As discussed above for Claim [1.3] in Section 12.1.4, the input clock signal CK is a boost signal. Ex. 1003, ¶¶293-294.

Furthermore, the right-side terminal ("second terminal") of capacitor 9 ("second capacitor") is coupled for receiving the input clock signal CK ("boost signal"). Specifically, as shown in above figure, the right-side terminal of capacitor 9 receives the input clock signal CK through inverters 8 and 10. Thus, the right-side terminal of capacitor 9 is coupled for receiving the input clock signal CK. *See* Section 7.3.1.3 above. Ex. 1003, ¶294.

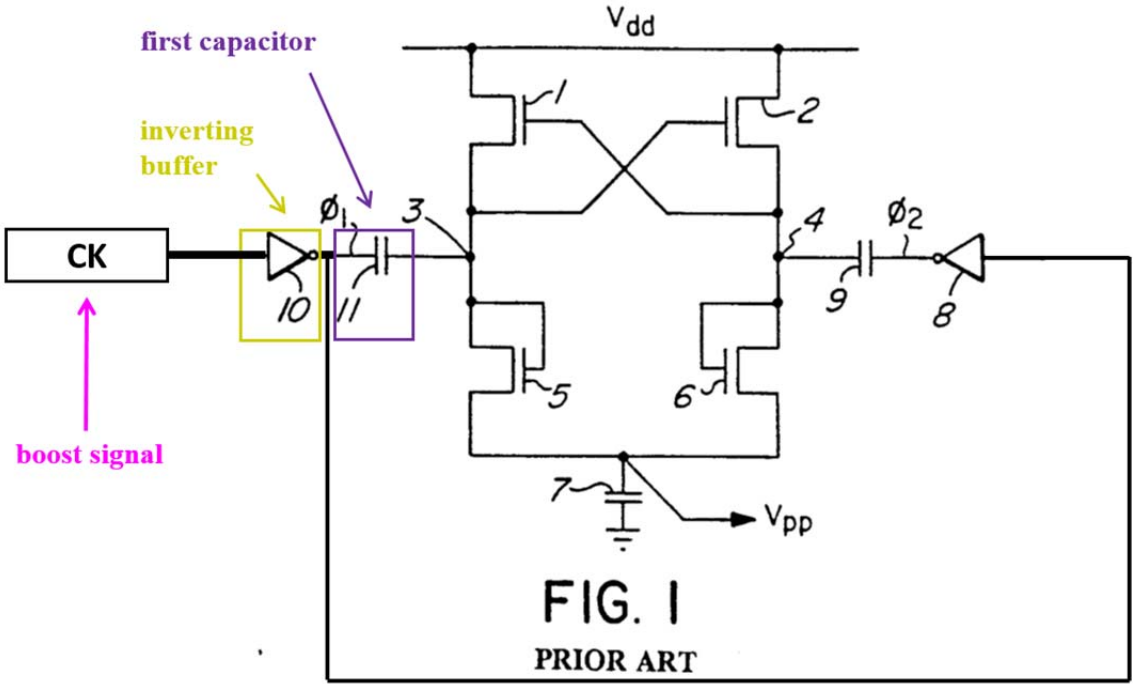
12.2. Claim 2 is obvious over Foss in view of Rabii

12.2.1. [2.0] "The boost circuit of claim 1, further including:"

The prior art combination discloses this limitation. *See* above analysis for Claim 1, Section 12.1.

12.2.2. [2.1] "an inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the first capacitor; and"

The prior art combination discloses this limitation. In the circuit that combines Foss' voltage boosting circuit and the teachings of Rabii's clock generation circuit (shown in the below figure), inverter 10 ("inverting buffer") has an input coupled for receiving the input clock signal CK ("boost signal") and an output coupled to the left-side terminal of capacitor 11 ("the second terminal of the first capacitor").



Ex. 1006, FIG. 1 (with annotations)

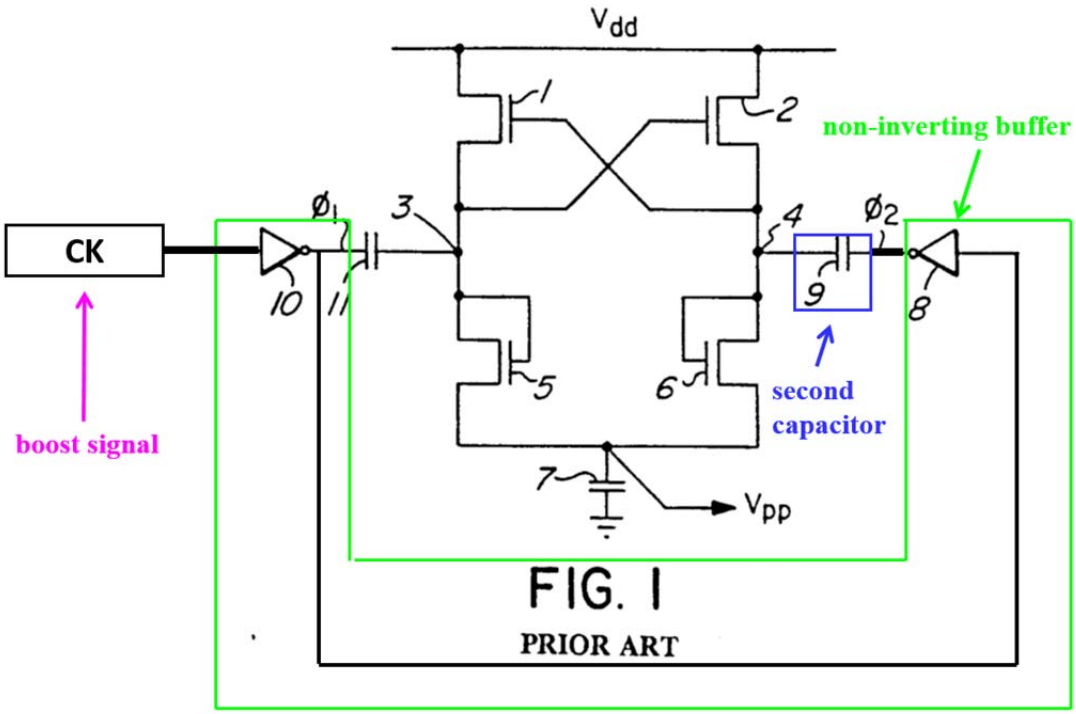
First, as discussed above with respect to the combination of Foss and Baker, inverter 10 is an inverting buffer. *See* above analysis for Claim [2.1] in Section 11.2.2. Ex. 1003, ¶¶296-297.

Second, as discussed above for Claim [1.3] in Section 12.1.4, the input clock signal CK is a boost signal. Ex. 1003, ¶298.

Third, as shown in the above figure, inverter 10 ("inverting buffer") has an input coupled for receiving the input clock signal CK ("boost signal") and an output coupled to the left-side terminal of capacitor 11 ("the second terminal of the first capacitor"). Ex. 1003, ¶298.

12.2.3. [2.2] "a non-inverting buffer having an input coupled for receiving the boost signal and an output coupled to the second terminal of the second capacitor."

The prior art combination discloses this limitation. In the circuit that combines Foss' voltage boosting circuit with the teachings of Rabii's clock generation circuit (shown in the below figure), a circuit consisting of inverters 10 and 8 ("non-inverting buffer") has an input coupled for receiving the input clock signal CK ("boost signal") and an output coupled to the right-side terminal of capacitor 9 ("the second terminal of the second capacitor").



Ex. 1006, FIG. 1 (with annotations)

First, just like the circuit consisting of the additional inverter and inverter 8 discussed above with respect to the combination of Foss and Baker, here the circuit

formed by inverter 10 and inverter 8 is a non-inverting buffer. *See* above analysis for Claim [2.2] in Section 11.2.3. Ex. 1003, ¶¶300-301.

Second, as discussed above for Claim [1.3] in Section 12.1.4, the input clock signal CK is the boost signal. Ex. 1003, ¶302.

Third, as shown in the above figure, the circuit formed by inverter 10 and inverter 8 ("non-inverting buffer") has an input coupled for receiving the input clock signal CK ("boost signal") and an output coupled to the right-side terminal of capacitor 9 ("the second terminal of the second capacitor"). Ex. 1003, ¶303.

12.3. Claim 3 is obvious over Foss in view of Rabii

12.3.1. [3.0] "The boost circuit of claim 1, further including:"

The prior art combination discloses this limitation. *See* above analysis for Claim 1, Section 12.1.

12.3.2. [3.1] "a third switch coupled between the first terminal of the first capacitor and the output terminal, and operated by the second phase signal; and"

Foss discloses this limitation. *See* above analysis for Claim [3.1], Section 10.2.2.

12.3.3. [3.2] "a fourth switch coupled between the first terminal of the second capacitor and the output terminal, and operated by the first phase signal."

Foss discloses this limitation. *See* above analysis for Claim [3.2], Section 10.2.3.

12.4. Motivations to combine Foss and Rabii

A POSA would have been motivated to combine Foss' voltage boosting circuit with the teaching of the clock generation circuit from Rabii for at least the following reasons. Ex. 1003, ¶307.

First, both references are in the same field of technology (*i.e.*, voltage boost circuits). Specifically, Foss is directed to the field of designing voltage boost circuits. Ex. 1006, Abstract, 1:5-21. Similarly, Rabii is directed to the design of integrated circuits (*e.g.*, converters, modulators, boosted clock drivers, etc.). Ex. 1008, Abstract, Index Terms. Also, Rabii is published in IEEE Journal of Solid-State Circuits, and includes terms such as "boosted clock driver" and "voltage doubler." Ex. 1008, Index Terms. Ex. 1003, ¶308.

Moreover, both references relate to the same specific problem of designing a boost circuit and describe essentially the same boost circuit. Specifically, Foss describes a prior art voltage boosting circuit. Ex. 1006, Abstract, 1:24-2:5. Similarly, Section III.B of Rabii describes a prior art boost circuit (*i.e.*, the boosted clock driver in FIG. 12), which essentially has the same structure and operates in the same manner as Foss' voltage boosting circuit. *See* above Section 9.3. Thus, a POSA would have been motivated to consider the boost circuits in both references. Ex. 1003, ¶309-310. Indeed, in reviewing Foss' teachings, and its reference to a common source (*i.e.*, an oscillator) for generating two opposite clock signals

without showing the internal schematics for the common source, a POSA would have been motivated to research clock generation circuits that provide opposite clock signals using an oscillator. Specifically, a POSA would have considered secondary resources, such as the Rabii paper, for further teachings in regards to generating opposite clock signals from a common source for voltage pump circuits. *Id.*, ¶310.

Second, a POSA would have found the solution taught by Rabii to be an ideal one for Foss' voltage boosting circuit. In particular, because Rabii discloses a circuit that generates the second clock signal from the first clock signal using a single inverter (*i.e.*, the right inverter in Fig. 12), the two clock signals would be opposite in phase. Ex. 1003, ¶311. This is precisely what Foss' prior art voltage boosting circuit calls for, *e.g.*, *see* FIG. 2 of Foss. *See* Section 9.3. Ex. 1003, ¶311.

Third, adapting Foss' voltage boosting circuit in view of the teachings from Fig. 12 of Rabii would have provided a predictable solution with a high expectation of success. This combination would simply apply a known technique (*i.e.*, using a series of inverters to generate two opposite clock signals from an input clock signal) to yield predictable results (*i.e.*, providing desired clock signals to drive Foss' voltage boosting circuit). Foss' voltage boosting circuit calls for two opposite clock signals (*i.e.*, $\phi 1$ and $\phi 2$), which is exactly what the clock generation

circuit in Fig. 12 of Rabii provides. In other words, Foss describes a requirement (*i.e.*, two opposite clock signals for a two-phase circuit operation) and discloses using a common source (*i.e.*, an oscillator) to fulfill that requirement. Rabii complements Foss by detailing how to generate two opposite clock signals from a common source. It was routine to use such simple circuitry to produce opposite signals, and such logic is easily compatible with Foss' voltage boosting circuitry. Ex. 1003, ¶313-314.

Furthermore, the boosted clock driver circuit in Fig. 12 of Rabii has substantially the same structure as Foss' voltage boosting circuit. Ex. 1008, Fig. 12; Ex. 1006, FIG. 1. Ex. 1003, ¶314. Specifically, as shown in Fig. 12 of Rabii and FIG. 1 of Foss, like capacitor 11 in Foss that is coupled between inverter 10 and transistor 1, capacitor C_1 in Rabii is coupled between the left inverter and transistor M_1. *Id.*, ¶315. Similarly, like capacitor 9 in Foss that is coupled between inverter 8 and transistor 2, capacitor C_2 in Rabii is coupled between the right inverter and transistor M_2. *Id.*, ¶315. Like transistors 1 and 2 in Foss, transistors M_1 and M_2 in Rabii are cross-coupled with each other. Ex. 1008, p. 791, col. 1 ("Capacitors C1 and C2 are charged to V_{DD} via the **cross-coupled NMOS transistors M1 and M2**"). The only difference is that inverters 10 and 8 in Foss are not directly connected, while the two inverters in Rabii are connected to form a

cascade. *Id*. Thus, the combination would have had a high expectation of success. Ex. 1003, ¶315.

Fourth, the combination would have been obvious to try. The teachings from Fig. 12 of Rabii provide an obvious and simple solution to generate the opposite clock signals in Foss' voltage boosting circuit. Particularly, Foss describes that the two opposite clock signals are generated from a common source (*e.g.*, an oscillator) (Ex. 1006, 6:27-30, 8:63-65), and Fig. 12 of Rabii teaches exactly how to generate two opposite clock signals from a common source (*e.g.*, an input clock signal CK) (Ex. 1008, p. 791). Notably, as discussed above, the only structural difference between Rabii's boosted clock driver circuit and Foss' voltage boosting circuit is that the inverters 10 and 8 in Foss are not directly connected, while the two inverters in Rabii are connected to form a cascade. It would have been obvious to a POSA that, in order to generate two opposite clock signals from a common source (*e.g.*, an input clock signal) for Foss' voltage boosting circuit, one simply needs to connect inverters 10 and 8 to form a cascade in the same way as shown in Fig. 12 of Rabii. Thus, it certainly would have been obvious to try to adapt Foss in view of Rabii. Ex. 1003, ¶¶316-317.

Finally, Foss describes that the two clock signals are used to drive the operation of the voltage boosting circuit (*i.e.*, serving as a boost signal) through an inverter (*i.e.*, inverter 10 and inverter 8 in FIG. 1) and then a capacitor (*i.e.*,

capacitor 11 and capacitor 9 in FIG. 1). Fig. 12 of Rabii shows exactly the same thing, *i.e.*, the two clock signals are used to drive the operation of the voltage boost circuit through an inverter and then a capacitor. The configuration of Foss' voltage boosting circuit is suitable for Rabii's teachings, and thus the combination would have been an obvious and easy choice. Ex. 1003, ¶318.

13. CONCLUSION

For the reasons set forth above, *inter partes* review of claims 1-3 of the 875 Patent is requested.

Respectfully submitted,

Dated: May 1, 2018 By: _____

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3237

CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,402 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2010, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2010 in Times New Roman 14 point font.

Dated: May 1, 2018

By: 

Jeremy Jason Lang
Lead Counsel for Petitioner
Registration No. 73,604
Weil, Gotshal & Manges LLP
201 Redwood Shores Parkway
Redwood Shores, CA 94065
Telephone: 650-802-3237

CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.105 and § 42.6(e), that service was made on the Patent Owner as detailed below.

Date of service	May 1, 2018
Manner of service	EXPRESS MAIL
Documents served	Petition for *Inter Partes* Review of U.S. Pat. No. 6,127,875 with Micron's Exhibit List Power of Attorney Exhibits Ex. 1001 - Ex. 1014, Ex. 1006 - Ex. 1018
Persons served	Patent Owner's Address of Record: NXP USA, Inc. Law Department 6501 William Cannon Drive West TX30/OE62 Austin, TX 78735 Additional Addresses Known as Likely to Effect Service: North Star Innovations, Inc. 600 Anton Blvd., Suite 1350 Costa Mesa, CA 92626 Edward C. Flynn Cohen & Grace, LLC 105 Braunlich Drive, Suite 300 Pittsburgh, PA 15237 Robert W. Morris Eckert, Seamans, Cherin & Mellott, LLC 10 Bank St., Suite 700 White Plains, NY 10606

Dated: May 1, 2018

By: 

Jeremy Jason Lang
Lead Counsel for Petitioner

Registration No. 73,604