UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., SK HYNIX AMERICA INC., AND SK HYNIX INC.
Petitioner

v.

BiTMICRO, LLC
Patent Owner

U.S. Patent No. 8,093,103

Case IPR2018-01545

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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PETITIONER'S EXHIBIT LIST

Exhibit No.	Description
1001	U.S. Patent No. 8,093,103 ("Bruce" or "'103 Patent")
1002	Declaration of Dr. R. Jacob Baker
1003	File History of U.S. Patent No. 8,093,103
1004	International Patent Application No. WO 2004/072667 ("Sato"), including certified translation
1005	U.S. Patent No. 6,236,115 ("Gaynes")
1006	U.S. Patent No. 5,612,570 ("Eide")
1007	U.S. Patent Application Publication No. 2003/0178228 ("Sung")
1008	U.S. Patent Application Publication No. 2005/0082664 ("Funaba")
1009	"IEEE Standard Test Access Port and Boundary-Scan Architecture," Institute of Electrical and Electronics Engineers, Inc., 2001
1010	File History of U.S. Patent No. 7,826,243
1011	U.S. Patent Application Publication No. 2004/0257847 ("Matsui")
1012	U.S. Patent No. 5,995,379 ("Kyougoku")
1013	Moore, G., "Cramming more Components onto Integrated Circuits," *Electronics*, April 19, 1965, pp. 112-117
1014	Lundstrom, M., "Moore's Law Forever?", *Science*, January 10, 2003, Vol. 299, Issue 5604, pp. 210-211
1015	Terrill, R. and Beene, G. L., "3D Packaging Technology Overview and Mass Memory Applications," *1996 IEEE Aerospace Applications Conference*, 1996, pp. 347-355
1016	U.S. Patent No. 5,523,619 ("McAllister")
1017	Intel 2000 Packaging Databook
1018	1994 DRAM Data Book
1019	U.S. Patent No. 5,514,907 ("Moshayedi")
1020	Karnezos, M., "3-D Packaging: Where All Technologies Come Together," *2004 IEEE/SEMI Int'l Electronics Manufacturing Technology Symposium*, 2004, pp. 1-4
1021	U.S. Patent No. 5,501,893 ("Laermer '893")
1022	U.S. Patent No. 6,531,068 ("Laermer '068")
1023	Spiesshoefer, S. and Schaper, L., "IC Stacking Technology Using Fine Pitch, Nanoscale Through Silicon Vias," *2003*

	Electronic Components and Technology Conference, 2003, pp. 631-633
1024	IEEE Std. 1149.1 (JTAG) Testability Primer, 1997
1025	Schieble, J., "A Survey of Storage Options," *Computer*, December, 2002, pp. 42-46
1026	Gervasi, "DRAM Module Market Overview"
1027	U.S. Patent No. 6,154,419 ("Shakkarwar")
1028	U.S. Patent No. 6,545,895 ("Li")
1029	Microsoft Computer Dictionary, 5th Ed.
1030	IEEE 100 The Authoritative Dictionary of IEEE Standard Terms, 7th Ed.
1031	Trumble, B., "Get The Lead Out!", *IEEE Spectrum*, May, 1998, pp. 55-60
1032	U.S. Patent No. 7,262,080 ("Go")

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc. ("Samsung entities"), SK hynix Inc. and SK hynix America Inc. ("SK hynix entities") (collectively, "Petitioner") request *inter partes* review of claims 12 and 16 ("Challenged Claims") of U.S. Patent No. 8,093,103 (the "'103 patent") (Ex. 1001).

I. INTRODUCTION

The '103 patent purports to disclose novel stacked module techniques. As explained in this Petition, however, the claimed techniques were well-known and obvious in view of the prior art.

II. MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1): Real Party-in-Interest

The Petitioner entities are the real parties-in-interest.

B. 37 C.F.R. § 42.8(b)(2): Related Matters

Patent Owner has asserted the '103 patent in Investigation No. 337-TA-1097 (USITC 2017). Petitioner seeks declaratory judgment of non-infringement in the Northern District of California, 5:18-CV-03502 and 5:18-CV-03505.

C. 37 C.F.R. § 42.8(b)(3): Counsel Information

Lead Counsel	Backup Counsel
Joseph Colaianni (No. 39,948)	F. Christopher Mizzo, P.C. (No. 73,156) Gregory S. Arovas, P.C. (No. 38,818) Craig Murray (No. 72,978) Linhong Zhang (No. 64,749) David Holt (No. 65,161)

Individual attorney contact information is in the signature block below.

D. 37 C.F.R. § 42.8(b)(4): Service Information

Petitioner concurrently submits Powers of Attorney, 37 C.F.R. § 42.10(b), and consent to electronic service directed to the following email address:

- Samsung_1097@kirkland.com
- IPR19968-0020IP3@fr.com (referencing No. 19968-0020IP3 and cc'ing PTABInbound@fr.com)

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103

The undersigned authorizes the Office to charge any fees with this Petition to Deposit Account No. 06-1050. Review of two claims is requested.

IV. CERTIFICATION OF STANDING UNDER 37 C.F.R. § 42.104(A)

Petitioner certifies that the '103 patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. 37 C.F.R. § 42.104(b)(1): Claims for Which IPR Is Requested

Petitioner challenges claims 12 and 16.

B. 37 C.F.R. § 42.104(b)(2): Grounds for Challenge

The claims are challenged based on the following references:

1. PCT Publication No. WO 2004/072667 ("Sato") (Ex. 1004), published on August 26, 2004; prior art under § 102(b). Included in Exhibit 1004 is a certified translation of Sato; all citations to Exhibit 1004 are to this certified translation.

2. U.S. Patent No. 6,236,115 ("Gaynes") (Ex. 1005), granted May 22, 2001; prior art under § 102(b).

3. U.S. Patent No. 5,612,570 ("Eide") (Ex. 1006), granted March 18, 1997; prior art under § 102(b).

4. U.S. Patent Publication No. 2003/0178228 ("Sung") (Ex. 1007), published September 25, 2003; prior art under § 102(b).

5. U.S. Patent Publication No. 2005/0082664 ("Funaba") (Ex. 1008), filed on Oct. 15, 2004, and published on April 21, 2005; prior art under § 102(a) and (e).

Petitioner requests cancellation on the following grounds under § 103:

Ground	Claims	Proposed Statutory Rejection
1	12 and 16	Obvious over Sato
2	12 and 16	Obvious over Sato in view of Gaynes
3	12 and 16	Obvious over Sato in view of Eide
4	12 and 16	Obvious over Sung in view of Funaba

C. 37 C.F.R. § 42.104(b)(3): Claim Construction

No terms need to be construed.

D. 37 C.F.R. § 42.104(b)(4): How the Claims Are Unpatentable

See Section IX below.

E. 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge

A list of exhibits is provided. The relevance of this evidence and the specific portions supporting the challenge are provided below in Section IX. Pursuant to 37 C.F.R. § 1.68, Petitioner submits the declaration of Dr. R. Jacob Baker (Ex. 1002).

VI. OVERVIEW OF THE '103 PATENT AND RELATED TECHNOLOGY

The '103 patent relates to "a method of using multiple chip module (MCM) and Package Stacking technique to support miniaturization and memory scalability." (Ex. 1001, 1:17-21.) The '103 patent states that semiconductor disk drives "typically use separate packages for the interface controller, the DMA controller, the processor and separate packages for the Flash devices, the FPROMs and the RAMs." (*Id.,* 1:23-26.) This method "limits the miniaturization of the entire storage device." (*Id* at 1:26-27.) The '103 patent purportedly addresses this issue by presenting a method where the semiconductor dies (e.g., flash devices) are mounted in a module and then

"stacked to create the desired memory capacity and different packages are stacked to create desired function." (*Id* at 1:54-61.) Module stacking, however, was not a novel idea at the time of the alleged invention. (Ex. 1002, ¶¶ 38-43, 48-86.)

The '103 patent describes multiple embodiments of this module stacking. Claims 12 and 16 cover the sole serial chain routing embodiment, which is shown in Figures 21a and 21b.[1] The serial chains allegedly enable the serial routing of a signal through all modules in the stack. (*Id* at 10:21-22.) In this embodiment, a first serial chain route 2146 is connected to a second serial chain route 2111 by a **routing path 2112**, as illustrated in Fig. 21a.[2]

[1] Most of the description provided for Figures 21a and 21b of the '103 patent was added by amendment to the patent application long after it was filed. (Ex. 1010, 256-310.) Petitioner does not concede that the filed application provides an adequate written description.

[2] All color annotations and emphasis added unless otherwise noted.

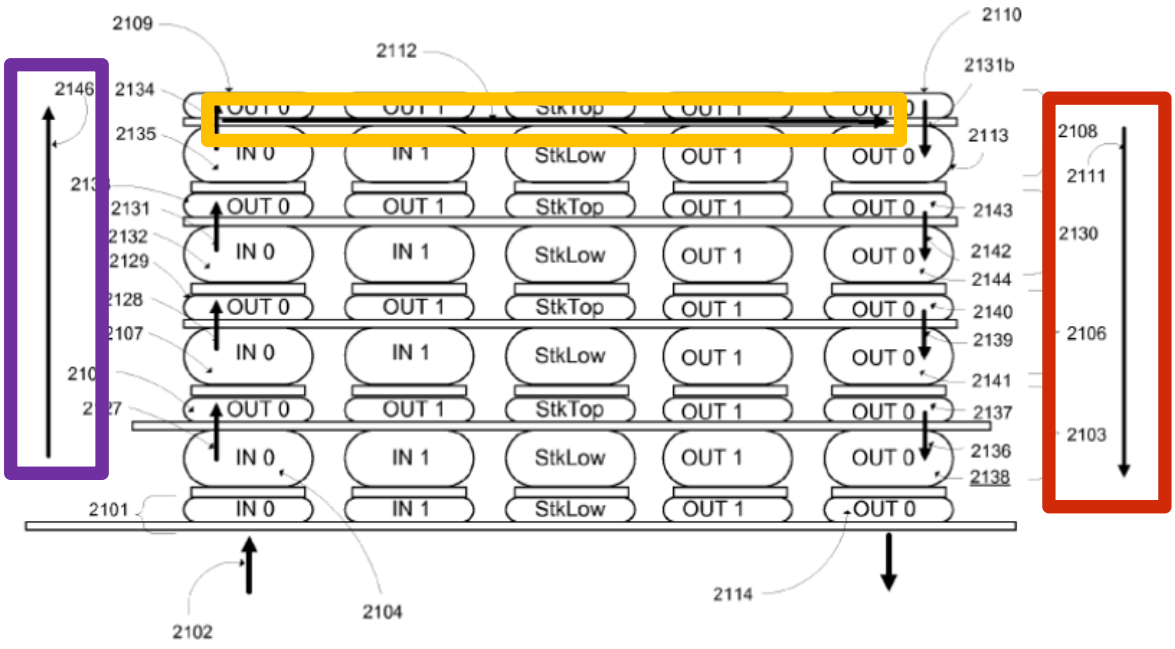


Figure 21a

(Ex. 1001, Fig. 21a.) The routing path described by the '103 patent that connects two serial chains is, for example, a JTAG TDI-TDO signal path. (*Id.,* 11:34-37.) JTAG (or Joint Test Action Group) is an industry standard for performing a boundary scan, which is a method of testing the interconnection (or wire lines) on PCBs, including those in semiconductor disk drives and memory modules. The JTAG standard teaches a configuration that has "[a] serial path formed by a daisy-chain connection of the serial test data pins (TDI and TDO)" of multiple devices. (Ex. 1009, 14 and Fig. 4-1.)

The '103 patent implements this well-known JTAG serial chain configuration with stacked modules. (Ex. 1001, 11:34-37.) Fig. 21b illustrates the connection:

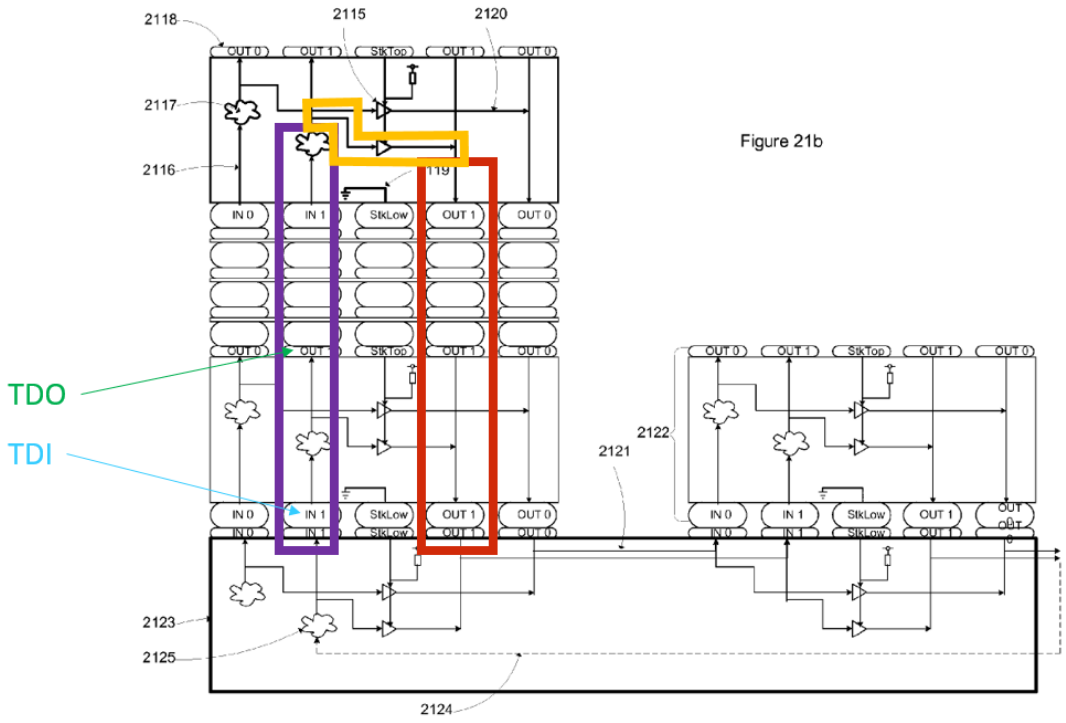


Figure 21b

(Ex. 1001, Fig. 21b.) In other words, the alleged invention in figures 21(a) and (b), covered by claims 12 and 16, is an implementation of JTAG in the context of a stacked memory module. But implementing JTAG in stacked memory was well-known in the part at the time of the alleged invention, as described below in Grounds 1-3.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention would have had at least a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in the fields of memory stacking and integrated circuits. More education can supplement practical experience and vice versa. (Ex. 1002, ¶¶ 33-37.)

VIII. OVERVIEW OF THE PRIMARY REFERENCES

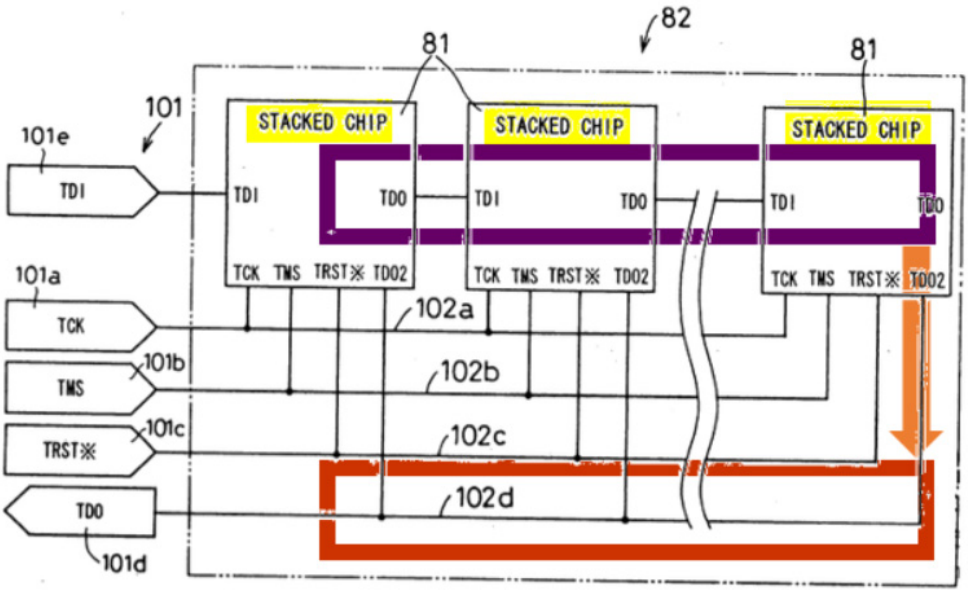
A. Overview of Sato

Sato discloses a stack of memory modules that are capable of performing a vertical JTAG boundary scan over all modules in the stack. (Ex. 1002, ¶ 66-68.) Sato's memory modules each contain a JTAG boundary scan controller. The boundary scan controller is "for testing connection states of input/output terminals of a plurality of semiconductor circuit chips which constitute a semiconductor device." (Ex. 1004, 1:9-11.) Sato provides a boundary scan controller on each stacked module so that the various modules can be identical, lowering manufacturing cost. (*Id.,* 6:22-24.)

Sato discloses that the boundary scan controller of the preferred embodiment uses the JTAG standard. (*Id.,* 13:16-25; Ex. 1002, ¶¶ 67-68.) The JTAG boundary scan test is performed in a "daisy chain" where the output of a "controller of a lower stage" is connected to the input of a "controller of an upper stage." (*Id.,* 8:6-8.) Specifically, a TDI (Test Data Input) signal enters each stacked memory module through a penetrating electrode. (*Id.,* 23:26-27.) A penetrating electrode is a conductive circuit that passes vertically through the memory module. The TDI signal is outputted from that module as a Test Data Output (TDO) signal. (*Id.,* 15:3-7.) This TDO signal then enters the next memory module, through its penetrating

electrode, as TDI. This "daisy chain" into and out of the stacked memory module is shown in two-dimensions in Figure 3:

FIG. 3



(Ex. 1004, Fig. 3.)

However, the uppermost stacked module cannot output the TDI on the TDO signal path because there is no module stacked above it. Instead, the uppermost module uses a routing path to output the TDI signal on the TDO2 contact pad. (*Id.,* 17:18-21.) The TDO2 signal path is then passed down the stack through each module and is connected to the JTAG tester at the bottom module. (*Id.,* Figs. 3 and 5.)

B. Overview of Sung

Sung discloses a three-dimensional stacked integrated circuit system in which every layer of the stack is identical. (Ex. 1007, Abstract; Ex. 1002, ¶¶ 74-82.)

Sung's stacking methods can "increase processing power, chip integration, operating speed and data storage density in the same planar area while minimizing global interconnect lengths." (*Id.,* [0006].)

The layers of Sung's "three-dimensional stack" communicate using connectors having "vertical conductors" and "terminators" connected by "conditional connection[s]" designed to be "aligned with the necessary offset, d, and then fused together." (*Id.,* [0025], [0044].)

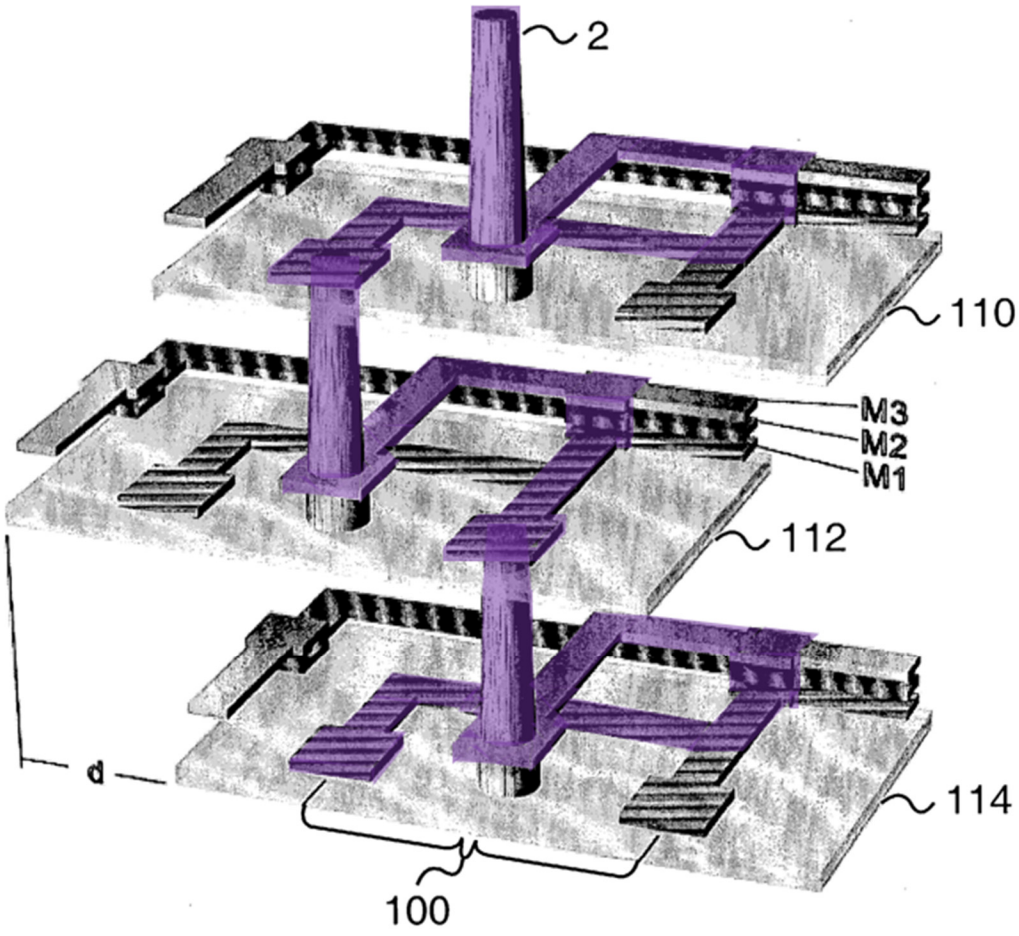


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

Sung also discloses circuits for "defin[ing] a communications boundary in a vertical stack." (*Id.,* [0020]; Ex. 1002, ¶¶74-82.) Each layer of the stack includes tristate buffers that are controlled by "top and bottom die identifier circuits" designed to determine whether the layer is the top or bottom layer in the stack, and to enable or disable the tristate buffers to route data so that it does not flow past the stack. (*Id.,* [0032], [0049].)

IX. SPECIFIC GROUNDS FOR PETITION

Pursuant to 37 C.F.R. § 42.104(b)(4)-(5), the sections below, as confirmed in the Baker Declaration (Ex. 1002), show how the prior art renders obvious the Challenged Claims.

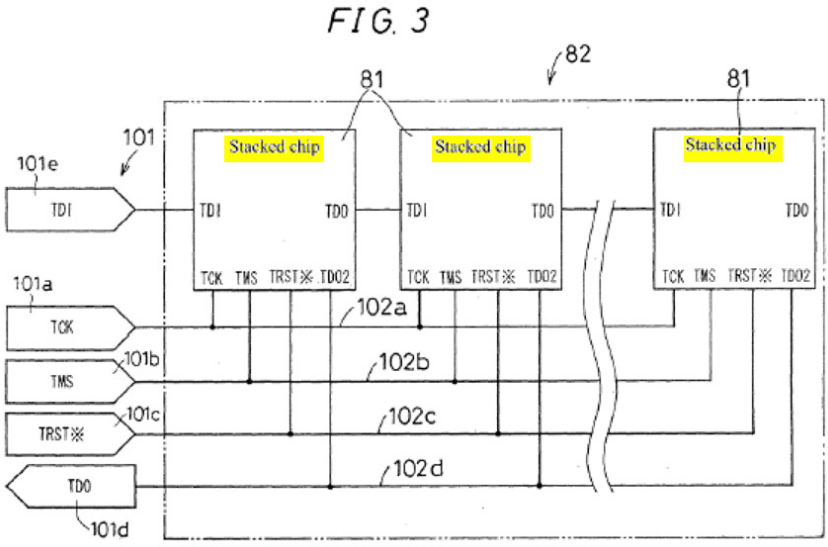
A. Ground 1: Claims 12 and 16 Are Obvious Over Sato

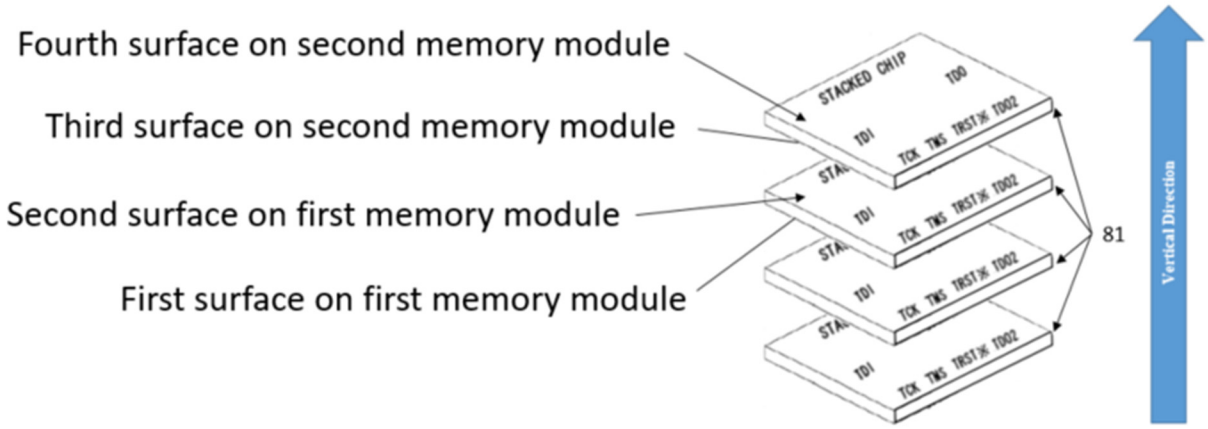
1. *Independent Claim 12*

a. "12. A method for stacking a plurality of modules, said plurality of modules including a first memory module and a second memory module; said first memory module having a first surface and a second surface; said second memory module having a third surface and a fourth surface; said method comprising;"

To the extent the preamble is considered limiting, Sato discloses the preamble. (Ex. 1002, ¶¶ 91-101.) For example, Sato discloses a method for stacking a plurality of modules wherein the stacked modules are memory modules. (Ex. 1004, Abstract ("semiconductor circuit chips are stacked"), 6:22-24, 8:2-12, 8:26-27, 10:29-11:10 ("the semiconductor circuit chip is a memory chip"), 28:26-29:2; Ex. 1002, ¶¶ 92-

95.) Below is Sato's Figure 3, which is a two dimensional block diagram of the stacked modules, along with an illustration created by Petitioner depicting them in three dimensions, as described in the text:





(Ex. 1004, Fig. 3; Ex. 1002, ¶¶ 94-95)

Sato further explains that the each stacked memory module has an upper surface with connection terminals. (*See* Ex. 1004, 22:15-20.) A POSITA would have understood that each of Sato's modules has a bottom surface. (*Id.*, 23:12-15;

Ex. 1002, ¶ 96.) Thus, Sato's module that is second from the top is a "first memory module having a first surface and a second surface." And the top module is a "second memory module having a third surface and a fourth surface." (Ex. 1002, ¶ 96.)

If extent Patent Owner argues that each of the memory modules must be an SDRAM module, Sato discloses such an SDRAM memory module. A POSITA would have understood the term "memory chip" used by Sato would include SDRAM and would have immediately envisioned SDRAM. (Ex. 1002, ¶¶ 99-100.) There were (and still are) a finite number of different memories, and SDRAM was the most common type of memory used before the filing of the '103 patent. (*Id.*)

Further, it would have been obvious to a POSITA to use SDRAM. (*Id.,* ¶¶ 99-101.) Nothing in Sato restricts the memory chip to a particular type of memory. (Ex. 1004, 10:29-11:10.) SDRAM was well-known in the art at the time, nearly all electronic devices used SDRAM, and SDRAM was widely used in computers as main memory. In addition, SDRAM designers have long sought methods of increasing the amount of SDRAM on a given package and Sato provides a method for stacking memory modules to increase the amount of memory in a package. (Ex. 1002, ¶¶ 99-101)

b. "forming one or more active ports on the first and second memory modules, said one or more active ports for carrying one or more active signals;"

Sato discloses forming one or more active ports on each stacked memory module, such as **connection terminals TDO 86A**, **TDI 83A**, **TDO2 89A**, **and TCK 83A**. (Ex. 1004, 18:10-19:30; Ex. 1002, ¶¶ 102-109.)

Figures 2 and 5 show these terminals. Figure 2 depicts a top-down view of a single semiconductor module with an integrated boundary scan controller. (Ex. 1004, 13:17-19, Figs. 2, 5.) Figure 5 depicts a perspective view ("A" being in the vertical direction) of some of the electrical connections within and through that same single module. (*Id.,* 23:5-7.)

FIG. 2

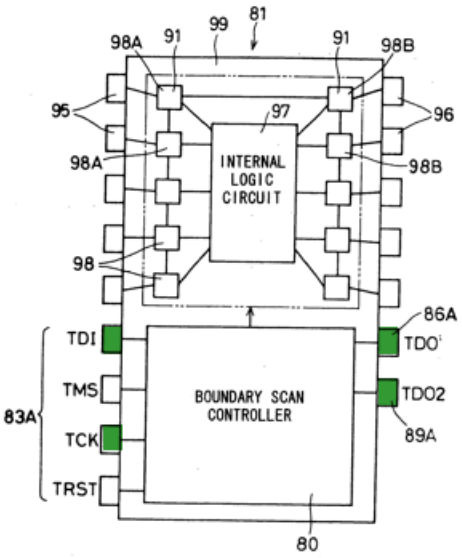
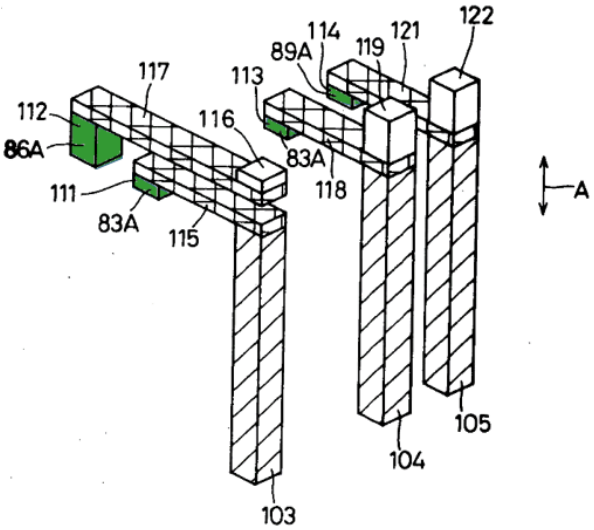


FIG. 5



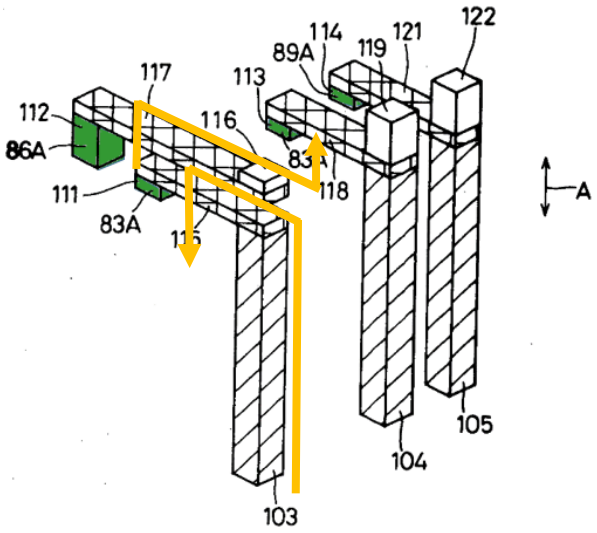
(Ex. 1002, ¶ 103.)

The connection terminals are active ports as they are electrical connections

that carry active signals (TDO, TDO2, TDI, and TCK). (Ex. 1004, 19:7-11, 20:24-30, 23:5-25); Ex. 1002, ¶ 104.) These active ports are repeated on each module.

A terminal, as indicated by its name, is the end of a conductor. A POSITA would have understood that each of Sato's "terminals" is a contact pad made from a conductive material. (Ex. 1002, ¶ 106.) The terminals are present on each of the stacked memory modules (Ex. 1004, 24:29-25:5) and carry a signal into or out of the module. For instance, the TDI signal is passed through penetrating electrode 103, along connection line 115, and onto **connection terminals 83A**. (Ex. 1004, 23:17-24:2.) The TDO signal is outputted through **connection terminal 86A** so that it can be sent to the next module in the stack. (*Id.,* 20:24-27.)

FIG. 5



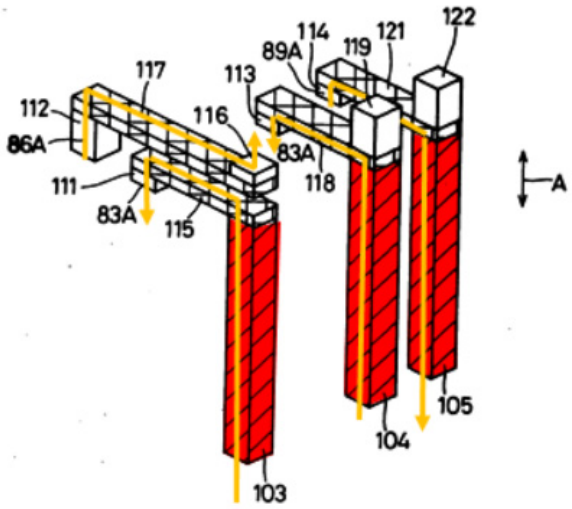
(*Id.*, Fig. 5.) Lastly, TDO, TDO2, TDI, and TCK are active signals because they are transmitted digital signals that carry information. (Ex. 1002, ¶ 105.)

c. "forming one or more passive ports on the first and second memory modules, said one or more passive ports for passing through said one or more active signals on the first and second memory modules;"

Sato discloses forming at least three passive ports on each module—**penetrating electrodes 103-105**—that pass the active signals (e.g., TDI/TDO, TDO2, and TCK) from one surface of a memory module to the other. (Ex. 1004, 23:5-24:24 (stating the "penetrating electrodes 103-105 penetrate through the semiconductor circuit chip assembly 81"); Ex. 1002, ¶¶ 110-19.)

Sato's Figure 5, below, illustrates signal paths over the penetrating electrodes when the memory modules are stacked.

FIG. 5



(Ex. 1002, ¶ 114.) Signals pass through the penetrating electrodes, connect to the chip's input terminals (e.g., 83A), and can be outputted through output terminals (e.g., 86A, 89A). (Ex. 1004, 24:17-19 (A signal from below the module "is ***passed***

through the first penetrating electrode 103 and transmitted to the terminal 111."); Ex. 1002, ¶ 112.) Additionally, penetrating electrodes 103-105 are interconnected with memory modules stacked below, which are not shown in Figure 5. (*Id.,* 23:26-24:16.)

Further, the structure of Sato's **penetrating electrodes** is similar to the passive port structure described by the '103 patent. (Ex. 1002, ¶ 115.) The passive ports in the '103 patent is a connection between the one surface of a memory module and the opposite surface of the same module.[3] (Ex. 1001, 9:19-24.) Thus, the penetrating electrodes are passive ports because they are vertical electronic connections that pass an active signal through the memory module from one surface to another. (Ex. 1004, 2:9-22, 23:5-16; Ex. 1002, ¶ 115.)

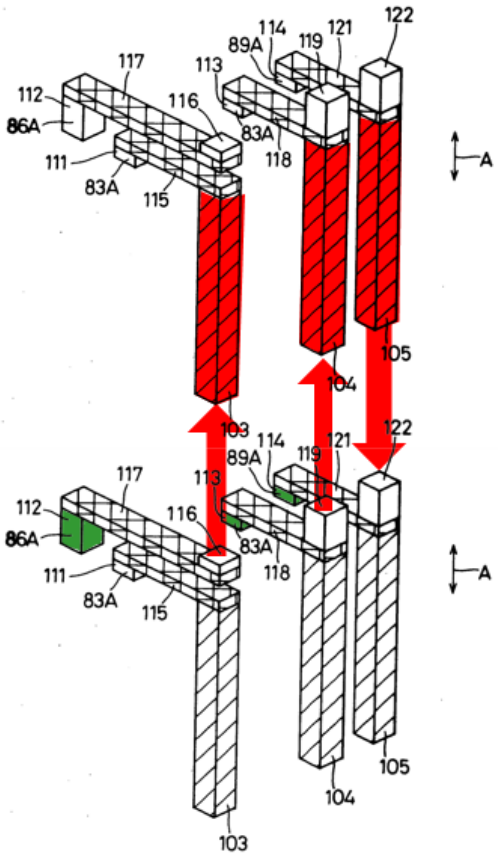
[3] If Patent Owner argues that the claimed "passive port" requires the particular ball and pad structures described in the '103 specification, a POSITA would have understood that Sato's connection terminals are pads that would necessarily be connected to the penetrating electrode of an adjacent module by conductive material (i.e., a solder ball). (Ex. 1002, ¶¶ 116-19.) It would have also been obvious to a POSITA to connect the connection terminals and penetrating electrode with a ball. (*Id.*, ¶ 117.) Thus, the **penetrating electrodes 103-105** connect a ball on one surface of the module to a pad on the other. (Ex. 1002, ¶ 118.)

d. "coupling one of said active ports formed on said first memory module to one of said passive ports formed on said second memory module by stacking said first memory module to said second memory module;"

Sato discloses this limitation by explaining that active ports (**connection terminals TDO 86A**, **TDI 83A**, **TDO2 89A**, **and TCK 83A)** of each stacked module are respectively coupled to passive ports **(penetrating electrodes 103-105)** of a memory module stacked above it. (Ex. 1004, 23:26-24:16; Ex. 1002, ¶¶ 120-22.)

For example, **penetrating electrode 103** is electrically connected to **connection terminal TDO 86A** on the memory module below it through connection terminal 116 and second connection line 117. (Ex. 1004, 23:28-24:22). Similarly, **Penetrating electrode 104 and 105** are electrically connected to **connection terminals TCK 83A and TDO2 89A**, respectively. (*Id.,* 24:3-16).

FIG. 5



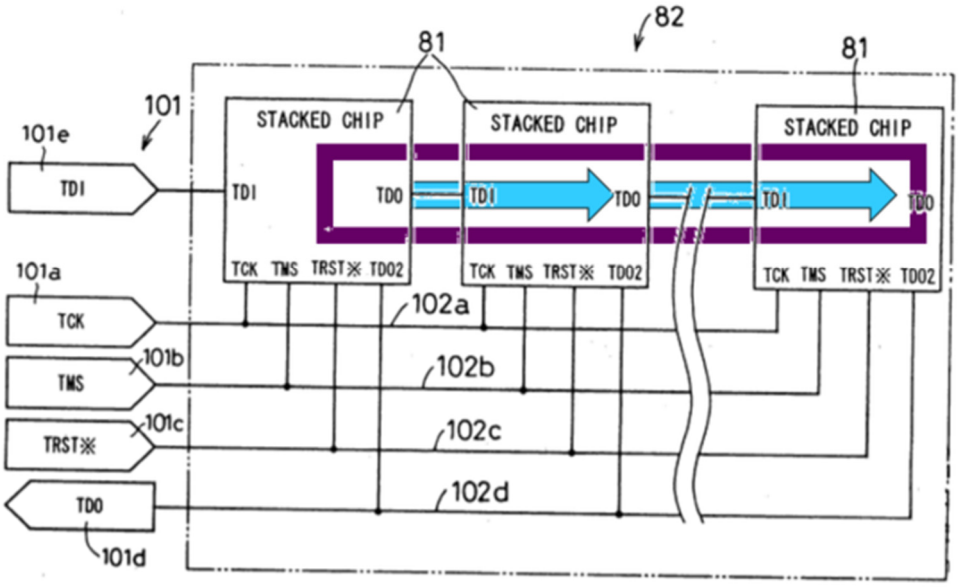
(Ex. 1002, ¶¶ 121-22 (modifying Fig. 5 to show interconnections after stacking).)

e. "forming a first serial chain route that includes at least one serial chain connection, said serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output;"

Sato discloses forming serial connections among memory modules to form a "**daisy chain**," which allows all the memory modules to be "simultaneously subjected" to a JTAG boundary scan test. (Ex. 1004, 20:31-21:4, Fig. 3; Ex. 1002, ¶ 123.) Specifically, the **daisy chain** is "the signal lines TDI and TDO of the boundary scan controller … [that] are connected in the shape of a chain." (Ex. 1004,

4:9-14.) Sato then discloses a stacked JTAG **daisy chain**, as illustrated in Fig. 3 (below).

FIG. 3



(Ex. 1002, ¶ 124.)

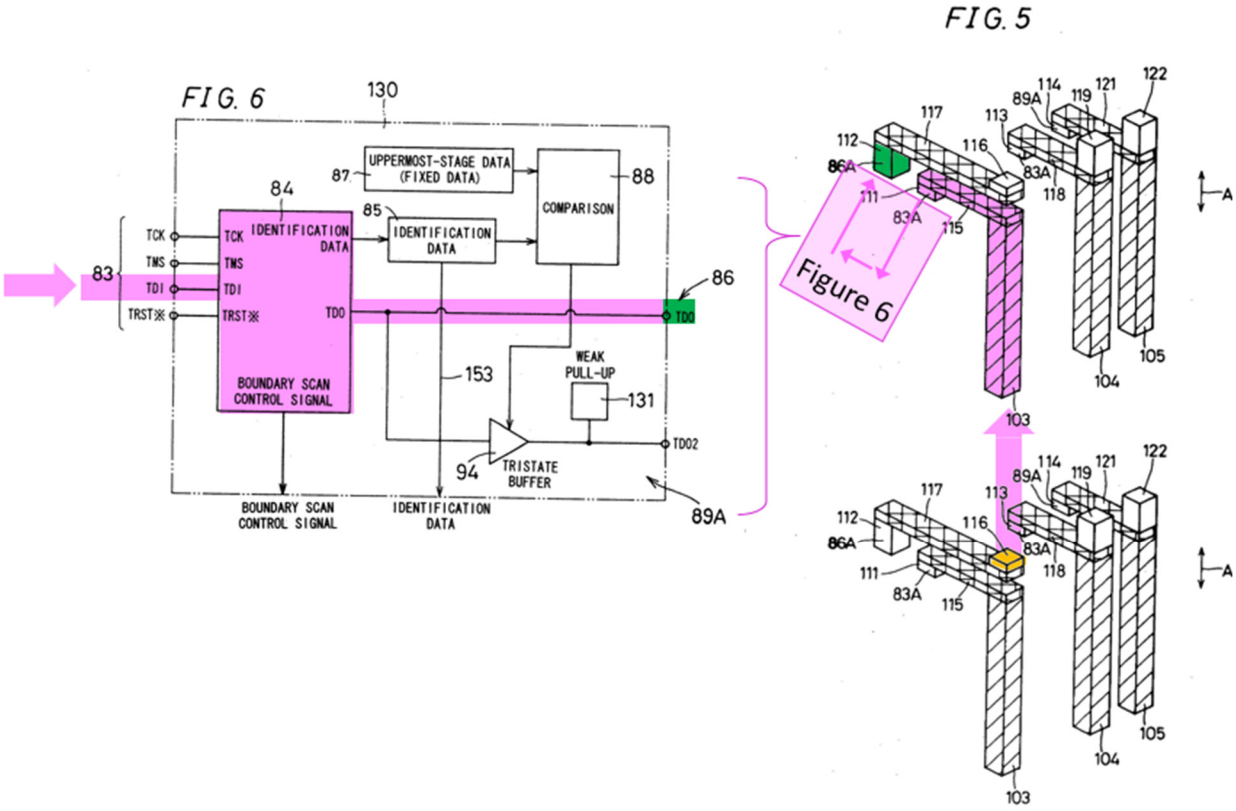
Sato's connections between stacked memory modules are the claimed serial chain connections. And, as illustrated above, a **serial chain route**, which includes multiple serial chain connections, is formed when the memory modules are stacked.

As further explained below, each of Sato's serial chain connection comprises a serial chain input connected to a serial chain circuit, which is connected to a serial chain output.

Further, each module's **connection terminal 116** is the serial chain input for

the module above it because it receives and carries the TDO signal.[4] (Ex. 1004, 24:19-22; Ex. 1002, ¶¶ 129.) As illustrated below, **connection terminal 116** is coupled with the **output section connection terminal 86A** (serial chain output) of the adjacent memory module through a **signal path over penetrating electrode 103, first connection line 115, connection terminal 83A, and boundary scan controller 84** (serial chain circuit). (Ex. 1004, 23:26-24:2; Ex. 1002, ¶¶ 128-36.) **Output section connection terminal 86A** then provides the TDO signal to the module above. (*Id*., 14:29-15:8, 15:26-29; Ex. 1002, ¶ 135.)

[4] The bottom surface of penetrating electrode 103 and/or the ball on connection terminal 116 (*see* footnote 3) are also serial chain inputs because they receive the TDO signal. (Ex. 1002, ¶ 130). Thus, to the extent Patent Owner argues the serial chain input must be a ball, Sato discloses that.



(Ex. 1002, ¶¶ 132-33 (modifying Fig. 5 to show interconnections after stacking).)

Thus, when the modules are stacked, the TDO signal on **connection terminal 116** becomes the TDI signal into the module above it, which is then carried along the serial chain circuit. (*Id.,* 23:28-32, Fig. 3.)

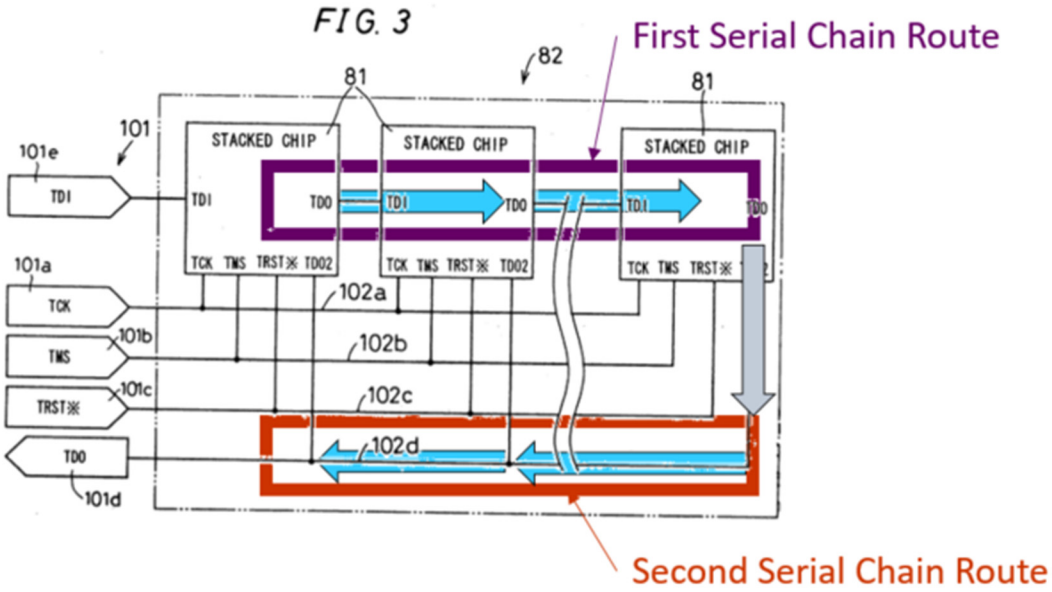
As shown in Figure 6, the serial chain circuit (carrying the TDI signal) passes through the **boundary scan controller circuit 84**. (Ex. 1002, ¶ 131-34.) **Boundary scan controller circuit 84** receives the TDI signal and outputs it as the TDO to the next upper module via **connection terminal TDO 86A.** (Ex. 1004, 13:30-14:15, 14:29-15:8, 15:26-29; Ex. 1002, ¶ 131-34.)

f. "coupling said serial chain input with said serial chain output through said serial chain circuit;"

As discussed above in Section IX.A.1.e, **connection terminal 116** is coupled with the **output section connection terminal 86A** of the adjacent memory module through a **signal path over penetrating electrode 103, first connection line 115, connection terminal 83A, and boundary scan controller 84**.

g. "forming a second serial chain route;"

Sato satisfies this claim element through its disclosure of the TDO2 signal being routed across circuitry connected in series, shown below. (Ex. 1004, 24:10-24.)



(Ex. 1004, Figs. 3.)

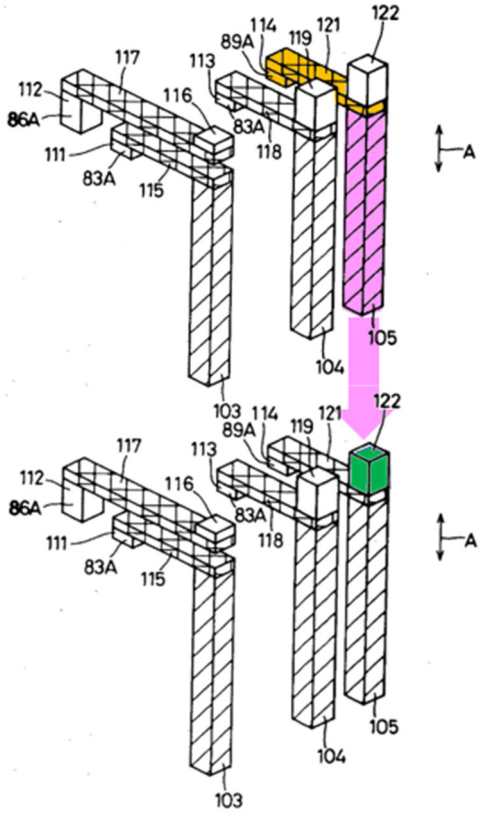
Unlike the "first serial chain route," claim 12 does not state that the "second serial chain route" must include a serial chain connection that itself includes a serial

chain circuit, input, and output.

Nevertheless, **connection terminal 89A** and **connection line 121** are (individually or collectively) a serial chain input because they receive the TDO2 signal. (Ex. 1004, 23:24-25, 24:10-24; Ex. 1002, ¶ 140.) **Connection terminal 89A** and **connection line 121** are coupled by **penetrating electrode 105** to the lower module's **connection terminal 122**, as shown below. (Ex. 1004, 24:10-16; Ex. 1002, ¶¶ 140-41.) **Connection terminal 122** is the serial chain output because it outputs the TDO2 signal to the lower module.[5] (Ex. 1002, ¶ 141).

[5] The bottom surface of penetrating electrode 105 and/or the ball on connection terminal 122 (*see* footnote 3) are also serial chain outputs because they provide the TDO2 signal to the lower module. (Ex. 1002, ¶ 141). Thus, to the extent Patent Owner argues the serial chain output must be a ball, Sato discloses that.

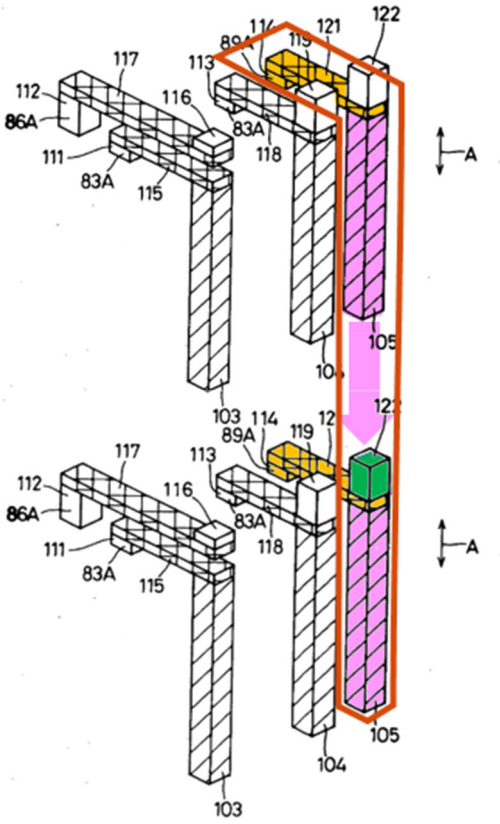
FIG. 5



(Ex. 1002, ¶¶ 143-44 (modifying Fig. 5 to show interconnections after stacking).)

Accordingly, when the memory modules are stacked, at least two of these serial chain connections forms a second serial chain route as shown below (*Id.*):

FIG. 5

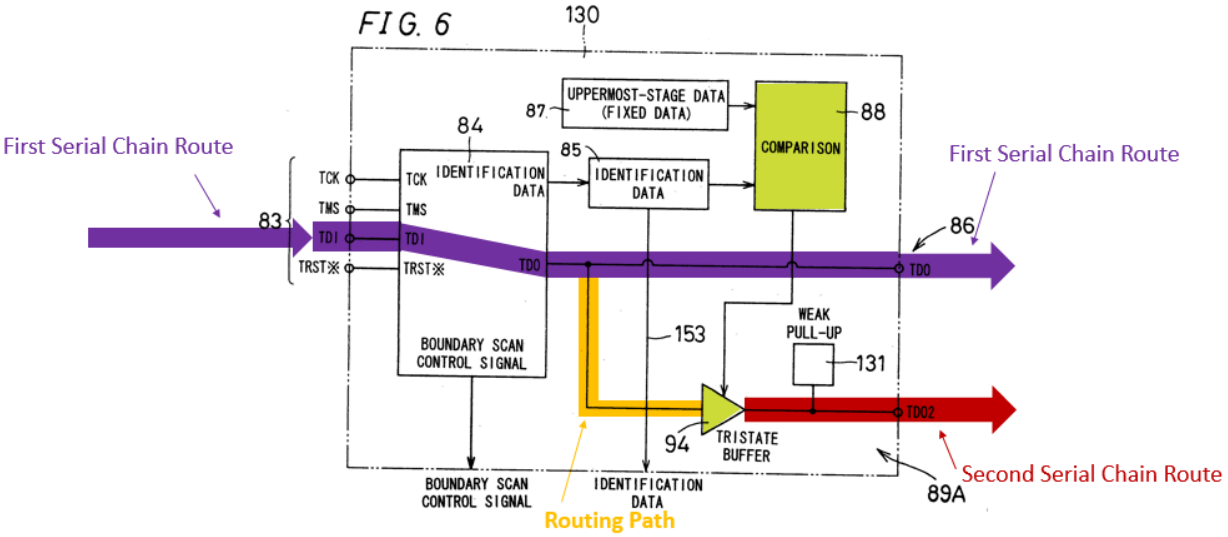


h. "forming a control circuit for enabling a routing path that connects said first serial chain route with said second serial chain route within an end module;"

Sato discloses forming control circuitry (**tri-state buffer 94** and **comparison means 88**) in each stacked memory module that can enable a routing path that connects the first serial chain route with the second serial chain route, as illustrated in Figure 6 below. As explained above, first serial chain route passes through boundary scan controller 84 and connection terminal TDO 86A. *See* Section IX.A.1.e. And the second serial chain route passes over connection terminal 89A. *See* Section IX.A.1.g.

As explained above, a serial circuit called a daisy chain carries the TDI signal into a memory module, which exits the module as TDO and then enters the next upper module as TDI. This is the claimed first serial chain route. However, when the TDI signal enters the uppermost memory module, there is no upper module for the TDI signal to enter. Instead, the signal exits the uppermost memory module through ***TDO2***, and then traverse the second serial chain route described in Section IX.A.1.g. Sato's routing path connects the TDI line to TDO2.

Sato's routing path is shown in annotated Figure 6 and connects the first serial chain route (TDI/TDO) to the second serial chain route (TDO2).



(Ex. 1002, ¶¶ 145-56.)

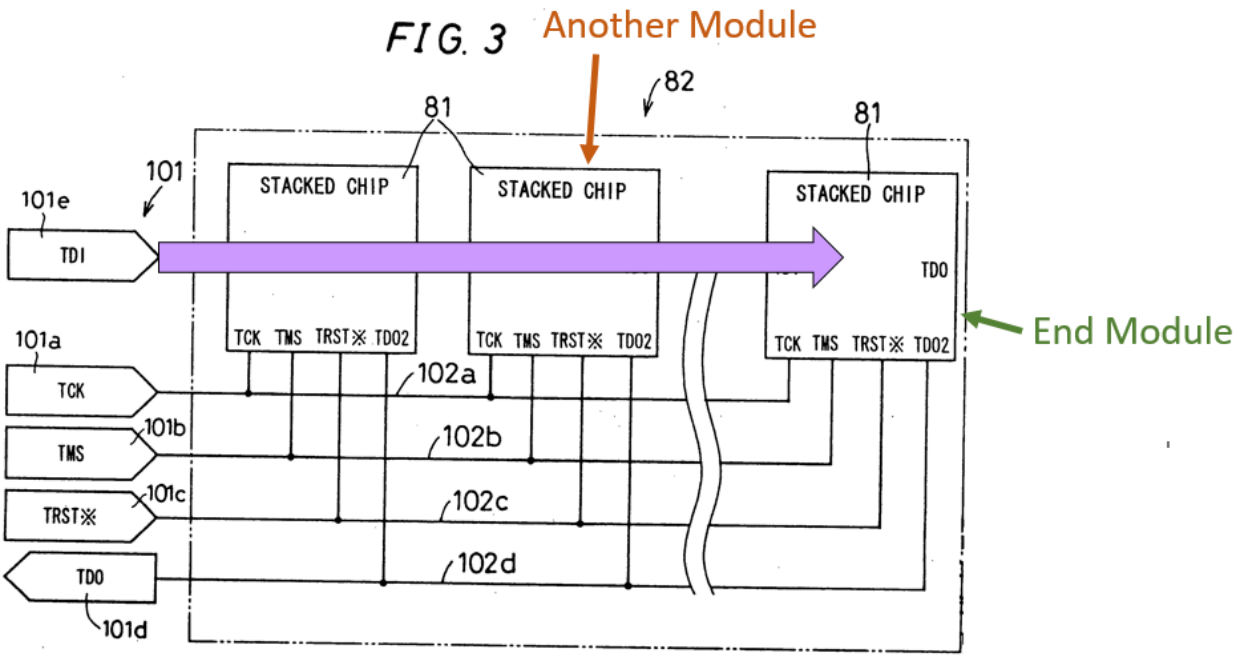
Sato's **routing path** is enabled by a control circuit: **tri-state buffer 94** and **comparison means 88**. (*Id.*, ¶ 146.) When the **tri-state buffer 94** is turned on, Sato states that the TDI signal line (first serial chain route) is connected to the TDO2

signal line (second serial chain route). (Ex. 1004, 25:19-25; Ex. 1002, ¶ 146.) If the **tri-state buffer 94** is turned off, the routing path is not enabled because the TDO2 signal line does not output the TDO signal. (*Id.*)

Further, Sato explains the tri-state buffer is only enabled when the **comparison means 88** determines that it is in the uppermost memory module, i.e., an end module. (Ex. 1004, 16:1-18, 25:19-25; Ex. 1002, ¶¶ 148-50.) Therefore, Sato discloses that the routing path is enabled in the end module. (*Id.,* Fig. 3.) The '103 patent's control circuit is also a tri-state buffer that detects whether it is located in the uppermost module. (Ex. 1001, 11:11-29.)

i. "said control circuit is disposed to enable said routing path in response to a control input signal received from another module from the plurality of modules when said end module is coupled to said another module."

Sato explains that the **tri-state buffer** and **comparison means 88** enable the routing path by comparing a control input signal (**identification data 85**) to uppermost-stage data 87. (Ex. 1004, 16:1-18, 25:19-25; Ex. 1002, ¶¶ 152-54.) The memory module receives **identification data 85** every time the device turns on. (Ex. 1004, 15:9-12; Ex. 1002, ¶ 153.) The end module's control circuit receives **identification data 85** from the penultimate memory module—"another module"—because **identification data 85** is sent over the daisy chain route from JTAG tester connector pins 101. (Ex. 1004, 20:12-13, 21:24-22:2, Fig. 3; Ex. 1002, ¶ 153.)



(Ex. 1002, ¶ 153.)

2. *Dependent Claim 16*

a. "The method of claim 12;"

See Section IX.A.1.

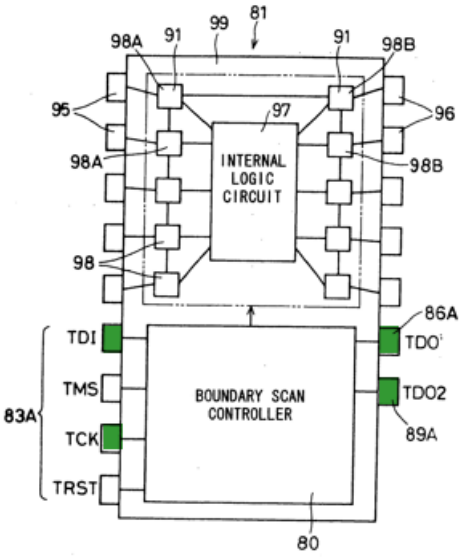
b. "adding to the plurality of modules a controller module that is disposed with an **active pad**;"

Sato discloses that each stacked memory module has a boundary scan controller. (Ex. 1004, 16:1-7 (stating that each of the modules in the stack has a "controller 80").) Therefore, any of Sato's stacked **memory modules** can also be considered to be a controller module. (Ex. 1002, ¶¶ 156-60.)

As discussed in Section IX.A.1.b, Sato discloses forming one or more active pads (e.g., **connection terminal 86A** and **89A**) on each stacked **memory module**. (Ex. 1004, 6:25-29, 18:10-19:30, Figs. 2 (below), 5; Ex. 1001 at 9:8-9 ("An active

pad may be also referred to herein as an 'active port.'"); Ex. 1002, ¶ 159.)

FIG. 2



(Ex. 1004, Fig. 2.)

c. "providing a ladder-like routing path that includes a connection between said active pad from said controller module and one of said passive ports by stacking said first memory module with said controller module."

As discussed in Section IX.A.1.d, Sato discloses that each active port is coupled to a passive port on an adjacent memory module and that each memory module can also be considered to be a controller module. The '103 patent explains that passive ports can follow a "ladder-like" routing path, "such as 1905." (Ex. 1001, 9:16-48.) Figure 19 of the '103 patent identifies three "ladder-like" routing paths. (*Id.*)

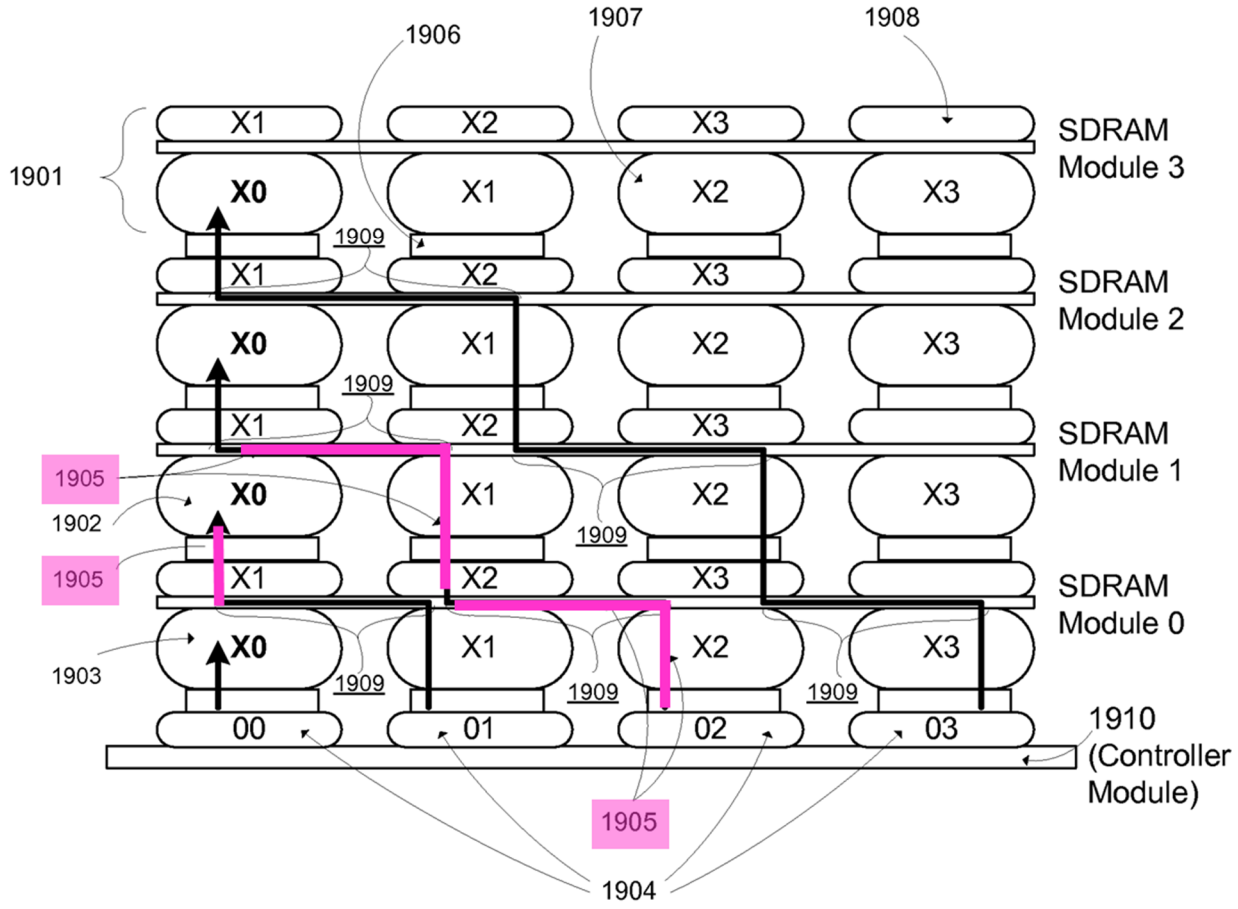


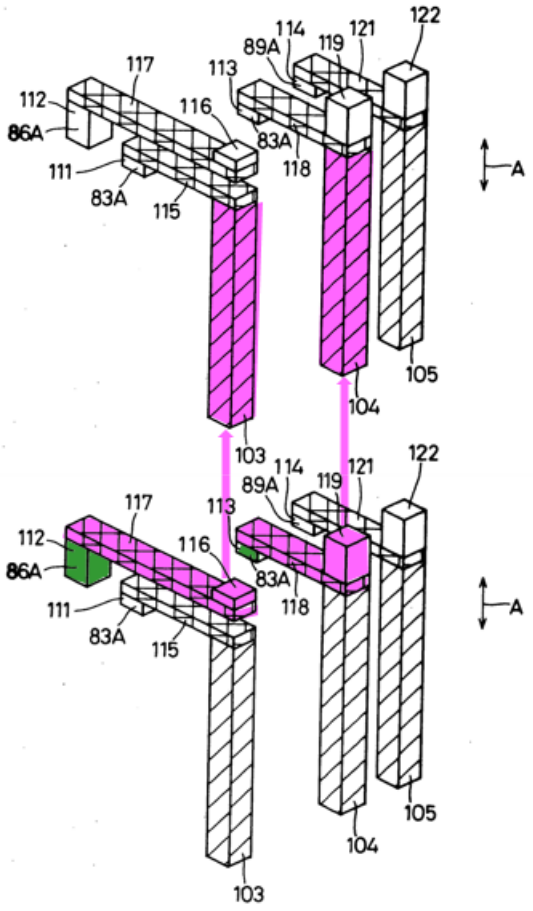
Figure 19

(Ex. 1001, Fig. 19.) The ladder-like routing path has one vertical portion, i.e., in a direction extending into or out of a surface of a module, and one horizontal portion, i.e., in a direction along the surface of the module. (Ex. 1001, 9:16-48; Ex. 1002, ¶¶ 162-63.)

Sato discloses the same ladder-like routing path. Modified Figure 5 (below) illustrates that a ladder-like routing path is formed between **TDO 86A** and the top end of penetrating electrode 103 when the memory modules are stacked. (Ex. 1004,

23:23-24:2.) This is a ladder-like routing path because it includes a horizontal portion (e.g., second connection line 117) and a vertical portion (e.g., penetrating electrodes 103). (Ex. 1002, ¶ 164.)

FIG. 5



(Ex. 1002, ¶ 165.)

B. Ground 2: Claims 12 and 16 Are Obvious Over Sato in view of Gaynes

1. *The Combination of Sato and Gaynes*

As shown above, Sato alone renders obvious claims 12 and 16. Patent Owner may argue that the claimed "active port" or "passive port" requires the particular ball

and pad structures described in the '103 specification (e.g., Ex. 1001, 9:21-24). This argument is incorrect and, in any event, Sato discloses ball and pads.[6] (Ex. 1002, ¶ 116.)

Further, it would have been obvious to a POSITA to use ball and pad structures in Sato. Before the filing of the '103 patent, balls and pads were well-known structures used to form interconnections between stacked modules. (Ex. 1002, ¶ 167.)

Gaynes provides an advantageous method and structure of connecting signal lines in stacked memory modules. (Ex. 1002, ¶ 170) For example, Gaynes discloses a method of forming penetrating electrodes in the form of thru-silicon vias ("TSVs") in connection with pads and balls. As shown in Figures 3 and 4, Gaynes discloses forming pads (surface deposits 33) on the surface of the silicon chip by depositing a conductor on the periphery of via 31. (Ex. 1005, 8:26-30.)

[6] *See* footnote 3.

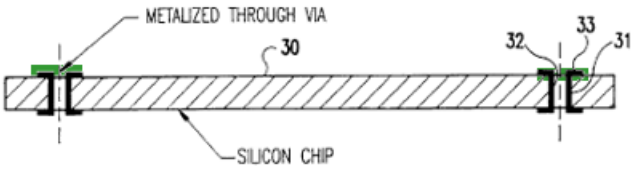


FIG.3

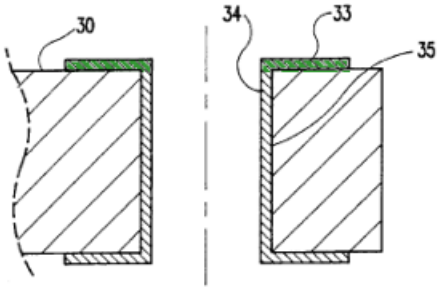


FIG.4

(Ex. 1002, ¶¶ 170-71 (discussing Figs. 3-4).) The pads are metal layers that "facilitate[] the formation of on-chip and chip-to-chip connections." (Ex. 1005, 8:20-25.) Gaynes further discloses forming balls by heating together layers of lead and tin to form an alloy to electrically and physically connect pads of two adjacent modules. (*Id.,* 9:45-10:7)

It would have been obvious to a POSITA to implement the ball, pad, and TSV structure taught by Gaynes when forming Sato's penetrating electrodes. While Sato generally describes pads (e.g., connection terminals), it does not describe the materials used to implement them. Further, Sato does not explicitly mention how to form balls. Thus, a POSITA would have been motivated to look to known prior art, such as Gaynes, for the implementation details of forming balls and pads in order to stack modules. (*Id.,* ¶ 172.) Additionally, a POSITA would have recognized that

the methods used by Gaynes to fabricate the balls, pads, and TSV provide several benefits, such as enhanced durability, noise immunity, and electrical performance. (Ex. 1002, ¶ 173.)

A POSITA would have had a reasonable expectation of success in combining these references. (Ex. 1002, ¶¶ 174-78.). Like Sato, Gaynes teaches connecting stacked memory chips with TSV interconnections. (*See* Ex. 1005, Abstract (referring to "[c]hip stacks … such as memory chips"); Ex. 1002, ¶ 174.) The via-to-via, via-to-pad, and pad-to-pad structures taught by Gaynes (Ex. 1005, 10:14-18) perform the same purpose as the penetrating electrodes and connection lines disclosed by Sato. (Ex. 1002, ¶ 175.) Further, Gaynes' pads perform the same purpose as Sato's connection terminals. (*Id.*) Sato's penetrating electrode could be implemented using Gaynes' TSV because they both connect provide to an electrical connection between surfaces of the silicon chip.

Thus, implementing the ball, pad, and TSV structure taught by Gaynes when forming the penetrating electrodes disclosed by Sato represents nothing more than the combination of known elements in known ways that would have yielded predictable results to a POSITA. (Ex. 1002, ¶¶ 176-77.)

2. *Independent Claim 12*

a. "12. A method for stacking a plurality of modules, said plurality of modules including a first memory module and a second memory module; said first memory module having a first surface and a second surface; said second memory module having a third surface and a fourth surface; said method comprising;"

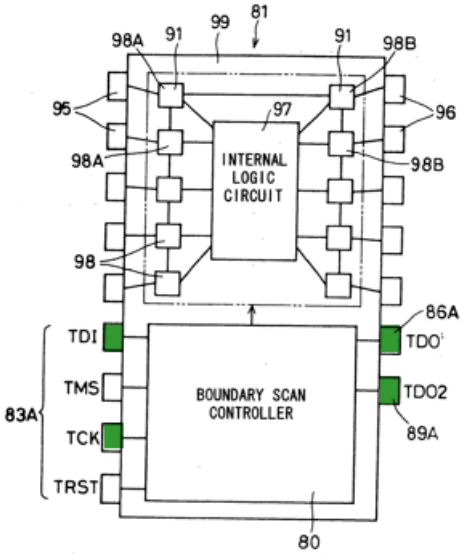
See Ground 1, Section IX.A.1.a.

b. "forming one or more active ports on the first and second memory modules, said one or more active ports for carrying one or more active signals;"

Sato, in view of Gaynes, renders obvious this element. (Ex. 1002, ¶¶ 180-83.)

As discussed in Section IX.B.2.b, Sato discloses forming active ports on the memory module.

FIG. 2



(Ex. 1002, ¶ 180.)

Gaynes discloses forming an active port using **surface deposits 33** on the surface of the silicon chip. (Ex. 1005, 8:26-30.)

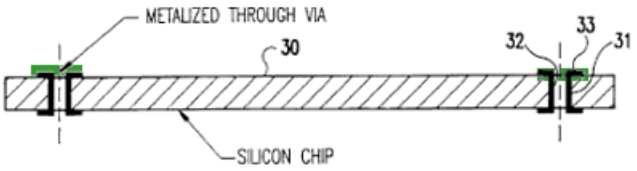


FIG.3

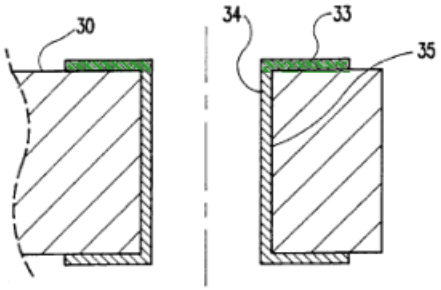


FIG.4

(Ex. 1002, ¶ 181.)

These **surface deposits 33** are active ports at least because they are metal contact pads that "facilitate[] the formation of on-chip and chip-to-chip connections." (Ex. 1005, 8:20-25; Ex. 1001 at 9:8-9 ("An active pad may be also referred to herein as an 'active port.'"); Ex. 1002, ¶ 182.) A POSITA would have found it obvious to use these surface deposits to form Sato's contact pads, as discussed above. (Ex. 1002, ¶¶ 166-78.)

c. "forming one or more passive ports on the first and second memory modules, said one or more passive ports for passing through said one or more active signals on the first and second memory modules;"

As discussed above in Section IX.B.1, a POSITA would have been motivated to use Gaynes' method of forming a **TSV** structure to form Sato's **penetrating electrodes**, which are formed on each module.

Gaynes explains that the **TSV** is filled with **metallization 34** to provide an electrical connection between surfaces of the silicon chip. (Ex. 1005, 8:26-34.) The **metallization 34** is a passive port at least because it passes through an active signal and is a connection between a passive pad on one surface of the module (surface deposit 33 on the lower surface of a chip) and a passive ball on another side of the module (regions 61 and 62). (Ex. 1001 at 9:19-23; Ex. 1002, ¶¶ 185-86.)

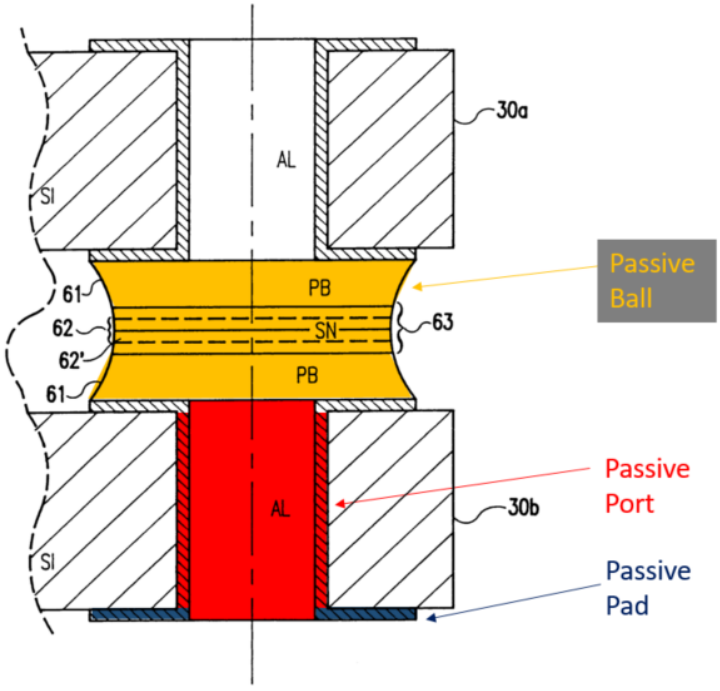


FIG.6

(*Id.*)

Lead layers 61 and tin layers 62 and 62' are heated together to form an alloy that electrically connects the surface deposit 33 on a module with the adjacent stacked module. (Ex. 1005, 9: 451-10:7.) A POSITA would have understood this process of melting tin and lead into an alloy is soldering. (Ex. 1002, ¶¶ 185-86.) Accordingly, to the extent Patent Owner argues a ball is required, lead layers 61 and tin layers 62 and 62' form a solder ball. (*Id.*)

d. "coupling one of said active ports formed on said first memory module to one of said passive ports formed on said second memory module by stacking said first memory module to said second memory module;"

Sato discloses coupling the penetrating electrodes of a memory module with contact pads of the memory module stacked below. *See* Section IX.A.1.d.

Similarly, the TSV structure taught by Gaynes couples the active ports of one memory module to the passive ports of a memory module stacked above. (Ex. 1002, ¶¶ 188-89.) As illustrated in Figure 6, the **surface deposit 33 (**active port**)** on the upper surface of the bottom module is coupled to the **metallization 34** (passive port) on a module stacked above layers 61 and 63. (*Id.*)

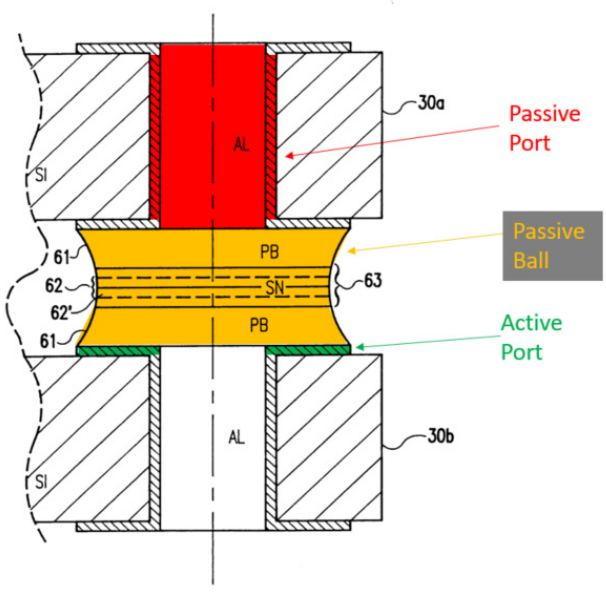


FIG.6

(Ex. 1005, Fig. 6.)

e. "forming a first serial chain route that includes at least one serial chain connection, said serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output;"

f. "coupling said serial chain input with said serial chain output through said serial chain circuit;"

g. "forming a second serial chain route;"

Sato renders obvious these elements for the reasons described above. *See* Sections IX.A.1.e-g. If Patent Owner argues Sato does not disclose or render obvious the balls described in footnotes 4 and 5, Sato, in view of Gaynes, renders them obvious. (Ex. 1002, ¶¶ 190-94.) As discussed above, a POSITA would have found it obvious to implement the balls taught by Gaynes when forming the penetrating electrodes disclosed by Sato. Section IX.B.1. And Gaynes discloses solder balls coupled to contact pads. *See* Sections IX.B.2.c-d. Accordingly, Sato, in view of Gaynes, renders obvious these elements. (Ex. 1002, ¶¶ 190-94.)

h. "forming a control circuit for enabling a routing path that connects said first serial chain route with said second serial chain route within an end module;"

i. "said control circuit is disposed to enable said routing path in response to a control input signal received from another module from the plurality of modules when said end module is coupled to said another module."

Sato renders obvious these elements for the reasons described above. *See* Sections IX.A.1.h-i.

3. *Dependent Claim 16*

a. "The method of claim 12;"

See Section IX.B.2

b. "adding to the plurality of modules a controller module that is disposed with an active pad;"

Sato discloses that each stacked **memory module**, including the bottommost module, could be considered a controller module. *See* Section IX.A.2.b. And Sato, in view of Gaynes, renders obvious active pads[7] on each stacked memory module. *See* Section IX.B.2.b.

c. "providing a ladder-like routing path that includes a connection between said active pad from said controller module and one of said passive ports by stacking said first memory module with said controller module."

Sato, in view of Gaynes, renders obvious that each active port is coupled to a passive port of an adjacent memory module. *See* Section IX.B.2.d. And Sato discloses coupling an active pad on a controller module to a passive port that is not directly above said active pad, which requires a ladder-like routing path. *See* Section IX.A.2.c.

Gaynes also discloses how to route signals horizontally and vertically. For example, Gaynes teaches "pad-to-pad" connections 71 and 73 that horizontally

[7] "An active pad may be also referred to herein as an 'active port.'" Ex. 1001 at 9:8-9.

connect contact pads on the same surface of a module. (Ex. 1005, 10:29-39; Ex. 1002, ¶¶ 199-201.) The contact pads that are connected by the pad-to-pad connections are then vertically routed through "via-to-pad" connections to other contact pads on the opposite surfaces of their respective modules. Accordingly, Gaynes teaches how to form a ladder-like routing path. (Ex. 1002, ¶¶ 199-201.)

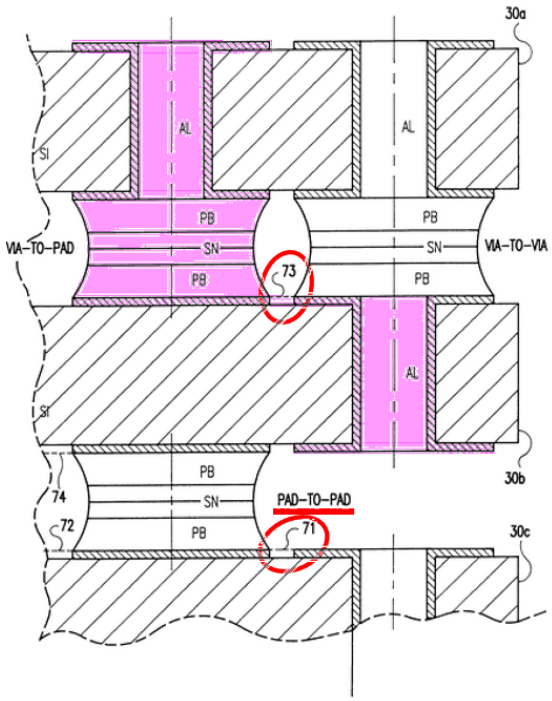


FIG.7

(Ex. 1005, Fig. 7.)

A POSITA would have understood that the ladder-like routing path taught by Gaynes would be obvious and useful to horizontally and vertically route the signals of Sato. (Ex. 1002, ¶ 200.) For example, Sato's connection line 117 and penetrating electrodes 103, which route TDO signals, can be implemented with the method of forming pad-to-pad connections and via-to-pad structures taught by Gaynes. (*Id.*)

Similarly, signal lines 118 and 121 and penetrating electrodes 104 and 105 can be formed with the method and structure disclosed by Gaynes. (*Id.*)

Additionally, Gaynes teaches that "[c]onnections may be provided by conductors having substantial vertical as well as horizontal segments" because, among other reasons, three degrees of freedom can lead to a more compact design. (Ex. 1005, 6:63-7:3.) Thus, a POSITA would be motivated to use the pad-to-pad and via-to-pad structures of Gaynes to connect the active pads of the Sato stacked modules to adjacent memory modules. (Ex. 1002, ¶ 200.)

C. Ground 3: Claims 12 and 16 Are Obvious Over Sato in view of Eide

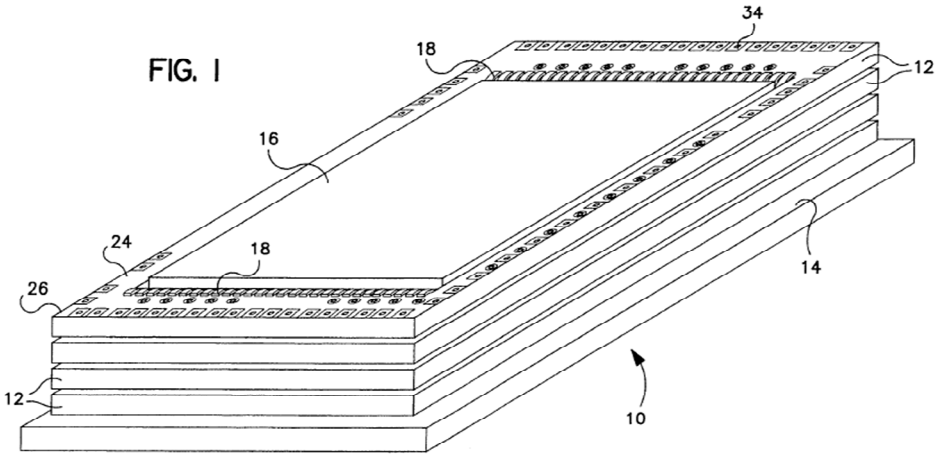
1. *The Combination of Sato and Eide*

Sato renders obvious claims 12 and 16, as discussed above. Nevertheless, Patent Owner may argue that the claimed "memory module" is limited to a semiconductor chip mounted on a PCB substrate. Such an argument would be misguided, however, as Eide discloses that structure, and it would have been obvious to a POSITA to implement it in Sato.

Sato discloses a method of stacking semiconductor chips using TSV. *See* Section IX.A.1.a. Sato does not explicitly state whether the chip is mounted on a PCB substrate before being stacked. (*Id.,* ¶ 203.) Nevertheless, stacking integrated circuit chips mounted on PCB substrates was well-known in the art at the time, and

a POSITA would be motivated to implement this method and structure with Sato's chips. (*Id.,* ¶ 204.)

Eide teaches a method of stacking integrated circuit chips mounted on PCB substrates. (Ex. 1006, 2: 59-62.) Eide's Figure 1 depicts the stacked PCBs:



(Ex. 1006, Fig. 1.) Chip package 12 is a printed circuit board ("PCB") frame that holds integrated circuit chip 19, which is embedded in TSOP package 16. (Ex. 1006, 5:32-50, 5:62-65, Figs. 2 and 5.) Multiple chip packages 12 are soldered together to form chip stack 10. (*Id.,* 5:15-31.)

It would have been obvious to a POSITA to use the PCB stacking method taught by Eide to stack Sato's memory chips. (Ex. 1002, ¶ 207.)

Both Sato and Eide are directed toward the stacking of semiconductor chips. (*See* Ex. 1006, 3:39-60; Ex. 1004, Abstract; Ex. 1002, ¶ 208.) Like Sato, Eide teaches connecting stacked memory using vertical vias. (*See* Ex. 1006, 8:22-26 (stating that the upper and lower conductive pads within each PCB "are coupled

together by vertically disposed vias 92"); Ex. 1004, Abstract, 10:29-11:10, 23:7-8 ("penetrating electrodes").)

The integrated circuit chip 19 taught by Eide is similar to the semiconductor chip assembly 81 of Sato. (Ex. 1002, ¶ 210.) Both are semiconductor memory chips. (*See* Ex. 1004, 10:29-11:10 ("[T]he semiconductor circuit chip is a memory chip . . . ."); Ex. 1006, 4:45-46 ("[T]he various chips within the stack 10 comprise memory chips.").) Both Sato and Eide teach methods of stacking identical chips. (*See* Ex. 1004, 10:26-28 ("[I]dentical semiconductor circuit chip assemblies are stacked …"); Ex. 1006, claim 9 ("integrated circuit chip packages . . . being of identical configuration to the other chip packages in the stack"); Ex. 1002, ¶ 211.)

Eide's vertical vias 54 and 92, and their respective conductive pads and conductive lines, serve a similar purpose as Sato's penetrating electrodes and connection lines—electrically connecting stacked modules. (Ex. 1002, ¶ 212.) For example, Eide teaches that conductive trace 48 "couples the conductive pads 20 and 22" to vias that "extend through the thickness of the frame." (Ex. 1006, 6:7-12.) And Sato discloses that "penetrating electrode 103 is interconnected to the terminal 111 . . . through the first connection line 115." (Ex. 1004, 23:26-27.)

Eide's PCB stacking method has several benefits over Sato's TSV stacking method. (Ex. 1002, ¶¶ 213-16.) Since Eide's PCB stacking requires just a few steps, the stack is easy to assemble and reassemble. (Ex. 1006, 2:39-55, 3:26-29; Ex. 1002,

¶ 214.) The ability to easily replace memory modules found to be defective is highly advantageous with respect to Sato, which teaches a boundary scan method, which is used for testing and debugging modules. (Ex. 1004, 1:9-12.) Thus, defective modules identified by Sato's boundary scan can be more easily and economically replaced using Eide's PCB stacking method. (Ex. 1002, ¶¶ 213-16.) Moreover, Eide's method is economical because it does not require the costly, advanced fabrication techniques required by TSV. (*Id.,* ¶¶ 215-16.) Eide's stacking method is also cost-effective because it requires only a few simple, well-known, process steps. (Ex. 1006, 2:39-51.) For instance, conductive traces, conductive pads, and through hole vias, which Eide uses, can be easily achieved with equipment commonly used in the field. (Ex. 1002, ¶ 215.) Further, Eide's method minimizes stress by mounting chips on PCBs. (Ex. 1006, 3:31-38; Ex. 1002, ¶ 216.)

A POSITA would have understood that Sato's memory modules could be stacked with a variety of different stacking methods. (Ex. 1002, ¶ 217.) Although Sato's stacking with penetrating electrodes (i.e., TSVs) has some benefits, such as decreased conductor length, it also has potential drawbacks: TSV fabrication can be more expensive, complex, and have lower yield than PCB stacking methods. (Ex. 1002, ¶ 217.) TSV is generally used in the higher margin, higher volume designs. A POSITA would weigh the costs and benefits of TSV compared to a more

traditional PCB stacking method, like the one disclosed by Eide, on a case-by-case basis. (*Id.*)

Thus, a POSITA would have understood that Sato's method of stacking using TSV provided certain benefits for certain specialized market segments, while Eide's simpler, less expensive, and proven approach would have been preferred for other market segments. (*Id.,* ¶ 219.) Indeed, TSVs through silicon wafers are, to this day, used less than Eide's more traditional packaging techniques. (*Id*.)

The combination of Sato and Eide would be simple and would not change Sato's serial chains or the semiconductor circuit assembly (including the boundary scan controller). (Ex. 1002, ¶¶ 221-22.) It would have been routine for a POSITA to mount Sato's chip (e.g., "semiconductor chip assembly 81") in Eide's stack structure as the integrated circuit chip 19.

Sato in view of Eide

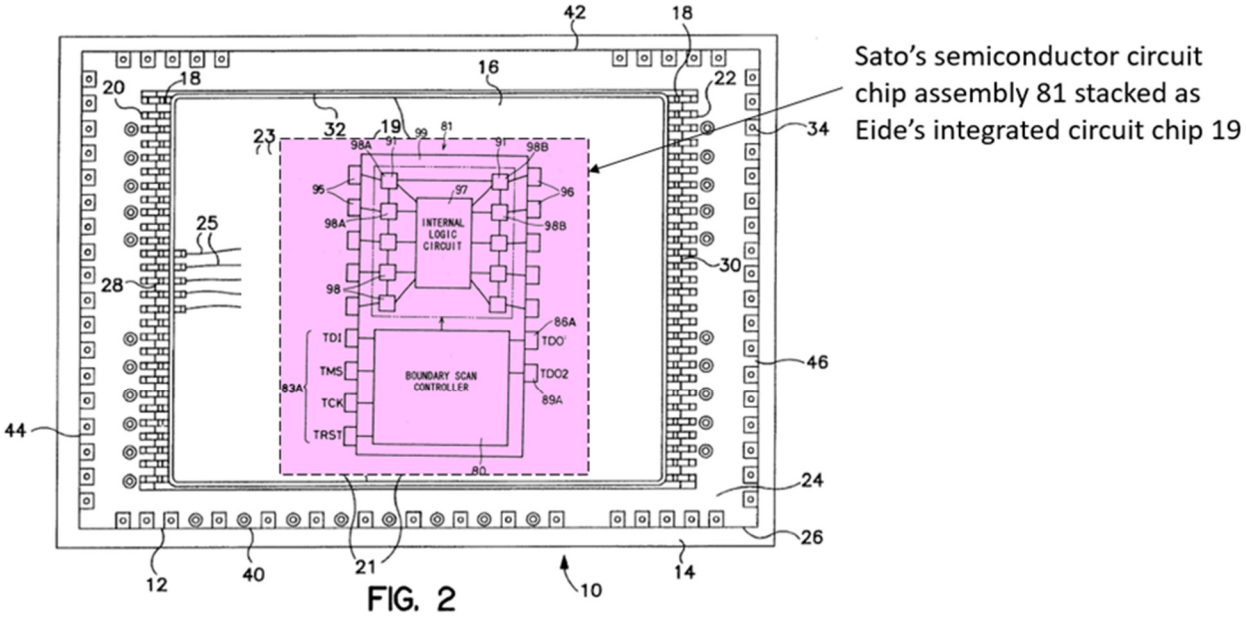


FIG. 2

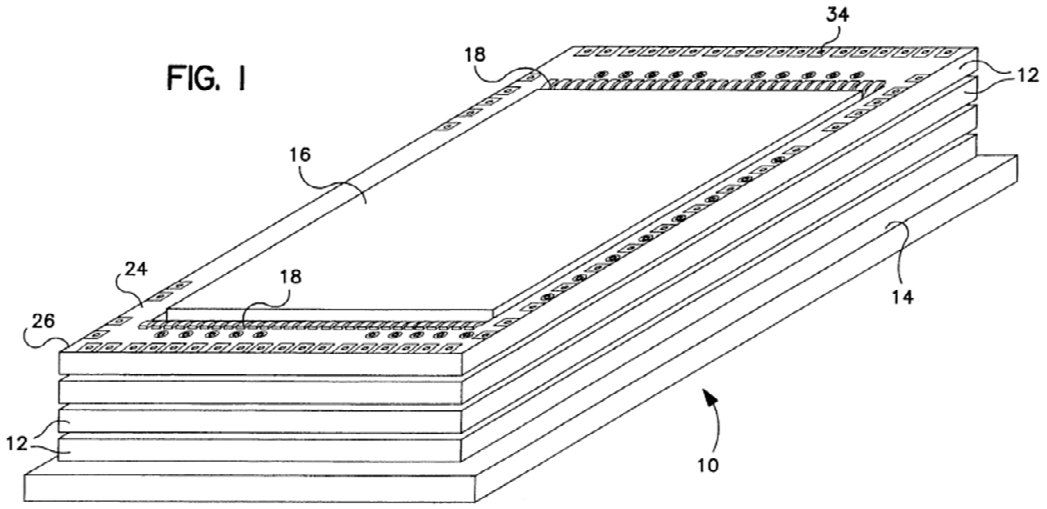
(Ex. 1002, ¶¶ 221-22 (depicting the combination of Sato and Eide).)

A POSITA would have understood that only small implementation details of Sato would be affected by this combination. (Ex. 1002, ¶ 222.) A POSITA would have understood that Sato's penetrating electrodes and terminals could be implemented using Eide's vertical vias and conductive pads, respectively, when Sato and Eide are combined. (Ex. 1002, ¶ 222.) Accordingly, POSITA would have had a reasonable expectation of success in combining these references. (Ex. 1002, ¶¶ 218-22.).

2. *Independent Claim 12*

a. "12. A method for stacking a plurality of modules, said plurality of modules including a first memory module and a second memory module; said first memory module having a first surface and a second surface; said second memory module having a third surface and a fourth surface; said method comprising;"

To the extent the preamble is limiting, Sato, in view of Eide, discloses the preamble. *See* Section IX.A.1.a (showing Sato discloses preamble). Moreover, Eide discloses a stack of modules. (Ex. 1006, 2:61-62 ("stack of chip packages mounted on a substrate").) Eide's stacked chip package 12 are memory modules. (Ex. 1006, 4:45-51.)



(Ex. 1006, Fig. 1.)

As illustrated in Figures 8 and 10, Eide's stacked PCBs each have an upper and a lower surface. (*See* Ex. 1006, 6:6-7 ("FIG. 8 shows the upper surface"), 5:9-12 ("[a]n opposite lower surface 36 of the frame").) Therefore, the first memory

module has a first and second surface, and the second memory module has a third and fourth surface. (Ex. 1002, ¶¶ 224-28.)

b. "forming one or more active ports on the first and second memory modules, said one or more active ports for carrying one or more active signals;"

Sato, in view of Eide, renders obvious this element. (Ex. 1002, ¶¶ 229-32.) Sato discloses this element. Section IX.A.1.b. Additionally, Eide discloses multiple active ports, as illustrated in Figure 12, in the form of **conductive pads 58, 34** that carry active signals to adjacent modules:

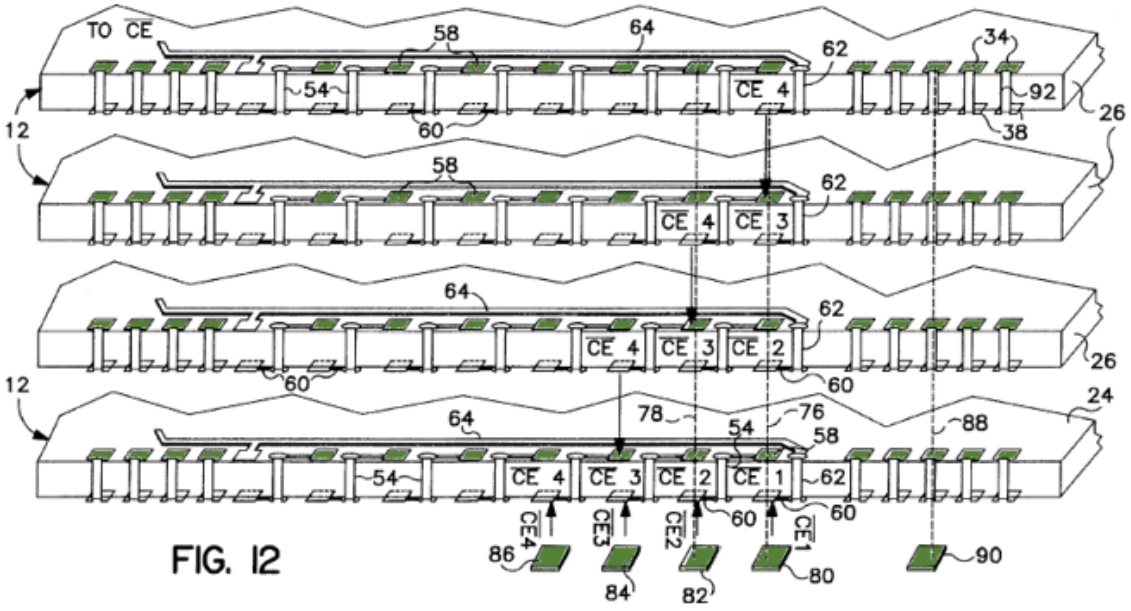


FIG. 12

(Ex. 1006, Fig. 12, 5:15-31, 8:25-30, 7:61-66; Ex. 1002, ¶¶ 229-32.)

Chip enable conductive pads 80, 82, 84, and 86 are also examples of active ports for carrying active signals such as chip enable signal CE 1. (Ex. 1006, 7:49-8:7; Ex. 1002, ¶ 231.)

c. "forming one or more passive ports on the first and second memory modules, said one or more passive ports for passing through said one or more active signals on the first and second memory modules;"

Sato, in view of Eide, renders obvious this element. Sato discloses this element. Section IX.A.1.c. Furthermore, Eide teaches forming multiple passive ports on each module—**vias 54 and 92**—that pass through the memory modules. (Ex. 1006, 6:26-39, 8:22-26; Ex. 1002, ¶ 233.) The **vias** are passive ports because they are electrical connections that pass active signals through the stacked memory modules from one surface to the other. (Ex. 1002, ¶¶ 234-38.)

For example, the **vias** couple conductive pads (e.g., 38 and 60) on the lower surface of a module to conductive pads (e.g., 34 and 58) on the upper surface of the same module. (*See, e.g.*, Ex. 1006, 6:22-33, 7:59-64, 8:18-33.) Figure 12 illustrates the passive ports.

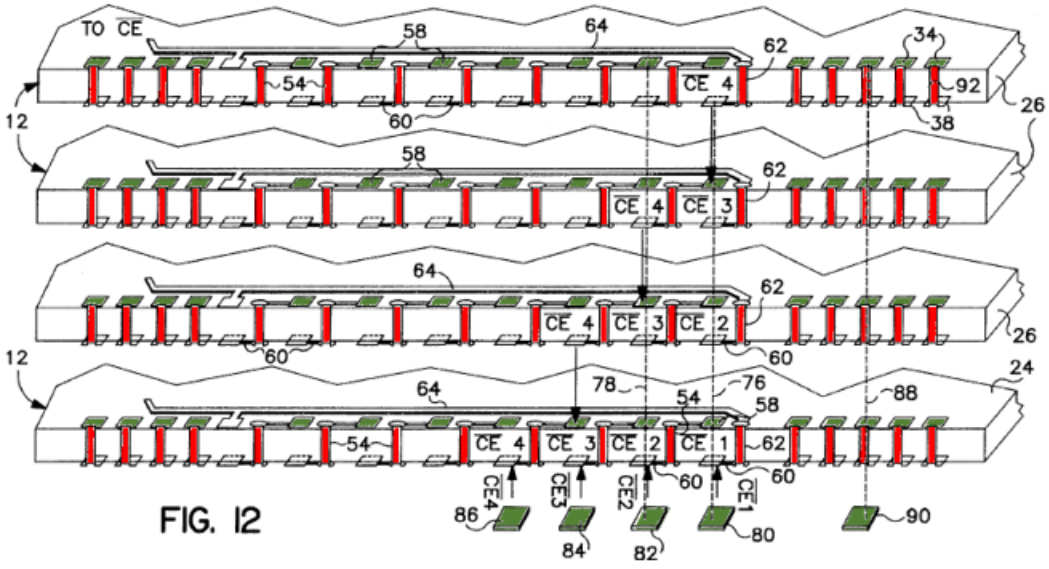
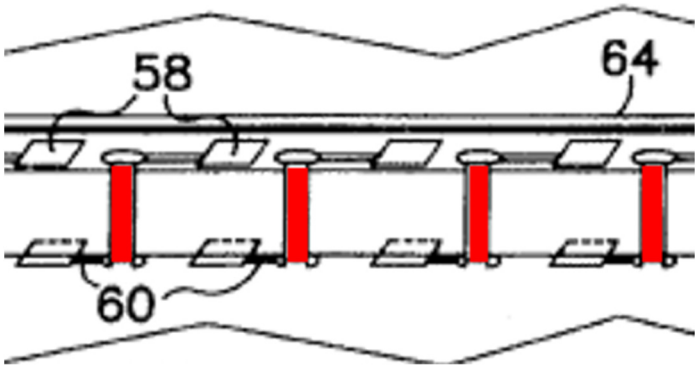
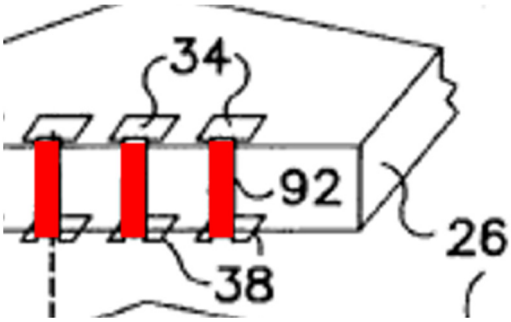


FIG. 12

(Ex. 1002, ¶ 234.)



(Ex. 1006, Fig. 12 (focusing on vias 54).)



(Ex. 1006, Fig. 12 (focusing on vias 92).)

As described in the next section, the **vias** are connected to a solder ball on the surface of chip package 12 because the conductive pads are soldered to the module stacked above or below it. (Ex. 1006, 5:29-31, 8:25-31.) Accordingly, if Patent Owner argues for a narrow construction of passive port, Sato, in view of Eide, renders obvious a connection between a passive ball (e.g., the solder on conductive pad 34 or 58) on one surface of a SDRAM module[8] and a passive pad (e.g., conductive pads 38 and 60) on another surface of the same SDRAM module. (Ex.

[8] *See* Section IX.A.1.a.

1002, ¶¶ 233-41.)

d. "coupling one of said active ports formed on said first memory module to one of said passive ports formed on said second memory module by stacking said first memory module to said second memory module;"

Sato, in view of Eide, renders obvious this element. Sato discloses this element. Section IX.A.1.d. Further, Eide teaches coupling one of said active ports **(e.g., 34 and 58)** formed on said first memory module to one of said passive ports **(vias 54 and 92)** formed on said second memory module by stacking said first memory module to said second memory module, as illustrated in Figure 12. (Ex. 1002, ¶ 242.)

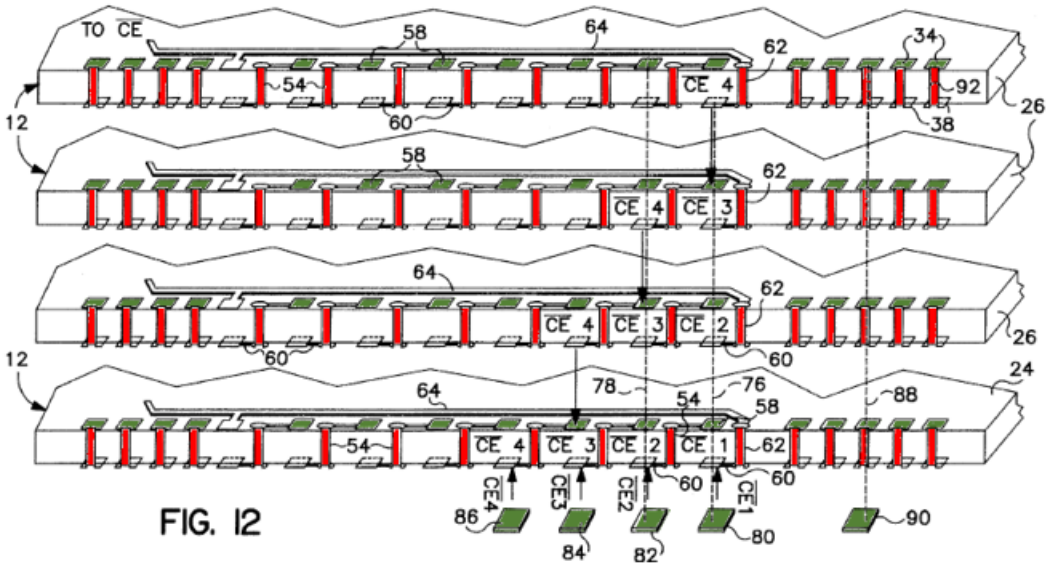


FIG. 12

(Ex. 1002, ¶ 242.)

As described above in Section IX.C.2.c, **via 54** couples conductive pad 60 on the lower surface to **conductive pad 58** on the upper surface, and **via 92** couples conductive pad 38 on the lower surface to **conductive pad 34** on the upper surface.

Then, **conductive pads 34 and 58** are soldered to the conductive pads 38 and 60, respectively, of the chip package stacked above it. (Ex. 1006, 5:29-31, 8:25-31.) Thus, the **conductive pads 34 and 58** are coupled to the **vias** of the module stacked above. (Ex. 1002, ¶¶ 242-44.)

e. "forming a first serial chain route that includes at least one serial chain connection, said serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output;"

f. "coupling said serial chain input with said serial chain output through said serial chain circuit;"

g. "forming a second serial chain route;"

Sato renders obvious these elements for the reasons described above. *See* Sections IX.A.1.e-g. The combination of Sato and Eide would be simple and would not change Sato's serial chains or the semiconductor circuit assembly (including the boundary scan controller). (Ex. 1002, ¶ 245.)

If Patent Owner argues Sato does not disclose or render obvious the balls described in footnotes 4 and 5, Sato, in view of Eide, renders them obvious. (Ex. 1002, ¶¶ 246-49.) Eide discloses solder balls coupled to contact pads, such as the solder ball on Eide's conductive pad 38 (*see* Sections IX.C.2.c-d) that would be used to implement Sato's connection terminals 116 and 89A in the proposed combination. (Ex. 1002, ¶¶ 246-49.) Accordingly, Sato, in view of Gaynes, renders obvious these elements. (*Id*.)

h. "forming a control circuit for enabling a routing path that connects said first serial chain route with said second serial chain route within an end module;"

i. "said control circuit is disposed to enable said routing path in response to a control input signal received from another module from the plurality of modules when said end module is coupled to said another module."

Sato renders obvious these elements for the reasons described above. Sections IX.A.1.h and IX.A.1.i. As discussed in Section IX.C.1, the proposed combination of Sato and Eide would not alter Sato's semiconductor circuit assembly (including boundary scan controller). Accordingly, Sato, in view of Eide, renders obvious these elements. (Ex. 1002, ¶ 250.)

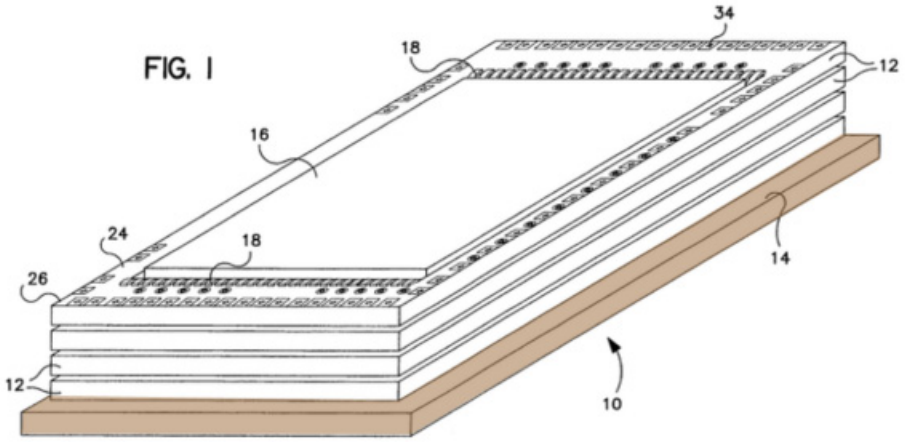
3. *Dependent Claim 16*

a. "The method of claim 12;"

See Section IX.C.2.

b. "adding to the plurality of modules a controller module that is disposed with an active pad;"

Sato, in view of Eide, renders obvious this element. Sato discloses adding to the plurality of modules a controller module that is disposed with an active pad. Section IX.A.2.b. Moreover, Eide teaches stacking memory modules on a **substrate 14**. (Ex. 1006, 4:38-39.)



(Ex. 1002, ¶ 252.) "[S]**ubstrate 14**, which has **conductive pads** on an upper surface thereof, is of conventional printed circuit board design." (Ex. 1006, 4:40-41.)

Substrate 14 is a controller module because it "electrically interacts with various chips in the chip stack" and controls the chip stack by sending a chip-enabling signal. (Ex. 1006, 4:43-44, 8:2-7; Ex. 1002 ¶ 254.) **Conductive pads 80, 82, 84,** and **86** are active pads because they carry active signals such as chip select signals CE 1-4. (*Id.,* 7:49-8:7, Fig. 12; Ex. 1002 ¶ 253.)

> c. "providing a ladder-like routing path that includes a connection between said active pad from said controller module and one of said passive ports by stacking said first memory module with said controller module."

Eide teaches "upper conductive pads 58 and the lower conductive pads 60 are coupled together in **stair step fashion**." (Ex. 1006, 7:20-24.) As illustrated in Figure 12, the **stair step routing path** connects **conductive pad 86**, which is formed on **substrate 14**, to **connecting via 54**. (Ex. 1006, 7:49-8:7.) As discussed above, **connecting via 54** is a passive port. Section IX.C.2.c.

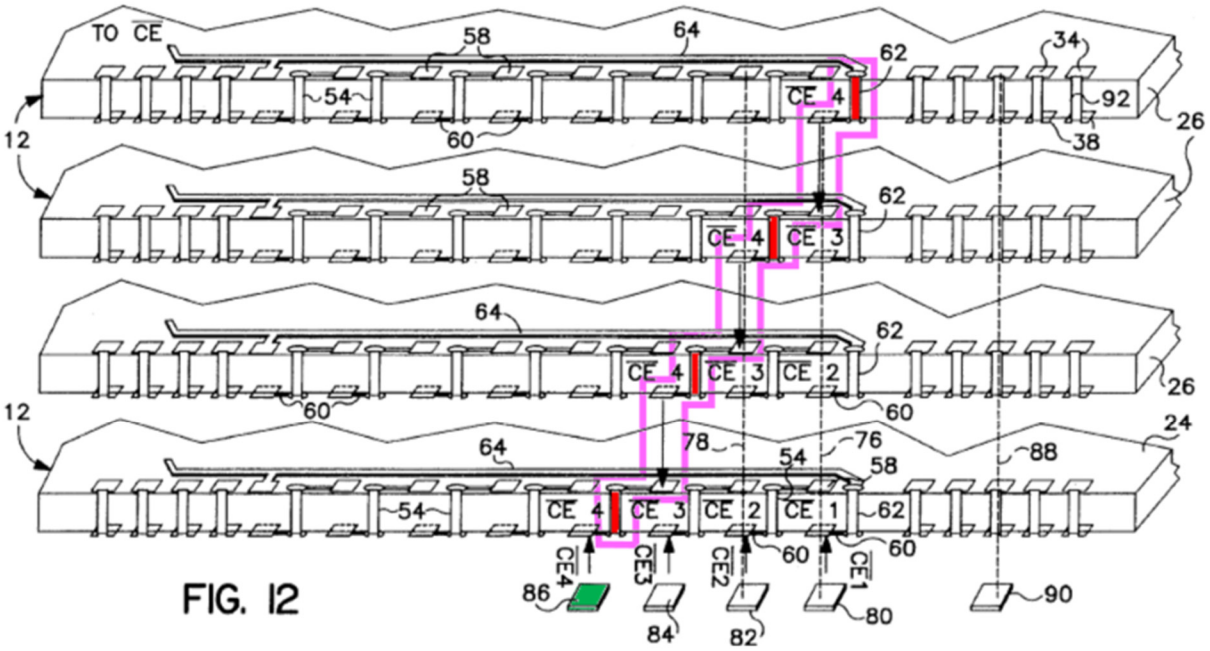


FIG. 12

(Ex. 1002, ¶ 256.)

D. Ground 4: Claims 12 and 16 Are Obvious Over Sung in View of Funaba

1. *Independent Claim 12*

a. "12. A method for stacking a plurality of modules, said plurality of modules including a first memory module and a second memory module; said first memory module having a first surface and a second surface; said second memory module having a third surface and a fourth surface; said method comprising"

Sung, in view of Funaba, renders obvious this element. Sung discloses and claims "methods and circuits" for constructing "three-dimensional integrated circuit systems" that include "layers" of "stacked multi-chip modules." (Ex. 1007, Abstract, [0005], [0029], [0043], [0050], [0052], [0053], cl. 1; Ex. 1002, ¶¶ 74-82,

258-280.) Sung's "three-dimensional stack" applies to "stacks of dies" as well as "stacked multi-chip modules." (Ex. 1007, [0025], [0052].)

Further, Sung discloses that the stacked modules consist of first and second memory modules. (Ex. 1007, Abstract; Ex. 1002, ¶¶ 74-82, 258-280.) Sung explains that "stacking has the potential to increase processing power, chip integration, operating speed and ***data storage density***." (Ex. 1007, [0006], [0042]). A POSITA would have therefore understood that Sung discloses multiple, *i.e.*, first and second, memory modules. (Ex. 1007, [0040], [0052]; Ex. 1002, ¶¶ 74-82, 258-280.)

In addition, it would have been obvious to a POSITA at the time of invention reviewing Sung and its method of three-dimensional stacking to stack a plurality of memory modules in view of Funaba. (Ex. 1002, ¶¶ 74-89, 258-280.) Sung explains that one type of "three-dimensional stack" uses layers of stacked "memory cells," and explains that its methods for stacking identical dies "can be applied to[] stacked multi-chip modules," among other structures. (Ex. 1007, [0005], [0052].) Further, Sung criticized prior art stacked memory because those designs "require[ed] at least two sets of layout masks." (Ex. 1007, [0005].) Funaba also provides a single layout solution, and discloses using "stacked semiconductor chips [that] are identical in design" to create "stacked memories." (Ex. 1008, [0030], [0158].) A POSITA reviewing Sung, in view of Funaba, would have therefore found it obvious to apply Sung's stacking teachings to memory modules. (Ex. 1002, ¶¶ 74-89, 258-280.)

A POSITA would have been further motivated to apply Sung's stacking methods to memory as taught by Funaba to take advantage of stacking's "potential to increase processing power, chip integration, operating speed, and data storage density in the same planar area," while "incurring no extra design effort." (Ex. 1007, [0006], [0025]; Ex. 1002, ¶¶ 258-280.) Because Sung and Funaba describe different aspects of a stacked integrated circuit system, a POSITA at the time would have been motivated to combine the teachings of Sung and Funaba to supplement the teachings of each. (Ex. 1002, ¶¶ 258-280.)

A POSITA reviewing the disclosures of Sung and Funaba would have understood the references to be directed to the same field of endeavor and for their teachings to be compatible. (Ex. 1002, ¶¶ 258-280.) For example, both references disclose stacked semiconductor devices in which each layer of the stack is identical. (*See* Ex. 1007, [0036]; Ex. 1008, [0060]; Ex. 1002, ¶¶ 74-89, 258-280.) In both, when a layer is stacked to another, their vias connect to create a serial bus connection. (Ex. 1007, [0047]; Ex. 1008, [0099]; Ex. 1002, ¶¶ 74-89, 258-280.) The two references use these buses for similar purposes, including, for example, providing external chip select signals to each layer of the stack to perform die addressing. (Ex. 1007, [0048]; Ex. 1008 [0034].) Moreover, both references are applicable to stacked modules. (Ex. 1007, [0052]; Ex. 1008, [0263]; Ex. 1002, ¶¶ 74-89, 258-280.) Accordingly, a POSITA would have had a reasonable

expectation of success in combining Sung and Funaba to stack memory modules. (Ex. 1002, ¶¶ 258-280.)

To the extent the Patent Owner argues the memory module must be a synchronous DRAM (SDRAM) module, Sung in view of Funaba renders that obvious. Funaba discloses DRAM, but does not explicitly say the DRAM is synchronous. (Ex. 1008, [0004]-[0011].) For the reasons described in Section IX.A.1.a, a POSITA would have understood the term DRAM used by Funaba would include SDRAM, and it would have been obvious to a POSITA to use SDRAM. (Ex. 1002, ¶¶ 74-89, 91-101, 258-280.)

Additionally, Figure 3 of Sung shows that each layer in the stack has at least a top and bottom surface. (Ex. 1002, ¶¶ 74-82, 258-280.)

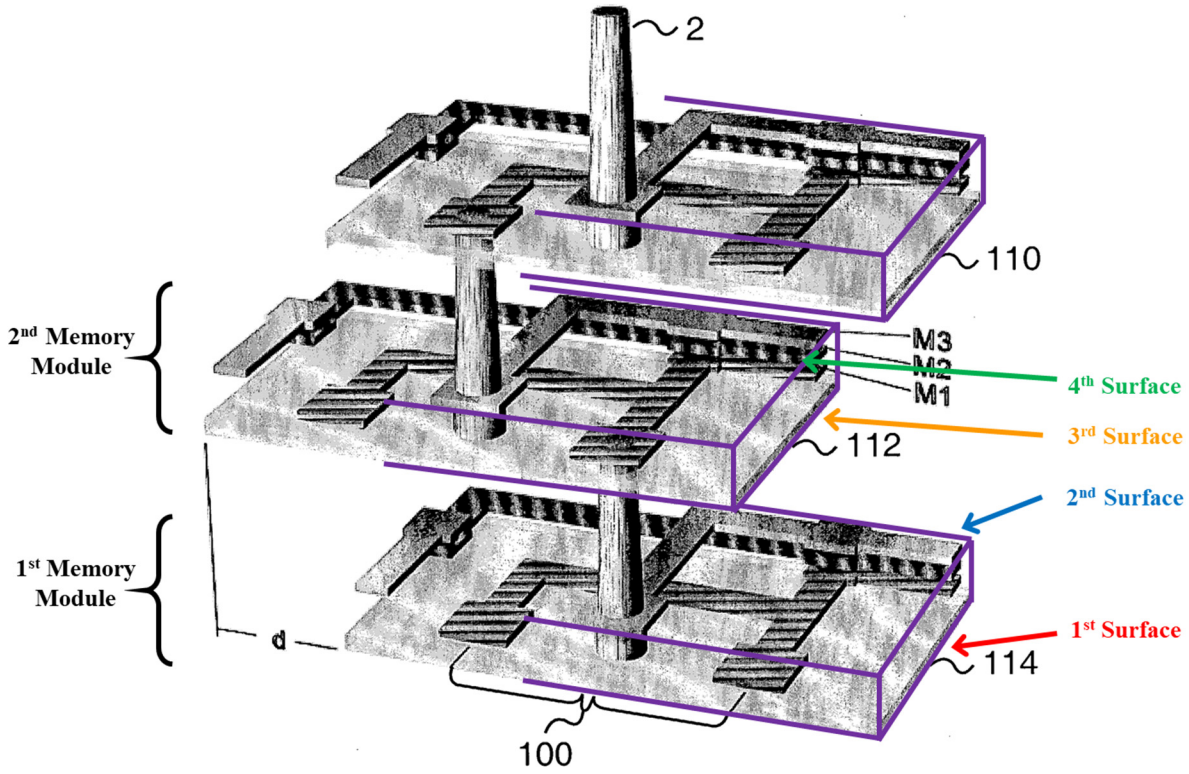


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.) Accordingly, the first and second memory modules disclosed by Sung also each have surfaces, including first and second surfaces on a first memory module and third and fourth surfaces on a second memory module. (Ex. 1002, ¶¶ 258-280.)

b. "forming one or more active ports on the first and second memory modules, said one or more active ports for carrying one or more active signals;"

Sung, in view of Funaba, renders obvious this element. Sung discloses forming one or more active ports on each stacked memory module, such as the pads of **conditional connection 104**. Sung explains that **conditional connection 104**

connects the vertical conductor 2 and terminators 4 to "implement[] various inter-die communication networks." (Ex. 1007, [0044]; Ex. 1002, ¶¶ 281-289.)

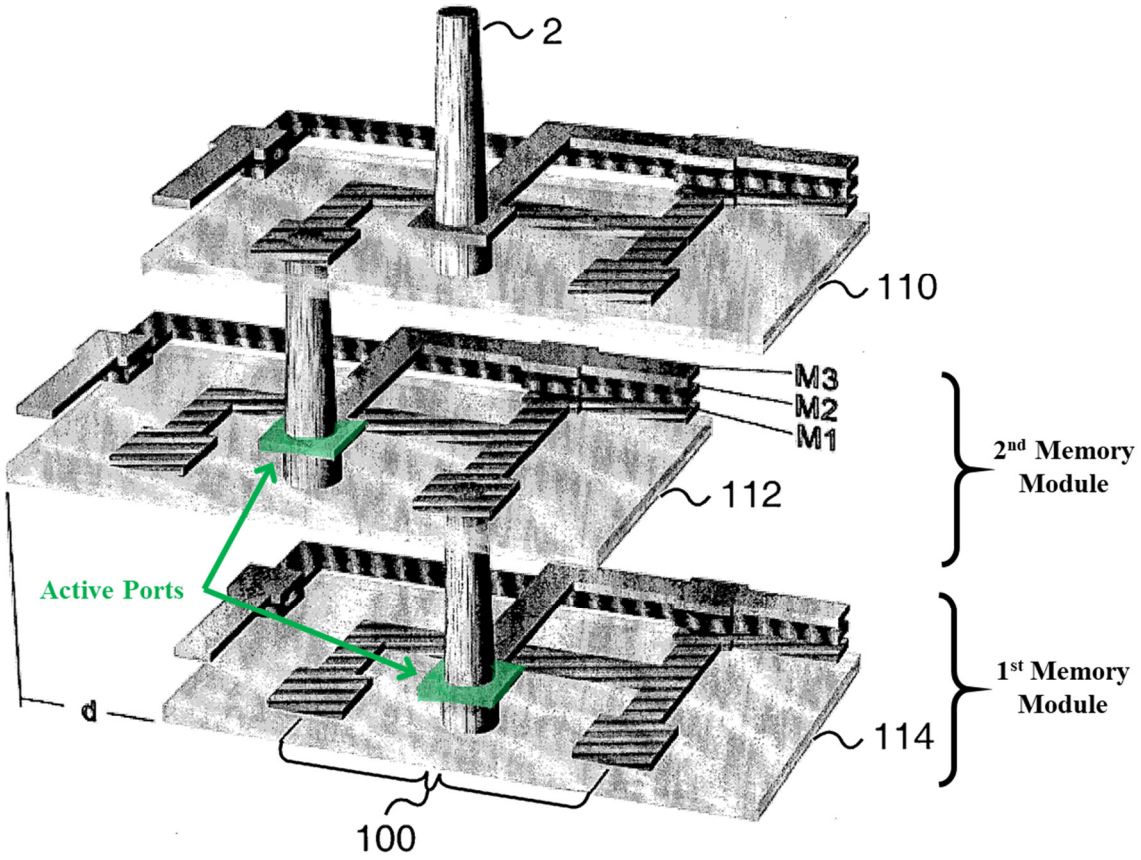


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.) A POSITA would have understood that the **square-shaped portion of conditional connection 104** surrounding vertical conductor 2 is a contact pad made from conductive material. (Ex. 1002, ¶¶ 281-289.)

Conditional connection 104, which is present in each layer of the stack, is an active port because it is an electrical connection that broadcasts active signals, such as addr_in. (Ex. 1007, [0044], [0047]; Ex. 1002, ¶¶ 281-289.) The addr_in signal

is an active signal because it is used for the "selection of [a] specific module" in the stack, just like the signals of the '103 patent's technique. (Ex. 1001, 8:66-9-1; Ex. 1007, [0048]; Ex. 1002, ¶¶ 281-289.)

c. "forming one or more passive ports on the first and second memory modules, said one or more passive ports for passing through said one or more active signals on the first and second memory modules;"

Sung, in view of Funaba, renders obvious this element. In particular, Sung discloses forming on each module passive ports—**through vias**—that pass through the active signals from one surface of a memory module to the other. (Ex. 1002, ¶¶ 290-301.)

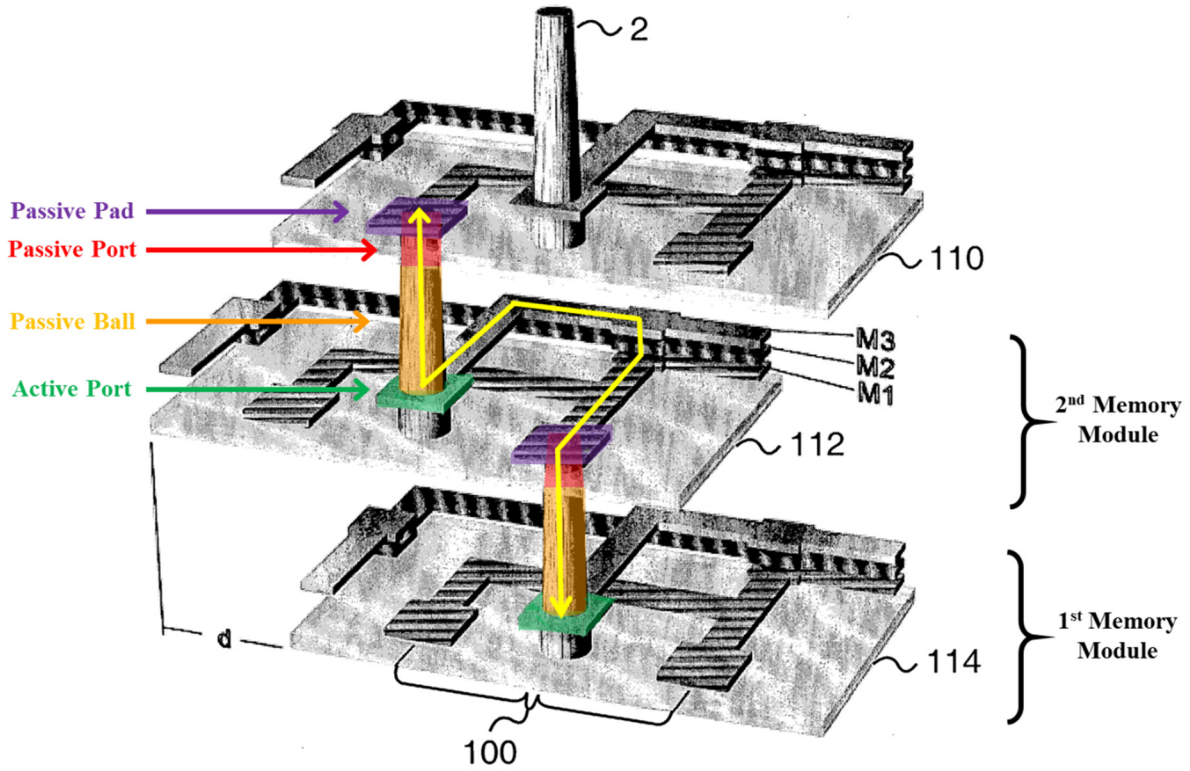


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

Sung discloses that a vertical conductor passes **"through the thickness of a substrate"** to couple with **terminator 4**, which is on the other surface of the module. (Ex. 1007, [0043], cls. 6-37; Ex. 1002, ¶¶ 290-301.) A POSITA would have understood that the portions of the vertical conductor that pass through the substrate are the "**through vias** formed through apertures" claimed by Sung. (Ex. 1007, cl. 15; Ex. 1002, ¶¶ 290-301.) In particular, Sung discloses that a "connector 100 with [a] vertical conductor 2," which includes the **through via**, "coupled 104 to its **terminators 4** will implement broadcasting" by passing through an active signal from a preceding layer to a next layer in the stack. (Ex. 1007, [0047], [0048], Figs. 3, 6, 9; Ex. 1002, ¶¶ 290-301.)

Further, Sung explains that vertical conductors are "solder mounds," which is another word for solder ball. (Ex. 1007, cls. 11-12; Ex. 1002, ¶¶ 290-301.) Accordingly, a POSITA would have understood that the **portion of the vertical conductor** that is not formed within the aperture in the substrate is a passive ball. (Ex. 1002, ¶¶ 290-301.) Likewise, Sung discloses that the **terminators** are "**3D via pads**," and so a POSITA would have understood that Sung's **through via** forms a connection between a passive **solder mound** on one surface of the module and a passive **3D via pad** on another surface of the memory module. (Ex. 1007, [0029]; [0030]; Claim 36; Ex. 1002, ¶¶ 290-301.)

Moreover, the structure of Sung's **through via** is analogous to the '103 patent's example structure of a passive port. (Ex. 1002, ¶¶ 290-301.) The '103 patent explains that "the connection between a passive ball on one surface of a SDRAM module and a passive pad on another surface of the same SDRAM module [...] is named 'passive port.'" (Ex. 1001, 9:19-24.) This connection, i.e., the **through via**, has the same structure as the passive port of the '103 patent. (Ex. 1002, ¶¶ 290-301.) And, as described in the previous section, it would have been obvious to use SDRAM for Sung's memory modules.

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not passive ports, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. For instance, the portion of the **conditional connection** shown in red below is a passive port that passes an active signal from the **vertical conductor solder mound** through the substrate to the **3D via pad** on the other side. (Ex. 1007, [0030], [0043], [0044], [0047], [0048], Claims 15, 37; Ex. 1002, ¶¶ 290-301.) While Figure 3 shows the **terminators** on the same side of the module substrate as the **vertical conductors**, it would have been obvious to a POSITA in view of Sung to locate the **terminators** on an opposite side of the modules from the **vertical conductors**. (Ex. 1007, [0003], Claims 8, 18, 35; Ex. 1002, ¶¶ 290-301.)

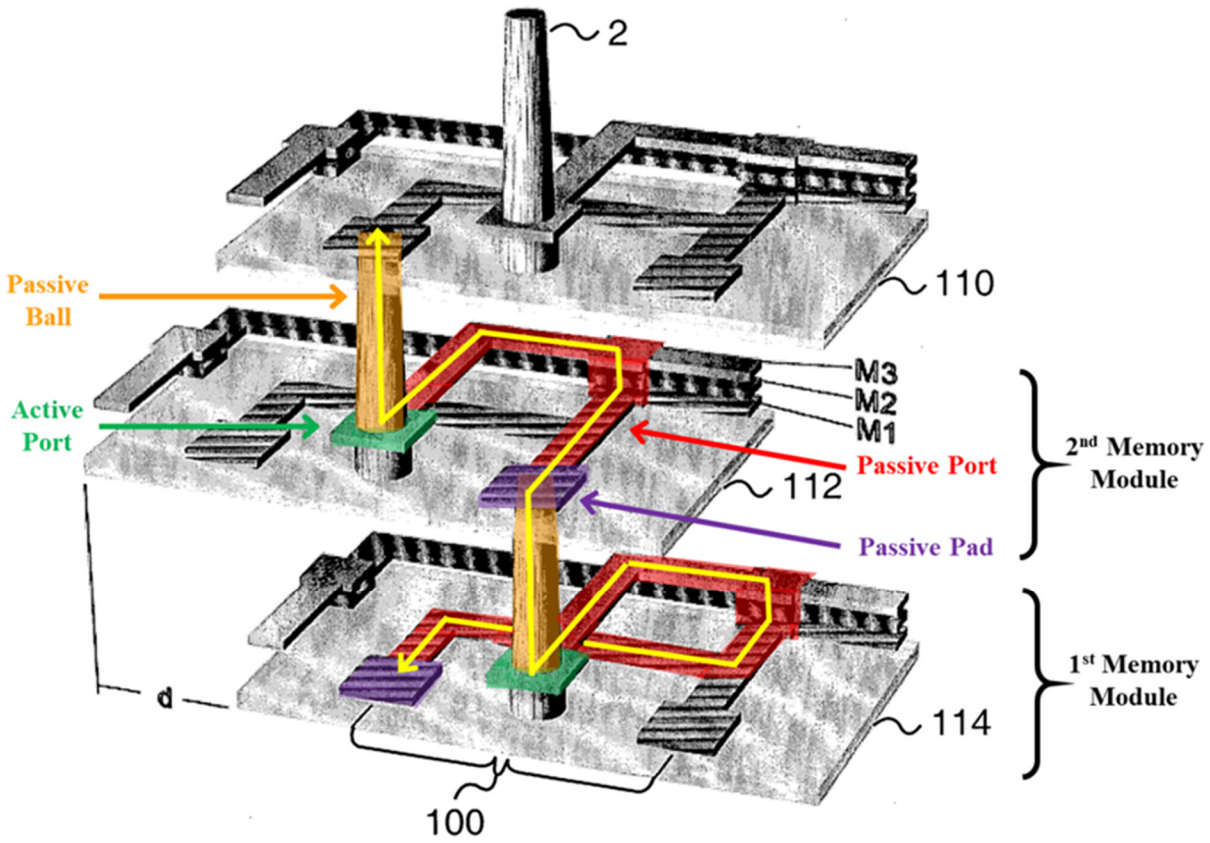


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

d. "coupling one of said active ports formed on said first memory module to one of said passive ports formed on said second memory module by stacking said first memory module to said second memory module;"

Sung, in view of Funaba, renders obvious this element. As discussed in Sections IX.D.1.b-c, Sung discloses i) a **conditional connection 104** and ii) a **through via** formed from the portions of the vertical conductors extending "through the thickness of [a] substrate."

Sung explains that the vertical conductors in each module in the stack are "aligned" so as to connect with a **terminator** on another module. (Ex. 1007, [0025],

[0029], [0044], [0050]; Ex. 1002, ¶¶ 302-308.) A POSITA would have understood, as shown in Figure 3, that stacking the modules and aligning the vertical conductors of each layer would involve coupling the **conditional connection 104** on one layer to a **through via** formed from the portions of the vertical conductors extending "through the thickness of [a] substrate" on another layer (Ex. 1007, [0040], [0044]; Ex. 1002, ¶¶ 302-308.)

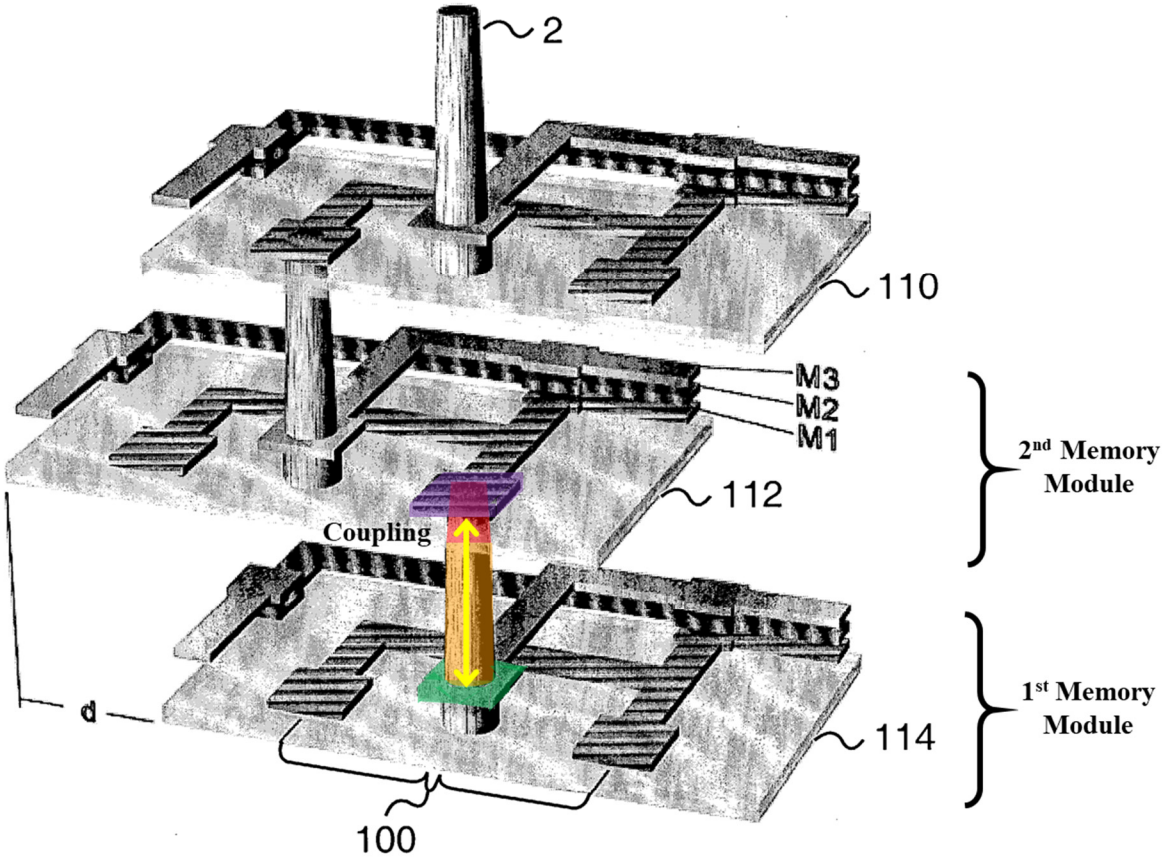


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not passive ports, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. As explained in the previous section, the portion of the **conditional connection** shown in red below is a passive port that passes an active signal from the **vertical conductor solder mound** through the substrate to the **3D via pad** on the other side. A **conditional connection** on one module is coupled with **conditional connection** on another module in the stack, as discussed at Section IX.D.1.c. (Ex. 1002, ¶¶ 302-308.)

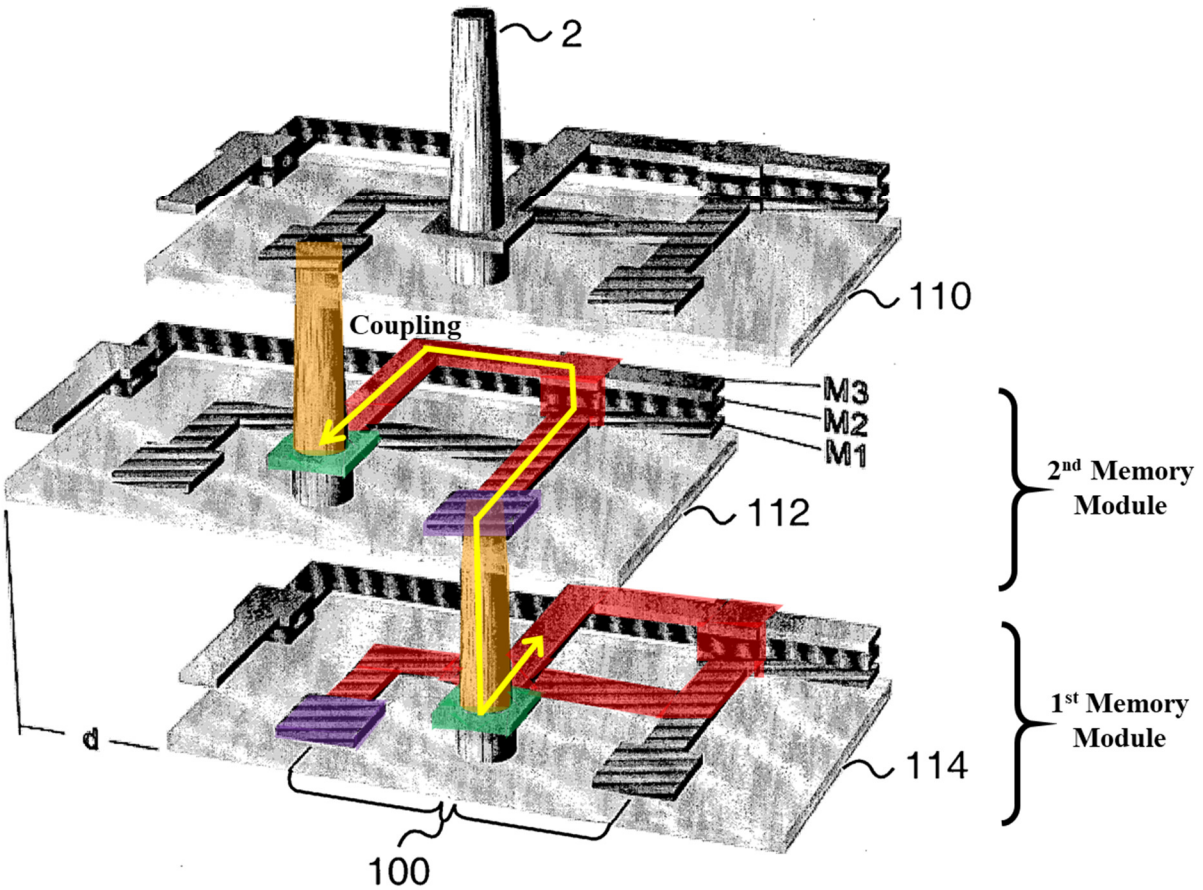


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

e. "forming a first serial chain route that includes at least one serial chain connection, said serial chain connection including: a serial chain circuit, a serial chain input, and serial chain output;"

Sung, in view of Funaba, renders obvious this element. Sung discloses methods for forming a first serial chain route that includes multiple serial chain connections connected in series. (Ex. 1007, [0029], [0050]; Ex. 1002, ¶¶ 309-322.) Specifically, Sung describes an **inter-die scan chain** that accomplishes "communication between multiple dies." (*Id.*, [0049].) For example, Figure 10 of Sung depicts an "**inter-die scan chain 290** across three dies 110, 112, and 114," although the **inter-die scan chain** could extend across any number of layers. (Ex. 1007, [0049].)

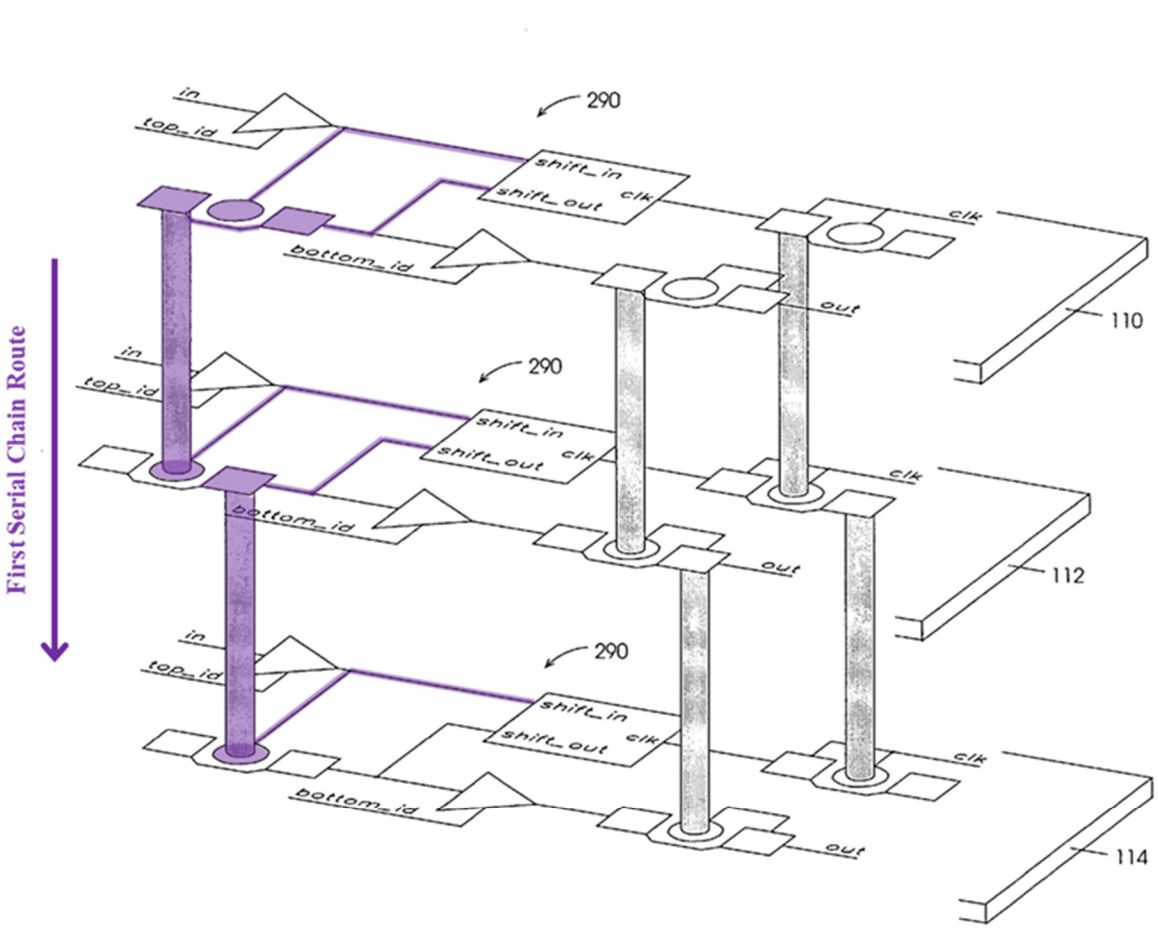


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Fig. 10.)

Serial chain connections (**connectors 100**) are serially connected to form the **inter-die scan chain 290**. (Ex. 1002, ¶¶ 309-322.) Sung explains that the input of each module (shift_in) is coupled to an output (shift_out) through a register. The output is "coupled to the die below 112 through a **connector 100**." (Ex. 1007, [0049].) This coupling pattern is repeated until the bottom module is reached. (*Id.*)

Sung's **connectors 100** each include a serial chain circuit, serial chain input, and serial chain output. (Ex. 1002, ¶¶ 309-322.)

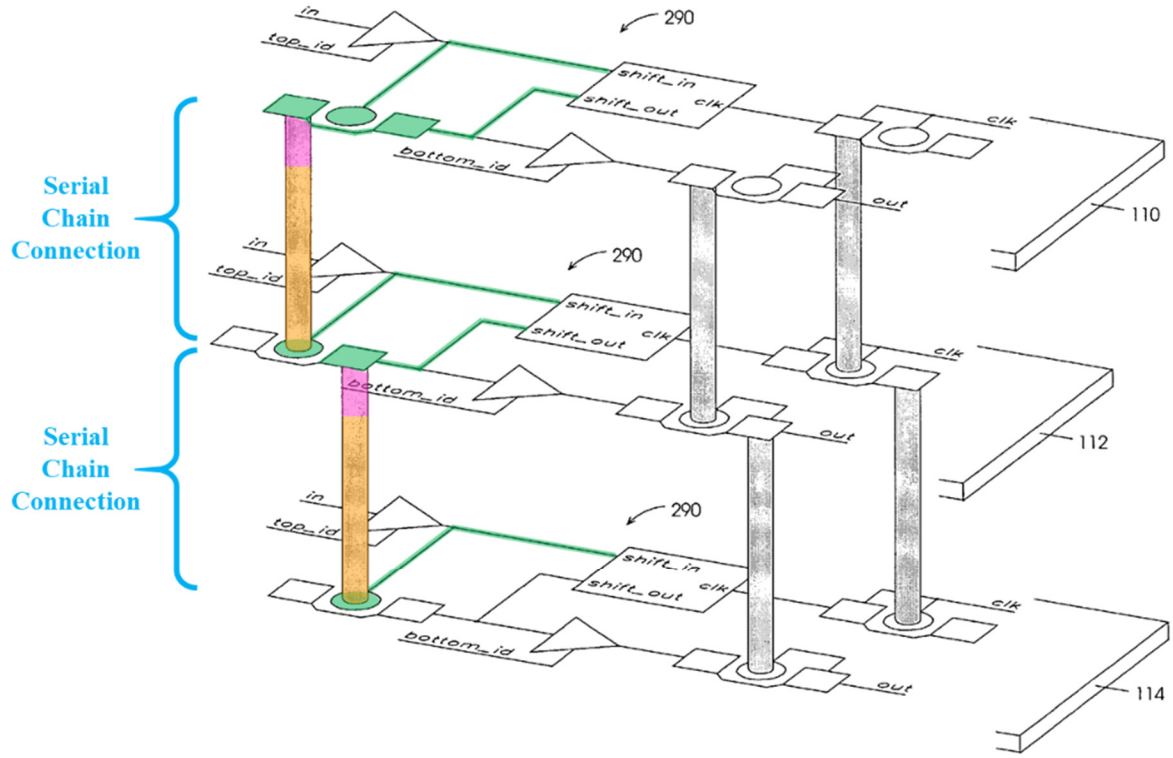


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Fig. 10.) **Connector 100** has a "vertical conductor 2 coupled [] to its **terminators**." (Ex. 1007, Fig. 10.) As discussed in Sections IX.D.1.c, Sung's vertical conductors 2 each include two portions i) a **ball** and ii) a **through via** (or passive port) that "extend[s] through the thickness of a substrate," which is connected to **terminator 4**. When a signal travels down the stack, **ball portions** of the vertical conductors 2 receive a signal from the module above, and **terminator 4**

pads provide the signal to the module below. (Ex. 1007, [0049]; Ex. 1002, ¶¶ 309-322.) This is analogous to the '103 patent's system, where the "serial chain input is disposed to receive a signal" and a "serial chain output is disposed to provide the signal." (Ex. 1001, 10:58-61; Ex. 1002, ¶¶ 309-322.) Like Sung, the '103 patent's "serial chain input" and "serial chain output" can be in the form of "balls and pads" that are connected by a "serial chain circuit" to form the serial chain connection. (Ex. 1001, 10:45-11:9.)

Moreover, Sung's **through vias** that "extend through the thickness of a substrate" of the modules are serial chain circuits, because, like the serial chain circuits of the '103 patent, each "functions as a passive port" to create a "signal route" that "coupl[es] a ball and pad." (Ex. 1007, [0044]; Ex. 1001, 10:45-49, 11:3-4; Ex. 1002, ¶¶ 309-322.)

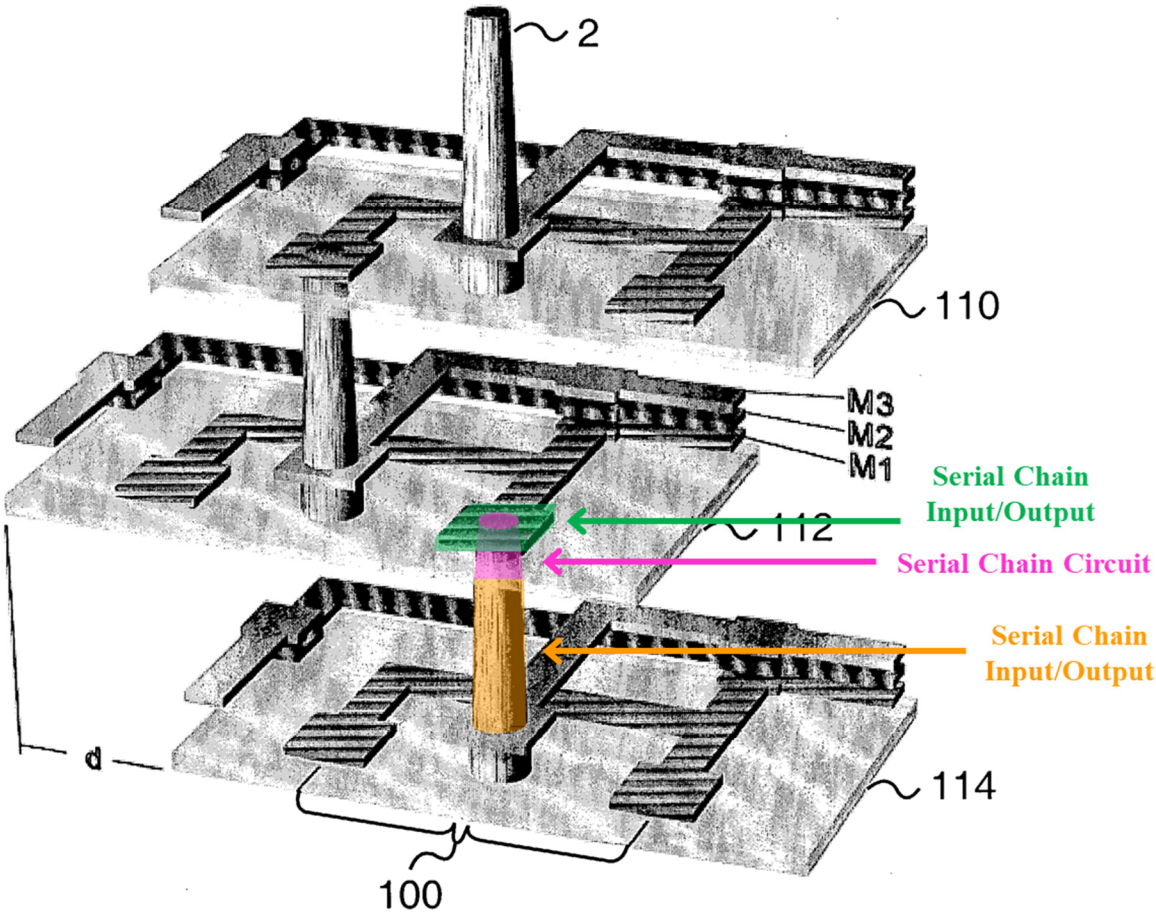


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not serial chain circuits, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. For instance, additional serial chain connections are shown in the below figures, where the active signal transmitted through the stack is received at each module by the **vertical conductor solder mound**, and passed through the **conditional connection** to the **terminator**

pad where it is output to the next module in the stack. (Ex. 1007, [0044], [0046], [0047], [0049]; Ex. 1002, ¶¶ 309-322.)

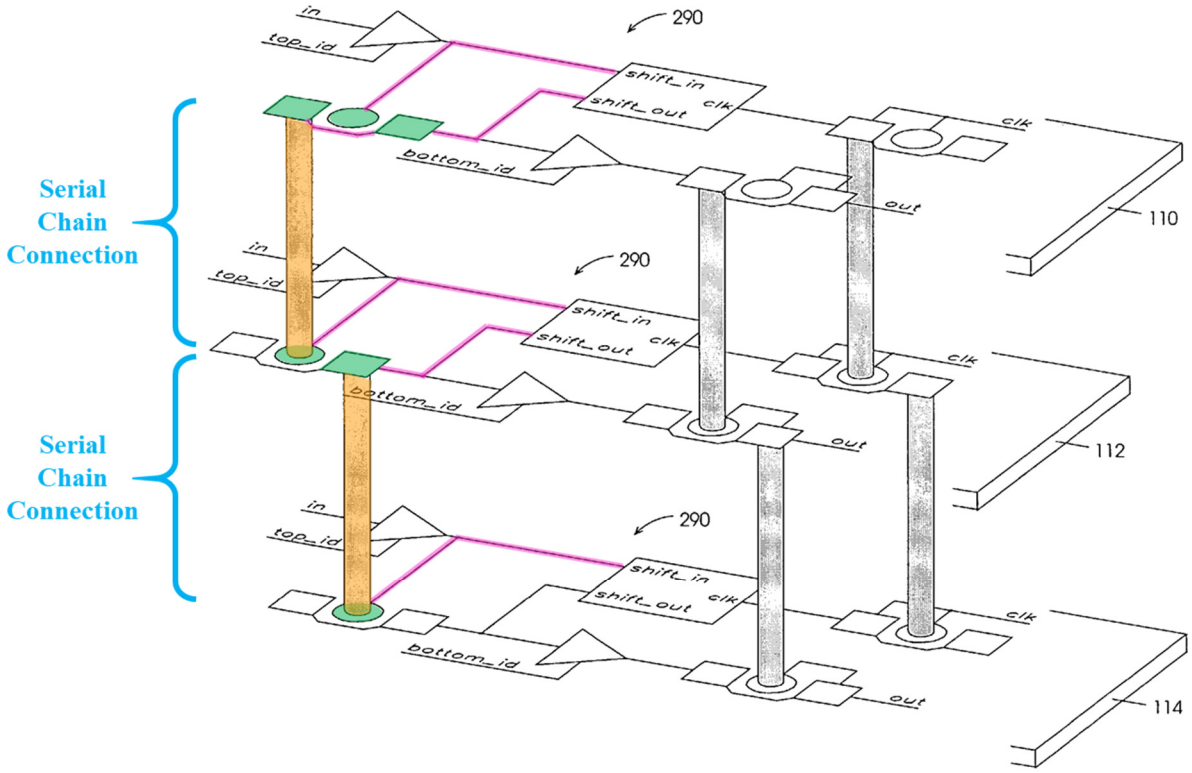


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Fig. 10.)

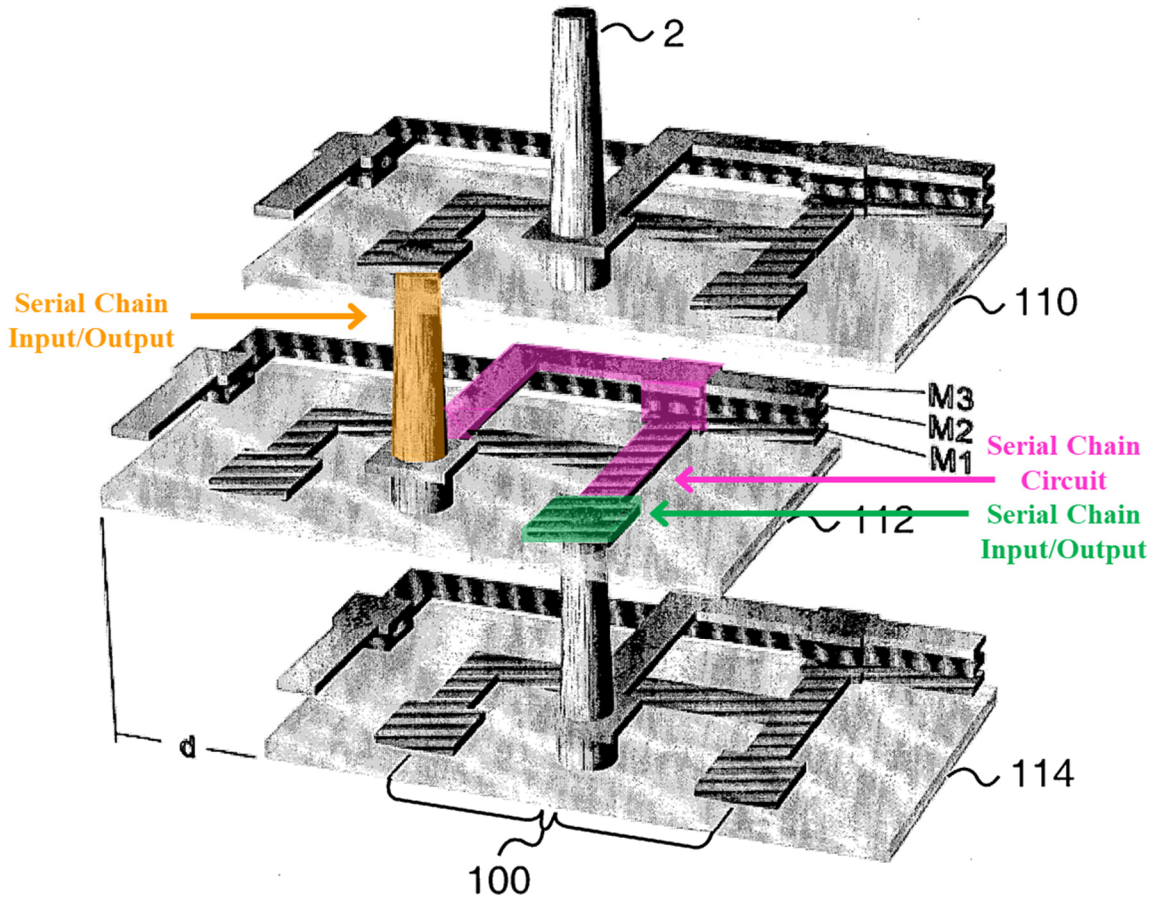


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

f. "coupling said serial chain input with said serial chain output through said serial chain circuit;"

Sung, in view of Funaba, renders obvious this element. As explained in Section IX.D.1.e, Sung's vertical conductor **ball portions** are serial chain inputs that are disposed to receive a signal, and the **terminator 4 pads** are serial chain outputs that are disposed to receive a signal. (Ex. 1007, [0044]; Ex. 1002, ¶¶ 323-329.) Sung also discloses serial chain circuits—the **through vias** formed from the portions of

the vertical conductors that extend through the substrates of the modules. (Ex. 1007, [0044], cl. 37; Ex. 1002, ¶¶ 323-329.)

Sung's "**terminator *electrically couples*** to the vertical conductors on an adjacent layer," which causes a **through via** formed from the portion of the vertical conductor to couple the **terminator** pad to the **ball portion**. (Ex. 1007, [0029], [0044], [0050], cl. 26; Ex. 1002, ¶¶ 323-329.)

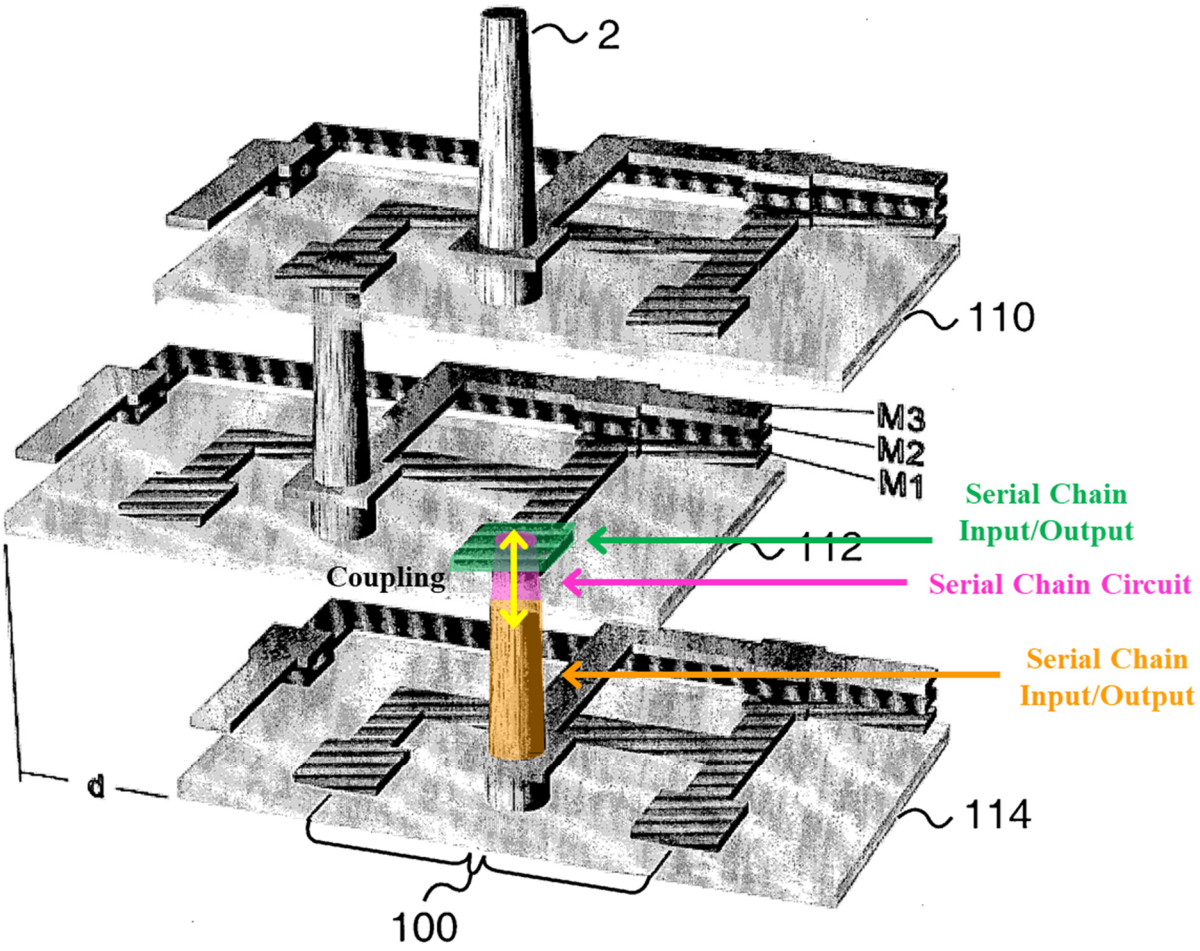


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not serial chain circuits, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. For instance, each **conditional connection** couples a **terminator pad** and a **vertical conductor** and is thus also a serial chain circuit. (Ex. 1007, [0044]; Ex. 1002, ¶¶ 323-329.)

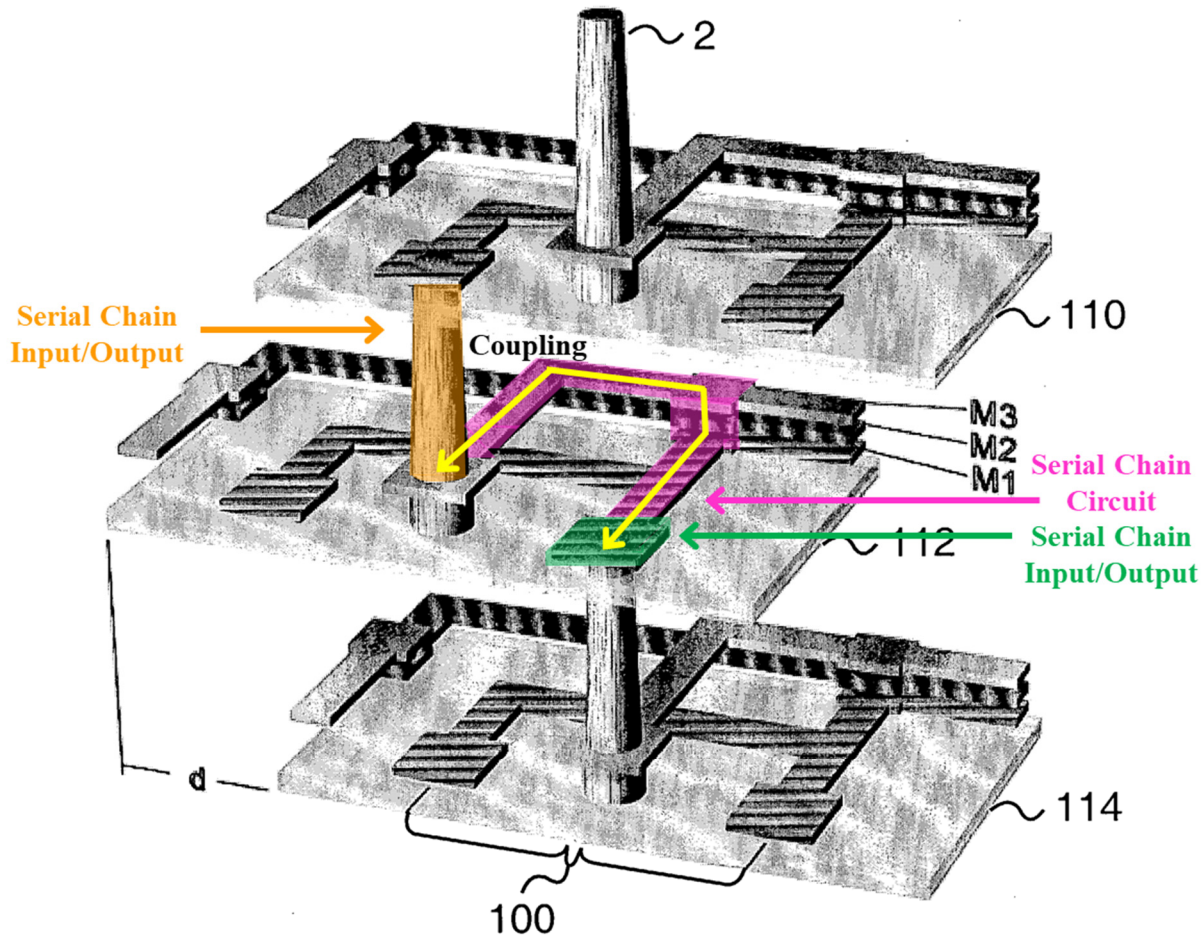


Figure 3: Staggered die offset alignment and die broadcast using die connectors.

(Ex. 1007, Fig. 3.)

g. "forming a second serial chain route;"

Sung, in view of Funaba, renders obvious this element. As explained above in Section IX.D.1.e, Sung's modules form serial chain connections (**connectors 100**) when coupled. (Ex. 1007, [0044], cls. 36-37, 39.) Those serial chain connections further form a second serial chain route—**broadcasting circuit 250**. (Ex. 1002, ¶¶ 330-337.)

Specifically, Sung discloses a **broadcasting circuit 250** that "conveys the data" in the bottom module "to the top of the stack." (*Id.*, [0049].) A POSITA would have understood that the **broadcasting circuit** depicted at Figure 10 is a second serial chain route formed by other serially connected **connectors 100**. (Ex. 1007, [0049]; Ex. 1002, ¶¶ 330-337.)

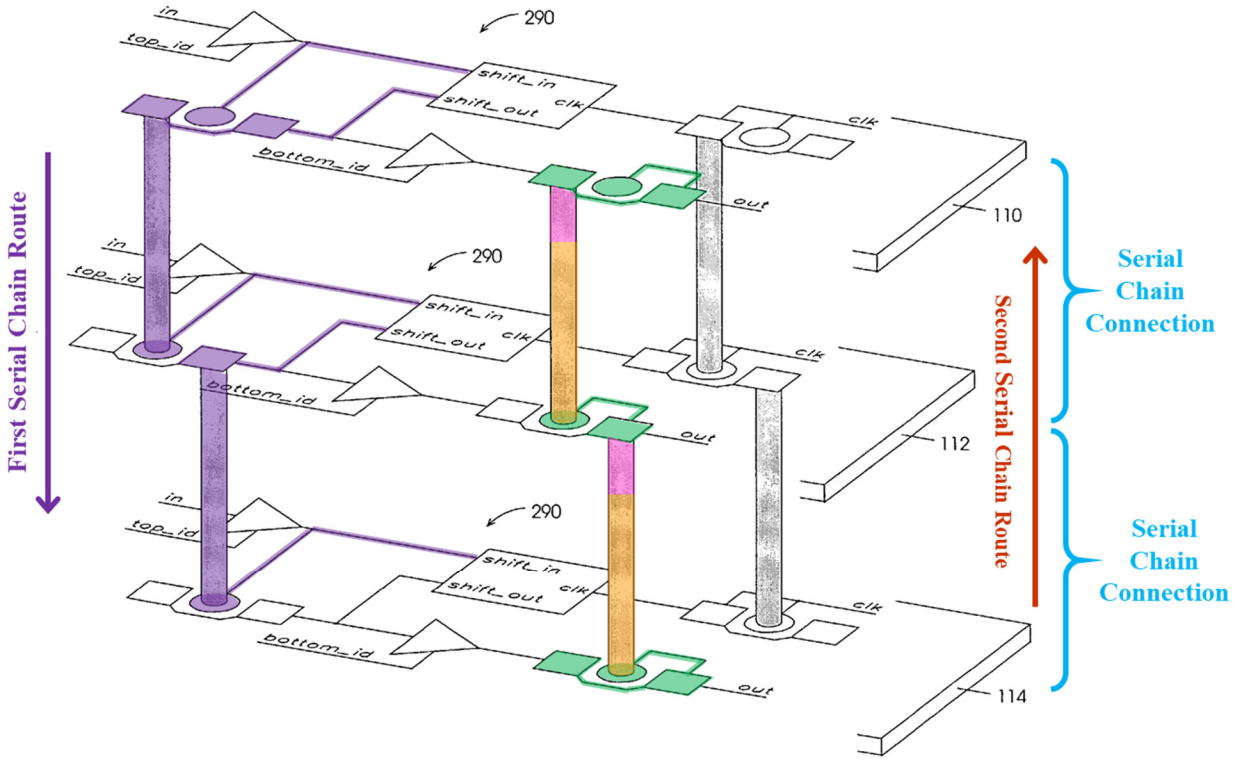


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Fig. 10.)

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not a serial chain circuit, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. For instance, the **conditional connections** coupling the **terminator pads** and **vertical conductors** of Sung are also serial chain circuits, such that the connectors of Sung's **broadcasting circuit** form a second serial chain route. (Ex. 1007, [0044]; Ex. 1002, ¶¶ 330-337.)

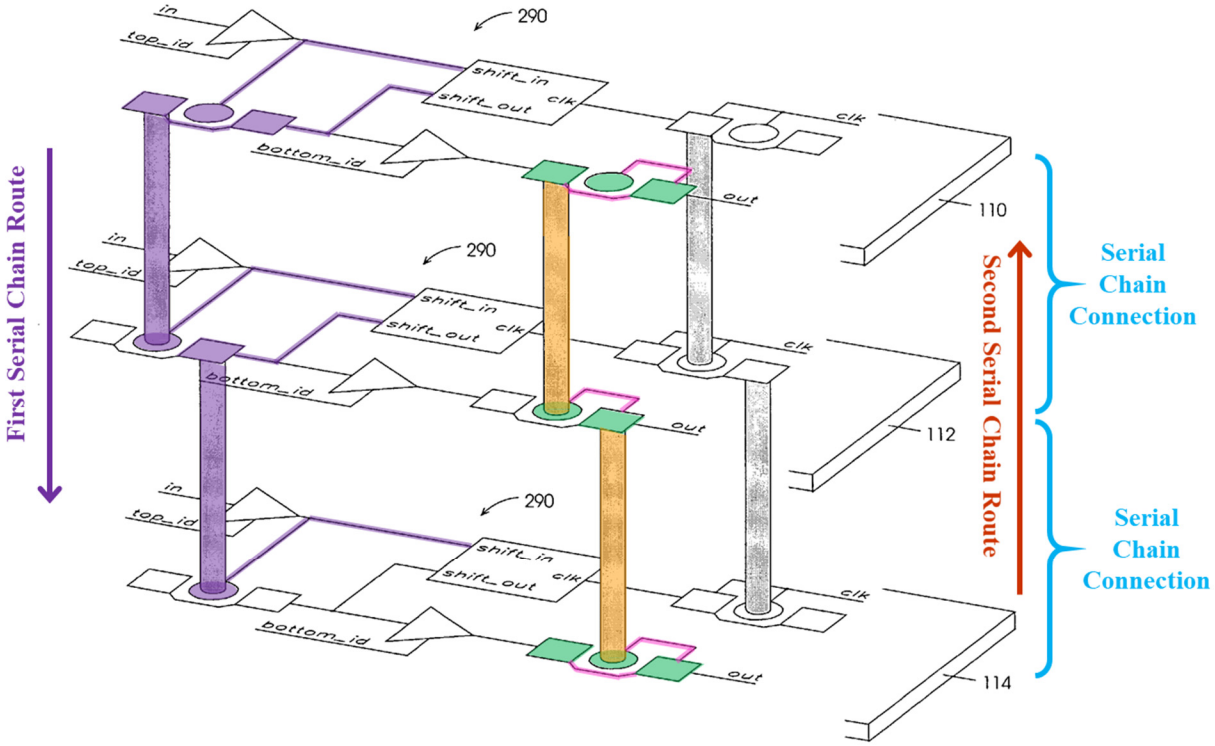


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Fig. 3.)

h. "forming a control circuit for enabling a routing path that connects said first serial chain route with said second serial chain route within an end module;"

Sung, in view of Funaba, renders obvious this element. Sung discloses methods for forming a control circuit (**die identifier circuit 230** and **tristate buffer 296**) for enabling the claimed routing path. (Ex. 1007, [0029], [0050]; Ex. 1002, ¶ 338-346.) A "bottom_id" signal is generated at the **die identifier circuit** in the bottom module. (Ex. 1007, [0046]; Ex. 1002, ¶¶ 338-346.) The bottom layer is an end module in the stack since no others are stacked below it. (Ex. 1002, ¶¶ 338-

346.) When "bottom_id" is asserted, it enables the **routing path** so that the input signal that passes through the **inter-die scan chain** is "coupled by [the] **tristate buffer 296** to a **broadcasting circuit 250** that conveys the data to the top of the stack 110." (Ex. 1007, [0049]; Ex. 1002, ¶¶ 338-346.) Thus, the **die identifier circuit** and **tristate buffer** in the bottom die enables a routing path between the first serial chain route and the second serial chain route. (Ex. 1007, [0049]; Ex. 1002, ¶¶ 338-346.)

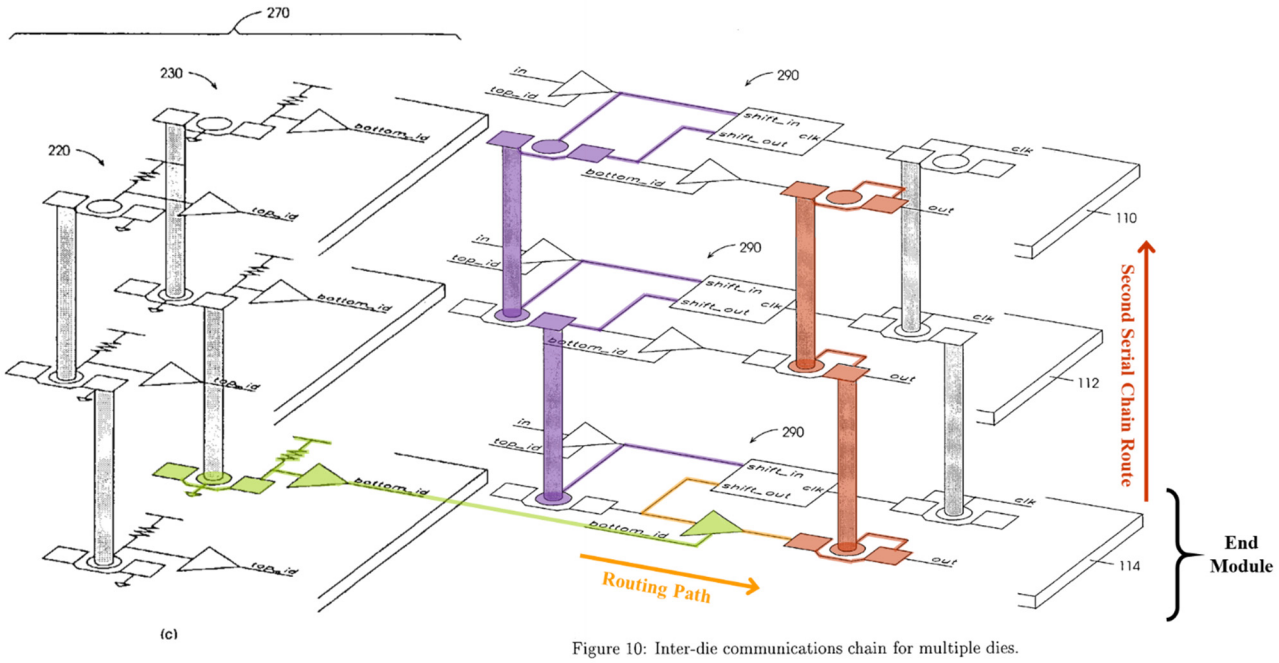


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Figs. 6, 10.)

Alternatively, to the extent that Patent Owner argues that the claimed "end module" is a module other than the top or bottom module in the stack and that a routing path can span multiple modules, Sung, in view of Funaba, nevertheless

renders obvious this element in additional ways. For instance, under such a construction, when "bottom_id" in the module 112 is not asserted, the **tristate buffer 296** in module 112 enables a **routing path** within the modules 112 and 114 so that the input signal passed through the **inter-die scan chain** is coupled to the **broadcasting circuit**. (Ex. 1007, [0049].)

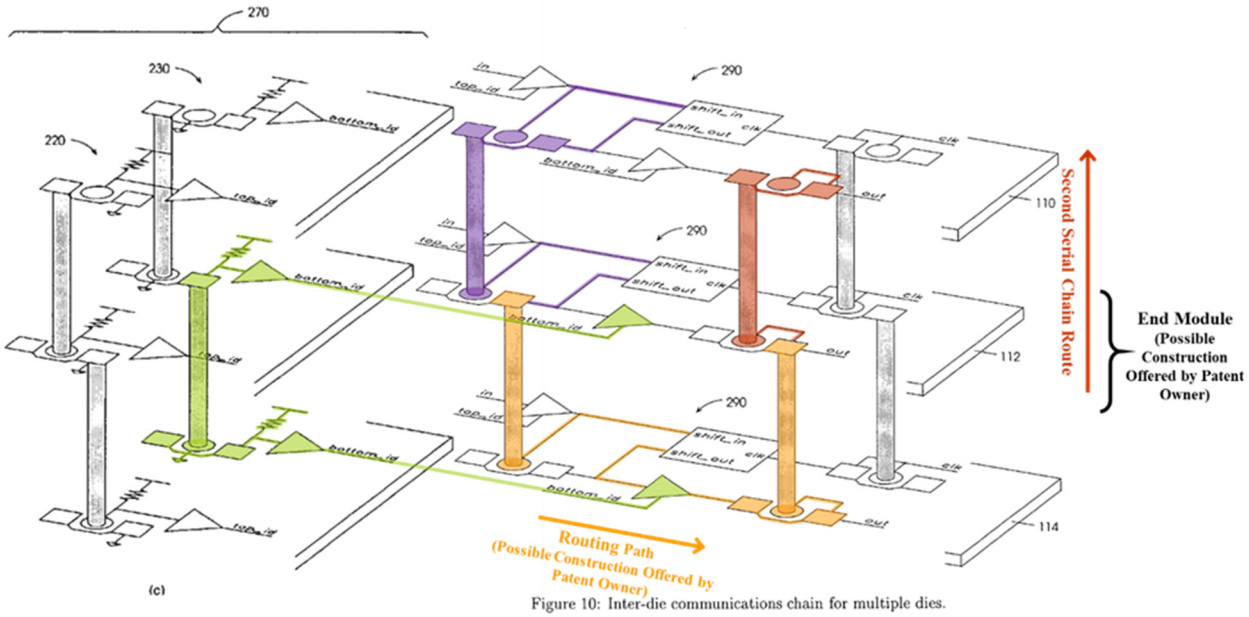


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Figs. 6, 10.) Under this construction, the first and second serial chain routes would not include the connectors in bottom module 114, but would include the connectors in modules 112 and 110, as well as the connectors forming the **interdie scan chain** and **broadcasting circuit** in additional modules stacked above module 110 that are not shown in Figure 3.

i. "said control circuit is disposed to enable said routing path in response to a control input signal received from another module from the plurality of modules when said end module is coupled to said another module."

Sung, in view of Funaba, renders obvious this element. As discussed in the previous section, Sung discloses a control circuit (**die identifier circuit 230** and **tristate buffer 296**) that enables a routing path connecting first and second serial chain routes in an end module. (Ex. 1007, [0046], [0049]; Ex. 1002, ¶¶ 347-357.) The control circuit is disposed to enable the routing path in response to a control input signal received from another module when the end module is coupled to the other module. (Ex. 1002, ¶¶ 347-357.)

Sung's "**tristate buffer 296**" has a **control line** that tri-states the input when pulled low to disable a routing path between the first and second serial chain routes, and to enable the routing path when pulled high. (Ex. 1001, 11:10-37; Ex. 1007, [0049]; Ex. 1002, ¶¶ 347-357.) When one of Sung's dies has another die stacked below it, the "bottom_id" signal output by its **bottom die self-identifier circuit** is **grounded** to disable the **tristate buffer 296**, just as the '103 patent's connection of the "StkLow" ball to **ground** disables the path "2120." (Ex. 1007, [0046], [0049]; Ex. 1002, ¶¶ 347-357.)

However, the **bottom die self-identifier circuit** in a bottom die does not receive this **ground signal**, and therefore its "bottom_id" signal is pulled high by a **voltage bias** from a weak pull-up device to enable the routing path through the

tristate buffer 296, just like in the '103 patent's configuration. (Ex. 1001, 11:10-37; Ex. 1007, [0049]; Ex. 1002, ¶¶ 347-357.) A POSITA would have understood that the **voltage bias** is provided to each layer of the stack using a bus, such as broadcasting circuit 250, such that the **voltage bias** is received from another module. (Ex. 1002, ¶¶ 347-357.)

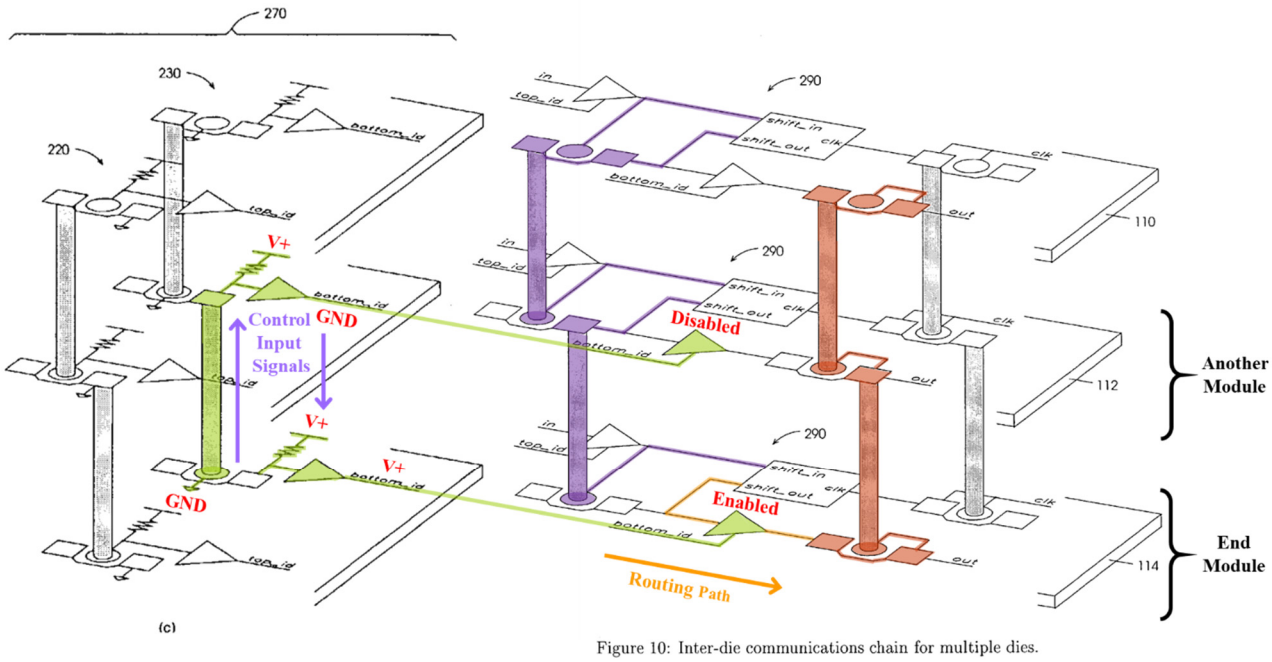


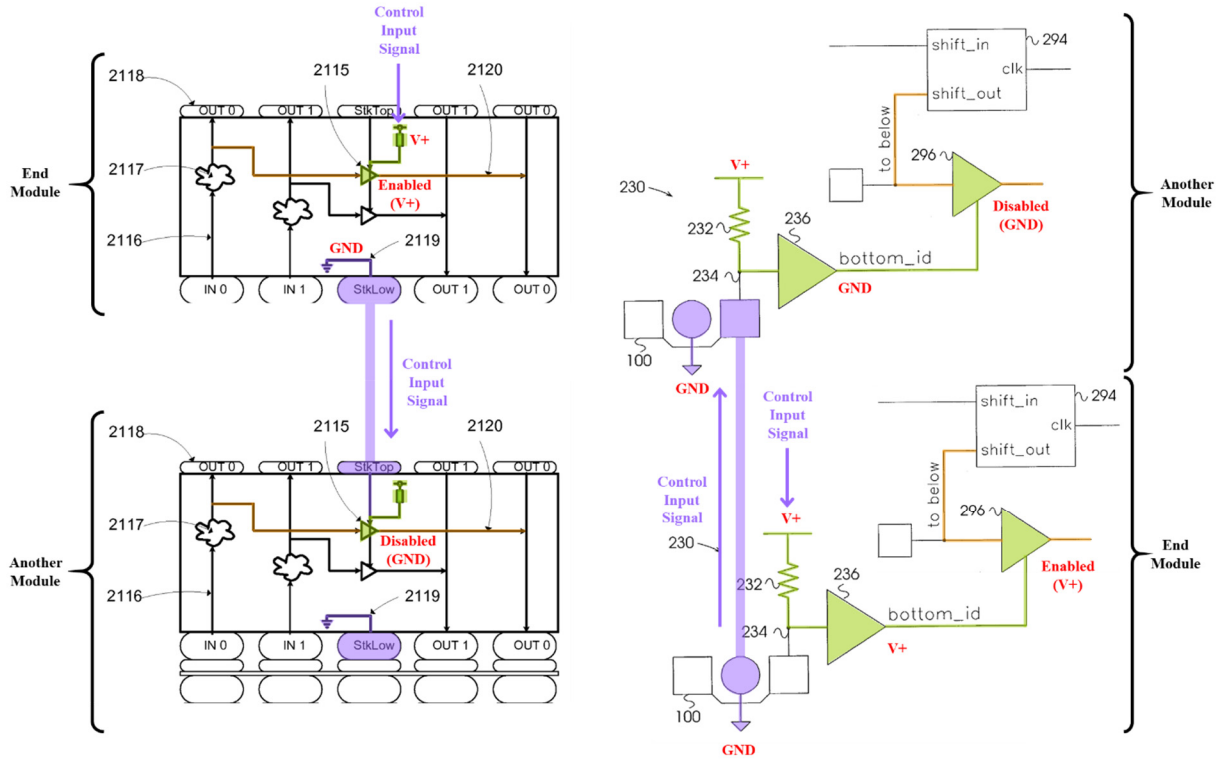
Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Figs. 6, 10.)

Sung's control circuits operate in the same manner as the control circuit described the '103 patent. (Ex. 1002, ¶¶ 347-357.) The '103 patent discloses that "[a]ll modules have … a selectable buffer 2115" with a control line "that tri-states the input when pulled low," to disable a routing path between first and second serial

chain routes, and to "let the input signal branch out 2120 to the other pads" when pulled high to enable the routing path. (Ex. 1001, 11:10-37; Ex. 1002, ¶¶ 347-357.) Each module's "StkLow" ball is "connected internally to GND 2119, thus pulling down the buffer control line when a module is stacked above it," and pulling it "up when no module is stacked directly above it." (*Id.*)

Below, Figures from the '103 patent and Sung have been highlighted and color-coded to demonstrate that the **die identifier circuit** and **tristate buffer** in Sung operate in the same manner as the control circuit in the '103 patent. (Ex. 1002, ¶¶ 347-357.)



(Ex. 1001, Fig. 21b; Ex. 1007, Figs. 5, 8.)

Thus, Sung discloses that the **tristate buffer** is disposed to enable a routing path between first and second serial chain routes in response to a control input signal received from another module when the end module is stacked to another module in exactly the same manner as the modules of the '103 patent. (Ex. 1002, ¶¶ 347-357.)

Alternatively, as discussed with respect to Section IX.D.1.h above, to the extent that Patent Owner argues that the claimed "end module" is a module other than the top or bottom module in the stack and that a routing path can span multiple modules, Sung, in view of Funaba, still renders obvious this element in additional ways. For example, under such a construction, the **control circuit** in module 112 enables the routing path within the modules 112 and 114 in response to a **control input signal** received from another module, such as module 114, when the other module 114 is stacked to the module 112. In that case, the control signal the **ground signal** received by module 112 from module 114. (Ex. 1007, [0046], [0049].)

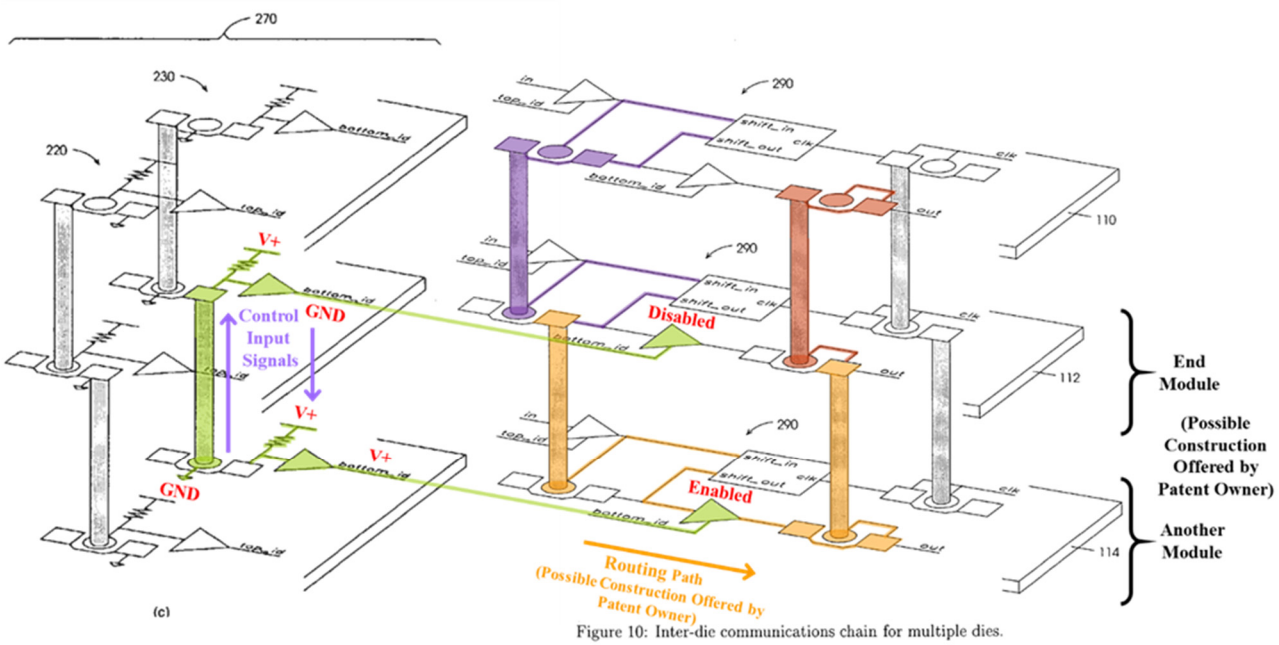


Figure 10: Inter-die communications chain for multiple dies.

(Ex. 1007, Figs. 6, 10.)

2. *Dependent Claim 16*

a. "The method of claim 12;"

See Section IX.D.1.

b. "adding to the plurality of modules a controller module that is disposed with an active pad;"

Sung, in view of Funaba, renders obvious this element.

As discussed in Section IX.D.1.a, Sung discloses, and it would have been obvious in view of Sung and Funaba, to stack memory modules. Further, it would have been obvious to a POSITA to mount the stack of memory modules on a **memory controller**, as taught by Funaba. (Ex. 1002, ¶¶ 359-367.)

Both Sung and Funaba disclose that various external signals will be input to and output from the stack. (Ex. 1002, ¶¶ 359-367.) For example, Sung discloses that its stacked modules can communicate with components external to the stack to receive or provide "external data input," "external data output," "global clocks, addresses, and control signals," that are each input to or output from the stack. (Ex. 1007, [0018], [0047], cls. 70-72.)

Funaba also describes a stacked system that receives and transmits external signals including clock, chip select, and data input/output signals. (Ex. 1008, Abstract, [0010]; Ex. 1002, ¶¶ 359-367.) To send these signals into and out of its stack, Funaba mounts its stack to a **memory controller** that relays and generates signals for controlling the stacked circuit, including signals for die addressing. (Ex. 1008, Abstract, [0010], [0055], [0105]; Ex. 1002, ¶¶ 359-367.) Because Funaba's **memory controller** is configured to "individually control[] the respective memory chips" in the stack, a POSITA would have understood Funaba's **memory controller** to be a controller module. (Ex. 1002, ¶¶ 359-367.)

From these teachings, a POSITA would have found it obvious to mount Sung's stacked system on Funaba's **memory controller** to enable Sung's stack to transmit and receive such external signals as "external data input," "external data output," "global clocks, addresses, and control signals." (Ex. 1007, [0047], cls. 70-72; Ex. 1008, Abstract; Ex. 1002, ¶¶ 359-367.) A POSITA would have mounted

Sung's stacked modules to Funaba's **memory controller**, for example, using the vertical conductors and terminators described in Sung. (Ex. 1007, [0043]-[0044].) A POSITA would have also connected the **memory controller** to a main board, such as a motherboard or PCB, to enable communication of signals, including addresses, "global clocks," "external data input," and "external data output signals," to and from the stack. (Ex. 1007, [0047], cls. 70-72; Ex. 1008, Abstract; Ex. 1002, ¶¶ 359-367.)

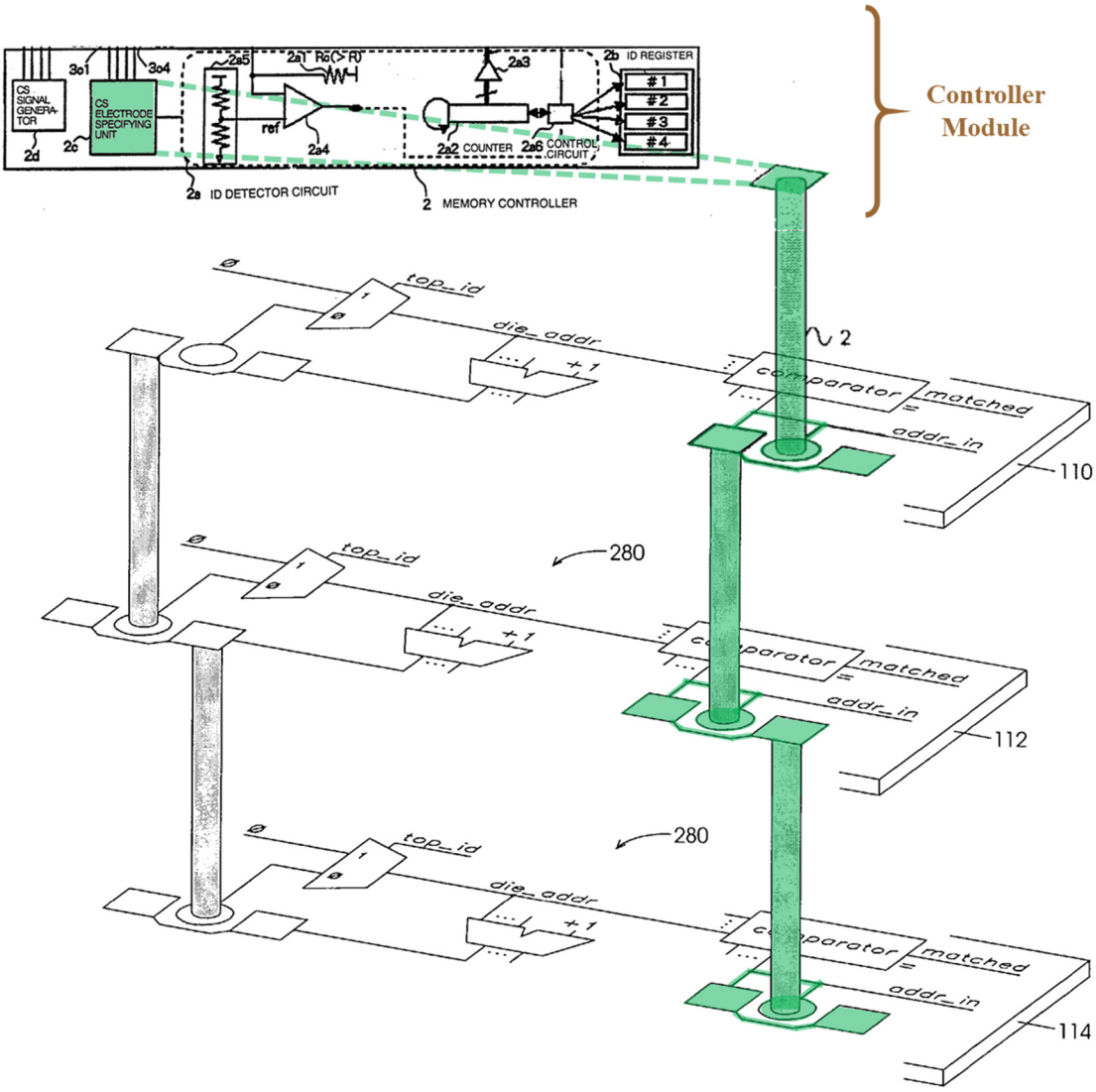


Figure 9: Die address precomputation and address resolution stack.

(Ex. 1007, Figs. 9; Ex. 1008, Fig. 4.)

Combining these references would have been routine for a POSITA because stacking memory and memory controllers was well-known in the prior art. (*See, e.g.*, Ex. 1011, [0100] (disclosing "an interposer substrate 210, an [input output (IO)] chip 211 mounted on the interposer substrate 210, and eight DRAM chips 201 stacked on the IO chip 211"); (Ex. 1002, ¶¶ 359-367.) Accordingly, a POSITA

would have had a reasonable expectation of success in mounting Sung's stack to Funaba's **memory controller**. (Ex. 1002, ¶¶ 359-367.)

The **memory controller** stacked with the memory modules is also disposed with an active pad. (Ex. 1002. ¶¶ 359-367.) For example, a vertical conductor of Sung's modules would connect with an active pad on the **memory controller** to carry one or more active signals, e.g., the "addr_in" signal, to the stack. (Ex. 1007, [0044], [0048]; Ex. 1002, ¶¶ 359-367.)

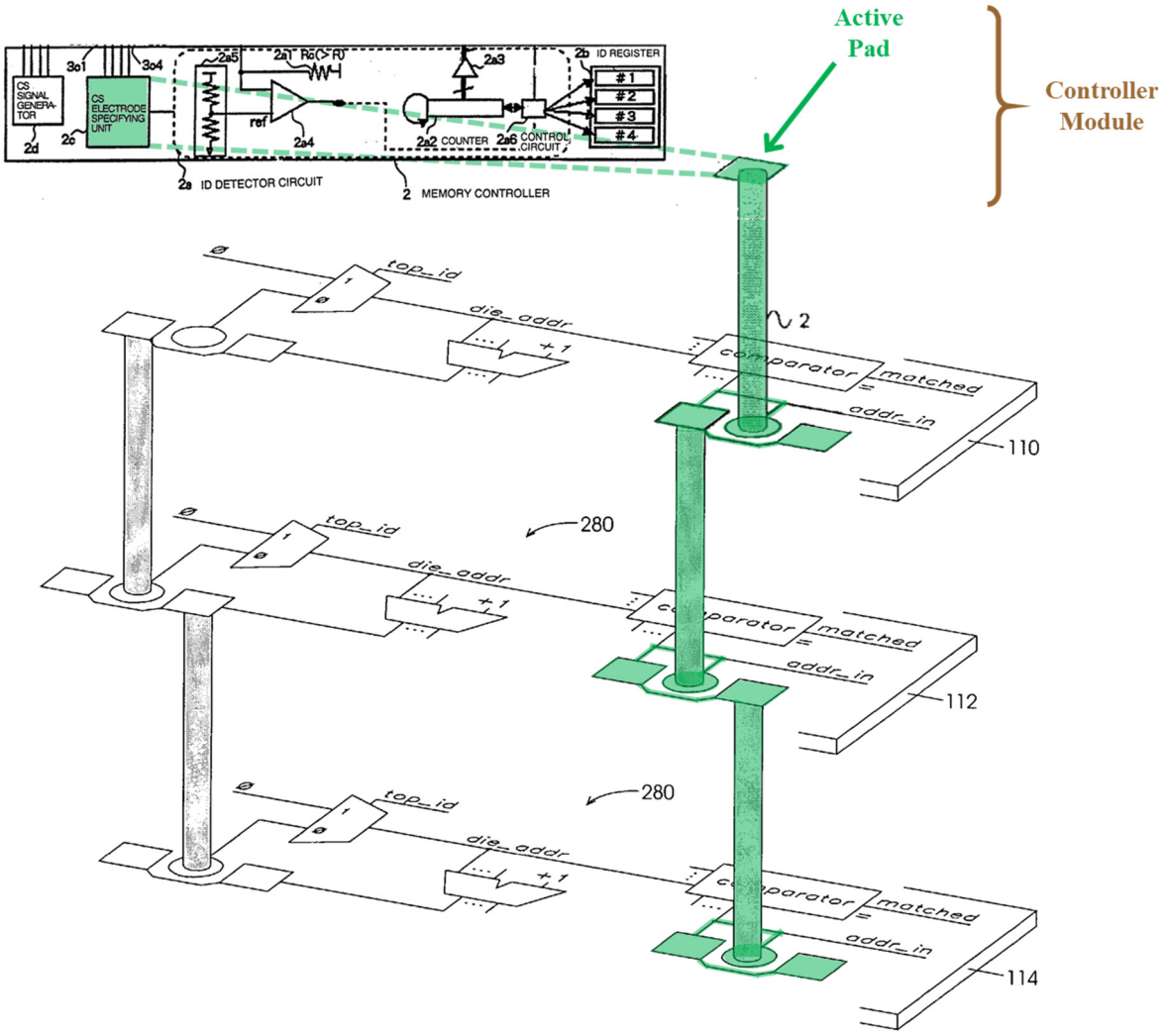


Figure 9: Die address precomputation and address resolution stack.

(Ex. 1007, Figs. 9; Ex. 1008, Fig. 4.)

Thus, a POSITA would have readily understood that the combination of Sung and Funaba renders obvious adding to the plurality of modules a controller module that is disposed with an active pad.

c. "providing a ladder-like routing path that includes a connection between said active pad from said controller module and one of said passive ports by stacking said first memory module with said controller module."

Sung, in view of Funaba, renders obvious this element.

First, Sung, in view of Funaba, renders obvious providing a connection between an active pad of a controller module and a passive port by stacking a first memory module with the controller module. As explained in Section IX.D.1.d, Sung discloses that stacking the modules and aligning the vertical conductors of each layer would couple the **pad of the conditional connection 104** on one module to a **through via** formed from the portions of vertical conductors extending "through the thickness of [a] substrate" on another module. A POSITA would have understood that aligning the connectors of each layer would cause the active pad of the controller module to connect with a passive port of a memory module stacked with the controller module. (Ex. 1007, [0040], [0044]; Ex. 1002. ¶¶ 368-376.)

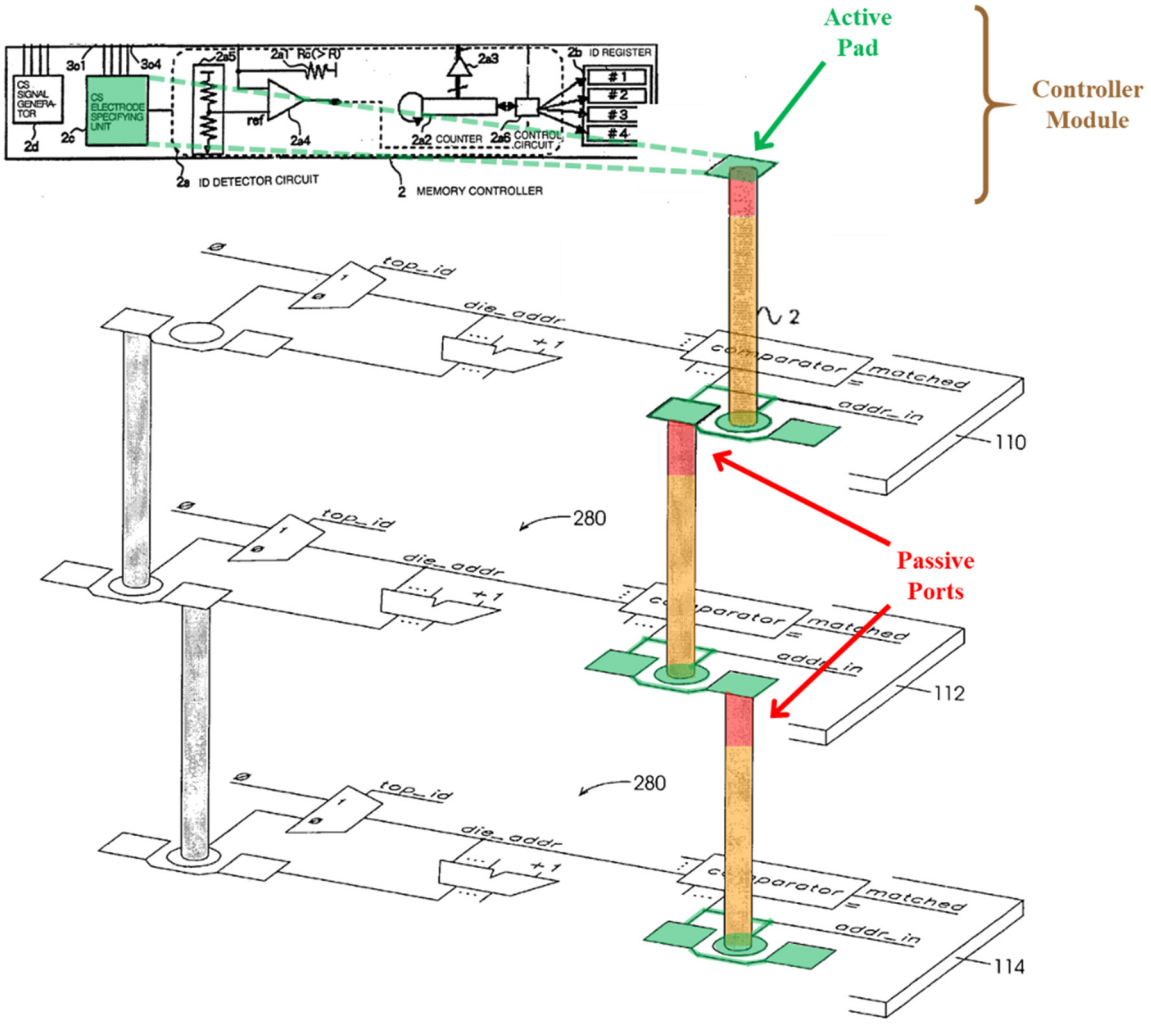


Figure 9: Die address precomputation and address resolution stack.

(Ex. 1007, Figs. 9, 6; Ex. 1008, Fig. 4.)

Second, Sung, in view of Funaba, renders obvious providing a ladder-like routing path that includes the connection between the active pad of the controller module and one of the passive ports. The broadcasting circuit of Sung provides a ladder-like routing path. (Ex. 1002, ¶¶ 368-376.) In particular, Sung shows a broadcasting circuit in which "alternating dies are offset by the distance, d, between the 3D via conductor and 3D via pads" of each connector. (Ex. 1007, [0030], [0044],

[0047].) This arrangement creates a ladder-like routing path having both vertical portions along the direction of the vertical conductors and horizontal portions along the direction of the metal conditional connection. (Ex. 1007, [0044]; Ex. 1002, ¶¶ 368-376.)

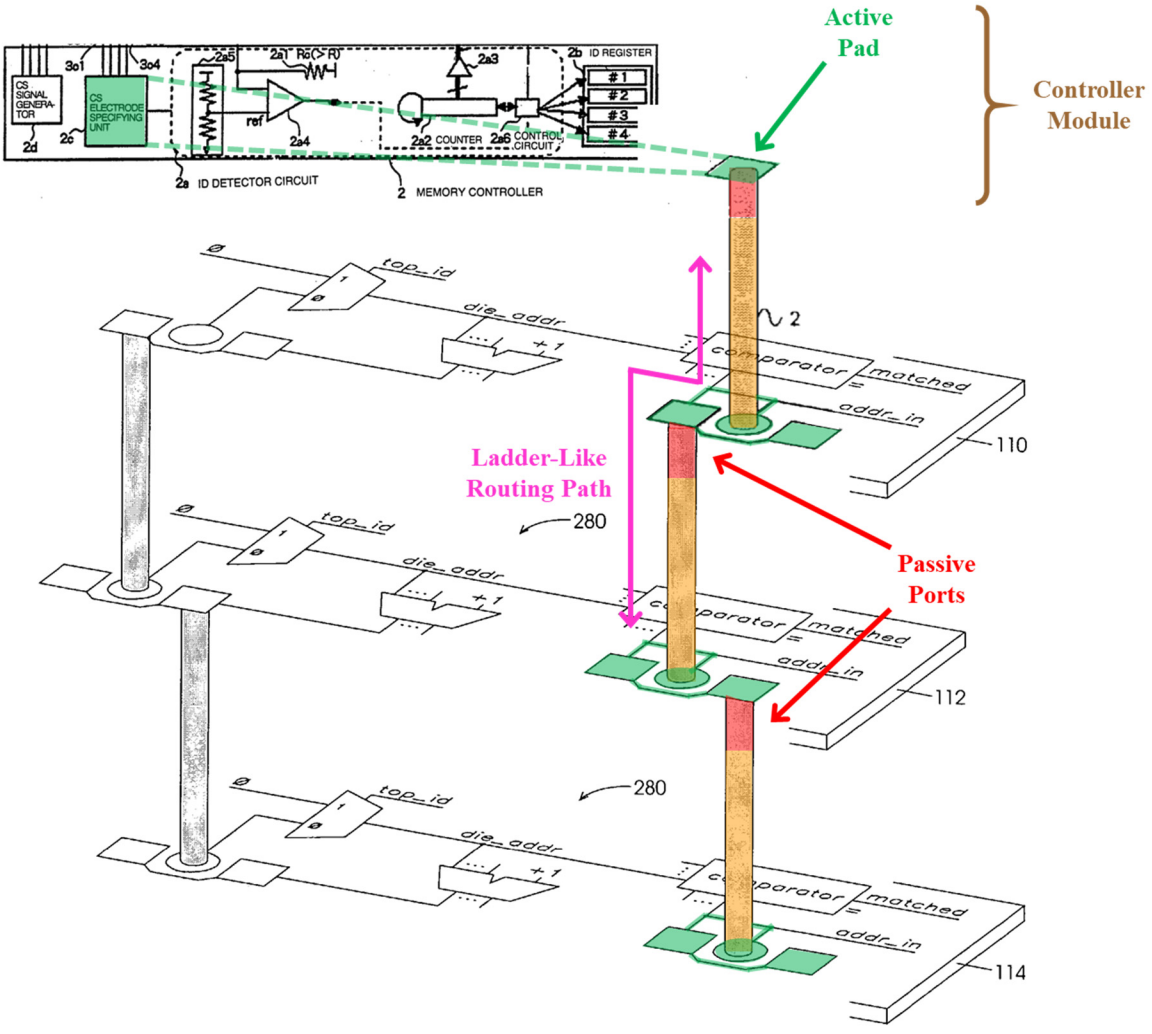


Figure 9: Die address precomputation and address resolution stack.

(Ex. 1007, Fig. 9; Ex. 1008, Fig. 4.)

Alternatively, to the extent that Patent Owner argues that the through vias of the vertical conductors of Sung are not a serial chain circuit, Sung, in view of Funaba, nevertheless renders obvious this feature in additional ways. For instance, the conditional connections coupling the terminator pads and vertical conductors of Sung are passive ports, such that the routing path between the active pad of the memory controller and the passive ports would have a ladder-like routing path.

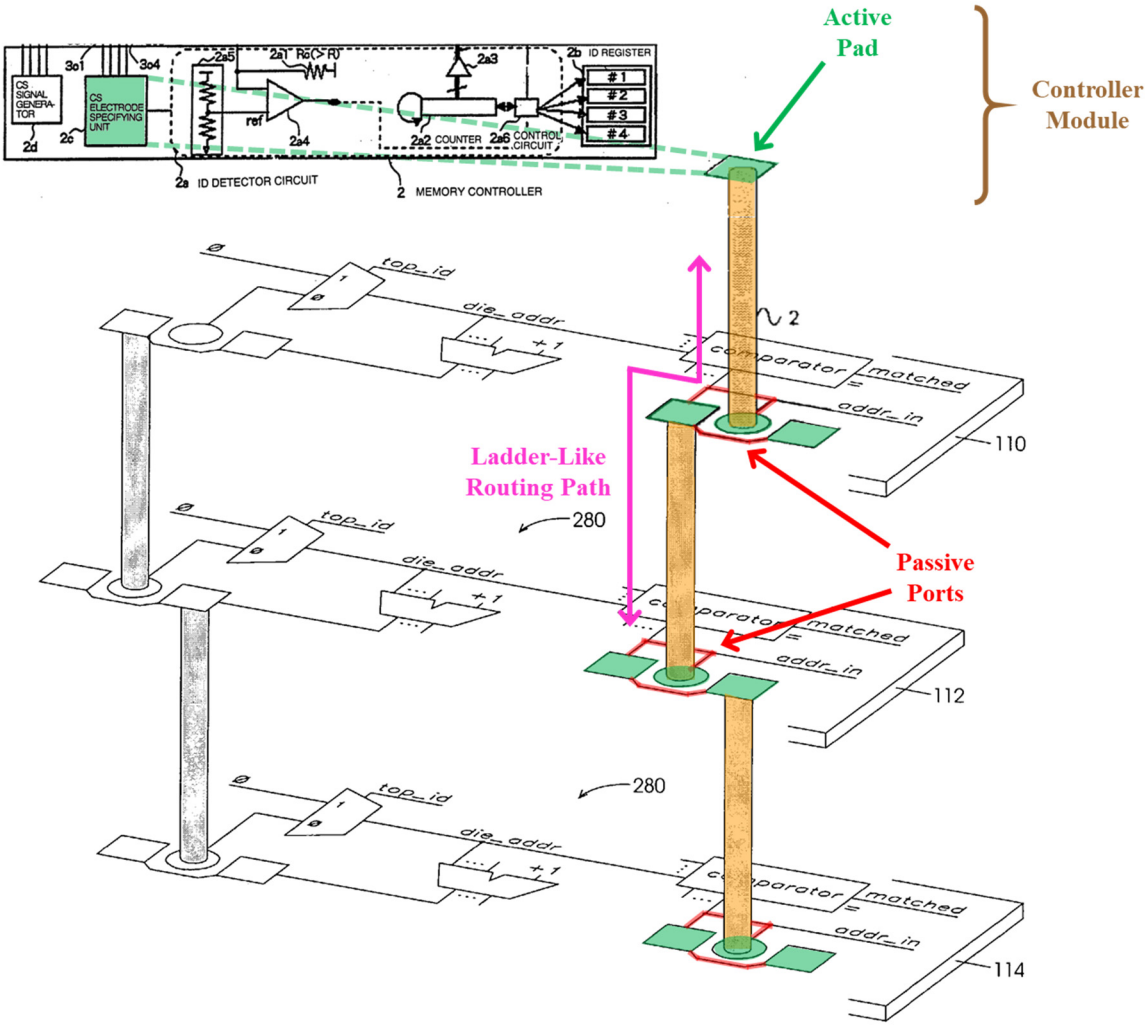


Figure 9: Die address precomputation and address resolution stack.

(Ex. 1007, Fig. 9; Ex. 1008, Fig. 4.)

X. SECONDARY CONSIDERATIONS

Petitioner is not aware of any secondary considerations that would tend to show the non-obviousness of the '103 patent.

XI. CONCLUSION

Petitioner requests institution of an *inter partes* review and cancellation of the Challenged Claims.

Date: August 23, 2018

Respectfully submitted,

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,545, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(i).

Respectfully submitted,

Date: August 23, 2018

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(1) and 42.105, the undersigned certifies that on August 23, 2018, a complete and entire copy of this Petition for Inter Partes Review and all supporting exhibits were provided via FedEx to the Patent Owner by serving the correspondence address of record as follows:

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