UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

Case No. Unassigned
Patent 8,773,871

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,773,871

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1013	Robert W. Erickson, Fundamentals of Power Electronics (Kluwer Academic Publishers, 1997)
1014	Paul Horowitz and Winfield Hill, The Art of Electronics (Cambridge

[1] Exhibit number 1005 is reserved to maintain consistent numbering for other exhibits that are also filed with concurrently filed Petition for the '871 Patent.

	University Press, 2nd ed. 1989) (reprinted 1998)
1015	U.S. Patent 6,061,257 ("Spampinato")
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1017	U.S. Patent 4,679,130 ("the '130 Patent")
1018	U.S. Patent 7,133,300 ("the '300 Patent")
1019	U.S. Patent 6,337,788 ("the '788 Patent")
1020	Nihal Kularatna, Power Electronics Design Handbook (Butterworth-Heinemann, 1998)

I. INTRODUCTION

Semiconductor Components Industries, LLC d/b/a ON Semiconductor ("ON Semiconductor" or "Petitioner") requests *inter partes* review ("IPR") under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq*. of Claims 1, 2, 3, 6, 8, 11, 12, 14, and 15 of U.S. Patent No. 8,773,871 ("'871 Patent").

Petitioner asserts that there is a reasonable likelihood that the challenged claims are unpatentable and requests review of, and cancellation of, the challenged claims under 35 U.S.C. §§ 102 and 103.

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices

Real Party in Interest: The real parties in interest are: (i) ON Semiconductor Corporation, (ii) Semiconductor Components Industries, LLC, doing business as ON Semiconductor, and (iii) Fairchild Semiconductor International, Inc., (iv) Fairchild Semiconductor Corporation, (v) Fairchild (Taiwan) Corporation, and (vi) System-General Corporation.

Related Matters: The '871 Patent is involved in a pending lawsuit entitled *ON Semiconductor Corp., et al. v. Power Integrations, Inc.*, No. 17-cv-247-LPS-CJB (D. Del.) ("Delaware Litigation"). Petitioner was first served with pleadings including the '871 Patent in the Delaware Litigation as part of Patent Owner's counterclaims in Patent Owner's Answer and Counterclaims to Plaintiff's First

Amended Complaint (Ex. 1009), served on September 29, 2017. Among the claims challenged herein, Claims 1, 2, 3, 6, 8, 12, 14, and 15 are at issue in the Delaware Litigation, while Claim 11 is *not* at issue in the Delaware Litigation. *See* Ex. 1012.

This Petition for IPR is being filed concurrently with an additional petition for IPR against different claims (i.e., Claims 9, 10, and 13) of the ’871 Patent, as well as two Petitions for IPR against U.S. Patent No. 8,077,483 (“the ’483 Patent”). The ’871 Patent is a continuation and claims benefit to the application of the ’483 Patent. In addition, Petitioner is concurrently filing a Petitions for IPR for two other patents held by Patent Owner (i.e., U.S. Patents Nos. 6,456,475 and 6,337,788). Further, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which are still pending: IPR2018-00160 (instituted 5-22-2018); IPR2018-00165 (instituted 5-18-2018); IPR2018-00166 (instituted 5-18-2018). In addition, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which have been decided, and/or are on appeal: IPR2016-00809 (FWD issued 9-22-2017); IPR2016-00995 (FWD issued 10-15-2017); IPR2016-01589 (FWD issued 2-14-2018); IPR2016-01590 (FWD issued 2-8-2018); IPR2016-01592 (FWD issued 2-8-2018); IPR2016-01594 (FWD issued 2-14-2018); IPR2016-01595 (FWD issued 2-14-2018); IPR2016-01597 (FWD issued 1-

25-2018); IPR2016-01600 (FWD issued 2-14-2018).

Lead Counsel: Lead Counsel is Roger Fulghum (Reg. 39,678) and Back-up Counsel are Brian Oaks (Reg. 44,981), Nick Schuneman (Reg. 62,088), and Brett Thompsen (Reg. 69,985), each of Baker Botts L.L.P.

Service Information: Baker Botts L.L.P., One Shell Plaza, 910 Louisiana Street, Houston, Texas 77002-4995; Tel. (713) 229-1234; Fax (713) 229-1522. Petitioner consents to service by electronic mail at: ONSemi_871IPR@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

B. Certification of Grounds for Standing

Petitioner certifies that the ’871 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the ’871 Patent.

C. Fees

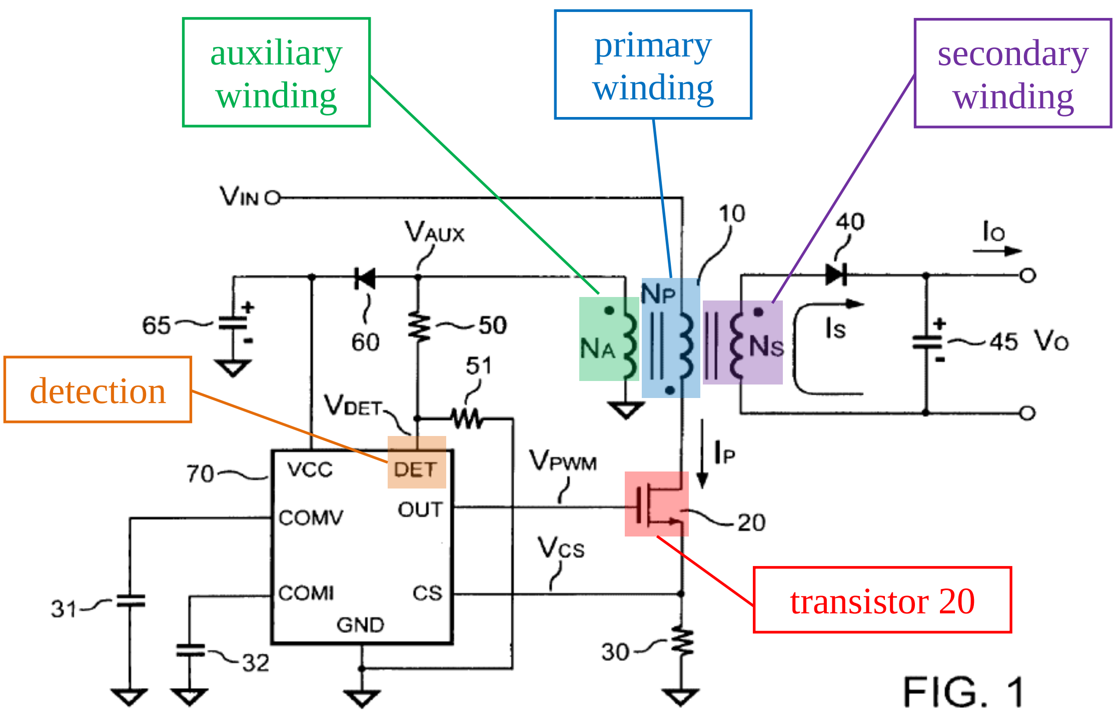
The Office is authorized to charge any fees that become due in connection with this Petition to Deposit Account No. 02-0384.

III. OVERVIEW OF THE ’871 PATENT

A. Background of the Technology

The ’871 Patent relates to switching power converters. Ex. 1001, Abstract. Such devices convert a first voltage (e.g., from a wall socket) to a second voltage to power an electronic device. *Id.*, 1:28-38. The ’871 Patent describes and claims a class of switching power converters that use the auxiliary winding of a transformer to detect information relevant to the control of the converter. But, as described by the background materials below, use of an auxiliary winding in switching power converters was well-known prior to the ’871 Patent. Ex. 1002, ¶ 33.

One example of a switching power converter that uses an auxiliary winding is provided by U.S. Patent 7,016,204 to Ta-Yung Yang et al. (“Yang”). Ex. 1006.



Id., Fig. 1 (annotations added); Ex. 1002, ¶ 34. Yang’s power converter includes transistor 20 coupled to transformer 10. Ex. 1006, Fig. 1. The transistor is turned on and off by a switching signal “V_{PWM}” to regulate how much energy is transferred from the input (V_{IN}) to the output (V_O) of the power converter. *Id.*, 2:34:40, Fig. 1.

When V_{PWM} goes high to turn on transistor 20, a current (I_P) flows from V_{IN}, through the primary winding N_P of transformer 10, and through transistor 20 and resistor 30 to ground. *Id.*, 2:41-43, Figs. 1-2. As the primary-side current I_P flows, the magnetic energy stored in transformer 10 builds. Then, when V_{PWM} goes low to turn off transistor 20, the magnetic energy stored in transformer 10 induces a secondary-side current I_S through the secondary winding N_S. *Id.*, 2:54-59, Figs. 1-2. The magnetic energy stored in transformer 10 is therefore transferred to the output by the secondary-side current I_S. In sum, the magnetic energy in the transformer is built up via primary winding N_P during the on-time of transistor 20 and transferred to the output of the power converter via secondary winding N_S during the off-time of transistor 20. Ex. 1002, ¶¶ 35-36.

As shown in Figure 1 of Yang, transformer 10 also includes auxiliary winding N_A. Because auxiliary winding N_A is magnetically coupled to the primary winding N_P and secondary winding N_S, auxiliary winding N_A "reflects" activity on the primary and secondary windings. Ex. 1002, ¶ 37. For example, when the secondary-side current I_S flows in the secondary side during the off-time of the primary-side switch, the auxiliary winding reflects the voltage present at the secondary winding.[2] Ex. 1006, 3:4-15. This voltage at the secondary winding is equal to the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40. Thus, as explained in Yang, the reflected voltage produced by the auxiliary winding equals the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40, multiplied by the winding ratio of the auxiliary and secondary windings:

$$V_{AUX} = \frac{T_{NA}}{T_{NS}} \times (V_O + V_F)$$

Id., 3:10 (Equation 3); Ex. 1002, ¶¶ 38-39.

Figure 2 of Yang illustrates this reflected voltage (V_{AUX}) produced on the auxiliary winding when the secondary-side current (I_S) flows:

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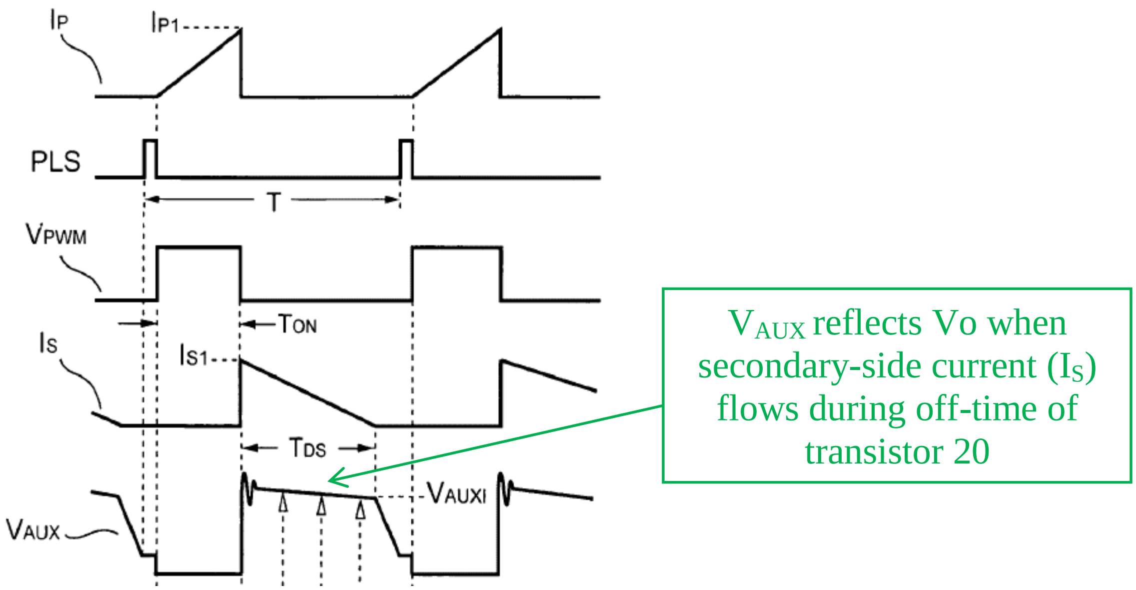
[2] The auxiliary winding reflects the voltage present at the secondary winding only during the portion of the off-time that current is flowing in the secondary side. *See* Ex. 1006, Fig. 2. Thus, when discussing herein the auxiliary winding's reflection of the voltage during the off-time of the power switch, the Petition is referring to the portion of the off-time when current flows through the secondary winding.



Ex. 1006, Fig. 2 (excerpt) (annotations added).

The auxiliary winding's reflected voltage can be used for multiple purposes. As shown in Figure 1 of Yang, V_{AUX} charges capacitor 65 via rectifier 60 to supply power for the internal circuitry of controller 70. Ex. 1006, 3:51-52, Fig. 1. In addition, V_{AUX} feeds information regarding output voltage V_O back to controller 70 via the DET pin. *See id.*, 3:36-50, 4:5-8, Fig. 1. In turn, controller 70 uses the feedback information to determine the pulse width of switching signal V_{PWM}, thereby regulating the flow of energy from the input V_{IN} to the output V_O of the converter. *See id.*, 4:5-38; Ex. 1002, ¶ 40.

Prior to the '871 Patent, it was well known that different functions could be performed based on the reflected voltage present at the auxiliary winding of a switching converter. Ex. 1002, ¶¶ 41-44. As described by Yang, it was known that the reflection of the output voltage on the auxiliary winding could be used as feedback for regulating the output voltage. Ex. 1006, 3:4-50, 4:5-8. It was also recognized that the reflection of the output voltage on the auxiliary winding could be used to detect various fault conditions at the output of the power converter, such as a short circuit fault condition (*see* Ex. 1015, 4:30-36; Ex. 1016, 3:26-63, Fig. 1) or an output over voltage fault condition (Ex. 1007, ¶ 0023; Ex. 1004, 3:58-67).

B. The Purported Advancement of the '871 Patent

Figure 1 of the '871 Patent illustrates a flyback-type power converter with a transformer that has an auxiliary winding:

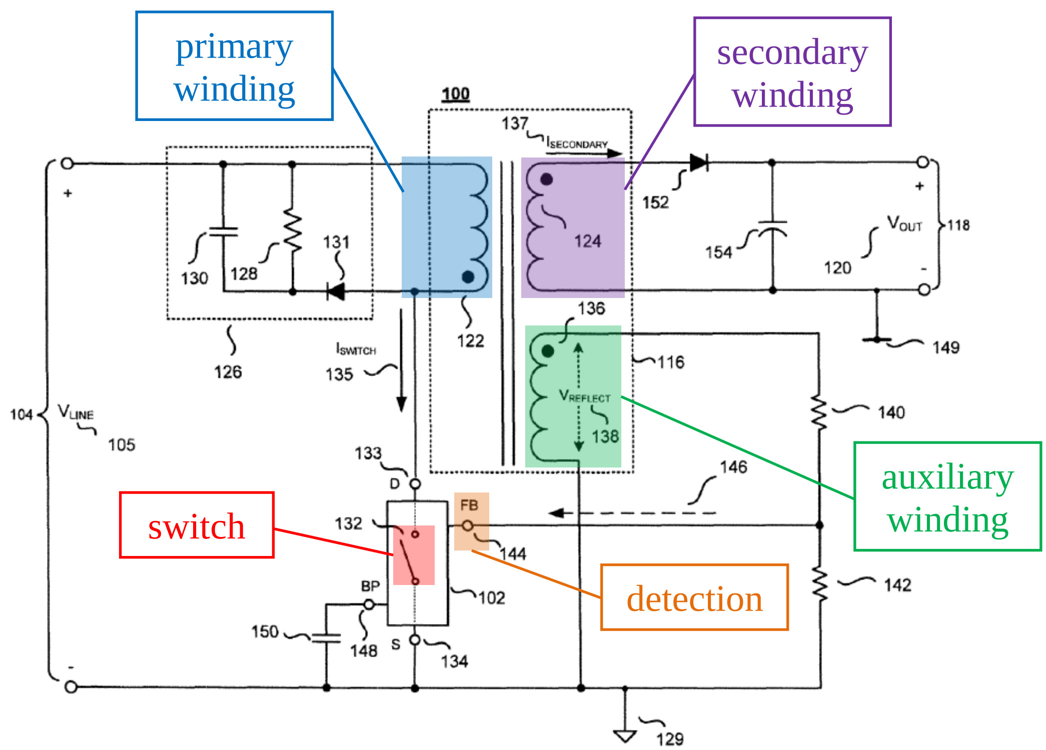
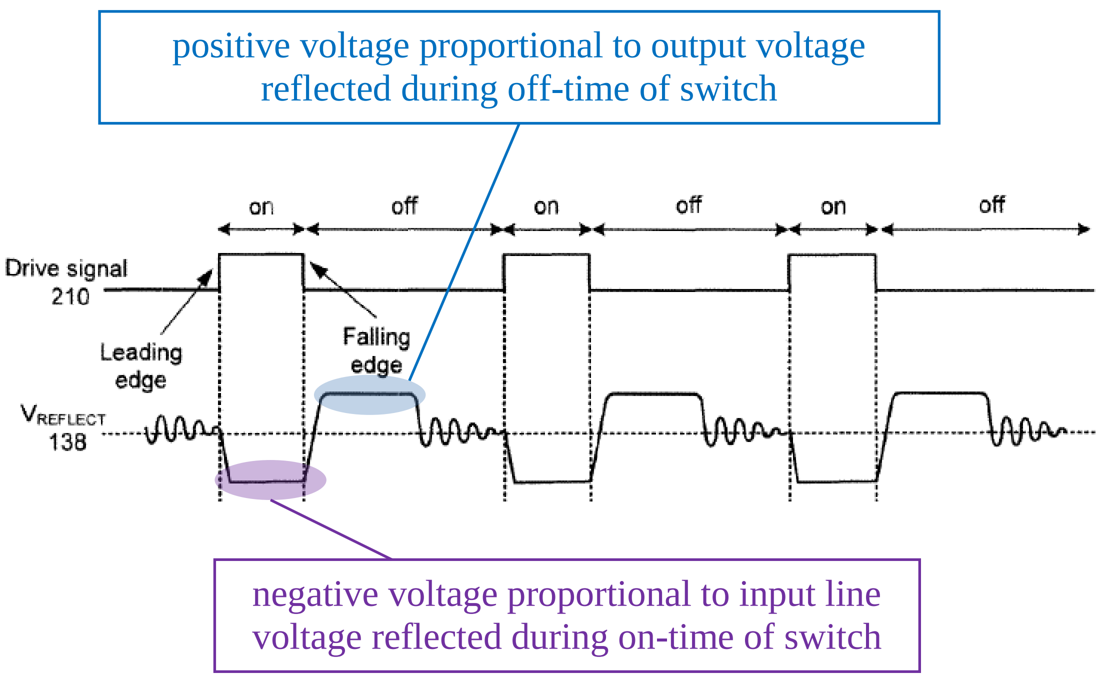


FIG. 1

Ex. 1001, Fig. 1 (annotations added); *see also id.*, 3:8-12; Ex. 1002, ¶ 45.

The ’871 Patent purports to improve upon known switching power converters by using the auxiliary winding to detect the input voltage (also referred to as the “line” voltage) in addition to the output voltage. Ex. 1001, 2:54-58, 3:47-58. The ’871 Patent explains that the “reflected voltage $V_{REFLECT}$” at the auxiliary winding is “representative of output voltage V_{OUT} 120 during at least a portion of the time when the power switch 132 is off.” *Id.*, 3:53-58. The ’871 Patent further explains that the “reflected voltage $V_{REFLECT}$” is also “representative of an input line voltage V_{LINE} 105 during at least a portion of the time of when the power switch 132 is on.” *Id.*; *see also id.*, 3:58-4:7.



Id., Fig. 4 (excerpt) (annotations added); Ex. 1002, ¶ 46.

However, the reflection of both the output voltage and the input line voltage[3] on the auxiliary winding at different times during the switching cycle is merely the result of the magnetic coupling between the different windings of the transformer. In other words, it is the magnetic coupling of the auxiliary winding in the flyback architecture that *dictates* the voltage that is reflected by the auxiliary winding during the on-time and off-time of the power switch. Ex. 1002, ¶ 48. As explained above, the auxiliary winding reflects the voltage present on the secondary winding (i.e., V_{OUT} plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). Ex. 1006, 3:4-15. The auxiliary winding likewise reflects the voltage present on the primary winding (i.e., the input line voltage) when current flows through the primary side (i.e., during the on-time of the switch). Ex. 1002, ¶ 48.

Thus, the purported invention of the '871 Patent is based on nothing more than the recognition of how an auxiliary winding naturally responds during the on-time and off-time of the switch due to the physical relationship (i.e., the magnetic coupling) between the auxiliary winding and the other windings, which exists in every flyback-type power converter with an auxiliary winding. Ex. 1002, ¶ 49.

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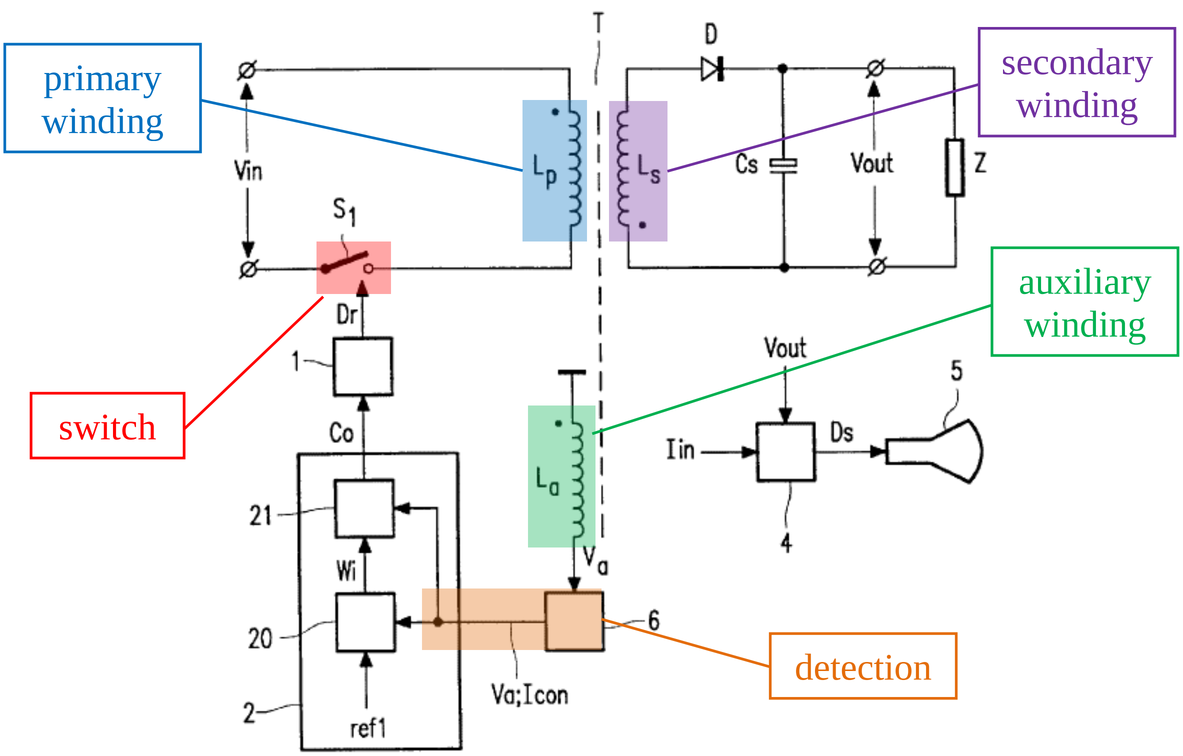
[3] The reflection of the line voltage is negative due to the opposing orientation of the windings in a flyback-type converter, as shown by the orientation of the dots on the individual windings in Figure 1 of the '871 Patent. Ex. 1002, ¶ 47.

C. Characteristics of Auxiliary Windings Were Well Known in the Art

Multiple prior art references (including prior art in the invalidity grounds relied upon herein) recognize and describe the relationship between the auxiliary winding and the primary and secondary windings. Ex. 1002, ¶¶ 50-54.

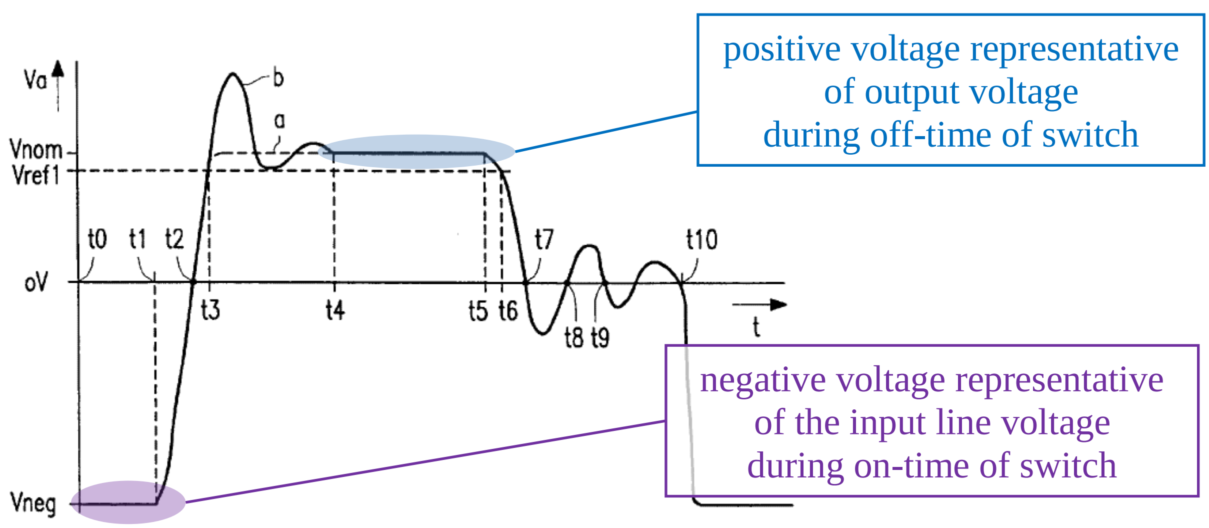
One example is U.S. Patent 5,831,839 ("Pansier"), which issued on November 3, 1998, over eight years before the claimed priority date of the '871 Patent. Ex. 1008. Like the '871 Patent, Pansier discloses a flyback-type switching power converter with an auxiliary winding:



Ex. 1008, Fig. 1 (annotations added); Ex. 1002, ¶ 50.

Pansier explains that, during the off-time of the switch, the auxiliary winding voltage Va "is equal to the DC output voltage Vout multiplied by the transformation ratio between the auxiliary winding La and the secondary winding Ls." Ex. 1008, 7:45-50, Fig. 3.[4] On the other hand, "auxiliary winding voltage Va has a negative value Vneg" during the on-time of the switch, "which equals the input voltage Vi multiplied by the transformation ratio between the auxiliary winding La and the primary winding Lp." *Id.*, 7:31-37.

Like Figure 4 of the '871 Patent, Figure 3 of Pansier illustrates the reflection at the auxiliary winding of both the output voltage (Vout) and input line voltage (Vi) at different times of the switching cycle:



Ex. 1008, Fig. 3 (annotations added); Ex. 1002, ¶¶ 51-52.

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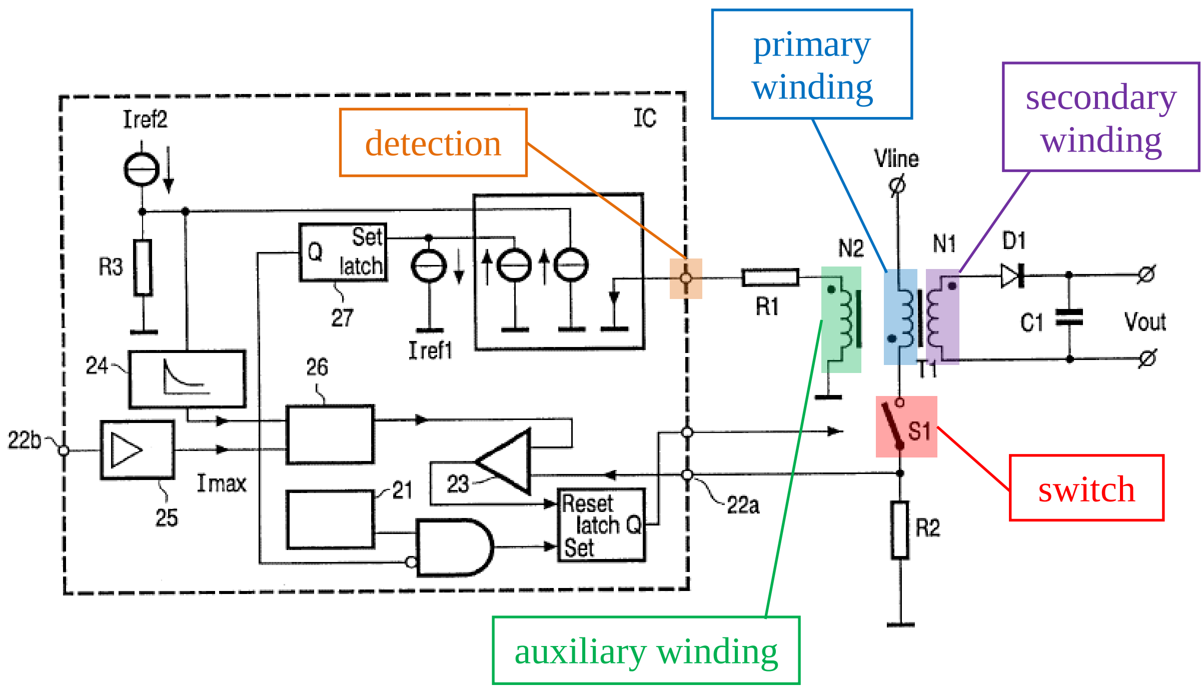
[4] *See also* Ex. 1008, 7:45-64 (explaining temporary overshoot of Va before settling to value representing output voltage).

Another example is U.S. Patent 6,542,386 ("Mobers"), which issued on April 1, 2003. Ex. 1004. Like Pansier, Mobers discloses a switching power converter with an auxiliary winding:



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 53. Mobers explains that by monitoring the auxiliary winding in a time-phased way, "not only V_{out} can be monitored …, but also V_{line} can be monitored … ." Ex. 1004, 5:5-10. Specifically, "information relating to the output voltage V_{out} will be present" on the auxiliary winding during the off-time of the switch, whereas "information relating to V_{line} will be present" on the auxiliary winding during the on-time of the switch. *Id.*, 5:50-53.

D. Examination History

The ’871 Patent is a continuation of U.S. Patent No. 8,406,013, which is a continuation of the ’483 Patent. During prosecution of the ’483 Patent, Patent Owner distinguished the purported invention by arguing that the prior art “fails to disclose ‘*a sensor coupled to receive a signal from* ***a single terminal*** *of the controller’ where the signal represents both* ***a line input voltage*** during the on time and ***an output voltage*** during the off time of a power converter.” Ex. 1010, 31 (bold and italics emphasis in original). For example, Patent Owner argued that the Yamada and Uruno references received the line input voltage information and the output voltage information from separate terminals, not a single terminal. *Id.*, 30-31. Patent Owner also distinguished the Balakrishnan ’161 reference because a diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on-time. *Id.*, 13.

Thus, Patent Owner emphasized that the distinguishing feature of the ’483 Patent (and by association the ’871 Patent) was the single terminal coupled to receive a signal representative of both the input and output voltage. But as described above, an auxiliary winding of a flyback switching power converter naturally reflects both the input and output voltage at different times during the switching cycle due to the physical properties of the transformer. *See, e.g.*, Ex. 1008, 7:31-43, Fig. 3; Ex. 1004, 5:11-14, 5:50-53. Thus, in the absence of a diode that blocks either the positive swing (representing the output voltage) or the negative swing (representing the input line voltage) of the signal from the auxiliary winding, a signal received from an auxiliary winding via a single terminal of the controller will represent both the input and the output voltage. Ex. 1002, ¶¶ 55-56.

The prior art relied upon in the grounds below was not considered during examination of the ’871 Patent or its parent ’483 Patent. Nonetheless, that prior art describes a single terminal coupled to an auxiliary winding in a flyback-type power supply, which receives a signal representative of both the output voltage and the input line voltage at different times during the switching cycle. The prior art therefore discloses and suggests what Patent Owner had previously identified as the distinguishing element of the ’483 Patent (and by association the ’871 Patent). And as shown in Section VI below, the prior art also discloses and suggests every other element of the challenged claims.

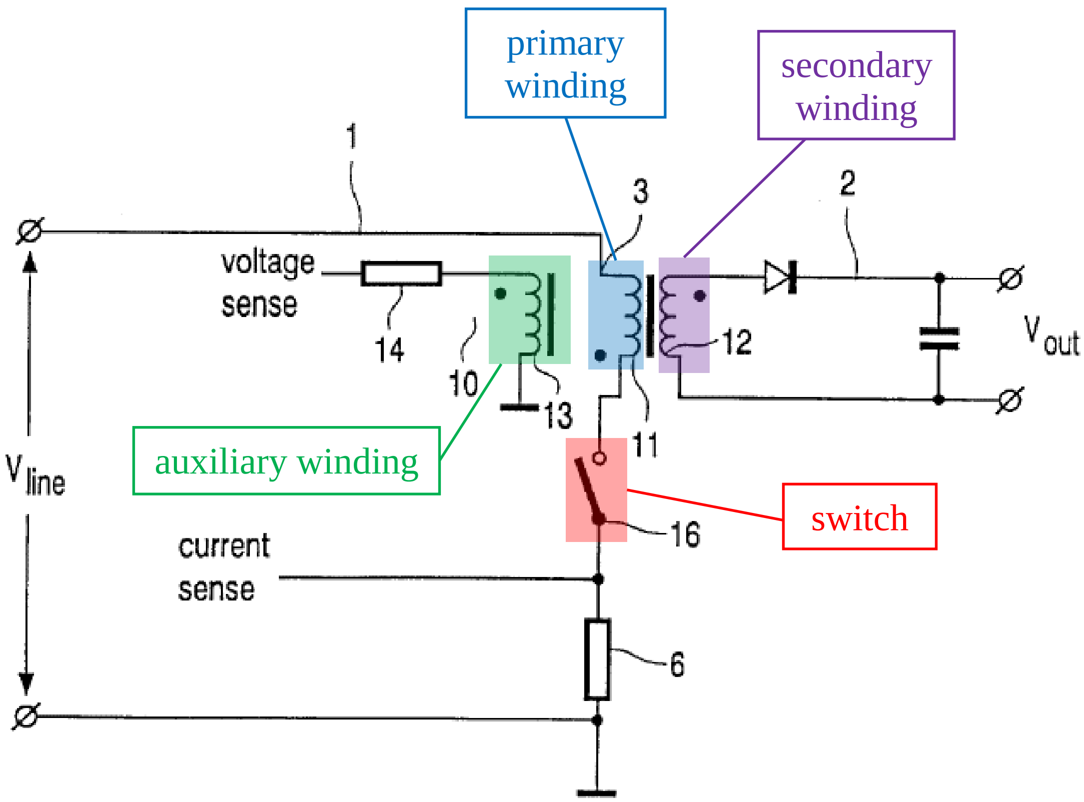
IV. SUMMARY OF PRIOR ART

A. Mobers

U.S. Patent 6,542,386 to Mobers et al. (“Mobers”) issued on April 1, 2003. Ex. 1004. The ’871 Patent was filed on February 26, 2013 and claims priority to a provisional application filed on April 6, 2007. Ex. 1001. Mobers is therefore prior art to the ’871 Patent under at least 35 U.S.C. § 102(b). Mobers was not considered by the Patent Office during examination of the ’871 Patent. *See*

Ex. 1001, 1-2 (References Cited).

Mobers discloses a switching power converter that utilizes a transformer with an auxiliary winding, which is referred to by Mobers as a "control winding." Ex. 1004, 4:1-28, Fig. 6. Figure 6 illustrates certain components of the switching power converter:



Ex. 1004, Fig. 6 (annotations added); Ex. 1002, ¶ 58. For flyback-type switching power converters like the one shown in Figure 6 of Mobers, the current through the primary winding builds up when the switch is turned on. Ex. 1004, 1:45-48, Fig. 3. As the primary-side current builds, the magnetic energy stored in the transformer also builds. Ex. 1002, ¶ 58. When the switch is turned off, the magnetic energy stored in the transformer is transferred to the output via a current produced by the transformer's secondary winding. Ex. 1004, 1:58-64; Ex. 1002, ¶ 58.

As described above in Section III.A-C, the auxiliary winding in a flyback-type switching power converter (i) reflects the voltage across the primary winding (indicative of input line voltage) when current flows through the primary side, and (ii) reflects the voltage across the secondary winding (indicative of the output voltage) when current flows through the secondary side. Ex. 1002, ¶ 59. Mobers recognizes this relationship and, with reference to Figure 6, explains: "When a current flows in either of windings 11 or 12, a current will also be induced in regulation circuit 10. The voltage generated across control winding 13 is related to V_{line} or V_{out} … ." Ex. 1004, 4:52-55; *see also id.*, 5:50-53 ("[T]he information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke.").

Mobers also discloses a technique for how to detect the V_{line} or V_{out} information provided by control winding 13 in Figure 6. Specifically, Mobers clamps the voltage on the left side of resistor 14 in Figure 6 to a fixed potential. *Id.*, 4:29-36. When a voltage (indicative of either V_{line} or V_{out}) is generated on the other side of resistor 14 by the control winding, the voltage potential across the resistor causes a current to flow. *Id.* During the on-time of the switch, the current through the resistor is:

$$I_r = \frac{kV_{line}}{R},$$

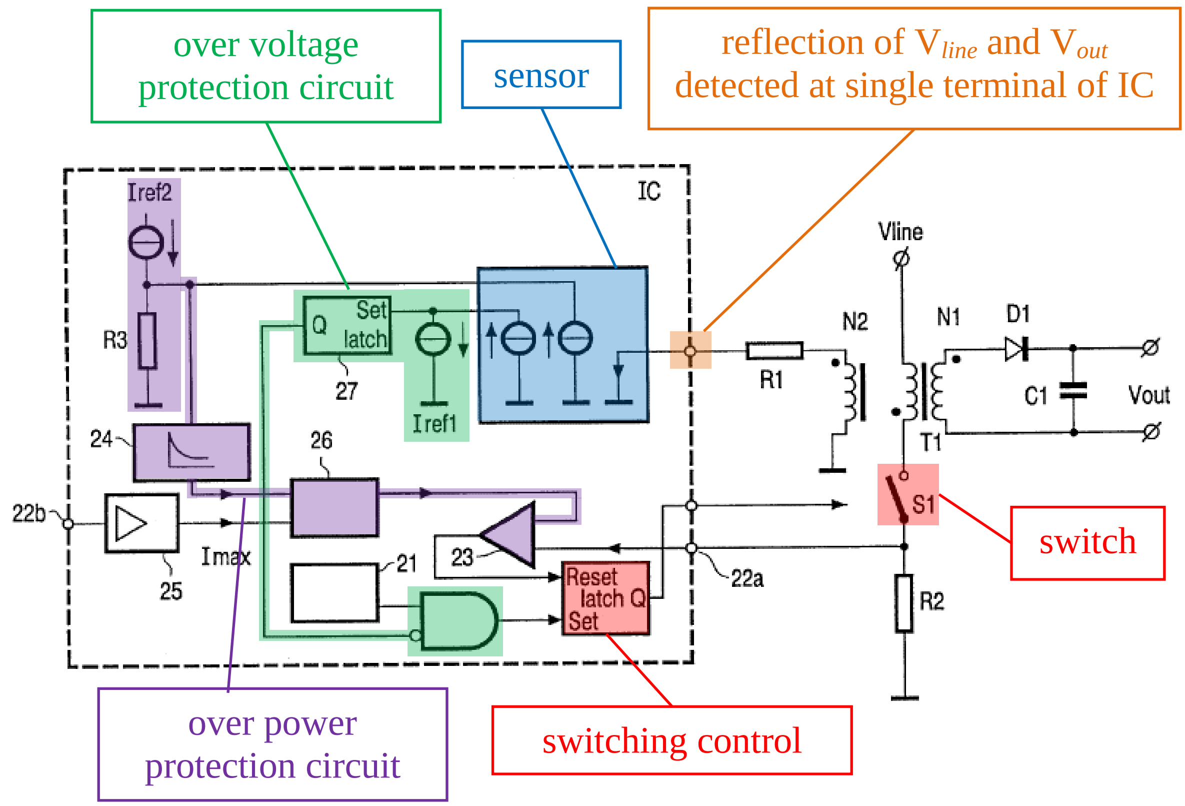
where *R* equals the resistor value and *k* is the winding ratio of the control winding to the primary winding. *Id.*, 4:54-65 (equation 2); *see also id.*, 4:12-20. And during the off-time of the switch, the current through the resistor is:

$$I_r = \frac{mV_{out}}{R}.$$

where *R* equals the resistor value and *m* is the winding ratio of the control winding to the secondary winding. *Id.*, 4:66-5:5 (equation 3); *see also id.*, 4:21-28; Ex. 1002, ¶ 60.

During the on-time of the switch, the control winding reflects a negative voltage indicative of V_{line}. Ex. 1002, ¶ 61. Thus, the current through resistor 14 in Figure 6 during the on-time of the switch is a "negative" current, i.e., a current flowing toward the control winding. Ex. 1004, 5:14-19. On the other hand, the control winding reflects a positive voltage indicative of V_{out} during off-time of the switch. Ex. 1002, ¶ 61. Thus, the current through resistor 14 in Figure 6 during the off-time of the switch is a "positive" current, i.e., a current flowing away from the control winding. Ex. 1004, 5:14-19.

Building on the explanation of the control winding shown in Figure 6, Mobers illustrates in Figure 7 how an integrated circuit (IC) controller utilizes the V_{line} and V_{out} information provided by control winding N2. Ex. 1004, Fig. 7; Ex. 1002, ¶ 62-66.



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 62.

For example, Mobers utilizes the output voltage information to implement output over voltage protection. Ex. 1004, 5:56-62. As shown in Figure 7, the sensor monitors the current from resistor R1, which represents either V_{out} or V_{line}. The sensor mirrors the current representative of V_{out} for comparison to a reference "Iref1." Ex. 1004, Fig. 7. If the current signal representing V_{out} exceeds "Iref1," then an output over voltage condition is detected and latch 27 is set. *See id.* In turn, the output of latch 27 causes a logic gate to block pulses from oscillator 21 to the switching control latch, which therefore blocks the switching control latch from turning on the switch. *See id.*, Fig. 7, 5:57-62 ("If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals."); *see also* Ex. 1002, ¶ 63; Ex. 1014, 28, 33 (explaining logic gates).

Mobers also utilizes the input line voltage information to implement an over power protection. Ex. 1004, 3:60-62, 5:26-45. As explained below, the over power protection scheme limits the on-time of the switch when the input line voltage V_{line} is high to prevent too much power from being transferred from the input to the output. Ex. 1002, ¶¶ 64-66.

Figure 7 of Mobers illustrates that a pulse from oscillator 21 sets the switching control latch to turn on switch S1 during each switching cycle (assuming no output over voltage fault condition). Ex. 1004, 5:27-28, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across resistor R2 (which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. The threshold for comparator 23 is set by minimum circuit 26. *Id.*, 5:48-50, Fig. 7. During normal conditions, minimum circuit 26 passes the feedback signal from error amplifier 25 to comparator 23. *See id.*, 5:46-50, Fig. 7. This forms what is known in the art as a current mode control loop, whereby the switch is turned off during each cycle when the current through the power switch reaches a threshold that is based on feedback from the output voltage. Ex. 1013, 16-18; Ex. 1002, ¶ 65.

However, when the input line voltage is high, the over power protection system intervenes by limiting the peak current set point as a function of the input line voltage. Minimum circuit 26 passes the smaller of the two thresholds provided by error amplifier 25 and curve circuit 24. *See* Ex. 1004, 5:46-48, Fig. 7. As depicted by the curve inside curve circuit 24 in Figure 7, curve circuit 24 outputs a lower threshold value at higher input line voltages. *Id.*, 5:38-45, Fig. 7. When the signal from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold from curve circuit 24 to comparator 23. *See id.*, 5:46-50, Fig. 7. This limits the peak current through switch S1 as a function of the input line voltage, thereby preventing the amount of power passed to the output from exceeding a maximum safe level. *Id.*, 5:46-50, Fig. 7; *see also id.*, Abstract, 1:5-13, 2:50-53, 3:60-62; Ex. 1002, ¶ 66.

Notably, Mobers explains that the "advantage" of its detection scheme is that both V_{out} and V_{line} are detected "via the same existing pin on the integrated circuit." Ex. 1004, 5:20-25; *see also id.*, 2:56-61, 3:14-20. The advantages of detecting both the output voltage and the input line voltage via a single terminal of an IC were therefore known well before the ’871 Patent. Ex. 1002, ¶ 67.

V. CLAIM CONSTRUCTION

In the Delaware Litigation, neither Petitioner nor Patent Owner raised a claim construction issue involving the ’871 Patent for the District Court to resolve. *See* Ex. 1011. Petitioner maintains that all terms should be given their plain and ordinary meaning. But, Petitioner provides some explanation below with respect to the “switching control” elements in the challenged claims of the ’871 Patent, in light of Patent Owner’s application of that language in its infringement contentions in the related Delaware Litigation. *See* Ex. 1002, ¶ 69.

A. “switching control” elements

Claim element 1[c] requires “a switching control to be coupled to switch the power switch to regulate the output of the power converter in response to the sensor.” Ex. 1001, 8:59-61 (emphasis added). Part of claim element 1[d] then recites “wherein the switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal.”[5] *Id.*, 8:64-67 (emphasis added). The phrase “further coupled to switch the power switch to regulate the output of the power converter in response to the

[5] Like Claim 1, Claim 8 and its dependent Claim 14 together recite the “coupled to” language (Claim 8) and the “further coupled to” language (Claim 14).

power limit signal" further defines the coupling of the switching control to specify that regulation of the output is specifically in response to the power limit signal from the sensor. This language does not, however, require a separate coupling between the sensor and the switching control, or between the switching control and the power switch, as compared to the coupling required by claim element 1[c]. *See* Ex. 1002, ¶ 70.

Patent Owner applied the same interpretation of this limitation in Patent Owner's infringement contentions served on Petitioner on January 5, 2018 in the Delaware Litigation. With respect to the alleged infringing device, Patent Owner pointed to the over power protection ("OPP") and the over voltage protection ("OVP") as mapping to claim element 1[c][6] (which includes the "coupled to" language). Ex. 1012, pp. 5-7 ("The NCP1250 implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage at the OPP/Latch pin. ... The NCP1250 also implements a latching output over-voltage protection ('OVP') that will stop the switching of the power switch when an output over voltage is detected.").

Patent Owner then pointed to the over power protection circuit again as

[6] The claim elements labeled 1[c] and 1[d] herein are respectively labeled 1[d] and 1[e] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7, 8-9.

mapping to claim element 1[d][7] (which includes the "further coupled to" language). Ex. 1012, pp. 8-9 ("The NCP1250 implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage at the OPP/Latch pin."). Thus, as applied by Patent Owner, the "further coupled to" language in claim element 1[d] would not require a separate or additional coupling for the switching control as compared to what is already identified in claim element 1[c]. *See* Ex. 1002, ¶¶ 71-72.

In any event, as explained below in Section VI.A.1, the Mobers prior art implements the same OVP and OPP functions using similar couplings between sensor, switching control, and power switch as the accused product. Thus, Mobers discloses the various "switching control" limitations under any reasonable construction that Patent Owner could propose while remaining consistent with its infringement contentions in the Delaware Litigation.

In sum, Petitioner maintains that no specific construction is required for this term. But if Patent Owner chooses to propose a construction in this IPR, Petitioner contends that any construction of the "switching control" limitations should be

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[7] The claim elements labeled 1[c] and 1[d] herein are respectively labeled 1[d] and 1[e] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7, 8-9.

consistent with Patent Owner's broad interpretation of that limitation as applied in its infringement contentions in the Delaware Litigation.

VI. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

Pursuant to 37 C.F.R. §§ 42.22 and 42.104(b), the challenged claims are unpatentable for the reasons set forth in detail below.

A. Ground 1: Mobers Anticipates Claims 1-3, 6, 8, 12, 14, and 15 Under 35 U.S.C. § 102

Mobers discloses each element of claims 1, 2, 3, 6, 8, 12, 14, and 15, a thus anticipates each of these claims under 35 U.S.C. § 102. *See* Ex. 1002, ¶ 73.

1. Claim 1

<u>Claim 1[pre]: "A controller for use in a power converter, comprising:"</u>

Mobers discloses a controller for use in a power converter. "The switched-mode power supply … may … comprise a <u>control circuit</u> for controlling the controllable current switching means. The <u>control circuit</u> may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz." Ex. 1004, 3:6-11 (emphasis added). The PWM control circuit is specifically shown in Figure 7:

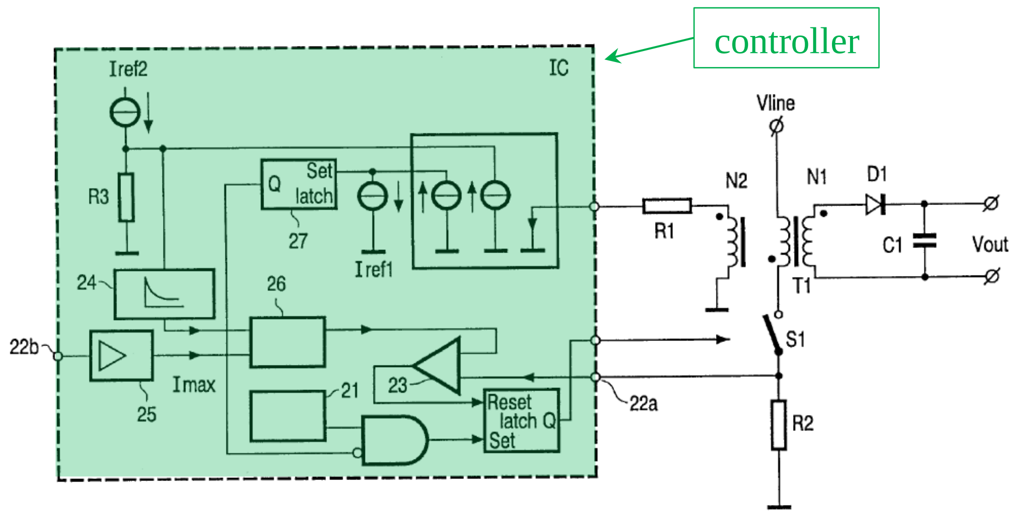


FIG. 7

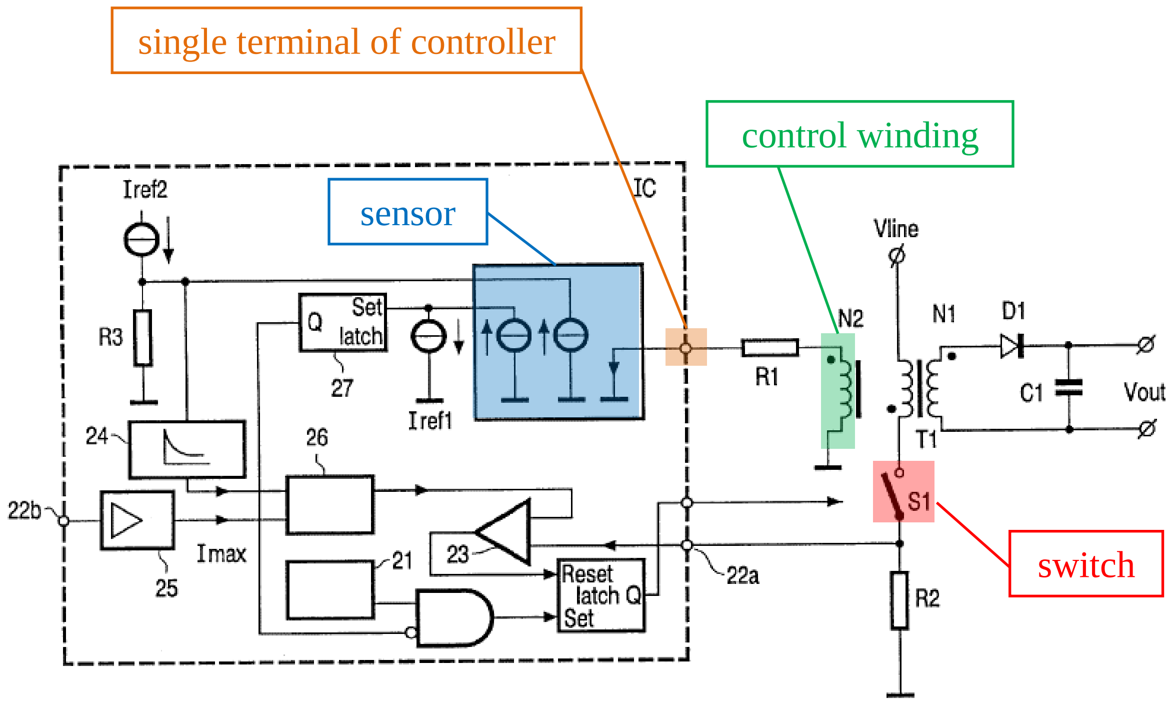
Ex. 1004, Fig. 7; *see also id.*, 5:26-33. Accordingly, Mobers discloses each element of the preamble of Claim 1.[8] Ex. 1002, ¶ 74.

1[pre]. A controller for use in a power converter, comprising:	Ex. 1004, 3:6-12: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. The control circuit typically response to a control signal from the third winding." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *See also* Ex. 1004, 5:20-25, 5:34-62, 5:63-6:3; Figs. 6-8, Claims 1, 3, 5, 6.

[8] The preamble is not limiting but is nonetheless disclosed by Mobers.

Claim 1[a]: "a sensor coupled to receive a signal from a single terminal of the controller,"

As shown in Figure 7, Mobers discloses a sensor coupled to receive a signal from a single terminal of the controller:



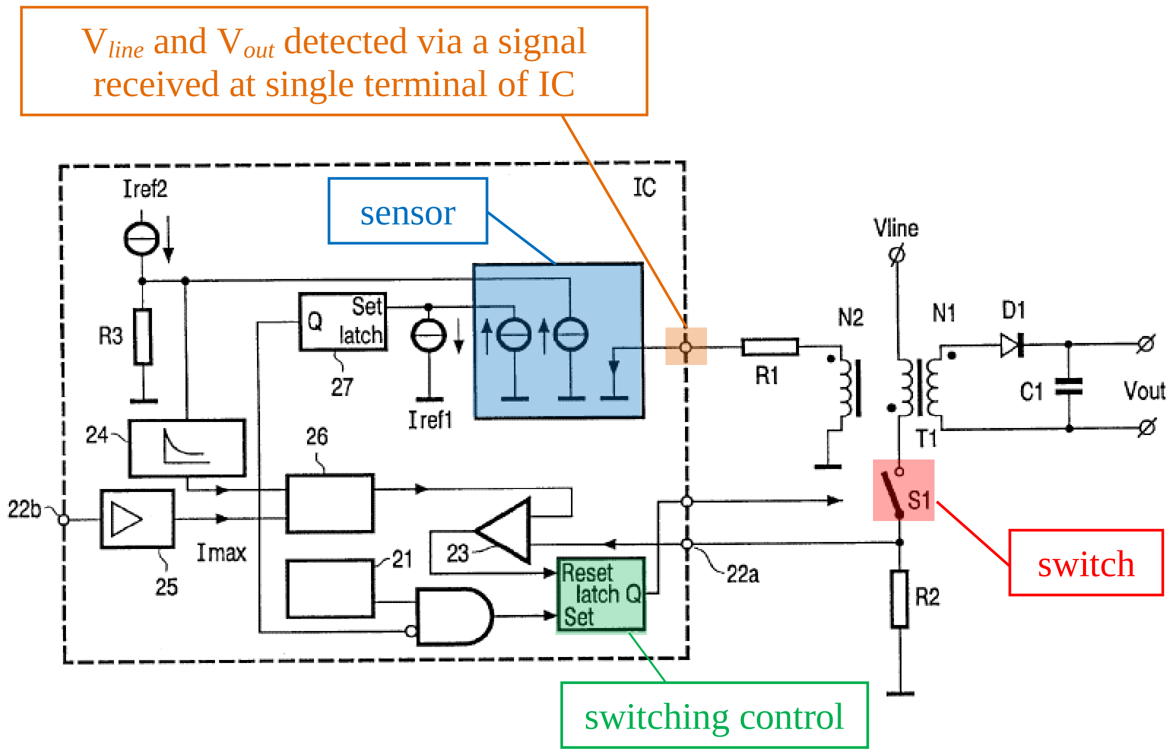
Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 75. Mobers explains that the controller typically responds "to a control signal from the third winding" (i.e., control winding N2). *Id.*, 3:11-12. "Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." *Id.*, 3:14-17. And because "a plurality of information is provided via the same control signal the control circuit may receive that information via a *single input pin*." *Id.*, 3:18-20 (emphasis added).

Accordingly, Mobers discloses each limitation of claim element 1[a]. Ex. 1002, ¶¶ 75-76.

[1a] a sensor coupled to receive a signal from a single terminal of the controller,	Ex. 1004, 5:50-55: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information." (emphasis added). Ex. 1004, 3:18-20: "Since a plurality of information is provided via the same control signal the control circuit may receive that information via a single input pin." (emphasis added). Ex. 1004, 5:20-25: "It is an advantage of the present invention that the information obtained during the primary and secondary strokes are provided via the same existing pin on the integrated circuit receiving and processing the information thereby avoiding the additional external components as suggested in the prior art." (emphasis added). Ex. 1004, Claim 5: "A switched-mode power regulator according to claim 3, wherein the control signal from the monitoring means is received by the control circuit via a single input pin." (emphasis added). *See also* Ex. 1004, Abstract, 1:5-13, 2:56-61, 3:1-17, 4:29-36, 4:52-5:4, 5:6-19, 5:63-6:3, Claims 1, 3, 4, 6, 10, Figures 6-8.

Claim 1[b]: "the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of a power switch and the signal from the single terminal to represent a line input voltage during a portion of an on time of the power switch,"

As shown in Figure 7 of Mobers, the sensor is coupled to receive, from a single terminal of the "IC," the signal that is generated by control winding N2 and resistor R1:



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 77.

The signal received by the sensor from resistor R1, via the single terminal of the controller, represents (i) the input line voltage (V_{line}) of the power converter during the on-time of switch S1, and (ii) the output voltage (V_{out}) of the power converter during at least a portion of the off-time of switch S1. *See* Ex. 1004, 5:50-55; Ex. 1002, ¶ 78.

Mobers discloses how V_{line} and V_{out} are represented by the signal that the sensor receives from the resistor (e.g., resistor R1 in Figure 7) coupled to the control winding. Specifically, Mobers clamps the voltage on the left side of the resistor to a fixed potential. Ex. 1004, 4:29-36, Figs. 6-7; *see also id.*, 5:63-6:3, Fig. 8; Ex. 1002, ¶ 79. When a voltage is generated by the control winding (indicative of either V_{line} or V_{out}) on the other side of the resistor, the voltage potential across the resistor causes a current to flow. *Id.* During the on-time of the switch (i.e., when V_{line} is reflected on the control winding), the current through the resistor is:

$$I_r = \frac{kV_{line}}{R},$$

where *R* equals the resistor value and *k* is the winding ratio of the control winding to the primary winding. *Id.*, 4:54-65 (equation 2); *see also id.*, 4:12-20. And during the off-time of the switch (i.e., when V_{out} is reflected on the control winding), the current through the resistor is:

$$I_r = \frac{mV_{out}}{R}.$$

where *R* equals the resistor value and *m* is the winding ratio of the control winding to the secondary winding. *Id.*, 4:66-5:5 (equation 3); *see also id.*, 4:21-28.

Because the control winding reflects a negative voltage indicative of V_{line} during the on-time of the switch (Ex. 1002, ¶ 80), the current through resistor 14 in

Figure 6 during the on-time of the switch is a "negative" current, i.e., a current flowing toward the control winding (Ex. 1004, 5:14-19). On the other hand, because the control winding reflects a positive voltage indicative of V_{out} during off-time of the switch (Ex. 1002, ¶ 80), the current through resistor 14 in Figure 6 during the off-time of the switch is a "positive" current, i.e., a current flowing away from the control winding (Ex. 1004, 5:14-19).

In sum, the signal received by the sensor represents both the input line voltage V_{line} and the output voltage V_{out} during different times of the switching cycle as required by claim element 1[b]. Accordingly, Mobers discloses each limitation of claim element 1[b]. Ex. 1002, ¶¶ 77-81.

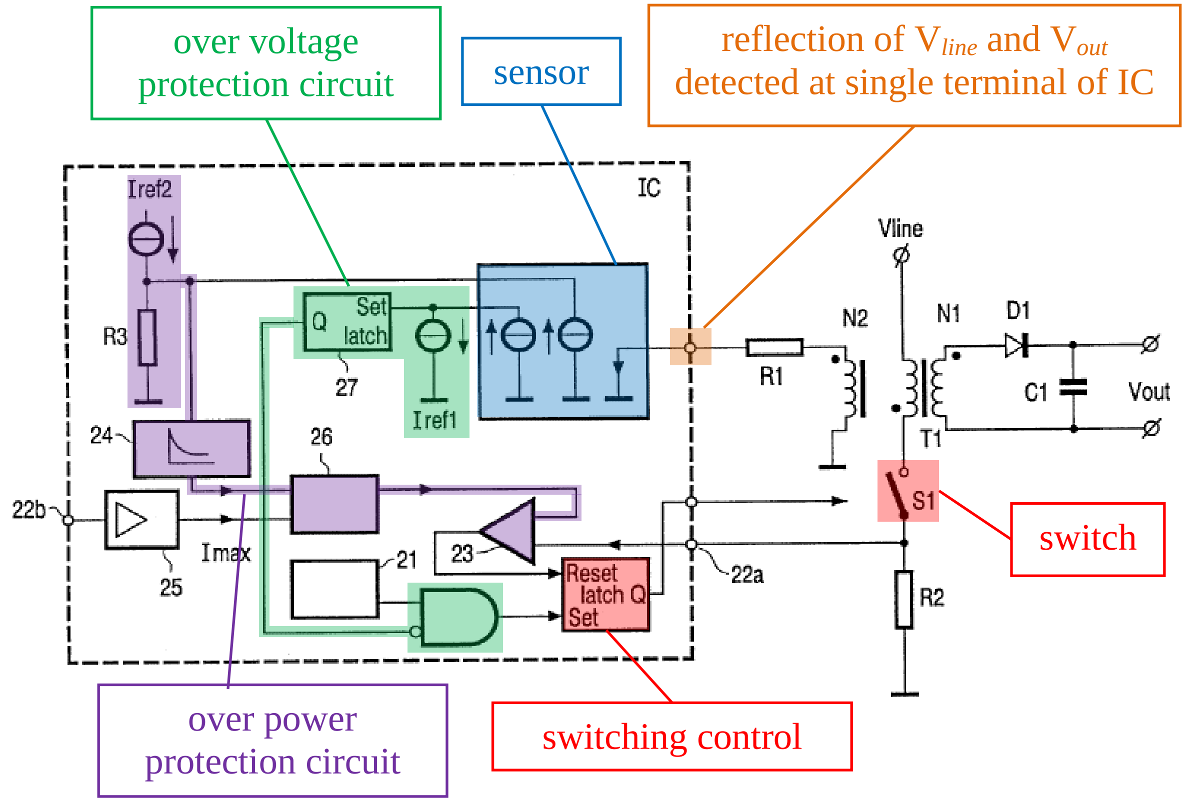
[1b] the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage during a portion of an on time of the power	*See* citations for claim element 1[a]. Ex. 1004, 3:11-17: "The control circuit typically response to a <u>control signal from the third winding</u>. This control signal may comprise a [sic] information relating to the performance or status of the switched mode power supply. <u>Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply</u>." (emphasis added). Ex. 1004, 5:50-53: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information." Ex. 1004, 4:29-36: "One end of the control winding 13 is connected to ground whereas the other and of the control winding is connected to resistor 14. By clamping the left side

switch,	of resistor 14 to a fixed potential a current will flow through resistor 14 when this potential is different from the voltage generated across control winding 13. By measuring the current flowing through resistor 14 the voltage generated across the control winding 13 can be determined." Ex. 1004, 4:52-5:5: "When a current flows in either of windings 11 or 12, a current will also be induced in regulation circuit 10. The voltage generated across control winding 13 is related to V_{line} or V_{out} according to ratios k and m, respectively. A sensing circuit (not shown) measures the current flowing through resistor 14. Thus, knowing the value of resistor 14, V_{line} and V_{out} can be monitored. If the resistor 14 has resistance R, the current in the regulation circuit 10, I_r, is related to Vl_{ine} during t_{on} in the following way $I_r = \frac{kV_{line}}{R}$, (2) whereas, during t_{off}, the current is related to Vout in the following way $I_r = \frac{mV_{out}}{R}$. (3) " Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." Ex. 1004, Claim 6: "A switched mode power regulator according to claim 1, further comprising an integrated circuit (IC) having a single pin for receiving both information relating to an input voltage to the primary circuit in a first period of time in which energy is stored in the energy storing device (3) and information relating to an output voltage from the secondary circuit in a second period of time in which energy is released from the energy device (3)."

	Ex. 1004, Claim 10: "A method according to claim 9, wherein the monitoring circuit provides a control signal in response a measured level of the input and output voltages, said control signal relating to the input voltage in the first period of time, and said control signal relating to the output voltage in the second period of time." *See* citations to Mobers in Section IV.A. *See also* Ex. 1004, Abstract, 1:5-13, 3:60-67, 5:14-19, 5:20-25, 5:56-57.

Claim 1[c]: "a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and"

Mobers discloses a latch (i.e., a switching control) that controls switch S1 (i.e., the power switch) to regulate V_{out} (i.e., an output of the power converter). As explained with reference to Figure 6, the output voltage (V_{out}) of the switched power supply is controlled by regulating the conduction time of the switch, and thereby the amount of energy that is transferred from the primary side to the secondary side of the converter. Ex. 1004, 4:37-51; *see also id.*, 1:36-54. In turn, Figure 7 illustrates the switching control latch inside the controller circuit that turns the power switch on and off:



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 82. Mobers discloses:

> [T]he switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off.

Ex. 1004, 5:26-33.

The switching control latch shown in Figure 7 controls switch S1 to regulate the output voltage. *See id.*, 5:26-62. And as shown in the above annotation of

Figure 7, the switching control latch is responsive to the sensor via both the over power protection circuit and the output over voltage protection circuit.

During operation, the switch is turned on when a set signal from oscillator 21 sets the switching control latch. *See id.*, 5:27-28, Fig. 7. However, if the level of V_{out} detected by the sensor during the off-time of the switch exceeds a predetermined level, the over voltage protection latch sends a fault signal to the logic gate located between oscillator 21 and the switching control latch. *See id.*, 5:57-62, Fig. 7; Ex. 1002, ¶ 84. When the fault signal is asserted, the logic gate blocks set signals that would otherwise be transmitted from oscillator 21 to the switching control latch, thereby preventing switch S1 from being turned on during subsequent switching cycles. Ex. 1004, 5:59-62; Ex. 1002, ¶ 84.

In addition, the output power protection circuit may determine when switching control latch turns off switch S1 during a given switching cycle based on V_{line} information from the sensor. Ex. 1002, ¶¶ 85-86. As shown in Figure 7, the current through switch S1 is monitored by comparator 23, which is coupled to sense resistor R2. Ex. 1004, 5:30-31, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across sense resistor R2 (which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. And, as described in Mobers, the over power protection circuit adjusts the peak current threshold provided by minimum circuit 21 based on information from the sensor relating to V_{line}. *Id.*, 5:34-50, Fig. 7; Ex. 1002, ¶ 85.

Specifically, curve circuit 24 processes the input line voltage information from the sensor and passes a threshold level to minimum circuit 26. Ex. 1004, 5:34-45. When the signal from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold from curve circuit 24 to comparator 23. *See id.*, 5:46-50, Fig. 7. This limits the peak current through switch S1 during the on-time of a given switching cycle as a function of the input line voltage, thereby preventing the amount of power passed to the output from exceeding a maximum safe level. *Id.*, 5:46-50, Fig. 7; *see also id.*, Abstract, 1:5-13, 2:50-53, 3:60-62. Accordingly, the switching control in Mobers is coupled to switch the power switch to regulate the output voltage V_{out} in response to the sensor via both the output over voltage protection circuit and the over power protection circuit. Ex. 1002, ¶ 86.

This mapping of claim element 1[c] to the Mobers prior art is analogous to Patent Owner's mapping of this element[9] in its infringement contentions for the Delaware Litigation. *See* Ex. 1012, 5-7. As discussed above in Section V.A, Patent Owner's infringement contentions identify both the over power protection circuit and the output over voltage protection circuit in the accused product as

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[9] The claim element labeled 1[c] herein is labeled as claim element 1[d] in Patent Owner's infringement contentions. *See* Ex. 1012, 5-7.

inputs to the switching control coupled to switch the power switch to regulate the output voltage. Ex. 1012, 5-7. Thus, Mobers discloses claim element 1[c] in the same manner as compared to Patent Owner's alleged mapping of the products accused in the Delaware Litigation. Ex. 1002, ¶ 87.

Mobers therefore discloses each limitation of claim element 1[c]. *Id.*, ¶¶ 82-87.

[1c] a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and	*See* citations for claim elements 1[a]. Ex. 1004, 3:6-17: "The switched-mode power supply according to the first aspect of the present invention may further comprise a <u>control circuit for controlling the controllable current switching means</u>. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. <u>The control circuit typically response [sic] to a control signal from the third winding</u>. This control signal may comprise a information relating to the performance or status of the switched mode power supply. Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." (emphasis added). Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection <u>by operating the gate driving circuit in an appropriate way</u>." (emphasis added). Ex. 1004, 3:60-67: "This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}. Additionally, the control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details

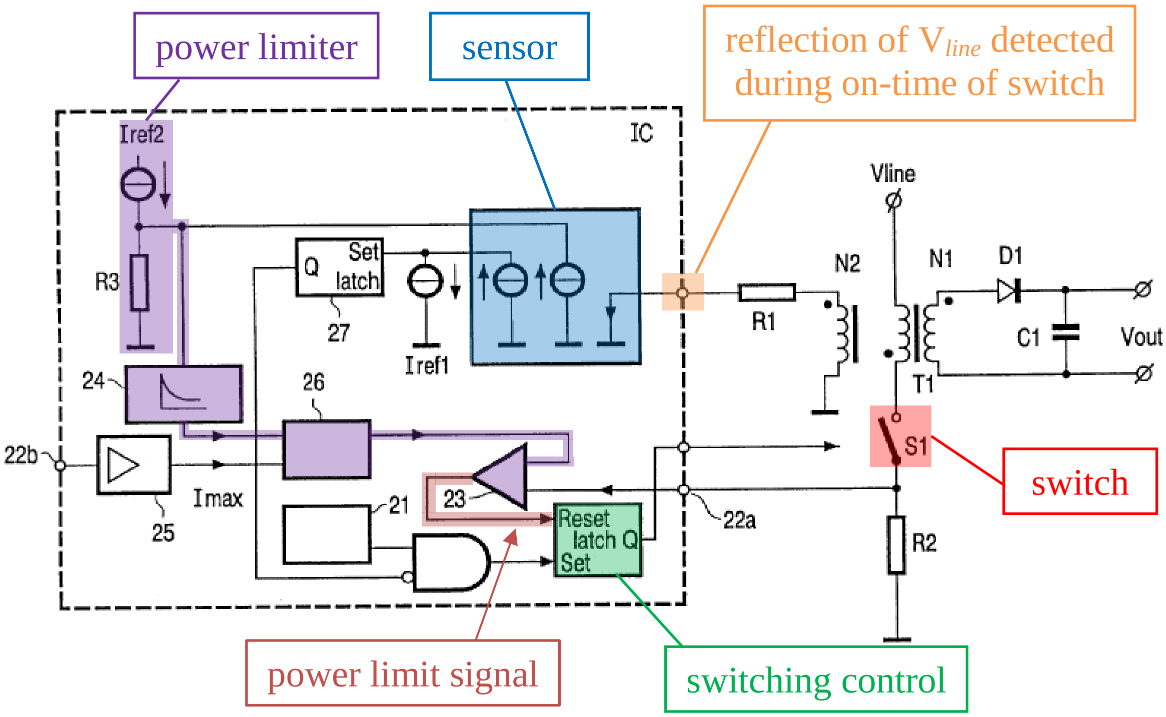
	below, the sensing of V_{line} and the monitoring of V_{out} is performed in a time phased way." Ex. 1004, 5:26-62: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off. Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used. This information is retrieved from the control winding N2 of the transformer. The V_{line} information is processed in the 'curve' circuit 24. The processor is a multiplier that transforms the input signal into the square root of the signal. The square root is taken, because for this system the optimum compensation will be made. Alternatively, a linear function will also do, but then the maximum output power still has quite some V_{line} dependence. The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22b. The magnitude of both signals is sensed by the minimum (min.) circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information. As previously mentioned, information relating to V_{out} is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply

	in case of an over voltage being present on the output terminals." Ex. 1004, 4:37-51: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown [in Fig. 6]). I_p is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown [in Fig. 6]), which—in response the control signal—controls the conduction time of switch 16. Upon switching switch 16 on I_p starts to build up in the primary circuit 1. When I_p reaches a predetermined level, switch 16 is turned off. After switching switch 16 off the energy stored in transformer 3 is transferred to the secondary circuit 2. This energy transfer induces a current Is in the secondary circuit 2." Ex. 1004, 1:36-65: "The level of V_{out} is controlled by controlling the current in the primary circuit, I_p, using the controllable switch 4. I_p is determined by measuring a voltage drop across resistor 5. The measured voltage drop—which represents I_p—is provided as a control signal to a Pulse Width Modulator (PWM) circuit. The PWM-circuit adjusts the conduction time of the controllable switch 4 so as to obtain a predetermined current value. Typically, the controllable switch 4 is a transistor. The primary winding of the transformer has the inductance L. When the PWM-circuit switches the transistor on, I_p starts to build up in the primary circuit. The increase of I_p during t_{on} (t_{on} is the conduction time of the transistor) is illustrated in FIG. 2. FIG. 2 also illustrates the voltage across the controllable switch 4 and the current in the secondary circuit, I_s. The dashed line shows V_{line}. The controllable switch is switched off when I_p has reached a predetermined value. Thus, the conduction time is dependent on the predetermined level of the I_p—i.e. increasing the level of I_p increases the conduction time. For obvious reasons the conduction time is also dependent on

	the level of the input voltage and the inductance, L, of the primary winding of the transformer. When the predetermined level of I_p has been reached the controllable switch 4 is turned off, and the magnetically stored energy in the transformer 3 is transformed to the secondary circuit 2. The transformation of energy to the secondary circuit induces a current, Is, in the secondary circuit. I_s is rectified using e.g. the diode based rectifier and the capacitor 7 in combination." *See also* Ex. 1004, Abstract, 1:5-13, 2:51-55, 3:6-32, 4:37-44, 5:20-25, 5:34-6:3; Figs. 1-4 and 6-8; Claims 1, 3, 8-11.

Claim 1[d]: "a power limiter coupled to the sensor to output a power limit signal to the switching control in response to the line input voltage of the power converter, wherein the switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal"

As described above for claim element 1[b], the signal received by the sensor from resistor R1 represents the input line voltage (V_{line}) of the power converter during the on-time of switch S1. *See* Ex. 1004, 5:50-55. Mobers utilizes this input line voltage information to implement over power protection. Ex. 1004, 3:60-62, 5:26-45. The over power protection circuitry limits the on-time of the switch when the input line voltage V_{line} is high to prevent too much power from being transferred from the input to the output. Ex. 1002, ¶ 88.



Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 88.

Figure 7 of Mobers illustrates that a pulse from oscillator 21 sets the switching control latch to turn on switch S1 during each switching cycle (assuming no output over voltage fault condition). Ex. 1004, 5:27-28, Fig. 7. Comparator 23 resets the switching control latch to turn off switch S1 when the voltage across resistor R2 (which represents the current through switch S1 and resistor R2) exceeds a threshold. *See id.*, 5:28-33, Fig. 7. The threshold for comparator 23 is set by minimum circuit 26. *Id.*, 5:48-50, Fig. 7. During normal conditions, minimum circuit 26 passes the feedback signal from error amplifier 25 to comparator 23. *See id.*, 5:46-50, Fig. 7. This forms what is known in the art as a current mode control loop, whereby the switch is turned off during each cycle when the current through the power switch reaches a threshold that is based on feedback from the output voltage. Ex. 1013, 16-18; Ex. 1002, ¶ 89.

However, when the input line voltage is high, the over power protection system intervenes by limiting the peak current set point as a function of the input line voltage. Based on the line voltage information from the sensor, curve circuit 24 passes a threshold level to minimum circuit 26. Ex. 1004, 5:34-45. As depicted by the curve inside curve circuit 24 in Figure 7, curve circuit 24 provides lower threshold values to minimum circuit 26 at higher input line voltages. *Id.*, Fig. 7, 5:38-45; Ex. 1002, ¶ 90. When the threshold value from curve circuit 24 is less than the feedback signal from error amplifier 25, minimum circuit 26 passes the threshold value from curve circuit 24 to comparator 23. *See* Ex. 1004, 5:46-50, Fig. 7. Based on a comparison of switch current and the threshold from curve circuit 24, comparator 23 outputs a power limit signal that determines when to reset the switching control latch to turn off switch S1. *Id.*, 5:26-33, 5:46-50, Fig. 7.

Power is equal to voltage times current. Ex. 1002, ¶ 91. Thus, by limiting the input current through switch S1 as a function of the input line voltage, Mobers limits the amount of power passed from the input to the output of the converter. *Id.*, 5:34-50, Fig. 7; *see also id.*, Abstract.

This mapping of claim element 1[d] to the Mobers prior art is analogous to Patent Owner's mapping in its infringement contentions for the Delaware

Litigation.[10] *See* Ex. 1012, 8-9. Specifically, Patent Owner alleges that the accused product "includes a power limiter that implements over power protection ('OPP') that reduces the peak current set point of the switching control in response to sensing the signal representative of the input voltage … ." *Id.*, 8. Moreover, Patent Owner alleges that the accused device includes a "power limit signal" at the output of a comparator, which is similarly situated to comparator 23 in Mobers to reset a PWM latch. *Id.*, 9. Thus, Mobers discloses claim element 1[d] in the same manner as compared to Patent Owner's alleged mapping of the products accused in the Delaware Litigation. Ex. 1002, ¶ 93.

Accordingly, Mobers discloses each limitation of claim element 1[d]. Ex. 1002, ¶¶ 88-93.

[1d] a power limiter coupled to the sensor to output a power limit signal to the switching control in response to the line input voltage of the power converter, wherein the switching control is further coupled	*See* citations for claim elements 1[b]-[c]. Ex. 1004, Abstract: "The present invention relates to a switched-mode power supply comprising a transformer (T1) having an additional control winding (N2). This control winding (N2) forms part of an over power protection system by providing information relating to the line voltage V_{line}." Ex. 1004, 3:60-62: "This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}." Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored in order to provide over voltage protection in

[10] The claim element labeled 1[d] herein is labeled as claim element 1[e] in Patent Owner's infringement contentions. Ex. 1012, 8-9.

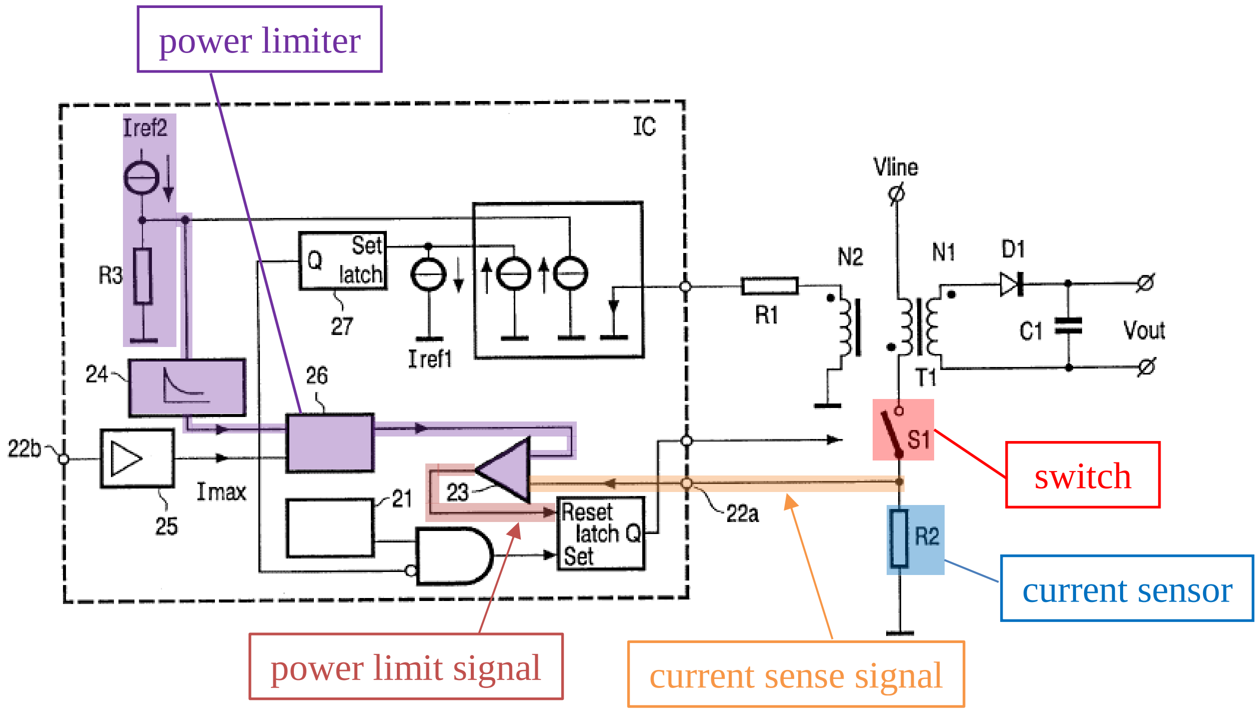
to switch the power switch to regulate the output of the power converter in response to the power limit signal.	the secondary circuit 2, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." Ex. 1004, 5:46-55: "The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22 b. The magnitude of both signals is sensed by the minimum (min.) circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining both types of information." Ex. 1004, 3:6-17: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means. The control circuit may comprise a PWM-circuit operating the switch at a frequency between 25-250 kHz. The control circuit typically response to a control signal from the third winding. This control signal may comprise a information relating to the performance or status of the switched mode power supply. Preferably, the control signal relates to the input voltage to the power supply in the first period of time. In the second period of time the control signal relates to the output voltage of the power supply." Ex. 1004, 4:37-44: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown). I_p

	is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown), which—in response the control signal—controls the conduction time of switch 16." *See* citations to Mobers in Section IV.A. *See also* Ex. 1004, Abstract, 2:51-61, 3:58-62, 5:5-10, 5:34-55; 5:63-6:3; Figs. 6-8; Claims 1, 3, 9-11.

2. Claim 2

Claim 2[a]: "The controller of claim 1, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch,"

Mobers discloses that the over power protection circuit (i.e., the power limiter) is further coupled to receive a current sense signal from resistor R2 (i.e., the current sensor), as shown in Figure 7. Ex. 1004, 5:34-45, Fig. 7. Because resistor R2 (i.e., the current sensor) is coupled in series with switch S1 (i.e., the power switch), the voltage generated across resistor R2 is indicative of the switch current, and therefore serves as a current sense signal. *Id.*, 5:26-33, Fig. 7. Indeed, "the peak current through S1 is sensed by sensing the voltage across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *Id.*, 5:30-33.



Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 94.

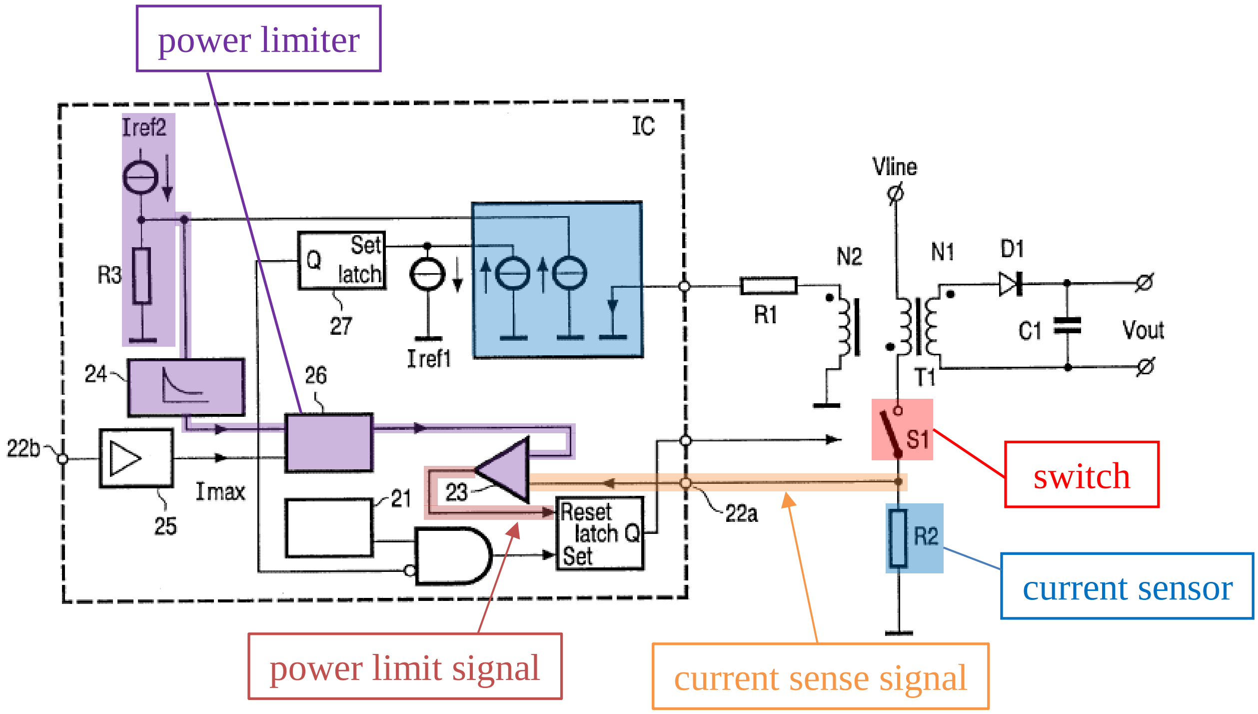
As described directly above, resistor R2 (i.e., the current sensor) in Mobers is coupled in series with switch S1, and thus generates voltage that is indicative of the current through switch S1. This is similar to the description of a switch current sensor in the ’871 Patent itself: “Any of the many know (sic) ways to measure switch current I_{SWITCH} 135, such as for example a current transformer, or the ***voltage across a discrete resistor***, or the voltage across a transistor when the transistor is conducting, may be implemented with current sensor 224.” Ex. 1001, 5:52-56 (emphasis added).

Accordingly, Mobers discloses each limitation of claim element 2[a]. Ex. 1002, ¶¶ 94-96.

2[a]. The controller of claim 1, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch,	*See* citations for Claim 1. Ex. 1004, 3:26-32: "Preferably, the controllable current switching means is connected in series with the primary winding of the transformer. In order to determine the current flowing in this circuit a resistor is included within the circuit so that the current may be determined by measuring the voltage generated across this resistor." Ex. 1004, 4:37-44: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown [in FIG. 6]). I_p, is sensed by measuring the voltage generated across resistor 5. The measured voltage is used as a control signal to the gate driving circuit (not shown [in FIG. 6]), which—in response the control signal—controls the conduction time of switch 16." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." *See also* Ex. 1004, 3:21-25, 4:52-5:4, Figs. 6-8.

Claim 2[b]: "wherein the power limiter is further coupled to output the power limit signal in response to the current sense signal."

Mobers discloses that the power limiter is further coupled to output the power limit signal in response to the current sense signal. As described with reference to Figure 7, "the peak current through S1 is sensed by sensing the voltage across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off.” Ex. 1004, 5:30-33.



Ex. 1004, Fig. 7 (annotations added). As shown in Figure 7, comparator 23 compares the current sense signal detected across R2. If the current sense signal exceeds the peak current determined by the power limiter, comparator 23 sends the power limit signal to the switching control to turn off switch S1.

Accordingly, Mobers discloses each limitation of claim element 2[b]. Ex. 1002, ¶¶ 97-98.

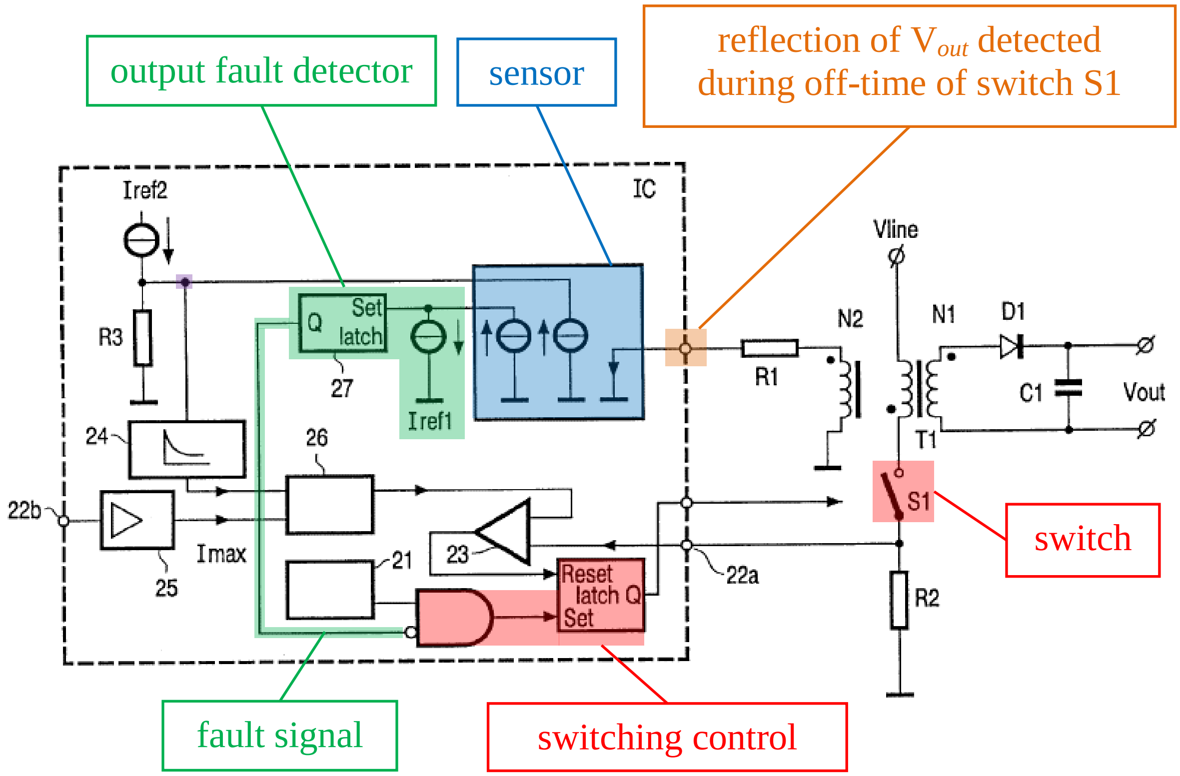
[2b] wherein the power limiter is further coupled to output the power limit signal in response to the current sense	*See* citations for Claim 1. Ex. 1004, 5:26-33: “Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. <u>The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current</u>

signal.	through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." (emphasis added). Ex. 1004, 5:34-52: "Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used. This information is retrieved from the control winding N2 of the transformer. The V_{line} information is processed in the 'curve' circuit 24. The processor is a multiplier that transforms the input signal into the square root of the signal. The square root is taken, because for this system the optimum compensation will be made. Alternatively, a linear function will also do, but then the maximum output power still has quite some Vline dependence. The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22b. The magnitude of both signals is sensed by the minimum (min.) circuit 26. As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke … ." *See* citations for claim element 2[a]. *See also* Ex. 1004, 3:14-17, 3:26-32, 4:37-44, 5:34-45, 5:63-6:3, Figs. 6-8.

3. Claim 3

Claim 3. The controller of claim 1 further comprising an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition.

Mobers discloses an over voltage protection circuit (i.e., an output fault detector) coupled between the sensor and the switching control latch:



Id., Fig. 7 (annotations added); *see also id.*, Ex. 1004, 4:52-5:5, 5:56-62.

As shown in Figure 7, the sensor monitors the current from resistor R1, which represents V_{out} during at least a portion of the off-time of the switch. Ex. 1004, 5:50-53. The sensor mirrors the current representative of V_{out} for comparison to a reference "Iref1." Ex. 1004, Fig. 7. If the current signal representing V_{out} exceeds "Iref1," then an output over voltage condition is detected and latch 27 is set. *See id.* The reference "Iref1" and latch 27 thus serve as an output fault detector. Ex. 1002, ¶¶ 99-100. If an over voltage condition is detected, latch 27 sends a signal (i.e., a fault signal) to the logic gate shown in Figure 7 between oscillator 21 and the switching control latch. *See* Ex. 1004, Fig. 7. In turn, the logic gate (which is also part of the switching control) blocks pulses from oscillator 21 to the switching control latch, thereby preventing the switching control latch from turning on switch S1 when an output over voltage fault condition is detected. *See id.*, Fig. 7, 5:57-62 ("If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals."). Ex. 1002, ¶ 100.

Accordingly, Mobers discloses each limitation of Claim 3. Ex. 1002, ¶¶ 99-101.

3. The controller of claim 1 further comprising an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power	*See* citations for Claim 1. Ex. 1004, 2:51-53: "Advantageously, an integrated circuit is provided with an integrated over voltage and over power protection circuit without the use of additional die demanding external components." Ex. 1004, 3:58-67: "In its simplest form, the present invention provides a switched-mode power supply comprising a transformer having a control winding. This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}. Additionally, the control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out} is performed in a time phased way."

converter and to output a fault signal to the switching control in response to the detection of the fault condition.	Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out} is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 5:63-6:3: "An implementation of the switched power supply according to the present invention is shown in FIG. 8. The over voltage protection circuit is block 17 whereas block 15 and 18 in combination forms the over power protection circuit. Terminal 28 is to be connected to the left leg of resistor R1 in FIG. 7. It will be evident for the skilled person in the art that there are several ways of implementing the over voltage protection circuit and the over power protection circuit." *See also* Ex. 1004, Abstract, 2:51-53, 5:50-55, Figs. 6-8.

4. Claim 6

Claim 6: The controller of claim 3 wherein the output fault detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter.

As described above for Claim 3, the fault condition that the output fault detector in Mobers is coupled to detect is an output over voltage fault condition. *See supra* Section VI.A.3, Claim 3; *see also* Ex. 1004, 5:56-62, 3:62-65. Accordingly, Mobers discloses each limitation of Claim 6. Ex. 1002, ¶ 102.

6. The controller of claim 3 wherein the output fault	*See* citations for Claims 1 and 3. Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out}. is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a

detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter.	latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 3:58-67: "[T]he present invention provides a switched-mode power supply comprising a transformer having a control winding. … [T]he control winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out}. is performed in a time phased way." (emphasis added). Ex. 1004, 5:63-6:3: "An implementation of the switched power supply according to the present invention is shown in FIG. 8. The over voltage protection circuit is block 17 whereas block 15 and 18 in combination forms the over power protection circuit. Terminal 28 is to be connected to the left leg of resistor R1 in FIG. 7. It will be evident for the skilled person in the art that there are several ways of implementing the over voltage protection circuit and the over power protection circuit." Ex. 1004, 2:51-53: "Advantageously, an integrated circuit is provided with an integrated over voltage and over power protection circuit without the use of additional die demanding external components." *See also* Ex. 1004, Abstract, 2:51-53, 5:50-55, Figs. 6-8.

5. Claims 8, 12, 14, and 15

Claims 8, 12, 14, and 15 collectively include similar subject matter as recited in Claims 1, 2, 3, and 6 (albeit with a different ordering of the elements). Thus, according to the following mapping, Claims 8, 12, 14, and 15 are disclosed in the same manner as described above for Claims 1, 2, 3, and 6. Ex. 1002, ¶ 103.

Claim elements 8[pre],[11] [a], and [c] are identical to claim elements 1[pre], [a], and [c]. Further, claim element 8[b] is identical to claim element 1[b], aside from the addition of "at least" prior to the common phrase "a portion of an on time of the power switch," which does not narrow the scope of the claim. In addition, claim element 8[d] recites the same subject matter as Claim 3. Thus, Claim 8 is disclosed by Mobers in the same manner as described above for Claims 1 and 3. Ex. 1002, ¶ 104.

Moreover, dependent Claims 12, 14, and 15 recite the same subject matter as Claim 6, claim element 1[d], and Claim 2, respectively. Thus, dependent Claims 12, 14, and 15 are disclosed by Mobers in the same manner as described above. Ex. 1002, ¶ 105.

8[pre]. A controller for use in a power converter, comprising:	*See* Section VI.A.1, Claim 1[pre].
[8a] a sensor coupled to receive a signal from a single terminal of the controller,	*See* Section VI.A.1, Claim 1[a].
[8b] the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage during at least a portion of an on time of the power switch,	*See* Section VI.A.1, Claim 1[b].
[8c] a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and	*See* Section V.A.1, Claim 1[c].

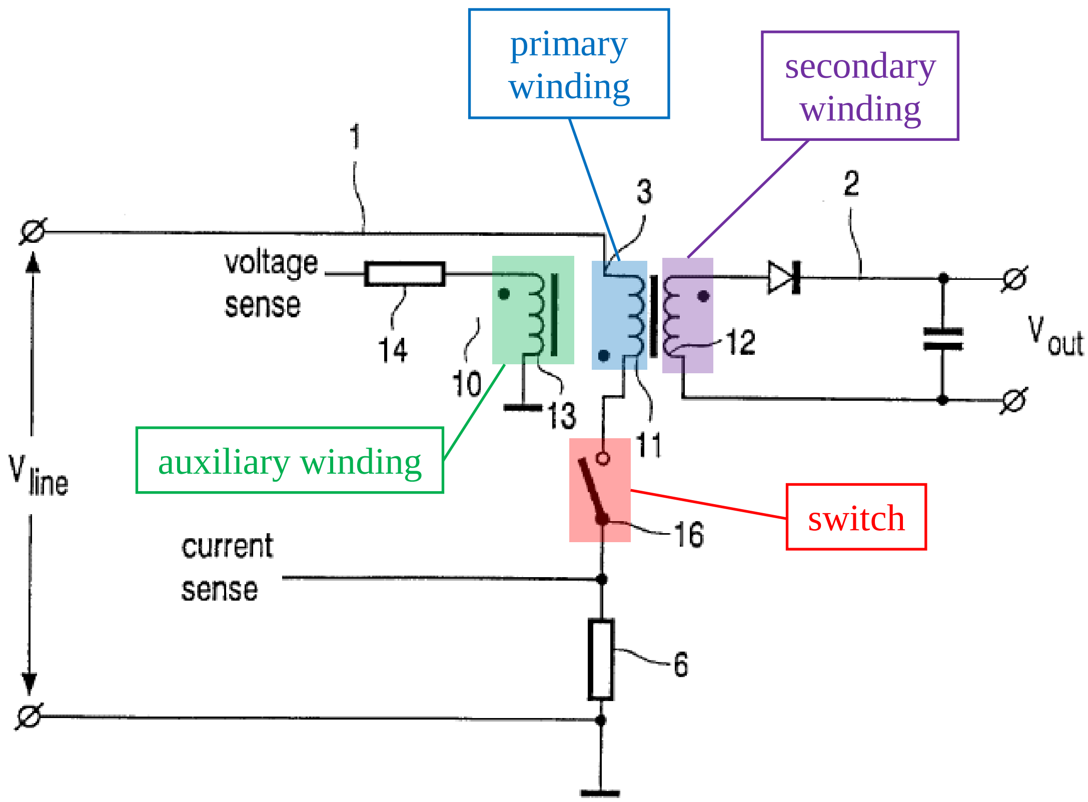
[11] The preamble is not limiting but is nonetheless disclosed by Mobers.

[8d] an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition.	*See* Section VI.A.3, Claim 3.
12. The controller of claim 8 wherein the output fault detector is coupled to detect an output over voltage fault condition in response to the signal representative of the output voltage of the power converter.	*See* Section VI.A.4, Claim 6.
14. The controller of claim 8 further comprising a power limiter coupled between the sensor and the switching control, the power limiter coupled to output a power limit signal to the switching control in response to the signal representative of line input voltage of the power converter, wherein the a switching control is further coupled to switch the power switch to regulate the output of the power converter in response to the power limit signal.	*See* Section VI.A.1, Claim 1[d].
15. The controller of claim 14, wherein the power limiter is further coupled to receive a current sense signal from a current sensor, wherein the current sense signal is generated in response to a switch current in the power switch, wherein the power limiter is further coupled to output the power limit signal in response to the current sense signal.	*See* Section VI.A.2, Claim 2.

B. Ground 2: Claims 1-3, 6, 8, 12, 14 and 15 Are Obvious Over Mobers Under 35 U.S.C. § 103

Mobers, combined with the knowledge of a person of ordinary skill in the art, discloses and suggests each element of Claims 1-3, 6, 8, 12, 14, and 15, and thus renders those claims obvious under 35 U.S.C. § 103. Ex. 1002, ¶ 106.

Mobers discloses a flyback-type switching power converter that utilizes a transformer with an auxiliary winding, which is referred to by Mobers as a "control winding." Ex. 1004, 4:1-28, Fig. 6. Figure 6 illustrates certain components of the switching power converter:



Ex. 1004, Fig. 6 (annotations added); Ex. 1002, ¶ 107.

In one section, Mobers states that "the control voltage generated across the control winding 13 is related to V_{line} during the conduction time (primary stroke)" (i.e., during the on-time of switch 16), and is "related to V_{line} during the non-conduction time (secondary stroke)" (i.e., during the off-time of switch 16). Ex. 1004, 5:10-13 (bold emphasis added). This snippet of text refers to "V_{line}"

twice. However, Petitioner's expert has identified the second instance of "V_{line}" in column 5, lines 10-13 as a typographical error that should instead be "V_{out}." Ex. 1002, ¶ 108.

As explained in Sections III.A-C, a person of ordinary skill in the art ("POSITA") would understand that an auxiliary winding in a flyback-type switching power converter naturally reflects the voltage present on the secondary winding (i.e., Vout plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). *See* Ex. 1002, ¶ 109; Ex. 1006, 3:4-15; Ex. 1008, 7:31-43. Moreover, other portions of Mobers clarify that "the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke." Ex. 1004, 5:50-53; *see also id.*, 4:52-5:5.

Thus, regardless of the misstatement in column 5, lines 10-13, of Mobers, a POSITA would understand Mobers to disclose and suggest the sensing of both the output voltage and the line input voltage via a single terminal of a controller IC at different times during the switching cycle. *See* Ex. 1004, 5:50-53, Figs. 6-7; Ex. 1002, ¶ 110. Moreover, Mobers discloses and suggests every other limitation of Claims 1-3, 6, 8, 12, 14, and 15 of the '871 Patent according to the mapping provided in Sections VI.A.1-5. Therefore, Mobers renders Claims 1-3, 6, 8, 12, 14, and 15 obvious to a person of ordinary skill in the art under 35 U.S.C. § 103. Ex. 1002, ¶ 110.

C. Ground 3: Claim 11 is Obvious Over Mobers Under 35 U.S.C. § 103

Mobers, combined with the knowledge of a person of ordinary skill in the art, discloses and suggests each element of Claim 11 and thus renders Claim 11 obvious under 35 U.S.C. § 103. *See* Ex. 1002, ¶ 111.

Claim 11 depends from Claim 8[12] and further recites: "wherein the output fault detector is coupled to detect an ***open loop condition fault condition*** in response to the signal representative of the output voltage of the power converter." Ex 1001, Claim 11 (emphasis added). The '871 specification does not define what is meant by an "open loop condition fault condition," or provide any examples of and open loop fault condition.[13] As explained by Petitioner's expert, however, a POSITA would understand that an open loop fault condition occurs when the feedback path from the output of the power supply to the control circuitry is broken. *See* Ex. 1002, ¶ 112. In other words, the normal closed-loop control is

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[12] As discussed above in Section VI.A.5 (which in turn points to Sections VI.A.1 and VI.A.3), Mobers discloses each limitation of Claim 8.

[13] To the extent that the '871 Patent relies on the knowledge of a POSITA to understand an "open loop condition," that same knowledge of a POSITA would also be applied to the prior art analysis.

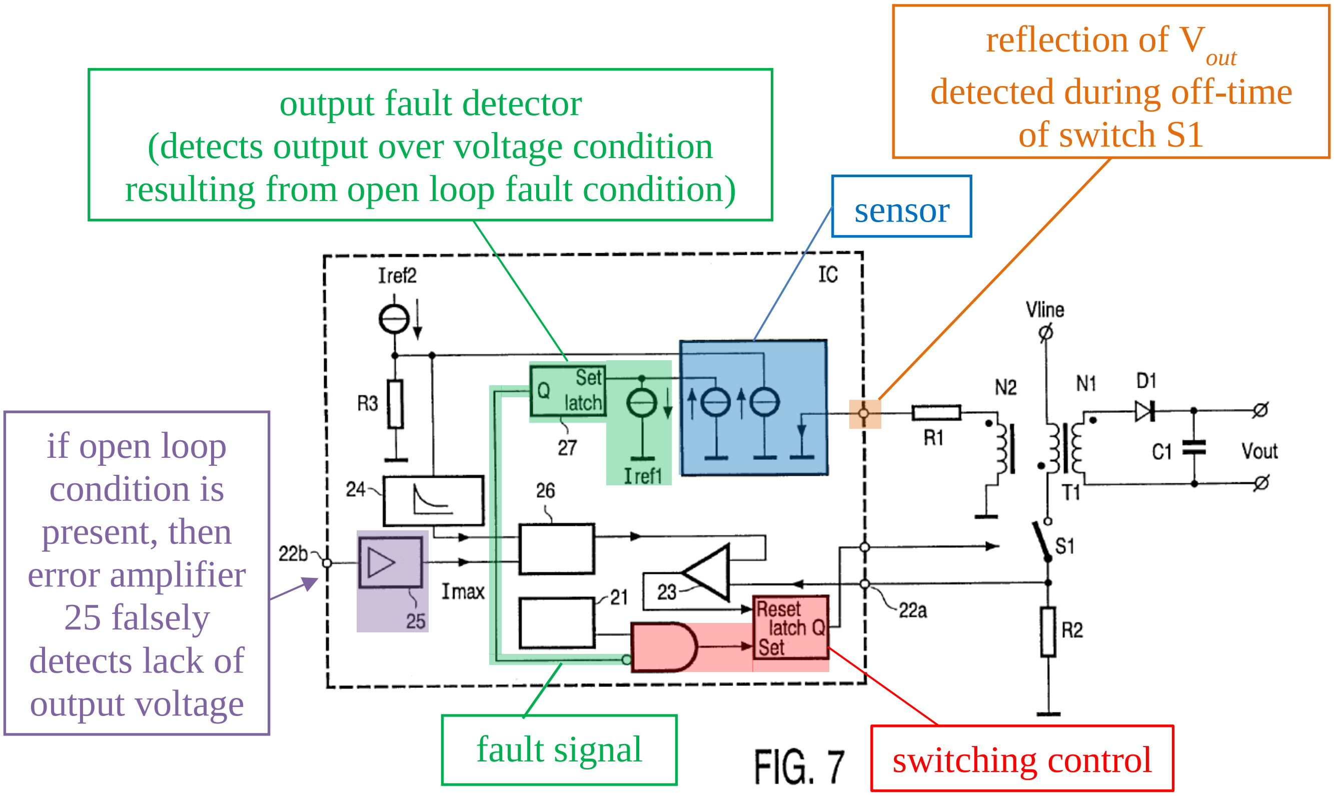
"opened" by a break in the feedback from the output of the power converter to the control circuitry. *Id.*

Because the feedback loop is broken, the control circuitry falsely detects that no voltage is present on the output of the power supply. *Id.*, ¶ 113. The control circuitry therefore attempts to provide more power to the output of the power supply. This additional power, in turn, causes an over voltage fault condition on the output. Ex. 1002, ¶ 113; Ex. 1020, 10 ("[T]he output of the switcher will go high if the feedback loop is opened."); Ex. 1017, 4:53-62 (describing "conventional open loop protection circuit" configured "to prevent any overvoltage" if feedback line is broken); Ex. 1018, 1:16-19 (referring to "an over-high output voltage during the period of feedback open loop"); Ex. 1019, 1:26-31 (describing a regulator circuit that responds to an "open loop condition on the feedback" by "delivering maximum power" to the output).

In other words, an output over voltage fault condition may be a symptom of an open loop fault condition. Indeed, the background of Mobers itself refers to an output over voltage condition caused by broken feedback loop. Ex. 1004, 2:41-44 ("In case such a loop is broken no information relating to the output voltage is available, and thus, no protection against damages due to over voltage on the secondary circuit is available."). Thus, as would be readily recognized by a POSITA, a circuit for detecting an output over voltage fault condition also detects the open loop condition that causes the output over voltage in the first place. Ex. 1002, ¶ 114.

Mobers discloses terminal 22b coupled to error amplifier 25, which in turn is coupled to comparator 23 via minimum circuit 26. Ex. 1004, 5:26-33, 5:46-48, Fig. 7. Error amplifier 25 is configured to receive a feedback signal from the output of the power supply. *Id.*, Fig. 7, 5:26-55; Ex. 1002, ¶ 115. When the error signal is lower than the output curve circuit 24 in the over power protection circuitry, minimum circuit 26 uses the error signal generated by error amplifier 25 to set the threshold for comparator 23, and thereby the peak current through switch S1. Ex. 1004, 5:26-33, 5:46-48, Fig. 7. Thus, the feedback from pin 22b and error amplifier 25 forms what is commonly known in the art as a current-mode feedback control loop. Ex. 1013, 16-18; Ex. 1002, ¶ 115.

And as described above, a POSITA would understand that an output over voltage fault condition may occur in response to an open loop fault condition in the feedback path. For example, if an open loop condition occurred at feedback pin 22b, the error amplifier 25 would falsely detect a lack of output voltage and cause the control circuitry to provide additional power to the output of the power supply. Ex. 1002, ¶ 116. This additional power, in turn, would cause an output over voltage condition. *Id.*



Ex. 1004, Fig. 7 (annotations added).

As described above for Claim 12, Mobers discloses that the output fault detector is coupled to detect an output over voltage fault condition via the control winding N2. *See supra* Section VI.A.5, Claim 12 (which in turn points to Section VI.A.4, Claim 6). Thus, a POSITA would recognize that in the event of an open loop condition (in the feedback path including error amplifier 25), Mobers's output fault detector would detect the open loop condition by detecting the resulting over voltage condition via the control winding. Ex. 1002, ¶¶ 116-117.

Accordingly, the circuitry disclosed by Mobers, combined with the knowledge of a POSITA, discloses and suggests each limitation of Claim 11. Ex. 1002, ¶¶ 112-117.

11. The controller of claim 8 wherein the output fault detector is coupled to detect an open loop condition fault condition in response to the signal representative of the output voltage of the power converter.	*See* citations in Section VI.A.5, Claim 12 (citing Section VI.A.4, Claim 6). Ex. 1004, 2:38-44: "It is a further disadvantage of the prior art power supplies shown in FIGS. 1 and 5 that in order to obtain information relating to the output voltage a separate feedback loop/control loop must be implemented. In case such a loop is broken no information relating to the output voltage is available, and thus, no protection against damages due to over voltage on the secondary circuit is available." Ex. 1004, 5:56-62: "As previously mentioned, information relating to V_{out}. is available during the secondary stroke. If it is determined that V_{out} comes above a predetermined level a latch is set in circuit 27. This latch prevents switch S1 from switching on again so as to shut down the switched-mode power supply in case of an over voltage being present on the output terminals." Ex. 1004, 3:58-67: "[T]he present invention provides a switched-mode power supply comprising a transformer having a control winding. … [T]he control winding forms part of an <u>over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply</u>. As it will be explained in further details 65 below, the sensing of V_{line}, and the monitoring of V_{out}. is performed in a time phased way." (emphasis added).

VII. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the ’871 Patent be instituted and that Claims 1, 2, 3, 6, 8, 11, 12, 14, and 15 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,
BAKER BOTTS L.L.P.

September 28, 2018
Date

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Lead Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 13653 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

September 28, 2018
Date

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 28th day of September, 2018, a complete and entire copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,773,871** and any accompanying exhibits was served on the patent owner at the correspondence address of record for the subject patent,

James Go
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via Express Mail or by means at least as fast and reliable as Express Mail. Additionally, the same were also served upon counsel for the subject patent's owner, Power Integrations, Inc.,

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because that is likely to affect service.

In accordance with § 42.51(b)(1), the undersigned certify that Petitioner is not aware of, and therefore does not provide any "relevant information that is inconsistent with a position advanced by petitioner[]."

September 28, 2018 /Roger Fulghum/

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