UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

Case No. Unassigned
Patent 8,773,871

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,773,871

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LIST OF EXHIBITS

1001	U.S. Patent No. 8,773,871 to Djenguerian et al. ("the '871 Patent")
1002	Expert Declaration of Dr. R. Jacob Baker
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1004	U.S. Patent No. 6,542,386 ("Mobers")
1005	David A. Johns and Ken Martin, Analog Integrated Circuit Design (John Wiley & Sons, Inc., 1997)
1006	U.S. Patent No. 7,016,204 ("Yang")
1007	U.S. Patent Application Publication 2005/0254268 ("Reinhard")
1008	U.S. Patent No. 5,831,839 ("Pansier")
1009	*ON Semiconductor Corp. v. Power Integrations, Inc.*, 17-cv-00247-LPS-CJB, Power Integration's Answer and Counterclaims to Plaintiffs' First Amended Complaint (D. Del. Sept. 29, 2017) (D.I. 34)
1010	Excerpts of File History for U.S. Patent No. 8,077,483 (parent of '871 Patent)
1011	*ON Semiconductor Corp. v. Power Integrations, Inc.*, 17-cv-00247-LPS-CJB, Amended Joint Claim Construction Chart (D. Del. May 22, 2018) (D.I. 78 and 78-1)
1012	**(CONFIDENTIAL)** *ON Semiconductor Corp. v. Power Integrations, Inc.*, 17-cv-00247-LPS-CJB, Power Integrations Infringement Contentions (D. Del. Jan. 5, 2018), Exhibit E, Claim Chart for '871 Patent
1013	Reserved[1]

[1] Exhibit numbers 1013 and 1017-1020 are reserved to maintain consistent numbering for other exhibits that are also filed with concurrently filed Petition for the '871 Patent.

1014	Paul Horowitz and Winfield Hill, *The Art of Electronics* (Cambridge University Press, 2nd ed. 1989) (reprinted 1998)
1015	U.S. Patent 6,061,257 ("Spampinato")
1016	U.S. Patent 4,447,841 ("Kent")
1017	Reserved
1018	Reserved
1019	Reserved
1020	Reserved
1021	European Patent Application EP0698960 ("Mohandes")
1022	U.S. Patent 7,447,601 ("Lhermite")
1023	U.S. Patent 5,949,154 ("Williams")

I. INTRODUCTION

Semiconductor Components Industries, LLC d/b/a ON Semiconductor ("ON Semiconductor" or "Petitioner") requests *inter partes* review ("IPR") under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq*. of Claims 9, 10, and 13 of U.S. Patent No. 8,773,871 ("'871 Patent").

Petitioner asserts that there is a reasonable likelihood that the challenged claims are unpatentable and requests review of, and cancellation of, the challenged claims under 35 U.S.C. § 103.

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices

Real Party in Interest: The real parties in interest are: (i) ON Semiconductor Corporation, (ii) Semiconductor Components Industries, LLC, doing business as ON Semiconductor, and (iii) Fairchild Semiconductor International, Inc., (iv) Fairchild Semiconductor Corporation, (v) Fairchild (Taiwan) Corporation, and (vi) System-General Corporation.

Related Matters: The '871 Patent is involved in a pending lawsuit entitled *ON Semiconductor Corp., et al. v. Power Integrations, Inc.*, No. 17-cv-247-LPS-CJB (D. Del.) ("Delaware Litigation"). Petitioner was first served with pleadings including the '871 Patent in the Delaware Litigation as part of Patent Owner's counterclaims in Patent Owner's Answer and Counterclaims to Plaintiff's First

Amended Complaint (Ex. 1009), served on September 29, 2017. The claims challenged herein (i.e., Claims 9, 10, and 13) are *not* at issue in the Delaware Litigation. *See* Ex. 1012.

This Petition for IPR is being filed concurrently with an additional petition for IPR against different claims (i.e., Claims 1, 2, 3, 6, 8, 11, 12, 14, and 15) of the '871 Patent, as well as two Petitions for IPR against U.S. Patent No. 8,077,483 ("the '483 Patent"). The '871 Patent is a continuation and claims benefit to the application of the '483 Patent. In addition, Petitioner is concurrently filing Petitions for IPR for two other patents held by Patent Owner (i.e., U.S. Patents Nos. 6,456,475 and 6,337,788). Further, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which are still pending: IPR2018-00160 (instituted 5-22-2018); IPR2018-00165 (instituted 5-18-2018); IPR2018-00166 (instituted 5-18-2018). In addition, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which have been decided, and/or are on appeal: IPR2016-00809 (FWD issued 9-22-2017); IPR2016-00995 (FWD issued 10-15-2017); IPR2016-01589 (FWD issued 2-14-2018); IPR2016-01590 (FWD issued 2-8-2018); IPR2016-01592 (FWD issued 2-8-2018); IPR2016-01594 (FWD issued 2-14-2018); IPR2016-01595 (FWD issued 2-14-2018); IPR2016-01597 (FWD issued 1-25-2018); IPR2016-01600 (FWD issued 2-14-2018).

Lead Counsel: Lead Counsel is Roger Fulghum (Reg. 39,678) and Back-up Counsel are Brian Oaks (Reg. 44,981), Nick Schuneman (Reg. 62,088), and Brett Thompsen (Reg. 69,985), each of Baker Botts L.L.P.

Service Information: Baker Botts L.L.P., One Shell Plaza, 910 Louisiana Street, Houston, Texas 77002-4995; Tel. (713) 229-1234; Fax (713) 229-1522. Petitioner consents to service by electronic mail at: ONSemi_871IPR@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

B. Certification of Grounds for Standing

Petitioner certifies that the '871 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the '871 Patent.

C. Fees

The Office is authorized to charge any fees that become due in connection with this Petition to Deposit Account No. 02-0384.

III. OVERVIEW OF THE '871 PATENT

A. Background of the Technology

The '871 Patent relates to switching power converters. Ex. 1001, Abstract. Such devices convert a first voltage (e.g., from a wall socket) to a second voltage to power an electronic device. *Id.*, 1:28-38. The '871 Patent describes and claims a class of converters that use the auxiliary winding of a transformer to detect

information relevant to the control of the converter. But, as described by the background materials below, use of an auxiliary winding in switching power converters was well-known prior to the '871 Patent. Ex. 1002, ¶ 33.

One example of a switching power converter that uses an auxiliary winding is provided by U.S. Patent 7,016,204 to Ta-Yung Yang et al. ("Yang"). Ex. 1006.

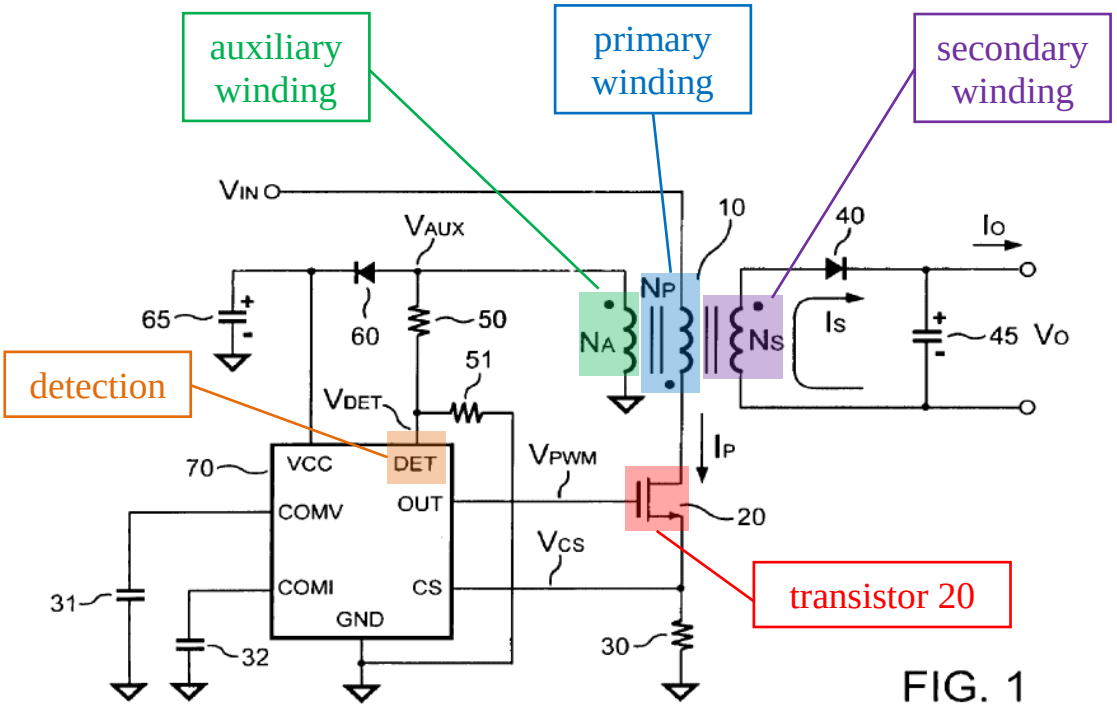


FIG. 1

Id., Fig. 1 (annotations added); Ex. 1002, ¶ 34. Yang's power converter includes transistor 20 coupled to transformer 10. Ex. 1006, Fig. 1. The transistor is turned on and off by a switching signal "V_{PWM}" to regulate how much energy is transferred from the input (V_{IN}) to the output (V_O) of the power converter. *Id.*, 2:34:40, Fig. 1.

When V_{PWM} goes high to turn on transistor 20, a current (I_P) flows from V_{IN},

through the primary winding N_P of transformer 10, and through transistor 20 and resistor 30 to ground. *Id.*, 2:41-43, Figs. 1-2. As the primary-side current I_P flows, the magnetic energy stored in transformer 10 builds. Then, when V_{PWM} goes low to turn off transistor 20, the magnetic energy stored in transformer 10 induces a secondary-side current I_S through the secondary winding N_S. *Id.*, 2:54-59, Figs. 1-2. The magnetic energy stored in transformer 10 is therefore transferred to the output by the secondary-side current I_S. Ex. 1002, ¶¶ 35-36.

As shown in Figure 1 of Yang, transformer 10 also includes auxiliary winding N_A. Because auxiliary winding N_A is magnetically coupled to the primary winding N_P and secondary winding N_S, auxiliary winding N_A "reflects" activity on the primary and secondary windings. Ex. 1002, ¶ 37. For example, when the secondary-side current I_S flows in the secondary side during the off-time of the primary-side switch, the auxiliary winding reflects the voltage present at the secondary winding.[2] Ex. 1006, 3:4-15. This voltage at the secondary winding is equal to the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40.

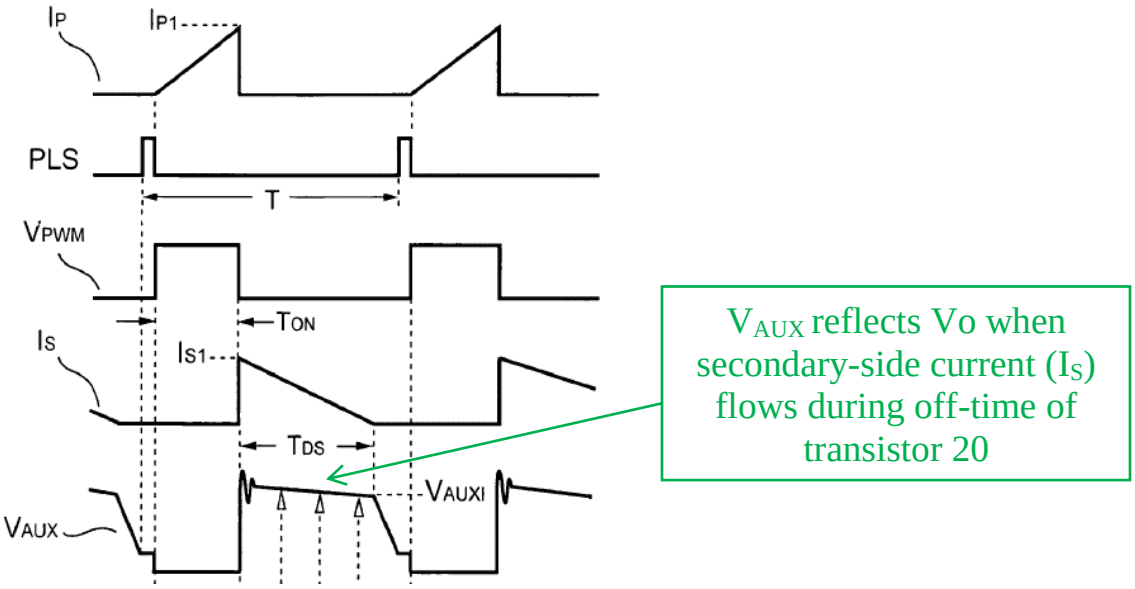
[2] The auxiliary winding reflects the voltage present at the secondary winding only during the portion of the off-time that current is flowing in the secondary side. *See* Ex. 1006, Fig. 2. Thus, when discussing herein the reflection of the output voltage during the off-time of the power switch, the Petition is referring to the portion of the off-time when current flows through the secondary winding.

Thus, the reflected voltage produced by the auxiliary winding equals the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40, multiplied by the winding ratio of the auxiliary and secondary windings:

$$V_{AUX} = \frac{T_{NA}}{T_{NS}} \times (V_O + V_F)$$

Id., 3:10 (Equation 3); Ex. 1002, ¶¶ 38-39.

Figure 2 of Yang illustrates this reflected voltage (V_{AUX}) produced on the auxiliary winding when the secondary-side current (I_S) flows:



Ex. 1006, Fig. 2 (excerpt) (annotations added).

Prior to the '871 Patent, it was well known in the art that different functions could be performed based on the reflected voltage present at the auxiliary winding

of a switching converter. Ex. 1002, ¶¶ 41-44. As described by Yang, it was known that the reflection of the output voltage on the auxiliary winding could be used as feedback for regulating the output voltage. Ex. 1006, 3:4-50, 4:5-8. It was also recognized that the reflection of the output voltage could be used to detect various fault conditions at the output of the power converter, such as a short circuit (*see* Ex. 1015, 4:30-36; Ex. 1016, 3:26-63, Fig. 1) or an output over voltage (Ex. 1007, ¶ 0023; Ex. 1004, 3:58-67). *See also* Ex. 1002, ¶¶ 42-44.

B. The Purported Advancement of the '871 Patent

Figure 1 of the '871 Patent illustrates a flyback-type power converter with a transformer that has an auxiliary winding:

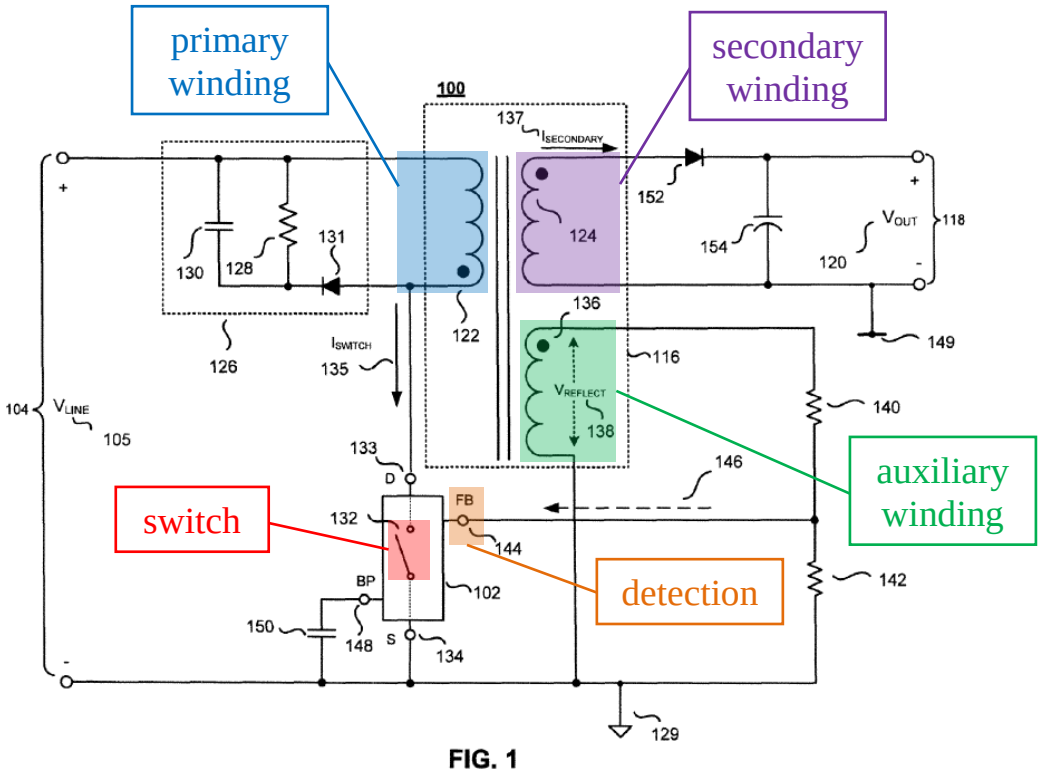
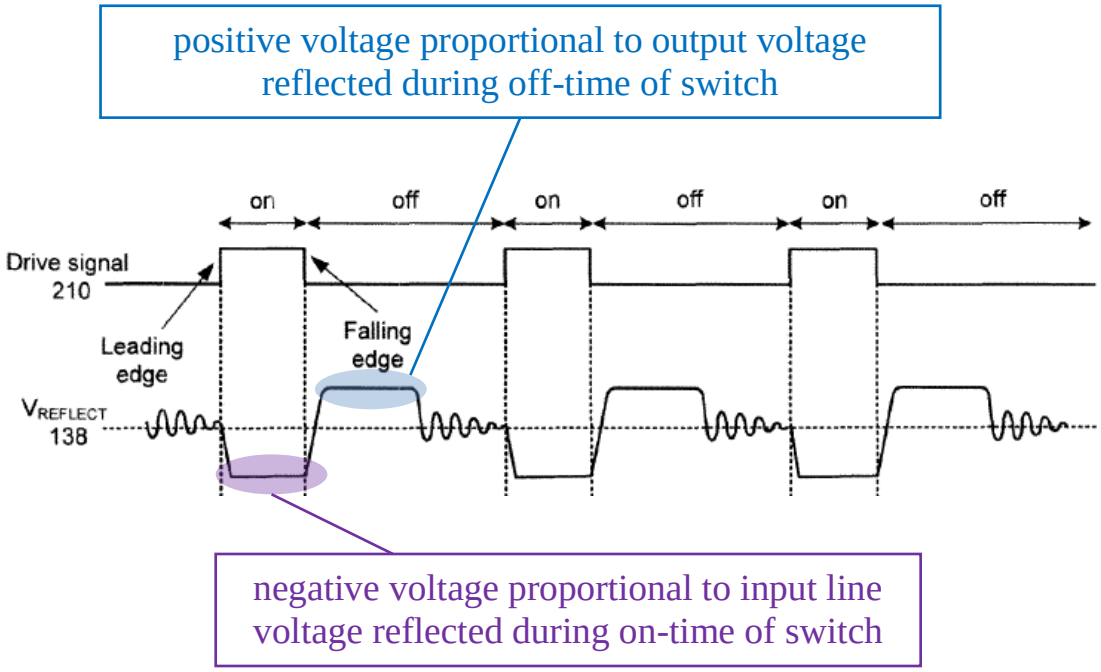


FIG. 1

Ex. 1001, Fig. 1 (annotations added); *see also id.*, 3:8-12; Ex. 1002, ¶ 45.

The ’871 Patent purports to improve upon known switching power converters by using the auxiliary winding to detect the input voltage (also referred to as the “line” voltage) in addition to the output voltage. Ex. 1001, 3:47-58. The ’871 Patent explains that the “reflected voltage $V_{REFLECT}$” at the auxiliary winding is “representative of output voltage V_{OUT} 120 during at least a portion of the time when the power switch 132 is off.” *Id.*, 3:53-58. The ’871 Patent further explains that the “reflected voltage $V_{REFLECT}$” is also “representative of an input line voltage V_{LINE} 105 during at least a portion of the time of when the power switch 132 is on.” *Id.*; *see also id.*, 3:58-4:7. The reflection of both output voltage V_{OUT} and input line voltage V_{LINE} is shown in Figure 4:



Id., Fig. 4 (excerpt) (annotations added); Ex. 1002, ¶ 46.

However, the reflection of both the output voltage and the input line voltage[3] on the auxiliary winding at different times during the switching cycle is merely the result of the magnetic coupling between the different windings of the transformer. In other words, it is the magnetic coupling of the auxiliary winding in the flyback architecture that *dictates* the voltage that is reflected by the auxiliary winding during the on-time and off-time of the power switch. Ex. 1002, ¶ 48. As explained above, the auxiliary winding reflects the voltage present on the secondary winding (i.e., V_{OUT} plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). Ex. 1006, 3:4-15. The auxiliary winding likewise reflects the voltage present on the primary winding (i.e., the input line voltage) when current flows through the primary side (i.e., during the on-time of the switch). Ex. 1002, ¶ 48.

Thus, the purported invention of the '871 Patent is based on nothing more than the recognition of how an auxiliary winding naturally responds during the on-time and off-time of the switch due to the physical relationship (i.e., the magnetic coupling) between the auxiliary winding and the other windings, which exists in every flyback-type power converter with an auxiliary winding. Ex. 1002, ¶ 49.

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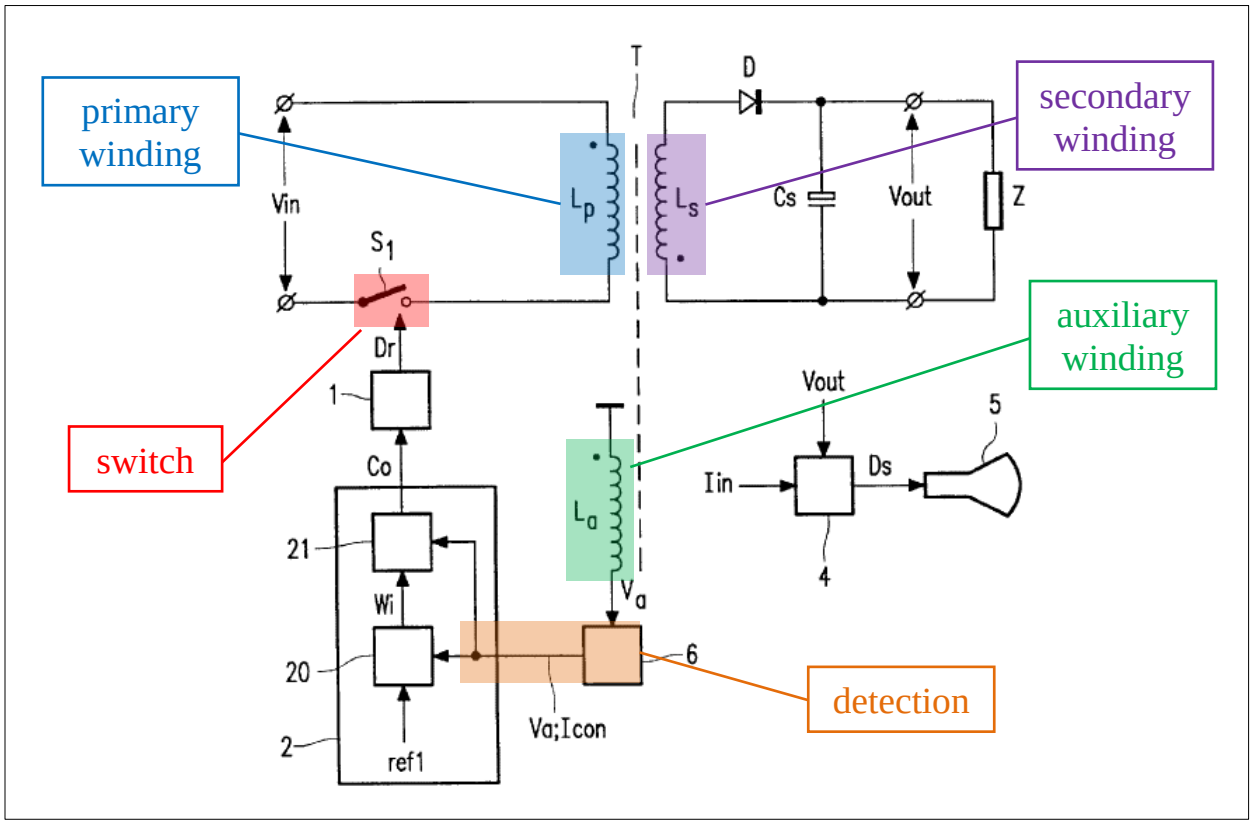
[3] The reflection of the line voltage is negative due to the opposing orientation of the windings in a flyback-type converter, as shown by the orientation of the dots on the individual windings in Figure 1 of the '871 Patent. Ex. 1002, ¶ 47.

C. Characteristics of Auxiliary Windings Were Well Known in the Art

Multiple prior art references recognize and describe the relationship between the auxiliary winding and the primary and secondary windings. Ex. 1002, ¶¶ 50-53. One example is U.S. Patent 5,831,839 ("Pansier"), which issued on November 3, 1998. Ex. 1008. Like the '871 Patent, Pansier discloses a flyback-type switching power converter with an auxiliary winding:

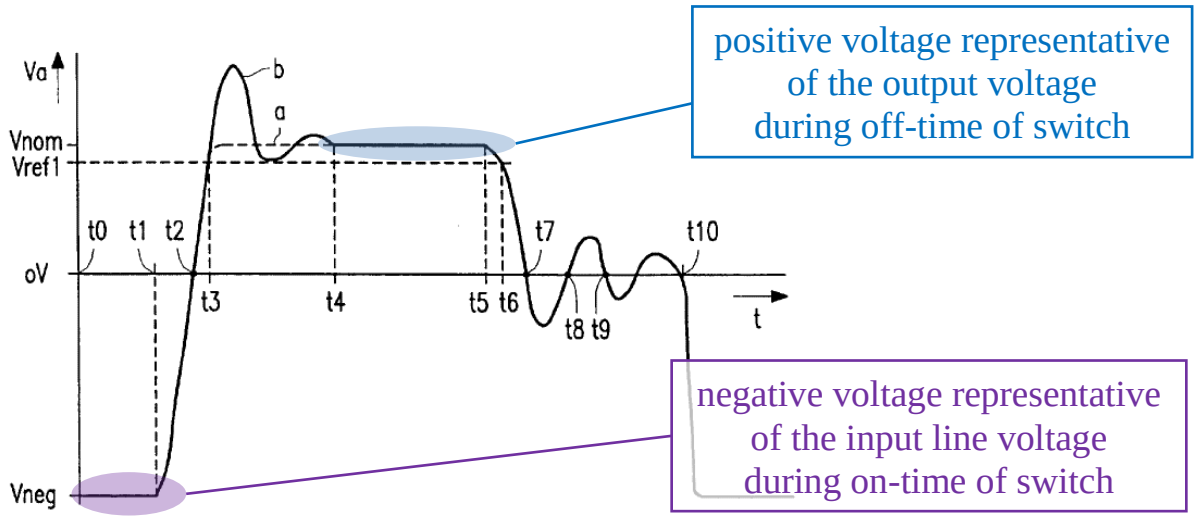


Id., Fig. 1 (annotations added); Ex. 1002, ¶ 50.

Pansier explains that, during the off-time of the switch, the auxiliary winding voltage Va "is equal to the DC output voltage Vout multiplied by the transformation ratio between the auxiliary winding La and the secondary winding

Ls." Ex. 1008, 7:45-50, Fig. 3.[4] On the other hand, "auxiliary winding voltage Va has a negative value Vneg" during the on-time of the switch, "which equals the input voltage Vi multiplied by the transformation ratio between the auxiliary winding La and the primary winding Lp." *Id.*, 7:31-37.

Like Figure 4 of the '871 Patent, Figure 3 of Pansier illustrates the reflection at the auxiliary winding of both the output voltage (Vout) and input line voltage (Vi) at different times of the switching cycle:



Ex. 1008, Fig. 3 (annotations added); Ex. 1002, ¶¶ 51-52.

Another example is U.S. Patent 6,542,386 ("Mobers"), which issued on April 1, 2003. Ex. 1004. Like Pansier, Mobers discloses a switching power converter with an auxiliary winding:

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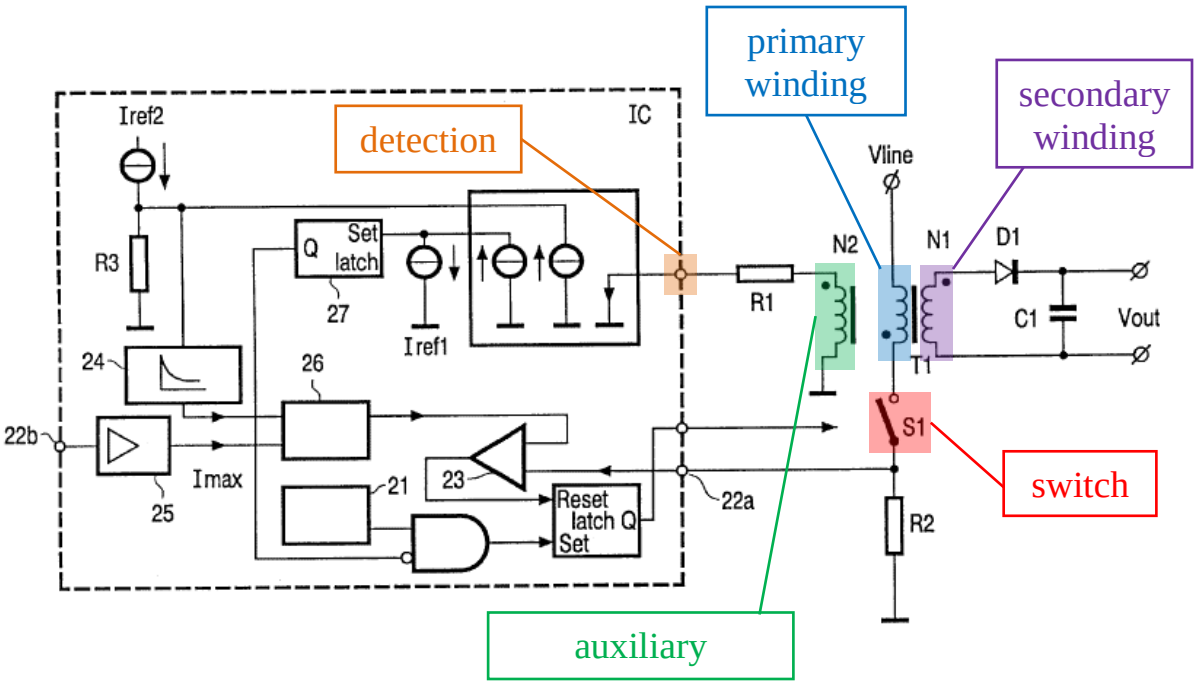
[4] *See also* Ex. 1008, 7:45-64 (explaining temporary overshoot of Va before settling to value representing output voltage).



Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 53. Mobers explains that by monitoring the auxiliary winding in a time-phased way, "not only V*out* can be monitored …, but also V_{line} can be monitored … ." Ex. 1004, 5:5-10. Specifically, "information relating to the output voltage V_{out} will be present" on the auxiliary winding during the off-time of the switch, whereas "information relating to V_{line} will be present" on the auxiliary winding during the on-time of the switch. *Id.*, 5:50-53.

D. Examination History

The '871 Patent is a continuation of U.S. Patent No. 8,406,013, which is a continuation of the '483 Patent. During prosecution of the '483 Patent, Patent Owner distinguished the purported invention by arguing that the prior art "fails to disclose '*a sensor coupled to receive a signal from* ***a single terminal*** *of the*

controller' where the signal represents both ***a line input voltage*** during the on time and ***an output voltage*** during the off time of a power converter." Ex. 1010, 31 (bold and italics emphasis in original). For example, Patent Owner argued that the Yamada and Uruno references received the line input voltage information and the output voltage information from separate terminals, not a single terminal. *Id.*, 30-31. Patent Owner also distinguished the Balakrishnan '161 reference because a diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on-time. *Id.*, 13.

Thus, Patent Owner emphasized that the distinguishing feature of the '483 Patent (and by association the '871 Patent) was the single terminal coupled to receive a signal representative of both the input and output voltage. But as described above, an auxiliary winding of a flyback switching power converter naturally reflects both the input and output voltage at different times during the switching cycle due to the physical properties of the transformer. *See, e.g.*, Ex. 1008, 7:31-43, Fig. 3; Ex. 1004, 5:11-14, 5:50-53. Thus, in the absence of a diode that blocks either the positive swing (representing the output voltage) or the negative swing (representing the input line voltage) of the signal from the auxiliary winding, a signal received from an auxiliary winding via a single terminal of the controller will represent both the input and the output voltage. Ex. 1002, ¶¶ 54-55.

IV. SUMMARY OF PRIOR ART

A. Reinhard

U.S. Patent Application Publication 2005/0254268 ("Reinhard") was filed on February 11, 2005 and published on November 17, 2005. Ex. 1007. The '871 Patent was filed on February 26, 2013 and claims priority to a provisional application filed on April 6, 2007. Ex. 1001. Reinhard is therefore prior art to the '871 Patent under at least 35 U.S.C. § 102(b). Reinhard was not considered by the Patent Office during examination of the '871 Patent. Ex. 1001, 1-2 (References Cited).

Reinhard discloses a switching power converter that utilizes a transformer with an auxiliary winding. Ex. 1007, ¶ 0001. As shown in Figure 1, Reinhard includes a sensor coupled to receive a signal from the auxiliary winding via the "U" terminal of control circuit 110:

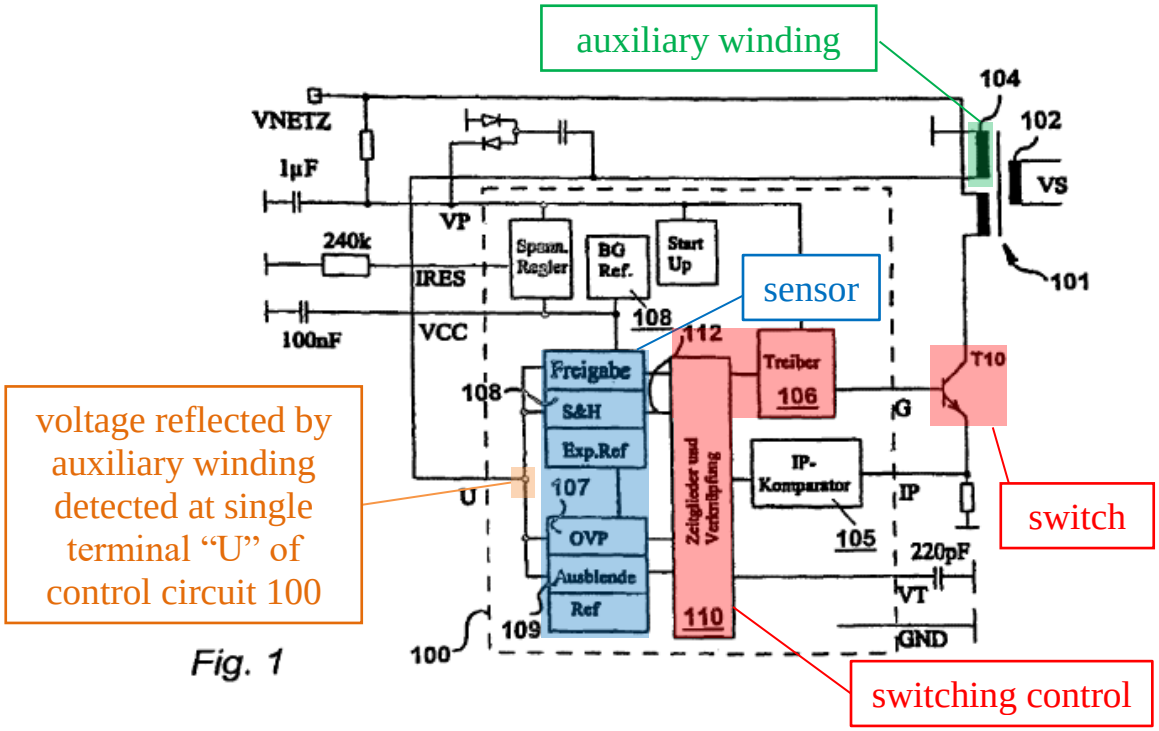


Fig. 1

Ex. 1007, Fig. 1 (annotations added); Ex. 1002, ¶¶ 56-57.

Reinhard's sensor includes a common sample and hold circuit 108, which samples the voltage value at the auxiliary winding during the off-time of switch T10 to detect the output voltage. Ex. 1007, ¶ 0022; *see also* Ex. 1002, ¶ 58; Ex. 1005, 14. The detected output voltage is, in turn, used by Reinhard as feedback for regulating the output of the power supply. *See* Ex. 1007, ¶¶ 0022, 0043; Ex. 1002, ¶ 58.

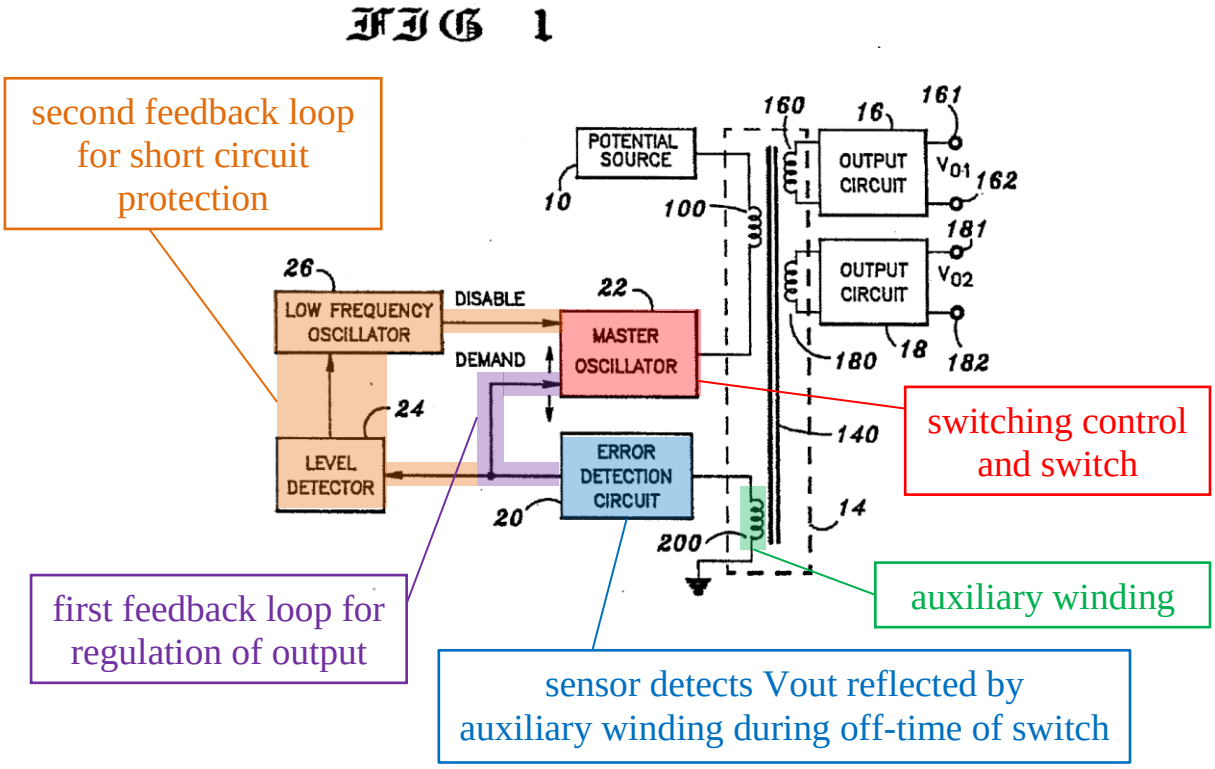
Reinhard's sensor also includes "an over-voltage protection [OVP] comparator 107 and a gating comparator 109, which are both supplied with the voltage that is induced at the auxiliary winding 104." Ex. 1007, ¶ 0023. OVP comparator 107 monitors the positive voltage (representative of the output voltage)

reflected by the auxiliary winding during the off-time of power switch T10 to implement output over-voltage protection. Ex. 1007, ¶ 0023. On the other hand, the gating comparator 109 detects the negative voltage (representative of the input line voltage) reflected at the auxiliary winding during the on-time of switch T10 to confirm proper connection of the auxiliary winding. Ex. 1007, Abstract, ¶ 0023; Ex. 1002, ¶ 59.

B. Kent

U.S. Patent 4,447,841 to Kent et al. ("Kent") issued on May 8, 1984. Ex. 1016. Kent is therefore prior art to the '871 Patent under at least 35 U.S.C. § 102(b). Kent was not considered by the Patent Office during examination of the '871 Patent. Ex. 1001, 1-2 (References Cited).

Kent discloses a switching power converter that uses a transformer with an auxiliary winding:



Ex. 1016, Fig. 1 (annotations added); Ex. 1002, ¶¶ 60-61. Like Reinhard, Kent uses the auxiliary winding to detect the output voltage. *See* Ex. 1016, 3:15-25.

A first feedback loop in Kent uses the output voltage information from error detection circuit 20 to control the duty cycle of the power switch (inside master oscillator 22) and thereby control the output of the power supply. Ex. 1016, 3:15-25, 2:62-3:2, Figs. 1-2. In addition, a second feedback loop uses the output voltage information from error detection circuit 20 to recognize "a short circuit or an overload in an output circuit" of the power supply. *Id.*, Abstract; *see also id.*, 3:26-51. When such a fault condition is detected, the second feedback path disables switching to prevent damage to the power supply that would otherwise result from

the short circuit condition. *Id.*, 3:39-44; Ex 1002, ¶ 62.

C. Spampinato

U.S. Patent 6,061,257 to Spampinato et al. ("Spampinato") issued on May 9, 2000. Ex. 1015. Spampinato is therefore prior art to the '871 Patent under at least 35 U.S.C. § 102(b). Spampinato was not considered by the Patent Office during examination of the '871 Patent. Ex. 1001, 1-2 (References Cited).

Spampinato discloses a flyback converter with an auxiliary winding:

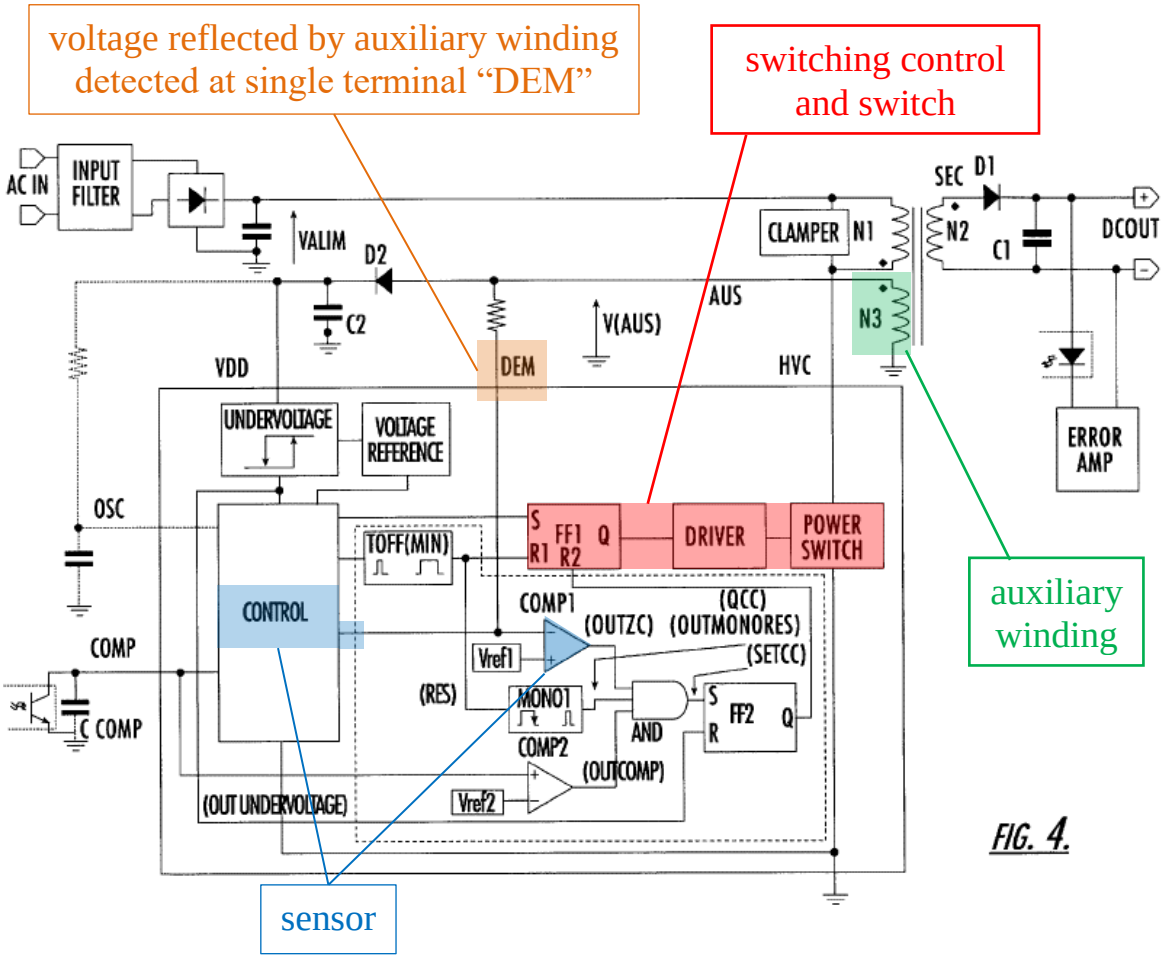


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶¶ 63-64. Spampinato uses the

reflection of the output voltage on the auxiliary winding during the off-time of the power switch to detect an output short circuit condition. *See* Ex. 1015, 3:21-29, 5:47-57. When such a fault is detected, switching is disabled to prevent damage to the power supply that would otherwise result from the short circuit condition. *Id.*, 5:47-57; Ex 1002, ¶ 64.

V. CLAIM CONSTRUCTION

In the Delaware Litigation, neither Petitioner nor Patent Owner raised a claim construction issue involving the '871 Patent for the District Court to resolve. *See* Ex. 1011. Petitioner maintains that all terms not listed below should be given their plain and ordinary meaning. Petitioner provides some explanation below regarding the plain and ordinary meaning of the requirement that the "signal" recited in Claim 8 must "represent" the output voltage and the line input voltage. Petitioner also proposes a construction for the "auto-restart signal" in Claim 13, which is not at issue in the Delaware Litigation. *See* Ex. 1002, ¶ 66.

A. "to represent" (Claim 8)

Challenged Claims 9, 10, and 13 each depend from Claim 8. Ex. 1001. Claim 8 recites a sensor that is coupled to receive "a signal." Claim 8 then separately recites characteristics of the signal: "the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an

off time of a power switch and the signal from the single terminal to represent a line input voltage during at least a portion of an on time of the power switch." *Id.*

Petitioner submits that the language regarding what "the signal" must "represent" requires no construction and should be given its plain and ordinary meaning. Consistent with the plain meaning of the claims, the "to represent" language defines characteristics of the recited "signal." However, the "to represent" phrase does ***not*** limit the operation of the separately recited sensor or any other structure recited in Claim 8. In other words, there is no requirement in the "to represent" phrase that limits whether or how the sensor responds to the information represented by the signal at different times during the switching cycle. Ex. 1002, ¶¶ 67-68.

Where Patent Owner intended to define actions taken by the sensor and/or other recited structures in the claims based on the information represented by the recited "signal," Patent Owner did so expressly. For example, other portions of Claim 8 recite an output fault detector that responds to the output voltage information. Ex. 1001, Claim 8. But, there is nothing in independent Claim 8 that must similarly respond to the line input voltage. *See id.* That is left instead to the "power limiter" in dependent Claim 14. *Id.*, Claim 14. Thus, there is no requirement in independent Claim 8 that the sensor, or any other recited structure,

must respond to the "line input voltage" information that is represented by the recited "signal" during the on-time of the switch. Ex. 1002, ¶ 69.

Lastly, there was no disclaimer of claim scope during prosecution that would further limit (beyond the limitations expressly recited Claim 8) whether or how the structures in Claim 8 respond to the information represented by the recited "signal." During prosecution of the parent application 12/058,530 (now issued as U.S. Patent No. 8,077,483), Patent Owner distinguished three references on the basis that these references did not disclose a terminal that received a signal that represented both output voltage and the line input voltage of the power converter at the specified different times. In a Response dated February 4, 2011, Patent Owner distinguished U.S. Patent Nos. 6,842,353 (Yamada) and 7,551,462 (Uruno) on the basis that both references receive different signals representing the input and output voltage at different terminals. Ex. 1010, 30-31. In a later Response to Office Action dated May 27, 2011, Patent Owner distinguished U.S. Patent No. 6,233,161 (Balakrishnan) on the basis that a diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on-time. Ex. 1010, 13.

Importantly, Patent Owner's arguments during examination relate to what the ***signal*** received from a single terminal ***represents***, not how any of the separately recited structures respond to that signal. Thus, there was no clear and

unmistakable disclaimer in the prosecution history that would require the separately recited structures in Claim 8 to respond to the information represented by the recited "signal" in any particular manner beyond what is already expressly recited in the claim. For example, there is nothing in the prosecution history that would require that the structures recited in Claim 8 to respond to the line input voltage information that is represented by the recited "signal" during the on-time of the switch in addition to the output voltage information that is represented by the signal during the off-time of the switch. Ex. 1002, ¶¶ 70-71.

B. "auto-restart signal" (Claim 13)

Independent Claim 8 recites: "the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to ***output a fault signal*** to the switching control in response to the detection of the fault condition." Ex. 1001 (emphasis added). Claim 13 depends from Claim 8 and further requires that "the output fault detector is coupled to ***output an auto restart signal*** to the switching control to indicate to the switching control to enter an auto restart mode." *Id*. (emphasis added).

Consistent with the intrinsic record, the "auto restart signal" in Claim 13 serves as a further definition of the "fault signal" in Claim 8. In other words, Claim 13 does not require a separate auto restart signal in addition to the fault signal of Claim 8. Ex. 1002, ¶ 72-73.

The ’871 specification does not specifically describe an “output fault detector.” *See* Ex. 1001. Rather, the specification discloses “auto-restart detector 216,” which outputs auto restart signal 218 to switching control 208 to engage an “auto restart mode” during a fault condition such as an “output overload” or “output short circuit.” *Id.*, 5:15-24. Thus, the ***only*** support in the specification for the “output fault detector” recited in Claim 8 element is auto-restart detector 216 shown in Figure 3 and described in column 5.[5]

Importantly, auto-restart detector 216 shown in Figure 3 outputs only a ***single signal*** (i.e., auto restart signal 218) to switching control 208. Ex. 1001, Fig. 3. That signal (i.e., auto restart signal 218) is therefore the only support in the specification for the “fault signal” that is output to the switching control in Claim 8, as well as the “auto-restart signal” that is output to the switching control in Claim 13. *See id.*, 5:14-24, Fig. 3; Ex. 1002, ¶¶ 74-75. To the extent that Claims 8 and 13 are considered enabled and supported by the written description of the ’871 specification, the “auto-restart” signal recited in Claim 13 should be considered a further definition of the same “fault” signal recited in Claim 8.

[5] The other blocks that respond to the detected output voltage (i.e., output regulator 212 and constant current regulator 219) regulate the output but are not described as detecting fault conditions. Ex. 1001, 5:5-13, 5:37-42.

The context of claims also supports Petitioner's interpretation. The structure of dependent Claims 9 through 13 confirms that Patent Owner used the dependent claims to further define generic elements in Claim 8. Dependent Claims 9-12 each recite a different type of output fault condition that the output fault detector of Claim 8 must detect (e.g., overload, short circuit, and over voltage). The auto-restart signal in Claim 13 should be similarly interpreted as a further, more specific, definition of the fault signal recited in Claim 8. Ex. 1002, ¶ 76.

VI. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: The Combination of Reinhard and Kent Renders Claims 9, 10, and 13 Obvious Under 35 U.S.C. § 103

The combination of Reinhard and Kent discloses and suggests to a person of ordinary skill in the art ("POSITA") each element of Claims 9, 10, and 13, and thus renders those claims obvious under 35 U.S.C. § 103. Ex. 1002, ¶ 77.

1. A POSITA Would Have Been Motivated to Combine Reinhard and Kent

Reinhard discloses a switching power converter that utilizes a transformer with an auxiliary winding. Ex. 1007, ¶ 0001. Figure 1 of Reinhard illustrates components of the controller for the switching power converter:

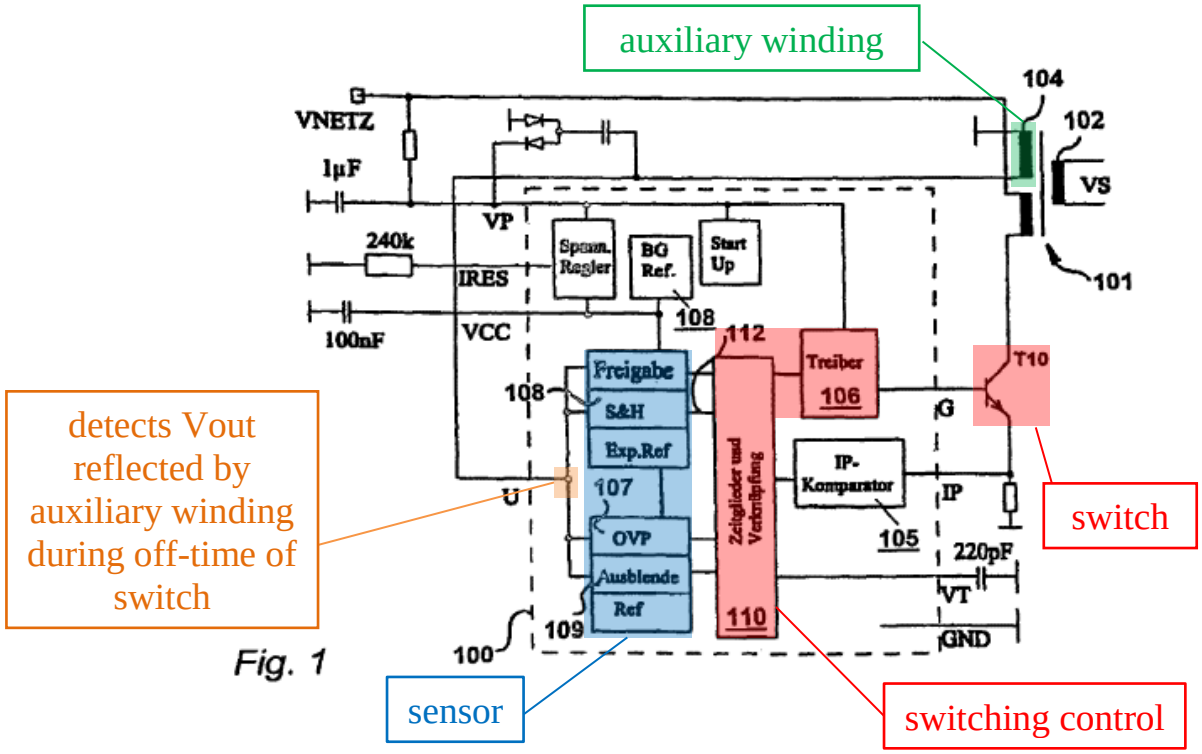


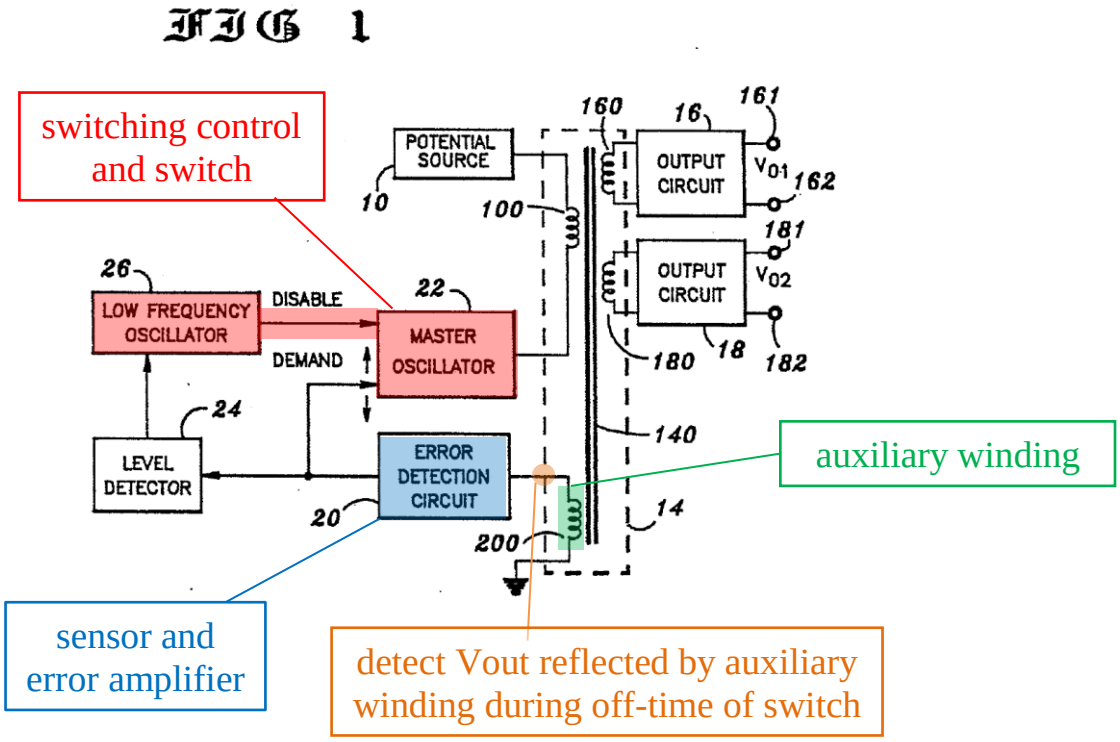
Fig. 1

Ex. 1007, Fig. 1 (annotations added); Ex. 1002, ¶ 78. As shown in Figure 1, Reinhard includes a sensor coupled to receive a signal from the auxiliary winding via the "U" terminal of control circuit 110. *See* Ex. 1007, Fig. 1.

Reinhard's sensor includes sample and hold circuit 108, which samples the voltage at the auxiliary winding during the off-time of switch T10 to detect the output voltage. Ex. 1007, ¶ 0022. The sampled voltage is used by Reinhard as feedback for controlling the output voltage of the power supply. *See id.*, ¶ 0043 (describing "an output voltage control that samples the voltage at a primary auxiliary winding"), ¶ 0022 ("In particular the positive voltage pulse at the auxiliary winding after the opening of the switch may be used for controlling the

output power of the switched mode power supply unit. Here the control is performed by means of a corresponding adapting of the time duration wherein the switch T10 is opened."); *see also* Ex. 1002, ¶ 79.

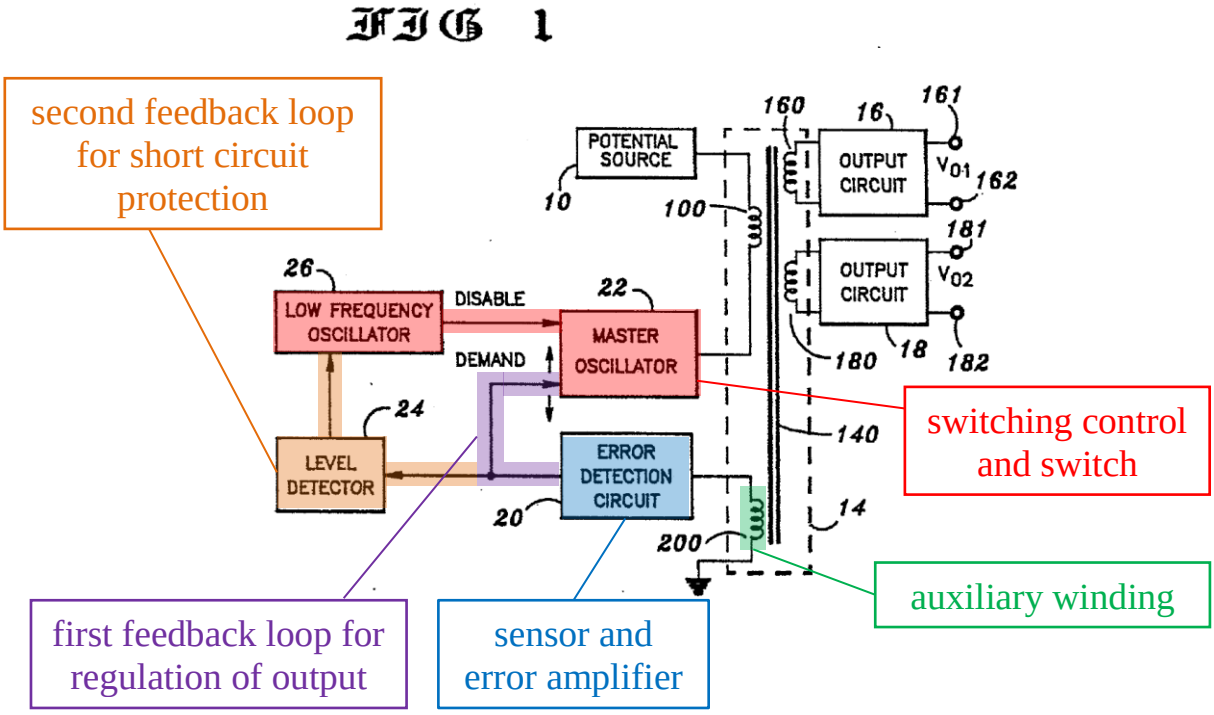
Similar to Reinhard, Kent discloses a switching power converter that utilizes a transformer with an auxiliary winding:



Ex. 1016, Fig. 1 (annotations added); Ex. 1002, ¶ 80. And like Reinhard, Kent uses the auxiliary winding to detect the output voltage. *See* Ex. 1016, 3:15-25. The detected output voltage is, in turn, used to control the duty cycle of the switch (inside master oscillator 22) to regulate the output of the power supply. Ex. 1016, 3:15-25; *see also id.*, 2:62-3:2.

In addition, Kent uses the output voltage information to detect "a short circuit or an overload in an output circuit" of the power supply. Ex. 1016, Abstract. Kent explains that when an output of the power supply is shorted, a large current caused by the short may damage components of the power supply (e.g., the rectifier diode in the output circuit). *Id.*, 1:12-21; Ex. 1002, ¶ 81. Indeed, it was well known in the art that continued switching during a short circuit condition could damage components of the switching power supply. Ex. 1002, ¶ 81; Ex. 1022, 1:23-26 ("In some cases, for example a short on the output, the controller increased the load current to a value that resulted in damage to the controller and the power supply system."); *see also* Ex. 1021, 1:29-31.

To prevent such damage, Kent implements an "overcurrent protection" by using the detected output voltage from the auxiliary winding as part of a second feedback loop. Ex. 1016, 3:26-32. As shown in Figure 1, the second feedback loop of Kent includes level detector 24 and a low frequency oscillator 26:



Ex. 1016, Fig. 1 (annotations added); Ex. 1002, ¶ 82. If the output voltage detected via the auxiliary winding is low enough to indicate a short circuit at the output of the power supply, Kent's level detector 24 triggers low frequency oscillator 26 to disable switching. Ex. 1016, 3:39-44 ("By setting a threshold of level detector 24 to respond only to a very high level of output from error detection circuit 20, the dramatic undervoltage associated with a short circuit in an output can be used to trigger low frequency oscillator 26 to disable master oscillator 22."). As noted by Kent, the disablement is "periodically removed" by low frequency oscillator 26 so that "normal functioning resumes" when the short circuit is removed. *Id.*, 3:44-51.

A POSITA would have been motivated to combine Reinhard with Kent's teaching of an overcurrent protection scheme to provide Reinhard with the same

protection from damage that could otherwise occur during a short circuit condition.[6] Ex. 1002, ¶ 83. Such a combination represents the use of a known technique (e.g., Kent's overcurrent protection) to improve a similar device (e.g., Reinhard's switching power converter) in the same way (e.g., by employing a second feedback loop that detects a short circuit via the output voltage reflected by the auxiliary winding during the off-time of the switch). *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1740 (2007); Ex. 1002, ¶ 83.

As described above, Reinhard and Kent are similar in that they both include a switching power supply that uses an auxiliary winding to detect the output voltage of the power converter. Moreover, Reinhard and Kent both use the detected output voltage to regulate the output voltage of the power converter. Kent teaches that a second feedback loop can be employed based on the output voltage information already detected via the auxiliary winding. Ex. 1016, 3:26-51. The second feedback loop is used to determine whether the voltage detected at the auxiliary winding indicates that there is a short circuit at the output of the power supply. *Id.* If so, the second feedback loop disables switching for a time period to

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[6] Kent describes its overcurrent protection circuit "for use in a multiple output switched power supply." Ex. 1016, Abstract. But, Kent also explains that its invention is applicable to switching power supplies, like the one in Reinhard, with "as few as one" output. *Id.*, 2:42-45.

protect against damage that may occur if the switching power supply keeps switching during such a short circuit condition. *Id.*

Given the similarities between Reinhard and Kent, a POSITA would have found it obvious to incorporate Kent's teaching of second feedback loop into Reinhard to provide Reinhard with the same improvement (i.e., short circuit protection). Ex. 1002, ¶¶ 84-85. In such a combination, Kent's error detection circuit 20,[7] level detector 24, and low frequency oscillator 26 (*see* Ex. 1016, 3:26-

[7] As shown in the schematic diagram of Figure 2, Kent's error detection circuit 20 includes a diode 201 and capacitor 203 to sample the positive voltages at the primary winding. Ex. 1016, Fig. 2, 4:14-19. However, Reinhard already includes a sample and hold circuit (S&H) 108 to sense a voltage from the auxiliary winding representative of the output voltage. Ex. 1007, Fig. 1, ¶¶ 0022, 0043; *see also* Ex. 1002, ¶ 85 (FN9); Ex. 1014, 22 (showing peak detector configured like Kent's diode 201 and capacitor 203), 25-26 (explaining that a sample-and-hold circuit provides a similarly sampled voltage). Thus, the proposed combination of Reinhard and Kent includes the portion of Kent's error detection circuit 20 (e.g., error amplifier 206) located *after* the sampling circuitry. Ex. 1002, ¶ 85 (FN9). By maintaining Reinhard's sample and hold circuitry as opposed to coupling a rectifying diode in series with the auxiliary winding, Reinhard's "U" terminal (i.e., the single terminal of the controller) would still receive a negative voltage during

51, Fig. 1) would be incorporated with Reinhard's sample and hold circuit 108 and switching control (*see* Ex. 1007, Fig. 1). Because the protection scheme would be employed in the Reinhard combination in the same manner as in Kent itself, a POSITA would expect the protection scheme to operate in the same predictable manner when combined with Reinhard. Ex. 1002, ¶ 85.

Moreover, the above-described combination of Reinhard and Kent represents the application of a known technique (e.g., Kent's use of a second feedback loop to detect short circuits) to improve a known device (e.g., Reinhard's switching power converter with an auxiliary winding) ready for improvement to yield a predictable result (i.e., a primary-controlled switched mode power supply with short circuit protection). *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. at 1740; Ex. 1002, ¶ 86.

As described above, Reinhard includes a "primary-controlled switched mode power supply unit" (Ex. 1007, Abstract) that uses an auxiliary winding to detect the output voltage of the power converter for the purpose of regulating the output of the power supply (*see id.*, ¶¶ 0022, 0043). Although Reinhard employs various other protection schemes (e.g., over voltage protection), it does not protect against the damage that may be caused by a short circuit at the output of the power supply.

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the on-time of the switch as expected by Reinhard's gating comparator 109. *See* Ex. 1007, ¶ 0023; Ex. 1002, ¶ 85 (FN9).

Ex. 1002, ¶ 87. Thus, a POSITA would recognize that Reinhard may be improved by incorporating the short circuit protection scheme taught by Kent. *Id.* And because Reinhard already detects the output voltage information via an auxiliary winding (similar to Kent), a POSITA would be able to implement Kent's protection scheme with Reinhard's controller with predictable results. *Id.*

2. Independent Claim 8

Claim 8 is challenged in a concurrently filed Petition but is *not* challenged herein. Nonetheless, the disclosure of Claim 8 is shown below to facilitate challenges to dependent claims.

8[pre]: "A controller for use in a power converter, comprising:"

Reinhard discloses a controller for use in a power converter:

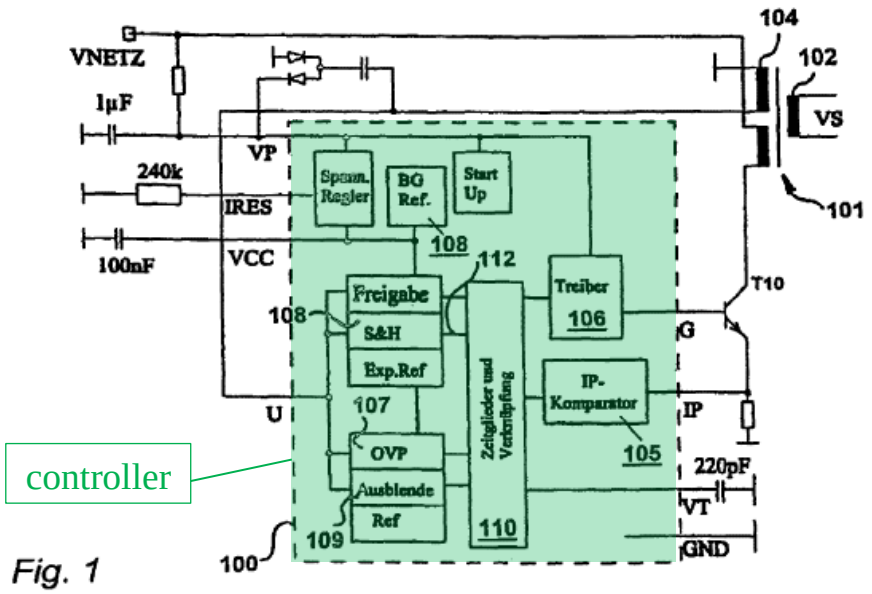


Fig. 1

Ex. 1007, Fig. 1 (annotations added); *see also id.*, Abstract, ¶¶, 0001, 0021.

Accordingly, the combination of Reinhard and Kent discloses and suggests to a POSITA each element of the preamble of Claim 8.[8] Ex. 1002, ¶ 88.

8[pre]	*See* Reinhard and Kent citations in Section VI.A.1. **Reinhard:** Ex. 1007, ¶ 0021: "Referring now to the drawings and in particular to FIG. 1, a control circuit for controlling the output power of a primary-controlled switch mode power supply unit is shown in its application environment." *See also* Ex. 1007, Abstract, ¶¶ 0001, 0005, 0007, 0010, 0021, 0022, 0023, 0043, Figs. 1-2, Claims 1-2, 6, 7, 10, 16, and 28.

Claim 8[a]: "a sensor coupled to receive a signal from a single terminal of the controller,"

Reinhard includes a sensor coupled to receive a signal from the auxiliary winding via the "U" terminal (i.e., a single terminal) of controller 100:

[8] The preamble is not limiting but is nonetheless disclosed by Reinhard.

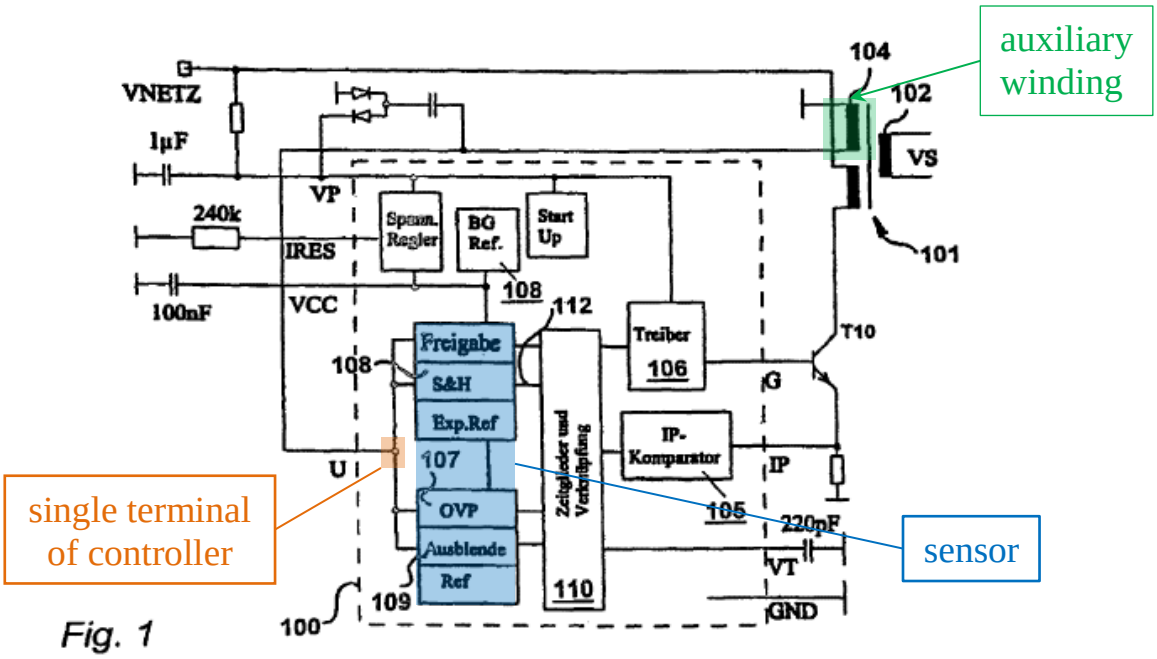


Fig. 1

Ex. 1007, Fig. 1 (annotations added); Ex. 1002, ¶ 89.

As described in Section V.A, Claim 8 requires that the "sensor" be coupled to receive a "signal" from the single terminal that represents the line input voltage and the output voltage at different times in the switching cycle. There is no requirement in Claim 8, however, regarding whether or how the sensor must respond, for example, to the line input voltage represented by the signal during the on-time of the switch. But regardless, Reinhard's sensor is configured to detect and act upon both the positive voltage (representative of the output voltage) during the off-time of the switch, and the negative voltage (representative of the line input voltage) during the on-time of the switch. *See* Ex. 1007, ¶ 0023.

For example, Reinhard's sensor includes sample and hold circuit 108, which samples the voltage value at the auxiliary winding during the off-time of switch

T10 to detect the output voltage. Ex. 1007, ¶ 0022. The detected output voltage is, in turn, used by Reinhard as feedback for regulating the output voltage of the power supply. *See id.*, ¶¶ 0022-0043; Ex. 1002, ¶ 91.

Reinhard's sensor also includes "an over-voltage protection [OVP] comparator 107 and a gating comparator 109, which are both supplied with the voltage that is induced at the auxiliary winding 104." Ex. 1007, ¶ 0023. "OVP comparator 107 detects positive voltages" induced on the auxiliary winding during the off-time of switch T10, and "gating comparator 109 detects the negative voltages" induced on the auxiliary winding during the on-time of the switch T10. *Id.*

Accordingly, the combination of Reinhard and Kent discloses and suggests to a POSITA each limitation of claim element 1[a]. Ex. 1002, ¶¶ 89-93.

[8a]	*See* Reinhard and Kent citations in Section VI.A.1. **Reinhard:** Ex. 1007, ¶ 0023: "[T]he control circuit 100 further comprises an over-voltage protection comparator 107 and a gating comparator 109, which are both supplied with the voltage that is induced at the auxiliary winding 104. The OVP comparator 107 detects positive voltages above the control region, switches off the driver 106 for the duration of a gating time and thus prevents the occurring of over-voltages. When the auxiliary winding works properly, a negative voltage pulse is induced when the primary-side switch is closed as shown in FIG. 4 in curve 401. … The gating comparator 109 detects the negative voltages during the closing of the primary-side switch and also triggers the blind-out time for the driver when a negative voltage pulse is missing." (emphasis added).

	Ex. 1007, ¶ 0022: "In particular the positive voltage pulse at the auxiliary winding after the opening of the switch may be used for controlling the output power of the switched mode power supply unit. Here the control is performed by means of a corresponding adapting of the time duration wherein the switch T10 is opened. … The sample and hold circuit 108 according to the present invention is supplied with a corresponding sample signal 112 from a circuit arrangement contained in the block 'timing circuit and interconnection' 110, when the voltage value at the auxiliary winding has to be sampled and stored." (emphasis added). Ex. 1007, ¶ 0043: "In a switched mode power supply unit with an output voltage control that samples the voltage at a primary auxiliary winding, an over-voltage protection circuit may be provided as a second control loop or an over-voltage interruption at the same auxiliary winding." (emphasis added). *See also* Ex. 1007, Abstract, ¶¶ 0003, 0005, 0007, 0022, 0023, 0027, 0028, 0034, 0043, Claims 1, 27, Figs. 1, 2, 4.

Claim 8[b]: "the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage during at least a portion of an on time of the power switch,"

Figure 1 of Reinhard illustrates auxiliary winding 104 magnetically coupled to both primary winding 101 and secondary winding 102:

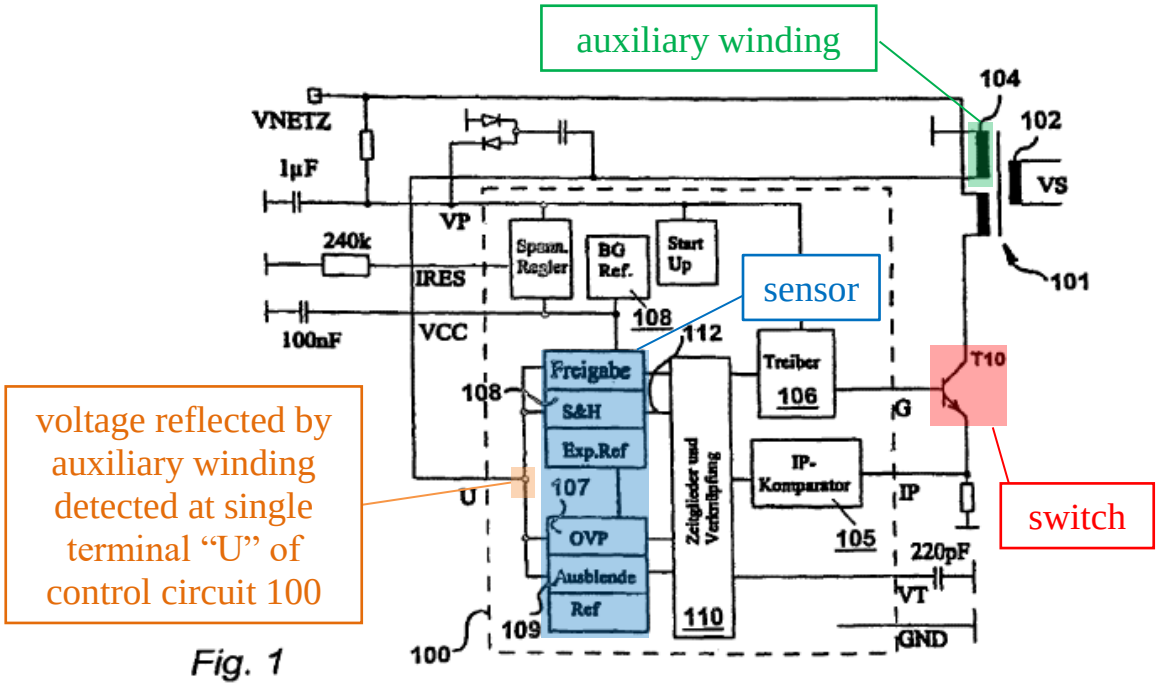
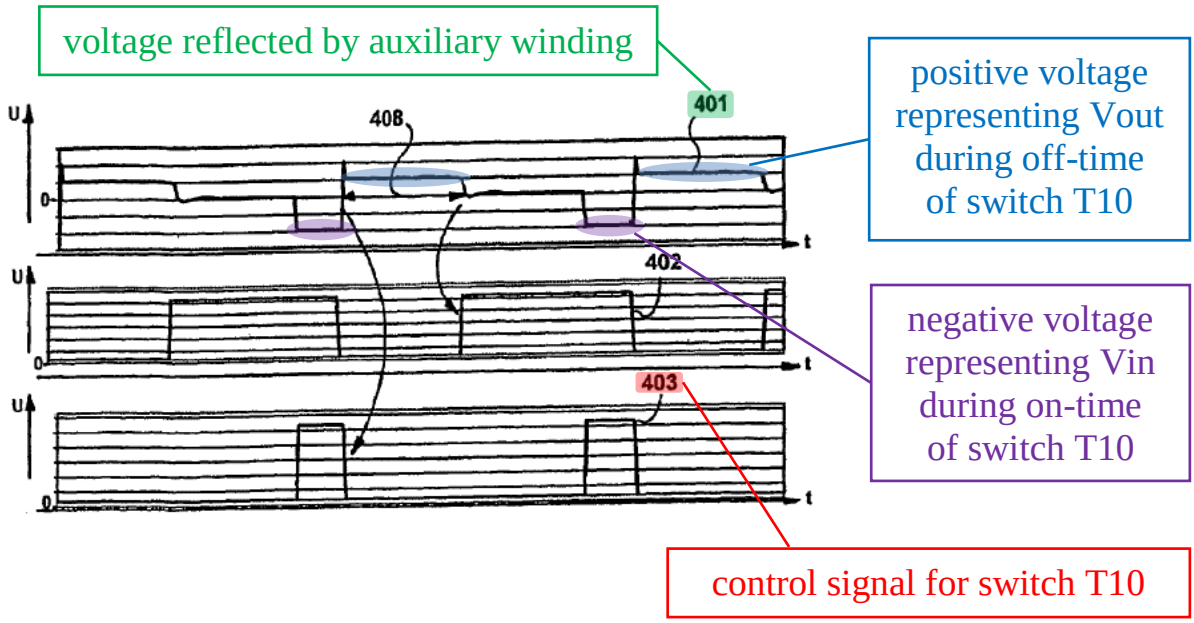


Fig. 1

Ex. 1007, Fig. 1 (annotations added); Ex. 1002, ¶ 94. As described in Section III, a POSITA would understand that the magnetic coupling of the transformer disclosed by Reinhard causes the auxiliary winding to (i) produce a positive voltage representative of the output voltage during at least a portion of the off-time of the switch, and (ii) produce a negative voltage representative of the input line voltage during the on-time of the switch. *See supra* Sections III.A-C; Ex. 1002, ¶ 94.

Consistent with this understanding, Reinhard discloses that the signal received from the auxiliary winding via the "U" terminal of control circuit 100 includes a "positive voltage pulse" during the off-time of switch T10, and a "voltage pulse in negative direction" during the on-time of switch T10. Ex. 1007, ¶ 0021 (emphasis added). Likewise, curve 401 in Figure 4 illustrates "the voltage

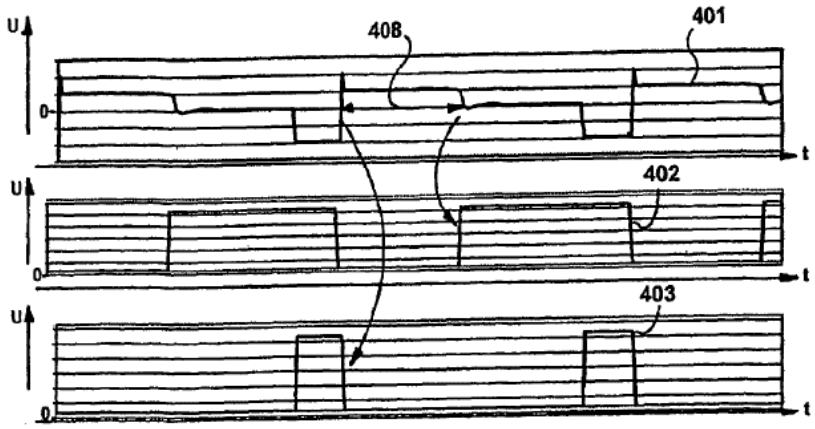
at the auxiliary winding" that is induced during the on-time and the off-time of power switch T10. Ex. 1007, ¶ 0032.



Id., Fig. 4 (excerpt) (annotations added); Ex. 1002, ¶ 95.

In sum, a POSITA would understand that the positive voltage swing of the signal received via the "U" terminal in Reinhard represents the output voltage of the power converter, while the negative voltage swing of that signal disclosed in Reinhard represents the line input voltage. Therefore, a POSITA would understand Reinhard to disclose and suggest each limitation of claim element 8[b]. Ex. 1002, ¶¶ 94-96.

[8b]	*See* Reinhard and Kent citations in Section VI.A.1. **Reinhard:** *See* citations for claim element 8[a]. Ex. 1007, ¶ 0032: "Here the curve 401 signifies the course of the voltage

	at the auxiliary winding, the curve 402 the course of the demagnetization detection, the curve 403 the course of the control signal for the primary-side switch T10, … .” (emphasis added). Ex. 1007, Fig. 4 (excerpt):  Ex. 1007, ¶ 0021: “As can be seen schematically from curve 401 of FIG. 4, a positive voltage pulse is induced within the auxiliary winding after the switch T10 has opened, which exhibits at first an overshoot and then a continuously decaying course. After the duration of the voltage pulse 408 has expired, the voltage at the auxiliary winding decays with a transient oscillation to zero. A voltage pulse in negative direction is induced within the auxiliary winding, when the switch is closed again.” (emphasis added). Ex. 1007, ¶ 0023: “[T]he control circuit 100 further comprises an over-voltage protection comparator 107 and a gating comparator 109, which are both supplied with the voltage that is induced at the auxiliary winding 104. The OVP comparator 107 detects positive voltages above the control region, switches off the driver 106 for the duration of a gating time and thus prevents the occurring of over-voltages. When the auxiliary winding works properly, a negative voltage pulse is induced when the primary-side switch is closed as shown in FIG. 4 in curve 401. If the auxiliary winding 104 is not connected or broken, this negative voltage pulse is missing. The gating comparator 109 detects the negative voltages during the closing of the primary-side switch and also triggers the blind-out time for the driver when a negative voltage pulse is missing.” (emphasis added). *See supra* Sections III.A-C.

	See also Ex. 1007, Abstract, ¶¶ 0007, 0010, 0022, 0027, 0034, 0043, Figs. 1-2, 4, Claims 1-2, 6, 7, 8, 10, 13, 16, 25, 28, 30.

Claim 8[c]: "a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and,"

Reinhard discloses "timing circuit and interconnection 110" and "driver 106," which collectively form a switching control that switches switch T10 (i.e., a power switch) on and off. Ex. 1007, ¶ 0022.

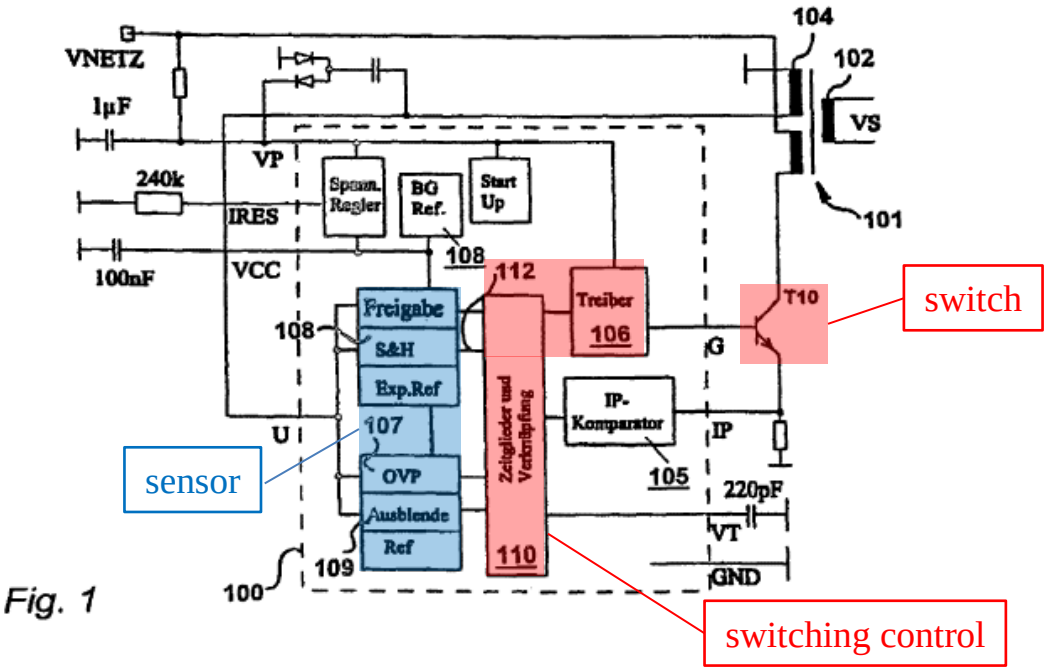


Fig. 1

Id., Fig. 1 (annotations added); Ex. 1002 ¶ 97. The output power of the power supply is regulated by controlling the on and off switching of switch T10:

> In particular the positive voltage pulse at the auxiliary winding after the opening of the switch may be used for *controlling the output power of the switched mode power supply* unit. Here the control is

> performed by means of a corresponding adapting of the *time duration wherein the switch T10 is opened*. The actual controlling of the bipolar transistor T10 is performed via a driver 106.

Ex. 1007, ¶ 0022 (emphasis added); *see also id.*, ¶¶ 0021-0022.

Reinhard's switching control[9] is responsive to the sensor in multiple ways. For example, the sample and hold circuit (S&H) 108 within Reinhard's sensor samples the voltage at the auxiliary winding to detect the output voltage. Ex. 1007, ¶ 0022, 0043. And as described directly above, the sampled output voltage is, in turn, used by Reinhard to control the switching of switch T10, and thereby control the amount of power that is transferred from the input to the output of the power supply. *See* Ex. 1007, ¶ 0022, Claim 25; Ex. 1002, ¶ 98.

The switching control is also responsive to both over-voltage protection [OVP] comparator 107 and gating comparator 109 in Reinhard's sensor. "OVP comparator 107 detects positive voltages above the control region, switches off the driver 106 for the duration of a gating time and thus prevents the occurring of over-voltages." Ex. 1007, ¶ 0023. Further, the "gating comparator 109 detects the negative voltages during the closing of the primary-side switch and also triggers the blind-out time for the driver when a negative voltage pulse is missing." *Id.*

[9] As described below for claim element 8[d] and Claim 13, Kent's low frequency oscillator 26 also forms part of the switching control in the proposed combination.

Accordingly, the combination of Reinhard and Kent discloses and suggests to a POSITA each limitation of claim element 8[c]. Ex. 1002, ¶¶ 97-100.

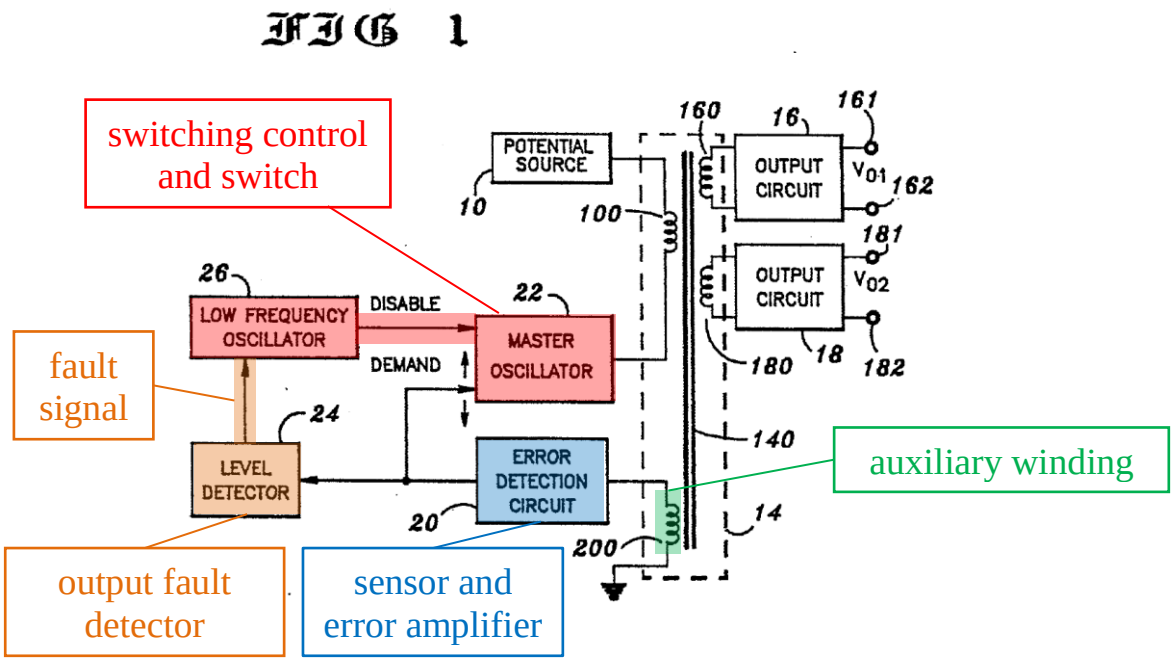
[8c]	*See* Reinhard and Kent citations in Section VI.A.1. **Reinhard:** Ex. 1007, ¶ 0022: "In particular the positive voltage pulse at the auxiliary winding after the opening of the switch may be used for controlling the output power of the switched mode power supply unit. Here the control is performed by means of a corresponding adapting of the time duration wherein the switch T10 is opened. The actual controlling of the bipolar transistor T10 is performed via a driver 106." Ex. 1007, ¶ 0043: "In a switched mode power supply unit with an output voltage control that samples the voltage at a primary auxiliary winding, an over-voltage protection circuit may be provided as a second control loop or an over-voltage interruption at the same auxiliary winding." Ex. 1007, ¶ 0043: "Therefore, in an advantageous manner the complete output voltage controlling, including the over-voltage protection, may be integrated into one integrated circuit … ." (emphasis added). Ex. 1007, Claim 25: "wherein the step of adjusting the output power comprises adapting the time period during which the primary-side switch is opened." Ex. 1007, ¶ 0023: "[T]he control circuit 100 further comprises an over-voltage protection comparator 107 and a gating comparator 109, which are both supplied with the voltage that is induced at the auxiliary winding 104. The OVP comparator 107 detects positive voltages above the control region, switches off the driver 106 for the duration of a gating time and thus prevents the occurring of over-voltages. … The gating comparator 109 detects the negative voltages during the closing of the primary-side switch and also triggers the blind-out time for the driver when a negative voltage pulse is missing." *See also* Ex. 1007, Abstract, ¶¶ 0001, 0005, 0007, 0010, 0012, 0021-0027, 0043, Figs. 1-2, 4, Claims 1-2, 7, 9-10, 13, 16, 25, 28, 30.

Claim 8[d]: "an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition."

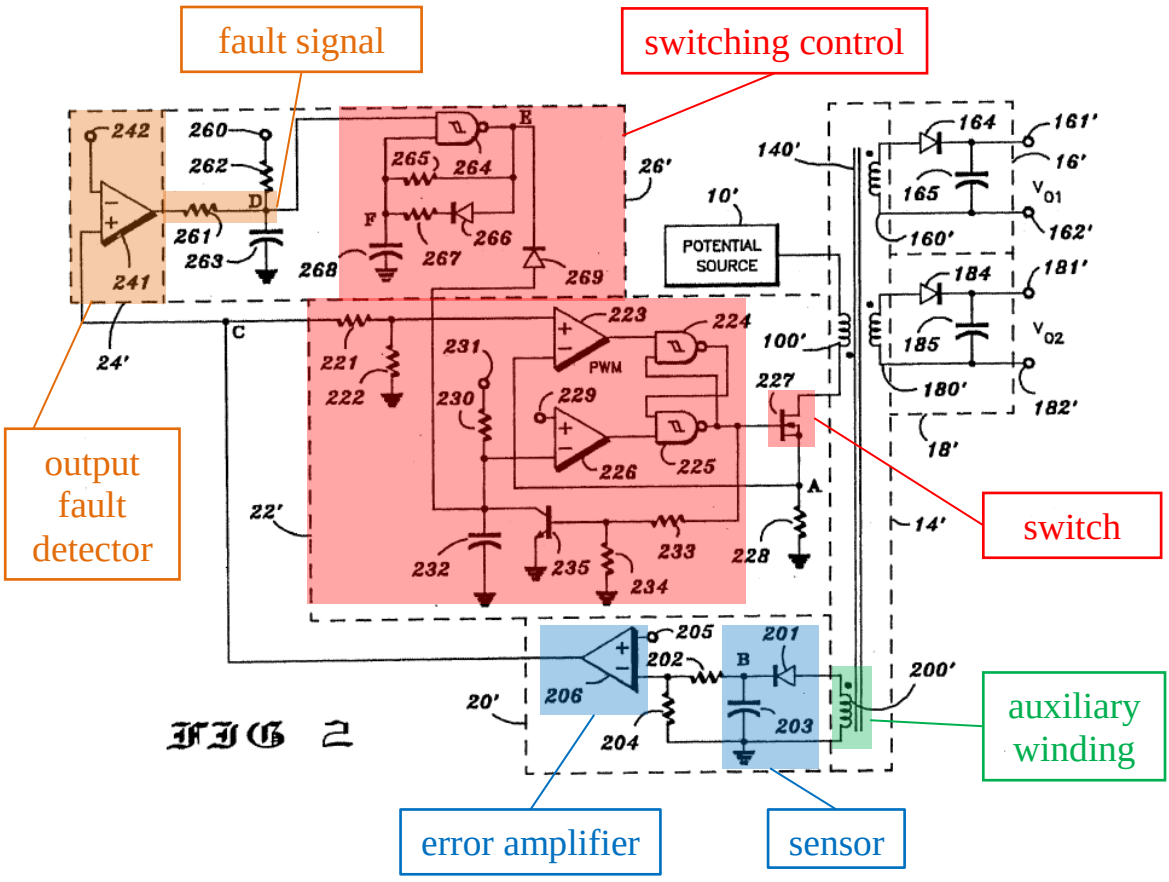
As described in Section VI.A.1, it would have been obvious to combine Kent's short circuit detection scheme with Reinhard. In such a combination, the "second feedback loop" formed by Kent's error detection circuit 20, level detector 24, and low frequency oscillator 26 (*see* Ex. 1016, 3:26-51, Fig. 1) would be incorporated between Reinhard's sample and hold circuit 108 (i.e., the sensor) and switching control circuitry (*see* Ex. 1007, Fig. 1).

Figure 1 provides a block diagram of Kent's short-circuit protection scheme:

FIG 1



Ex. 1016, Fig. 1 (annotations added); Ex. 1002, ¶ 102. Figure 2 of Kent provides a more detailed schematic diagram of the short-circuit protection scheme:



Ex. 1016, Fig. 2 (annotations added); Ex. 1002, ¶ 102.

As shown in Figure 2, Kent's error detection circuit 20[10] includes a sensor for sampling the positive voltage (representing the output voltage) from the auxiliary winding and error amplifier 206. *See* Ex. 1016, Fig. 2; 4:14-19, 6:63-7:8;

[10] Figure 2 of Kent adds a prime to the number labels for the similar elements from Figure 1. Ex. 1016, 3:52-57.

Ex. 1002, ¶ 103. Per the discussion in Section VI.A.1, Reinhard already includes sample and hold circuit 108 to sample the voltage from the auxiliary winding representing the output voltage during the off-time of the power switch. Ex. 1007, ¶¶ 0005, 0022; *See supra* Section VI.A.1, FN7. Thus, the proposed combination of Reinhard and Kent includes the portion of Kent's error detection circuit 20 (e.g., error amplifier 206) located after the sampling circuitry. Ex. 1002, ¶ 103.

Based on the comparison of the sampled output voltage to a reference, error amplifier 206 in Kent's error detection circuit 20 outputs an error signal to level detector 24 (i.e., the output fault detector). Ex. 1016, 3:26-32. If the error signal is large enough to indicate a short circuit condition, level detector 24 (i.e., the output fault detector) outputs a fault signal to low frequency oscillator 26. *Id.*, 3:32-44. In turn, low frequency oscillator 26 disables the switching operation of master oscillator 22 (which includes the power switch):

> A short circuit in an output causes a large current to pass through the secondary winding associated with that output resulting in a large undervoltage as sensed by winding 200. In response, error detection circuit 20 provides a very high level output signal … . By setting a threshold of level detector 24 to respond only to a very high level of output from error detection circuit 20, the dramatic undervoltage associated with a short circuit in an output can be used to trigger low frequency oscillator 26 to disable master oscillator 22.

Id.

Thus, level detector 24 serves as an output fault detector that specifically detects a short circuit fault condition at the output of the power supply and provides a fault signal to low frequency oscillator 26, which forms part of the switching control.[11] *See id.*, 3:24-51, Fig. 1.

Accordingly, the combination of Reinhard and Kent discloses and suggests to a POSITA each limitation of claim element 8[d]. Ex. 1002, ¶¶ 101-106.

[8d]	*See* Reinhard and Kent citations in Section VI.A.1 **Reinhard:** *See* Reinhard citations for claim elements 8[a]-[c]. **Kent:** Ex. 1016, Abstract: "An overcurrent protection circuit and method therefor for use in a multiple output switched power supply wherein the overcurrent condition accompanying a short circuit or an overload in an output circuit is detected as an undervoltage in a transformer." Ex. 1016, 2:9-13: "The method according to the present invention comprises detecting an overcurrent condition as a consequent undervoltage on the second secondary winding and disabling the master oscillator in response to said detecting of an overcurrent condition." (emphasis added). Ex. 1016, 2:36-41: "An error detection circuit 20 is coupled to a first terminal of a third secondary winding 200 of transformer 14, while a second terminal of winding 200 is coupled to a ground. A master

[11] As described in further detail below for Claim 13, low frequency oscillator 26 is included in the switching control in the proposed combination to implement the "auto restart mode" of the switching control, whereby the switching control periodically attempts to restart until the fault condition is removed and normal operation resumes.

oscillator 22 is coupled to error detection circuit 20 and to primary winding 100."

Ex. 1016, 3:26-44: "[O]vercurrent protection can be provided to such a switching power supply by using error detection circuit 20 as part of a second feedback loop, as shown in FIG. 1, in which error detection circuit 20 is coupled to a level detector 24 which is in trun [sic] coupled to low frequency oscillator 26 which is also coupled to master oscillator 22. A short circuit in an output causes a large current to pass through the secondary winding associated with that output resulting in a large undervoltage as sensed by winding 200. In response, error detection circuit 20 provides a very high level output signal in an attempt to greatly increase the duty cycle of master oscillator 22 in order to overcome the sensed undervoltage. By setting a threshold of level detector 24 to respond only to a very high level of output from error detection circuit 20, the dramatic undervoltage associated with a short circuit in an output can be used to trigger low frequency oscillator 26 to disable master oscillator 22." (emphasis added).

Ex. 1016, Fig. 3:

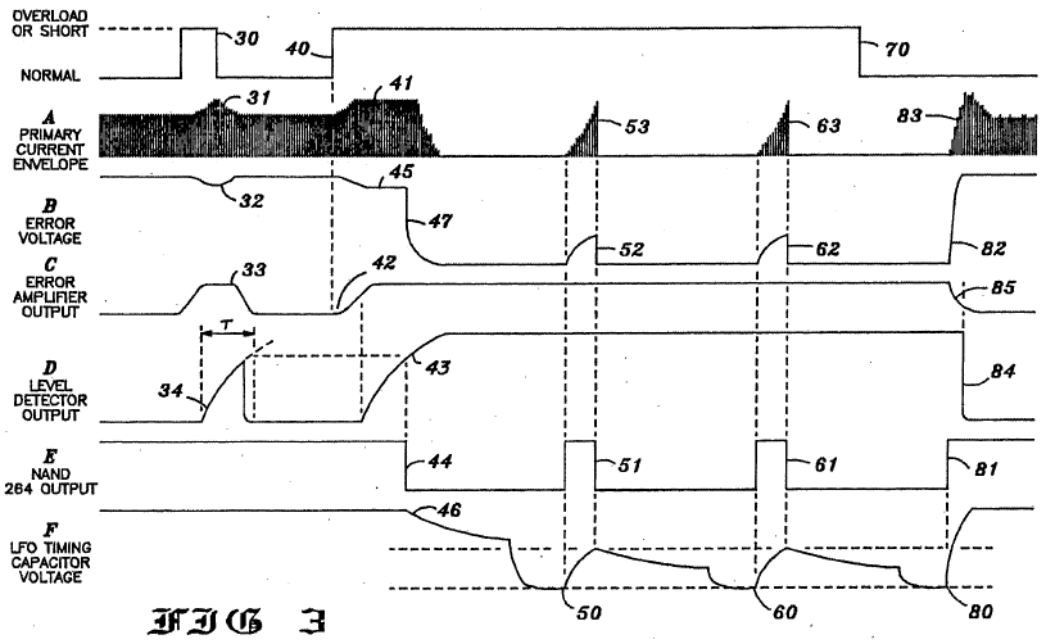


FIG 3

See also Ex. 1016, 1:7-12, 1:20-23, 2:42-45, 2:46-59, 2:62-3:25, 3:44-51, 4:14-26, 4:62-66, 4:67-5:18, 6:59-7:2, 7:20-31, 7:32-8:14, 8:32-9:10, Figs. 1-2, Claims 1, 8.

3. Claims 9 and 10

Claim 9 depends from Claim 8 and requires that "the output fault detector is coupled to detect an output overload fault condition in response to the signal representative of the output voltage of the power converter." Claim 10 is similar to Claim 9 but recites an "output short circuit fault condition" instead of an "output overload fault condition." As described below, an output short circuit fault condition is an example of an output overload fault condition. Thus, a prior art disclosure of an output short circuit fault condition also covers an output overload fault condition. Ex. 1002, ¶ 107.

An output short circuit fault condition occurs when the output of the power converter is shorted, for example, to ground. Ex. 1002, ¶ 108. Such a short circuit provides a direct path to ground, and thus causes an overly *high* load current. *See* Ex. 1021, 1:29-31 ("If load 150 develops a short or otherwise draws too much current, an overload occurs which could damage load 150 and voltage converter 100."); *see also* Ex. 1023, 2:59-62, Ex. 1022, 1:23-26. Indeed, Kent itself refers to "overload" a "short circuit" conditions together. Ex. 1016, Abstract ("An overcurrent protection circuit and method therefor for use in a multiple output switched power supply wherein the ***overcurrent condition accompanying a short circuit or an overload*** in an output circuit is detected as an undervoltage in a transformer.") (emphasis added).

As described above for claim element 8[d], the specific fault that is detected by the output fault detector in the combination of Reinhard and Kent is an output short circuit fault condition. *See* Ex. 1016, 3:26-51. Accordingly, the combination of Reinhard and Kent, discloses and suggests to a POSITA each limitation of both Claims 9 and 10. Ex. 1002, ¶¶ 107-109.

9. The controller of claim 8 wherein the output fault detector is coupled to detect an output overload fault condition in response to the signal representative of the output voltage of the power converter. 10. The controller of claim 8 wherein the output fault detector is coupled to detect an output short circuit fault condition in response to the signal representative of the output voltage of the power converter.	*See* Reinhard and Kent citations in Section VI.A.1. *See* Reinhard and Kent citations in Section VI.A.2, Claim 8. **Kent:** *See* Kent citations above for claim element 8[d]. Ex. 1016, Abstract: "An overcurrent protection circuit and method therefor for use in a multiple output switched power supply wherein the overcurrent condition accompanying a short circuit or an overload in an output circuit is detected as an undervoltage in a transformer. When the undervoltage exceeds a threshold the power supply is switched off and then on again during the cycling of a low frequency oscillator until the short or overload is removed in order to maintain the average power through the output circuit at a safe level." (emphasis added).

4. Claim 13

Claim 13 depends from Claim 8 and further recites that "the output fault detector is coupled to output an auto restart signal[12] to the switching control to indicate to the switching control to enter an auto restart mode."

As described above for claim element 8[b], level detector 24 outputs a "fault" signal to low frequency oscillator 26 to disable switching when a short circuit condition is detected. *See* Ex. 1016, 3:26-44. And as described below, low-frequency oscillator 26 implements an auto restart mode based on the fault signal. Thus, the "fault" signal from level detector 24 also serves as the "auto restart" signal recited by Claim 13.

In the proposed combination, low frequency oscillator 26 is incorporated as part of the switching control. Ex. 1002, ¶¶ 111-112. Low frequency oscillator 26 periodically disables and re-enables the switching operation in response to the fault/auto-restart signal from level detector 24. Ex. 1016, 3:39-51. In other words, low frequency oscillator 24 implements an auto restart mode where switching is automatically allowed to restart during the detected fault. Ex. 1002, ¶ 112. If the short circuit remains during the attempted restart, switching operation is again

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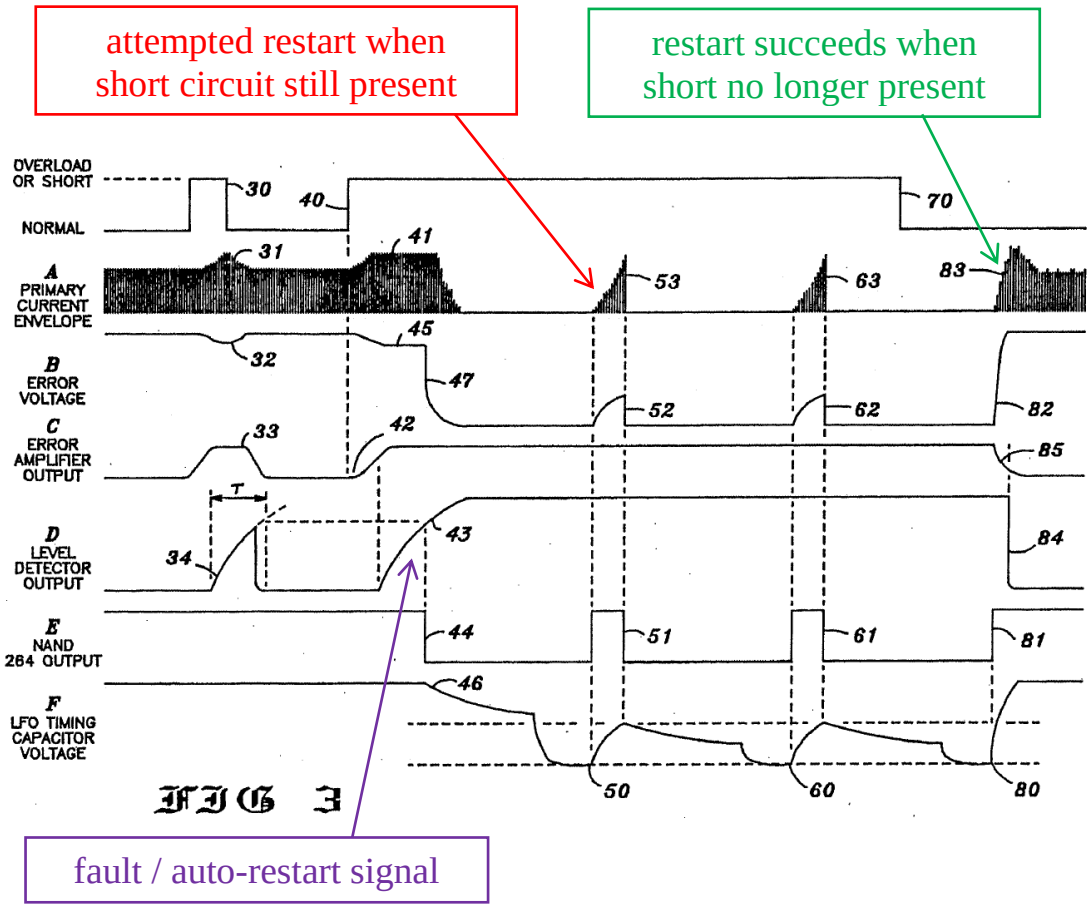
[12] As described in Section V.B, the "auto restart signal" recited in dependent Claim 13 represents a further definition of the generic "fault signal" recited in Claim 8 and does not require a separate signal.

disabled. *See* Ex. 1016, 8:53-62, Fig. 3. But if "the short circuit is removed … normal functioning resumes during the next cycle of low frequency oscillator in which the disablement of master oscillator 22 is removed." Ex. 1016, 3:46-51; *see also id.*, 8:67-9:9, Fig. 3.

Figure 3 of Kent illustrates the timing of the auto-restart mode. *Id.*, Fig. 3. Cross-referencing Figure 3 with the block diagram of Figure 1 and the schematic diagram of Figure 2 shows that signal "D" serves as the fault/auto-restart signal output by level detector 24. *See id.*, 8:15-25, Figs. 1-3. Further, signal "A" represents the current through the sense resistor 228 that is coupled in series with power switch 227, and thus illustrates when switching occurs during attempted restarts. *See id.*, 8:20-22, Figs. 2-3.



Ex. 1016, Fig. 3 (annotations added); Ex. 1002, ¶ 113.

Signal "D" (i.e., the fault/auto-start signal) goes high in response to an overload or short circuit condition. Ex. 1016, 8:15-25, Fig. 3. In response, low-frequency oscillator 26 (which is part of the switching control) generates signal "E" to periodically disable and re-enable switching. *See* Ex. 1016, 8:15-52, Fig. 3.[13] If the short circuit remains, switching is again disabled. *Id.*, 8:63-66,

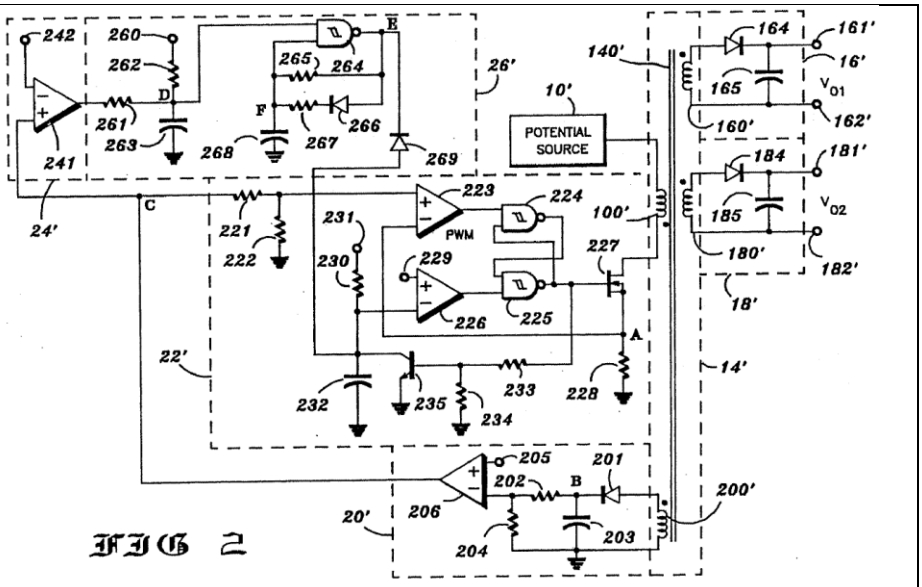
[13] In an alternative mapping of Kent, low frequency oscillator 26 may also be considered part of the output fault detector coupled between the sensor and the

Fig. 3. But if the short circuit is removed, normal switching operation resumes. *Id.*, 8:67-9:9, Fig. 3.

Accordingly, the combination of Reinhard and Kent, discloses and suggests to a POSITA each limitation of Claim 13. Ex. 1002, ¶¶ 110-115.

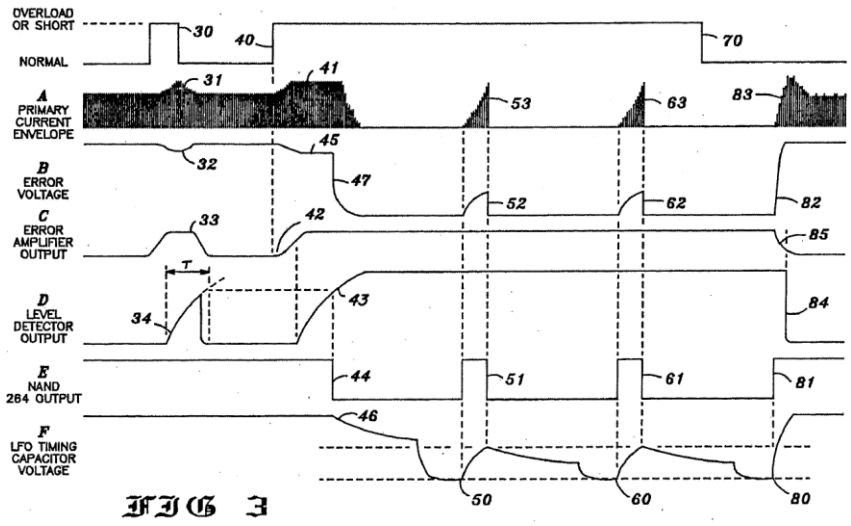
13. The controller of claim 8 wherein the output fault detector is coupled to output an auto restart signal to the switching control to indicate to the switching control to enter an auto restart mode.	*See* Reinhard and Kent citations in Section VI.A.1. *See* Reinhard and Kent citations in Section VI.A.2, Claim 8. **Kent:** Ex. 1016, 3:39-51: "By setting a threshold of level detector 24 to respond only to a very high level of output from error detection circuit 20, the dramatic undervoltage associated with a short circuit in an output can be used to trigger low frequency oscillator 26 to disable master oscillator 22. The disablement of master oscillator 22 is periodically removed due to the cycling of low frequency oscillator 26. Thus, after the short circuit is removed and the output level of error detection circuit 20 drops as a result, normal functioning resumes during the next cycle of low frequency oscillator in which the disablement of master oscillator 22 is removed." (emphasis added). Ex. 1016, Fig. 2:

switching control. In this alternative mapping, the low-level of the "E" signal shown in Figure 3 may serve as the "fault signal" in Claim 8, and the high-level of the "E" signal may serve as the "auto-restart" signal in Claim 13. Similarly, the "D" signal (which forces "E" low during the fault condition) may serve as the "fault signal" recited in Claim 8, and the "F" signal (which forces "E" high during the automatic restart) may serve as the "auto-restart" signal recited in Claim 13. *See* Ex. 1016, 8:32-52, Figs. 2-3; Ex. 1002, ¶ 114 (FN15).



Ex. 1016, 8:4-14: “If a short is still present, the threshold of the first input of NAND gate 264 is still high at the time when capacitor 268 is charged above the threshold of the second input to NAND gate 264 so that master oscillator 22' is again shut down for another cycle of low frequency oscillator 26'. If the short is not present when master oscillator 22' begins to oscillate, the error amplifier output falls so that the first input of NAND gate 264 falls below its threshold and is maintained below its threshold allowing continued normal operation of master oscillator 22'.”

Ex. 1016, 8:53-62: “Because the disablement of master oscillator 22' is removed, the primary current envelope as detected at node A rises as shown at 53 and the error voltage rises as shown at 52. The output of NAND gate 264 remains high, as shown at 51, during the period during which capacitor 268 is charged above the threshold of the second input to NAND gate 264. Because this threshold is exceeded, the short circuit condition still remains and the error amplifier output is still high, master oscillator 22' is again disabled.”

	Ex. 1016, Fig. 3:  FIG 3 Ex. 1016, 8:63-66: "If the short is sustained for another cycle of the frequency oscillator 60, 61, 62 and 63, which respectively correspond to 50, 51, 52 and 53, illustrate that master oscillator 22' is again shut down." Ex. 1016, 8:67-9:9: "If the short is removed, as indicated by trailing edge 70, at the next time that the voltage of capacitor 268 drops below the threshold of the second input to NAND gate 264, as shown at 80, the error voltage at node B, as indicated at 82, rises to a level that causes the output of error amplifier 206 to go low, as shown at 85, so that the primary current envelope returns to normal, as illustrated at 83, and so that the output of level detector 241 falls as shown at 84, thus simultaneously ending the enablement of low frequency oscillator 26' and the disablement of master oscillator 22'." *See also* Ex. 1016, 3:26-39, 7:48-8:4, 8:15-52, Figs. 1, 3.

B. Ground 2: Claims 9, 10, and 13 Are Obvious Over Spampinato Under 35 U.S.C. § 103

Spampinato, combined with the knowledge of a POSITA, discloses and suggests each element of Claims 9, 10, and 13, and thus renders Claims 9, 10, and 13 obvious under 35 U.S.C. § 103.

1. Independent Claim 8

Claim 8 is challenged in a concurrently filed Petition but is *not* challenged herein. Nonetheless, the disclosure of claim 8 by the combination of Spampinato and the knowledge of a POSITA is shown below to facilitate challenges to dependent claims.

8[pre]: "A controller for use in a power converter, comprising:"

Figure 4 of Spampinato illustrates a controller for use in a flyback-type power converter:

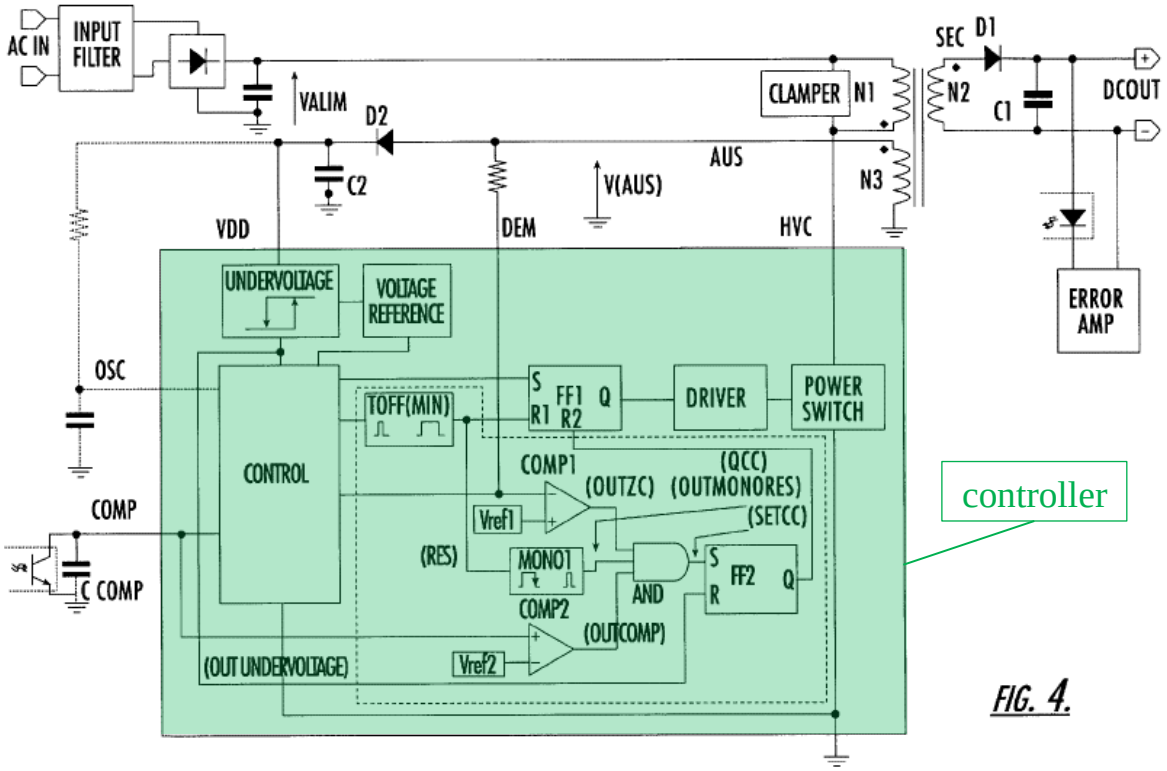


FIG. 4.

Ex. 1015, Fig. 4; *see also id.*, Abstract, 4:49-55, 5:14-28; Ex. 1002, ¶ 117.

Accordingly, Spampinato discloses and suggests to a POSITA each element of the preamble of Claim 8.[14] Ex. 1002, ¶¶ 117-118.

8[pre]	Ex. 1015, Abstract: "A method and device of protection from the effects of a persistent short circuit of the output of a DC-DC flyback converter self-oscillating either at a variable frequency or functioning at a fixed frequency in a discontinuous manner is provided. The voltage induced from the current flowing in a secondary winding of a transformer on the auxiliary winding is rectified and filtered to power, during a steady state of operation, the control circuitry of the converter." *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 4:6-26, 4:49-60, 5:14-28, Claims 6-7, Fig. 4.

Claim 8[a]: "a sensor coupled to receive a signal from a single terminal of the controller,"

Spampinato's controller includes comparator COMP1 (i.e., a sensor) that is coupled to receive a signal from the DEM pin of the integrated controller (i.e., a single terminal of the controller).

[14] The preamble is not limiting but is nonetheless disclosed by Spampinato.

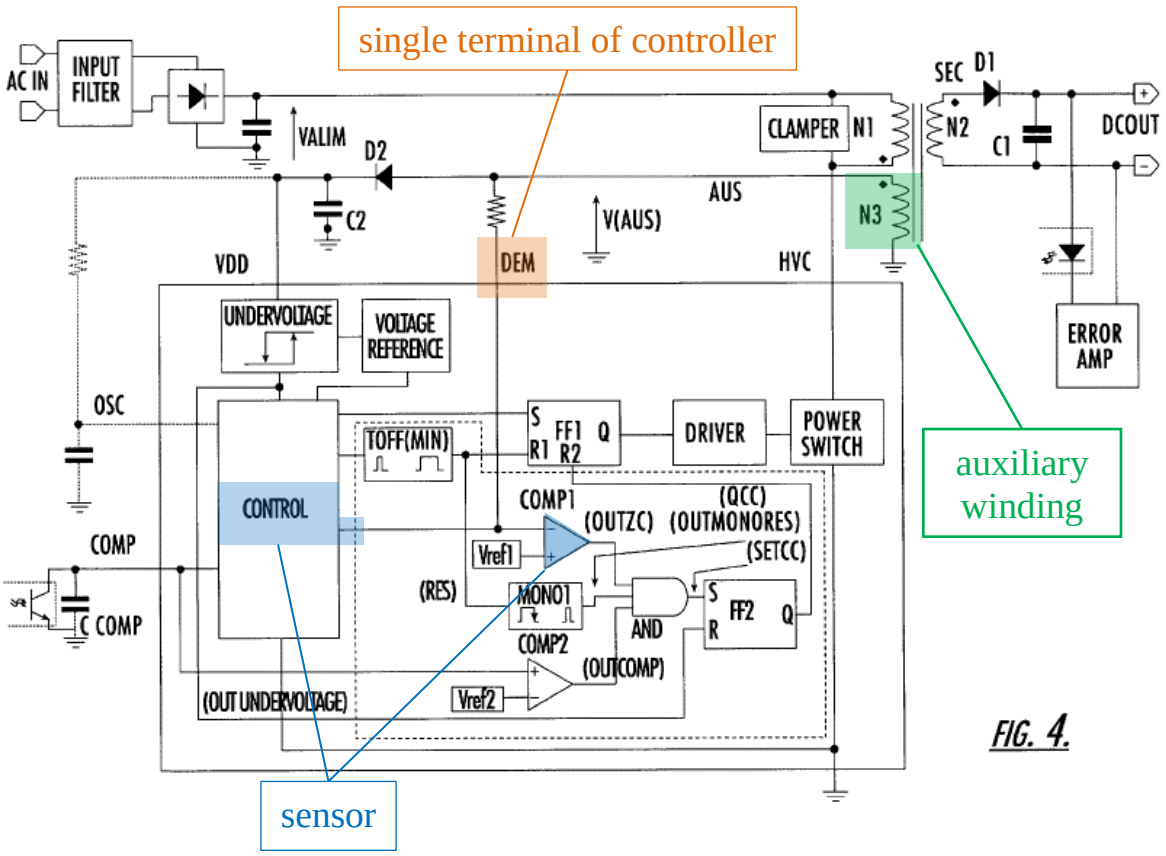


FIG. 4.

Ex. 1015, Fig. 4; Ex. 1002, ¶ 119. Spampinato explains that the comparator COMP1 (i.e., the sensor) monitors the voltage reflected by the auxiliary winding to implement an output short circuit protection scheme. *See, e.g.*, Ex. 1015, 4:31-36. As shown in Figure 4, the signal from the DEM pin is also routed to the "CONTROL" block, which uses the signal "for synchronizing the turning on of the power transistor." *Id.*, 2:11-23. Thus, the "CONTROL" block also forms part of the sensor. Ex. 1002, ¶ 119.

Accordingly, the Spampinato discloses and suggests to a POSITA each limitation of claim element 8[a]. Ex. 1002, ¶¶ 119-120.

[8a]	Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." (emphasis added). Ex. 1015, 6:21-27: "The protection of the integrated device from a short circuit does not require the use of any additional external component or of any pin in the case of SOPS or fixed frequency converters which already implement a sensing of the voltage VAUS through a dedicated pin DEM … ." (emphasis added). Ex. 1015, 2:11-14: "In the control circuits of SOPS converters there is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) under demagnetization conditions of the transformer." *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-39, 4:49-60, Claims 6-7, Figs. 1, 3, 4, 6B.

Claim 8[b]: "the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch, the signal from the single terminal to represent a line input voltage during at least a portion of an on time of the power switch,"

Figure 4 of Spampinato illustrates auxiliary winding N3 magnetically coupled to both primary winding N1 and secondary winding N2.

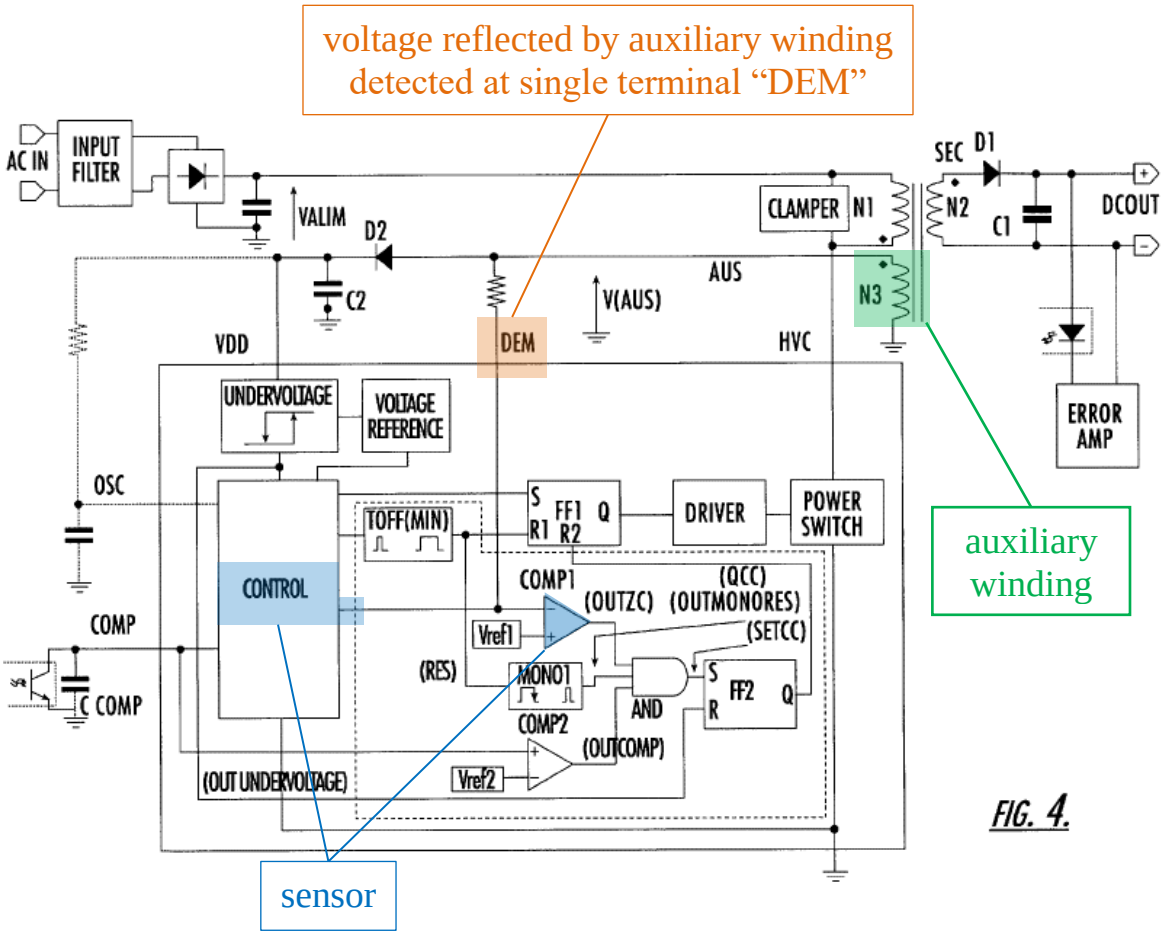
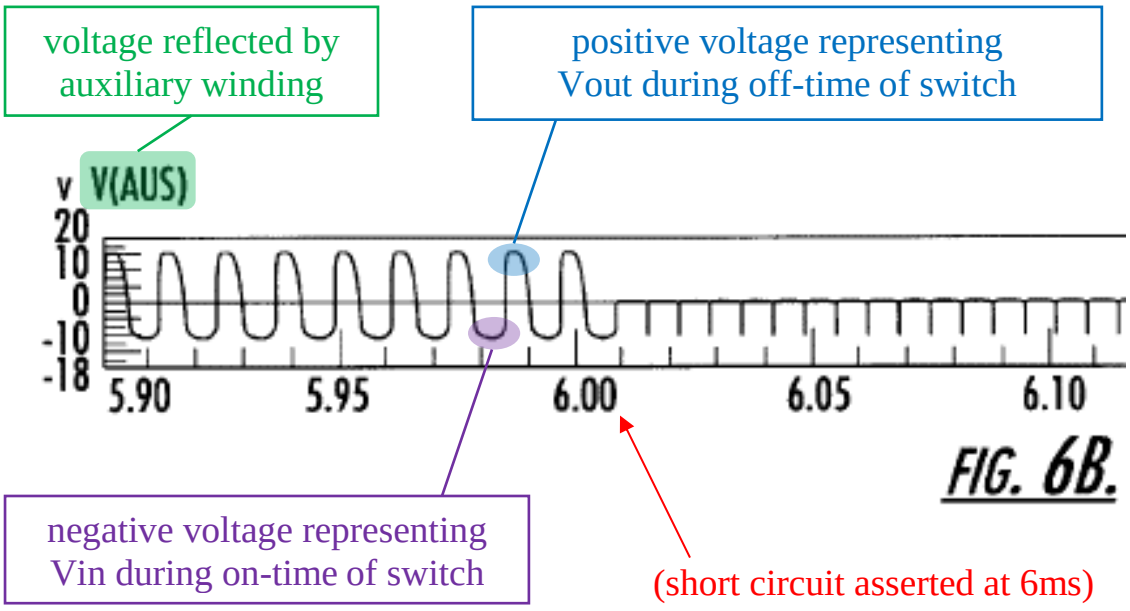


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 121. As described in Section III, a POSITA would understand that the magnetic coupling causes the auxiliary winding to (i) produce a positive voltage representative of the output voltage during at least a portion of the off-time of the switch, and (ii) produce a negative voltage representative of the input line voltage during the on-time of the switch. *See supra* Sections III.A-C; Ex. 1002, ¶ 121.

Consistent with this understanding, Figure 6B illustrates the signal received from the auxiliary winding at the DEM pin includes both positive voltage

(representative of the output voltage during the off-time of the switch) and negative voltage (representative of the input voltage during the on-time of the switch):

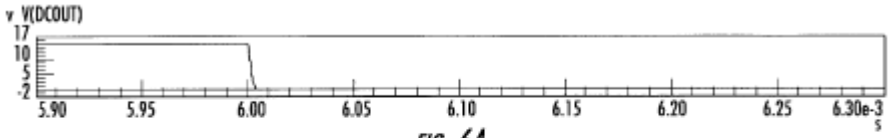
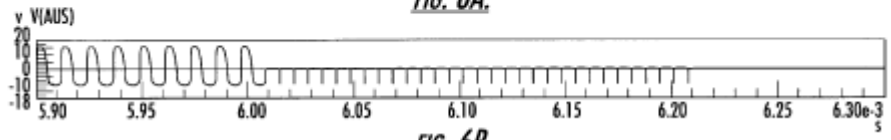


Ex. 1015, Fig. 6B (annotations added); *see also id.*, 6:7-14; Ex. 1002, ¶ 122.

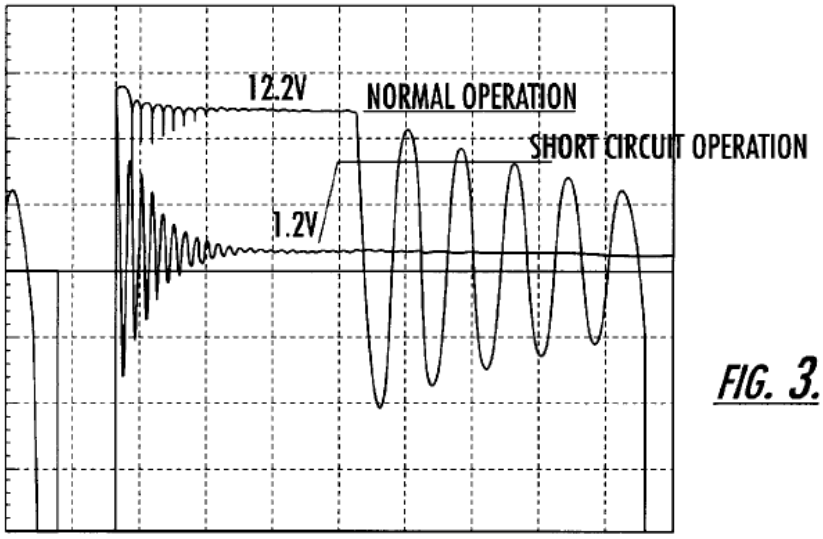
In sum, a POSITA would understand that the positive voltage swing of the signal received via the "DEM" terminal in Spampinato represents the output voltage of the power converter, while the negative voltage swing of that signal disclosed in Spampinato represents the line input voltage.[15] Ex. 1002, ¶ 121-123.

[15] As described in Section V.A, the recited "signal" must *represent* the line input voltage during the on-time of the switch. However, there is no requirement in Claim 8 regarding whether or how the separately recited structures (e.g., the

Therefore, a POSITA would understand Spampinato to disclose and suggest each limitation of claim element 8[b]. Ex. 1002, ¶¶ 121-123.

[8b]	*See* citations for claim element 8[a]. Ex. 1015, Fig. 6 (excerpt):  FIG. 6A.  FIG. 6B. Ex. 1015, 6:7-12: "FIGS. 5 and 6 show operation diagrams of a simulation of the protecting circuit of the invention. The diagrams refer to the case of normal functioning of the converter loaded with a 2 ohm resistor for an output power of about 100 watt, and illustrate a start-up phase up to reaching a steady state of operation." Ex. 1015, 2:32-45: "In practice, if the output voltage becomes null because of a short circuit on the OUT terminals, in the secondary winding (and therefore on the diode D1) there will be, during the off phase of the power transistor, a current whose maximum value is given by: $Isec_{cc} = (N1:N2)\ Ip_{max}$ The voltage mirrored on the auxiliary winding AUS, coincides with the voltage on the secondary (which during a short circuit, will be equal to the voltage drop Vf on the diode D1), multiplied by their turn ratio (N3:N2), that is: $V_{AUS(cc)} = (N3:N2)\ V_{sec(cc)} = (N3:N2)\ Vf\ (D1)$" Ex. 1015, 3:60-63: "FIG. 3 shows the diagrams of the voltage on the auxiliary winding of the flyback transformer in case of normal operating condition and in case of short circuit of the output of the converter;"

sensor) must respond, for example, to the line input voltage that is represented by the recited "signal" during the on-time of the switch.

	Ex. 1015, Fig. 3:  FIG. 3. Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." *See also* Ex. 1015, Abstract, 2:11-29, 3:21-35, 4:6-26, 4:26-39, 6:21-27, Claims 6-7, Figs. 1, 3, 4.

Claim 8[c]: "a switching control to be coupled to switch the power switch to regulate an output of the power converter in response to the sensor; and,"

Spampinato's controller includes a flip flop FF1 and a driver, which collectively form a switching control coupled to switch the power switch to regulate the output of the power converter:

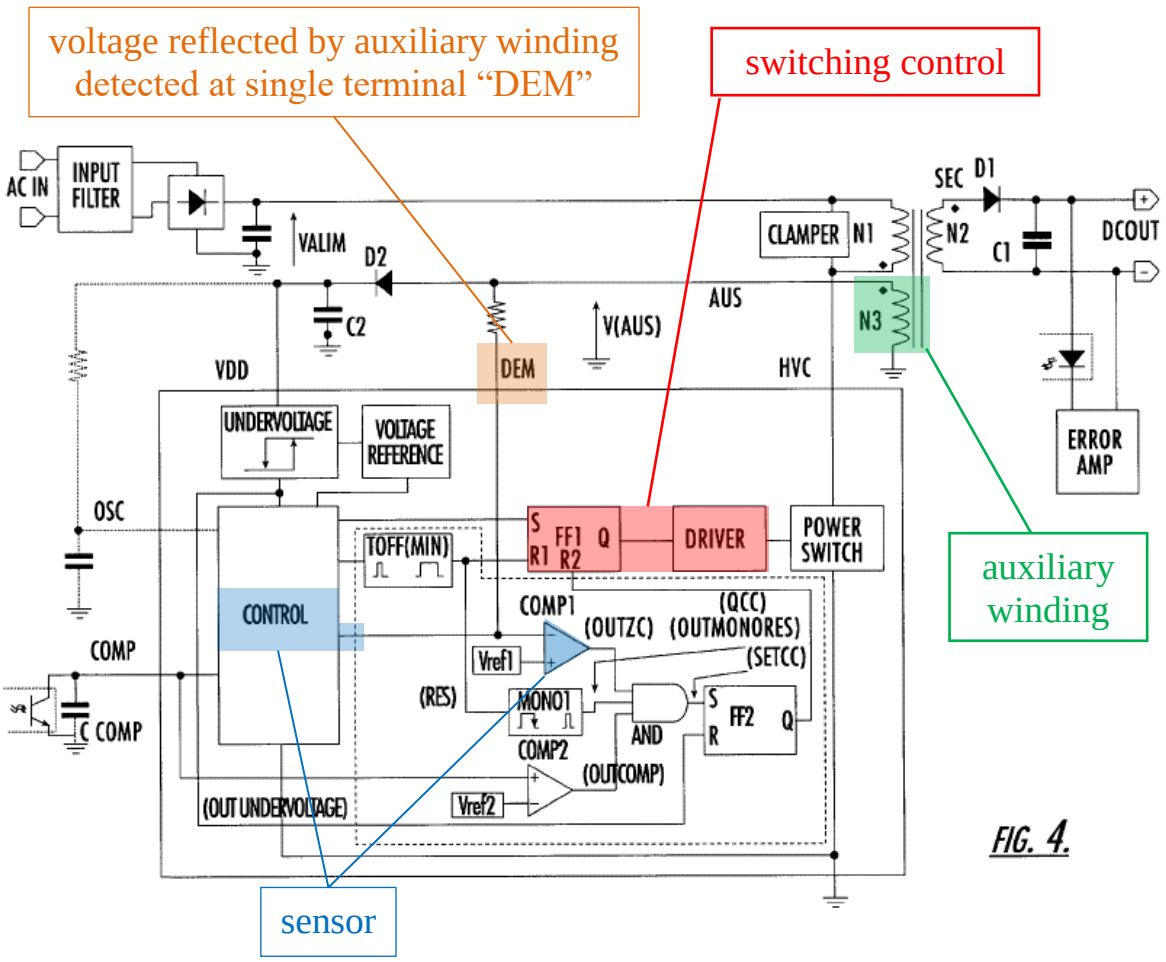


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 124. Under normal conditions, the power switch is turned on and off to regulate the "power that may be transferred" from the input to the output of the power converter. *See* Ex. 1015, 4:49-60.

The switching control is responsive to the sensor in multiple ways. Ex. 1002, ¶ 125. For example, during normal operation of the power supply, the signal from the DEM pin is detected by the "CONTROL" circuit. Ex. 1015, Fig. 4. And as shown in Figure 4, the "CONTROL" circuit is also coupled to set flip-flop

FF1 to turn on the power switch during each cycle. *Id.*; *see also id.* 2:11-13 ("[T]here is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) … ."); Claim 7 ("a power switch for driving the primary winding and for being synchronized by the auxiliary winding to turn on under a predetermined condition in the primary winding"). Thus, part of the control for turning on and off the switch to regulate the output is based on the sensor even under normal operating conditions. Ex. 1002, ¶ 126.

The switching control is also responsive to portions of Spampinato's sensor (i.e., comparator COMP1) during fault conditions. As shown in Figure 4, comparator COMP1 compares the reflected voltage from the auxiliary winding (representative of the output voltage during the off-time of the switch) against a threshold. Ex. 1015, 4:30-39. The output of COMP1 is provided to an AND gate and then passed flip-flop FF2. *See id.*, Fig. 4. The other inputs to the AND gate ensure that COMP1 can only pass a short circuit detection signal to flip-flop FF2 during a valid time window (i.e., after start-up has completed and during the off-time of the switching cycle when V_{AUS} represents the output voltage). *Id.*, 5:47-57. When a short circuit condition is detected, flip-flop FF2 is set, which in turn resets flip-flop FF1 to hold the power switch off. *Id.*

Accordingly, the Spampinato discloses and suggests to a POSITA each limitation of claim element 8[c]. Ex. 1002, ¶¶ 124-127.

[8c]	Ex. 1015, 2:11-14: "In the control circuits of SOPS converters there is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) under demagnetization conditions of the transformer." (emphasis added). Ex. 1015, 4:49-60: "In a current mode type of control, as in implemented by the basic control circuit of the converter, there is a relationship between the error voltage VCOMP provided by photocoupling the output of the error amplifier of the output voltage ERROR AMP to the CONTROL circuitry through the dedicated pin COMP and the current flowing in the power switch POWER. Therefore, there exists a maximum error voltage value $VCOMP_{max}$ error, tied to the maximum current that may flow through the power transistor, that limits the current on a pulse by pulse basis, therefore limiting the maximum power that may be transferred from the primary circuit to the secondary circuit." (emphasis added). Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." (emphasis added). Ex. 1015, 5:47-57: "The logic combination of the signals existing on the outputs of the two comparators COMP1 and COMP2 performed through the AND gate during the interval of time defined by the monostable circuit MONO1, after the masking interval defined by the $T_{OFF(min)}$ circuit, ensures that only a short circuit condition of the comparator output produce a simultaneous high state of all the three signals so to cause the setting of the flip-flop FF2 and thereby a stable condition of a high logic value of the flip-flop FF2, a condition that keeps the POWER switch turned off by keeping the driving flip-flop FF1 in a reset state." (emphasis added). *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-42, 4:49-60, 5:29-45, Claims 6-7, Figs. 1, 3, 4, 6B.

Claim 8[d]: "an output fault detector coupled between the sensor and the switching control, wherein the output fault detector is coupled to detect a fault condition in response to the signal representative of the output voltage of the power converter and to output a fault signal to the switching control in response to the detection of the fault condition."

Figure 4 of Spampinato illustrates an AND gate and flip-flop FF2, which collectively form an output fault detector coupled between the sensor and the switching control:

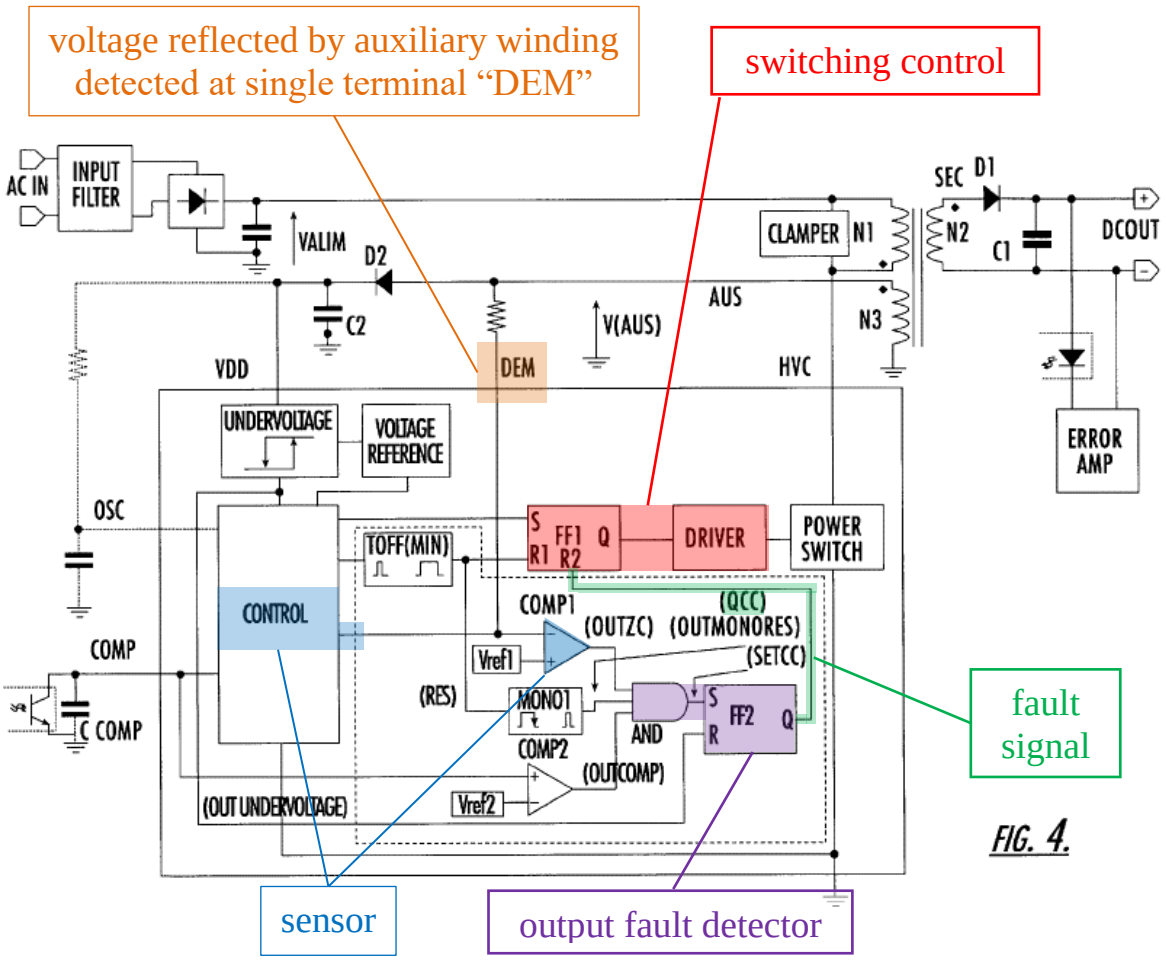


FIG. 4.

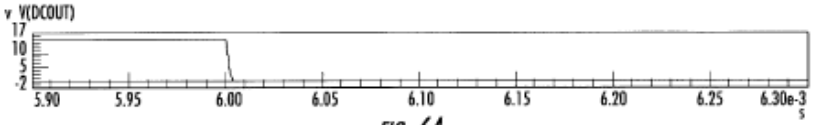
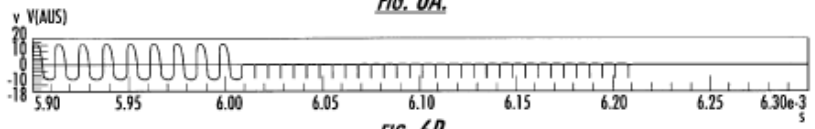
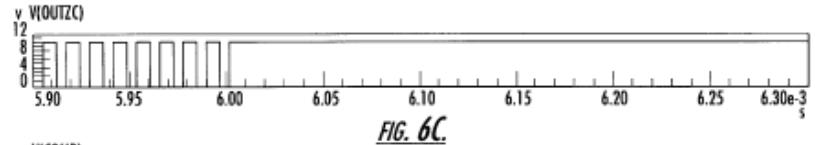
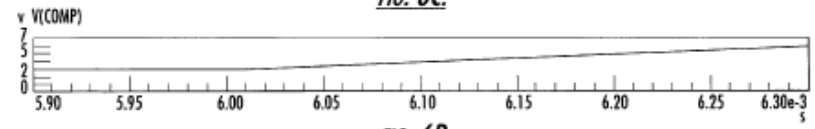
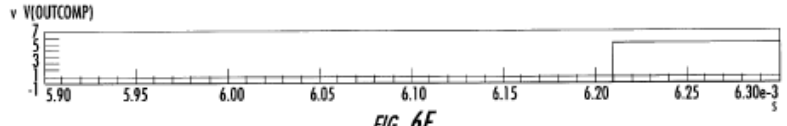
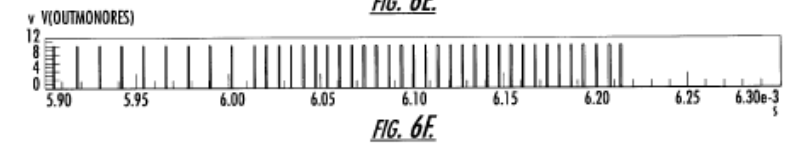
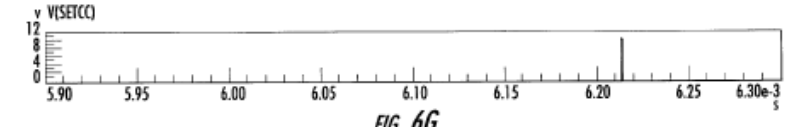
Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 128.

As shown in Figure 4, the AND gate includes three inputs. Ex. 1015, Fig. 4. The AND gate inputs from monostable circuit MONO1 and from comparator COMP2 provide a "masking interval" that ensure that the sensing of a short circuit condition by comparator COMP1 (i.e., the sensor) is carried out at the proper time during the switching cycle. Ex. 1015, 5:28-39; *see also id.*, 5:40-57. In other words, the masking interval ensures that the short circuit condition (i.e., the fault condition) is detected by comparator COMP1 during the off-time of the switch when the signal received from the auxiliary winding via the DEM pin is representative of the output of the power converter. *See id.*, 5:28-57; Ex. 1002, ¶ 129. When the fault condition is detected, the AND gate outputs a "SETCC" signal to set flip-flop FF2. *See* Ex. 1015, 5:47-57, Fig. 4. In turn, flip-flop FF2 outputs a fault signal to reset flip-flop FF1 in Spampinato's switching control, thereby disabling the switching operation. *Id.*

Accordingly, the Spampinato discloses and suggests to a POSITA each limitation of claim element 8[d]. Ex. 1002, ¶¶ 128-130.

[8d]	Ex. 1015, 5:47-57: "The logic combination of the signals existing on the outputs of the two comparators COMP1 and COMP2 performed through the AND gate during the interval of time defined by the monostable circuit MONO1, after the masking interval defined by the $T_{OFF(min)}$ circuit, ensures that only a short circuit condition of the comparator output produce a simultaneous high state of all the three signals so to cause the setting of the flip-flop FF2 and thereby a stable condition of a high logic value of the flip-flop FF2, a condition that keeps the POWER switch

	turned off by keeping the driving flip-flop FF1 in a reset state." (emphasis added). Ex. 1015, 5:28-39: "According to the preferred embodiment shown in FIG. 4, the protecting circuit comprises also a $T_{OFF(min)}$ block whose function is to impose a minimum turn-off time and the sensing of a short circuit condition is carried out after such a masking interval, in a way to be sufficiently delayed from the turn-off instant of the power switch when oscillations on the V_{AUS} voltage have decayed, in order to avert spurious comparisons by the two comparators COMP1 and COMP2. The minimum turn-off time or masking interval may be fixed so to safeguard a correct functioning of the converter at its typical switching frequencies." Ex. 1015, 5:40-46: "The signal comparisons by the two comparators COMP1 and COMP2 are performed within a definite time interval, precisely determined by the monostable circuit MONO1. Such time interval immediately follows the instant that defines the turn-off time and is sufficiently short to guarantee that the turn-off condition of the power switch be verified under all conditions." Ex. 1015, 6:7-14: "FIGS. 5 and 6 show operation diagrams of a simulation of the protecting circuit of the invention. The diagrams refer to the case of normal functioning of the converter loaded with a 2 ohm resistor for an output power of about 100 watt, and illustrate a start-up phase up to reaching a steady state of operation. Thereafter a short circuit condition is imposed (at the instant t=6 ms in the diagrams of FIGS. 5 and 6) to verify the effectiveness of the intervention of the protecting circuit of the invention."

	Ex. 1015, Fig. 6:  FIG. 6A.  FIG. 6B.  FIG. 6C.  FIG. 6D.  FIG. 6E.  FIG. 6F.  FIG. 6G.  FIG. 6H. *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-42, 4:49-60, 5:29-45, Claims 6-7, Figs. 1, 3, 4, 5A-5E, 6A-6H.

2. Claims 9 and 10

As described above in Section VI.A.3, an "output short circuit fault condition" (Claim 10) is an example of an "output overload fault condition" (Claim 9). Thus, a prior art disclosure of an output short circuit fault condition

also covers an output overload fault condition. Ex. 1002, ¶¶ 131-132.

As described above for claim element 8[d], the specific fault that is detected by Spampinato's output fault detector is an output short circuit fault condition. *See* Ex. 1015, 3:21-24, 5:47-57. Accordingly, the Spampinato discloses and suggests to a POSITA each limitation of each element of Claims 9 and 10. Ex. 1002, ¶ 133.

9. The controller of claim 8 wherein the output fault detector is coupled to detect an output overload fault condition in response to the signal representative of the output voltage of the power converter. 10. The controller of claim 8 wherein the output fault detector is coupled to detect an output short circuit fault condition in response to the signal representative of the output voltage of the power converter.	*See* Spampinato citations in Section VI.B.2, Claim 8[d]. Ex. 1015, Title: "Wholly integrated protection from the effects of a short circuit of the output of a flyback converter" (emphasis added). Ex. 1015, 3:21-24: "An object of this invention is to provide a wholly integrated circuit that implements a protecting function against the effects of a short circuit at the output of a DC-DC flyback converter." *See also* Ex. 1015, Abstract, 2:30-45, 3:25-47, 4:6-26, 4:26-42, 5:28-57, 5:58-6:6, 6:7-18, Claims 1, 2, 6-9, 11, Figs. 3, 4, 5A-5E, 6A-6H

3. Claim 13

Claim 13 depends from Claim 8 and further recites that "the output fault detector is coupled to output an auto restart signal[16] to the switching control to

[16] As described in Section V.B, the "auto restart signal" recited in dependent Claim 13 represents a further definition of the generic "fault signal" recited in Claim 8 and does not require a separate signal.

indicate to the switching control to enter an auto restart mode."

As shown in Figure 4 of Spampinato, output fault detector outputs a "QCC" signal (i.e., an auto-restart signal) to the R2 reset input of flip-flop FF2 in Spampinato's switching control:

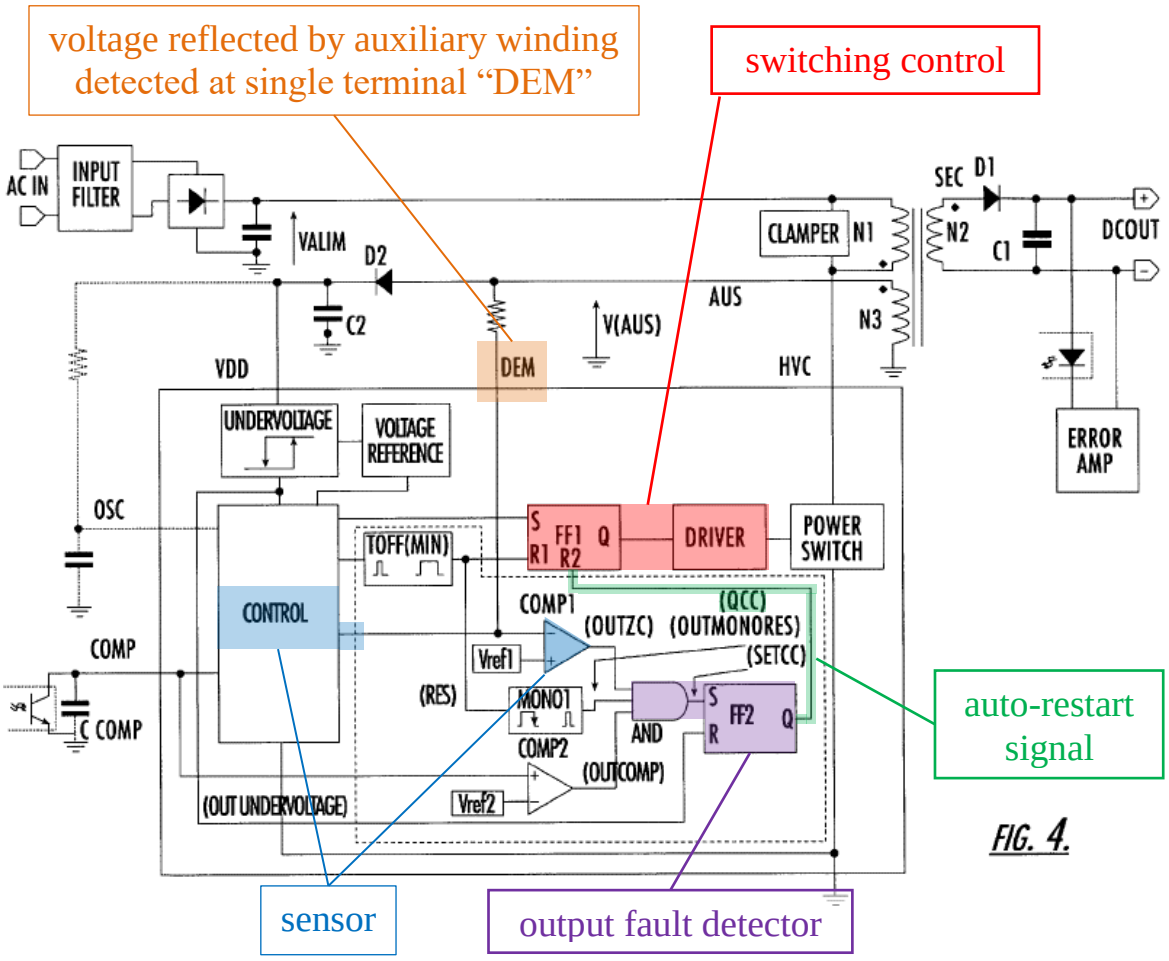


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); *see also id.*, Figs. 5A-5E, 5:47-57. Ex. 1002, ¶ 135. The AND gate sets flip-flop FF2 when a short circuit condition is detected, which in turn resets flip-flop FF1 in the switching control to disable switching. Ex. 1015, 5:47-57, Fig. 4. With switching disabled, the VDD voltage supply no

longer draws power from the auxiliary winding, and VDD decreases. *See id.*, 5:58-60, Figs. 2, 7; *see also id.*, 7:60-66. Subsequently, "[w]hen the VDD voltage supply drops under of the lower undervoltage threshold, the flip-flop FF2 is reset allowing for a ***new start-up transient***." *Id.*, 5:58-60 (emphasis added). In other words, the "UNDERVOLTAGE" block shown in Figure 4 resets flip-flop FF2, thereby forcing the QCC signal (i.e., the auto-restart signal) low, to allow switching to resume. *See id.*, Fig. 4; Ex. 1002, ¶ 135.[17]

If the short circuit persists, Spampinato's protection circuity will detect the condition and repeat the disabling and subsequent re-enabling of switching. Ex. 1015, 5:60-67. Thus, Spampinato's circuitry "guarantees an ***automatic start-up*** of the converter once the short circuit condition ceases to exist." *Id.*, 6:1-6 (emphasis added).

Accordingly, the Spampinato discloses and suggests to a POSITA each limitation of each element of Claim 13. Ex. 1002, ¶¶ 134-137.

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[17] In an alternative mapping of Spampinato, the high level of the "QCC" signal (which triggers the reset input of flip-flop FF1) may serve as the "fault signal" recited in Claim 8, and the low-level of the "QCC" signal (which releases the reset input of flip-flop FF1) may serve as the "auto-restart signal" recited in Claim 13. *See* Ex. 1015, Fig. 4, 5:47-67; Ex. 1002, ¶ 135 (FN19).

13. The controller of claim 8 wherein the output fault detector is coupled to output an auto restart signal to the switching control to indicate to the switching control to enter an auto restart mode.	*See* Spampinato citations in Section VI.B.2, Claim 8[d]. Ex. 1015, 5:58-67: "When the VDD voltage supply drops under of the lowest undervoltage threshold, the flip-flop FF2 is reset allowing for a new start-up transient. If the short circuit condition persists, the device will be enabled to function only during the charging transient of the compensation capacitor CCOMP. However, such a time interval will be far shorter than the charging transient of the supply capacitor C2 (at least an order of magnitude less) during which, by contrast, the known converters remain active, thus providing for a remarkable reduction of the average power dissipation." (emphasis added). Ex. 1015, 6:1-6: "Moreover, the wholly integratable circuit of the invention guarantees an automatic start-up of the converter once the short circuit condition ceases to exist, if compared to protecting devices based on the use of latches whose reset may be made only by disconnecting the converter from the mains." (emphasis added). *See also* Ex. 1015, 5:28-46, 5:47-57, Figs. 1, 2, 4, 5A-5E, 6A-6H, 7. Claims 6-7.

VII. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the ’871 Patent be instituted and that Claims 9, 10, and 13 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,
BAKER BOTTS L.L.P.

September 28, 2018
Date

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Lead Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 13907 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 28th day of September 2018, a complete and entire copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,773,871** and any accompanying exhibits was served on the patent owner at the correspondence address of record for the subject patent,

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via Express Mail or by means at least as fast and reliable as Express Mail. Additionally, the same were also served upon counsel for the subject patent's owner, Power Integrations, Inc.,

Michael R. Headley
Fish & Richardson P.C.
500 Arguello Street, Suite 500
Redwood City, CA 94063

because that is likely to affect service.

In accordance with § 42.51(b)(1), the undersigned certify that Petitioner is not aware of, and therefore does not provide any "relevant information that is inconsistent with a position advanced by petitioner[]."

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