UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC d/b/a
ON SEMICONDUCTOR
Petitioner

v.

POWER INTEGRATIONS, INC.
Patent Owner

Case No. Unassigned
Patent 8,077,483

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,077,483

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1013	Robert W. Erickson, Fundamentals of Power Electronics (Kluwer Academic Publishers, 1997)
1014	Paul Horowitz and Winfield Hill, The Art of Electronics (Cambridge University Press, 2nd ed. 1989) (reprinted 1998)

[1] Exhibit number 1005 is reserved to maintain consistent numbering for other exhibits that are also filed with concurrently filed Petition for the '483 Patent.

1015	U.S. Patent 6,061,257 ("Spampinato")
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I. INTRODUCTION

Semiconductor Components Industries, LLC d/b/a ON Semiconductor ("ON Semiconductor" or "Petitioner") requests *inter partes* review ("IPR") under 35 U.S.C. §§ 311–319 and 37 C.F.R. § 42.100 *et seq*. of Claims 6, 8, 9, 12 and 13 of U.S. Patent No. 8,077,483 ("'483 Patent").

Petitioner asserts that there is a reasonable likelihood that the challenged claims are unpatentable and requests review of, and cancellation of, the challenged claims under 35 U.S.C. 103.

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices

Real Party in Interest: The real parties in interest are: (i) ON Semiconductor Corporation, (ii) Semiconductor Components Industries, LLC, doing business as ON Semiconductor, and (iii) Fairchild Semiconductor International, Inc., (iv) Fairchild Semiconductor Corporation, (v) Fairchild (Taiwan) Corporation, and (vi) System-General Corporation.

Related Matters: The '483 Patent is involved in a pending lawsuit entitled *ON Semiconductor Corp., et al. v. Power Integrations, Inc.*, No. 17-cv-247-LPS-CJB (D. Del.) ("Delaware Litigation"). Petitioner was first served with pleadings including the '483 Patent in the Delaware Litigation as part of Patent Owner's counterclaims in Patent Owner's Answer and Counterclaims to Plaintiff's First

Amended Complaint (Ex. 1009), served on September 29, 2017. The claims challenged herein (i.e., Claims 6, 8, 9, 12 and 13) are *not* at issue in the Delaware Litigation. *See* Ex. 1012.

This Petition for IPR is being filed concurrently with an additional petition for IPR against different claims (i.e., Claims 1, 2, 3, and 7) of the '483 Patent, as well as two Petitions for IPR against U.S. Patent No. 8,773,871 ("the '871 Patent"). The '871 Patent is a continuation and claims benefit to the application of the '483 Patent. In addition, Petitioner is concurrently filing Petitions for IPR for two other patents held by Patent Owner (i.e., U.S. Patents Nos. 6,456,475 and 6,337,788). Further, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which are still pending: IPR2018-00160 (instituted 5-22-2018); IPR2018-00165 (instituted 5-18-2018); IPR2018-00166 (instituted 5-18-2018). In addition, Petitioner previously filed petitions for IPR against other patents held by Patent Owner, including the following IPRs which have been decided, and/or are on appeal: IPR2016-00809 (FWD issued 9-22-2017); IPR2016-00995 (FWD issued 10-15-2017); IPR2016-01589 (FWD issued 2-14-2018); IPR2016-01590 (FWD issued 2-8-2018); IPR2016-01592 (FWD issued 2-8-2018); IPR2016-01594 (FWD issued 2-14-2018); IPR2016-01595 (FWD issued 2-14-2018); IPR2016-01597 (FWD issued 1-25-2018); IPR2016-01600 (FWD issued 2-14-2018).

Lead Counsel: Lead Counsel is Roger Fulghum (Reg. 39,678) and Back-up Counsel are Brian Oaks (Reg. 44,981), Nick Schuneman (Reg. 62,088), and Brett Thompsen (Reg. 69,985), each of Baker Botts L.L.P.

Service Information: Baker Botts L.L.P., One Shell Plaza, 910 Louisiana Street, Houston, Texas 77002-4995; Tel. (713) 229-1234; Fax (713) 229-1522. Petitioner consents to service by electronic mail at: ONSemi_483IPR@bakerbotts.com. A Power of Attorney is filed concurrently herewith under 37 C.F.R. § 42.10(b).

B. Certification of Grounds for Standing

Petitioner certifies that the '483 Patent is available for IPR. Petitioner is not barred or estopped from requesting IPR of the '483 Patent.

C. Fees

The Office is authorized to charge any fees that become due in connection with this Petition to Deposit Account No. 02-0384.

III. OVERVIEW OF THE '483 PATENT

A. Background of the Technology

The '483 Patent relates to switching power converters. Ex. 1001, Abstract. Such devices convert a first voltage (e.g., from a wall socket) to a second voltage to power an electronic device. *Id.*, 1:25-35. The '483 Patent describes and claims a class of switching power converters that use the auxiliary winding of a

transformer to detect information relevant to the control of the converter. But, as described by the background materials below, use of an auxiliary winding in switching power converters was well-known prior to the '483 Patent. Ex. 1002, ¶ 33.

One example of a switching power converter that uses an auxiliary winding is provided by U.S. Patent 7,016,204 to Ta-Yung Yang et al. ("Yang"). Ex. 1006.

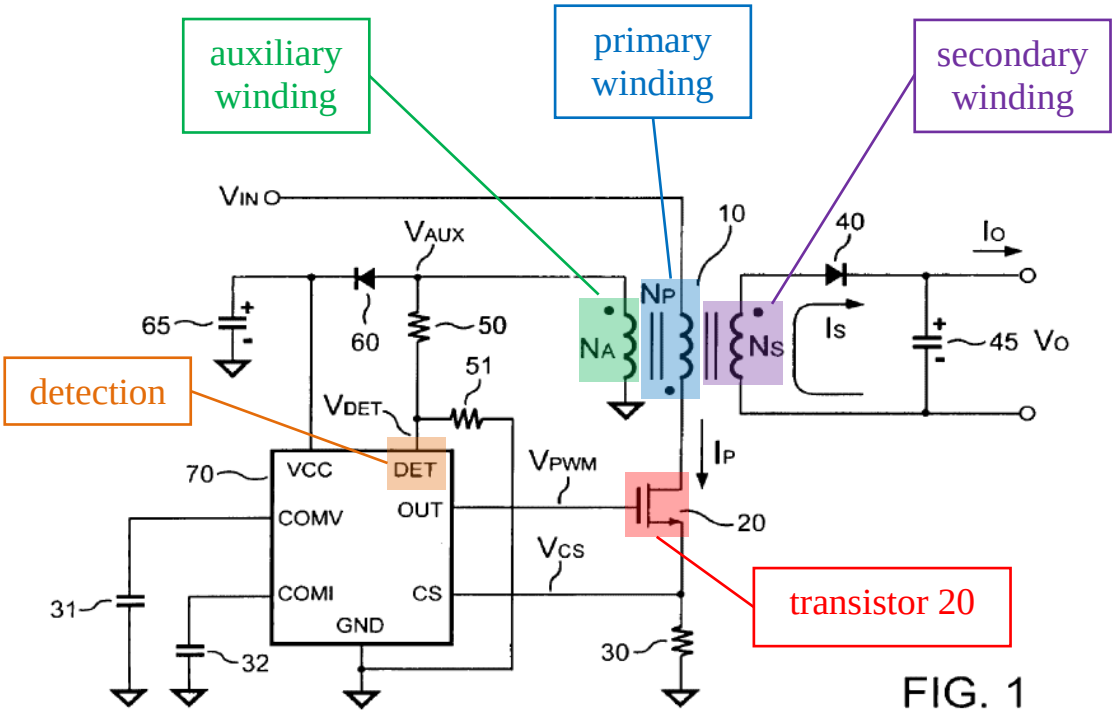


FIG. 1

Id., Fig. 1 (annotations added); Ex. 1002, ¶ 34. Yang's power converter includes transistor 20 coupled to transformer 10. Ex. 1006, Fig. 1. The transistor is turned on and off by a switching signal "V_{PWM}" to regulate how much energy is transferred from the input (V_{IN}) to the output (V_O) of the power converter. *Id.*, 2:34:40, Fig. 1.

When V_{PWM} goes high to turn on transistor 20, a current (I_P) flows from V_{IN}, through the primary winding N_P of transformer 10, and through transistor 20 and resistor 30 to ground. *Id.*, 2:41-43, Figs. 1-2. As the primary-side current I_P flows, the magnetic energy stored in transformer 10 builds. Then, when V_{PWM} goes low to turn off transistor 20, the magnetic energy stored in transformer 10 induces a secondary-side current I_S through the secondary winding N_S. *Id.*, 2:54-59, Figs. 1-2. The magnetic energy stored in transformer 10 is therefore transferred to the output by the secondary-side current I_S. Ex. 1002, ¶ 36. In sum, the magnetic energy in the transformer is built up via primary winding N_P during the on-time of transistor 20 and transferred to the output of the power converter via secondary winding N_S during the off-time of transistor 20. *Id.*, ¶¶ 35-36.

As shown in Figure 1 of Yang, transformer 10 also includes auxiliary winding N_A. Because auxiliary winding N_A is magnetically coupled to the primary winding N_P and secondary winding N_S, auxiliary winding N_A "reflects" activity on the primary and secondary windings. Ex. 1002, ¶ 37. For example, when the secondary-side current I_S flows in the secondary side during the off-time of the primary-side switch, the auxiliary winding reflects the voltage present at the

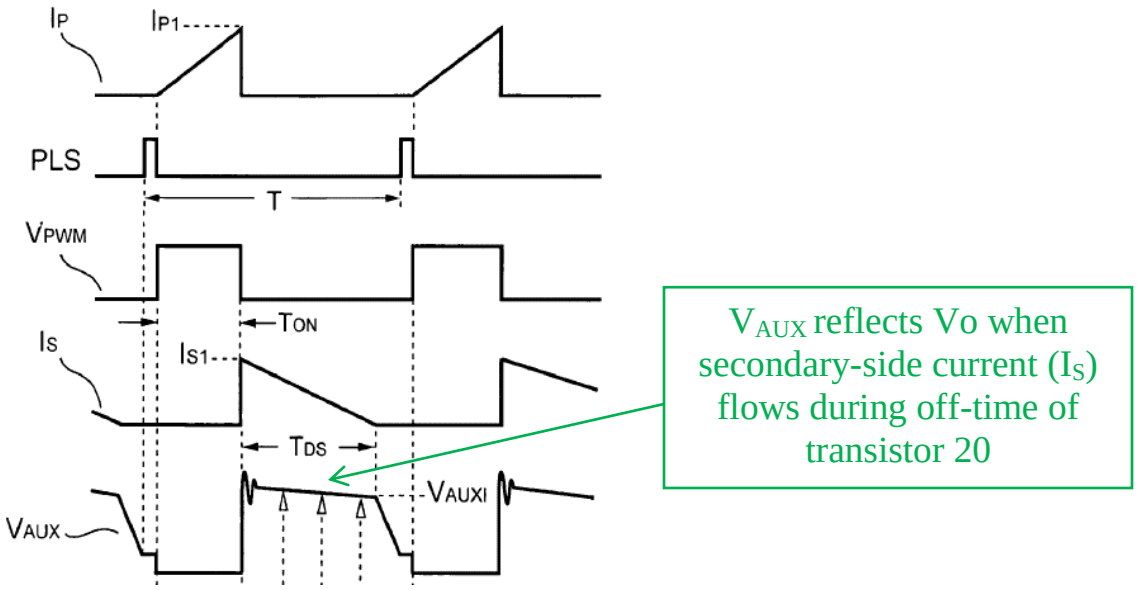
secondary winding.[2] Ex. 1006, 3:4-15. This voltage at the secondary winding is equal to the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40. Thus, the reflected voltage produced by the auxiliary winding equals the output voltage (V_O) plus the forward voltage drop (V_F) of rectifier 40, multiplied by the winding ratio of the auxiliary and secondary windings:

$$V_{AUX} = \frac{T_{NA}}{T_{NS}} \times (V_O + V_F)$$

Id., 3:10 (Equation 3); Ex. 1002, ¶¶ 38-39.

Figure 2 of Yang illustrates this reflected voltage (V_{AUX}) produced on the auxiliary winding when the secondary-side current (I_S) flows:

[2] The auxiliary winding reflects the voltage present at the secondary winding only during the portion of the off-time that current is flowing in the secondary side. *See* Ex. 1006, Fig. 2. Thus, when discussing herein the auxiliary winding's reflection of the voltage during the off-time of the power switch, the Petition is referring to the portion of the off-time when current flows through the secondary winding.



Ex. 1006, Fig. 2 (excerpt) (annotations added).

Prior to the '483 Patent, it was well known in the art that different functions could be performed based on the reflected voltage present at the auxiliary winding of a switching converter. Ex. 1002, ¶¶ 40-44. As described by Yang, it was known that the reflection of the output voltage on the auxiliary winding could be used as feedback for regulating the output voltage. Ex. 1006, 3:4-50, 4:5-8. It was also recognized that the reflection of the output voltage on the auxiliary winding could be used to detect various fault conditions at the output of the power converter, such as a short circuit fault condition (*see* Ex. 1015, 4:30-36; Ex. 1016, 3:26-63, Fig. 1) or an output over voltage fault condition (Ex. 1007, ¶ 0023; Ex. 1004, 3:58-67).

B. The Purported Advancement of the '483 Patent

Figure 1 of the '483 Patent illustrates a flyback-type power converter with a transformer that has an auxiliary winding:

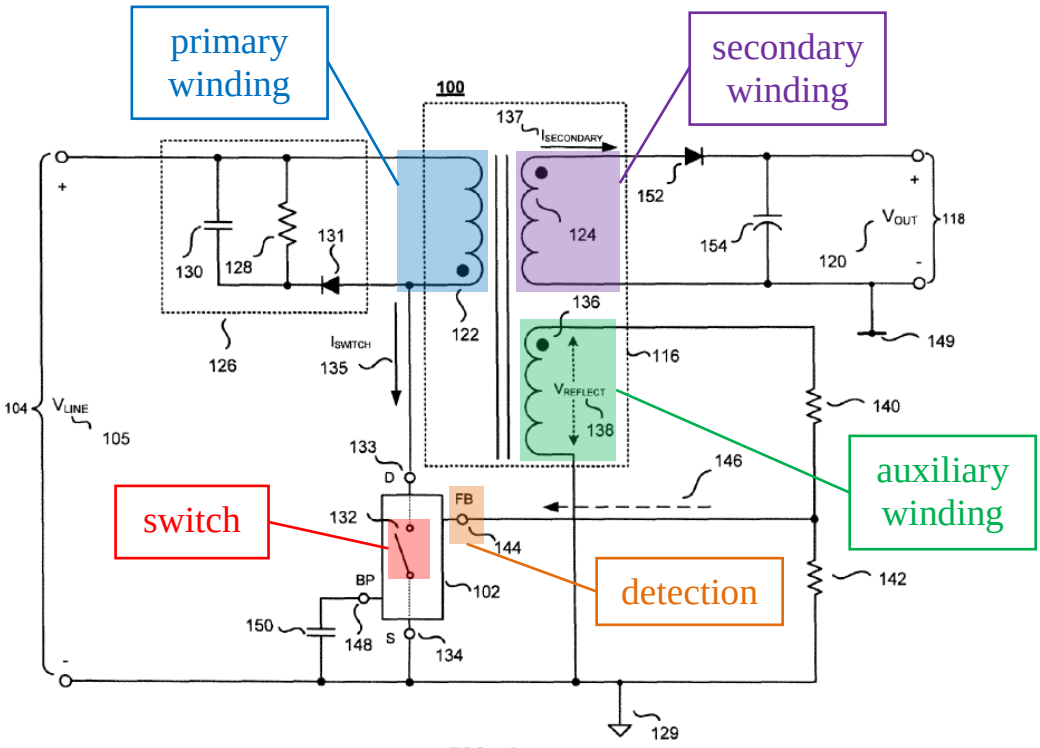
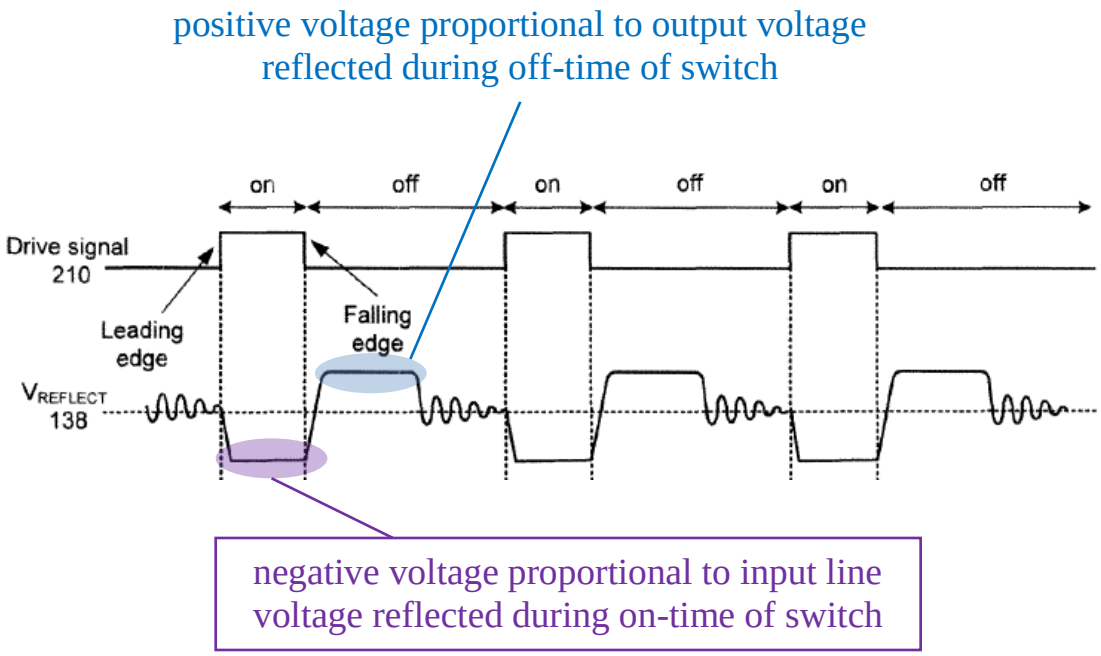


FIG. 1

Ex. 1001, Fig. 1 (annotations added); *see also id.*, 3:5-10; Ex. 1002, ¶ 45.

The '483 Patent purports to improve upon known switching power converters by using the auxiliary winding to detect the input voltage (also referred to as the "line" voltage) in addition to the output voltage. Ex. 1001, 2:52-55, 3:48-60. The '483 Patent explains that the "reflected voltage $V_{REFLECT}$" at the auxiliary winding is "representative of output voltage V_{OUT} 120 during at least a portion of the time when the power switch 132 is off." *Id.*, 3:55-60. The '483 Patent further

explains that the "reflected voltage $V_{REFLECT}$" is also "representative of an input line voltage V_{LINE} 105 during at least a portion of the time of when the power switch 132 is on." *Id.*; *see also id.*, 3:60-4:10.



Id., Fig. 4 (excerpt) (annotations added)[3]; Ex. 1002, ¶ 46.

However, the reflection of both the output voltage and the input line voltage on the auxiliary winding at different times during the switching cycle is merely the result of the magnetic coupling between the different windings of the transformer. In other words, it is the magnetic coupling of the auxiliary winding in the flyback

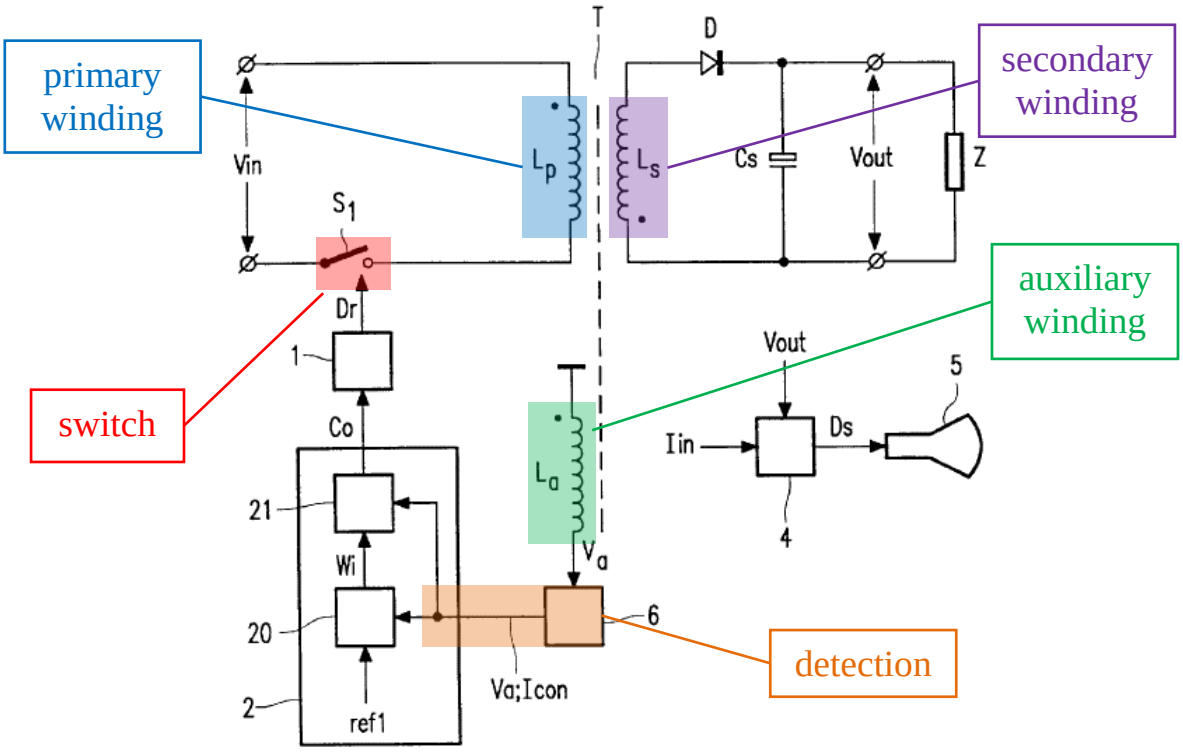
[3] The reflection of the line voltage is negative due to the opposing orientation of the windings in a flyback-type converter, as shown by the orientation of the dots on the individual windings in Figure 1 of the '871 Patent. Ex. 1002, ¶ 47.

architecture that *dictates* the voltage that is reflected by the auxiliary winding during the on-time and off-time of the power switch. Ex. 1002, ¶ 48. As explained above, the auxiliary winding reflects the voltage present on the secondary winding (i.e., V_{OUT} plus the voltage drop of the rectifier) when current flows through the secondary side (i.e., during off-time of the switch). Ex. 1006, 3:4-15. The auxiliary winding likewise reflects the voltage present on the primary winding (i.e., the input line voltage) when current flows through the primary side (i.e., during the on-time of the switch). Ex. 1002, ¶ 48.

Thus, the purported invention of the '483 Patent is based on nothing more than the recognition of how an auxiliary winding naturally responds during the on-time and off-time of the switch due to the physical relationship (i.e., the magnetic coupling) between the auxiliary winding and the other windings, which exists in every flyback-type power converter with an auxiliary winding. Ex. 1002, ¶ 49.

C. Characteristics of Auxiliary Windings Were Well Known in the Art

Multiple prior art references recognize and describe the relationship between the auxiliary winding and the primary and secondary windings. Ex. 1002, ¶¶ 50-53. One example is U.S. Patent 5,831,839 ("Pansier"), which issued on November 3, 1998. Ex. 1008. Like the '483 Patent, Pansier discloses a flyback-type switching power converter with an auxiliary winding:

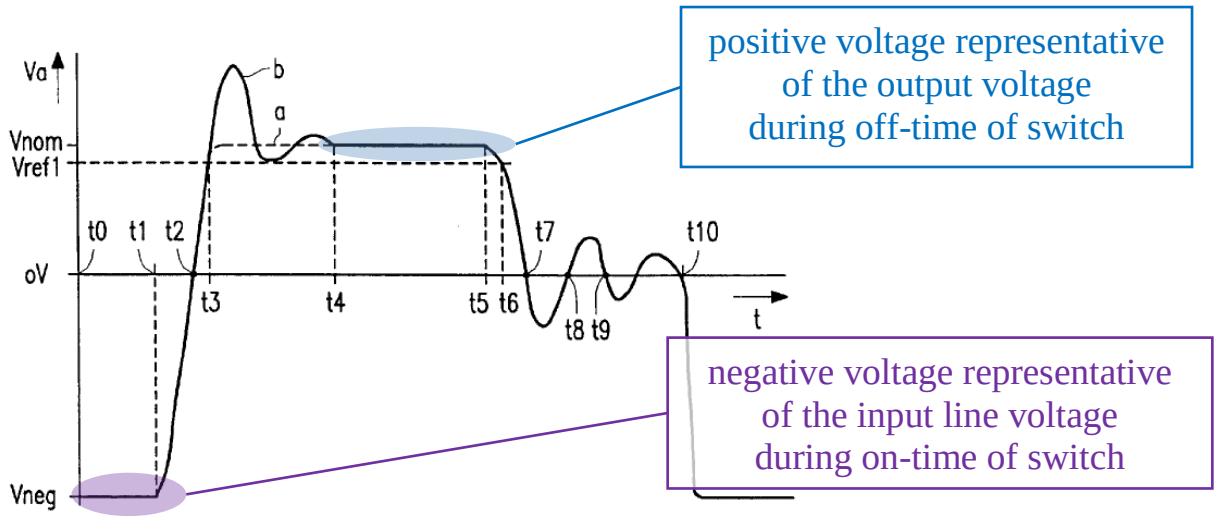


Ex. 1008, Fig. 1 (annotations added); Ex. 1002, ¶ 50.

Pansier explains that, during the off-time of the switch, the auxiliary winding voltage Va "is equal to the DC output voltage Vout multiplied by the transformation ratio between the auxiliary winding La and the secondary winding Ls." Ex. 1008, 7:45-50, Fig. 3.[4] On the other hand, "auxiliary winding voltage Va has a negative value Vneg" during the on-time of the switch, "which equals the input voltage Vi multiplied by the transformation ratio between the auxiliary winding La and the primary winding Lp." *Id.*, 7:31-37.

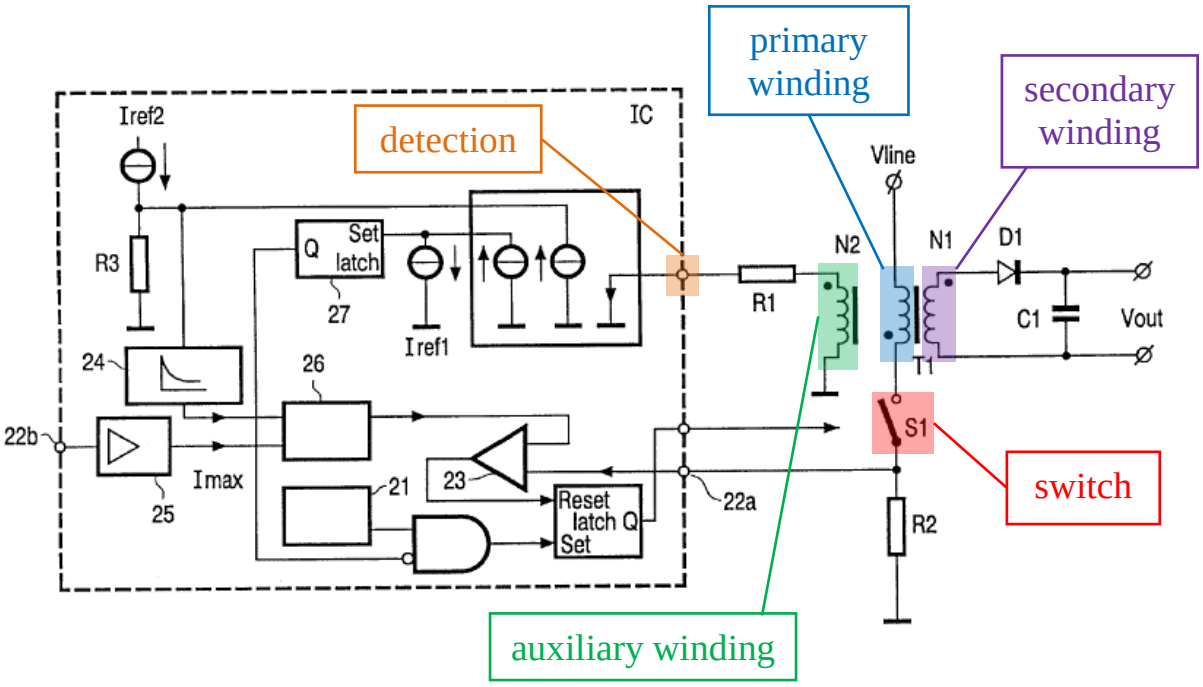
[4] *See also* Ex. 1008, 7:45-64 (explaining temporary overshoot of Va before settling to value representing output voltage).

Like Figure 4 of the '483 Patent, Figure 3 of Pansier illustrates the reflection at the auxiliary winding of both the output voltage (Vout) and input line voltage (Vi) at different times of the switching cycle:



Id., Fig. 3 (annotations added); Ex. 1002, ¶¶ 51-52.

Another example is U.S. Patent 6,542,386 ("Mobers"), which issued on April 1, 2003. Ex. 1004. Like Pansier, Mobers discloses a switching power converter with an auxiliary winding:



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 53. Mobers explains that by monitoring the auxiliary winding in a time-phased way, "not only V_{out} can be monitored …, but also V_{line} can be monitored." Ex. 1004, 5:5-10. Specifically, "information relating to the output voltage V_{out} will be present" on the auxiliary winding during the off-time of the switch, whereas "information relating to V_{line} will be present" on the auxiliary winding during the on-time of the switch. *Id.*, 5:50-53.

D. Examination History

During prosecution of the '483 Patent, Patent Owner distinguished the purported invention by arguing that the prior art "fails to disclose '*a sensor coupled to receive a signal from* ***a single terminal*** *of the controller' where the*

signal represents both ***a line input voltage*** during the on time and ***an output voltage*** during the off time of a power converter." Ex. 1010, 31 (bold and italics emphases in original). For example, Patent Owner argued that the Yamada and Uruno references received the line input voltage information and the output voltage information from separate terminals, not a single terminal. *Id.*, 30-31. Patent Owner also distinguished the Balakrishnan '161 reference because a diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on-time. *Id.*, 13.

Thus, Patent Owner emphasized that the distinguishing feature of the '483 Patent was the single terminal coupled to receive a signal representative of both the input and output voltage. But as described above, an auxiliary winding of a flyback switching power converter naturally reflects both the input and output voltage at different times during the switching cycle due to the physical properties of the transformer. *See, e.g.*, Ex. 1008, 7:31-43, Fig. 3; Ex. 1004, 5:11-14, 5:50-53. Thus, in the absence of a diode that blocks either the positive swing (representing the output voltage) or the negative swing (representing the input line voltage) of the signal from the auxiliary winding, a signal received from an auxiliary winding via a single terminal of the controller will represent both the input and the output voltage. Ex. 1002, ¶¶ 54-55.

IV. SUMMARY OF PRIOR ART

A. Spampinato

U.S. Patent 6,061,257 to Spampinato et al. ("Spampinato") issued on May 9, 2000. Ex. 1015. Spampinato is therefore prior art to the '483 Patent under at least 35 U.S.C. § 102(b). Spampinato was not considered by the Patent Office during examination of the '483 Patent. Ex. 1001, 1-2 (References Cited).

Spampinato discloses a flyback converter with an auxiliary winding:

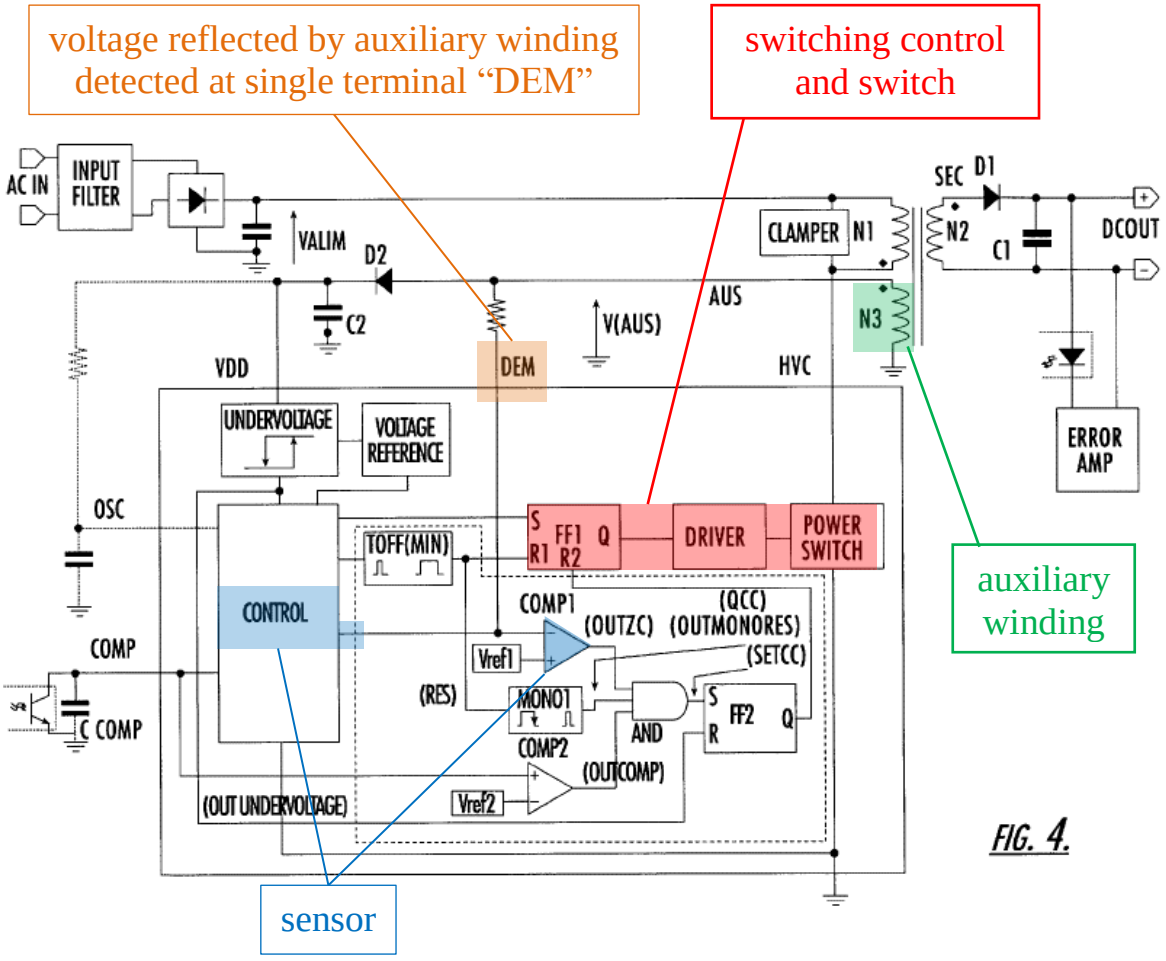


FIG. 4.

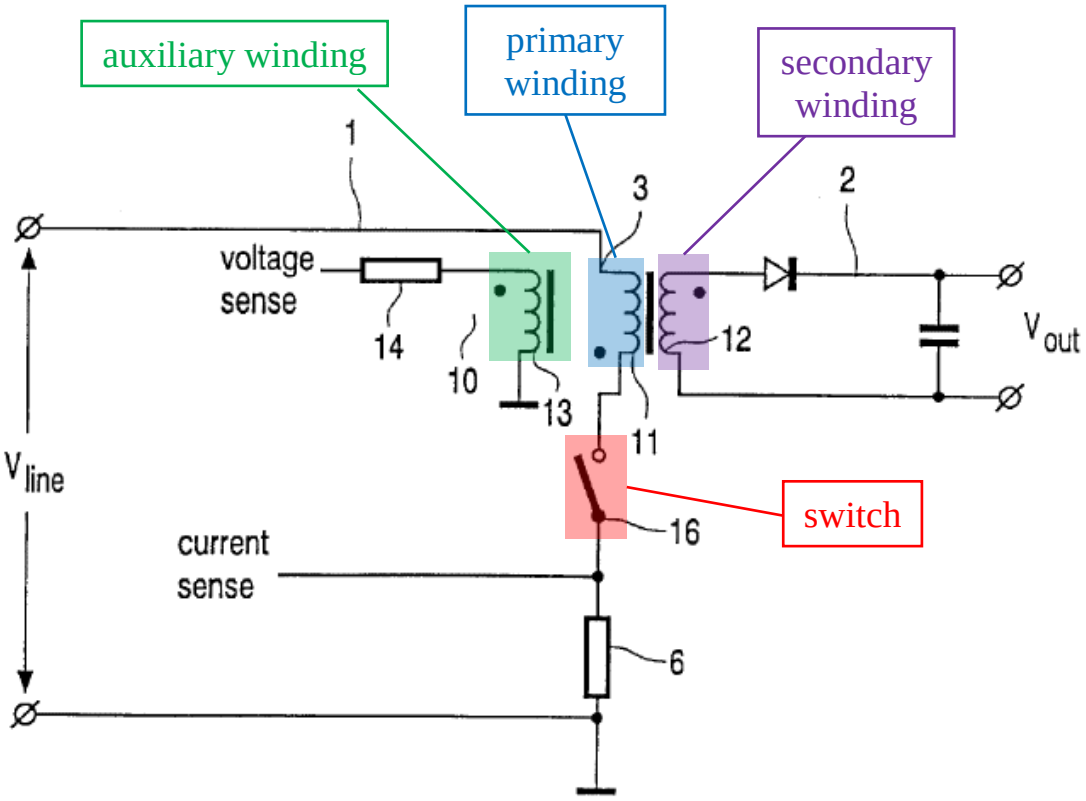
Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶¶ 56-57. Spampinato uses the

reflection of the output voltage on the auxiliary winding during the off-time of the power switch to detect an output short circuit condition. *See* Ex. 1015, 3:21-29, 5:47-57. When such a fault is detected, switching is disabled to prevent damage to the power supply that would otherwise result from the short circuit condition. *Id.*, 5:47-57; Ex 1002, ¶ 57.

B. Mobers

U.S. Patent 6,542,386 to Mobers et al. ("Mobers") was filed on October 12, 2001 and issued on April 1, 2003. Ex. 1004. Mobers is therefore prior art to the '483 Patent under at least 35 U.S.C. § 102(b). Mobers was not considered by the Patent Office during examination of the '483 Patent. *See* Ex. 1001, 1-2 (References Cited).

Mobers discloses a flyback converter with an auxiliary winding (referred to as a "control winding" in Mobers). Ex. 1004, 4:1-28, Fig. 6.



Ex. 1004, Fig. 6 (annotations added); Ex. 1002, ¶¶ 58-59.

Mobers recognizes that the auxiliary winding reflects the input line voltage in addition to the output voltage during different points in the switching cycle. Ex. 1004, 5:50-53 ("[T]he information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke.").

Moreover, Mobers teaches that *both* the input line voltage information and the output voltage information can be used to implement various protection schemes. Ex. 1002, ¶¶ 60-65. For example, the output voltage information is used to implement an output over voltage protection. Ex. 1004, 3:62-65 ("[T]he control

winding forms part of an over voltage protection system by monitoring the output voltage V_{out} of the switched-mode power supply."); *see also* Ex. 1002, ¶ 62. In addition, the input line voltage information is used to implement an over power protection system. Ex. 1004, 3:60-62 ("This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}."); *see also* Ex. 1002, ¶¶ 63-65. Mobers explains that an "advantage" of such a scheme is that both V_{out} and V_{line} are detected "via the same existing pin on the integrated circuit." *Id.*, 5:20-25; *see also id.*, 2:56-61, 3:14-20; Ex. 1002, ¶ 66.

V. CLAIM CONSTRUCTION

In the Delaware Litigation, neither Petitioner nor Patent Owner raised a claim construction issue involving the '483 Patent for the District Court to resolve. *See* Ex. 1011. Petitioner maintains that all terms should be given their plain and ordinary meaning. But, Petitioner provides some explanation below regarding the plain and ordinary meaning of the requirement that the "signal" recited in Claim 1 must "represent" the output voltage and the line input voltage. *See* Ex. 1002, ¶ 68.

A. "to represent" (Claim 1)

Claim 1 recites a sensor that is coupled to receive "a signal." Claim 1 then separately recites characteristics of the signal: "the signal from the single terminal to represent a line input voltage of the power converter during at least a portion of an on time of the power switch, the signal from the single terminal to represent an

output voltage of the power converter during at least a portion of an off time of the power switch." Ex. 1001, Claim 1.

Petitioner submits that the language regarding what "the signal" must "represent" requires no construction and should be given its plain and ordinary meaning. Consistent with the plain meaning of the claims, the "to represent" language defines characteristics of the recited "signal." However, the "to represent" phrase does ***not*** limit the operation of the separately recited sensor or any other structure recited in Claim 1. In other words, there is no requirement in the "to represent" phrase that limits whether or how the sensor responds to the information represented by the signal at different times during the switching cycle. Ex. 1002, ¶¶ 69-70.

Where Patent Owner intended to define actions taken by the sensor and/or other recited structures in the claims based on the information represented by the recited "signal," Patent Owner did so expressly. For example, Claim 14 requires the sensor "to *sample* the signal from the terminal" and "to *generate* a sample output voltage signal." Ex. 1001, Claim 14. By contrast, there is no definition in Claim 1 with respect to any action the sensor must take in response to the recited signal that the sensor receives from the single terminal. Ex. 1002, ¶ 71.

Lastly, there was no disclaimer of claim scope during prosecution that would limit whether or how the recited structures in Claim 1 respond to the various

information represented by the recited "signal." During prosecution, Patent Owner distinguished three references on the basis that these references did not disclose a terminal that received a signal that represented both output voltage and the line input voltage of the power converter at the specified different times. In a Response dated February 4, 2011, Patent Owner distinguished U.S. Patent Nos. 6,842,353 (Yamada) and 7,551,462 (Uruno) on the basis that both references receive different signals representing the input and output voltage at different terminals. Ex. 1010, 30-31. In a later Response to Office Action dated May 27, 2011, Patent Owner distinguished U.S. Patent No. 6,233,161 (Balakrishnan) on the basis that the diode in the path of the identified terminal blocked that terminal from receiving a signal representing the line input voltage during the on-time. Ex. 1010, 13; *see also* Ex. 1002, ¶¶ 72-73; Ex. 1014, 18.

Importantly, Patent Owner's arguments during examination relate to what the ***signal*** received from a single terminal ***represents***, not how any of the separately recited structures respond to that signal. Thus, there was no clear and unmistakable disclaimer in the prosecution history that would require the separately recited structures in Claim 1 to respond to the information represented by the recited "signal" in any particular manner.

VI. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: The Combination of Spampinato and Mobers Renders Obvious Claims 6, 8, 9, 12, and 13 Under 35 U.S.C. § 103

The combination of Spampinato and Mobers discloses and suggests to a person of ordinary skill in the art (POSITA) each element of Claims 6, 8, 9, 12, and 13, and thus renders those claims obvious under 35 U.S.C. § 103. Ex. 1002, ¶ 74.

1. A POSITA Would Have Been Motivated to Combine Spampinato and Mobers

Spampinato discloses a flyback-type power converter with an auxiliary winding. *See* Ex. 1015, 4:26-31, Fig. 4. The auxiliary winding is used to monitor the output voltage during the off-time of the power switch and to thereby detect output short circuit conditions. *Id.*, 4:30-39.

Mobers also discloses a flyback-type power converter that utilizes a transformer with an auxiliary winding. Ex. 1004, Fig. 7. Like Spampinato, Mobers uses the auxiliary winding to monitor the output voltage during the off-time of the power switch. *Id.*, 3:60-62. Mobers recognizes that the auxiliary winding can ***also*** be used to monitor the input voltage during the on-time of the power switch. *Id.*, 3:60-67, 5:50-55. Mobers uses this input line voltage information to implement "an over power protection circuit for switched-mode power supplies." *Id.*, 2:51-53. The over power protection circuit monitors the

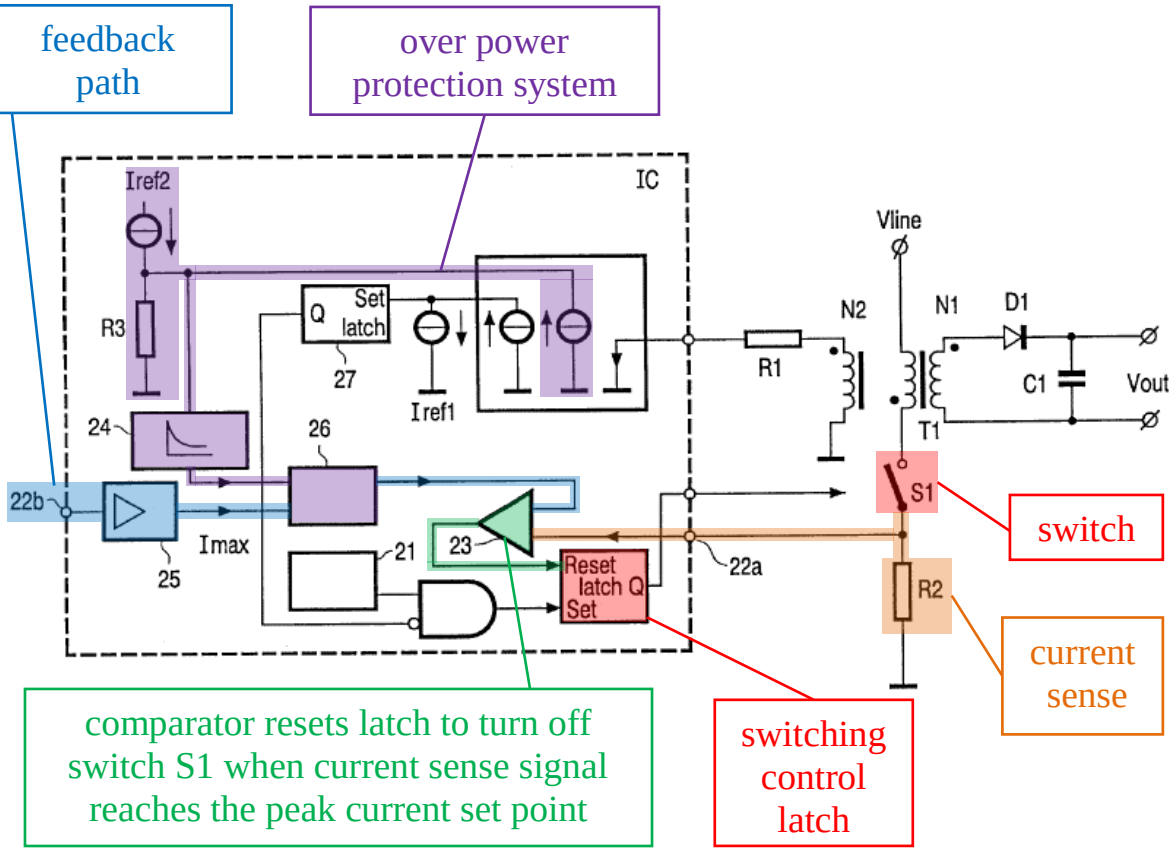
input line voltage (*id.*, 3:60-62) and ensures that the power provided to the transformer does not reach damaging levels (*id.*, 2:8-22).

A POSITA would have found it obvious to combine Mobers's teaching of an over power protection system with Spampinato. Ex. 1002, ¶¶ 75-77. Such a combination represents the use of a known technique (e.g., the over power protection system from Mobers) to improve a similar device (e.g., the switch mode power supply in Spampinato) in the same way. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S.Ct. 1727, 1740 (2007); Ex. 1002, ¶ 77.

Spampinato and Mobers describe similar architectures with respect to the baseline control circuitry that works in conjunction with the over power protection system taught by Mobers. *See* Ex. 1002, ¶ 78. For example, Spampinato discloses "a current mode type control" whereby the current through the power switch is limited on a "pulse by pulse basis" based on a feedback signal that is indicative of the output voltage.[5] Ex. 1015, 4:49-60; *see also* Ex. 1002, ¶ 78; Ex. 1013, 16-17.

[5] Although Figure 4 of Spampinato does not illustrate a particular way in which current through the switch is measured, a POSITA would recognize that the current could be measured in any of the many known ways (e.g., measuring voltage across a sense resistor in series with the power switch). Ex. 1002, ¶ 78. Indeed, the '483 patent concedes that switch current can be measured in any of the "many *known* ways to measure switch current." Ex. 1001, 5:52-56 (emphasis added).

Mobers includes a similar current mode control architecture. Ex. 1002, ¶ 79. Mobers includes a switching control latch that is reset by comparator 23 to turn the switch off during each switching cycle when the current sense signal reaches the peak current setpoint. Ex. 1004, Fig. 7, 5:27-29 ("The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off.").



Ex. 1004, Fig. 7 (annotations added).

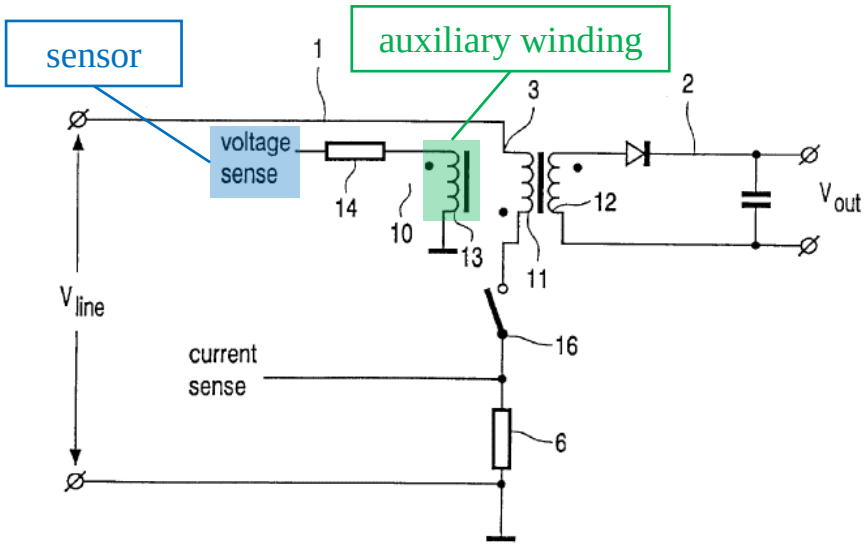
Mobers also teaches that the overpower protection system may intervene by adjusting the peak current setpoint if the input line voltage is high. Ex. 1004, 5:34-37 ("Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used."). The V_{line} information detected from the auxiliary winding is processed by curve circuit 24. *Id.*, 5:37-45. As depicted by the symbol for curve circuit 24 in Figure 7, the output of curve circuit 24 decreases with higher line voltages. *See id.*, Fig. 4; Ex. 1002, ¶ 80. If the output of curve circuit 24 is lower than the signal from error amplifier 25, minimum circuit 26 uses the output of curve circuit 24 to set the peak current set point. Ex. 1004, 5:46-50. Thus, the maximum amount of power passed through the transformer may be controlled by reducing the peak current through the switch during each cycle as a function of the input line voltage. Ex. 1002, ¶ 80.

Given the similar current-mode control disclosed in Spampinato and Mobers, a POSITA would be both motivated and able to implement the overpower protection system with Spampinato in the same manner as it is disclosed in Mobers. Ex. 1002, ¶ 82. In such a combination, the overpower protection system would be incorporated in Spampinato to reduce the peak switch current on a pulse-by-pulse basis during high input line voltage conditions to achieve the same benefit touted by Mobers. Ex. 1002, ¶ 82. Because the over power protection system

would be used in Spampinato in the same manner it is used in Mobers, a POSITA would correctly expect the over power protection system to operate in the same predictable manner as disclosed in Mobers. *Id.*

As explained in detail below, the way that Mobers senses the input line voltage via the auxiliary winding during the on-time of the switch is compatible with the way that Spampinato senses the output voltage from the auxiliary winding during the off-time of the switch. Ex. 1002, ¶¶ 83-88.

Like the resistor coupled between the auxiliary winding and the DEM pin in Spampinato (*see* Ex. 1015, Fig. 4), Figure 6 of Mobers illustrates resistor 14 coupled between the control winding 13 (i.e., the auxiliary winding) and the sensor:



Ex. 1004, Fig. 6 (annotations added). Mobers discloses that the voltage on the left side of resistor 14 in Figure 6 can be clamped to fixed potential. Ex. 1004, 4:29-

36. Thus, when a voltage is generated by the auxiliary winding on the other side of resistor 14, the voltage potential across the resistor induces a current to flow that represents the voltage reflected by the auxiliary winding. *Id.* In this way, the voltage reflected by the auxiliary winding (e.g., the input line voltage during the on-time of the switch) may be sensed in the form of a current signal. Specifically, a negative current (i.e., a current flowing toward the auxiliary winding) representative of the input line voltage is generated during the on-time of the switch. *Id.*, 4:54-65, 5:14-19.

However, as explained in detail below, the voltage clamp attributable to the over power protection system in Mobers only clamps the voltage at the single terminal of the controller when the voltage at the auxiliary winding swings negative during the on-time of the switch. Ex. 1002, ¶ 85. Thus, the voltage clamp in the over power protection circuitry taught by Mobers would not interfere with Spampinato's ability to sense a positive voltage, at the single terminal of the controller, that is induced by the auxiliary winding during the off-time of the switch.

The circuitry in Figure 8 of Mobers shows that separate sensor circuitry is used in Mobers for the over power protection circuitry (which senses the negative swing of the auxiliary winding representing the input line voltage) and the over voltage protection circuitry (which senses the positive swing of the auxiliary

winding representing the output voltage). Ex. 1004, Fig. 8; Ex. 1002, ¶ 86

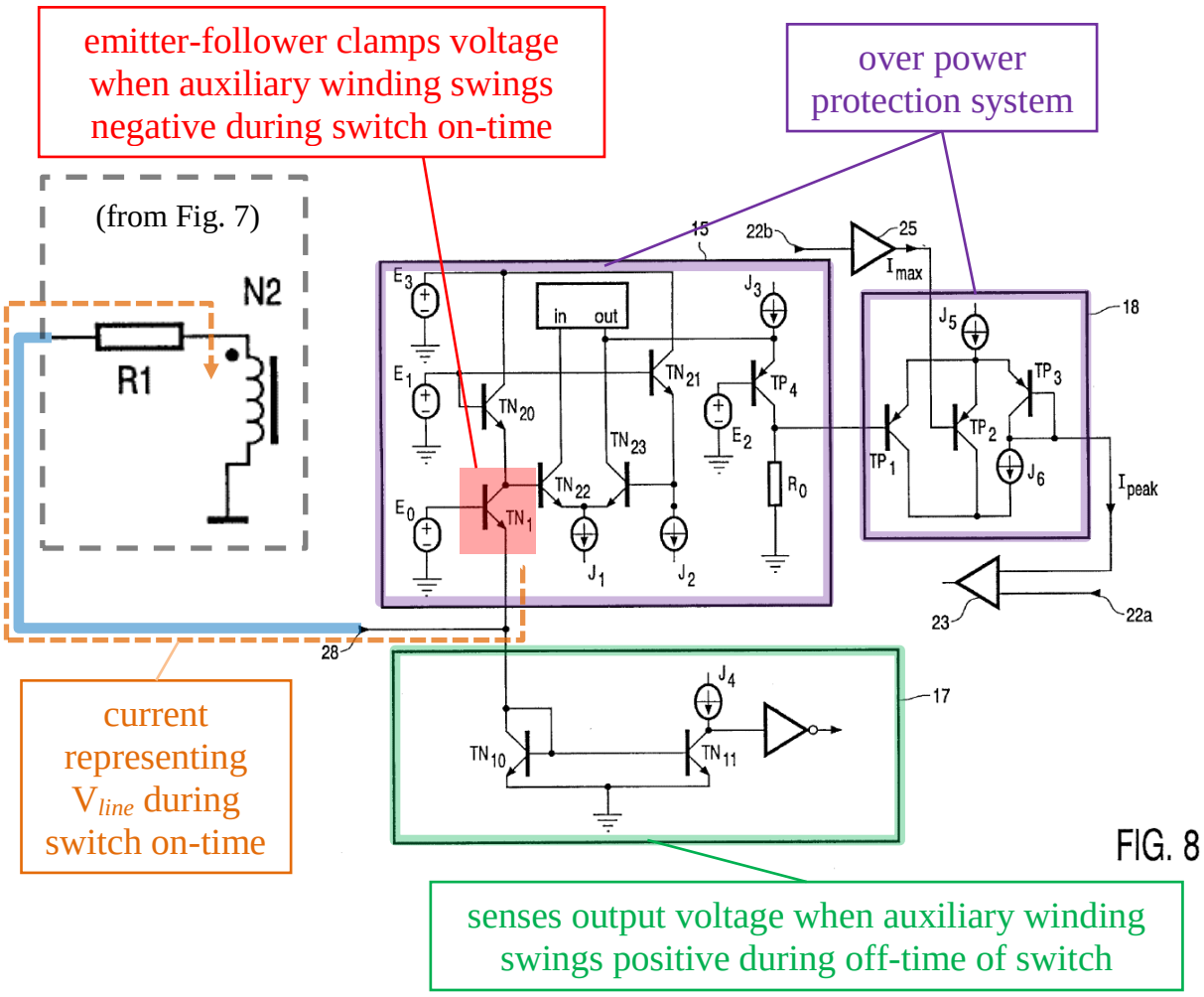


FIG. 8

Ex. 1004, Fig. 8 (annotations added with the auxiliary winding N2 and resistor R1 from Fig. 7 coupled via gray line to terminal 28 of Figure 8); Ex. 1002, ¶ 86. As explained in Mobers, terminal 28 is coupled to the auxiliary winding via resistor R1. Ex. 1004, 5:67-6:1 ("Terminal 28 is to be connected to the left leg of resistor R1 in FIG. 7."). Blocks 15 and 18 in Figure 8 correspond to the over power protection circuit, while block 17 corresponds to the over voltage protection circuitry. *Id.*, 5:64-66.

As shown in Figure 8, the over power protection circuit includes transistor TN_1 coupled to terminal 28. *Id.*, Fig. 8, 5:67-6:1. Transistor TN_1 is configured in what is known as an emitter-follower configuration. Ex. 1002, ¶ 87. When the voltage on the auxiliary winding swings negative to reflect the input line voltage during the on-time of the power switch, transistor TN_1 clamps terminal 28 to a voltage that equals the voltage reference E_0 minus the base-to-emitter threshold of TN_1. *Id.* Thus, a current representative of the input line voltage will flow from the emitter of transistor TN_1 and through resistor R1 to the auxiliary winding. *Id.* However, when the voltage on the auxiliary winding swings high to reflect the output voltage during the off-time of the power switch, transistor TN_1 simply turns off and does not affect the voltage or current otherwise present at terminal 28. *Id.*

Notably, transistor TN_1 in Figure 8 of Mobers is configured in a similar manner as transistor 334 inside sensor 202 in Figure 3 of the '483 Patent. *Compare* Ex. 1004, Fig. 8; *and* Ex. 1001, 7:24-37, Fig. 3; *see also* Ex. 1002, ¶ 88. Thus, like transistor 334 in Figure 3 of the '483 Patent, transistor TN_1 in Figure 8 of Mobers clamps the voltage at the single terminal when the auxiliary winding voltage goes negative, and thereby receives a current signal representative of the line input voltage during the on-time of the switch. *See* Ex. 1001, 7:24-37. And like transistor 334 in Figure 3 of the '483 Patent, transistor TN_1 in Figure 8 turns off and does not interfere with other portions of the sensor when the auxiliary

winding voltage swings positive during the off-time of the switch. Ex. 1002, ¶ 88. Therefore, when combining Spampinato with the over power protection system taught by Mobers, the additional circuitry from Mobers does not affect the ability of Spampinato to detect positive voltages from the auxiliary winding during other portions of the switching cycle.[6] Ex. 1002, ¶ 89.

In sum, a POSITA would have been motivated to combine Spampinato with the over power protection system taught by Mobers in order to provide Spampinato with the same protection. Ex. 1002, ¶ 90. Because Spampinato and Mobers both disclose current-mode control, such a combination represents the use of a known technique (e.g., the over power protection system in Mobers) to improve a similar device (e.g., the switch mode power supply in Spampinato) in the same way. *KSR Int'l Co.*, 127 S.Ct. at 1740. Moreover, the way that Mobers's over-power-protection scheme senses a current from the auxiliary winding representative of the input line voltage during the on-time of the switch is compatible with the way that

[6] Because Spampinato already includes its own scheme for sensing the output voltage reflected by the auxiliary winding during the off-time of the switch, the proposed combination of Spampinato and Mobers does not include block 17 from Figure 8 of Mobers. Thus, the circuitry in Spampinato for detecting positive voltages from the auxiliary winding representative of the output voltage during the off-time of the switch would not be affected by by transistor TN_{10} in block 17 of Mobers. Ex. 1002, ¶ 89, FN11.

Spampinato's short-circuit-protection scheme senses a voltage from the auxiliary winding representative of the output voltage during the off-time of the switch. The proposed combination may therefore be implemented with predictable results. Ex. 1002, ¶ 90.

2. Independent Claim 1

Claim 1 is challenged in a concurrently filed Petition, but *not* herein. But, the disclosure of claim 1 is shown below to support challenge of dependent claims.

Claim 1[pre]: "A controller for a power converter, comprising:"

Spampinato discloses a controller for a flyback-type power converter:

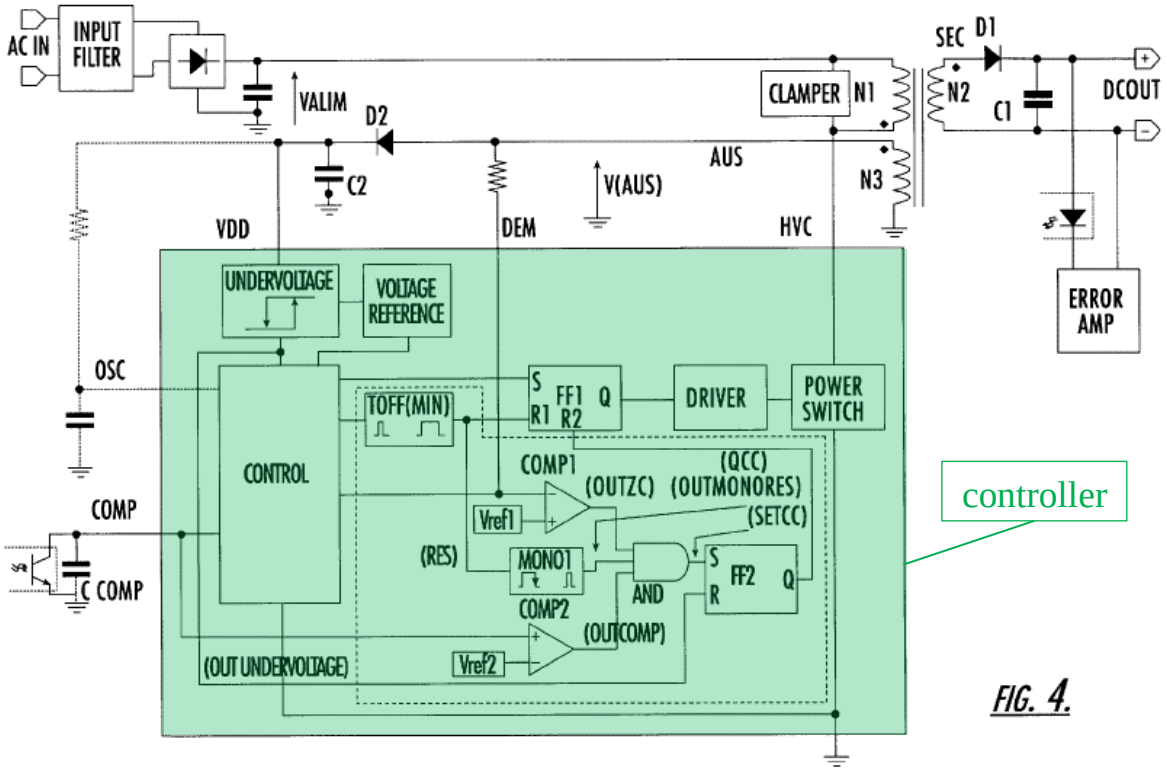


FIG. 4.

Ex. 1015, Absract, Fig. 4; Ex. 1002, ¶ 91.

Mobers similarly discloses a "control circuit" for a switched mode power converter. Ex. 1004, 3:6-11.

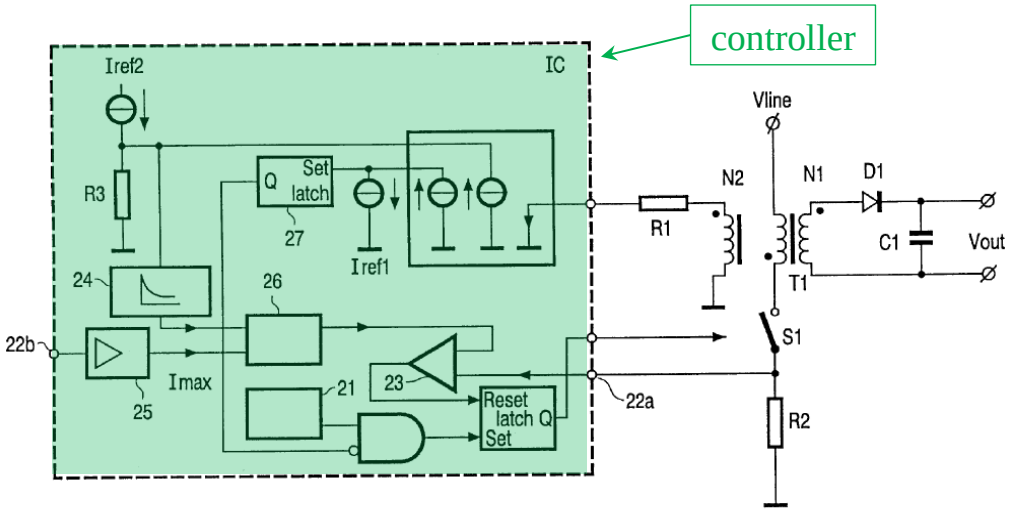


FIG. 7

Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 92.

Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each element of the preamble of Claim 1. Ex. 1002, ¶¶ 91-93.

1[pre]. A controller for a power converter, comprising:	*See* Spampinato and Mobers citations in Section VI.A.1. **Spampinato:** Ex. 1015, 4:49-55: "In a current mode type of control, as in implemented by the basic control circuit of the converter, there is a relationship between the error voltage VCOMP provided by photocoupling the output of the error amplifier of the output voltage ERROR AMP to the CONTROL circuitry through the dedicated pin COMP and the current flowing in the power switch POWER." (emphasis added). Ex. 1015, Abstract: "The voltage induced from the current flowing in a secondary winding of a transformer on the auxiliary winding

	is rectified and filtered to power, during a steady state of operation, the control circuitry of the converter." *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 4:6-26, 4:49-60, 5:14-28, Claims 6-7, Fig. 4. **Mobers:** Ex. 1004, 3:6-9: "The switched-mode power supply according to the first aspect of the present invention may further comprise a control circuit for controlling the controllable current switching means." *See also* Ex. 1004, 3:9-12, 5:20-25, 5:26-62, 5:63-6:3; Figs. 6-8, Claims 1, 3, 5, 6.

Claim 1[a]: "a switching control that switches a power switch to regulate an output of the power converter; and;"

Spampinato's controller includes a flip flop FF1 and a driver, which collectively form a switching control coupled to switch the power switch to regulate the output of the power converter:

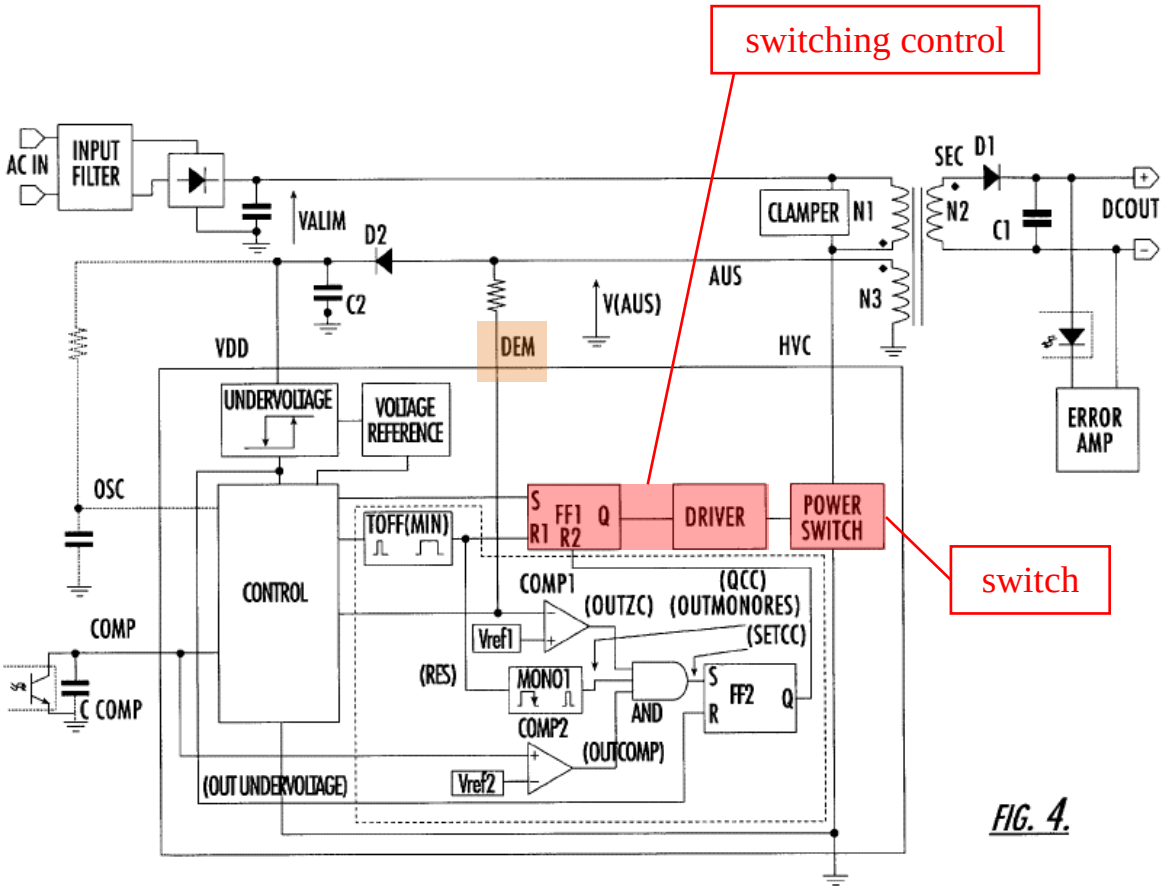
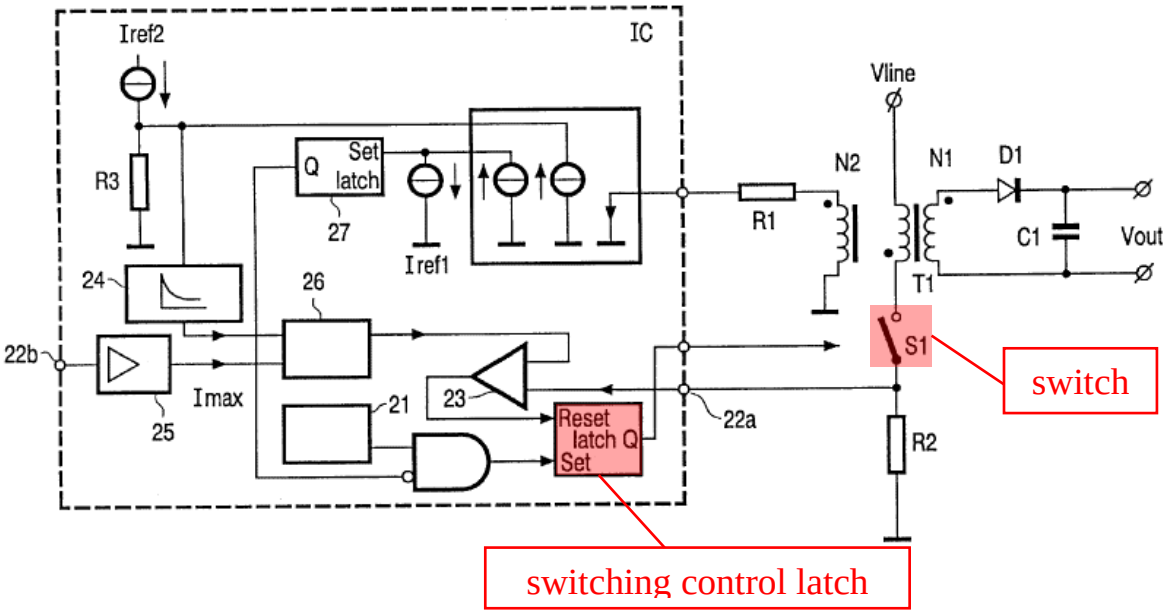


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 94. Under normal conditions, the power switch is turned on and off to regulate the "power that may be transferred" from the input to the output of the power converter. *See* Ex. 1015, 4:49-60. And when a short circuit is detected, the switching control latches the power switch off. *Id.*, 5:47-57.

Similar to Spampinato, Mobers discloses a latch (i.e., a switching control) that controls switch S1 (i.e., a power switch) to regulate V_{out} (i.e., an output of the power converter). As described by Mobers, V_{out} is controlled by regulating the conduction time of the switch, and thereby the amount of energy that is transferred

from the primary side to the secondary side of the converter. Ex. 1004, 4:37-51; *see also id.*, 1:36-54, 5:26-33.



Id., Fig. 7 (annotations added); Ex. 1002, ¶ 95.

Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of claim element 1[a]. Ex. 1002, ¶¶ 94-96.

[1a] a switching control that switches a power switch to regulate an output of the power converter; and	*See* Spampinato and Mobers citations in Section VI.A.1. **Spampinato:** Ex. 1015, 4:49-60: "In a current mode type of control, as in implemented by the basic control circuit of the converter, there is a relationship between the error voltage VCOMP provided by photocoupling the output of the error amplifier of the output voltage ERROR AMP to the CONTROL circuitry through the dedicated pin COMP and the current flowing in the power switch POWER. Therefore, there exists a maximum error voltage value $VCOMP_{max}$ error, tied to the maximum current that may flow through the power transistor, that limits the current on a pulse by pulse basis, therefore limiting the maximum power that may be

	transferred from the primary circuit to the secondary circuit." (emphasis added). Ex. 1015, 2:11-14: "In the control circuits of SOPS converters there is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) under demagnetization conditions of the transformer." (emphasis added). Ex. 1015, 5:54-57: "the setting of the flip-flop FF2 and thereby a stable condition of a high logic value of the flip-flop FF2, a condition that keeps the POWER switch turned off by keeping the driving flip-flop FF1 in a reset state." *See also* Ex. 1015, Abstract, 1:20-30, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-42, 4:49-60, 5:29-57, Claims 6-7, Figs. 1, 3, 4, 6B. **Mobers:** Ex. 1004, 4:37-51: "The output voltage of the switched power supply, V_{out}, is controlled by controlling the current in the primary circuit I_p. I_p is controlled by operating switch 16 in a time phased way using a driving circuit (not shown [in Fig. 6])." Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22 a. As soon as the comparator 23 trips, S1 is switched off." Ex. 1004, 5:46-50: "The information from the over power protection circuit can reduce the peak current if the output signal is lower than the signal from the error amplifier 25 on pin 22b. The magnitude of both signals is sensed by the minimum (min.) circuit 26." *See also* Ex. 1004, Abstract, Figs. 1-4 and 6-8, 1:36-65, 3:6-32, 4:37-51, 5:5-10, 5:34-62, Claims 1, 3, 8-11.

Claim 1[b]: "a sensor coupled to receive a signal from a single terminal of the controller,"

Spampinato's controller circuit includes comparator COMP1 (i.e., a sensor) that is coupled to receive a signal from the DEM pin of the integrated controller (i.e., a single terminal of the controller):

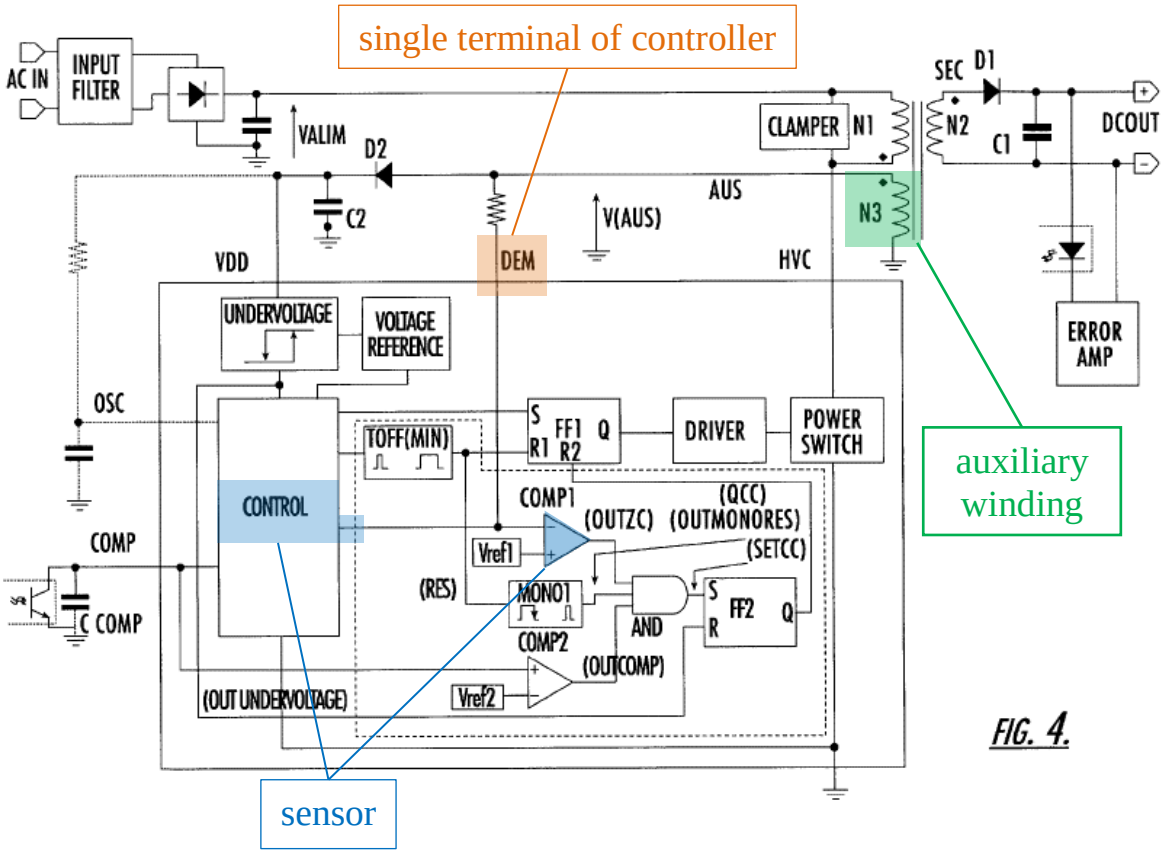


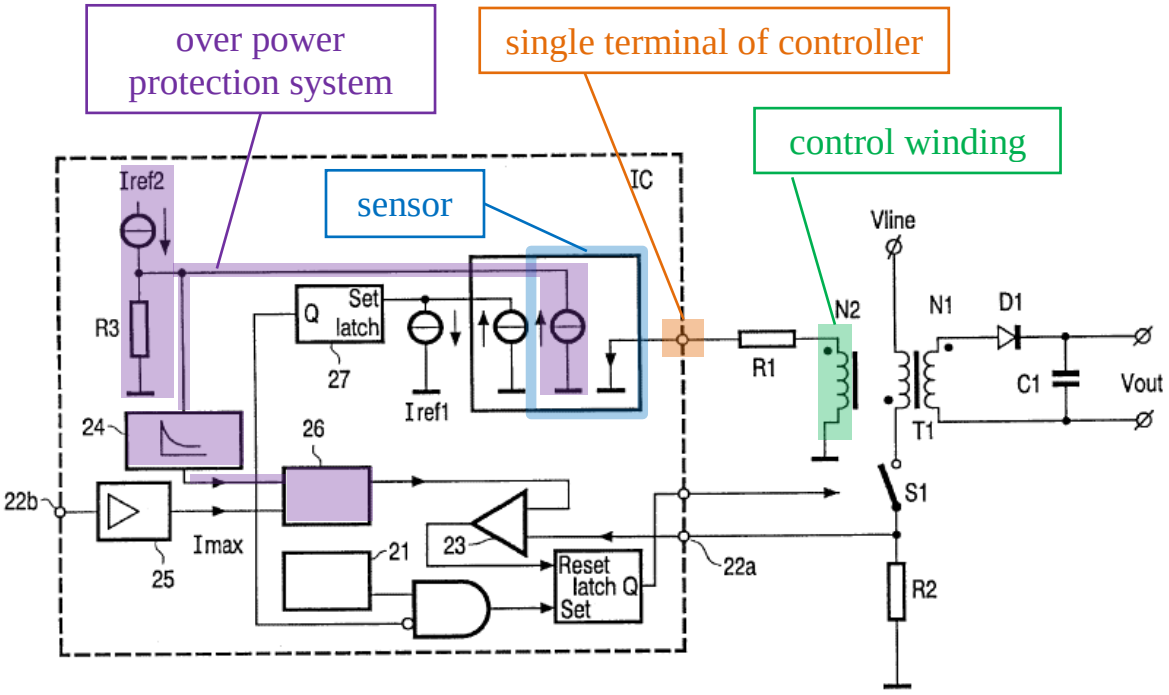
FIG. 4.

Ex. 1015, Fig. 4; Ex. 1002, ¶ 97. Spampinato explains that the comparator COMP1 (i.e., the sensor) monitors the voltage reflected by the auxiliary winding to implement an output short circuit protection scheme. *See, e.g.*, Ex. 1015, 4:31-36. The signal from the DEM pin is also routed to the "CONTROL" block. *Id.*, Fig. 4.

The "CONTROL" block uses the signal from the DEM pin "for synchronizing the turning on of the power transistor." *Id.*, 2:11-14. Thus, the "CONTROL" block is also part of the sensor in Spampinato. Ex. 1002, ¶ 97.

As described in Section VI.A.1, a POSITA would have been motivated to combine Spampinato with the over power protection system taught in Mobers. Therefore, the sensor in the proposed combination includes the portion of the sensing circuitry in Mobers attributable to the over power protection system.

Like Spampinato, the sensing circuitry in Mobers is coupled to receive a signal from the auxiliary winding via a single terminal of the controller.

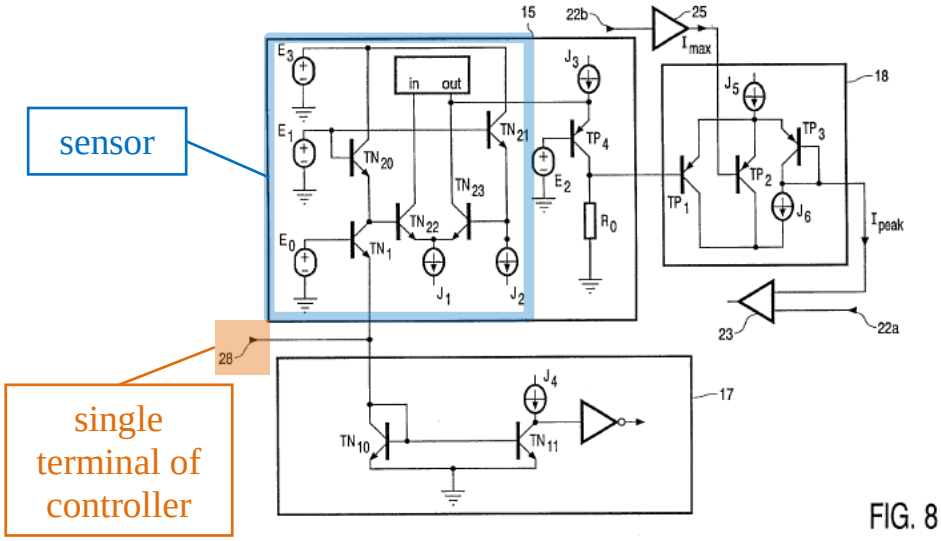


Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 99. Mobers recognizes that, in addition to sensing the output voltage via the auxiliary winding, the input line

voltage may be sensed to implement the over power protection system. Ex. 1004, 3:58-67. And because "a plurality of information is provided via the same control signal the control circuit may receive that information via a *single input pin*." *Id.*, 3:18-20 (emphasis added).

Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of claim element 1[b]. Ex. 1002, ¶¶ 97-100.

[1b] a sensor coupled to receive a signal from a single terminal of the controller,	*See* Spampinato and Mobers citations in Section VI.A.1. **Spampinato:** Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." Ex. 1015, 6:21-27: "The protection of the integrated device from a short circuit does not require the use of any additional external component or of any pin in the case of SOPS or fixed frequency converters which already implement a sensing of the voltage VAUS through a dedicated pin DEM … ." Ex. 1015, 2:11-14: "In the control circuits of SOPS converters there is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) under demagnetization conditions of the transformer." *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-39, 4:49-60, Claims 6-7, Figs. 1, 3, 4, 6B. **Mobers:** Ex. 1004, 5:50-55: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke. Therefore, the very same pin on the IC can be used for obtaining

	both types of information." (emphasis added). Ex. 1004, 3:18-20: "Since a plurality of information is provided via the same control signal the control circuit may receive that information via a single input pin." (emphasis added). Ex. 1004, Fig. 8:  FIG. 8 *See also* Ex. 1004, Abstract, 1:5-13, 2:56-61, 3:1-8, 3:11-17, 4:29-36, 5:6-19, 5:20-25, 5:63-6:3, Claims 1, 3-6, 10, Figures 6-7.

Claim 1[c]: "the signal from the single terminal to represent a line input voltage of the power converter during at least a portion of an on time of the power switch, the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch,"

Figure 4 of Spampinato illustrates auxiliary winding N3 magnetically coupled to both primary winding N1 and secondary winding N2.

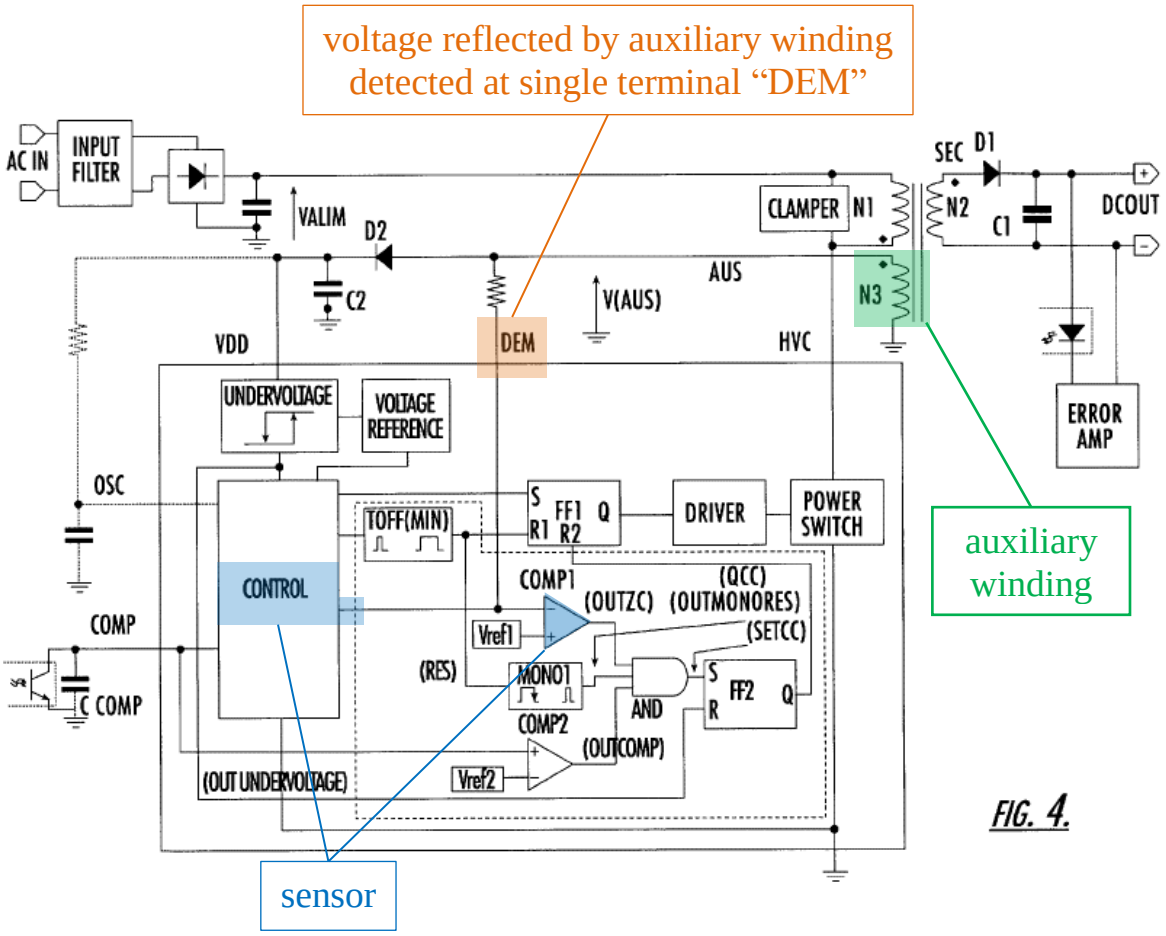
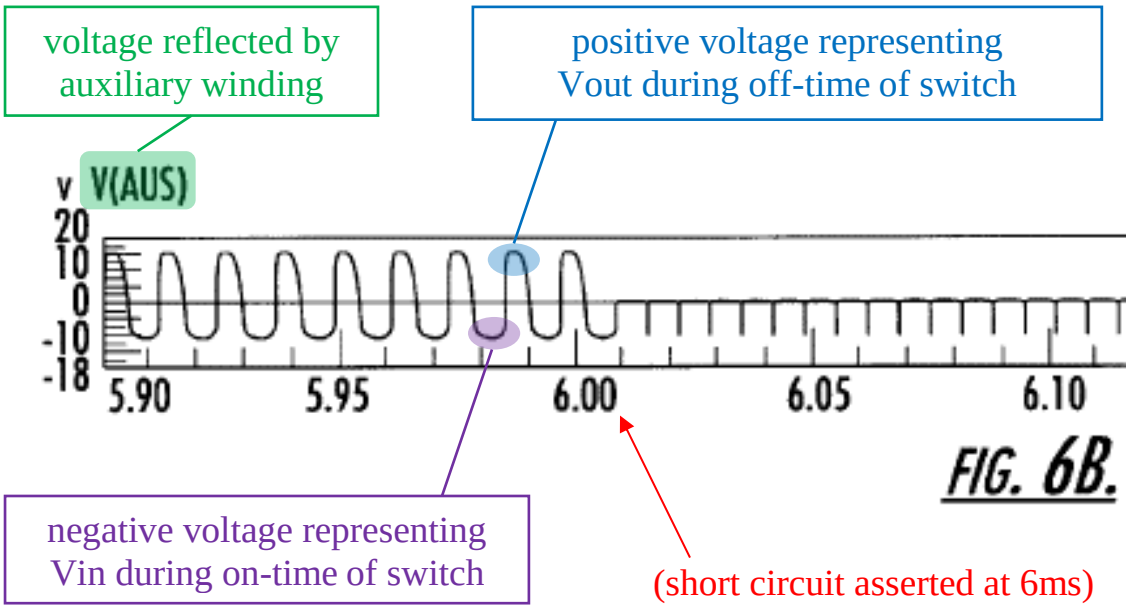


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 101. As described in Section III, a POSITA would understand that the magnetic coupling causes the auxiliary winding to (i) produce a positive voltage representative of the output voltage during at least a portion of the off-time of the switch, and (ii) produce a negative voltage representative of the input line voltage during the on-time of the switch. *See supra* Sections III.A-C; Ex. 1002, ¶ 102.

Consistent with this understanding, Figure 6B illustrates that the signal received from the auxiliary winding via the DEM pin includes both a positive

voltage (representative of the output voltage during the off-time of the switch) and a negative voltage (representative of the input line voltage during the on-time of the switch):

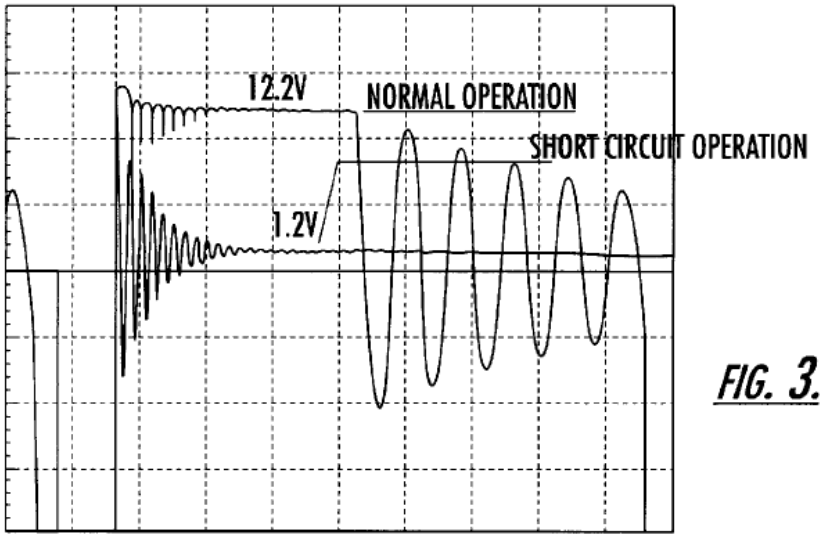


Ex. 1015, Fig. 6B (annotations added); *see also id.*, 6:7-18; Ex. 1002, ¶ 103.

In addition to the disclosure of Figure 6B, Spampinato describes receiving the signal from the auxiliary winding via the DEM pin to sense the output voltage during the off-time of the power switch. *See* Ex. 1015, 2:32-45, 4:31-36. Using a similar architecture, Mobers teaches that the signal received from an auxiliary winding can ***also*** be used to sense the input line voltage during the on-time of the switch. *See e.g.*, Ex. 1004, 5:5-10. Thus, Spampinato and Mobers together recognize that the ***signal*** from the same single terminal (i.e., the terminal coupled to the auxiliary winding of a flyback-type power converter) ***represents*** both the

line input voltage during the on-time of the switch and the output voltage during the off-time of the switch. Ex. 1002, ¶ 104.

Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of claim element 1[c]. Ex. 1002, ¶¶ 101-105.

[1c] the signal from the single terminal to represent a line input voltage of the power converter during at least a portion of an on time of the power switch, the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch,	*See* Spampinato and Mobers citations in Section VI.A.1. **Spampinato:** Ex. 1015, 2:40-45: "The voltage mirrored on the auxiliary winding AUS, coincides with the voltage on the secondary (which during a short circuit, will be equal to the voltage drop Vf on the diode D1), multiplied by their turn ratio (N3:N2), that is: $V_{AUS(cc)} = (N3:N2)\ V_{sec(cc)} = (N3:N2)\ Vf\ (D1)$" Ex. 1015, 4:11-20: "As already mentioned, if the converter output is in a short circuit condition, when the power switch in turned off, the voltage induced on the auxiliary winding of the transformer, apart from the initial oscillatory transient, stabilizes to a V_{AUScc} value which is much lower than the voltage induced during the normal functioning of the converter." Ex. 1015, Fig. 3:  FIG. 3.

	Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." *See also* Ex. 1015, Abstract, 2:11-29, 3:21-35, 4:6-26, 4:26-39, 6:21-27, Claims 6-7, Figs. 1, 3, 4, 6B. **Mobers:** Ex. 5:50-53: "As previously mentioned the information relating to V_{line} will be present on the control winding N2 during the primary stroke, whereas information relating to the output voltage V_{out} will be present during the secondary stroke." Ex. 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored …, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." Ex. 1004, 4:52-5:5: "When a current flows in either of windings 11 or 12, a current will also be induced in regulation circuit 10. The voltage generated across control winding 13 is related to V_{line} or V_{out} according to ratios k and m, respectively. A sensing circuit (not shown) measures the current flowing through resistor 14. Thus, knowing the value of resistor 14, V_{line} and V_{out} can be monitored. If the resistor 14 has resistance R, the current in the regulation circuit 10, I_r, is related to V_{line} during t_{on} in the following way $$I_r = \frac{kV_{line}}{R}, \quad (2)$$ whereas, during t_{off}, the current is related to Vout in the following way $$I_r = \frac{mV_{out}}{R}. \quad (3)$$ "

	See also Ex. 1004, Abstract, 1:5-13, 3:11-17, 3:60-67, 4:29-36, 5:14-19, 5:20-25, 5:56-57, Claims 6, 10, Figs. 6-8.

Claim 1[d]: "wherein the switching control is responsive to the sensor."

Spampinato's controller includes a flip flop FF1 and a driver, which collectively form the switching control:

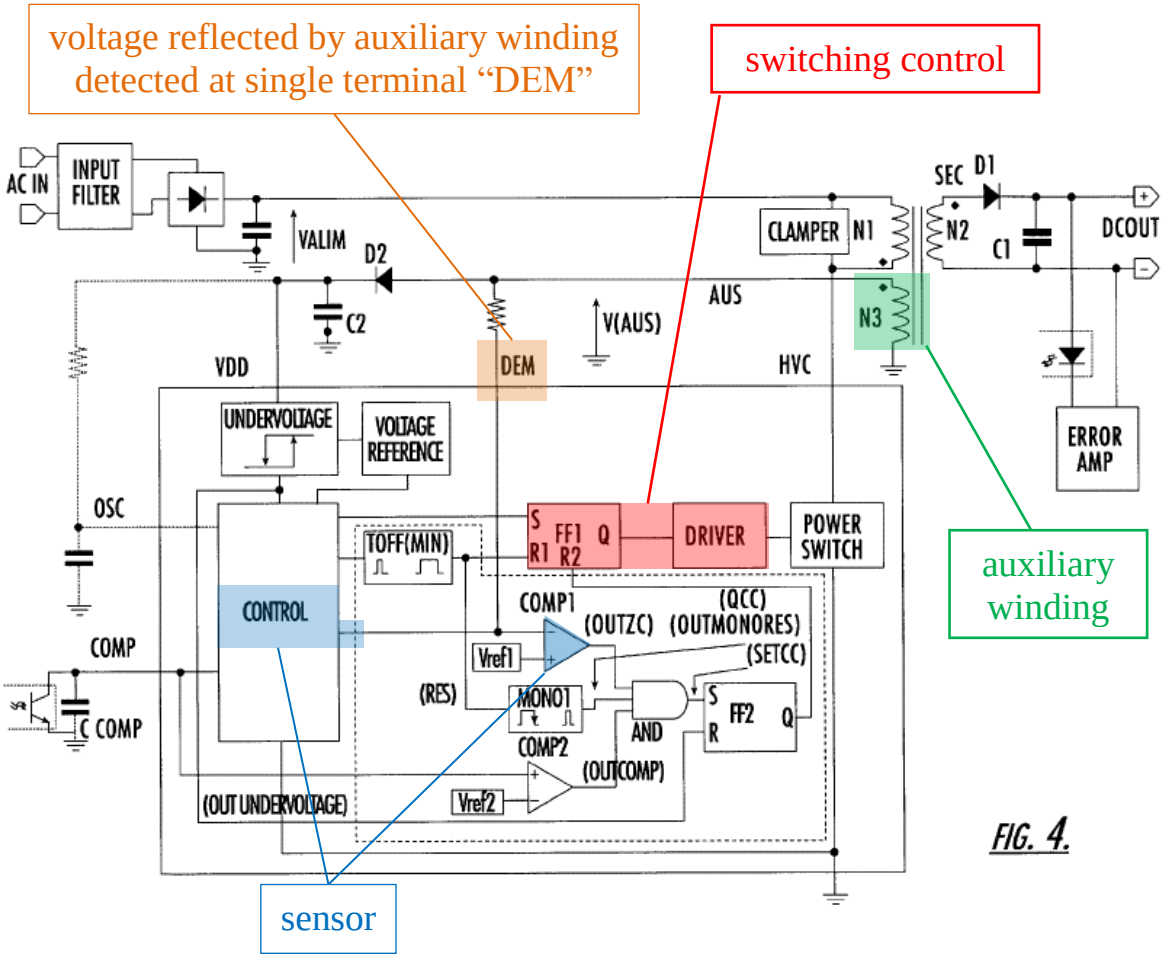


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 106.

The switching control is responsive to the sensor in multiple ways. Ex. 1002, ¶ 107. For example, the signal from the DEM pin is detected by the

"CONTROL" circuit. Ex. 1015, Fig. 4. And as shown in Figure 4, the "CONTROL" circuit is also coupled to set flip-flop FF1 to turn on the power switch. *Id.*; *see also id.* 2:11-13 ("[T]here is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) … .").

The switching control is also responsive to the COMP1 comparator. As shown in Figure 4, comparator COMP1 compares the reflected voltage from the auxiliary winding (representative of the output voltage during the off-time of the switch) against a threshold. Ex. 1015, 4:30-39. The output of COMP1 is provided to an AND gate and then passed flip-flop FF2.[7] *See id.*, Fig. 4. When a short circuit condition is detected, flip-flop FF2 is set, which in turn resets flip-flop FF1 to hold the power switch off. *Id.*

Moreover, as described in Section VI.A.1, the proposed combination implements the over voltage protection system taught by Mobers with the controller disclosed by Spampinato. The over power protection system may set the peak current setpoint of the current sense comparator based on the input line voltage information from the sensor. *See* Ex. 1004, Fig. 7, 5:35-37 ("[T]he over

[7] The other inputs to the AND gate ensure that COMP1 can only pass a short circuit detection signal to flip-flop FF2 during a valid time window (i.e., after start-up has completed and during the off-time of the switching cycle when V_{AUS} represents the output voltage). *Id.*, 5:47-57.

power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used."). During each switching cycle, the current sense comparator resets the latch (i.e., the switching control) to turn off the switch when the current through the switch hits the peak current threshold. *See id.*, Fig. 7, 5:28-33. Thus, in the proposed combination, the switching control would also be responsive to the sensor via the over power protection system taught by Mobers. Ex. 1002, ¶ 109.

The combination of Spampinato and Mobers therefore discloses and suggests to a POSITA each limitation of claim element 1[d]. Ex. 1002, ¶¶ 106-110.

[1d] wherein the switching control is responsive to the sensor.	*See* Spampinato and Mobers citations in Section VI.A.1. *See* Spampinato and Mobers citations for claim elements 1[a]-[b]. **Spampinato:** Ex. 1015, 2:11-14: "In the control circuits of SOPS converters there is also a pin DEM, for synchronizing the turning on of the power transistor (POWER) under demagnetization conditions of the transformer." (emphasis added). Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." (emphasis added). Ex. 1015, 5:47-57: "The logic combination of the signals existing on the outputs of the two comparators COMP1 and COMP2 performed through the AND gate during the interval of time defined by the monostable circuit MONO1, after the

	masking interval defined by the $T_{OFF(min)}$ circuit, ensures that only a short circuit condition of the comparator output produce a simultaneous high state of all the three signals so to cause the setting of the flip-flop FF2 and thereby a stable condition of a high logic value of the flip-flop FF2, a condition that keeps the POWER switch turned off by keeping the driving flip-flop FF1 in a reset state." (emphasis added). *See also* Ex. 1015, Abstract, 1:48-56, 2:11-29, 3:21-35, 4:6-26, 4:26-42, 4:49-60, 5:29-45, Claims 6-7, Figs. 1, 3, 4, 6B. **Mobers:** Ex. 1004, 5:5-10: "Hence by monitoring the voltage in control winding 13 in a time phased way, not only V_{out} can be monitored …, but also V_{line} can be monitored in order to provide over power protection by operating the gate driving circuit in an appropriate way." (emphasis added). Ex. 1004, 5:26-33: "Referring now to FIG. 7, the switch S1 is controlled by a PWM signal from a PWM circuit. The switch is switched on by the set signal from the oscillator 21. The switch is switched off if a certain peak current through S1 is sensed. As previously mentioned, the peak current through S1 is sensed by sensing the voltage generated across R2. This sensed voltage is provided through pin 22a. As soon as the comparator 23 trips, S1 is switched off." Ex. 1004, 5:34-39: "Besides the input signal from 22a, also a signal from the over power protection circuit is used to determine the peak current through S1 and R2. For this purpose the information relating to V_{line} is used. This information is retrieved from the control winding N2 of the transformer. The V_{line} information is processed in the 'curve' circuit 24." *See also* Ex. 1004, 1:5-13, 2:51-55, 3:6-17, 3:60-67, 4:37-44, 5:20-25, 5:39-45, 5:46-55, 5:56-6:3, Figs. 6-8, Claims 1, 3, 5-6, 9-11.

3. Claim 6

Claim 6: "The controller of claim 1, wherein the signal comprises a first signal and a second signal, wherein the first signal is a voltage that is representative of the output voltage of the power converter and wherein the second signal is a current that is representative of the line input voltage of the power converter."

As explained in Section VI.A.1, the proposed combination of Spampinato and Mobers includes Spampinato's controller and the over power protection system taught by Mobers.

Spampinato's controller circuit includes comparator COMP1 that is coupled to receive a signal from the auxiliary winding via the DEM pin. Ex. 1015, Fig. 4. Comparator COMP1 monitors the ***voltage*** reflected by the auxiliary winding that is representative of the output voltage during the off-time of the switch to implement an output short circuit protection. *See, e.g.*, Ex. 1015, 4:31-36 ("By monitoring the voltage V_{AUS} ***voltage*** on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … .") (emphasis added); *see also* Ex. 1002, ¶ 112.

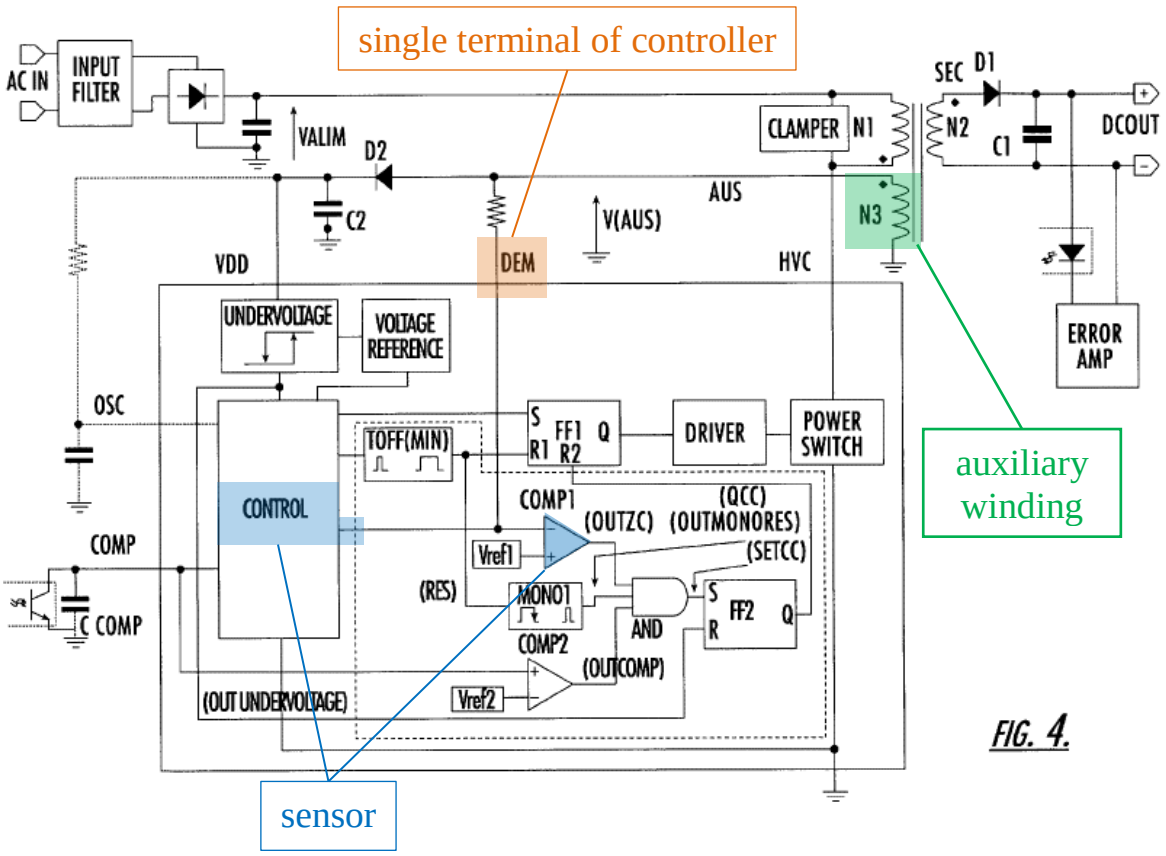


FIG. 4.

Ex. 1015, Fig. 4; Ex. 1002, ¶ 112.

In addition, the over power protection system taught by Mobers senses the negative voltage swing on the auxiliary winding that is representative of the input line voltage during the on-time of the switch. *See e.g.*, Ex. 1004, 3:60-62 ("This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}."); *see also id.*, 3:11-17, 3:62-67, 5:5-10; 5:50-55. And, as described above in Section VI.A.1, the sensor taught by Mobers receives the input line voltage information in the form of a ***current*** signal. Ex. 1002, ¶ 113.

The sensing circuit taught by Mobers clamps the voltage potential at the sensing circuit. Ex. 1004, 4:28-36.[8] When the voltage at the auxiliary winding swings negative, a ***current*** signal that that is representative of the input line voltage flows through the resistor between the auxiliary winding and the sensing circuit. *See supra* Section VI.A.1; Ex. 1004, 4:29-36, 5:52-65; Ex. 1002, ¶ 114. That current signal is described by equation (2) in Mobers:

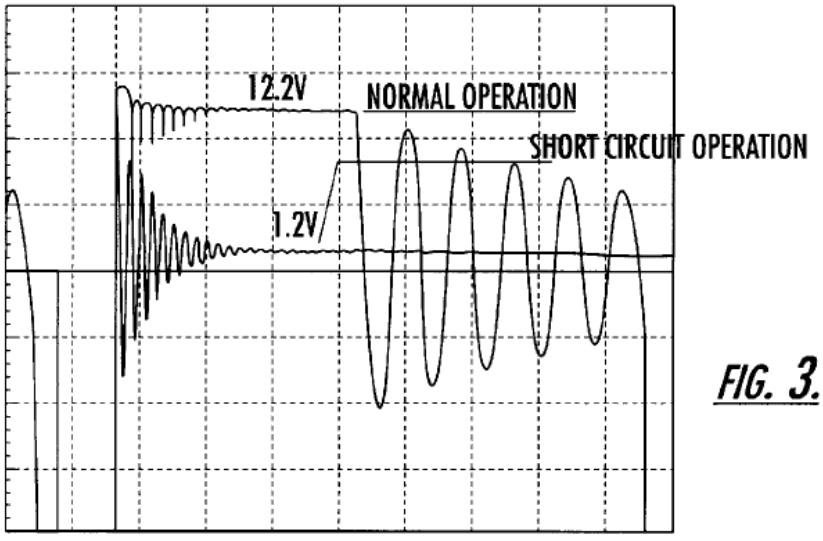
$$I_r = \frac{kV_{line}}{R},$$

where "*k*" is the winding ratio between the primary and control windings and "*R*" is the value of the resistor between the auxiliary winding and the sensing circuit. Ex. 1004, 4:52-64 (describing equation 2); *see also id.*, 4:15-20.

In sum, the sensing circuitry in the proposed combination of Spampinato and Mobers is configured to receive a signal from the auxiliary winding that takes the

[8] As described in Section VI.A.1, the proposed combination incorporates the over power protection taught by Mobers into the controller of Spampinato. The portion of Mobers's sensing circuit associated with the over power protection system clamps the voltage potential at the input of the sensing circuit only during the negative voltage swings on the auxiliary winding. Thus, incorporating this portion of Mobers into Spampinato's controller does not affect the circuitry already present in Spampinato for sensing the positive voltage swings of the auxiliary winding.

form of a voltage representative of the output voltage of the power converter during the off-time of the switch, and takes the form of a current representative of the input line voltage of the power converter during the on-time of the switch. Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of Claim 6. Ex. 1002, ¶¶ 111-115.

6. The controller of claim 1, wherein the signal comprises a first signal and a second signal, wherein the first signal is a voltage that is representative of the output voltage of the power converter and wherein the second signal is a current that is representative of the line input voltage of the power converter.	*See* Spampinato and Mobers citations in Section VI.A.1. *See* Spampinato and Mobers citations for Claim 1. **Spampinato:** Ex. 1015, 4:31-36: "By monitoring the voltage V_{AUS} voltage on the auxiliary winding AUS of the transformer during a turn-off phase of the power switch, through a first comparator COMP1 whose reference threshold is Vref1 higher than V_{AUScc}, it is possible to discriminate a possible short circuit condition from a 'normal' operating condition … ." Ex. 1015, Fig. 3:  FIG. 3. Ex. 1015, 2:40-45: "The voltage mirrored on the auxiliary winding AUS, coincides with the voltage on the secondary (which during a short circuit, will be equal to the voltage drop Vf on the diode D1), multiplied by their turn ratio (N3:N2),

	that is: $V_{AUS(cc)} = (N3:N2)\ V_{sec(cc)} = (N3:N2)\ Vf\ (D1)$" Ex. 1015, 4:11-20: "As already mentioned, if the converter output is in a short circuit condition, when the power switch in turned off, the voltage induced on the auxiliary winding of the transformer, apart from the initial oscillatory transient, stabilizes to a V_{AUScc} value which is much lower than the voltage induced during the normal functioning of the converter." *See also* Ex. 1015, Abstract, 2:11-29, 3:21-35, 4:6-26, 4:26-39, 6:21-27, Claims 6-7, Figs. 1, 3, 4, 6B. **Mobers:** Ex. 1004, 3:60-62: "This control winding forms part of an over power protection system by providing information relating to the line voltage V_{line}." Ex. 1004, 4:29-36: "One end of the control winding 13 is connected to ground whereas the other and of the control winding is connected to resistor 14. By clamping the left side of resistor 14 to a fixed potential a current will flow through resistor 14 when this potential is different from the voltage generated across control winding 13. By measuring the current flowing through resistor 14 the voltage generated across the control winding 13 can be determined." Ex. 1004, 4:53-65: "The voltage generated across control winding 13 is related to V_{line} or V_{out} according to ratios k and m, respectively. A sensing circuit (not shown) measures the current flowing through resistor 14. Thus, knowing the value of resistor 14, V_{line} and V_{out} can be monitored. If the resistor 14 has resistance R, the current in the regulation circuit 10, I_r, is related to V_{line} during t_{on} in the following way $$I_r = \frac{kV_{line}}{R}, \quad (2)$$ " *See also* Ex. 1004, Abstract, 1:5-13, 3:11-17, 3:60-67, 5:5-13, 5:14-19, 5:20-25, 5:50-55, 5:63-6:8, Claims 6, 10, Figs. 6-8.

4. Claim 8 (and intervening Claim 7)

7. The controller of claim 1, wherein the controller is an integrated circuit controller for the power converter.[9]

8. The controller of claim 7, wherein the power switch is integrated into the integrated circuit controller.

The controller disclosed by Spampinato is depicted and described as an "integrated" controller for the power converter. Ex. 1015, 5:14-17 ("In the scheme of FIG. 4 the components and the functional blocks of the protecting circuit of the invention are identified by a dashed line perimeter, within the integrated converter device.").[10] Moreover, Spampinato expressly contemplates "integration of the power transistor" within the integrated circuit controller. *Id.* 5:17-19.

[9] Claim 7 is challenged in a concurrently filed Petition, but not herein. Nonetheless, the disclosure of Claim 7 by Spampinato and Mobers is shown below to facilitate the challenge to dependent Claim 8.

[10] To be clear, the "dashed line perimeter" indicates the short circuit detection circuitry, which is located "*within* the integrated converter device," whose solid-line boundary is annotated in green in Petitioner's reproduction of Figure 4. *See* Ex. 1015, 5:14-17 (emphasis added); Ex. 1002, ¶ 116.

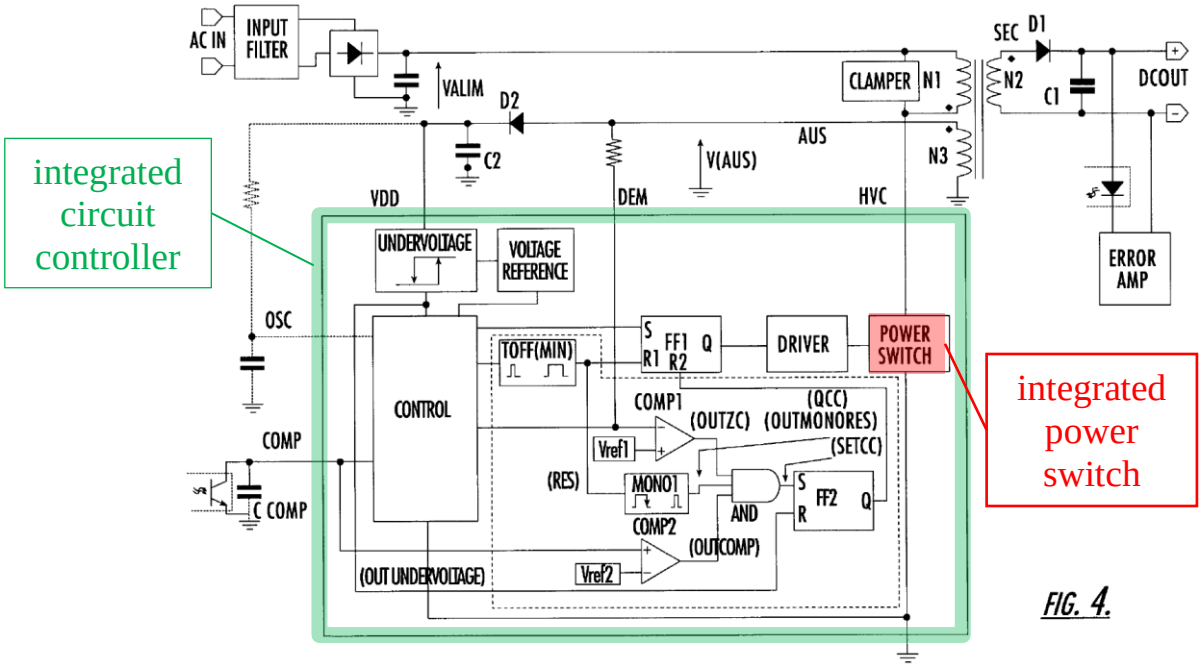
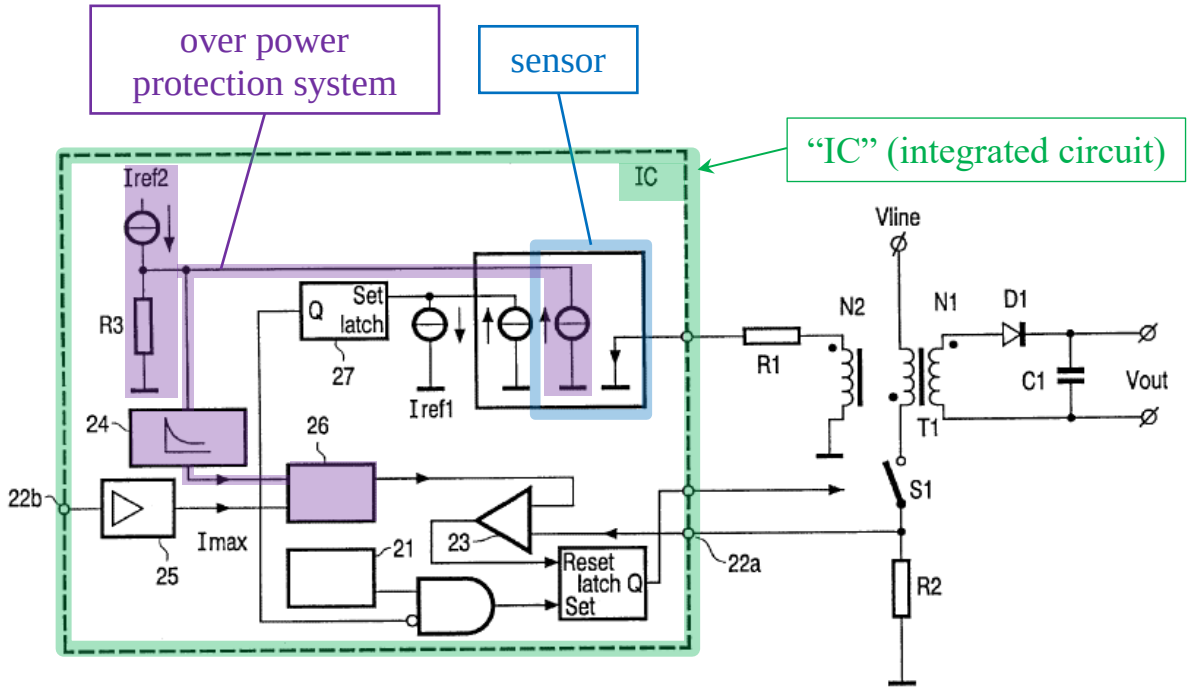


FIG. 4.

Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 116.

Moreover, the portions of Mobers that are incorporated with Spampinato's controller in the proposed combination are also depicted as part of an "IC":



Ex. 1004, Fig. 7 (annotations added); Ex. 1002, ¶ 117.

Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of Claims 7 and 8. Ex. 1002, ¶¶ 116-118.

7. The controller of claim 1, wherein the controller is an integrated circuit controller for the power converter. 8. The controller of claim 7, wherein the power switch is integrated into the integrated circuit controller.	*See* Spampinato and Mobers citations in Section VI.A.1. *See* Spampinato and Mobers citations for Claim 1. **Spampinato:** Ex. 1015, 3:21-24: "An object of this invention is to provide a wholly integrated circuit that implements a protecting function against the effects of a short circuit at the output of a DC-DC flyback converter." (emphasis added). Ex. 1015, 5:14-28: "In the scheme of FIG. 4 the components and the functional blocks of the protecting circuit of the invention are identified by a dashed line perimeter, within the integrated converter device. In the illustrated example, integration of the power transistor that drives the primary winding of the flyback transformer is contemplated, the power transistor being integrated by using a so-called Smart Power technology which permits the realization of integrated power devices capable to withstand voltages that may reach or exceed a thousand Volts. However, it is evident that the protecting circuit of the invention may be integrated even using a low voltage fabrication technology for the device containing the control circuitry in case of converters employing externally connected discrete high voltage POWER switches." (emphasis added). *See also* Ex. 1015, Title, 1:12-18, 1:48-56, 2:53-3:18, 3:42-46, 4:6-42, 4:61-65, 6:19-30, Figs. 1, 4, Claim 11. **Mobers:** Ex. 1004, 2:56-60: "Advantageously, an integrated circuit is provided with an integrated over voltage and over power protection circuit without the use of additional die demanding external components. A consequence of this is the fact that no additional pins on the integrated circuit are required." (emphasis added).

	Ex. 1004, Claim 6: "6. A switched mode power regulator according to claim 1, further comprising an integrated circuit (IC) having a single pin for receiving both information relating to an input voltage to the primary circuit in a first period of time in which energy is stored in the energy storing device (3) and information relating to an output voltage from the secondary circuit in a second period of time in which energy is released from the energy device (3)." (emphasis added). *See also* Ex. 1004, 2:30-48, 4:37-44, 5:20-25, 5:46-62, 5:63-6:3, Figs. 6-8, Claim 1.

5. Claim 9

The combination of Spampinato and Mobers discloses and suggests to a POSITA each element of Claim 9 according to the mapping and charting below pointing to the same or similar elements from other claims. Ex. 1002, ¶ 119.

Claim elements 9[pre] and 9[b] are identical to claim elements 1[pre] and 1[a] respectively. Moreover, the "terminal" of claim element 9[a] overlaps with the "single terminal of the controller" recited in claim element 1[b]. Further, claim element 9[e] overlaps in subject matter with claim elements 1[a] and 1[d]. Thus, claim elements 9[pre], 9[a], 9[b], and 9[e] are disclosed in the same manner as described above for their respective counterparts in Claim 1. Ex. 1002, ¶ 120.

Claim element 9[c] recites "a sensor coupled between the terminal and the switching control." As described above for claim elements 1[b] and 1[d], however, the proposed combination of Spampinato and Mobers discloses that the sensor is coupled to receive a signal from a single terminal of the controller, and that in turn,

the switching control is responsive to the sensor. Because the sensor receives a signal from the single terminal and outputs a signal to the switching control, the sensor is "between" the terminal and the switching control. Therefore, claim element 9[c] is disclosed in the same matter as described above for claim elements 1[b] and 1[d]. Ex. 1002, ¶ 121.

Finally, claim element 9[d] recites similar subject matter as the combination of claim elements 1[b] (reciting the sensor coupled to receive a signal from the single terminal of the controller), 1[c] (reciting that the signal is to represent the line voltage and the output voltage during respective portions of the on-time and off-time), and claim 6 (specifying the current/voltage form of the respective signals representative of the input voltage and output voltage). Thus, claim element 9[d] is disclosed in the same manner as described above for claims elements 1[b], 1[c], and Claim 6. Ex. 1002, ¶ 122.

9[pre]. A controller for a power converter, comprising:	*See* Section VI.A.2, Claim 1[pre].
[9a] a terminal	*See* Section VI.A.2, Claim 1[b].
[9b] a switching control that switches a power switch to regulate an output of the power converter;	*See* Section VI.A.2, Claim 1[a].
[9c] a sensor coupled between the terminal and the switching control,	*See* Section VI.A.2, Claim 1[b]. *See* Section VI.A.2, Claim 1[d].

[9d] the sensor coupled to sense a voltage at the terminal of the integrated controller, wherein the sensed voltage is representative of an output voltage of the power converter, and wherein the sensor is further coupled to sense a current at the terminal of the integrated controller, wherein the sensed current is representative of an input voltage of the power converter, and	*See* Section VI.A.2, claim elements 1[b], [c]. *See* Section VI.A.3, Claim 6.
[9e] wherein the switching control switches the power switch in response to the sensor.	*See* Section VI.A.2, Claim 1[a]. *See* Section VI.A.2, Claim 1[d].

6. Claims 12 and 13

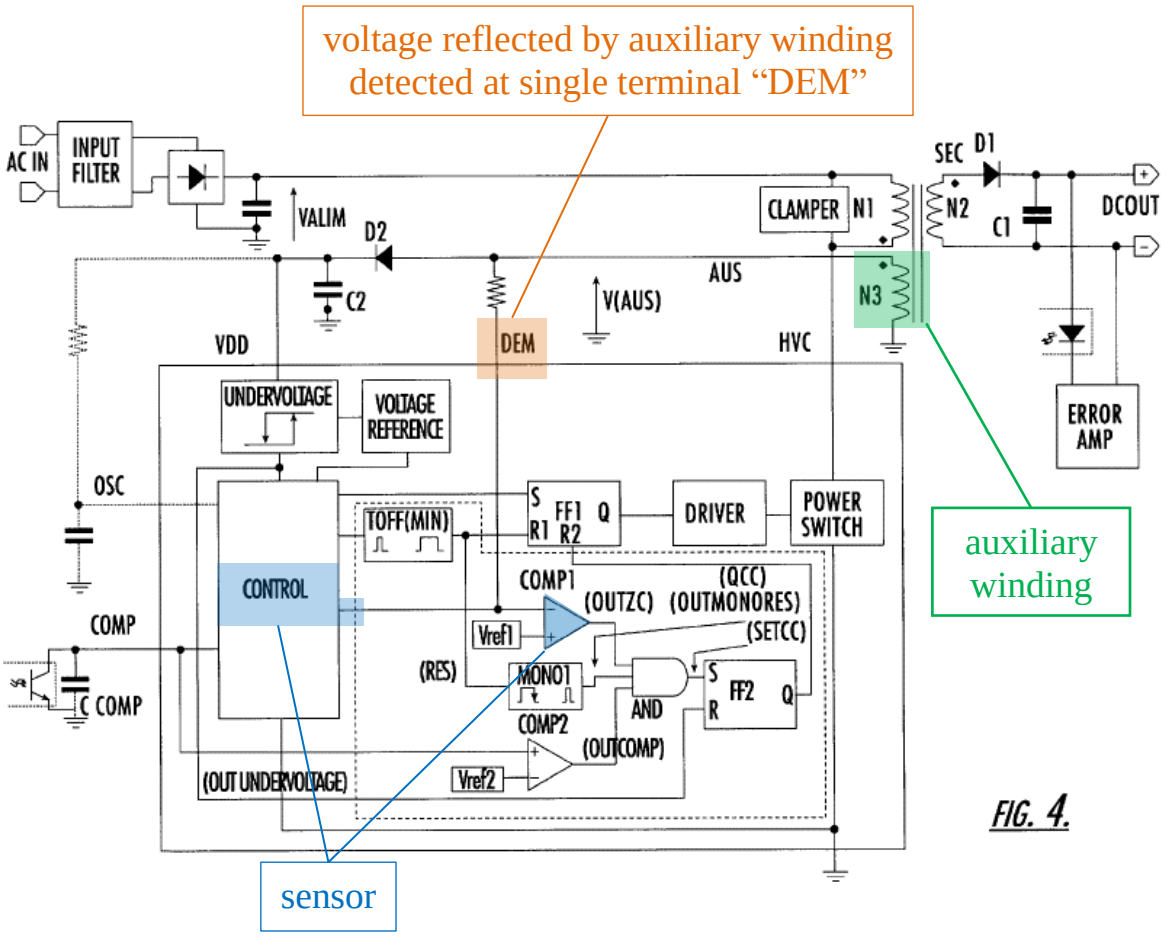
Claim 12 and 13 depend from Claim 9, but otherwise recite the same subject matter as Claims 7 and 8. Accordingly, the combination of Spampinato and Mobers discloses and suggests to a POSITA each limitation of Claims 12 and 13 in the same manner as described above. Ex. 1002, ¶ 123.

12. The controller of claim 9, wherein the controller is an integrated circuit controller for the power converter. 13. The controller of claim 12, wherein the power switch is integrated into the integrated circuit controller.	*See* citations for Claim 9. *See* citations for Claims 7 and 8 in Section VI.A.4.

B. Ground 2: Claim 8 is Obvious Over Spampinato Under 35 U.S.C. § 103

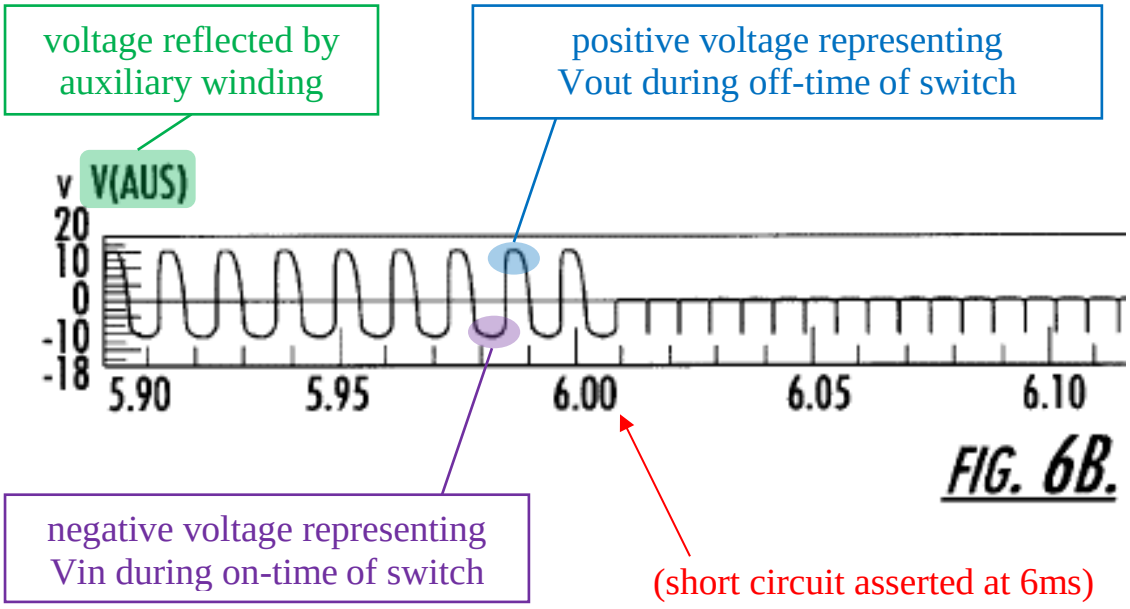
Spampinato, combined with the knowledge of a person of ordinary skill in the art, discloses and suggests each element of Claim 8 and thus renders Claim 8 obvious under 35 U.S.C. § 103. *See* Ex. 1002, ¶¶ 124-128.

Spampinato illustrates a controller, including a sensor, that receives a signal from auxiliary winding N3 via the "DEM" pin (i.e., the single terminal).



Ex. 1015, Fig. 4 (annotations added); Ex. 1002, ¶ 125. As described in Section III, a POSITA would understand that the magnetic coupling of the auxiliary winding causes the auxiliary winding to (i) produce a positive voltage representative of the output voltage during the off-time of the power switch, and (ii) produce a negative voltage representative of the input line voltage during the on-time of the power switch. Ex. 1002, ¶ 125.

Thus, a POSITA would understand that the positive voltage swing of the signal received from Spampinato's DEM pin during the off-time of the switch ***represents*** the output voltage of the power converter, while the negative voltage swing the signal received from Spampinato's "DEM pin during the on-time of the switch ***represents*** the line input voltage:



Ex. 1015, Fig. 6B (annotations added); *see also id.*, 6:7-18; Ex. 1002, ¶ 126.

Moreover, as described in Section V.A, the plain meaning of the claims requires that the "sensor" be coupled to receive a signal from the single terminal that represents the line input voltage and the output voltage at different times in the switching cycle. There is no requirement in Claim 1, however, regarding whether or how the sensor must respond to the various items of information represented by the signal at different times during the switching cycle. Thus, Spampinato meets

the limitations of claim element 1[b] regardless of whether the Spampinato's sensor is configured to detect the input line voltage information, in addition to the output voltage information, that is present on the signal received from the DEM pin. Ex. 1002, ¶ 127.

A POSITA would therefore understand Spampinato to disclose and suggest each limitation of claim elements 1[b] (reciting the sensor) and 1[c] (reciting what the signal received from the single terminal must represent). Ex. 1002, ¶ 128. Spampinato also discloses and suggests every other element of Claim 8 (and intervening Claims 1 and 7) as described and charted above for Ground 1.

1[pre]. A controller for a power converter, comprising:	*See* Spampinato citations in Section VI.A.2, Claim 1[pre].
[1a] a switching control that switches a power switch to regulate an output of the power converter; and	*See* Spampinato citations in Section VI.A.2, Claim 1[a].
[1b] a sensor coupled to receive a signal from a single terminal of the controller,	*See* Spampinato citations in Section VI.A.2, Claim 1[b].
[1c] the signal from the single terminal to represent a line input voltage of the power converter during at least a portion of an on time of the power switch, the signal from the single terminal to represent an output voltage of the power converter during at least a portion of an off time of the power switch,	*See* Spampinato citations in Section VI.A.2, Claim 1[c].
[1d] wherein the switching control is responsive to the sensor.	*See* Spampinato citations in Section VI.A.2, Claim 1[d].

7. The controller of claim 1, wherein the controller is an integrated circuit controller for the power converter. 8. The controller of claim 7, wherein the power switch is integrated into the integrated circuit controller.	*See* Spampinato citations in Section VI.A.4, Claims 7-8.

VII. CONCLUSION

Petitioner respectfully requests that *inter partes* review of the '483 Patent be instituted and that Claims 6, 8, 9, 12, and 13 be cancelled as unpatentable under 35 U.S.C. § 318(b).

Respectfully submitted,
BAKER BOTTS L.L.P.

September 28, 2018
Date

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Lead Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition, exclusive of the exempted portions as provided in 37 C.F.R. § 42.24(a), contains no more than 11348 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24(a). The word count was calculated by starting with Microsoft Word's total document word count and subtracting the words for the Table of Contents, the Exhibit List, the Mandatory Notices, the Certificate of Compliance, and the Certificate of Service.

September 18, 2018
Date

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CERTIFICATE OF SERVICE

In accordance with 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on the 28th day of September, 2018, a complete and entire copy of the **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,077,483** and any accompanying exhibits was served on the patent owner at the correspondence address of record for the subject patent,

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Seattle, WA 98101

via Express Mail or by means at least as fast and reliable as Express Mail. Additionally, the same were also served upon counsel for the subject patent's owner, Power Integrations, Inc.,

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because that is likely to affect service.

In accordance with § 42.51(b)(1), the undersigned certify that Petitioner is not aware of, and therefore does not provide any "relevant information that is inconsistent with a position advanced by petitioner[]."

September 28, 2018
Date

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