UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

MEMORY TECHNOLOGIES, LLC
Patent Owner

Case No.: To Be Assigned
U.S. Patent No. 9,367,486

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,367,486

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED (37 C.F.R. §42.22(A))

Kingston Technology Company, Inc. ("Petitioner" or "Kingston") hereby petitions to institute an *inter partes* review of Claims 8-10, 14-17, and 21 (the "Challenged Claims") of U.S. Patent No. 9,367,486 (the "'486 Patent") to Hyvonen *et al*. (Ex. 1001), and cancel those claims as unpatentable.

As discussed below, the prior art anticipates and/or renders obvious the Challenged Claims of the '486 Patent under 35 U.S.C. § 102 and/or § 103. Accordingly, there is a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim, and Petitioner respectfully requests that the Board institute a trial for *inter partes* review and cancel all Challenged Claims as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. §42.8(A)(1))

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Kingston Technology Company, Inc., is a real party-in-interest. Petitioner's parent company, Kingston Technology Corporation ("Kingston Holding"), is a holding company without any employees or operations. However, because Kingston Holding is the sole owner of Petitioner and shares some directors, Petitioner identifies Kingston Holding as an additional real party-in-interest.

B. Identification of Related Matters (37 C.F.R. §42.8(b)(2))

Patent Owner Memory Technologies, LLC ("MTL") has asserted the Challenged Claims of the '486 Patent, as well as claims from seven other patents, against Kingston in a co-pending litigation, *Memory Technologies, LLC v. Kingston Technology Co., Inc*., 8:18-cv-00171 (C.D. Cal.). MTL's original Complaint was filed on January 31, 2018, and served on Kingston, at the earliest, on February 1, 2018.

In addition to this Petition, Kingston has or will be filing petitions for *inter partes* review of the other seven patents that MTL has asserted against it.

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **Kingston-486ipr@pillsburylaw.com**.

Lead Counsel	Back-Up Counsel
Robert C.F. Pérez (Reg. No. 39,328) PILLSBURY WINTHROP SHAW PITTMAN LLP 1650 Tysons Boulevard, 14th Floor McLean, VA 22101 Telephone: 703.770.7900 Facsimile: 703.770.7901	**Christopher Kao** (*Pro hac vice* motion to be filed) **Brock S. Weber** (*Pro hac vice* motion to be filed) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200

D. Payment of Fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit Account No. 033975 for the petition fee and for any other required fees.

III. REQUIREMENTS FOR *INTER PARTES* REVIEW

A. Identification of Challenge

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests that the Challenged Claims of the ’486 Patent be cancelled as anticipated or render obvious based on the following grounds:

Ground	'486 Patent Claims	Basis for Rejection
1	8, 10, 14, 15, 17, and 21	§ 103 based on *CompactFlash* and *Toombs*
2	8, 14, 15, and 21	§ 103 based on *Ziv, Vogt,* and *Toombs*
3	8, 14, 15, and 21	§ 103 based on *Sinclair* and *Toombs*
4	9 and 16	§ 103 based on *CompactFlash* and *Elhamias*
5	9 and 16	§ 103 based on *Ziv, Vogt,Toombs*, and *Elhamias*
6	10 and 17	§ 103 based on *Ziv*, *Vogt,* and *Toombs*
7	10 and 17	§ 103 based on *Sinclair* and *Toombs*

The Declaration of R. Jacob Baker, Ph.D., P.E., filed herewith (Ex. 1002, "Baker Decl."), supports the challenge in this Petition that the Challenged Claims are invalid as anticipated and obvious.

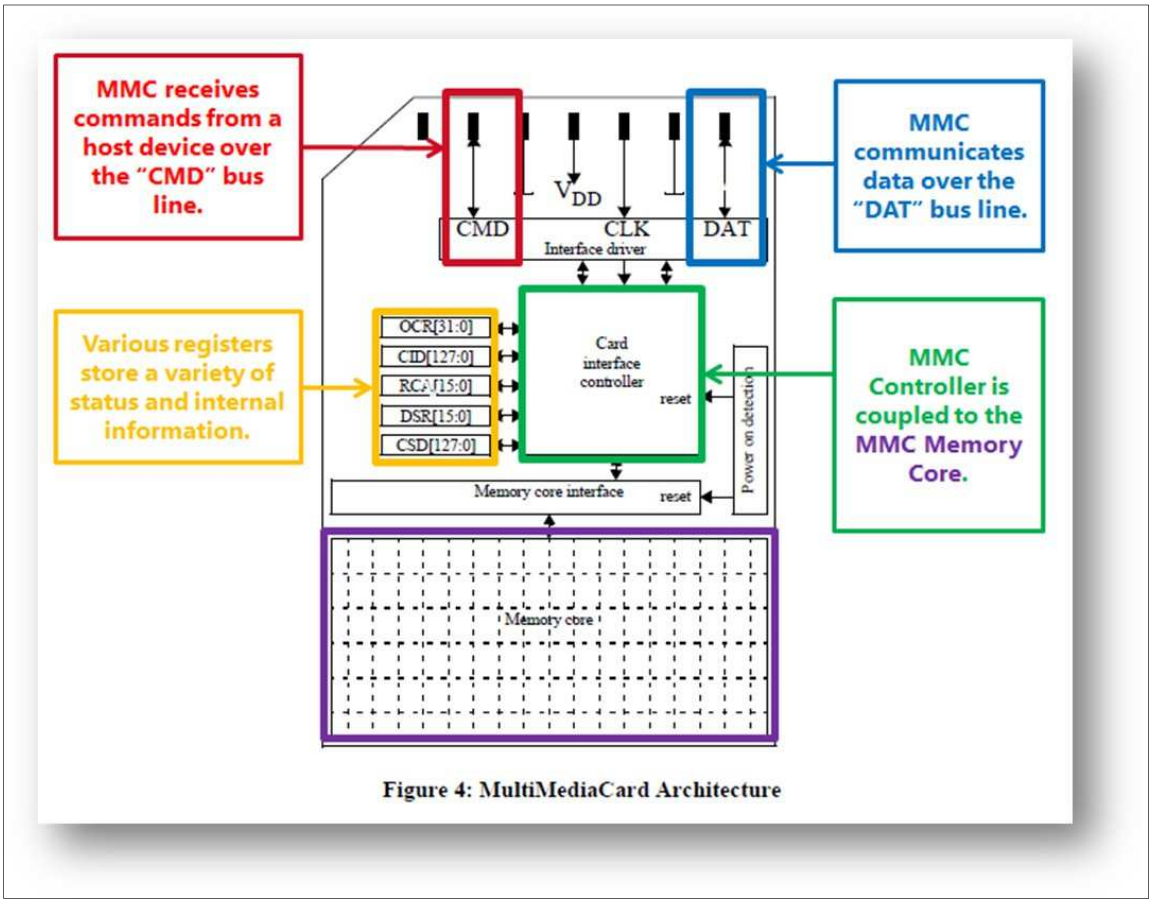
IV. A PERSON OF ORDINARY SKILL IN THE ART

Relative to the '486 Patent, a person of ordinary skill in the art ("POSITA") is a person having at least a bachelor's degree in electrical engineering, computer engineering, or equivalent training, with at least two years of academic or industry experience in the field of memory system design. Ex. 1002 at ¶65. However, a higher level of education could make up for less experience, and vice versa. *Id*.

V. BACKGROUND OF THE TECHNOLOGY

A memory device is used to store electronic data. Ex. 1002 at ¶68. By 2008, several types of memory devices that use flash or EEPROM memory were in existence, including MultiMediaCard ("MMC") and CompactFlash ("CF"). *Id.* An MMC can communicate with a host device. Ex. 1010 at 19. As depicted below, for example, an MMC receives commands from a host device over a

"CMD" bus and communicates data over the "DAT" bus line. Ex. 1002 at ¶74; *see* Ex. 1010 at 142, Fig. 4 (shown below).



Ex. 1010 at Fig. 4 (annotated).

VI. OVERVIEW OF THE '486 PATENT

The '486 Patent issued on June 14, 2016 from U.S. Patent Application No. 14/732,507 ("'507 Application") filed on June 5, 2015. The '486 Patent is a continuation of application No. 13/951,169 filed on July 25, 2013, now U.S. Patent No. 9,063,850, which is a continuation of application No. 13/645,588 filed on October 5, 2012, now U.S. Patent No. 8,601,228, which is a continuation of

application No. 12/039,672, filed on February 28, 2008, now U.S. Patent No. 8,307,180.

A. Summary of the Claimed Subject Matter

The Challenged Claims generally relate to access profiles. An access profile "governs the current access operations to the memory device." Ex. 1001 at 5:2-4. The Challenged Claims, in particular, relate to activating an access profile and configuring a memory device in accordance with an access profile, so that the device is effective for a usage in accordance with the activated profile. The access profile "governs the current access operations to the memory device." Ex. 1001 at 5:2-4. The access profiles correspond to memory access operations, such as "a read, a write, an erase, and a modify attribute operation." Ex. 1001 at 2:9-10.

The '486 Patent specification describes the invention as applicable "in any stand-alone or embedded system that comprises or accesses a memory device." *Id.* at 5:38-40. When connected to such a system, the memory device can "receive one or more commands . . . for activating a particular access profile." *Id.* at 4:42-45. The portion of the system that issues commands to the memory device is referred to as a "host." *Id.* at 3:5-9.

The '486 Patent specification also describes configurations that may correspond to access profiles. For instance, in a "burst profile mode, [an access profile,] corresponding to fast, contiguous data access," the memory device is

configured so that "after receiving all the data" to be written from a host, it may "indicate 'exit busy' and set the transfer mode to 'transfer state,' thus facilitating faster execution of subsequent accesses by the host." *Id.* at 7:32-35.

Other access profiles may cause the device to configure itself such that a particular profile is "associated with different partitions of the memory device," including either "logical or physical partitions." *Id.* at 7:50-51.

B. The '486 Patent Prosecution History

The '486 Patent issued from U.S. Application No. 14/732,507. Before issuance, Applicant responded to two office actions. Ex. 1009 at 114, 243.

The first office action rejected a set of claims that Applicant eventually cancelled. By way of example, the Applicants asserted the following exemplary claim:

> 1. A method for configuring access to a memory device, comprising:
>
> receiving one or more commands for activating one or more access profiles associated with the memory device; and
>
> configuring access to the memory device in accordance with at least one of the access profiles.

Id. at 50 (displaying originally presented claims prior to First Office Action).

The Examiner initially rejected the claims under Double Patenting over claims 1-37 of U.S. Patent No. 8,307,180. The claims were further rejected as

being anticipated by *Burgan*. In response to the rejection, the Applicant subsequently cancelled all pending claims and asserted a new set of Claims 21-48.

A second, final office action maintained the rejection under Double Patenting over claims 1-37 of U.S. Patent No. 8,307,180. *Id.* at 188. However, the Examiner provided that Claims 21-48 would be allowable if they were to overcome the double patenting rejection by filing a terminal disclaimer. *Id.* at 190.

In response, the Patent Owner submitted a Terminal Disclaimer and a Notice of Allowance subsequently issued. *Id.* at 251, 286.

C. The '180 Patent Prosecution History

The '486 Patent claims priority to the '672 Application, which later issued as U.S. Pat. No. 8,307,180 ("'180 Patent"). As such, the prosecution history of the '180 Patent is relevant to the '486 Patent. *Ormco Corp. v. Align Tech., Inc*., 498 F.3d 1307, 1314 (Fed. Cir. 2007).

Before issuance of the '180 Patent, Applicant responded to three office actions and submitted a notice of appeal and a pre-appeal brief. Ex. 1011 at 327, 393, 406, 440. The resulting '180 Patent issued on Nov. 6, 2012.

The first office action rejected the claims as anticipated by *Burgan*. *Id.* at 443. *Burgan* teaches smart phones with various profiles, such as a work profile and a family profile, that are accessed in response to caller ID information of a received call. Ex. 1012 at ¶¶5-6.

Applicant's response to the first office action is relevant to the "command" claim element. According to Applicant, "***[a] command in the context of the various embodiments of the present application***, and in any other context for that matter, ***suggests some type of authoritative direction or instruction to do/not to do something."*** Ex. 1011 at 427 (emphasis supplied). Using this definition, Applicant submitted that a POSITA would not equate the received Caller ID information in *Burgan* with an actual "command," because a Caller ID is a "passive" identifier. Ex. 1011 at 427.

Unconvinced by the Applicant's argument, the Patent Office subsequently issued a final rejection on July 6, 2011, maintaining the rejection. *Id.* at 408. The Examiner again rejected the claims over *Suwa* and *Bertone*. *Id.* at 329. Applicant made substantial amendments to the claims to distinguish *Suwa* and *Bertone* by further limiting a predefined access profile and the received one or more commands. *Id.* at 259-268. The amendments to Claim 17 are shown below:

17. (Currently Amended) A memory device, comprising:

one or more registers for storing one or more predefined access profiles associated with said memory device, said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;

~~receiving means~~ a controller for receiving one or more commands related to said at least one usage of said memory device, said one or more commands for activating said one or more predefined access profiles associated with said memory device, said controller also

~~; and~~

~~configuring means~~ for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.

Id. at 261.

Applicant also clarified the claim limitation "configuring access to said memory device." Applicant argued that, unlike the claim requiring "configuring access to said memory device," the memory device in *Bertone* only configures the memory device according to "timing characteristics to control the speed performance of the memory module." Ex. 1013 at 266-67. Applicant argued that merely changing an operating speed for the memory device ***does not*** constitute an access configuration.

Applicant also contended that *Suwa* does not configure an access profile, because the switcher in *Suwa* "automatically completes necessary changes to use the selected mode" upon activation. *Id.* at 266. Applicant argued that the claimed

invention requires that the activation of an access profile ***occurs separately*** from the access configuration of the memory device.

A Notice of Allowance subsequently issued. Ex. 1011 at 244.

VII. CLAIM CONSTRUCTION

A. Legal overview

Claims are construed under "the standard used in federal courts, . . . which is articulated in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005)." 83 FR 51340. Under this standard, claim construction starts with the intrinsic evidence. *Phillips*, 415 F.3d at 1312-17. The "words of a claim are generally given their ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13.

All claim terms of Challenged Claims of the '486 Patent have been accorded their plain and ordinary meaning as understood by POSITA and consistent with the intrinsic record. Petitioner's interpretation of the claim terms in the '486 Patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below, in Grounds 1-7.

Under the *Phillips* standard and for clarity, Petitioner provides the following specific constructions.[1]

B. Claim Terms

1. "predefined access profile"

The Challenged Claims describe "access profiles" in several different ways. An access profile may be a mode, setting, control, or logic for an access operation, each of which is disclosed in the specification. The Board should construe "predefined access profile" to mean a "mode, setting, control, or logic defined in advance for reading, writing, modifying, deleting, or changing the attributes of data." Ex. 1002 at ¶¶141-143.

For example, the '486 Patent discloses that a profile can be a mode: "one profile may be defined as a burst profile **mode**, corresponding to a fast, contiguous data access **mode.**" Ex. 1001 at 7:29-31 (emphasis added); *id.* at 4:56-68 (random mode profile).

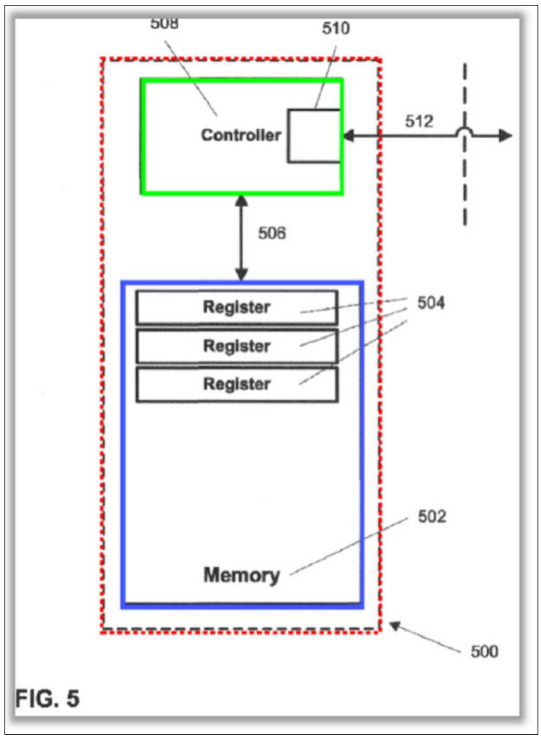
[1] Petitioner reserves the right to address any claim construction positions taken by the Patent Owner in its Preliminary Response, if any, including under 37 C.F.R. § 42.108(c). Petitioner further reserves its ability to show that claims of the '486 Patent are invalid under 35 U.S.C. §112 in the co-pending litigation, despite offering explicit and implicit claim constructions herein.

The specification also describes that profiles can be a control or setting: "the access profile associated with a media device may be adapted to comprise different **control and/or setting** profiles that are associated with different partitions of the memory device." *Id.* at 7:46-51(emphasis added). Lastly, the specification states that "an access profile may be implemented as a binary file that further comprises the required **logic** to implement an access profile." *Id.* at 5:28-31 (emphasis added).

2. "configuring access"

The Challenged Claims provide that the "predetermined access profiles" configure access to the "memory device." The Board should construe "configuring access" to mean "setting the memory device for reading, writing, modifying, deleting, or changing the attributes of data." Ex. 1002 at ¶¶144-146.

In Fig. 5 of the '486 Patent, the "memory device" (red box) includes many components. Ex. 1001 at Fig. 5. For example, as depicted below, memory device 500 contains a "memory" 502 (blue box), "controller" 508 (green box), an interface (506) through which communications between the controller and the memory may be conducted, and another interface (512) for communications with a host device. *Id*.



Ex. 1001 at Fig. 5.

Thus, the proposed construction provides that the predefined access profiles can also configure data on the controller (green box) or other components of the "memory device" (red box), as indicated by the intrinsic evidence. Ex. 1002 at ¶¶144-146.

3. "usage"

The Challenged Claims provide that the "usage" means "host activity in accordance with the predefined access profile." Ex. 1002 at ¶¶147-148.

For example, the Challenged Claims provide that the memory device "receives one or more commands related to a least one usage of said memory device and that the predefined access profiles determine how access is configured

for said at least one usage." Ex. 1001 at 2:39-67 (emphasis added). Because the commands are "received" for a usage "of the memory device" and the "access is configured" for the usage, it is clear that "usage" refers to host activity, as that is where the commands can originate and the device that is accessing the memory card. This is also clear from the specification. Specifically, the '850 Patent states that an access profile "governs the current access operations to the memory device" by the host device. Ex. 1001 at 5:2-3.

VIII. SUMMARY OF PRIOR ART

A. CompactFlash

A CompactFlash device is a flash memory mass storage device. Ex. 1002 at ¶150. SanDisk first manufactured a CompactFlash device in 1994. Ex. 1016 at 1:56-59. CompactFlash quickly became the go-to portable mass storage device for electronic devices. Ex. 1002 at ¶151. CompactFlash remains popular and is supported by many devices. *Id.*

In 1995, the CompactFlash Association was formed by a group of international companies with the goal of creating an industry standard for flash-based mass storage. *Id.* at ¶152. The CompactFlash specification establishes the methods, processes, and practices for both the CompactFlash device and a host interacting with the device. *Id.* at ¶153.

On December 23, 2004, the CompactFlash Association released CompactFlash Specification Revision 3.0 (*CompactFlash*). Ex. 1003 at 1; Ex. 1022 at ¶7 (Declaration of Michael Asao, consultant for the CompactFlash Association). *CompactFlash* was made publicly available to any interested member of the public free of charge prior to 2008, as, for example, the CompactFlash Association publicly announced on January 6, 2005 that *CompactFlash* "is available to download free from the CFA website at http://www.compactflash.org." Ex. 1024 at 9; Ex. 1023 at ¶6 (authenticating page 9 of Ex. 1024 as an accurate representation of the January 6, 2005 announcement by the CompactFlash Association); *see also* Ex. 1015 (Jan. 7, 2005 article stating that "[t]he CF Specification Revision 3.0 is available to download free from the CFA web site at http://www.compactflash.org"); Ex. 1016 at ¶3 (describing an exemplary hard drive that utilizes a CompactFlash interface "as described in the CF+ and CompactFlash Specification Revision 3.0, published by the CompactFlash Association, Palo Alto, Calif., Dec. 23, 2004, http://www.compactflash.org.") (published on Apr. 5, 2007).

Moreover, *CompactFlash* was freely and publicly available online from the CompactFlash website as of at least January 13, 2005. Ex. 1022 at ¶7; Ex. 1024 at 2-3 (displaying the CompactFlash homepage indicating that *CompactFlash* "is now available to download" on Jan. 13, 2005); *Id.* at 6 (displaying the registration form

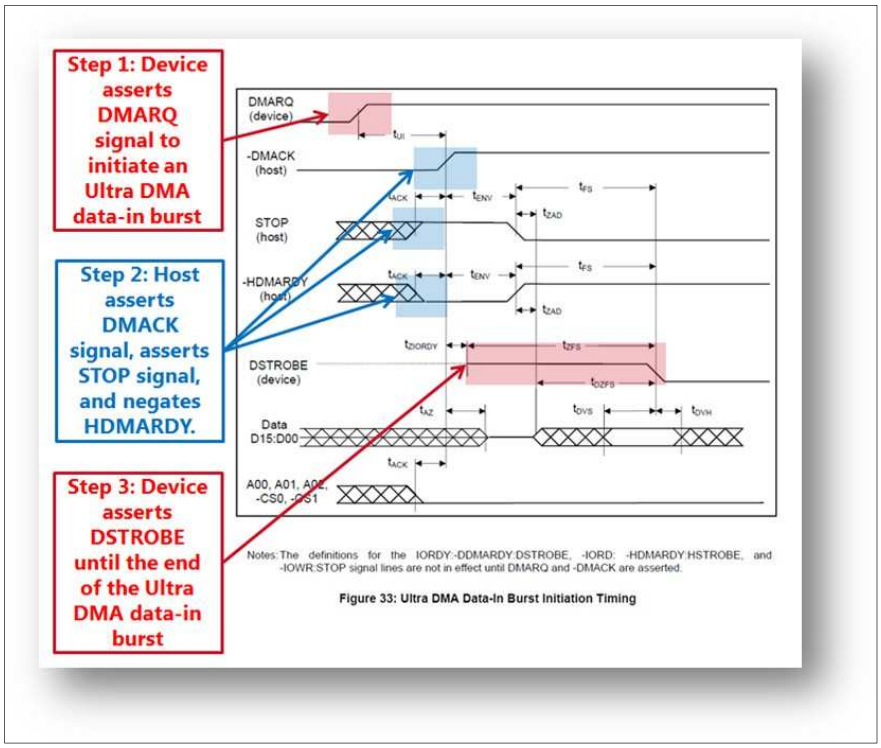
that once submitted included a link for a free download for *CompactFlash*); Ex. 1023 at ¶6 (authenticating pages 2-3 of Ex. 1024 as an accurate representation of the CompactFlash Association website on January 13, 2005 and page 6 of Ex. 1024 as an accurate representation of the CompactFlash registration form on January 27, 2005). *See Crestron Electronics Inc. v. Intuitive Building Controls Inc.,* Case IPR2015-01460, slip op. at 12-22 (PTAB Jan. 14, 2016) (Paper 14). Accordingly, *CompactFlash* qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 102(b). *CompactFlash* was not previously presented to the PTO in the context of the '486 Patent.

The CompactFlash Association made improvements to direct memory access (DMA) data transfer in Revision 3. A DMA data transfer occurs directly between the hardware subsystem and the memory device, rather than involving the host's CPU as an intermediary. Ex. 1002 at ¶157. In this manner, transfer speeds are boosted and the CPU is freed to work on other tasks while the transfer occurs. *Id.* Starting with Revision 3.0, "UltraDMA" was introduced, which boosted DMA transfer speed four-fold from the prior "MultiWord DMA" transfer. Ex. 1016 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").

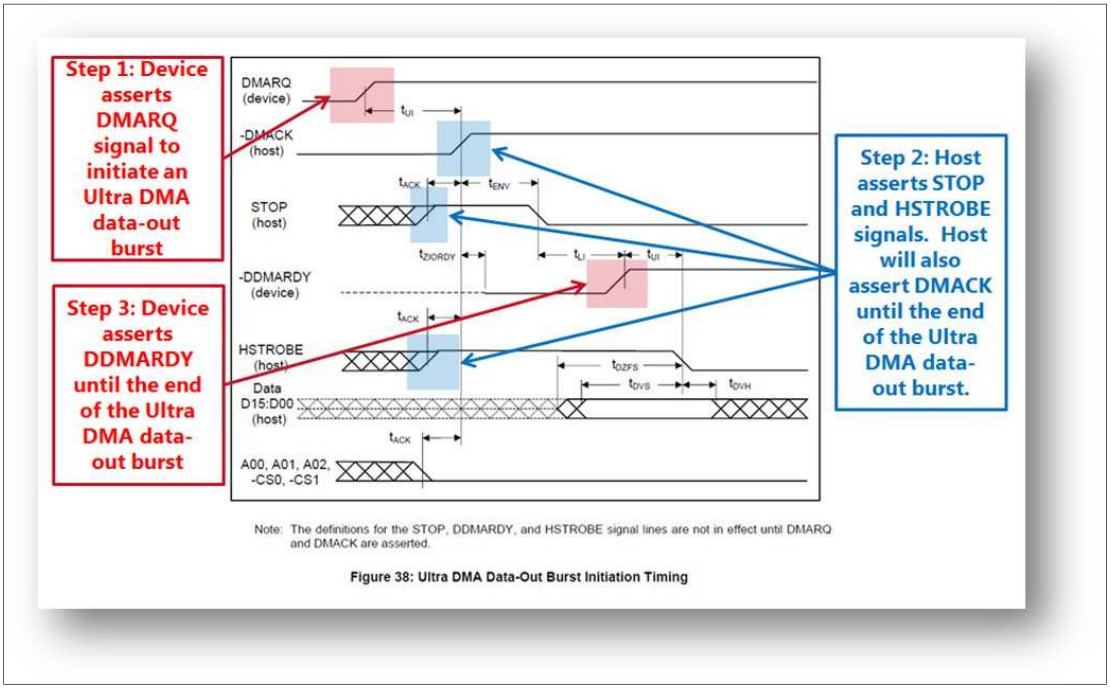
CompactFlash also introduced several Ultra DMA modes. Ex. 1003 at 137. A CompactFlash controller configures a CompactFlash device to perform the

Ultra-DMA transfer according to a protocol based on the mode selected. When a host sets an Ultra DMA mode, the memory device automatically disables any enabled MultiWord DMA mode. *Id.* at 158. In response, the memory device sets the selected Ultra DMA mode in a task file register. *Id.* at 120.

The host may subsequently communicate a READ DMA or WRITE DMA command to transfer data to the device. *Id.* at 68. The CompactFlash device, in response, will begin the Ultra DMA-specific initiation protocol to configure the memory device for an Ultra DMA transfer. *Id.* at 68-70. As illustrated for a data-in burst in Fig. 33 and a data-out burst in Fig. 38 (both shown below), the controller starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal. *Id.* at 75-76, 81-82. After the host responds by asserting and/or negating several signals, the controller will assert either a DSTROBE signal or DDMARDY signal until the end of the burst. *Id.* at 75-76, 81-82. Finally, unlike the older MultiWord DMA modes, the device will calculate a CRC value to ensure the accuracy of the data transferred in the Ultra DMA modes. *Id.* at 90. If the memory device detects errors, an Error Register is updated to reflect the error. *Id.* at 90.



Id. at 76, Fig. 33 (annotated).

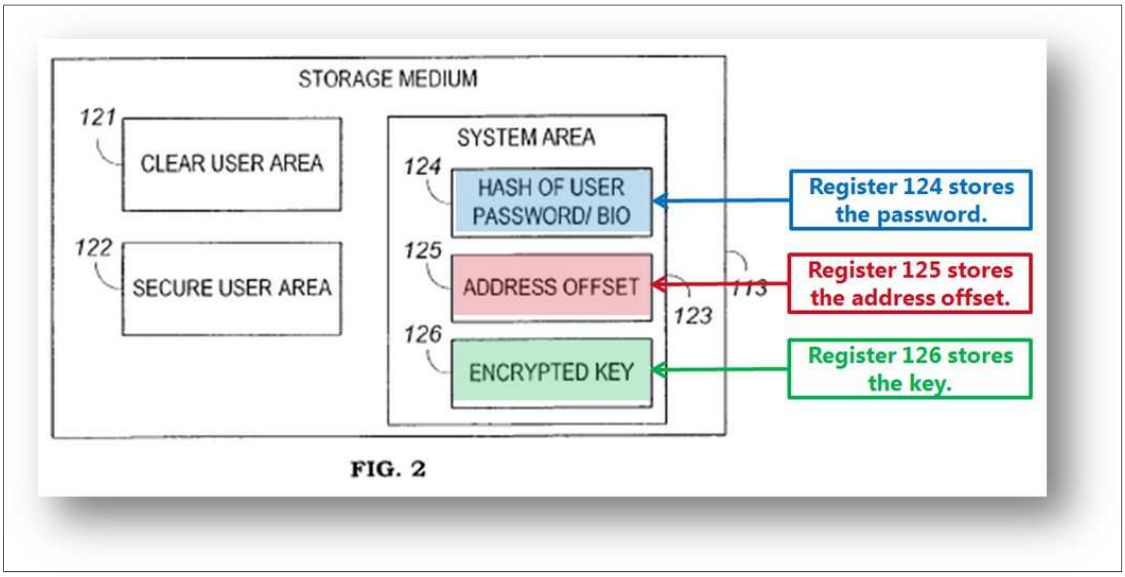


Id. at 85, Fig. 38 (annotated).

B. United States Patent No. 7,478,248 (Ziv)

Ziv was filed November 27, 2002, and published on May 27, 2004. *Ziv* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Ziv* was not previously presented to the PTO in the context of the '486 Patent.

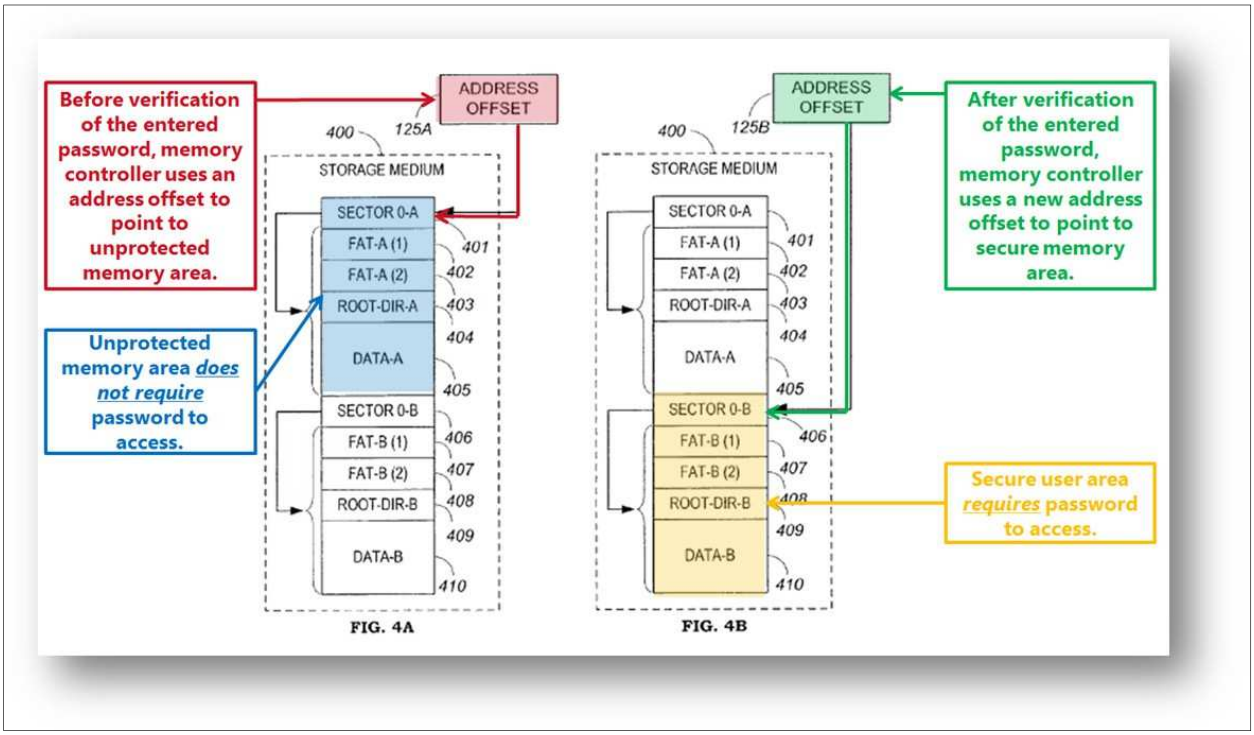
Ziv discloses a memory controller that allows profile-based access to an encrypted partition of memory. Ex. 1004 at Abstract. A user first selects a password that is hashed and stored in a register. *Id.* at 4:15-20. The system also generates a cryptographic key, which is used with a stored address offset for accessing the secure area. *Id.* at 5:14-15.



Id. at Fig. 2 (annotated).

The secure memory area is activated when the host transmits a valid password to the controller. *Id.* at 6:15-22. Then the memory controller remounts

the memory by using the stored address offset in the register to point to the secure partition (as illustrated in Fig. 4B). *Id.* at 6:42-49, Fig. 4B (shown below).



Id. at Figs. 4A-B (annotated).

C. United States Patent No. 6,681,304 (*Vogt*)

Vogt was filed June 30, 2000 and issued on January 20, 2004. *Vogt* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Vogt* was not previously presented to the PTO in the context of the '486 Patent.

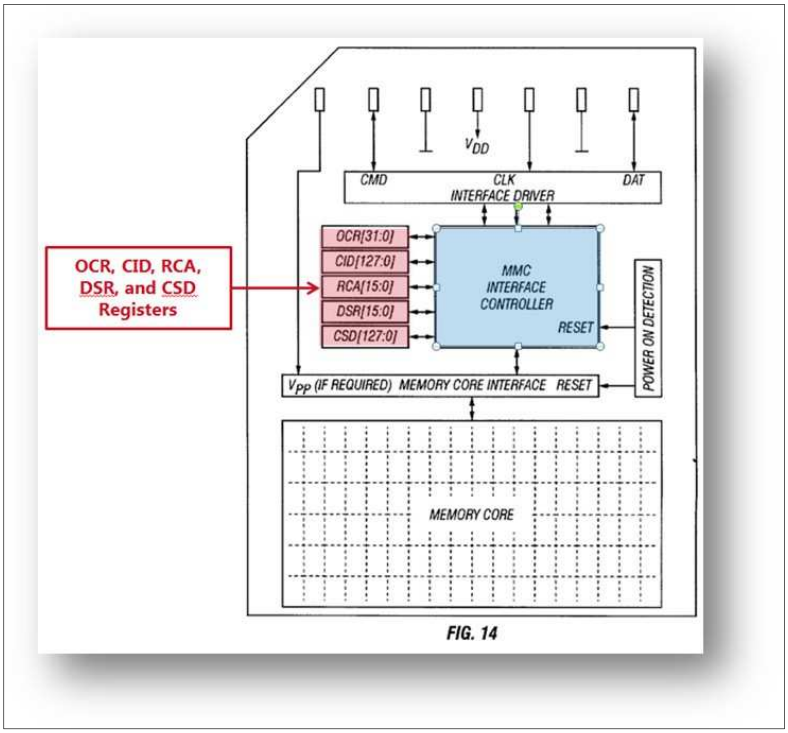
Vogt teaches a "password verify" command to access hidden storage in a memory device. Ex. 1005 at 6:35-37, 8:11-30, 11:53-55. *Vogt* also teaches implementing the hidden storage in a flash memory embedded in a device. *Id.* at 11:16-19.

Vogt further discloses a specific configuration for a read/write operation accessing a hidden storage area in the memory device. Upon receiving a memory read or write signal that attempts to access a hidden storage area address, the controller must then create a hidden storage read signal or write signal. *Id.* at 4:7-10. To create the hidden storage read/write signal, a Valid_HS_Access signal is logically "ANDed" with the memory read/write signal. *Id.* at 4:7-10. The Valid_HS_Access signal accounts that a valid user password has been entered for that specific password-protected hidden storage area. *Id.* at 3:45-4:6. Moreover, in read operations accessing a hidden storage, data is uniquely sent to a "hidden storage bus out" before transferring to the external data bus. *Id.* at 5:24-28. *Vogt* teaches a "password verify" command to access hidden storage in a memory device. Ex. 1005 at 6:35-37, 8:11-30, 11:53-55.

D. United States Patent No. 6,279,114 (*Toombs)*

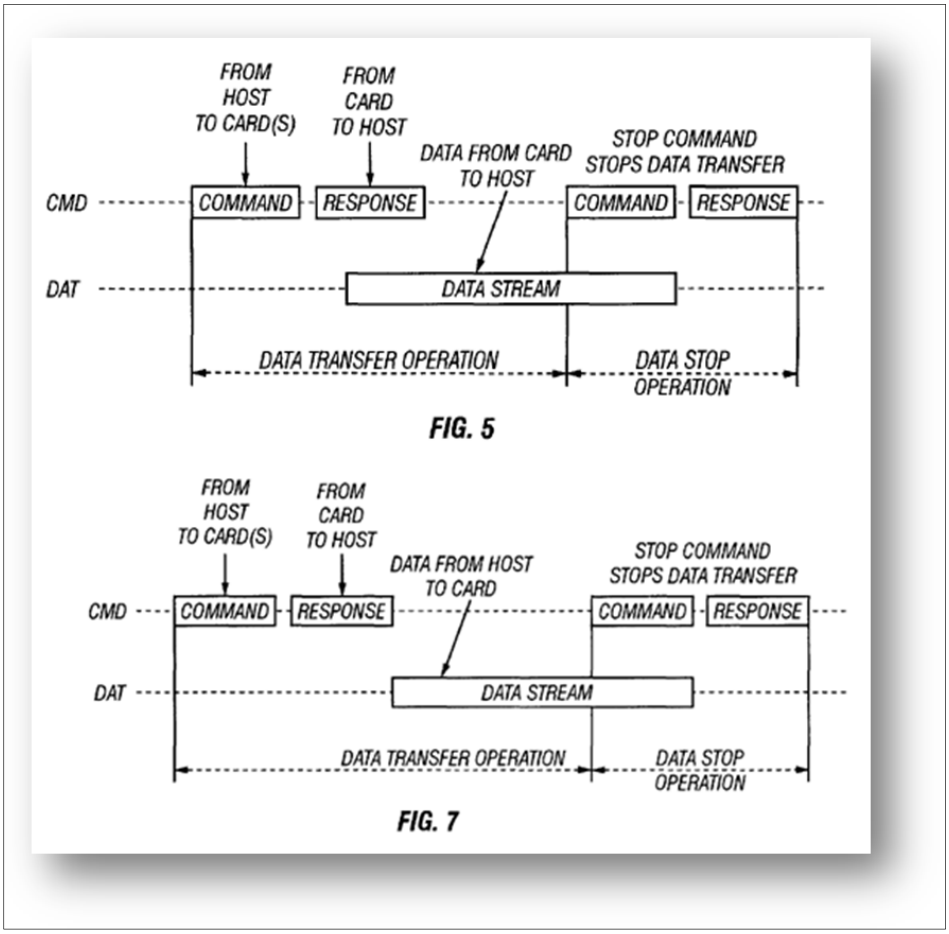
Toombs was filed November 4, 1998, and issued on August 21, 2001. *Toombs* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Toombs* was not previously presented to the PTO in the context of the '486 Patent.

Toombs teaches a MultiMediaCard having parameters stored in various registers as shown in Fig. 14 below. Ex. 1006 at 1:9-14, 6:18-38, 10:22-33, Fig. 14.



Id. at Fig. 14 (annotated).

Toombs also teaches two types of data transfer processes. *Id.* at 8:33-34. One type involves sequential data transfer commands, which initiate a sequential, "continuous data stream." *Id.* at 8:35-37; Fig. 5, 7 (shown below); Ex 1002 at ¶205. The sequential data transfer commands reduce command overhead to a minimum, because data is transferred sequentially in a DAT line. Ex. 1006 at 8:39-43.



Id. at Figs. 5, 7.

E. United States Patent No. 7,409,489 (*Sinclair)*

Sinclair was filed on October 25, 2005, claims priority to U.S. Provisional App. No. 60/705,388 filed on August 3, 2005, and was published on February 8, 2007. *Sinclair* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Sinclair* was not previously presented to the PTO in the context of the '486 Patent.

Sinclair discloses selectable reclaim operation modes that provide optimizations to the rate that memory reclaim operations (*i.e.,* background/management operations) occur. Ex. 1007 at Abstract. Reclaim

operations convert memory containing obsolete data into writeable memory. *Id.* at 2:9-11. An exemplary reclaim operation mode is the Reclaim Normal mode, which can be activated by the host sending a "Reclaim_normal" command to the memory controller. *Id.* at 23:27-30, 23:47-51. This changes the configuration of the memory device to interject reclaim operations between write commands received from the host. *Id.* at 23:47-51, 2:50-57. The device calculates an optimal interleave ratio of reclaim operations to write commands such that the memory card will run out of writeable memory only when no reclaimable memory remains. *Id.* at 2:50-57.

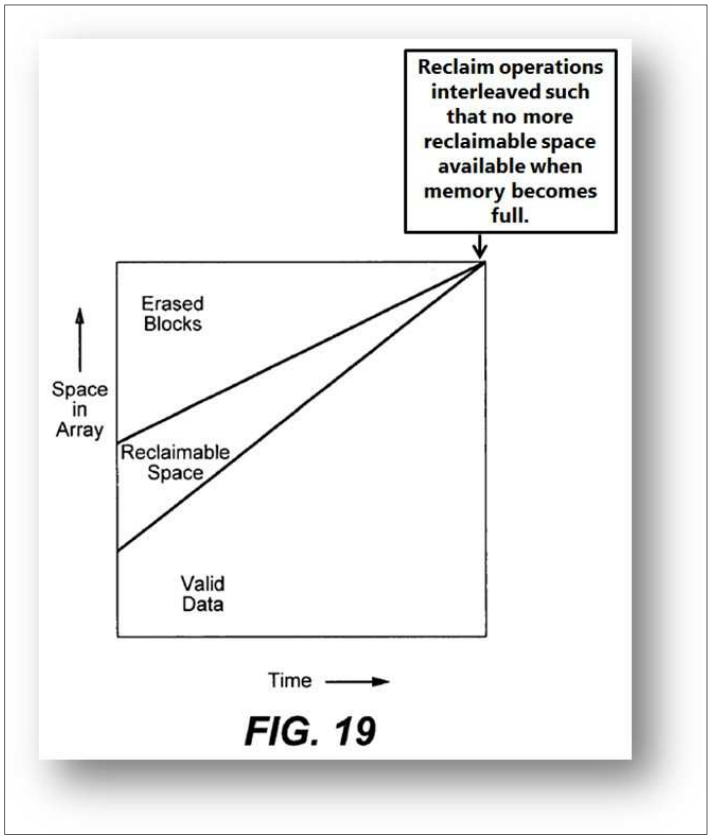
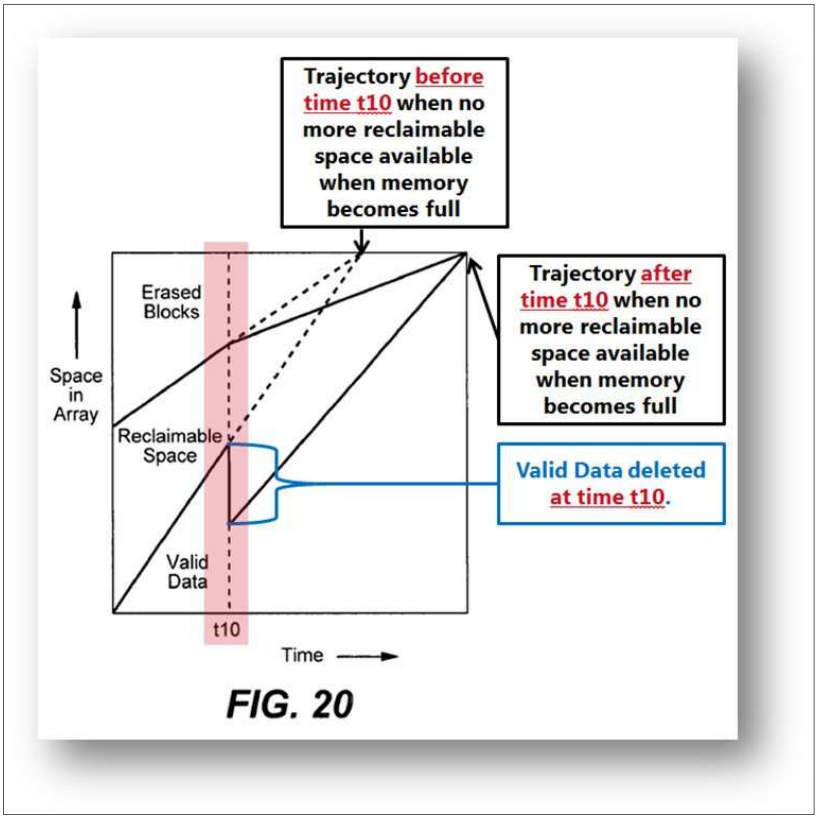


FIG. 19

Id. at Fig. 19 (displaying a time graph illustrating an optimal interleave of reclaim operations to write operations) (annotated).

The interleave ratio can be recalculated periodically or when triggered by a host command. *Id.* at 18:17-26. As shown in Fig. 20, when host issues a delete command to the memory device at time t10, the system alters the interleave ratio such that the time when no more reclaimable space is available shifts to the newly anticipated time when the memory will be filled to capacity. *Id.* at 18:12-26.



Id. at Fig. 20 (annotated).

Sinclair also describes other reclaim modes selectable by the host, such that that "the host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity." *Id.* at 23:27-30, 23:36-59.

F. United States Patent Publication No. 2006/00220054 (*Elhamias*)

Elhamias was filed on July 28, 2004 and was published on Feb. 2, 2006. *Elhamias* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Elhamias* was not previously presented to the PTO in the context of the '486 Patent.

Elhamias discloses a memory card that adapts its operation according to the application to which it is applied or the conditions under which it is operated. Ex. 1008 at ¶0008. *Elhamias* further discloses that the "maximum rate of data transfer between the host and the card is limited by the number of parallel data paths that are used." *Id.* at ¶0022. Thus, the memory card is able to receive data in parallel for its storage and send data to the host in parallel from the memory. *Id*.

IX. GROUNDS FOR CHALLENGE

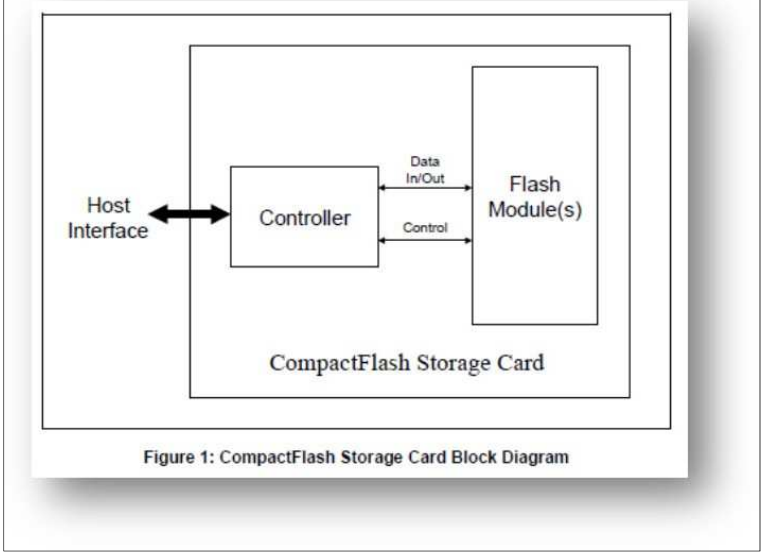
A. GROUND 1: CLAIMS 8, 10, 14, 15, 17, AND 21 ARE RENDERED OBVIOUS BY COMPACTFLASH AND TOOMBS

As shown below, *CompactFlash* and *Toombs* render obvious Claims 8, 10, 14, 15, 17, and 21 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶217-271.

1. Independent Claim 8

i. (Preamble) A method comprising:

CompactFlash discloses at least a method for improvements to direct memory access (DMA) data transfer of a flash memory storage device that contains a "controller and flash memory module(s)." Ex. 1015 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").



Ex. 1003 at 19, Fig 1 (annotated).

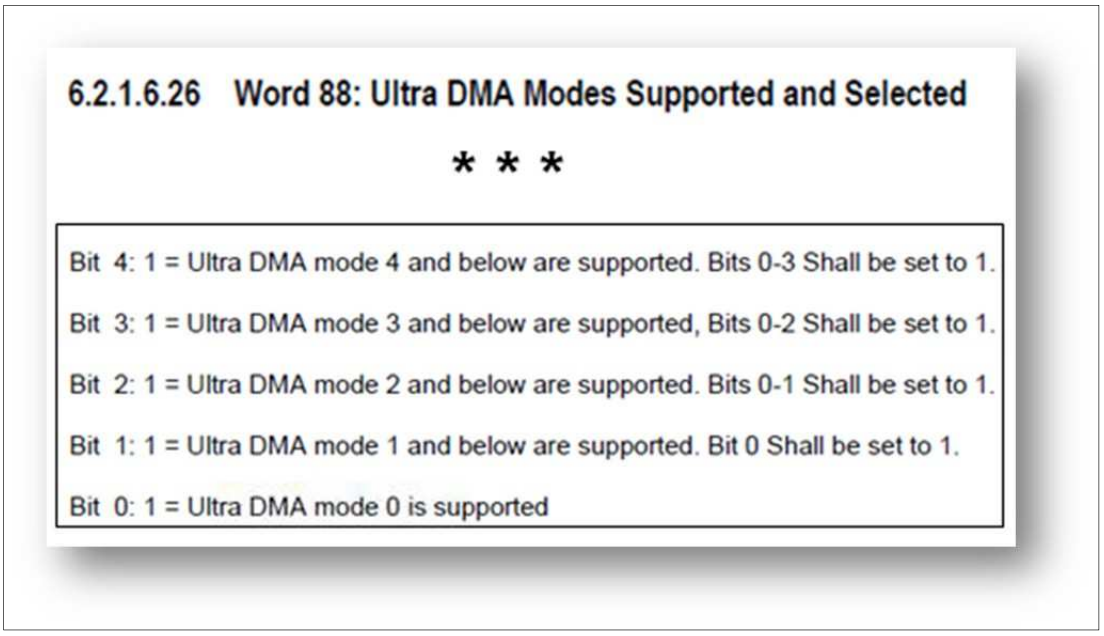
ii. receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with a memory device,

CompactFlash discloses MultiWord and Ultra DMA modes stored on the CompactFlash device. As shown in Table 53, various MultiWord DMA and Ultra DMA modes are supported, each of which constitutes a predefined access profile.

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at 158 (equating MultiWord DMA and Ultra DMA "Mode[s]" as "transfer mode number[s]"). For example, the following Ultra DMA Modes are possible:



6.2.1.6.26 Word 88: Ultra DMA Modes Supported and Selected

* * *

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

Id. at 132-33, 137.

Each DMA mode is an access profile, because the selected mode is used to determine the memory device configuration for the subsequent DMA access operations to the memory device. *See* Ex. 1001 at 5:2-4 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis supplied); Ex. 1002 at ¶¶226-229. For instance, if an Ultra DMA mode is activated (unlike MultiWord DMA modes) the device configures itself to perform a CRC check calculation after the data transfer. Ex. 1003 at 90 ("CRC errors are detected and reported only while operating in Ultra mode."). In addition, unlike the MultiWord DMA modes, each Ultra DMA mode utilizes both the rising and falling edge of the clock signal to transfer data and utilizes HDMARDY, DDMARDY, and DSTROBE signals,

which are not party of a MultiWord DMA access operation. Ex. 1002 at ¶229; Ex. 1003 at 68, Fig. 32 (illustrating the MultiWord DMA transfer initialization process).

Furthermore, each Ultra DMA mode is different. As an example, after a pause in an Ultra DMA data burst, a memory device will be prepared to receive up to two additional data words for Ultra DMA Modes 0-2 and up to three additional data word for DMA Modes 3-5. *Id.* at 70. Finally, each mode is associated with different maximum transfer rates. *Id.* at 67, 72; Tables 21-22; Ex. 1002 at ¶232.

Each MultiWord and Ultra DMA mode is effective for determining access configuration for the usage. Specifically, the controller configures the CompactFlash device for an access operation according to the host-selected DMA mode. *Cf.* Ex. 1003 at 68, Fig. 32 with *id.* at 68, 83; Figs. 32, 38 (illustrating the difference in initialization process between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command (*i.e.,* at least one usage of the memory device) from the host. Ex. 1003 at 68. Similarly, enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ

DMA or WRITE DMA command (*i.e.,* usage) from the host. Ex. 1003 at 68; Ex. 1002 at ¶¶227-229.

These DMA modes are access profiles because use of each DMA Mode requires the use of a specific DMA *protocol*, not merely the selection of particular timing characteristics. Ex. 1003 at 68 ("[T]he *Ultra DMA protocol* shall be used instead of the *Multiword DMA protocol.*… This protocol applies to the Ultra DMA data burst only."). *See* Ex. 1011 at 266-67. Moreover, in the example of Ultra DMA, "[s]everal signal lines are redefined to provide different functions during an Ultra DMA burst." *Id.* at 68.

Furthermore, the selected DMA mode dictates the specific DMA protocol that the memory device utilizes. And the selection of an Ultra DMA profile rather than a MultiWord DMA profile requires the device to perform a CRC comparison to ensure the accuracy of the data transferred. Ex. 1003 at 90 ("CRC errors are detected and reported ***only while operating in an Ultra mode***.") (emphasis supplied); Ex. 1002 at ¶228.

The CompactFlash device further includes a "controller and flash memory module(s)." Ex. 1003 at 19. *CompactFlash* has a CompactFlash controller, which receives a SET FEATURES command from the host. The SET FEATURES command is communicated from the host to the CompactFlash controller to select one of the MultiWord or Ultra DMA modes. *Id.* at 15, 156-57. The SET

FEATURES command instructs the controller to set the DMA mode to the selected MultiWord DMA mode or Ultra DMA mode for subsequent DMA access operations (*i.e.*, the usage), such as READ DMA and WRITE DMA. *Id.* at 15, 157-58.

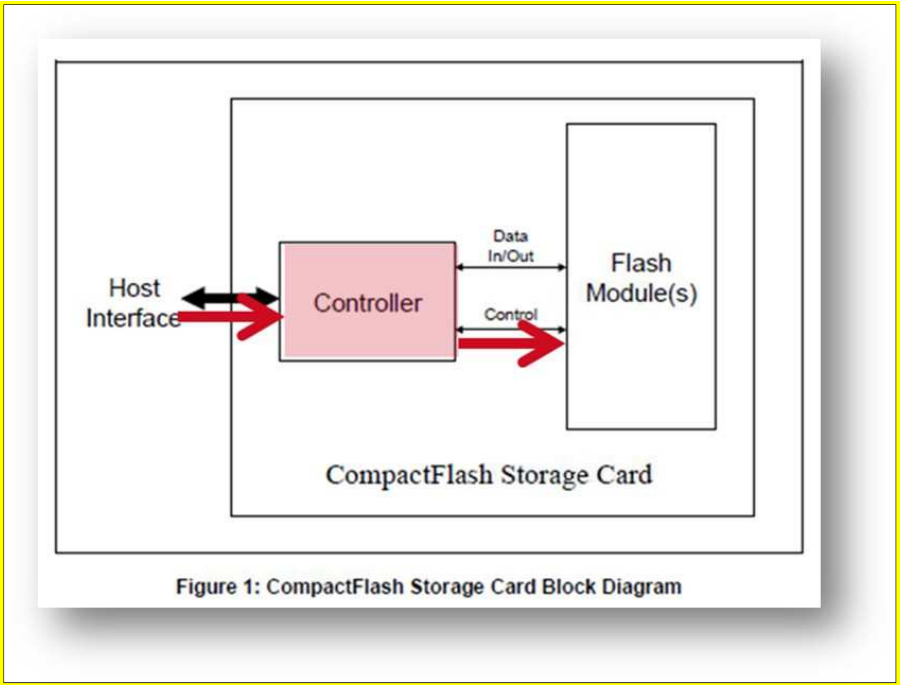


Figure 1: CompactFlash Storage Card Block Diagram

Id. at 19, Fig. 1 (annotated).

The SET FEATURES command sent from the host activates a selected MultiWord DMA mode or Ultra DMA mode (*i.e.*, a predefined access profile) from among the available modes supported by the device. *Id.* at 158, Table 53

(indicating bits representing a host-selected DMA mode) (shown below).

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at 158, Table 53 (annotated).

For example, for Ultra DMA modes, the Set transfer mode subcommand (using the transfer mode values in Table 53) in the SET FEATURES command allows "a host to select the Ultra DMA mode at which the system operates." *Id.* at 69. Thus, CompactFlash discloses this element. Ex. 1002 at ¶¶226-232.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device,

As discussed above, *CompactFlash* discloses that each MultiWord and Ultra DMA mode (*i.e.*, predefined access profile) is effective for determining how access to the memory device is configured for a usage. *See supra* Section IX.A.1(ii).

The "usage" in *CompactFlash* relates to the host activity in accordance with the selected DMA mode (*e.g.*, a READ DMA or WRITE DMA operation). *Id.* at

68. Specifically, the controller configures the CompactFlash device for a host-initiated access operation according to the host-selected DMA mode. *Cf.* Ex. 1003 at Fig. 32 *with id.* at Figs. 32, 38 (illustrating the difference in initialization process between a MultiWord DMA transfer and an Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id.* at 68. Similarly, enabling a MultiWord DMA mode causes the controller to initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when receiving a READ DMA or WRITE DMA command from the host. *Id.* at 68.

Thus, *CompactFlash* discloses this element. Ex. 1002 at ¶¶233-234.

iv. wherein: at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

As discussed above, *CompactFlash* discloses the memory device and at least a method for improvements to direct memory access (DMA) data transfer, including a plurality of predefined access modes (each DMA mode). *See supra* Section IX.A.1(ii)-(iii).

Toombs teaches two fundamental types of data transfer—sequential data transfer (sequential mode of access) and block-oriented data transfer (random mode of access). Ex. 1006 at 8:32-34. ("[T]wo types of data transfer commands

are defined: Sequential commands, and Block-oriented commands."). The sequential data transfer commands initiate a sequential, "continuous data stream[.]" Ex. 1006 at 8:35-37, Figs. 5, 7. During a sequential data transfer, the host reads or writes continuous data stream, only to be terminated by a stop command. Ex. 1006 at 8:35-39. On the other hand, a single block transfer initiates a transfer of a single block of memory. Ex. 1006 at 22:6-10.

A POSITA would understand that the read and write commands associated with the access profiles in *CompactFlash* (*see* claim element (iii), above) may also include the single-block read and write commands disclosed by *Toombs.* Ex. 1002 at ¶¶238-40.

A POSITA would further understand that the single-block read or write commands in *Toombs* correspond to a random mode of access. Ex. 1002 at ¶¶239-240. The memory device transfers/stores the data in sequential (*i.e.*, contiguous) memory blocks during a sequential read or write command. Ex. 1006 at 8:35-37. This allows the memory device to access the sequential memory using a data sequence. During a single-block read or write command, the memory device transfers/stores the data in a single block of memory. Ex. 1006 at 22:6-10. Upon receiving a following single block-write read or write command, the memory device may then transfer/store the data from a block that is not contiguous to (*i.e.*, random to) the previously-used memory block. Ex. 1002 at ¶239. Moreover,

unlike a sequential read or write command, the single block read or write command permits access to data without needing to proceed sequentially. Ex. 1002 at ¶239. The single block read or write command, instead, is able to access data directly. *Id*.

A POSITA would readily understand that using a block-oriented read and write command (*i.e*., random mode of access) is a fundamental way and highly desirable design choice to pass along data to or from the memory in *CompactFlash*, which discloses a plurality of predefined access profiles, as discussed above. Ex. 1002 at ¶240.

A POSITA would be motivated to combine CompactFlash with Toombs to arrive at this claim limitation. Ex. 1002 at ¶¶217-223. For instance, *CompactFlash* discloses read and write operations performed under well-established protocols. Ex. 1002 at ¶218. Two standard transfer techniques to perform reading and writing operations are sequential read/write operations and block-oriented (i.e., random mode of access) read/write operations. *Id*.; Ex. 1006 at 8:34-34 ("[T]wo types of data transfer commands are defined: Sequential commands, and Block-oriented commands."). Advantageously, block-oriented access (*i.e*., random access) ensures the successful transfer of data by using CRC comparisons. Ex. 1002 at ¶218; Ex. 1006 at 8:44-45. Accordingly, a POSITA would have looked to a basic transfer technique, like block-oriented read and write

operations, as disclosed in *Toombs*, in order to perform the read/write operations expressed in *CompactFlash.* Ex. 1002 at ¶218.

A POSITA would have been further motivated to combine the teachings of *CompactFlash* with *Toombs* because *CompactFlash* and *Toombs* deal with the similar field of technology and a similar time frame. Ex. 1002 at ¶219.

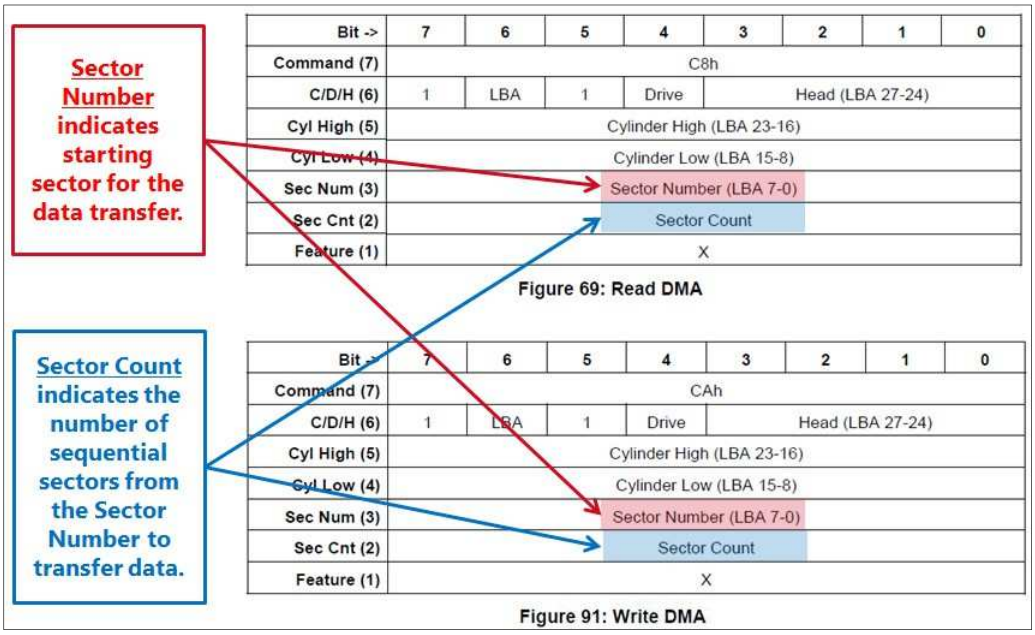
Furthermore, as described in *CompactFlash*, protocols control the read and write operations to the memory device. Ex. 1002 at ¶220; Ex. 1003 at 71, Figs. 32, 33, and 38. Two standard transfer techniques to perform reading and writing operations are sequential operations and block-oriented (*i.e.* random mode) operations. Ex. 1002 at ¶220; Ex. 1006 at 8:34-34 ("[T]wo types of data transfer commands are defined: Sequential commands, and Block- oriented commands."). Thus, the application of the known technique of block read/write operations (*i.e*., random mode of access) that apply to flash memory devices, as disclosed in *Toombs*, can also improve the flash memory device disclosed in *CompactFlash.* Ex. 1002 at ¶221. Predictably, combining the block read operations and write operations (*i.e*., random mode of access) in *Toombs* would result in a memory device that can perform single block read operations and write operations on the memory device in *CompactFlash*, leading to greater efficacy of communication (as Toombs' random access modes allow for CRC checks, as explained above). *Id*.

The resulting memory device disclosed in the *CompactFlash-Toombs* combination that performs sequential read/write operations, or block-oriented read/write operations (as disclosed in *Toombs*), to the memory device would have been predictable to one of ordinary skill in the art. *Id.* at ¶222. Moreover, the combination of the block read and write commands in *Toombs* with the simple read and write commands in *CompactFlash* would be highly desirable as the block-oriented read and write commands ensure the accuracy of the data transferred. Ex. 1002 at ¶222; Ex. 1006 at 9:12-16 (stating that, unlike a sequential transfer, the block-oriented data transfer performs a CRC checksum after transfer).

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

CompactFlash discloses a READ DMA and WRITE DMA command under one of the MultiWord or Ultra DMA modes (*i.e.*, a predefined access profile) that corresponds to a sequential mode of access. Ex. 1003 at 145 ("[The Read DMA] command uses DMA mode ***to read from 1 to 256 sectors as specified in the Sector Count*** register.... ***The transfer begins at the sector specified in the Sector Number*** Register"), 164 ("[The Write DMA] command uses DMA mode ***to write from 1 to 256 sectors as specified in the Sector Count*** register.... ***The transfer begins at the sector specified in the Sector Number*** Register."). The CompactFlash device performs read and write access operations by accessing the starting place of the

transfer in the memory (*i.e.,* the Sector Number) and continuing for a number of sequential sectors (*i.e.,* the Sector Count). *Id.* at 145, 164; Ex. 1002 at ¶¶241-250.



Ex. 1003 at Figs. 69, 91 (annotated).

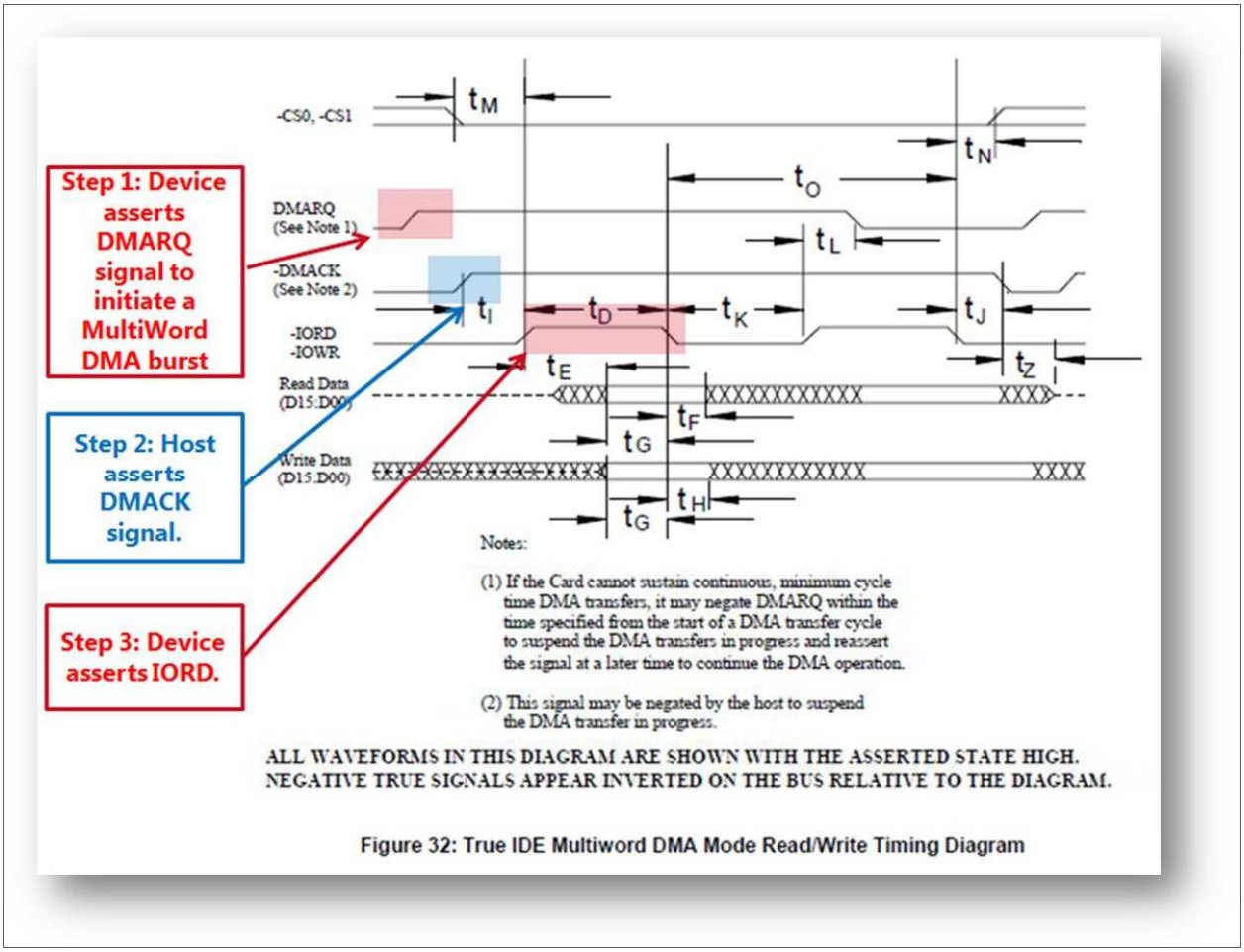
Accordingly, READ and WRITE DMA operations correspond to a sequential mode of access. *See id.* at 145; Ex. 1002 at ¶250. Both start at a specified Sector Number and continue to access (*i.e.,* read or write) in sequence the number sectors indicated in the Sector Count. Ex. 1003 at 145, 164; Ex. 1002 at ¶¶241-250.

vi. configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.

The CompactFlash controller configures the access to the memory device according to the selected DMA mode (*i.e.*, one of the MultiWord or Ultra DMA modes), so that the CompactFlash device is effective to perform a DMA access operation (*i.e.*, usage) using the selected DMA mode.

After a host communicates a READ DMA or WRITE DMA command following the selection of a DMA mode, the controller will begin the DMA-specific initiation protocol to configure access to the memory device for either a MultiWord DMA transfer or an Ultra DMA transfer in the selected mode.
Ex. 1003 at 68, 76, 83; Figs. 32-33, 38.

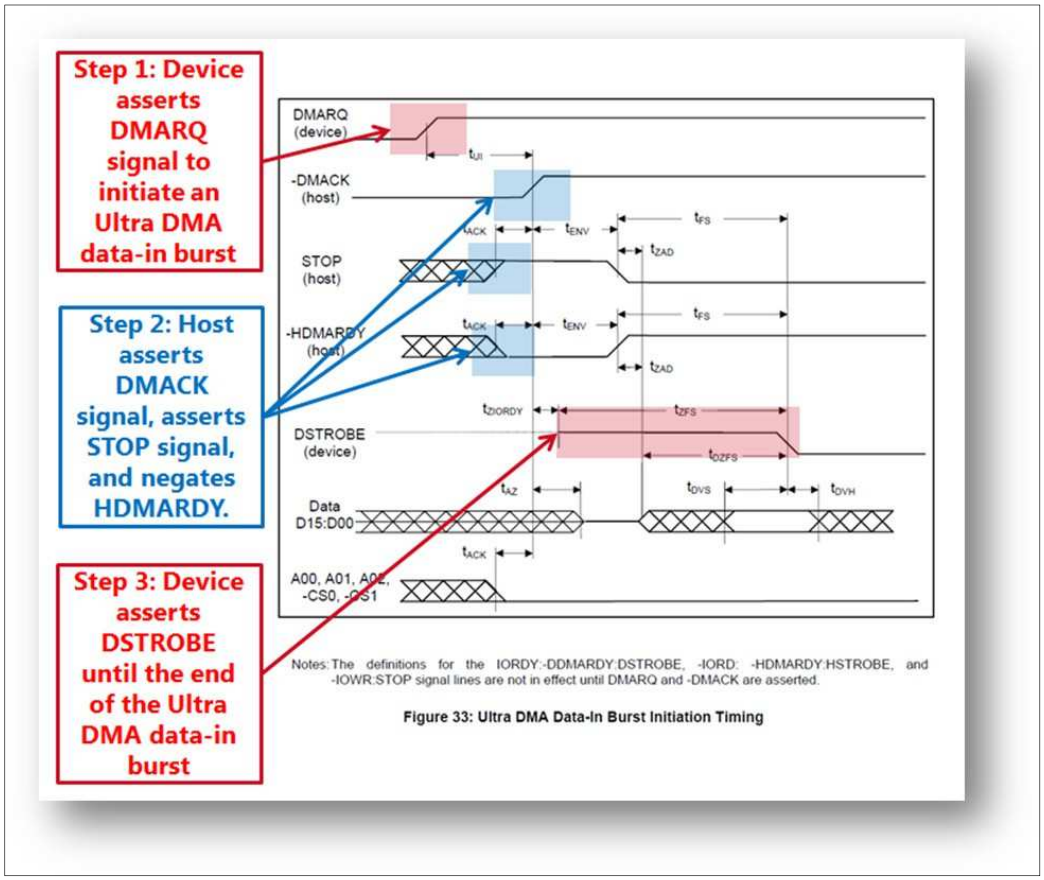
For example, in a MultiWord DMA mode, the controller starts the initiation phase of the MultiWord DMA burst by asserting a DMARQ signal (Step 1 of Fig. 32). The host, in response, asserts a DMACK signal (Step 2 of Fig. 32), and, in turn, the controller response by asserting the IORD signal (Step 3 of Fig. 32).



Id. at 68, Fig. 32 (annotated).

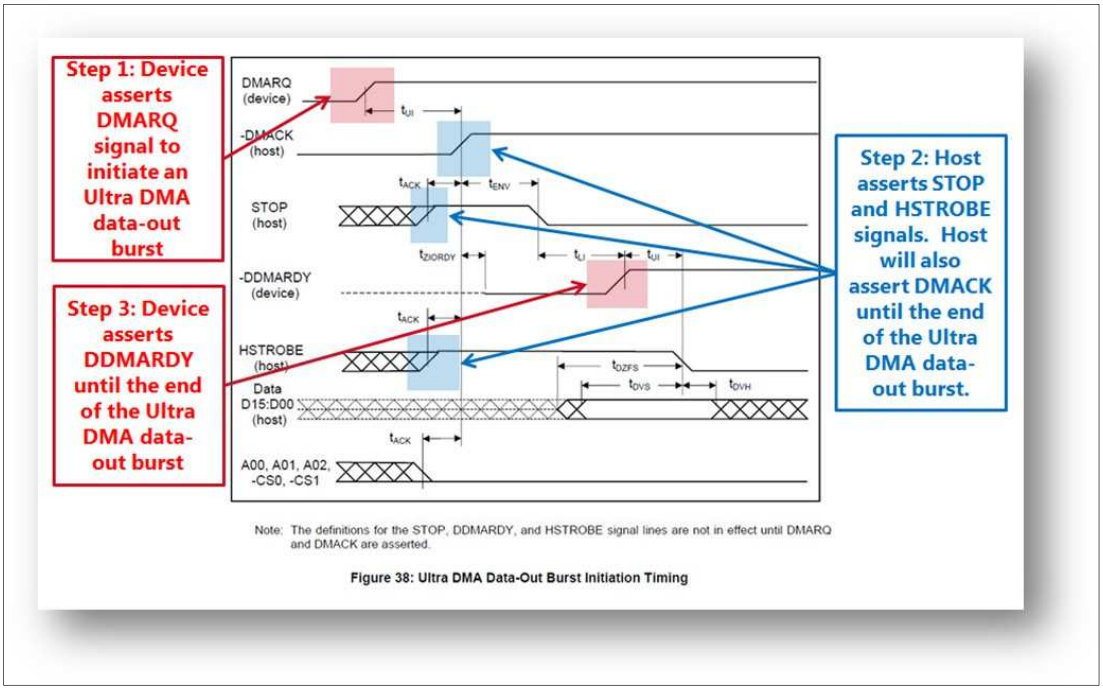
As another example, when an Ultra DMA mode is activated, the controller starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal (Step 1 of Fig. 33). Ex. 1003 at 76. The host then asserts a DMACK signal (Step 2 of Fig. 33). *Id.* at Fig. 33. Only at that point do the other signal lines become effective, permitting the transfer. *Id.* ("The definitions for the …DSTROBE… and - IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are

asserted). The device will assert a DSTROBE signal line to start the data-in burst (Step 3 of Fig. 33). *Id.* at 76, Fig. 33.



Id. At 76, Fig. 33 (annotated).

For a data-out burst, the device will wait to negate any signal until generating a STROBE edge (*see* Step 3 of Fig. 38). *Id.* at 70. At this point, the memory device is now configured for usage (*i.e.*, to perform a data transfer under the selected Ultra DMA mode).



Id. at 83, Fig. 38 (annotated). CompactFlash thus discloses this element. Ex. 1002 at ¶¶252-253.

2. Dependent Claim 10

i. The method of claim 8, wherein the at least one predefined access profile comprises a default access profile.

When executing a power-on or hardware reset, *CompactFlash* discloses that the device may revert to a default non-Ultra DMA mode, like a MultiWord DMA mode. Ex. 1003 at 69. As discussed above, each MultiWord DMA mode may be an access profile. Ex. 1002 at ¶254; *see supra* IX.A.1(ii).

3. Dependent Claim 14

i. The method of claim 8, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

In *CompactFlash*, the various DMA profiles correspond to and support READ DMA (*i.e.*, a read operation) and WRITE DMA (i.e., a write operation). Ex. 1003 at 145, 164.

4. Independent Claim 15

i. (Preamble) A memory device comprising:

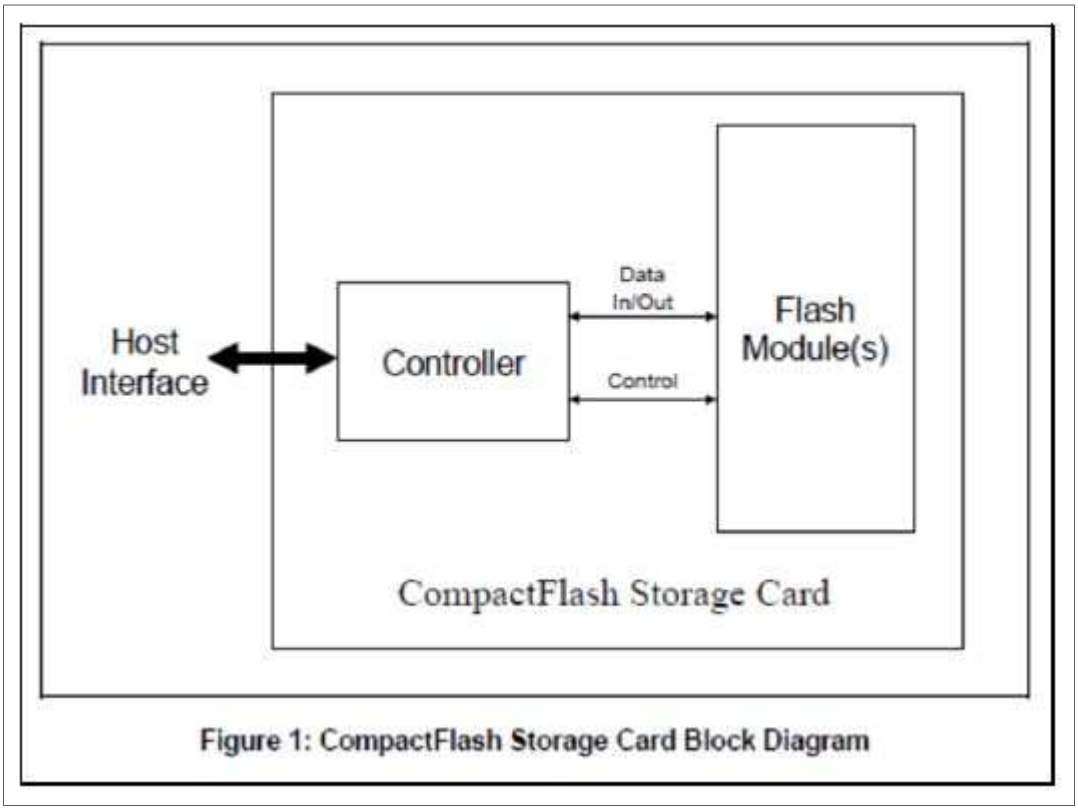
See Section above at IX.A.1.(i).

ii. means for receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with the memory device,[2]

As explained above in Section IX.A.1.(ii), *CompactFlash* discloses this function. Further, as explained above in Section IX.A.1.(ii), *CompactFlash* discloses that this functionality is carried out by a "controller" that communicates both control signals and data signals to the flash memory through an interface and

[2] Petitioner and Patent Owner agreed that this phrase is a means-plus-function limitation, with the function being, "receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with the memory device," and the structure being "controller 508, communication interface 512, and interface 506 of Figure 5, 4:38-55; and structural equivalents thereof." Ex. 1025 at 4.

that communicates to the host through a "host interface." This is shown, for example, in Fig. 1



Ex. 1003 at 19, Fig. 1.

The CompactFlash device receives a READ DMA or WRITE DMA command at the "controller" (*i.e.*, the controller 508 as disclosed in the '486 Patent) through the "host interface" (*i.e.*, the interface 512 as disclosed in the '486 Patent) that causes the CompactFlash device to invoke a protocol for the subsequent data either read from or written to the CompactFlash memory (*i.e.*, the protocol for transmissions to the flash memory in CompactFlash corresponding to the interface 506 in the '486 Patent). Ex. 1002 at ¶262.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device, wherein:

See Section above at IX.A.1.(iii).

iv. at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

See Section above at IX.A.1.(iv).

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

See Section above at IX.A.1.(v).

vi. means for configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.[3]

As explained above in Section IX.A.1.(vi), *CompactFlash* discloses this function. Further, as explained above in Section IX.A.1.(vi), *CompactFlash* discloses that this functionality is carried out by a "controller," which corresponds to the controller 508 of the '486 Patent, as explained in Section IX.A.4.(ii).

[3] Petitioner and Patent Owner agreed that this phrase is a means-plus-function limitation, with the function being, "configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile," and the structure being "controller 508 of Figure 5, 4:38-55; and structural equivalents thereof." Ex. 1025 at 4.

5. Dependent Claim 17

i. The memory device of claim 15, wherein the at least one predefined access profile comprises a default access profile.

CompactFlash discloses the method of Claim 15, as disclosed above in Section IX.A.4. When executing a power-on or hardware reset, *CompactFlash* discloses that the device may revert to a default non-Ultra DMA mode, like a MultiWord DMA mode. Ex. 1003 at 69. As discussed above, each MultiWord DMA mode may be an access profile. Ex. 1002 at ¶268; *see supra* Section IX.A.1(ii).

6. Dependent Claim 21

ii. The memory device of claim 15, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

In *CompactFlash*, the various DMA profiles correspond to and support READ DMA (*i.e*., a read operation) and WRITE DMA (*i.e*., a write operation). Ex. 1003 at 145, 164.

B. GROUND 2: CLAIMS 8, 14, 15, AND 21 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) OVER ZIV, VOGT, AND TOOMBS

As shown below, *Ziv, Vogt,* and *Toombs* render obvious Claims 8, 14, 15, and 21 of the ’486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶272-335.

1. Independent Claim 8

i. (Preamble) A method comprising:

Ziv discloses a memory device, such as a portable storage device that includes a storage memory. Ex. 1004 at 3:48-55, Fig. 2.

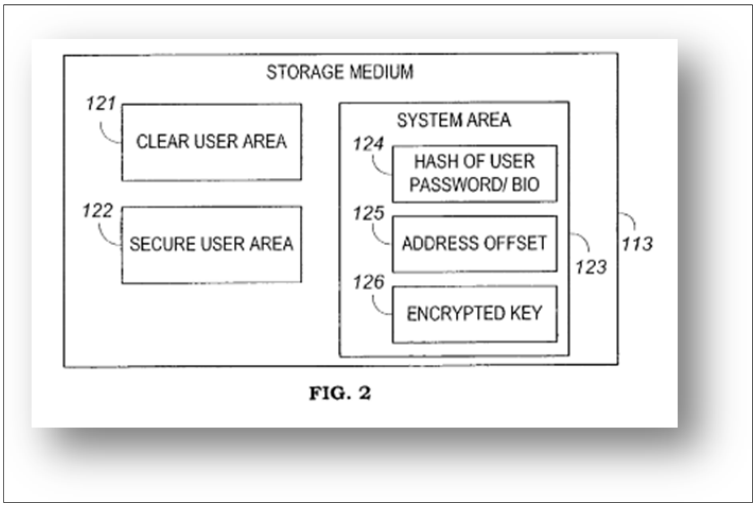


FIG. 2

Id. at Fig. 2.

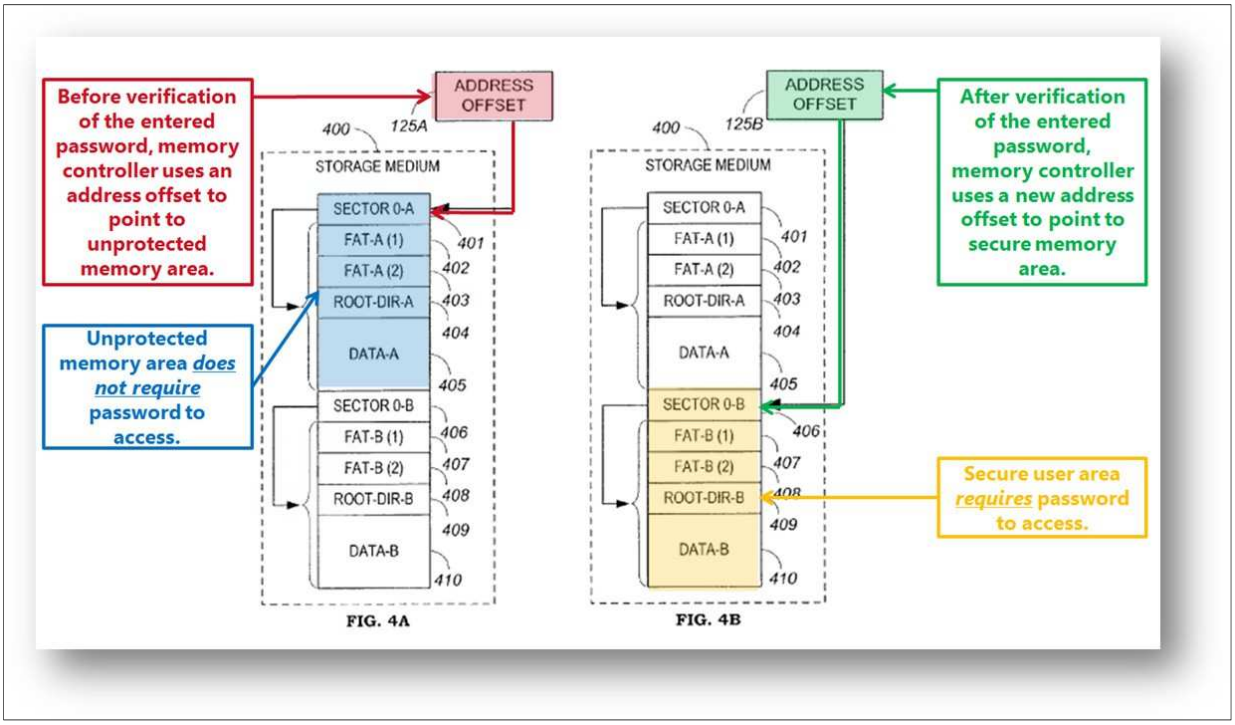
Furthermore, Ziv discloses at least a method for securing data on a portable storage device. Ex. 1004, *Title* and *Abstract*.

ii. receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with a memory device,

The password hash, address offset, and key in *Ziv* each constitute a predefined access profile that governs the access operations to the memory. *See* Ex. 1001 at 3:56-58 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory***

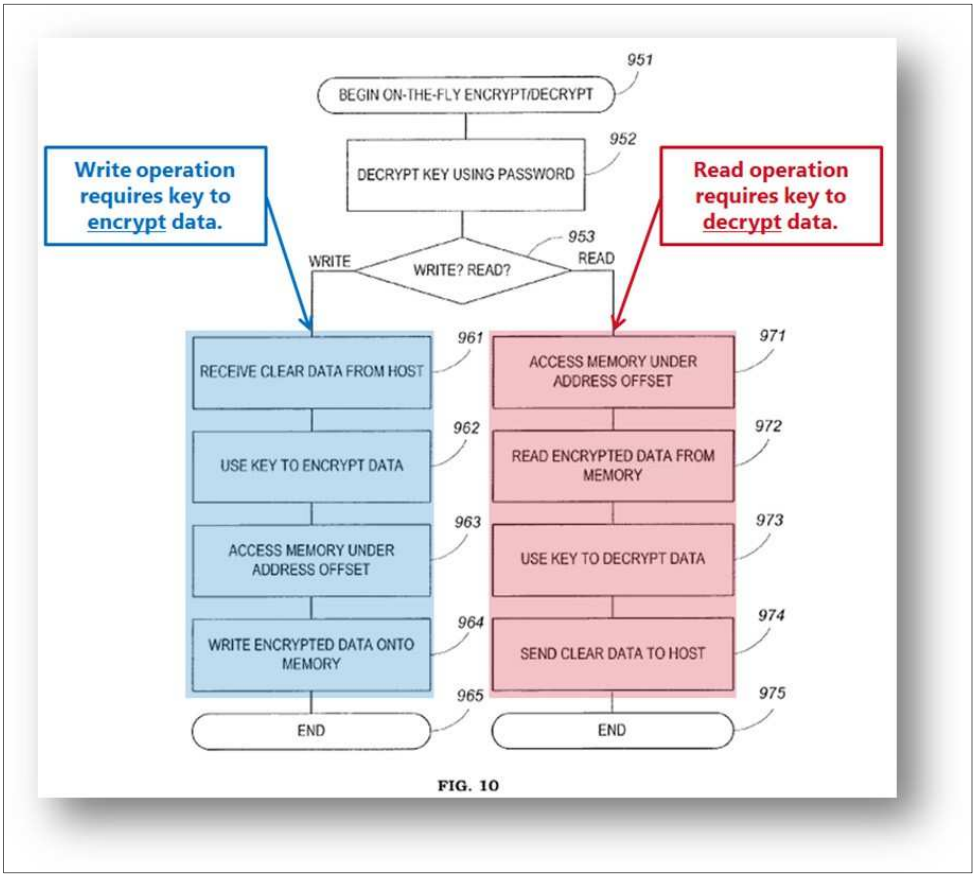
device.") (emphasis supplied). Additionally, each of these components forms an access profile. Ex. 1002 at ¶¶290-293.

Access to the secure user data is only available when a hash of an entered password matches the password hash stored in the register. Ex. 1004 at 4:11-12 ("[A] secure area 122 that contains secure user data [is] accessible only upon the provision of a password[.]"). In addition, the address offset governs access operations to the memory. After entering the proper password, the memory device uses the stored address offset to properly view the secure memory area. Ex. 1004 at 6:46-48 ("[H]ost 101 will seek 'sector 0' of the remounted device, controller 111 will use offset 125B to point at 'sector 0-B' 406[.]"). Without the address offset, the secure area will not be properly mounted. *Id.*; Ex. 1002 at ¶291.



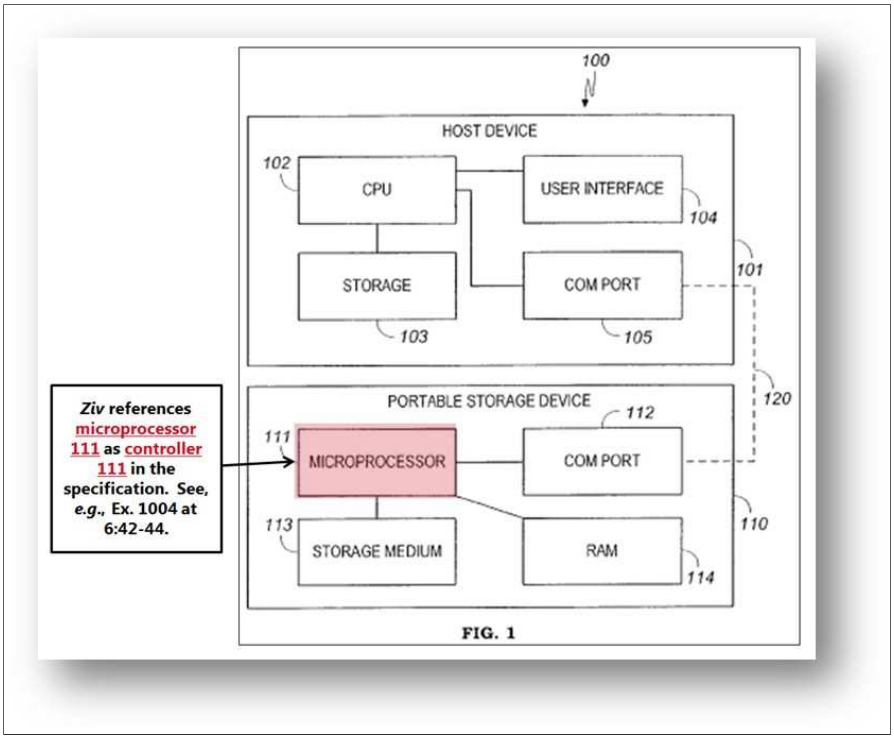
Ex. 1004 at Fig. 4A-4B (illustrating the use of the address offset to access the secure area) (annotated).

Moreover, the key governs the access operations to the memory. The key is the "permanent encryption key for all data stored in the secure memory." *Id.* at 7:7-9. Without the key, a user cannot read or write to the secure area. *Id.* at 7:7-9, 7:36- 46 (instructing the controller to decrypt data being read from and encrypt data being read to the secure memory area using the key), Fig. 10 (shown below); Ex. 1002 at ¶292.



Ex. 1004 at Fig. 10 (annotated).

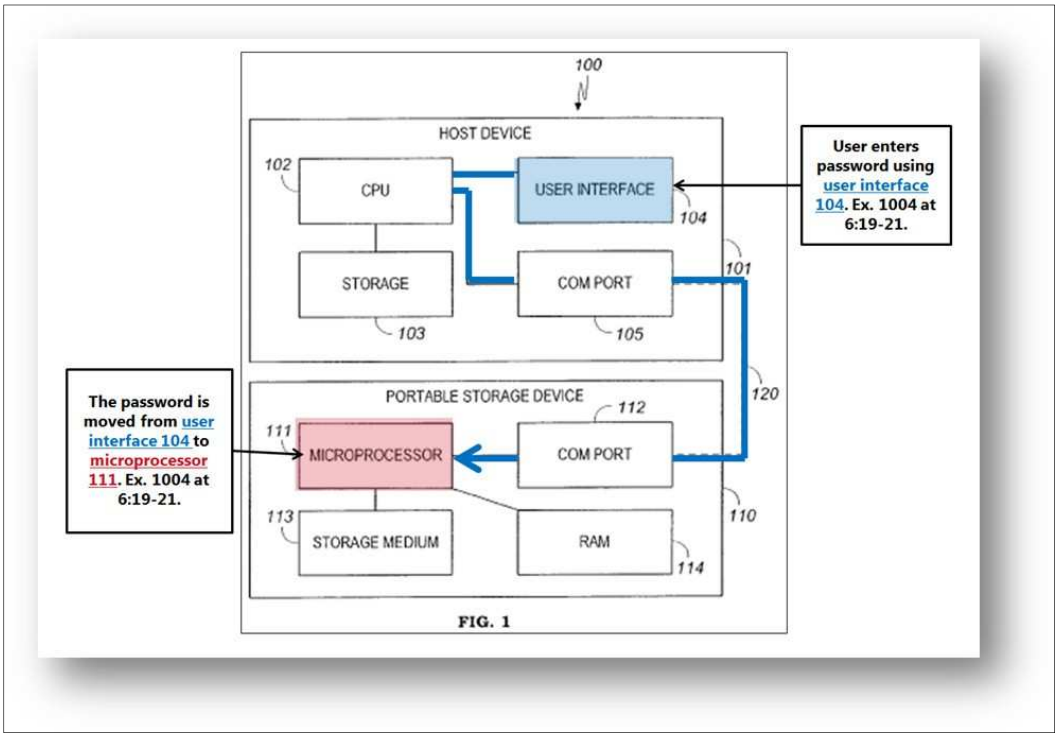
Furthermore, *Ziv* discloses a controller (microprocessor) in the memory device that receives a command indicating the password entered to gain access the secure area. Ex. 1004 at 6:42-44 ("***[C]ontroller 111*** dismounts and remounts portable storage device 110[.]") (emphasis supplied). A POSITA would understand the microprocessor to be a controller. Ex. 1002 at ¶296.



Ex. 1004 at Fig. 1 (annotated).

The controller receives a command indicating the password entered. *Id.* at 6:19-30 ("If the password has been entered ... via user interface 104, then in step 702 this password is moved to microprocessor 111.... [T]he hashed entered password is then compared to the hashed stored password in register 124."), Fig. 1 (below). In other words, the host system instructs (*i.e.,* sends a command to) the

controller (microprocessor) to use the entered password to gain access to the secure memory area (*i.e.*, the usage). Ex. 1002 at ¶297.



Ex. 1004 at Fig. 1 (annotated).

Additionally, the password in *Ziv* activates the decryption of the stored key. Ex. 1002 at ¶304. When the entered password matches the stored password, the microprocessor decrypts the key of the predefined access profile. Ex. 1004 at 7:32-35.

The communication of a proper password also activates the remounting of the memory according to the address offset. Ex. 1002 at ¶305. After remounting, the stored address offset is used to point to the secure memory area. Ex. 1004 at

6:44-46 ("[W]hen remounting device 110, controller 111 will use an address offset[.]").

To the extent that Board disagrees that an instruction to use the entered password to gain access to the secure memory area in *Ziv* teaches the claimed "command," it would have been obvious nevertheless to use the command-based password authentication method in *Vogt* in the memory device of *Ziv*. In particular, *Vogt* discloses a "password verify" command that communicates the entered password to the flash device, like a MMC card. Ex. 1005 at 6:36-38 ("The OS sends a 'password verify' command to the flash. ***The command*** ... ***includes the entered password***.") (emphasis supplied). The "password verify" command instructs the internal processor to "compare[] the entered password with the stored password value." Ex. 1005 at 6:30-32.

It would have been obvious to combine the teachings of *Ziv* and *Vogt* to form a memory controller that receives the "password verify" command in *Vogt* for the following reasons.

Simple Substitution of One Known Element for Another

Commands, especially commands communicating a password, were well-known in the art to be a fundamental approach to communicating information between devices. Ex. 1002 at ¶276; Ex. 1005 at 6:36-38. A POSITA could have substituted one known element (a controller receiving a password) for the other (a

controller receiving a command containing the password) and the results would have been predictable (a controller receiving a command containing the password). Ex. 1002 at ¶¶273-275.

Moreover, those predictable results would have included the known advantages of *Ziv*'s memory device, which provides access to a secure memory area, and the known advantages of a command, which include reliably and efficiently communicating a password from the host system to memory device. Ex. 1004 at 6:19-23; Ex. 1005 at 3:23-24; Ex. 1002 at ¶276.

Analogous Art

A POSITA would have been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Vogt* and *Ziv.* Ex. 1002 at ¶277. Both patents concern securing data using non-volatile memory in the early 2000s. Ex. 1004 at 3:48-55; Ex. 1005 at 1:13-15. In addition, both patents describe a solution to a similar problem–improving security of portable flash drives using a secure memory and password. Ex. 1004 at 1:60-63 ("[A] portable storage device for securing data stored in the device in a way that will be both convenient and secure."); Ex. 1005 at 2:5-12 ("Techniques for implementing hidden storage in a non-volatile memory storage," where "[t]he hidden storage area cannot be accessed without a valid password.").

Known Technique to a Known Device to Yield Predictable Results

Base system: *Ziv* discloses a memory device, such as a SecureDigital or CompactFlash device, that receives an entered password from the host system. Ex. 1004 at 6:19-30; Ex. 1002 at ¶281.

Known technique: As shown by *Vogt*, receiving a command containing a password was well-known. Ex. 1005 at 6:36-38.

Predictable results and improved system: A POSITA would have recognized that implementing *Vogt*'s structured communication protocol of the "password verify command" in *Ziv*'s memory device would yield the predictable result of a memory device that receives an entered password through a structured command, like the password verify command. Ex. 1002 at ¶282.

As such, using *Vogt*'s password-command implementation of communicating a password was an obvious design choice to implement *Ziv*'s teaching of communicating a password. *Id.* at ¶282.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device,

The "at least one usage," in the context of *Ziv*, is the host's access to the secure memory area. *See* Ex. 1004 at 1:60-63.

As explained with respect to the previous claim element, the password hash, address, and key in *Ziv* are all effective for determining how access to the memory

device is configured, as each is necessary to view, read from, or write to the secure memory area. Ex. 1002 at ¶¶307-309.

iv. wherein: at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

The read/write commands to the secure area using the hashed password, address offset, and key (*i.e.*, predefined access profile) correspond to a random or sequential mode of access. Random mode of access and sequential mode of access are the only two types of access methods for reading from and/or writing to memory. Ex. 1002 at ¶310.

Toombs teaches these two fundamental types of data transfer: sequential data transfer (sequential mode of access) and block-oriented data transfer (random mode of access). Ex. 1002 at ¶311; Ex. 1006 at 8:34-34 ("[T]wo types of data transfer commands are defined: Sequential commands, and Block-oriented commands."). The sequential data transfer commands initiate a "continuous data stream[.]" Ex. 1006 at 8:35-37. A single block-oriented transfer initiates a single block transfer. *Id.* at 22:6-10.

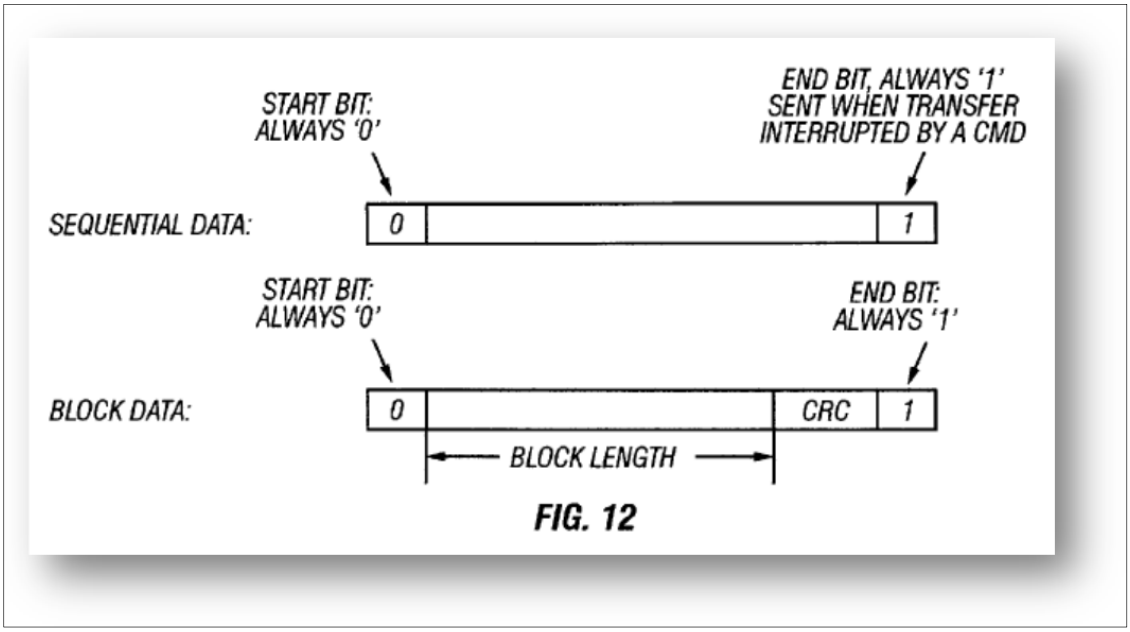


FIG. 12

Id. at Fig. 12 (illustrating the difference between sequential data and block data).

A POSITA would understand that the read/write commands associated with the access profile in *Ziv* may also include the sequential read/write commands or block read/write commands (*i.e.*, random access) disclosed by *Toombs*. Ex. 1002 at ¶¶312-314. It would have been obvious to include the random access read and write command as taught by *Toombs* in the combined *Ziv*-*Vogt* memory device:

Explicit Teaching to Combine

As described in *Ziv*, the read and write operations perform under well-established standards. Ex. 1004 at 1:23-25 ("[T]he computer controls all read/write operations under well-established standards."). Sequential and single block read operations and sequential write operations are basic transfer techniques to perform reading and writing operations. Ex. 1006 at 8:34-34. Accordingly, a POSITA

would have looked for a basic transfer technique, like the sequential or single block read and write operations of *Toombs*, to perform the read/write operations of *Ziv.* Moreover, the sequential operations of *Toombs* were known to be advantageous as they reduce addressing overhead and improve efficiency during sequential access. *See id.* at 8:39-43 ("This [sequential data transfer] mode reduces the command overhead to an absolute minimum[.]"); Ex. 1002 at ¶279. Block-oriented commands (*i.e.*, random access) were also advantageous as they ensured a successful data transfer. Ex. 1006 at 8:44-45.

A POSITA would have further been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Toombs* to *Ziv* and *Vogt.* Ex. 1002 at ¶¶272-287. All three patents center on accessing flash memory. Ex. 1004 at 4:4-9; Ex. 1005 at 2:19-20; Ex. 1006 at 1:30-33; Ex. 1002 at ¶280.

Use of Known Technique to Improve Similar Devices in the Same Way

As described in *Ziv*, "well-established standards" control the read and write operation to the secure memory area. Ex. 1004 at 1:23-25. As taught in *Toombs*, sequential and single-block read/write operations were known standard techniques for reading and writing operations. Ex. 1006 at 8:34-34.

It was within the level of skill in the art to apply the technique of sequential and single-block read and write commands in *Toombs* with the read and write command in the memory device described in *Ziv.* M.P.E.P. 2143(I)(B); Ex. 1002

at ¶¶284-287. Predictably, the *Ziv-Vogt* memory device would efficiently perform sequential read and write operations, or single-block read and write operations (*i.e.*, random access), to read from or write to the secure memory area. *Id.* at ¶¶284-287.

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

See Section above at IX.B.1.(iv).

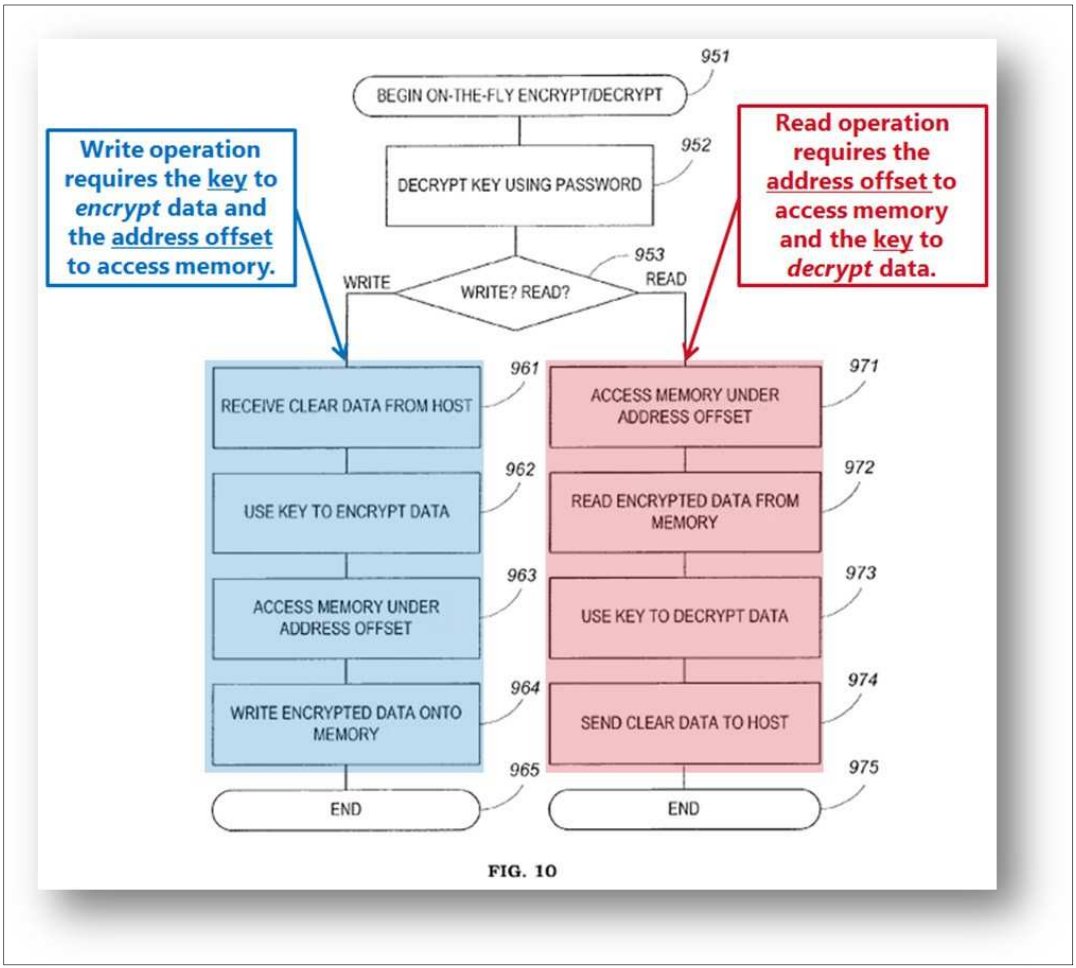
vi. configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.

The controller in *Ziv* configures access to the secure memory area in accordance with the password hash, address offset, and key (*i.e.*, predefined access profile), so that the memory device is effective for the host to view, read from, or write to the secure memory area (*i.e.*, the usage). Ex. 1002 at ¶¶320-322.

The secure memory area is only accessible when the microprocessor uses the stored address offset to point to the proper memory sector, which it does after the user enters the correct password. Ex. 1004 at 6:45-52; Ex. 1002 at ¶321.

The microprocessor must also configure the access operations to perform on-the-fly encryption/decryption. Ex. 1002 at ¶322. When accessing the secure memory area, the microprocessor must apply the encryption key to properly read

from and/or write to the secure memory area. Ex. 1004 at 7:35-46, Fig. 10 (shown below); Ex. 1002 at ¶322.



Ex. 1004 at Fig. 10 (annotated).

2. Dependent Claim 14

i. The method of claim 8, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

The method of independent Claim 8 in view of *Ziv*, *Vogt*, and *Toombs* is addressed in Ground 2 above in Section IX.B.1.

The address offset and key in *Ziv* corresponds to at least read and write operations. Ex. 1002 at ¶323. The address offset allows the host to properly read from and write to the secure memory area by pointing the controller to the secure memory area. *See* Ex. 1004 at 6:46-49, Fig. 10 (noting address offset is used in on-the-fly encryption/decryption). In addition, because the key is required to properly read from and write to the secure memory area, the key also corresponds to reading and writing operations. *Id.* at 7:36-46.

3. Independent Claim 15

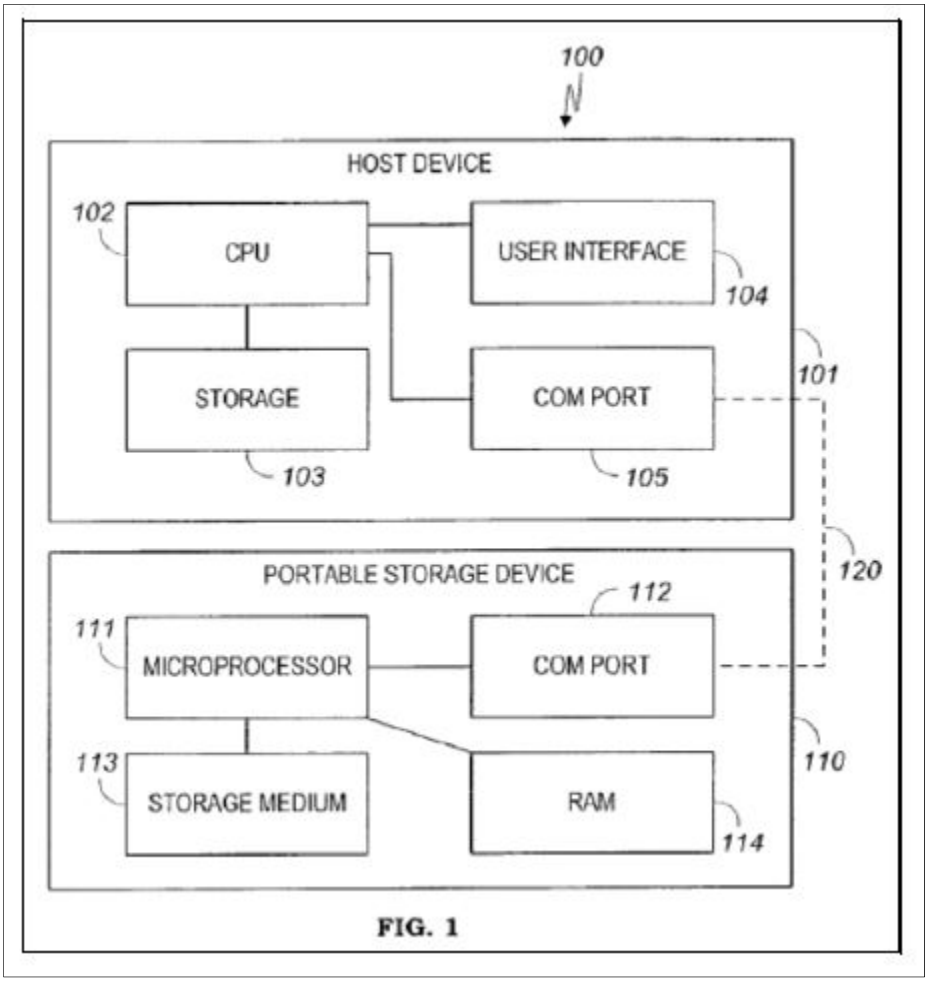
i. (Preamble) A memory device comprising:

See Section above at IX.B.1.(i).

ii. means for receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with the memory device,

As explained above in Section X.B.1.(ii), the *Ziv*-*Vogt* combination discloses this function. Further, as explained above in Section X.2.(ii), *Ziv* discloses that this functionality is carried out by a microprocessor that is a known and disclosed as a controller that communicates to the flash memory through an interface and that communicates to the host through a host interface. Ex. 1002 at ¶¶327-329.

Again, *Ziv* discusses the microcontroller as a controller. Ex. 1004 at 6:42-44 ("[C]ontroller 111 dismounts and remounts portable storage device 110[.]").



Ex. 1004 at Fig. 1.

As can be seen from Fig. 1 of *Ziv*, there is a "controller" (*i.e.*, the controller 508 as disclosed in the '486 Patent) that communications with the host through COM PORT 112 and interface 120 (*i.e.*, the interface 512 as disclosed in the '486 Patent) that causes the microprocessor to read from or write to the memory (*i.e.*, corresponding to the interface 506 in the '486 Patent). Ex. 1002 at ¶329.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device, wherein:

See Section above at IX.B.1.(iii).

iv. at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

See Section above at IX.B.1.(iv).

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

See Section above at IX.B.1.(v).

vi. means for configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.

As explained above in Section IX.B.1.(vi), the *Ziv-Vogt* combination discloses this function. Further, as explained above in Section IX.B.1.(vi), the Ziv-Vogt combination discloses that this functionality is carried out by a "controller," which corresponds to the controller 508 of the '486 Patent, as explained in Section IX.B.3.(ii).

4. Dependent Claim 21

i. The memory device of claim 15, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

See Section above at IX.B.2.(i)

C. GROUND 3: CLAIMS 8, 14, 15 AND 21 ARE UNPATENTABLE UNDER 35 U.S.C. 35 U.S.C. § 103(a) OVER SINCLAIR AND TOOMBS

As shown below, *Sinclair* and *Toombs* render obvious Claims 8, 14, 15, and 21 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶336-378.

1. Independent Claim 8

i. (Preamble) A method comprising:

Sinclair discloses at least a "method for managing space in a non-volatile memory." Ex. 1007 at Abstract, Claims 1-14.

ii. receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with a memory device,

Sinclair discloses a Reclaim Normal mode that is a predefined access profile associated with the memory device and is stored in a portion of the memory (*i.e.*, register). Ex. 1007 at 2:50-57, 10:20-22; *see* Ex. 1001 at 5:2-4 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis supplied). The Reclaim Normal mode is the default mode that governs the access operations to the memory

device. Ex. 1007 at 23:36-24:8. In this mode, the memory device calculates an optimal interleave ratio of reclaim operations to write commands such that a memory card will not run out of writeable memory until there is no reclaimable memory left. *Id.* at 2:50-57, Fig. 19.

The controller receives commands to select the appropriate reclaim mode. Ex. 1007 at 23:28-30 ("[T]he host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity"); Ex. 1002 at ¶¶350-351. The selection is related to at least one usage (*i.e.*, "expected host activity" including "idle"). Ex. 1007 at 23:27-30, 41-44.

Similarly, the host may also issue a "Reclaim_on" command or a "Reclaim_off" command to select other reclaim modes. *Id.* at 23:36-59. The controller performs continuous reclaim operations in Reclaim On mode and, conversely, prohibits reclaim operations in Reclaim Off mode. *Sinclair*, further, contemplates optional Maximum and Minimum Interleave modes that perform reclaim operations at a maximum or minimum interleave rate. *Id.* at 23:64-24:6. The Reclaim On, Maximum Interleave, Reclaim Normal, Minimum Interleave, and Reclaim Off mode each constitutes a predefined access profile. Ex. 1002 at ¶¶346-348. These various reclaim modes are selectable by the host based on the host's expected activity. Ex. 1007 at 23:25-29.

After receiving a reclaim mode command, such as the "Reclaim normal" command, the controller begins reclaiming memory as specified by the selected profile. Ex. 1007 at 23:27-30. For instance, in Reclaim Normal mode, reclaiming occurs "according to an adaptive schedule." *Id.* at 24:1-3.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device,

The host selects a predefined access profile, like Reclaim Normal mode, to optimally interrupt host write operations (*i.e.*, determine how access to the memory device is configured) based on an expected host activity (*i.e.*, usage). *Id.* at 23:28-30.

The selection of Reclaim Normal mode, for example, causes the memory controller to configure the device to optimally interleave memory access operations (*e.g.,* write/read) with reclaim operations. *Id.* at Abstract. ("A memory controller ... schedules the reclaim operations to be evenly distributed between write operations until the memory is full.").

Reclaim On mode and Reclaim Off mode similarly cause access configuration changes. In Reclaim On mode, the host sits "idle" by not sending additional commands as the memory device performs continuous reclaim operations. *Id.* at 23:38-44. In Reclaim Off mode, the memory device inhibits reclaim operations and only host operations are performed. *Id.* at 23:55-56.

iv. wherein: at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

During the Reclaim Normal mode, reclaim operations are interleaved with write operations. Ex. 1007 at 17:58-60. Moreover, these write operations can either be a sequential or random mode of access.

One method of reclaim operations is data compaction, which rearranges blocks into ***a non-sequential format,*** or randomly. *Id.* at 12:4-7; Ex. 1002 at ¶¶357-358. *Sinclair* teaches that the data may be "copied to a block where they are stored non-sequentially." *Id.* at 12:4-7.

Accordingly, the reclaim operation associated with the Reclaim Normal mode corresponds to a non-sequential, or random, mode of access as the controller can now access a randomly-arranged set of data. Ex. 1002 at ¶¶357-358.

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

During the Reclaim Normal mode, reclaim operations are interleaved with write operations. Ex. 1007 at 17:58-60. Moreover, these write operations can either be a sequential or random mode of access.

One method of reclaim operations is data compaction, which rearranges blocks into ***a sequential format.*** *Id.* at 12:28-30; Ex. 1002 at ¶¶359-360. *Sinclair* teaches the benefit of sequential access: "one advantage of sequentially storing

data is that it may not necessary to maintain an index of the locations of different sectors, thus reducing the overhead associated with maintaining such an index." Ex. 1007 at 12:51-54. Accordingly, the reclaim operation associated with the Reclaim Normal mode corresponds to a sequential mode of access as the controller can now access a sequentially-arranged set of data. Ex. 1002 at ¶¶360-361.

vi. configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.

The memory controller calculates an optimal interleave ratio of reclaim operations to write operations in Reclaim Normal mode. Ex. 1007 at 2:56-57. Once calculated, the memory controller configures access to the memory device according to the optimal interleave ratio. *Id.* at 18:46-49. The memory device will then interleave memory access operations, like write and reclaim operations. *Id.* at 18:46-49; Ex. 1002 at ¶362. This ensures write operations to the memory device are effective as long as reclaimable memory remains. Ex. 1007 at 18:17-26.

Similarly, the memory controller configures access to the device in Reclaim On mode and Reclaim Off mode. In Reclaim On mode, the host is "idle" while the memory device performs continuous reclaim operations. *Id.* at 23:38-44. In Reclaim Off mode, reclaim operations are inhibited and only host access operations are performed. *Id.* at 23:55-56.

2. Dependent Claim 14

i. The method of claim 8, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

Sinclair teaches that the Reclaim Normal mode corresponds to interleaving reclaim operations ***with host data write operations.*** Ex. 1007 at 24:1-3 (emphasis supplied).

3. Independent Claim 15

i. (Preamble) A memory device comprising:

See Section above at IX.C.1.(i).

ii. means for receiving one or more commands to activate at least one predefined access profile of two or more predefined access profiles associated with the memory device,

See Section above at IX.C.1.(ii).

As explained above in Section IX.C.1.(ii), *Sinclair* discloses this function. Further, as explained above in IX.C.1.(ii), *Sinclair* discloses that this functionality is carried out by a controller that communicates to the flash memory through an interface and that communicates to the host through a host interface.

Sinclair explicitly describes a memory device that includes a "memory controller" that receives commands from a host through a "host interface." Ex. 1007 at Fig. 1 (depicted below).

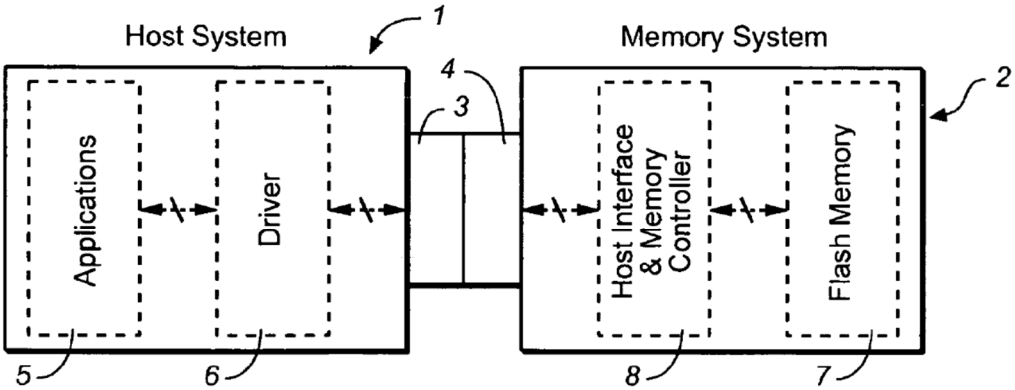


FIG. 1

As can be seen from Fig. 1 of Sinclair, there is a "controller" (*i.e.*, the controller 508 as disclosed in the '486 Patent) that communications with the host through a "host interface" (*i.e.*, the interface 512 as disclosed in the '486 Patent) that causes the controller to read from or write to the memory through the dashed arrow (*i.e.*, corresponding to the interface 506 in the '486 Patent). Ex. 1002 at ¶¶370-371.

iii. the two or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device, wherein:

See Section above at IX.C.1.(iii).

iv. at least a first predefined access profile of the two or more predefined access profiles corresponds to a random mode of access; and

See Section above at IX.C.1.(iv).

v. at least a second predefined access profile of the two or more predefined access profiles corresponds to a sequential mode of access; and

See Section above at IX.C.1.(v).

vi. means for configuring, based at least in part on the one or more commands, access to the memory device in accordance with the at least one predefined access profile such that at least a portion of the memory device is configured according to the at least one predefined access profile for the at least one usage.

As explained above in Section IX.C.1.(vi), *Sinclair* discloses this function. Further, as explained above in Section IX.C.1.(vi), *Sinclair* discloses that this functionality is carried out by a "controller," which corresponds to the controller 508 of the '486 Patent, as explained in Section IX.C.3.(ii).

4. Dependent Claim 21

i. The memory device of claim 15, wherein the at least one predefined access profile corresponds to at least one of: one or more write operations; one or more read operations; or one or more erase operations.

See Section above at IX.C.2.(i).

D. GROUND 4: CLAIMS 9 AND 16 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) OVER *COMPACTFLASH*, *TOOMBS*, AND *ELHAMIAS*

As shown below, *CompactFlash*, *Toombs*, and *Elhamias* render obvious Claims 9 and 16 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶379-384.

1. Dependent Claim 9

i. The method of claim 8, further comprising activating, based at least in part on the one or more commands, at least two predefined access profiles of the two or more predefined access profiles in parallel.

Ground 1 in Section IX.A.1 applies *CompactFlash* to independent Claim 8 and shows why a POSITA would combine *CompactFlash* with *Toombs*. Non-volatile memory cards were disclosed in *Elhamias*. Ex. 1002 at ¶380.

CompactFlash includes a controller, which receives a SET FEATURES command from the host. *See* Ex. 1003 at Fig. 1 (shown below). The SET FEATURES command is communicated from the host to the CompactFlash controller to select and activate one of the MultiWord or Ultra DMA modes (*i.e.*, a predefined access profile) from among the available modes supported by the device. *Id.* at 15, 156-58, Table 53 (indicating bits representing a host-selected DMA mode) (shown below). Specifically, the SET FEATURES command instructs the controller to set the DMA mode to the selected MultiWord DMA mode or Ultra DMA mode for subsequent DMA access operations (*i.e.*, the usage), such as READ DMA and WRITE DMA. *Id.* at 15, 157-58.

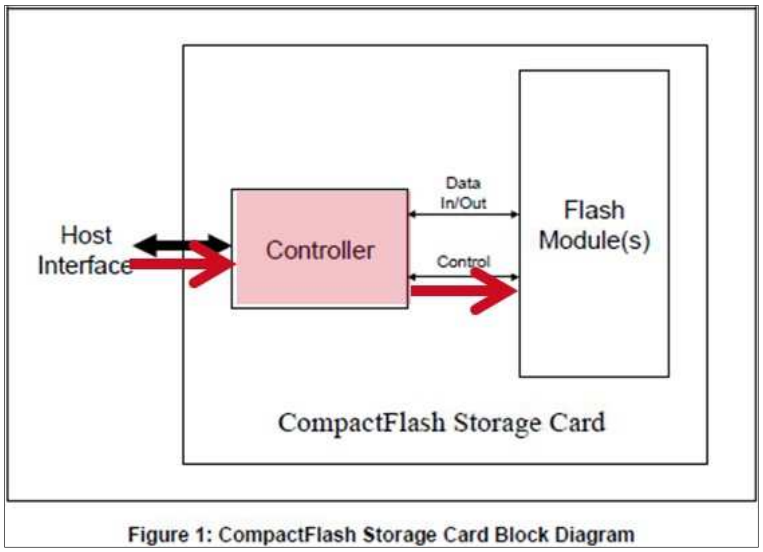


Figure 1: CompactFlash Storage Card Block Diagram

Id. at 19, Fig. 1 (annotated).

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at 158, Table 53 (annotated).

For example, for Ultra DMA modes, the Set transfer mode subcommand (using the transfer mode values in Table 53) in the SET FEATURES command allows "a host to select the Ultra DMA mode at which the system operates." *Id.* at 69.

Elhamias discloses that a memory device may include predetermined access profiles that are activated in parallel. Ex. 1002 at ¶388. For example, *Elhamias*

discloses that the disclosed storage device can utilize "memorize access sequences issued by the host under various predefined conditions, such as host reset or power on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to optimize operation for the expected commands." Ex. 1008 at ¶10. *Elhamias* further discloses that the "SD card 35 contains nine surface electrical contacts 10-18…Contact 12 receives commands (CMD) from the host and sends responses and status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2, DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its non-volatile memory and send data to the host in parallel from the memory." Ex. 1008 at ¶22. Thus, *Elhamias* discloses that a memory device may include predetermined access profiles that are activated in parallel. Ex. 1002 at ¶388.

A POSITA would combine the memory device from *CompactFlash*, where the memory device receives commands from one or more predefined access profiles, with *Elhamias*, where a memory card is capable of adapting to its operation by adapting to conduct two or more memory access operations in parallel. Ex. 1002 at ¶389. Indeed, the memory device in *Elhamias* is a desirable type of storage medium that a skill artisan would implement in the memory device of *CompactFlash* as an obvious design choice. Ex. 1002 at ¶389. For example, *Elhamias* specifically suggests that *Elhamias* is "removable non-volatile memory

cards [that] include a memory array and a controller that performs as the memory control and the host interface function. These removable cards are plugged into a different of variety of devices[.]" Ex. 1008 at ¶7.

In addition, a POSITA would combine *CompactFlash* and *Elhamias* because both *CompactFlash* and *Elhamias* disclose memory storage solutions in the same time frame. Ex. 1002 at ¶381.

Moreover, a POSITA would have especially been motivated to combine *CompactFlash* and *Elhamias*, because *Elhamias* improves the efficiency of data transfer, a stated goal of *CompactFlash.* Ex. 1002 at ¶382; Ex. 1015 ("Ultra DMA … modes will increase the CompactFlash interface data transfer rate[.]").

Elhamias also provides greater control for the host to order its operations. Ex. 1002 at ¶383. As disclosed in *Elhamias*, a host may impose requirements on read and write operations communicated to a memory device. Ex. 1008 at ¶9 ("the card uses host profiling where it will learn about the host during host-card interactions and collect information such read/write buffer transfer speed, idle times between sequential commands and other information and the card's controller will optimize its algorithms accordingly."). Using the advantages of *CompactFlash* of performing read and write operations under a well-established standard, a POSITA would have been motivated by the teachings of *Elhamias* to

use host prioritization of data to gain the advantage of meeting read and write operations in *CompactFlash*. Ex. 1002 at ¶383.

2. Dependent Claim 16

i. The memory device of claim 15, further comprising means for activating, based at least in part on the one or more commands, at least two predefined access profiles of the two or more predefined access profiles in parallel.[4]

Ground 1 under Section IX.A.4 applies to *CompactFlash* to independent Claim 15.

Further, as shown above in Section IX.A.4.(ii), *CompactFlash* discloses a controller that corresponds with controller 508 of the '486 Patent, a host interface that corresponds with interface 512 of the '486 Patent, and an interface with the memory that corresponds with the interface 506 of the '486 Patent. In addition, CompactFlash discloses "flash memory" that corresponds with physical memory 502 of the '486 Patent. Ex. 1003 at 19, Fig. 1; Ex. 1002 at ¶391.

Also, a POSITA would understand that data indicating the DMA Modes supported and selected are stored in portions of memory (*i.e.*, registers that

[4] Petitioner and Patent Owner agreed that this phrase is a means-plus-function limitation, with the function being, "activating, based at least in part on the one or more commands, at least two predefined access profiles of the two or more predefined access profiles in parallel," and the structure being "controller 508, physical memory 502, memory registers 504, communication interface 512, and interface 506 of Figure 5, 4:38-55; and structural equivalents thereof." Ex. 1025 at 4.

correspond to the registers 504 of the '486 Patent) on a CompactFlash device. Ex. 1002 at ¶392. The data is made accessible to the host via a "buffer" (*i.e.*, a register). Ex. 1003 at 115, 133-34. Ex. 1002 at ¶392.

Moreover, the selected access profile is stored in a register in the CompactFlash device when the host selects a supported profile. Ex. 1002 at ¶393. The host may use the "Set transfer mode subcommand" (designated "Feature 03h") to "select the Ultra DMA mode at which the system operates." Ex. 1003 at 69, 156-5. The "Set transfer mode subcommand" is part of the "SET FEATURES" command. Ex. 1003 at 158. The selected DMA mode is identified by storing a value corresponding to the selected access profile "in the Sector Count register" when the subcommand is involved. Ex. 1003 at 157 (emphasis added). Specifically, after receiving a SET FEATURES command, the memory controller will set a Sector Count register value to the bits indicated by Bits (7:3) (indicating the selected DMA protocol) and Bits (2:0) (indicating the selected DMA mode). Ex. 1003 at 158.

Thus, CompactFlash discloses registers for storing the predefined access profiles that correspond with the registers 504 of the '486 Patent. Ex. 1002 at ¶¶393-394. In addition, as discussed above, a POSITA would readily combine *CompactFlash* and *Elhamias*, and when combined, they disclose that two or more predefined access profiles are activated in parallel. Ex. 1002 at ¶¶379-84, 395-399.

E. GROUND 5: CLAIMS 9 AND 16 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) OVER *ZIV*, *VOGT*, *TOOMBS*, AND *ELHAMIAS*

As shown below, *Ziv, Vogt, Toombs,* and *Elhamias* render obvious Claims 9 and 16 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶400-418.

1. Dependent Claim 9

i. The method of claim 8, further comprising activating, based at least in part on the one or more commands, at least two predefined access profiles of the two or more predefined access profiles in parallel.

Ground 2 under Section IX.B.1 applies *Ziv*, *Vogt,* and *Toombs* to independent Claim 8. Non-volatile memory cards were disclosed in *Elhamias*. Ex. 1008 at ¶ 22.

Additionally, *Vogt* discloses embedding the flash memory within a device (*e.g.*, cell phone). *See* Ex. 1005 at 2:32-42. The "flash memory is ***embedded*** in the device, and cannot be easily reset or replaced." *Id.* at 11:16-19 (emphasis added).

A POSITA would combine the flash memory device in *Vogt* and/or *Elhamias* with the storage medium described in *Ziv* and would see benefits in doing so. Ex. 1002 at ¶¶402-403. The flash memory device in *Elhamias* and *Vogt* is a desirable type of storage medium that a skilled artisan would implement in the memory device in *Ziv* as an obvious design choice. Ex. 1002 at ¶402. *Elhamias* discloses that a memory device may include predetermined access profiles that are activated in parallel. Ex. 1002 at ¶410. For example, *Elhamias* discloses that the

disclosed storage device can utilize "memorize access sequences issued by the host under various predefined conditions, such as host reset or power on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to optimize operation for the expected commands." Ex. 1008 at ¶10. *Elhamias* further discloses that the "SD card 35 contains nine surface electrical contacts 10-18…Contact 12 receives commands (CMD) from the host and sends responses and status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2, DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its non-volatile memory and send data to the host in parallel from the memory." Ex. 1008 at ¶22.

Similarly, *Vogt* discloses the "benefit from inclusion of security primitives in flash memory", further confirming the desirability of combining *Vogt* with systems, such as *Ziv*, that involve secure access to data in a memory device. Ex. 1005 at 2:32-35.

2. Dependent Claim 16

i. The memory device of claim 15, further comprising means for activating, based at least in part on the one or more commands, at least two predefined access profiles of the two or more predefined access profiles in parallel.

Ground 2 in Section IX.B.3 applies to *Ziv*, *Vogt,* and *Toombs* to independent Claim 15.

Elhamias, when combined with *Ziv-Vogt-Toombs*, discloses that two or more predefined access profiles are activated in parallel. *See Supra* at IX.E.1.(i); Ex. 1002 at ¶¶415-418.

As discussed above, the *Ziv-Vogt-Toombs* combination discloses the memory device of Claim 15. *See Supra* at IX.B.3. Further, as shown above in Section IX.B.3.(ii), *Ziv* discloses a controller that corresponds with controller 508 of the ’486 Patent, a host interface that corresponds with interface 512 of the ’486 Patent, and an interface with the memory that corresponds with the interface 506 of the ’486 Patent. In addition, *Ziv* discloses flash memory 113 that corresponds with physical memory 502 of the ‘486 Patent. Ex. 1004 at Fig. 1; Ex. 1002 at ¶413.

Further, *Ziv’s* predefined access profiles (the password, address offset, and key) are stored in individual registers that correspond with registers 504 of the ’486 Patent. Ex. 1002 at ¶414. Specifically, the hashed password is stored in register

124, the address offset is stored in register 125, and the encrypted key is stored in

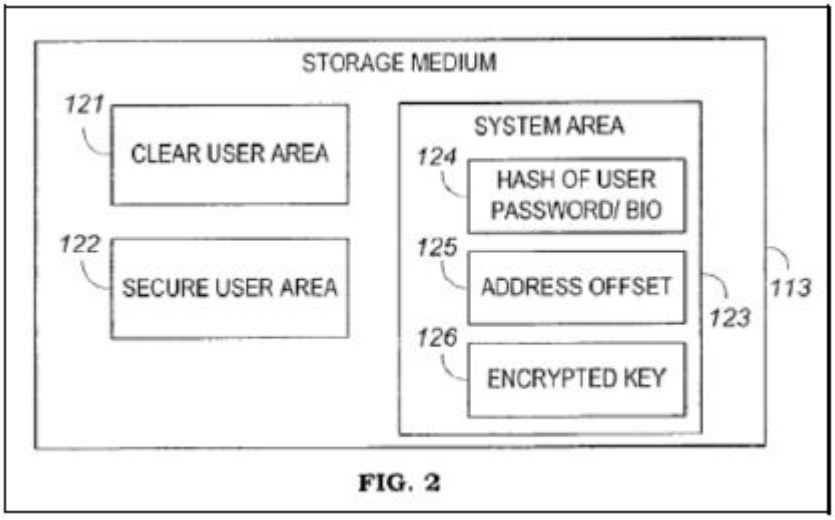


FIG. 2

register 126. Ex. 1004 at Fig. 2 (shown below).

Ex. 1004 at Fig. 2.

F. GROUND 6: CLAIMS 10 AND 17 ARE UNPATENTABLE UNDER 35 U.S.C. § 103(a) OVER *ZIV*, *VOGT*, AND *TOOMBS*

As shown below, *Ziv, Vogt,* and *Toombs* render obvious Claims 10 and 17 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶419-422.

1. Dependent Claim 10

i. The method of claim 8, wherein the at least one predefined access profile comprises a default access profile.

Ground 2 in Section IX.B.1 applies *Ziv*, *Vogt,* and *Toombs* to independent Claim 8.

Ziv comprises a default access profile (*i.e.,* access to the clear user area) that is used to set up the memory device upon power up. Ex. 1004 at 6:2-4 ("By

default, microprocessor 111 uses an address offset of zero, thus the host sees clear user area 121[.]"). The access to the clear user area does not require entry of a password. *Id.* at 6:4-7.

2. Dependent Claim 17

ii. The memory device of claim 15, wherein the at least one predefined access profile comprises a default access profile.

Ground 2 in Section IX.B.3 applies *Ziv* and *Vogt* to independent Claim 15. *See* Section above at IX.F.1.(i).

G. GROUND 7: CLAIMS 10 and 17 ARE RENDERED OBVIOUS BY SINCLAIR AND TOOMBS

As shown below, *Sinclair* and *Toombs* render obvious Claims 10 and 17 of the '486 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶423-426

1. Dependent Claim 10

i. The method of claim 8, wherein the at least one predefined access profile comprises a default access profile.

Ground 3 in Section IX.C.1 applies *Sinclair* and *Toombs* to independent Claim 8.

Sinclair discloses a default access profile, like the Reclaim Normal mode, that configures the memory device upon power up. Ex. 1007 at 23:47-48.

2. Dependent Claim 17

i. The memory device of claim 15, wherein the at least one predefined access profile comprises a default access profile.

Ground 3 in Section IX.C.3 applies *Sinclair* and *Toombs* to independent Claim 15.

See Section above at IX.G.1.(i).

X. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests that a trial for *inter partes* review of the '486 Patent be instituted and that Claims 8-10, 14-17, and 21 be rejected and canceled.

Dated: January 31, 2019

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1. The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,983 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2016, the word processing program used to create it.

2. The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14-point font.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true copy of the foregoing **PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,367,486** and supporting materials (Exhibits 1001 - 1025 and Power of Attorney) have been served in its entirety this 31st of January, 2019, by e-mail and Federal Express on Patent Owner at the correspondence address for the attorney of record for the 9,367,486 Patent shown in USPTO PAIR, as well as on counsel for Patent Owner in the co-pending litigation:

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