UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

MEMORY TECHNOLOGIES, LLC
Patent Owner

Case No.: To Be Assigned
U.S. Patent No. 9,063,850

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,063,850**

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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1015	U.S. Pat. Publ. No. 2007/079015 to Royer, Jr. et al.
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I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED (37 C.F.R. §42.22(a))

Kingston Technology Company, Inc. ("Petitioner" or "Kingston") hereby petitions to institute an *inter partes* review of Claims 1-4, 9-13, 19-22, and 27-31 (the "Challenged Claims") of U.S. Patent No. 9,063,850 (the "'850 Patent") to Hyvonen *et al*. (Ex. 1001), and cancel those claims as unpatentable.

As discussed below, the prior art anticipates and/or renders obvious the Challenged Claims of the '850 Patent under 35 U.S.C. § 102 and/or § 103. Accordingly, there is a reasonable likelihood that Petitioner will prevail with respect to at least one challenged claim, and Petitioner respectfully requests that the Board institute a trial for *inter partes* review and cancel all Challenged Claims as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. §42.8(a)(1))

A. Real Party-In-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Kingston Technology Company, Inc., is a real party-in-interest. Petitioner's parent company, Kingston Technology Corporation ("Kingston Holding"), is a holding company without any employees or operations. However, because Kingston Holding is the sole owner of Petitioner and shares some directors, Petitioner identifies Kingston Holding as an additional real party-in-interest.

B.   **Identification of Related Matters (37 C.F.R. §42.8(b)(2))**

Patent Owner Memory Technologies, LLC ("MTL") has asserted the Challenged Claims of the '850 Patent, as well as claims from seven other patents, against Kingston in a co-pending litigation, *Memory Technologies, LLC v. Kingston Technology Co., Inc*., 8:18-cv-00171 (C.D. Cal.). MTL's original Complaint was filed on January 31, 2018, and served on Kingston, at the earliest, on February 1, 2018.

In addition to this Petition, Kingston has or will be filing petitions for *inter partes* review of the other seven patents that MTL has asserted against it.

C.   **Counsel and Service Information (37 C.F.R. §§42.8(b)(3) & (b)(4))**

Petitioner designates the following Lead and Backup Counsel. Concurrently filed with this Petition is a Power of Attorney for appointing the following Lead and Backup Counsel, per 37 C.F.R. § 42.10(b). Service via hand-delivery may be made at the postal mailing addresses below. Petitioner consents to electronic service by e-mail at the following address: **Kingston-850ipr@pillsburylaw.com**.

Lead Counsel	Back-Up Counsel
Robert C.F. Pérez (Reg. No. 39,328) PILLSBURY WINTHROP SHAW PITTMAN LLP 1650 Tysons Boulevard, 14th Floor McLean, VA 22101 Telephone: 703.770.7900 Facsimile: 703.770.7901	**Christopher Kao** (*Pro hac vice* motion to be filed) **Brock S. Weber** (*Pro hac vice* motion to be filed) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200

D.   Payment of Fees (37 C.F.R. §42.103)

Petitioner authorizes the Patent and Trademark Office to charge Deposit

Account No. 033975 for the petition fee and for any other required fees.

III.   REQUIREMENTS FOR *INTER PARTES* REVIEW

A.   Identification of Challenge

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests that the Challenged

Claims of the '850 Patent be cancelled as anticipated or render obvious based on

the following grounds:

Ground	'850 Patent Claims	Basis for Rejection
1	1, 3, 9, 10, 12, 19, 21, 27, 28, and 30	§ 102 based on *CompactFlash*
2	1, 3, 9, 10, 12, 19, 21, 27, 28, and 30	§ 103 based on *Ziv and Vogt*
3	4, 13, 22, and 31	§ 103 based on *Ziv, Vogt,* and *eMMC*
4	2, 11, 20, and 29	§ 103 based on *CompactFlash* and *Elhamias*

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Ground	'850 Patent Claims	Basis for Rejection
5	2, 11, 20, and 29	§ 103 based on *Ziv, Vogt,* and *Elhamias*
6	1, 3, 9, 10, 12, 13, 19, 21, 27, 28, and 30	§ 102 based on *Sinclair*
7	13	§ 103 based on *Sinclair* and *eMMC*

The Declaration of R. Jacob Baker, Ph.D., P.E., filed herewith (Ex. 1002, "Baker Decl."), supports the challenge in this Petition that the Challenged Claims are invalid as anticipated and obvious.

IV.   A PERSON OF ORDINARY SKILL IN THE ART

Relative to the '850 Patent, a person of ordinary skill in the art ("POSITA") is a person having at least a bachelor's degree in electrical engineering, computer engineering, or equivalent training, with at least two years of academic or industry experience in the field of memory system design. Ex. 1002 at ¶65. However, a higher level of education could make up for less experience, and vice versa. *Id*.

V.   BACKGROUND OF THE TECHNOLOGY

A memory device is used to store electronic data. Ex. 1002 at ¶¶68-71. By 2008, several types of memory devices that use flash or EEPROM memory were in existence, including MultiMediaCard ("MMC") and CompactFlash ("CF"). *Id.* An MMC can communicate with a host device. Ex. 1008 at 19. As depicted below, for example, an MMC receives commands from a host device over a

"CMD" bus and communicates data over the "DAT" bus line. Ex. 1002 at ¶74; *see*

Ex. 1008 at 142, Fig. 4 (shown below).

Figure 4: MultiMediaCard Architecture
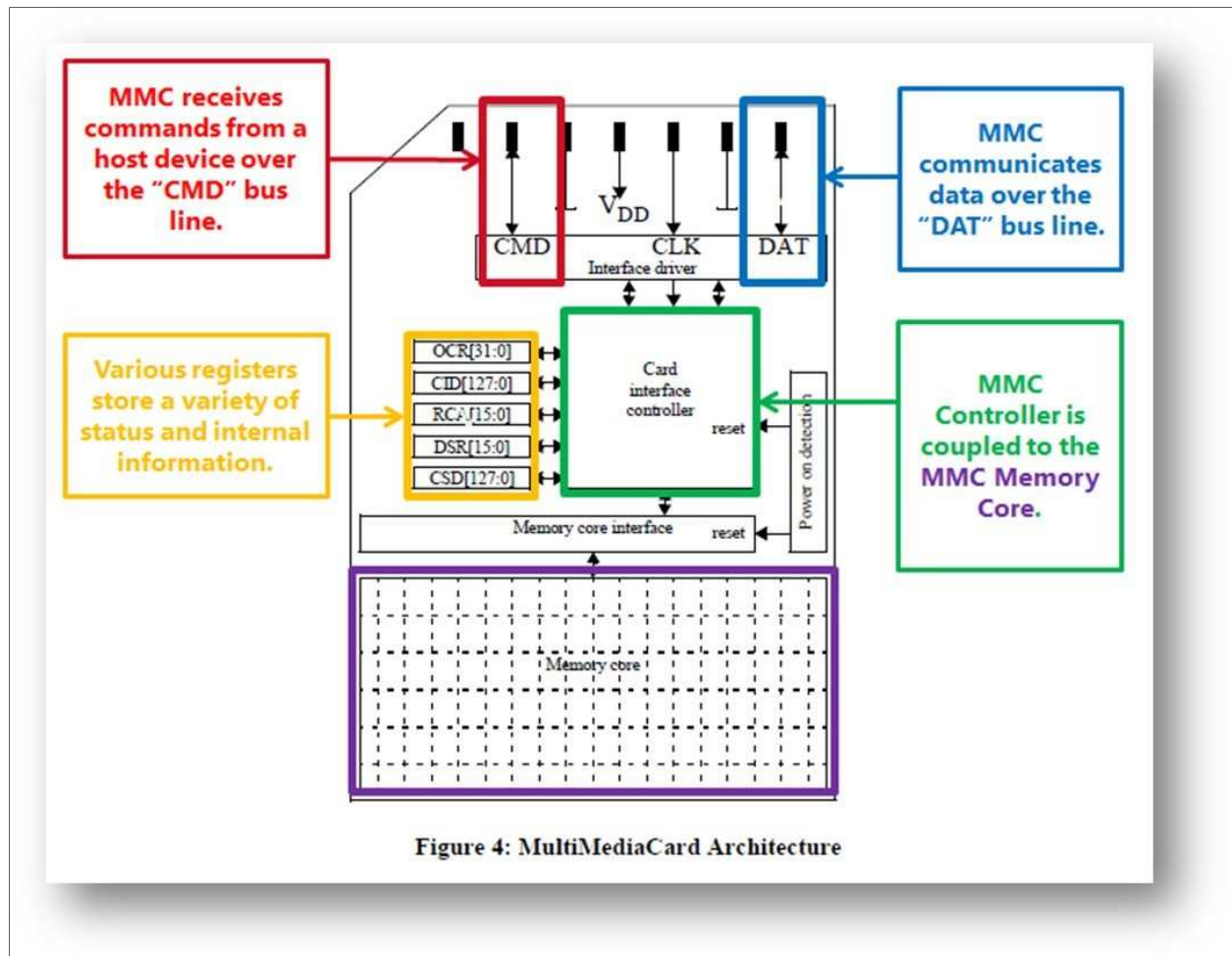
Ex. 1008 at Fig. 4 (annotated).

VI. OVERVIEW OF THE '850 PATENT

The '850 Patent issued on November 6, 2012 from U.S. Patent Application

No. 13/951,169 ("'169 Application"), filed on July 25, 2008. The '850 Patent

claims priority to U.S. Patent Application No. 12/039,672, which was filed on

February 28, 2008.

A.   **Summary of the Claimed Subject Matter**

The Challenged Claims generally relate to activating access profiles and configuring memory devices in accordance with the active access profile. The access profile "governs the current access operations to the memory device." Ex. 1001 at 4:63-64. The access profiles correspond to memory access operations, such as "a read, a write, an erase, and a modify attribute operation." *Id.* at 2:1-3, 5:7-9, 6:25-27.

The '850 Patent specification describes the invention as applicable "in any stand-alone or embedded system that comprises or accesses a memory device." *Id.* at 5:30-33. When connected to such a system, the memory device can "receive one or more commands ... for activating a particular access profile." *Id.* at 4:35-38. The system is also described as being able to "issue commands for configuring the memory device in accordance with an access profile." *Id.* at 3:44-50. The portion of the system that issues commands to the memory device is referred to as a "host." *Id.* at 2:65-66.

The '850 Patent specification also describes configurations that may correspond to access profiles. For instance, in a "burst profile mode, [an access profile,] corresponding to fast, contiguous data access," the memory device is configured so that "after receiving all the data" to be written from a host, it may

"indicate 'exit busy' and set the transfer mode to 'transfer state,' thus facilitating faster execution of subsequent accesses by the host." *Id.* at 7:21-26.

Other access profiles may cause the device to configure itself such that a particular profile is "associated with different partitions of the memory device," including either "logical or physical partitions." *Id.* at 7:37-42. Similarly, a profile may result in a device configuration such that access operations are "map[ped] … to certain sections of the physical memory with special characteristics." *Id.* at 7:54-57. Finally, some access profiles may result in a configuration such that the device postpones "management" or "background operations" until after the data transfer. *Id.* at 4:1-4, 4:52-56.

In addition, the memory controller may conduct or interleave simultaneous memory access operations. *Id.* at 6:58-61. In the event that the memory access operations conflict with each other, the controller may designate access priority levels to resolve the conflict. *Id.* at 2:32-34.

B. The '850 Patent Prosecution History

The '850 Patent issued from the '169 Application. Before issuance, the Applicant responded to three office actions. Ex. 1012 at 238, 440, 495.

The first and second office actions rejected a set of claims that Applicant eventually cancelled. Prior to the first office action, Applicants asserted the following exemplary claim:

> 1. (Currently Amended) A method ~~for configuring access to a memory device,~~ comprising:
>
>   receiving ~~one or more commands for activating~~ <u>a command to activate</u> one or more access profiles associated with [[the]] <u>a</u> memory device<u>, the command specifying a preferred access profile metadata</u>;
>
>   <u>selecting the preferred access profile from one or more access profiles based on the command;</u> and
>
>   configuring access to the memory device in accordance with ~~at least one of the access profiles~~ <u>the preferred access profile</u>.

Id. at 594 (displaying presented claims after a preliminary amendment).

The Examiner rejected the claims over *Suwa* and *Burgan*. In response to the rejection, the Applicant amended the claims and argued that the references do not teach the amendment. The following is an exemplary amendment submitted by the Applicant:

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1. (Currently Amended) A method comprising:

~~in response to~~ receiving a first command, ~~to activate one or more access profiles associated with a memory device, the command specifying a preferred access profile metadata;~~

selecting ~~the preferred~~ a first access profile from ~~one or more~~ a plurality of access profiles based on the command; [[and]]

configuring access to the memory device ~~in accordance with the preferred~~ for a first type of access based on the first access profile;

in response to receiving a second command, configuring access to the memory device for a second type of memory access based on a second access profile from the plurality of access profiles; and

interleaving access to the memory device between the first type of access and the second type of access.

Id. at 496.

The Examiner issued a Final Office Action, allowing dependent Claims 12-14 if rewritten in independent form and rejecting the Claims 1-4, 6-11, and 15-21 under 35 U.S.C. § 103. The Examiner rejected the claims over *Suwa* and *Tomaiuolo*. *Id.* at 461.

The Applicant subsequently cancelled all pending claims and asserted a new set of claims. The origin of Claim 10 of the '850 Patent can be found in Claim 31 of the '169 Application (shown below).

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31.   (New) A memory device comprising:

    one or more predefined access profiles to determine how access to the memory device is configured for at least one usage of the memory device;

    a controller configured to:

        receive a first set of one or more commands to activate the one or more predefined access profiles associated with the memory device; and

        receive a second set of one or more commands to configure access to the memory device in accordance with the one or more predefined access profiles such that the memory device is effective for the at least one usage.

Id. at 443.

The third office action rejected the claims under 35 U.S.C. § 112. In response, the Applicants filed a Response amending the claims and arguing that the amended claims render the § 112 rejection moot. *Id.* at 251-52. An exemplary amended claim (that issued as Claim 10 of the '850 Patent) is shown below:

> 31.   (Currently Amended) A memory device comprising:
>
>   one or more predefined access profiles to determine how access to the memory device is configured for at least one usage of the memory device;
>
>   a controller configured to:
>
>   receive ~~a first set of one or more commands~~ at least one first command to activate at least one of the one or more predefined access profiles associated with the memory device; and
>
>   receive ~~a second set of one or more commands~~ at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is ~~effective~~ configured according to the at least one of the one or more predefined access profiles for the at least one usage.

Id. at 256.

A Notice of Allowance subsequently issued. *Id.* at 13.

C.   The '180 Patent Prosecution History

The '850 Patent claims priority to the 672 Application, which later issued as U.S. Pat. No. 8,307,180 ("'180 Patent"). As such, the prosecution history of the '180 Patent is relevant to the '850 Patent. *Ormco Corp. v. Align Tech., Inc.*, 498 F.3d 1307, 1314 (Fed. Cir. 2007) ("statements in the familial application are relevant in construing the claims at issue.").

Before issuance of the '180 Patent, Applicant responded to three office actions and submitted a notice of appeal and a pre-appeal brief. Ex. 1007 at 327, 393, 406, 440. The resulting '180 Patent issued on Nov. 6, 2012.

The first office action rejected the claims as anticipated by *Burgan*. *Id.* at 443. *Burgan* teaches smart phones with various profiles, such as a work profile and a family profile, that are accessed in response to caller ID information of a received call. Ex. 1009 at ¶¶5-6.

Applicant's response to the first office action is relevant to the "command" claim element. According to Applicant, "***[a] command in the context of the various embodiments of the present application***, and in any other context for that matter, ***suggests some type of authoritative direction or instruction to do/not to do something.***" Ex. 1007 at 427 (emphasis supplied). Using this definition, Applicant submitted that a POSITA would not equate the received Caller ID information in *Burgan* with an actual "command," because a Caller ID is a "passive" identifier. *Id.* at 427.

Unconvinced by the Applicant's argument, the Patent Office subsequently issued a final rejection on July 6, 2011, maintaining the rejection. *Id.* at 408. In response, Applicant repeated its arguments in a Reply to the Final Office Action. *Id.* at 401. Applicant thereafter filed a notice of appeal and a pre-appeal brief. *Id.* at 382, 393-96. The Pre-Appeal Panel decided to withdraw the rejection and issue a new office action. *Id.* at 357.

The Examiner then rejected the claims over *Suwa* and *Bertone*. *Id.* at 329.

Applicant made substantial amendments to the claims to distinguish *Suwa* and

Bertone by further limiting a predefined access profile and the received one or

more commands. *Id.* at 259-268. For example, the amendments to Claim 17 are

shown below:

17. (Currently Amended) A memory device, comprising:

one or more registers for storing one or more predefined access profiles associated with said memory device, said predefined access profiles being effective for determining how access to said memory device is configured for at least one usage;

~~receiving means~~ a controller for receiving one or more commands related to said at least one usage of said memory device, said one or more commands for activating said one or more predefined access profiles associated with said memory device, said controller also ~~; and~~

———————— ~~configuring means~~ for configuring access to said memory device in accordance with at least one of said predefined access profiles so that said memory device is effective for said at least one usage.

Id. at 261

Applicant also clarified the claim limitation, "configuring access to said

memory device." Applicant argued that, unlike the claim requiring "configuring

access to said memory device," the memory device in *Bertone* only configures the

memory device according to "timing characteristics to control the speed

performance of the memory module." Ex. 1007 at 266-67. Applicant argued that merely changing an operating speed for the memory device **does not** constitute an access configuration.
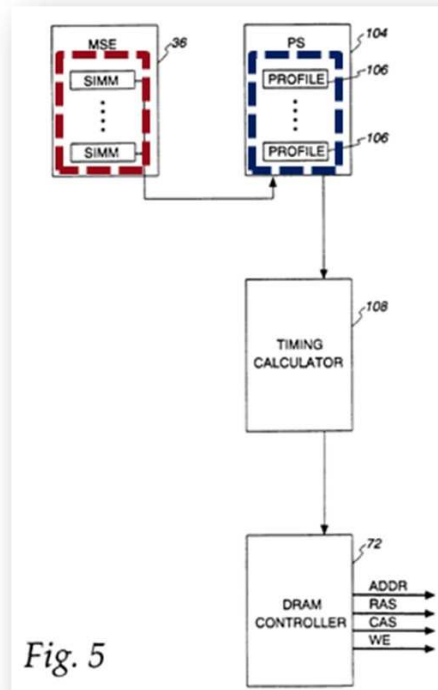
Fig. 5

Ex. 1010 at Fig. 5 (annotated).

Applicant also contended that *Suwa* does not configure an access profile, because the switcher in *Suwa* "automatically completes necessary changes to use the selected mode" upon activation. *Id.* at 266. Applicant argued that the claimed invention requires that the activation of an access profile **occurs separately** from the access configuration of the memory device.

A Notice of Allowance subsequently issued. Ex. 1007 at 244.

VII.   **CLAIM CONSTRUCTION**

A.   **Legal overview**

The Patent Office has adopted a rule by which claims are construed in accordance with "the standard used in federal courts, in other words, the claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005)." 83 FR 51340. This rule reflects that the PTAB in an AIA proceeding will apply the same standard applied in federal courts to construe patent claims. For example, claim construction begins with the language of the claims. *Phillips*, 415 F.3d at 1312-14. The "words of a claim are generally given their ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1312-13. The specification is "the single best guide to the meaning of a disputed term and . . . acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." *Id.* at 1321 (internal quotation marks omitted). Although the prosecution history "often lacks the clarity of the specification and thus is less useful for claim construction purposes," it is another source of intrinsic evidence that can "inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the

invention in the course of prosecution, making the claim scope narrower than it

would otherwise be." *Id.* at 1317.

All claim terms of Challenged Claims of the '850 Patent have been accorded

their plain and ordinary meaning as understood by POSITA and consistent with the

intrinsic record. Petitioner's interpretation of the claim terms in the '850 Patent is

further explained for each claim limitation in relation to the prior art discussed in

the proposed grounds for invalidity, below, in Grounds 1-7.

Under the *Phillips* standard and for clarity, Petitioner provides the following

specific constructions.[1]

B. Claim Terms

1. "predefined access profile"

The Challenged Claims describe "access profiles" in several different ways.

An access profile may be a mode, setting, control, or logic for an access operation,

each of which is disclosed in the specification. The Board should construe

"predefined access profile" to mean a "mode, setting, control, or logic defined in

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[1] Petitioner reserves the right to address any claim construction positions taken by
the Patent Owner in its Preliminary Response, if any, including under 37 C.F.R.
§ 42.108(c). Petitioner further reserves its ability to show that claims of the '850
Patent are invalid under 35 U.S.C. §112 in the co-pending litigation, despite
offering explicit and implicit claim constructions herein.

advance for reading, writing, modifying, deleting, or changing the attributes of data." Ex. 1002 at ¶¶133-135.

For example, the '850 Patent discloses that a profile can be a mode: "one profile may be defined as a burst profile **mode**, corresponding to a fast, contiguous data access **mode."** Ex. 1001 at 7:19-22 (emphasis added); *id.* at 4:44-52 (random mode profile).

The specification also describes that profiles can be a control or setting: "the access profile associated with a media device may be adapted to comprise different **control and/or setting** profiles that are associated with different partitions of the memory device." *Id.* at 7:37-41 (emphasis added). Lastly, the specification states that "an access profile may be implemented as a binary file that further comprises the required **logic** to implement an access profile." *Id.* at 5:20-25 (emphasis added).

2. **"configuring access"**

The Challenged Claims provide that the "predetermined access profiles" configure access to the "memory device." The Board should construe "configuring access" to mean "setting the memory device for reading, writing, modifying, deleting, or changing the attributes of data." Ex. 1002 at ¶¶136-138.

In Fig. 5 of the '850 Patent, the "memory device" (red box) includes many components. Ex. 1001 at Fig. 5. For example, as depicted below, memory device

500 contains a "memory" 502 (blue box), "controller" 508 (green box), an

interface (506) through which communications between the controller and the

memory may be conducted, and another interface (512) for communications with a
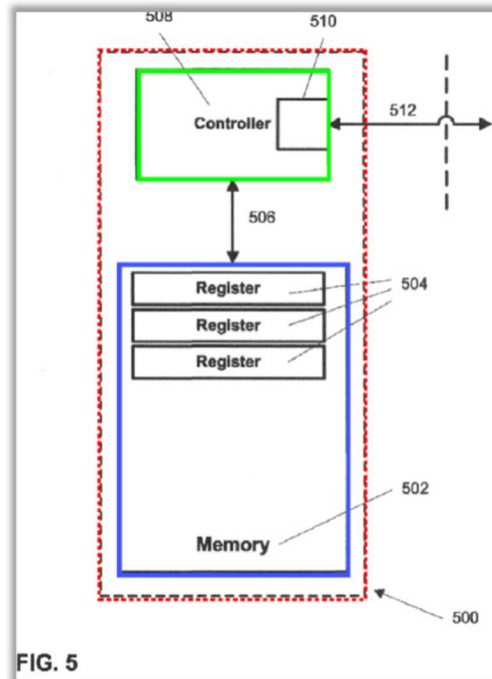
FIG. 5

host device. *Id*.

Ex. 1001 at Fig. 5

Thus, the proposed construction provides that the predefined access profiles

can also configure data on the controller (green box) or other components of the

"memory device" (red box), as indicated by the intrinsic evidence. Ex. 1002 at

¶¶136-138.

3. "usage"

The Challenged Claims provide that the term "usage" is associated with use

of the claimed memory device by the host. Ex. 1002 at ¶¶139-140. The Board

should construe the term "usage" to mean "host activity in accordance with the predefined access profile."

For example, the Challenged Claims provide that the memory device "<u>receives</u> one or more commands <u>related to a least one usage</u> <u>of</u> said memory device and that the predefined access profiles" determine <u>how access</u> is configured for said at least one <u>usage</u>. Ex. 1001 at 2:39-67 (emphasis added). Because the commands are "received" for a usage "of the memory device" and the "access is configured" for the usage, it is clear that "usage" refers to host activity, as that is where the commands can originate and the device that is accessing the memory card. This is also clear from the specification. Specifically, the '850 Patent states that an access profile "governs the current access operations to the memory device" by the host device. Ex. 1001 at 4:62-65.

VIII. <u>SUMMARY OF PRIOR ART</u>

A. <u>CompactFlash</u>

A CompactFlash device is a flash memory mass storage device. Ex. 1002 at ¶142. SanDisk first manufactured a CompactFlash device in 1994. Ex. 1013 at 1:56-59. CompactFlash quickly became the go-to portable mass storage device for electronic devices. Ex. 1002 at ¶143. CompactFlash remains popular and is supported by many devices. *Id.*

In 1995, the CompactFlash Association was formed by a group of international companies with the goal of creating an industry standard for flash-based mass storage. *Id.* at ¶144. The CompactFlash specification establishes the methods, processes, and practices for both the CompactFlash device and a host interacting with the device. *Id.* at ¶145.

On December 23, 2004, the CompactFlash Association released CompactFlash Specification Revision 3.0 (*CompactFlash*). Ex. 1003 at 1; Ex. 1020 at ¶7 (Declaration of Michael Asao, consultant for the CompactFlash Association). *CompactFlash* was made publicly available to any interested member of the public free of charge prior to 2008, as, for example, the CompactFlash Association publicly announced on January 6, 2005 that *CompactFlash* "is available to download free from the CFA website at http://www.compactflash.org." Ex. 1019 at 9; Ex. 1018 at ¶6 (authenticating page 9 of Ex. 1019 as an accurate representation of the January 6, 2005 announcement by the CompactFlash Association); *see also* Ex. 1014 (Jan. 7, 2005 article stating that "[t]he CF Specification Revision 3.0 is available to download free from the CFA web site at http://www.compactflash.org"); Ex. 1015 at ¶3 (describing an exemplary hard drive that utilizes a CompactFlash interface "as described in the CF+ and CompactFlash Specification Revision 3.0, published by the

CompactFlash Association, Palo Alto, Calif., Dec. 23, 2004,

http://www.compactflash.org.") (published on Apr. 5, 2007).

Moreover, *CompactFlash* was freely and publicly available online from the

CompactFlash website as of at least January 13, 2005. Ex. 1020 at ¶7; Ex. 1019 at

2-3 (displaying the CompactFlash homepage indicating that *CompactFlash* "is now

available to download" on Jan. 13, 2005); *Id.* at 6 (displaying the registration form

that once submitted included a link for a free download for *CompactFlash*); Ex.

1018 at ¶6 (authenticating pages 2-3 of Ex. 1019 as an accurate representation of

the CompactFlash Association website on Jan. 13, 2005 and page 6 of Ex. 1019 as

an accurate representation of the CompactFlash registration form on January 27,

2005). *See Crestron Electronics Inc. v. Intuitive Building Controls Inc.,* Case

IPR2015-01460, slip op. at 12-22 (PTAB Jan. 14, 2016) (Paper 14). Accordingly,

CompactFlash qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and

102(b). *CompactFlash* was not previously presented to the PTO in the context of

the '850 Patent.

The CompactFlash Association made improvements to direct memory

access (DMA) data transfer in Revision 3. A DMA data transfer occurs directly

between the hardware subsystem and the memory device, rather than involving the

host's CPU as an intermediary. Ex. 1002 at ¶148. In this manner, transfer speeds

are boosted and the CPU is freed to work on other tasks while the transfer occurs.

Id. at ¶149. Starting with Revision 3.0, "UltraDMA" was introduced, which boosted DMA transfer speed four-fold from the prior "MultiWord DMA" transfer. Ex. 1014 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").

CompactFlash also introduced several Ultra DMA modes. Ex. 1003 at 137. A CompactFlash controller configures a CompactFlash device to perform the Ultra-DMA transfer according to a protocol based on the mode selected. When a host sets an Ultra DMA mode, the memory device automatically disables any enabled MultiWord DMA mode. *Id.* at 158. In response, the memory device sets the selected Ultra DMA mode in a task file register. *Id.* at 120.

The host may subsequently communicate a READ DMA or WRITE DMA command to transfer data to the device. *Id.* at 52. The CompactFlash device, in response, will begin the Ultra DMA-specific initiation protocol to configure the memory device for an Ultra DMA transfer. *Id.* at 68-70. As illustrated for a data-in burst in Fig. 33 and a data-out burst in Fig. 38 (both shown below), the controller starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal. *Id.* at 75-76, 81-82. After the host responds by asserting and/or negating several signals, the controller will assert either a DSTROBE signal or DDMARDY signal until the end of the burst. *Id.* at 75-76, 81-82. Finally, unlike the older MultiWord DMA modes, the device will calculate a CRC value to ensure

the accuracy of the data transferred in the Ultra DMA modes. *Id.* at 90. If the

memory device detects errors, an Error Register is updated to reflect the error. *Id.*

at 90.

Figure 33: Ultra DMA Data-In Burst Initiation Timing

Id. at Fig. 33 (annotated).

Figure 38: Ultra DMA Data-Out Burst Initiation Timing
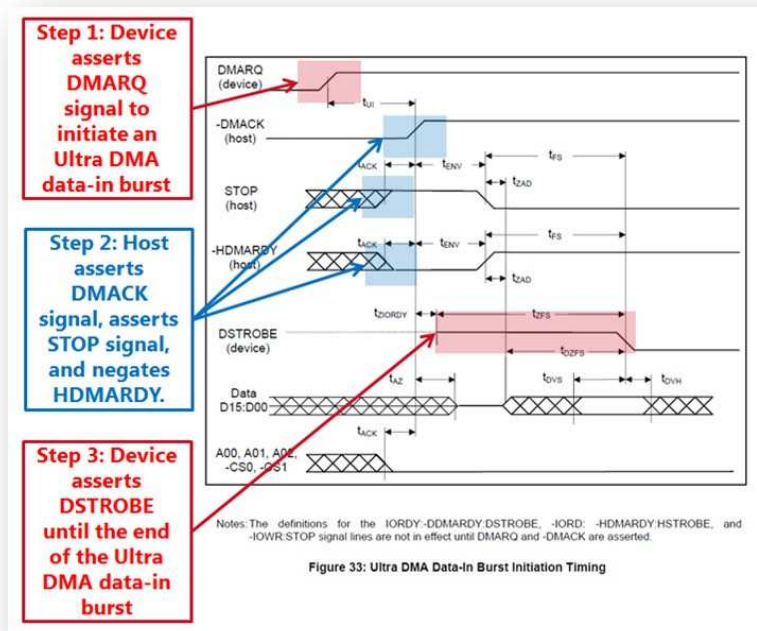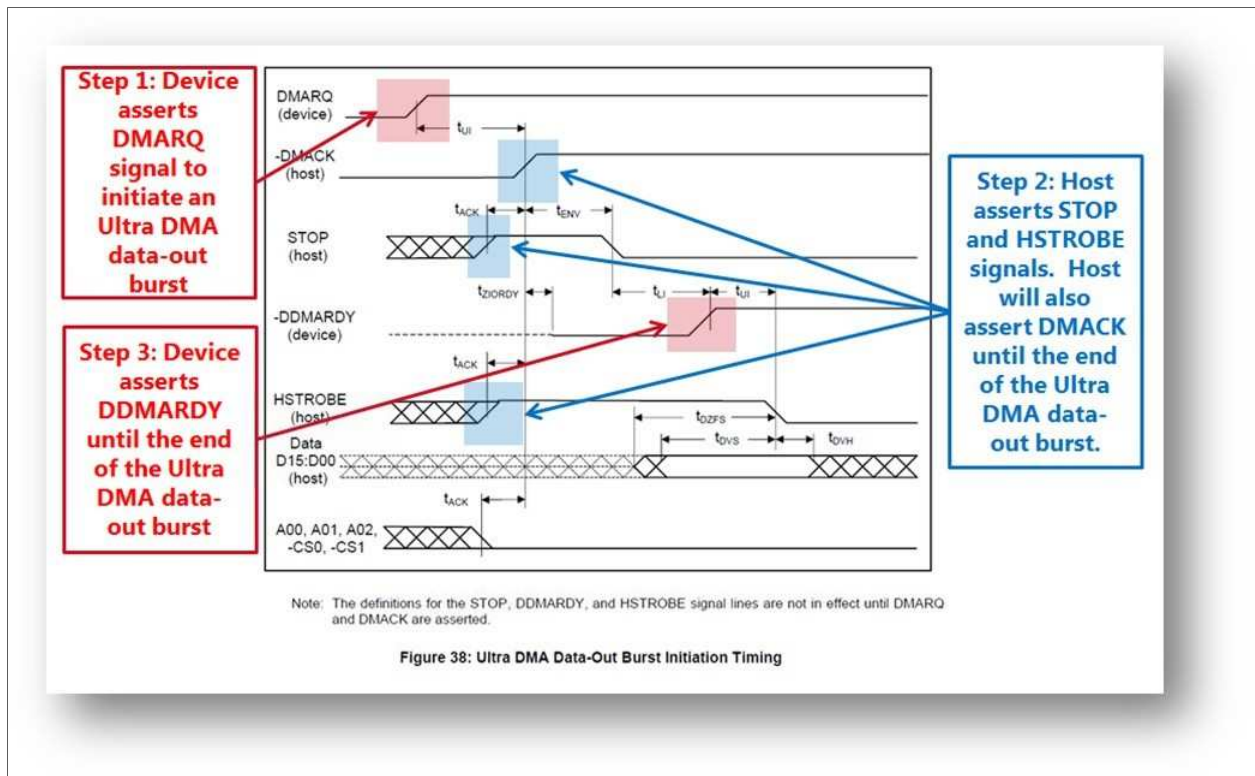
Id. at Fig. 38 (annotated).

B.   eMMC

eMMC is an embedded memory module standard promulgated and

announced by JEDEC via a press release on December 20, 2006. Ex. 1016. An

index describing the press release was publicly available on the JEDEC website no

later than June 29, 2007, when the Internet Archive Wayback Machine captured

the JEDEC index. Ex. 1018 at ¶5 (indicating that press release in Ex. 1016 was

posted on the JEDEC website on December 20, 2006); Ex. 1018 at ¶6

(authenticating page 12 of Ex. 1019 as an accurate representation of the June 29,

2007 JEDEC index of press releases). The underlying eMMC specification was

also made publicly available at the time of the press release. Ex. 1016 (noting that "eMMC™ is the first product standard from the partnership [of JEDEC and the MultiMediaCard Association]" and that "[a]ll JEDEC standards are available online, at no charge."); *see also* Ex. 1019 at 14 (JEDEC standard policy captured by the Wayback Machine on July, 3, 2007, noting "JEDEC standards, publications, package outlines and all other documents posted on JEDECs worldwide web site (collectively referred to as the files) may be downloaded free of charge," subject to accepting the terms of JEDEC's copyright statement); Ex. 1018 at ¶6 (authenticating page 14 of Ex. 1018 as an accurate representation of the July, 3, 2007 JEDEC copyright agreement). The public availability of eMMC as prior art against the '850 Patent is corroborated by the file history and the patent specification, where the Applicant admitted the prior art status of eMMC. Ex. 1007 at 355; Ex. 1001 at 2:30-32 (discussing "JESD84 standard for eMMC"), 7:1-4 (discussing "the current JEDEC JC64 eMMC version 4.3 (JESD84) [standard]"). Thus, eMMC is available as prior art under §§ 102(a) and 102(b).

An eMMC module consists of flash memory and a controller, in a small BGA package that can be embedded in a host. Ex. 1016. The eMMC module used the pre-existing MMC standard for host/memory communications. *Id*. This enabled hosts to access "all major classes of mass storage memory subsystems,

including embedded memory ... memory cards, or even hard disk drives (via ATA-on-MMC specification) with one common MMC interface[.]" *Id.*

C.   United States Patent No. 7,478,248 (*Ziv*)

Ziv was filed November 27, 2002, and published on May 27, 2004. *Ziv* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Ziv* was not previously presented to the PTO in the context of the '850 Patent.

Ziv discloses a memory controller that allows profile-based access to an encrypted partition of memory. Ex. 1004 at Abstract. A user first selects a password that is hashed and stored in a register. *Id.* at 4:15-20. The system also generates a cryptographic key, which is used with a stored address offset for accessing the secure area. *Id.* at 5:14-15.

Id. at Fig. 2 (annotated)

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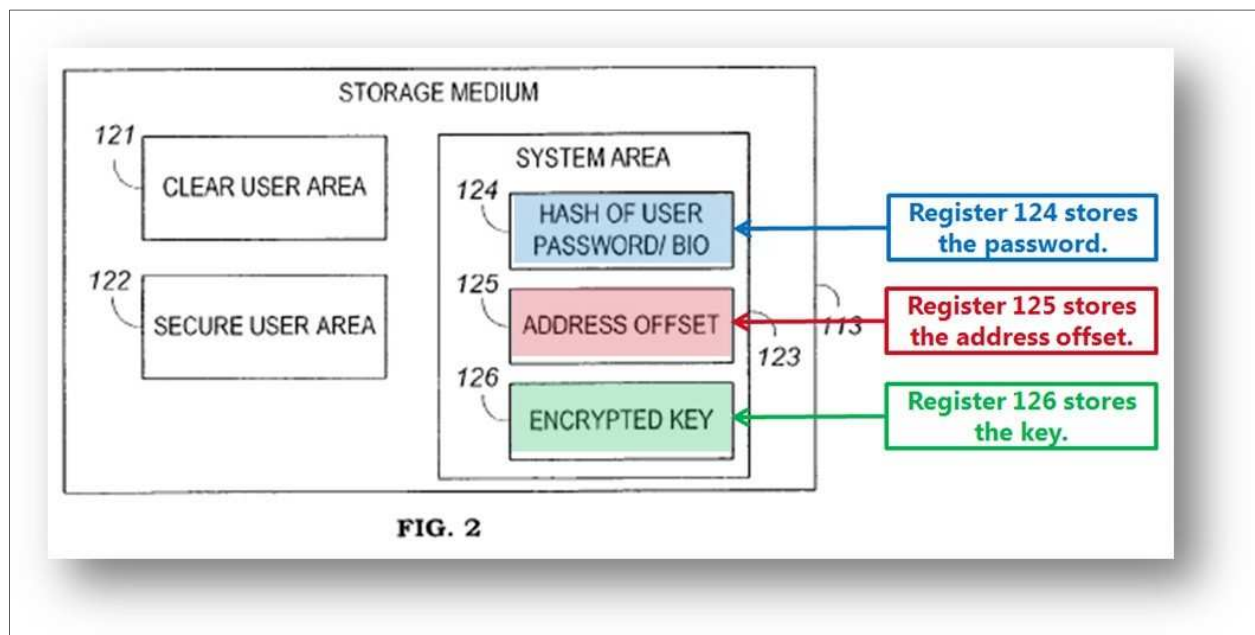
The secure memory area is activated when the host transmits a valid

password to the controller. *Id.* at 6:15-22. Then the memory controller remounts

the memory by using the stored address offset in the register to point to the secure

partition (as illustrated in Fig. 4B). *Id.* at 6:42-49, Fig. 4B (shown below).
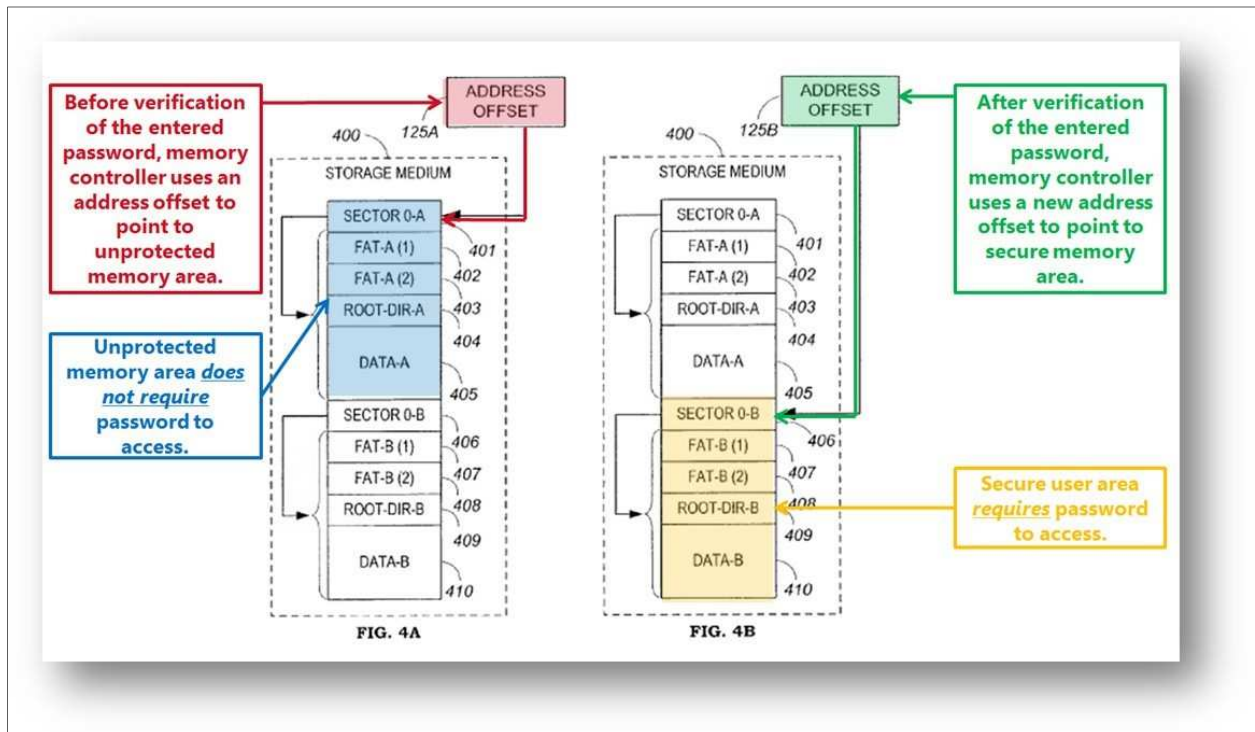
Id. at Figs. 4A-B (annotated).

Next, after receiving a subsequent read or write command, the controller

must configure the memory device by encrypting/decrypting the data and using the

address offset to point to the proper memory address. *Id.* at 7:29-47. Once

completed, the memory device can successfully complete the read or write

operation to/from the secure memory area. *Id.* at 7:40-47.
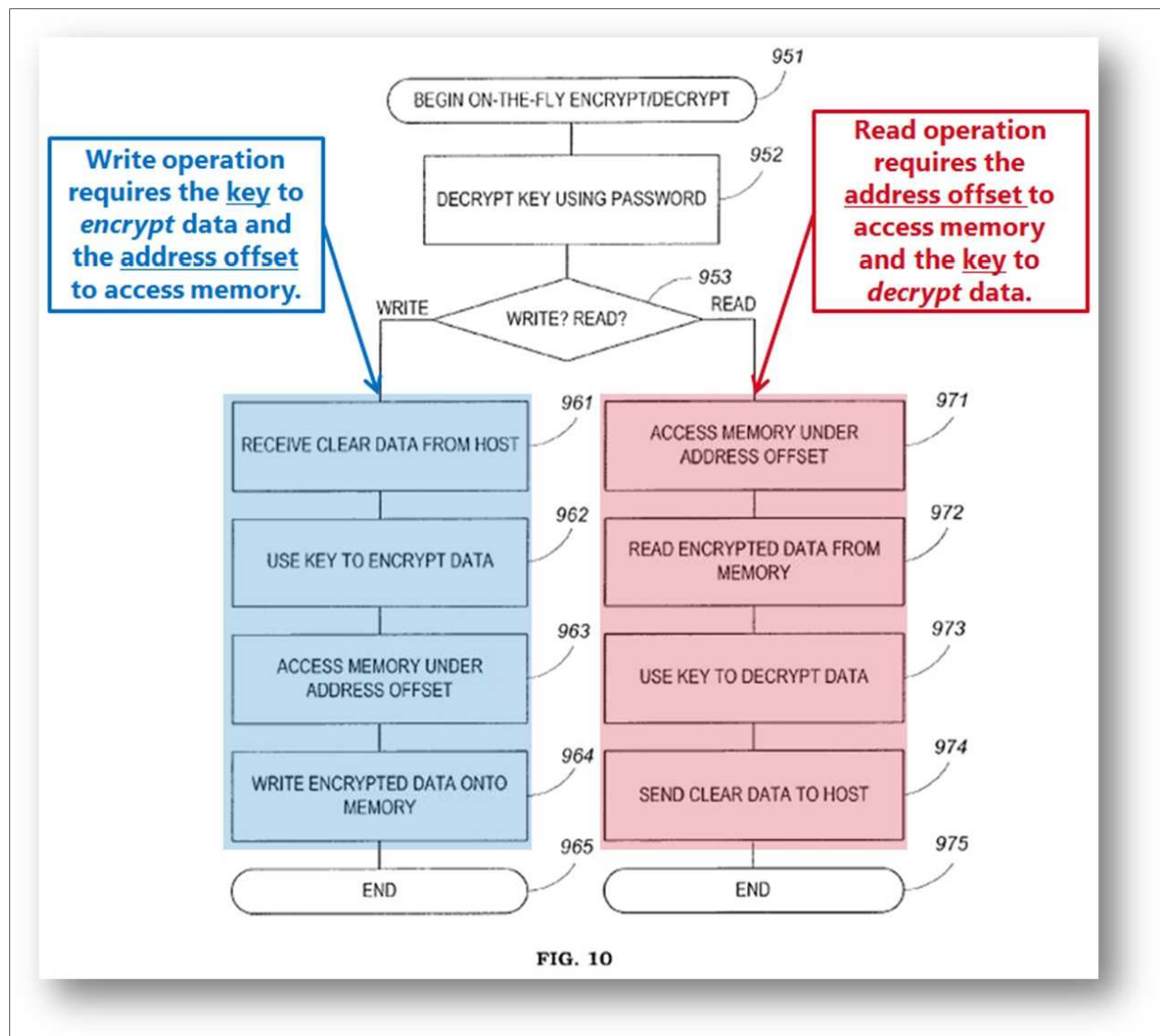
Id. at Fig. 10 (annotated).

D.   United States Patent No. 6,681,304 (*Vogt*)

Vogt was filed June 30, 2000 and issued on January 20, 2004. *Vogt* is prior

art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Vogt* was not

previously presented to the PTO in the context of the '850 Patent.

Vogt teaches a "password verify" command to access hidden storage in a memory device. Ex. 1005 at 6:35-37, 8:11-30, 11:53-55. *Vogt* also teaches implementing the hidden storage in a flash memory embedded in a device. *Id.* at 11:16-19.

Vogt further discloses a specific configuration for a read/write operation accessing a hidden storage area in the memory device. Upon receiving a memory read or write signal that attempts to access a hidden storage area address, the controller must then create a hidden storage read signal or write signal. *Id.* at 4:7-10. To create the hidden storage read/write signal, a Valid_HS_Access signal is logically "ANDed" with the memory read/write signal. *Id.* at 4:7-10. The Valid_HS_Access signal accounts that a valid user password has been entered for that specific password-protected hidden storage area. *Id.* at 3:45-4:6. Moreover, in read operations accessing a hidden storage, data is uniquely sent to a "hidden storage bus out" before transferring to the external data bus. *Id.* at 5:24-28.

E.   United States Patent Publication No. 2006/00220054 (*Elhamias*)

Elhamias was filed on July 28, 2004 and was published on February 2, 2006. *Elhamias* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Elhamias* was not previously presented to the PTO in the context of the '850 Patent.

Elhamias discloses a memory card that adapts its operation according to the application to which it is applied or the conditions under which it is operated. Ex. 1006 at ¶8. *Elhamias* further discloses that the "maximum rate of data transfer between the host and the card is limited by the number of parallel data paths that are used." *Id.* at ¶22. Thus, the memory card is able to receive data in parallel for its storage and send data to the host in parallel from the memory. *Id*.

F.   United States Patent No. 7,409,489 (*Sinclair*)

Sinclair was filed on October 25, 2005, claims priority to U.S. Provisional App. No. 60/705,388 filed on August 3, 2005, and was published on February 8, 2007. *Sinclair* is prior art under at least pre-AIA 35 U.S.C. §§ 102(a), (b), and (e). *Sinclair* was not previously presented to the PTO in the context of the '850 Patent.

Sinclair discloses selectable reclaim operation modes that provide optimizations to the rate that memory reclaim operations (*i.e.*, background/management operations) occur. Ex. 1017 at Abstract. Reclaim operations convert memory containing obsolete data into writeable memory. *Id.* at 2:9-11. An exemplary reclaim operation mode is the Reclaim Normal mode, which can be activated by the host sending a "Reclaim_normal" command to the memory controller. *Id.* at 23:27-30; 23:47-51. This changes the configuration of the memory device to interject reclaim operations between write commands received from the host. *Id.* at 23:47-51, 2:50-57. The device calculates an optimal

interleave ratio of reclaim operations to write commands such that the memory

card will run out of writeable memory only when no reclaimable memory remains.

Id. at 2:50- 57.
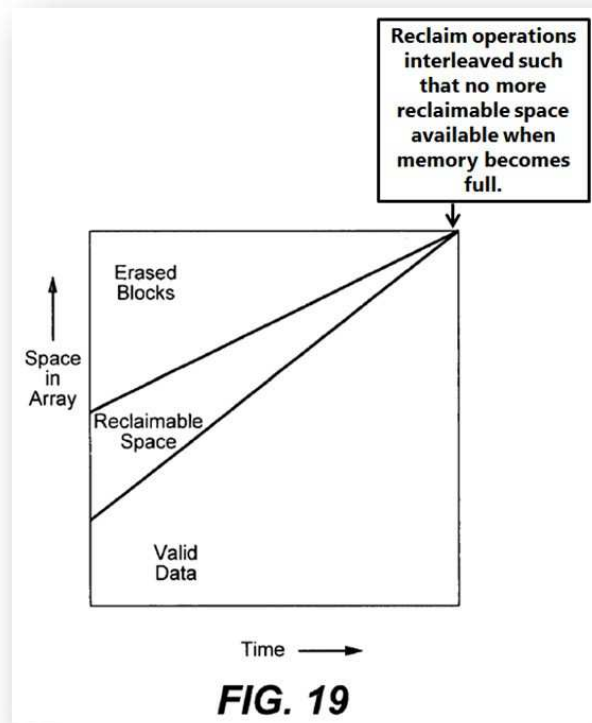
FIG. 19

Id. at Fig. 19 (displaying a time graph illustrating an optimal interleave of

reclaim operations to write operations) (annotated).

The interleave ratio can be recalculated periodically or when triggered by a host command. *Id.* at 18:17-26. As shown in Fig. 20, when host issues a delete command to the memory device at time t10, the system alters the interleave ratio such that the time when no more reclaimable space is available shifts to the newly anticipated time when the memory will be filled to capacity. *Id.* at 18:12-26.
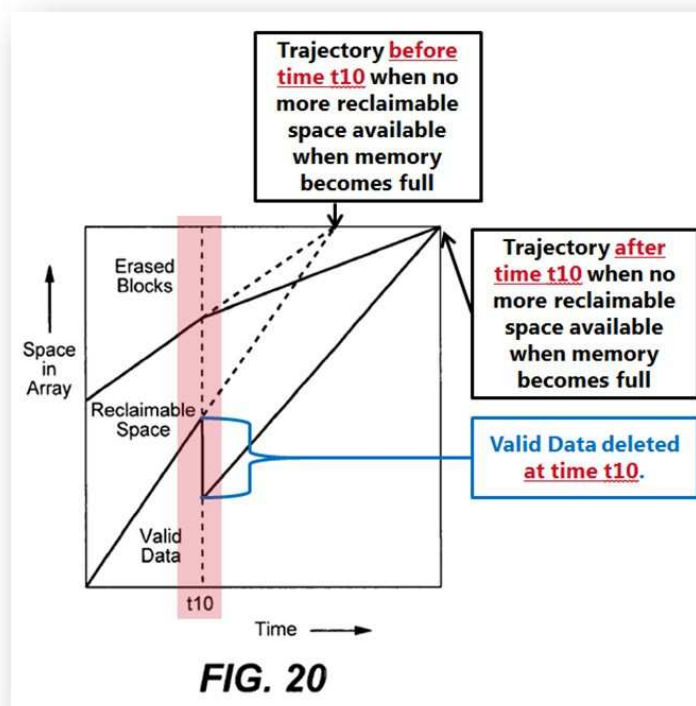
FIG. 20

Id. at Fig. 20 (annotated).

Sinclair also describes other reclaim modes selectable by the host, such that that "the host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity." *Id.* at 23:27-30, 23:36-59.

IX. GROUNDS FOR CHALLENGE

A. GROUND 1: Claims 1, 3, 9, 10, 12, 19, 21, 27, 28, and 30 are unpatentable under 35 U.S.C. § 102 over *CompactFlash*

As shown below, *CompactFlash* anticipates Claims 1, 3, 9, 10, 12, 19, 21,

27, 28, and 30 of the '850 Patent under 35 U.S.C. § 102. *See also* Ex. 1002 at

¶¶211-252.

1. Independent Claim 1

(i) (Preamble)A memory device comprising:

The CompactFlash device is a memory device and contains a "controller and

flash memory module(s)." Ex. 1003 at 19, Fig. 1 (below); Ex. 1002 at ¶211.
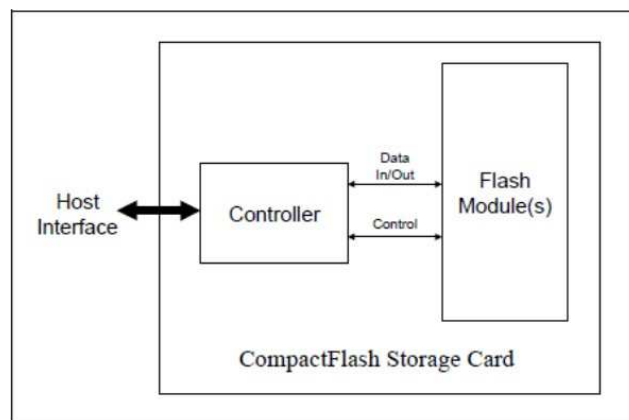
Figure 1: CompactFlash Storage Card Block Diagram

(ii) one or more registers to store one or more predefined access profiles associated with the memory device, the one or more predefined access profiles used to determine how access to the memory device is configured for at least one usage; and

CompactFlash discloses MultiWord and Ultra DMA modes that determine

how access to the memory device is configured for a usage. As shown in Table

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53, various MultiWord DMA and Ultra DMA modes are supported, each of which

constitutes a pre-defined access profile.

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Ex. 1003 at 158 (equating MultiWord DMA and Ultra DMA "Mode[s]" as

"transfer mode number[s]"). For example, the following Ultra DMA Modes are

possible:

6.2.1.6.26   Word 88: Ultra DMA Modes Supported and Selected

* * *

Bit 4: 1 = Ultra DMA mode 4 and below are supported. Bits 0-3 Shall be set to 1.

Bit 3: 1 = Ultra DMA mode 3 and below are supported, Bits 0-2 Shall be set to 1.

Bit 2: 1 = Ultra DMA mode 2 and below are supported. Bits 0-1 Shall be set to 1.

Bit 1: 1 = Ultra DMA mode 1 and below are supported. Bit 0 Shall be set to 1.

Bit 0: 1 = Ultra DMA mode 0 is supported

Id. at 137, 132-33.

Each DMA mode is an access profile, because the selected mode is used to determine the memory device configuration for the subsequent DMA access operations to the memory device. *See* Ex. 1001 at 3:56-58 ("***This profile***, which may be any one of the supported predefined profiles, ***governs the current access operations to the memory device***.") (emphasis supplied); Ex. 1002 at ¶¶219-23. For instance, if an Ultra DMA mode is activated (unlike MultiWord DMA modes) the device configures itself to perform a CRC check calculation after the data transfer. Ex. 1003 at 90 ("CRC errors are detected and reported only while operating in Ultra mode."). In addition, unlike the MultiWord DMA modes, each Ultra DMA mode utilizes both the rising and falling edge of the clock signal to transfer data and utilizes HDMARDY, DDMARDY, and DSTROBE signals, which are not part of a MultiWord DMA access operation. Ex. 1002 at ¶222-23; Ex. 1003 at 52; Fig. 32 (illustrating the MultiWord DMA transfer initialization process).

Furthermore, each Ultra DMA mode is different. As an example, after a pause in an Ultra DMA data burst, a memory device will be prepared to receive up to two additional data words for Ultra DMA Modes 0-2 and up to three additional data word for DMA Modes 3-5. Ex. 1003 at 70. Finally, each mode is associated with different maximum transfer rates. *Id.* at Tables 21-22; Ex. 1002 at ¶222-23.

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These DMA modes are access profiles because use of each DMA Mode

requires the use of a specific DMA *protocol*, not merely the selection of particular

timing characteristics. Ex. 1003 at 68 ("[T]he *Ultra DMA protocol* shall be used

instead of the *Multiword DMA protocol.…* This protocol applies to the Ultra DMA

data burst only."). *See* Ex. 1007 at 266-67. Moreover, in the example of Ultra

DMA, "[s]everal signal lines are redefined to provide different functions during an

Ultra DMA burst." *Id.* at 68.

Each MultiWord and Ultra DMA mode is effective for determining access

configuration for a usage. The "usage" in *CompactFlash* relates to the host

activity in accordance with the selected DMA mode (*e.g.*, a READ DMA or

WRITE DMA operation). *Id.* Specifically, the controller configures the

CompactFlash device for a host-initiated access operation according to the host-

selected DMA mode. *Cf.* Ex. 1003 at Fig. 32 *with id.* at Figs. 32, 38 (illustrating

the difference in initialization process between a MultiWord DMA transfer and an

Ultra DMA transfer). For example, enabling an Ultra DMA mode causes the

controller to initiate the Ultra DMA protocol (rather than the MultiWord DMA

protocol) when receiving a READ DMA or WRITE DMA command from the host.

Id. at 68. Similarly, enabling a MultiWord DMA mode causes the controller to

initiate the MultiWord DMA protocol (rather than the Ultra DMA protocol) when

receiving a READ DMA or WRITE DMA command from the host. *Id.* at 68.

Furthermore, unlike the Patent Owner's argument in the Prosecution History that changing the operating speed does not affect an access operation, the DMA modes ***directly affect*** access operations. *See* Ex. 1007 at 266-67. The selected DMA mode dictates the specific DMA protocol that the memory device utilizes. Moreover, the selection of an Ultra DMA profile rather than a MultiWord DMA profile requires the device to perform a CRC comparison to ensure the accuracy of the data transferred. Ex. 1003 at 90 ("CRC errors are detected and reported ***only while operating in an Ultra mode***.") (emphasis supplied); Ex. 1002 at ¶222.

The predefined profiles are stored in the card and are available via the "IDENTIFY DEVICE data [which] indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting." Ex. 1003 at 69, 128

Table 47: Identify Device Information

Word Address	Default Value	Total Bytes	Data Field Type Information
			***
63	0X0Xh	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected

("Table 47 specifies ... data returned by the Identify Device Command"), 132-33.

The IDENTIFY DEVICE data also indicates support of certain MultiWord DMA

modes. *Id.* at 132-33.

For instance, Word 88 of the Identify Device Information "identifies the

Ultra DMA transfer modes supported by the device and indicates the mode that is

currently selected." *Id* at 137. This data is stored in a portion of memory (i.e., a

register) in the device, and is made available to the host via a "buffer" (i.e.,

register), which the host can access, in response to an IDENTIFY DEVICE

command. Ex. 1002 at ¶216; Ex. 1003 at 128 ("The parameter words in the buffer

have the ... meanings defined in Table 47[.]").

Moreover, when the host selects a supported profile, the selected access

profile is stored in a register in the CompactFlash device. Ex. 1002 at ¶¶212-217.

For example, the host may use the "Set transfer mode subcommand" (designated

"Feature 03h") which is part of the "SET FEATURES" command to "select the

Ultra DMA mode at which the system operates." Ex. 1003 at 69, 156-58. When

invoking this subcommand, the selected MultiWord or Ultra DMA mode is

identified by storing a value corresponding to the selected access profile "in the

Sector Count register." Ex. 1003 at 157 (emphasis added).

> **(iii)** <u>**a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles; and**</u>

CompactFlash has a CompactFlash controller, which receives a SET FEATURES command from the host. *See* Ex. 1003 at Fig. 1 (shown below); Ex. 1002 at ¶¶226-27. The SET FEATURES command is communicated from the host to the CompactFlash controller to select and activate one of the MultiWord or Ultra DMA modes (*i.e.*, a predefined access profile) from among the available modes supported by the device. Ex. 1003 at 15, 156-58, Table 53 (indicating bits representing a host-selected DMA mode) (shown below). Specifically, the SET FEATURES command instructs the controller to set the DMA mode to the selected MultiWord DMA mode or Ultra DMA mode for subsequent DMA access operations (*i.e.*, the usage), such as READ DMA and WRITE DMA. *Id.* at 15, 157-58.

Figure 1: CompactFlash Storage Card Block Diagram
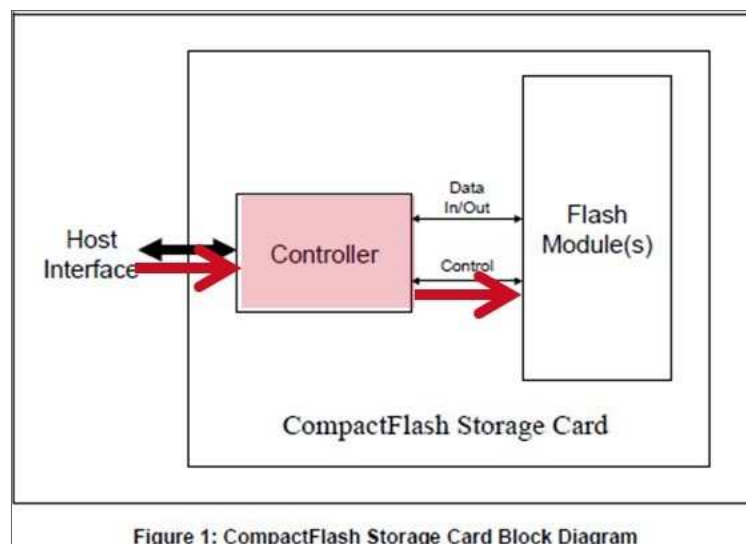
Id. at Fig. 1 (annotated).

Table 53: Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode
Reserved	00010b	N/A
Multiword DMA mode	00100b	Mode
Ultra DMA Mode	01000b	Mode
Reserved	10000b	N/A
Mode = transfer mode number		

Id. at Table 53 (annotated).

For example, for Ultra DMA modes, the Set transfer mode subcommand

(using the transfer mode values in Table 53) in the SET FEATURES command

allows "a host to select the Ultra DMA mode at which the system operates." *Id.* at

69. Thus, *CompactFlash* discloses this element. Ex. 1002 at ¶¶226-27.

> **(iv)** **receive at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage**.

CompactFlash teaches the CompactFlash controller receiving a READ

DMA or WRITE DMA command (*i.e.*, a second command) to configure access to

the memory device for a read or write operation in accordance with the activated

MultiWord or Ultra DMA mode (*i.e.*, a predefined access profile). Ex. 1003 at 52.

Ex. 1002 at ¶¶228-34. As noted above, the configuration of the memory device,

including the protocol used to carry out the READ DMA or WRITE DMA

command, will depend on which DMA mode was previously set by the host. Ex.

1003 at 68 (noting that when the Ultra DMA protocol is enabled, it is "used instead

of the Multiword DMA protocol" when the "READ DMA, and WRITE DMA

commands" are "issued by the host"); *see supra* Section VIII.A.

After a host communicates a READ DMA or WRITE DMA command

following the selection of a DMA mode, the controller will begin the DMA-

specific initiation protocol to configure access to a portion of the memory device

(*i.e.*, the readable and writeable area for the memory device) for either a

MultiWord DMA transfer or an Ultra DMA transfer in the selected mode.

Ex. 1003 at Figs. 32-33, 38. Specifically, the controller configures the

CompactFlash device to perform a DMA transfer under the selected DMA mode

on specified memory sectors in the CompactFlash memory (*i.e.*, a portion of the

memory device). *Id.* at 145 ("[The Read DMA] command uses DMA mode to

read from 1 to 256 sectors as specified in the Sector Count register.... The transfer

begins at the sector specified in the Sector Number Register"), 164 ("[The Write

DMA] command uses DMA mode to write from 1 to 256 sectors as specified in the

Sector Count register.... The transfer begins at the sector specified in the Sector

Number Register."); Ex. 1002 at ¶¶229-30. Immediately following the

configuration of the device, a data transfer will occur between the host and the

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memory device under the host-activated MultiWord or Ultra DMA mode.

Ex. 1003 at 68-83, Figs. 32, 33, 38; Ex. 1002 at ¶232.

In a MultiWord DMA mode, the controller starts the initiation phase of the

MultiWord DMA burst by asserting a DMARQ signal (Step 1 of Fig. 32). The

host, in response, asserts a DMACK signal (Step 2 of Fig. 32), and, in turn, the

controller response by asserting the IORD signal (Step 3 of Fig. 32).

Figure 32: True IDE Multiword DMA Mode Read/Write Timing Diagram
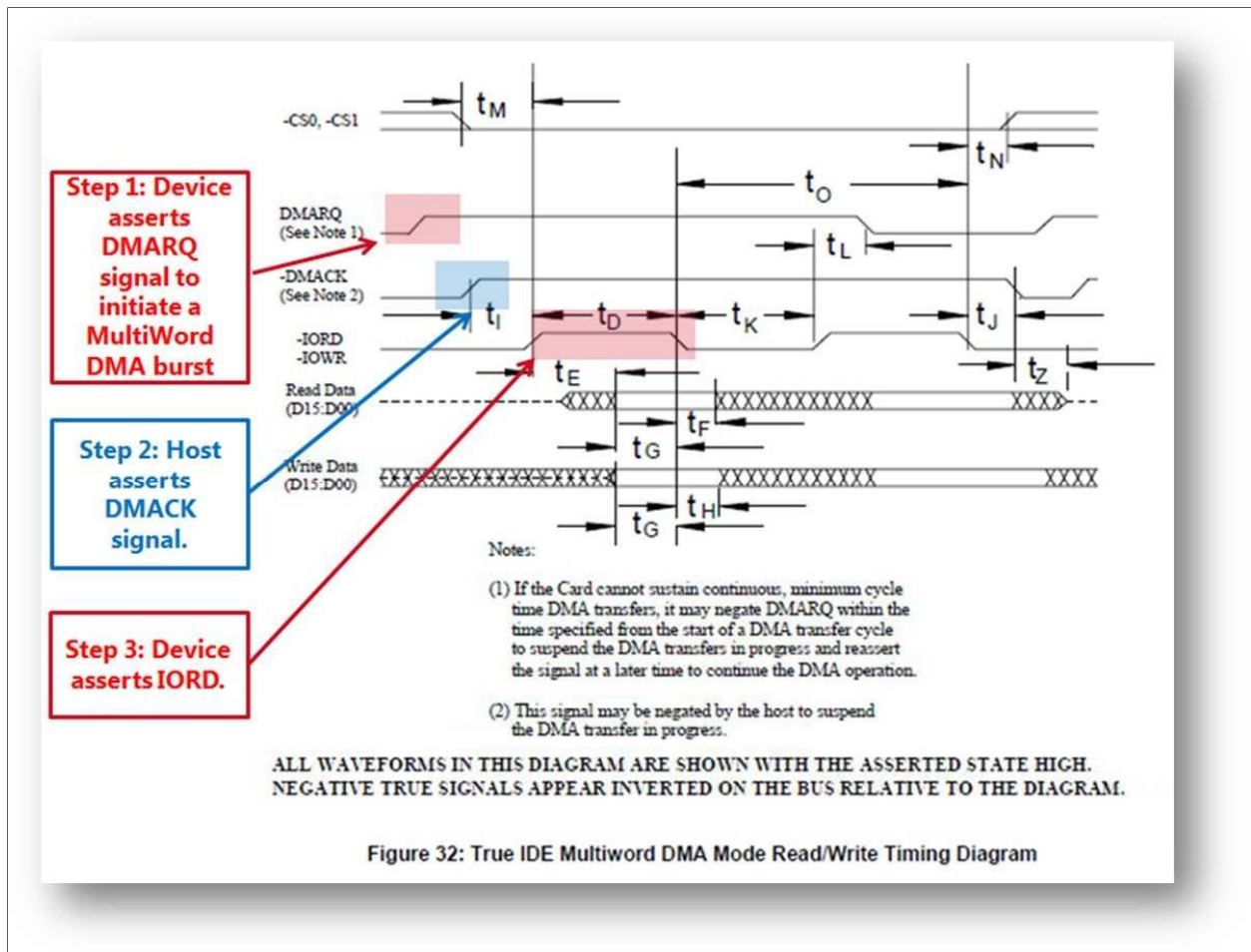
Ex. 1003 at Fig. 32 (annotated).

As another example, when an Ultra DMA mode is activated, the controller

starts the initiation phase of the Ultra DMA burst by asserting a DMARQ signal

(Step 1 of Fig. 33). *Id.* at 76. The host then asserts a DMACK signal (Step 2 of

Fig. 33). *Id.* at Fig. 33. Only at that point do the other signal lines become

effective, permitting the transfer. *Id.* ("The definitions for the …DSTROBE… and

- IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are

asserted). The device will assert a DSTROBE signal line to start the data-in burst

(Step 3 of Fig. 33). *Id.* at Fig. 33.

Figure 33: Ultra DMA Data-In Burst Initiation Timing
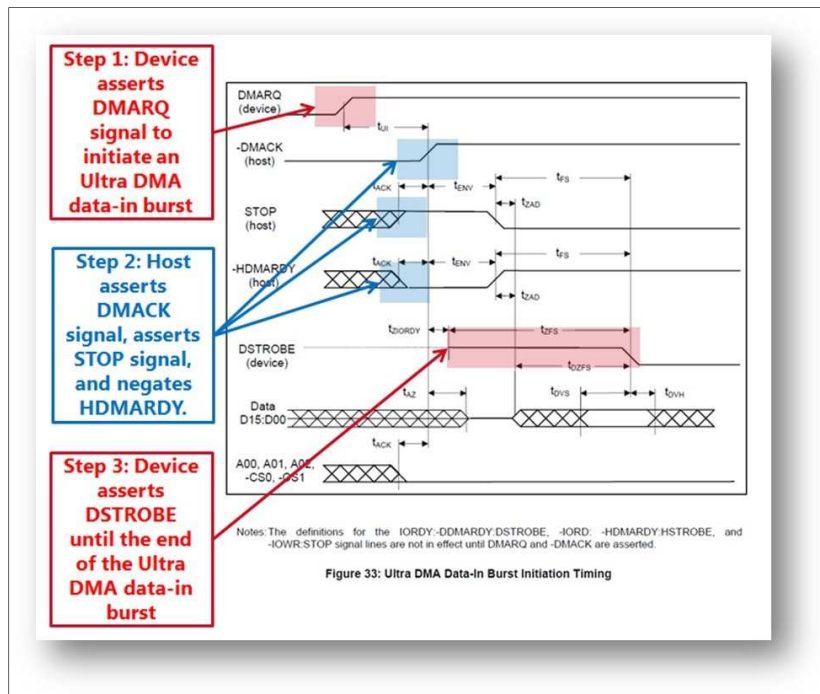
Id. at Fig. 33 (annotated).

For a data-out burst, the device will wait to negate any signal until

generating a STROBE edge (*see* Step 3 of Fig. 38). *Id.* at 70. At this point, the

memory device is now configured for usage (*i.e.*, to perform a data transfer under

the selected Ultra DMA mode).

Figure 38: Ultra DMA Data-Out Burst Initiation Timing
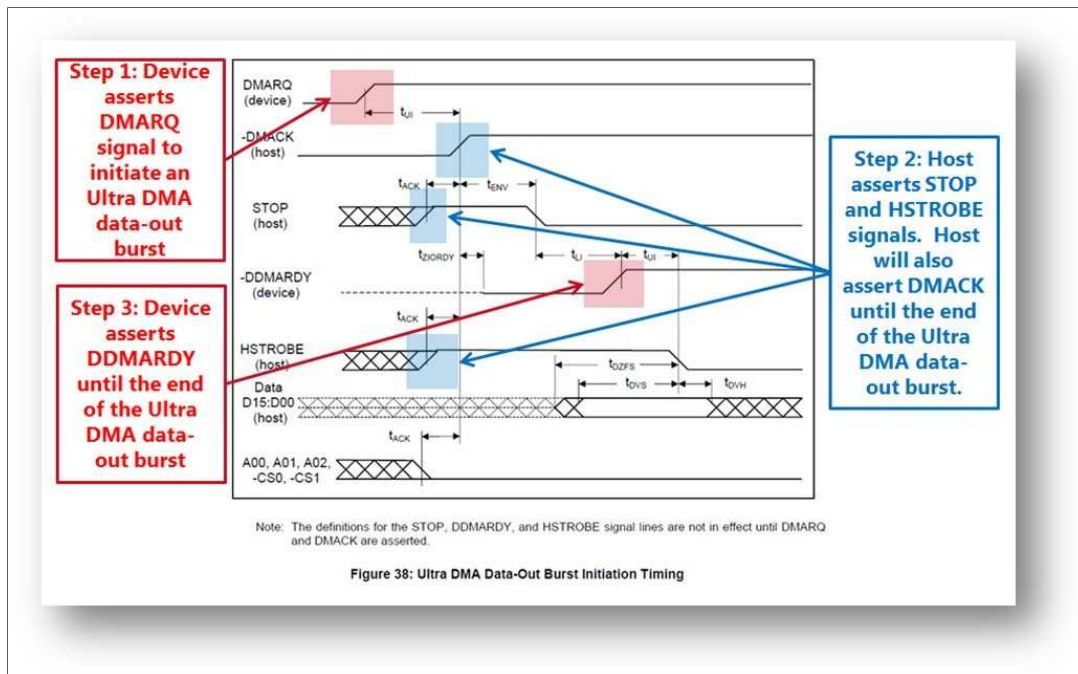
Id. at Fig. 38 (annotated).

Finally, as opposed to a READ SECTOR and WRITE SECTOR command

in *CompactFlash* that causes the CompactFlash device to only perform a data

transfer, the READ DMA and WRITE DMA command causes the CompactFlash

device to first configure the memory device and then perform a data transfer. After

receiving a READ SECTOR or WRITE SECTOR command, the host specifies the

memory sectors for the data transfer and the CompactFlash device performs the

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data transfer on the specified memory sectors. *Id.* at 148; Ex. 1002 at ¶¶233-34.

On the other hand, after receiving a READ DMA and WRITE DMA command, the

CompactFlash controller must first configure the CompactFlash device for a DMA

transfer and only then may the CompactFlash device perform the DMA transfer.

Ex. 1003 at 68-83, Figs. 32, 33, 38; Ex. 1002 at ¶233.

2. Dependent Claims 3, 12

(i) **The memory device of claim (1, 10) wherein at least one of the one or more predefined access profiles comprises a default access profile**.

When executing a power-on or hardware reset, *CompactFlash* discloses that

the device may revert to a default non-Ultra DMA mode, like a MultiWord DMA

mode. Ex. 1003 at 69. As discussed above, each MultiWord DMA mode may be

an access profile. Ex. 1002 at ¶¶218-25; *see supra* IX.A.1(ii).

3. Dependent Claim 9

(i) **The memory device of claim 1, wherein the one or more registers comprise a plurality of registers for storing a plurality of the predefined access profiles**.

As discussed above, each DMA mode is a predefined access profile.

Consequently, *CompactFlash* discloses a plurality of predefined access profiles as

each MultiWord and Ultra DMA Mode is a predefined access profile that are

stored. Ex. 1003 at 137, 132-33, 158; *see supra* IX.A.1(ii).

4. Independent Claim 10

(i) (Preamble) A memory device comprising:

See Section above at IX.A.1(i).

(ii) one or more predefined access profiles to determine how access to the memory device is configured for at least one usage of the memory device;

See Section above at IX.A.1(ii).

(iii) a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles associated with the memory device; and

See Section above at IX.A.1(iii).

(iv) receive at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.

See Section above at IX.A.1(iv).

5. Independent Claim 19

(i) (Preamble) A method comprising:

CompactFlash discloses a method for improvements to direct memory access (DMA) data transfer. Ex. 1014 ("Ultra DMA 33 and UltraDMA66 [sic] interface modes will increase the CompactFlash interface data transfer rate to 66 MB/sec.").

> **(ii)** **receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device, the one or more predefined access profiles stored in one or more registers**,

See Section above at IX.A.1(ii) –(iii).

> **(iii)** **the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and**

See Section above at IX.A.1(ii).

> **(iv)** **receiving at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage**.

See Section above at IX.A.1(iv).

6. Dependent Claim 21, 30

> **(i)** **The method of claim (19, 28), wherein at least one of the one or more predefined access profiles comprises a default access profile**.

See Section above at IX.A.2.

7. Dependent Claim 27

> **(i)** **The method of claim 19, wherein the one or more registers comprise a plurality of registers for storing a plurality of the predefined access profiles**.

See Section above at IX.A.3.

8. **Independent Claim 28**

(i) **(Preamble) A method comprising**:

See Section above at IX.A.5(i).

(ii) **receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device**,

See Section above at IX.A.1(iii).

(iii) **the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and**

See Section above at IX.A.1(ii).

(iv) **receiving at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the one or more predefined access profiles for the at least one usage**.

See Section above at IX.A.1(iv).

B. **GROUND 2: Claims 1, 3, 9, 10, 12, 19, 21, 27, 28, and 30 are unpatentable under 35 U.S.C. § 103(a) over *Ziv* and *Vogt***

As shown below, *Ziv* and *Vogt* render obvious Claims 1, 3, 9, 10, 12, 19, 21, 27, 28, and 30 of the '850 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶253-314.

1. **Independent Claim 1**

(i) **(Preamble)A memory device comprising**:

Ziv discloses a memory device, such as a portable storage device that

includes storage memory. Ex. 1004 at 3:48-55, Fig. 2; Ex. 1002 at ¶264.
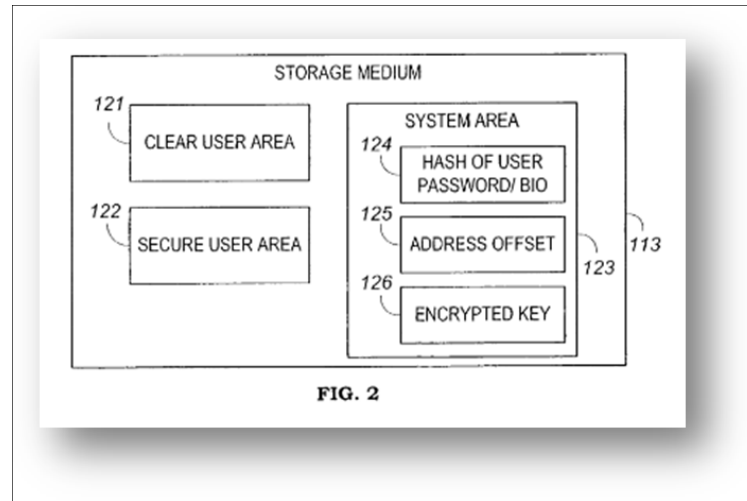
Id. at Fig. 2.

(ii) **one or more registers to store one or more predefined access profiles associated with the memory device, the one or more predefined access profiles used to determine how access to the memory device is configured for at least one usage; and**

Ziv discloses a predefined access profile that contains a password hash, an

address offset, and a key, which are predefined. Ex. 1004 at 5:1-25 (describing

initial setup); Ex. 1002 at ¶¶265-71. The password hash, address offset, and key in

Ziv constitutes a predefined access profile that determines how access to the

memory device is configured for the host's access to the secure memory area (*i.e.*,

the usage). *See* Ex. 1004 at 1:60-63. The password hash, address offset, and key

are each stored in registers (as illustrated in Fig. 2). Ex. 1004 at 4:16-20, Fig. 2.
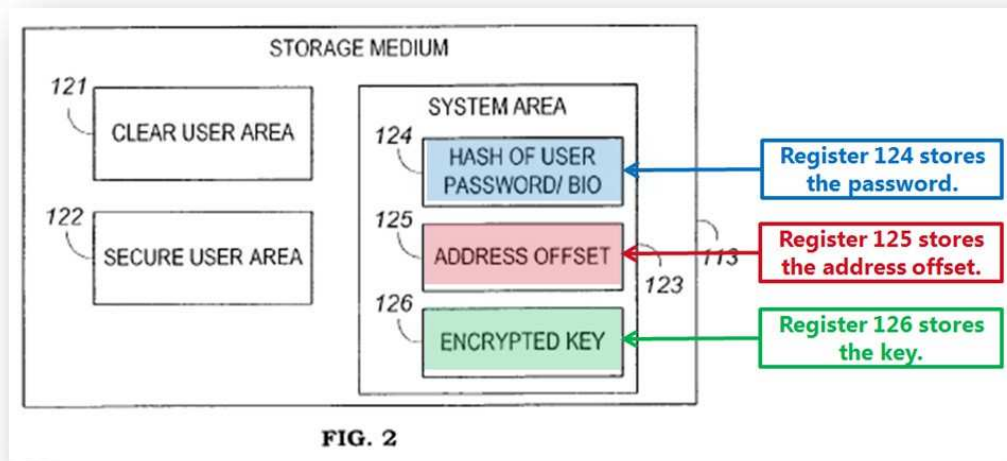
FIG. 2

Id. at Fig. 2 (annotated).

The password hash, address offset, and key in *Ziv* constitutes a predefined

access profile that governs the access operations to the memory. *See* Ex. 1001 at

3:56-58 ("***This profile***, which may be any one of the supported predefined profiles,

governs the current access operations to the memory device.") (emphasis

supplied). Additionally, each of these components individually forms an access

profile. Ex. 1002 at ¶¶265.

Access to the secure user data is only available when a hash of an entered

password matches the password hash stored in the register. Ex. 1004 at 4:11-12

("[A] secure area 122 that contains secure user data [is] accessible only upon the

provision of a password[.]"). In addition, the address offset governs access

operations to the memory. After entering the proper password, the memory device

uses the stored address offset to properly view the secure memory area. *Id.* at

6:46- 48 ("[H]ost 101 will seek 'sector 0' of the remounted device, controller 111

will use offset 125B to point at 'sector 0-B' 406[.]"). Without the address offset,

the secure area will not be properly mounted. *Id.*; Ex. 1002 at ¶267.
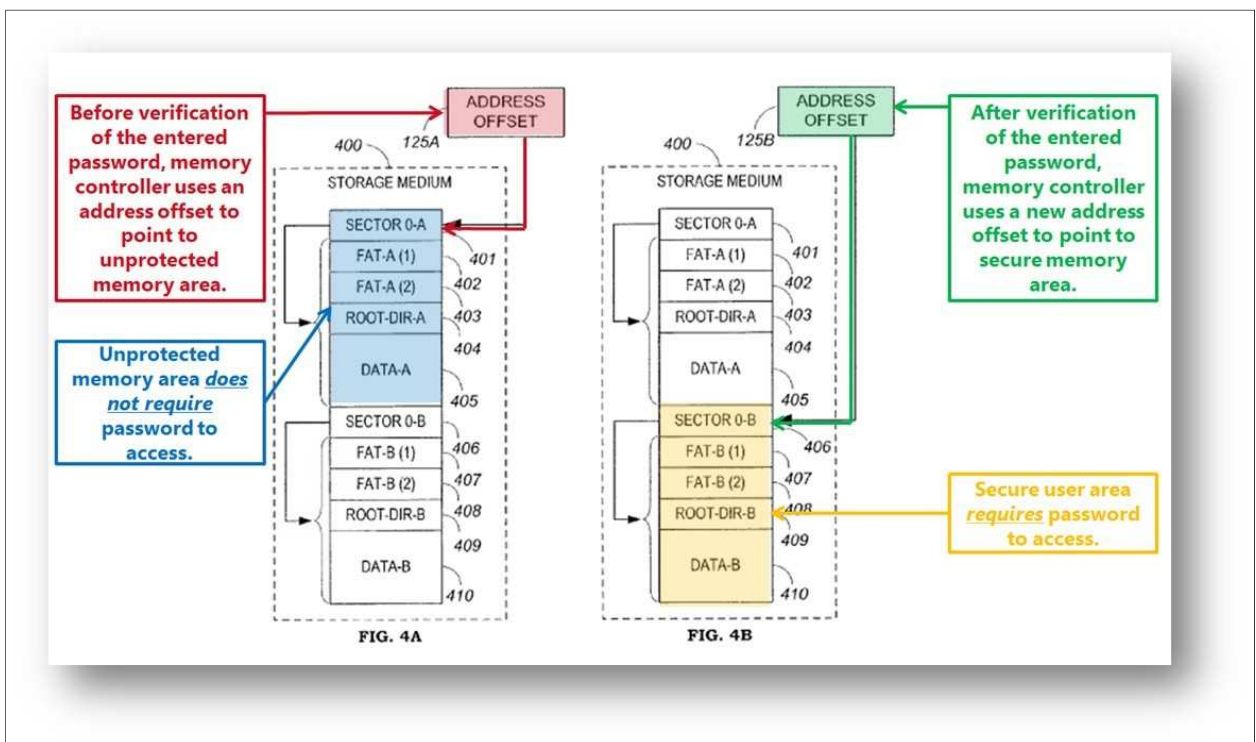
Ex. 1004 at Fig. 4A-4B (illustrating the use of the address offset to access the

secure area) (annotated).

Moreover, the key governs the access operations to the memory. The key is

the "permanent encryption key for all data stored in the secure memory." *Id.* at

7:7-9. Without the key, a user cannot read or write to the secure area. *Id.* at 7:7-9;

7:36-46 (instructing the controller to decrypt data being read from and encrypt data

being written to the secure memory area using the key); Fig. 10 (shown below);

Ex. 1002 at ¶268.
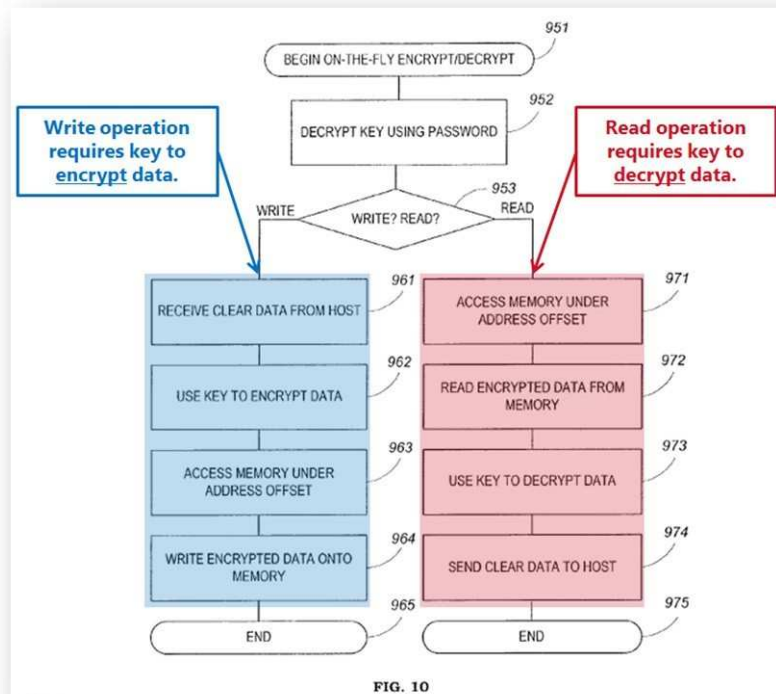
FIG. 10

Ex. 1004 at Fig. 10 (annotated).

(iii) <u>a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles; and</u>

Ziv discloses a controller (microprocessor) in the memory device that

receives a command indicating the password entered to gain access the secure area.

Ex. 1004 at 6:42-44 ("*[C]ontroller 111* dismounts and remounts portable storage

device 110[.]") (emphasis supplied). A POSITA would understand the

microprocessor in *Ziv* to be a controller. Ex. 1002 at ¶273. *Ziv* further discloses

that a password entry from the host triggers several activation procedures

associated with the predefined access profile.
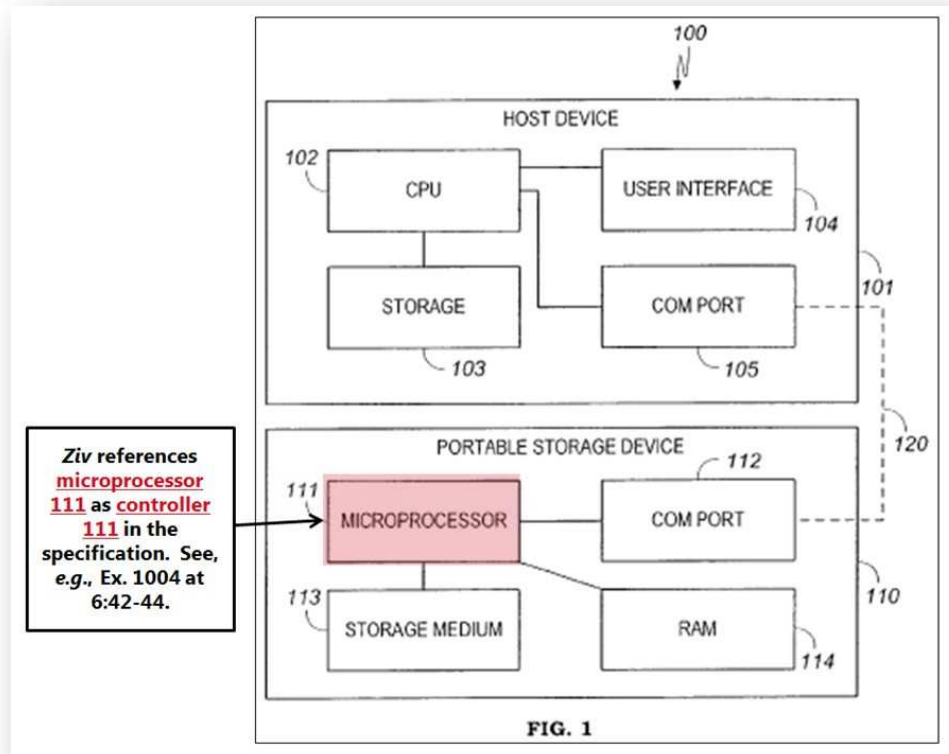
FIG. 1

Ex. 1004 at Fig. 1 (annotated).

The controller receives a command indicating the password entered. *Id.* at

6:19-30 ("If the password has been entered ... via user interface 104, then in step

702 this password is moved to microprocessor 111.... [T]he hashed entered

password is then compared to the hashed stored password in register 124."), Fig. 1

(below). In other words, the host system instructs (*i.e.,* sends a command to) the

controller (microprocessor) to use the entered password to gain access to the secure

memory area. Ex. 1002 at ¶274.
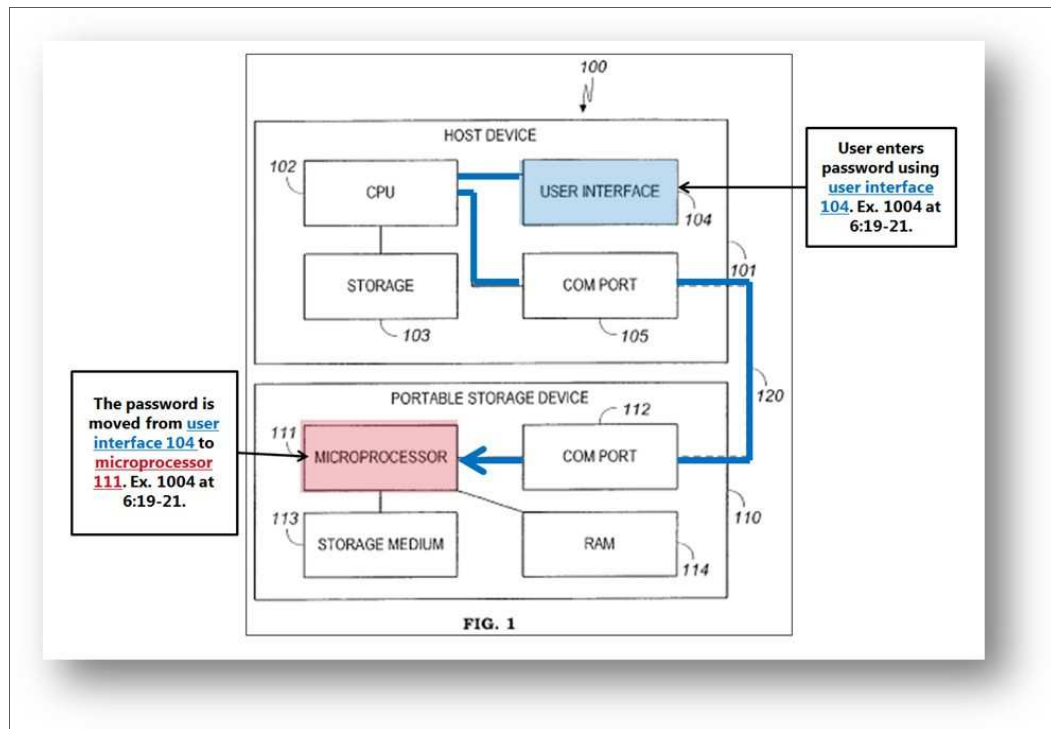
Ex. 1004 at Fig. 1 (annotated).

The entered password in *Ziv* activates a comparison of a hash of the entered

password with the stored password hash. Ex. 1004 at 6:28-30; Ex. 1002 at ¶277.

Additionally, the password in *Ziv* activates the decryption of the stored key.

Ex. 1002 at ¶278. When the entered password matches the stored password, the

microprocessor decrypts the key of the predefined access profile. Ex. 1004 at

7:32- 35.

The communication of a proper password also activates the remounting of

the memory according to the address offset. Ex. 1002 at ¶279. After remounting,

the stored address offset is used to point to the secure memory area. Ex. 1004 at

6:44-46 ("[W]hen remounting device 110, controller 111 will use an address

offset[.]").

If the Board disagrees that *Ziv* teaches a "command," it would have been

obvious nevertheless to use the command-based password authentication method

in *Vogt* in the memory device of *Ziv*. In particular, *Vogt* discloses a "password

verify" command that communicates the entered password to the flash device, like

a MMC card. Ex. 1005 at 6:36-38 ("The OS sends a 'password verify' command

to the flash. ***The command*** ... ***includes the entered password***.") (emphasis

supplied). The "password verify" command instructs the internal processor to

"compare[] the entered password with the stored password value." *Id.* at 6:30-32.

Moreover, the "password verify" command in the *Ziv-Vogt* combination

activates the predefined access profile for substantially similar reasons as discussed

above. *Id.* at 6:30-32; Ex. 1002 at ¶276.

It would have been obvious to combine the teachings of *Ziv* and *Vogt* to

form a memory controller that receives the "password verify" command in *Vogt*

for the following reasons. Ex. 1002 at ¶¶253-263.

Simple Substitution of One Known Element for Another

Ziv's memory device differs from the claimed device at most by the command element. Ex. 1002 at ¶254. Commands were well-known in the art to be a fundamental approach to communicating information, such as a password, between devices. *Id.*; Ex. 1005 at 6:36-38. A POSITA could have substituted one known element (a controller receiving a password) for the other (a controller receiving a command containing the password) and the results would have been predictable (a controller receiving a command containing the password). Ex. 1002 at ¶¶255-57.

Moreover, those predictable results would have included the known advantages of *Ziv*'s memory device, which provides access to a secure memory area, and the known advantages of a command, which include reliably and efficiently communicating a password from the host system to memory device. Ex. 1004 at 6:19-23; Ex. 1005 at 3:23-24; Ex. 1002 at ¶¶257-58.

Analogous Art

A POSITA would have been motivated to look to the teachings of the prior art due to the similar field, technology, and time frame of *Vogt* and *Ziv*. Ex. 1002 at ¶258. Both patents concern securing data using non-volatile memory in the early 2000s. Ex. 1004 at 3:48-55; Ex. 1005 at 1:13-15; Ex. 1002 at ¶258. In

addition, both patents describe a solution to a similar problem–improving security of portable flash drives using a secure memory and password. Ex. 1004 at 1:60-63 ("[A] portable storage device for securing data stored in the device in a way that will be both convenient and secure."); Ex. 1005 at 2:5-12 ("Techniques for implementing hidden storage in a non-volatile memory storage," where "[t]he hidden storage area cannot be accessed without a valid password.").

Known Technique to a Known Device to Yield Predictable Results

Base system: *Ziv* discloses a memory device, such as a SecureDigital or CompactFlash device, that receives an entered password from the host system. Ex. 1004 at 6:19-30; Ex. 1002 at ¶260.

Known technique: As shown by *Vogt*, receiving a command containing a password was well-known. Ex. 1005 at 6:36-38.

Predictable results and improved system: A POSITA would have recognized that implementing *Vogt*'s structured communication protocol of the "password verify command" in *Ziv*'s memory device would yield the predictable result of a memory device that receives an entered password through a structured command, like the password verify command. Ex. 1002 at ¶262.

As such, using *Vogt*'s password-command implementation of communicating a password was an obvious design choice to implement *Ziv*'s teaching of communicating a password. *Id.* at ¶263.

> **(iv)** <u>**receive at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage**</u>.

The controller in *Ziv* may receive a second command (in the form of a read or write access command) to configure access to the secure memory area in accordance with the password hash, address offset, and key (*i.e.*, predefined access profile). Ex. 1004 at 2:10-12 ("[T]he host device selectably sending data to be written onto the portable storage device and receiving data read from the portable storage device"); 7:35-36 ("In step 953, it is decided whether a read or a write process is required."); Ex. 1002 at ¶281. *See* Ex. 1001 at 5:47-50 (indicating that a second command may indicate an upcoming read or write operation). Using a read or write command, the host ***instructs*** the memory device to read or write to the secure memory area. Ex. 1004 at 2:4-6 ("[A] microprocessor [is] operable to use the clear key to decrypt data read from the secure user area and encrypt data written onto the secure user area."). As shown in Figure 10, the device then enters the appropriate state to process the read or write command (*i.e.*, performing steps 961-965 in the case of a write command, or steps 971-975 in case of a read command). The memory device is then effective for the host to read from or write to the secure memory area (*i.e.*, the usage).

Upon receiving the second command, the memory device is configured to properly read to or write from the secure area. After receiving a read or write access, the microprocessor must point to the proper memory sector in order to access the correct memory to perform the access operation. Ex. 1004 at Fig. 10 (shown below); Ex. 1002 at ¶282.

The microprocessor must also configure the read/write access operations to perform on-the-fly encryption/decryption. When accessing the secure memory area, the microprocessor must apply the encryption key to properly read from and/or write to the secure memory area. Ex. 1004 at 7:35-46, Fig. 10 (shown below); Ex. 1002 at ¶283. Erase operations, however, will not require on-the-fly encryption/decryption. Ex. 1002 at ¶283.
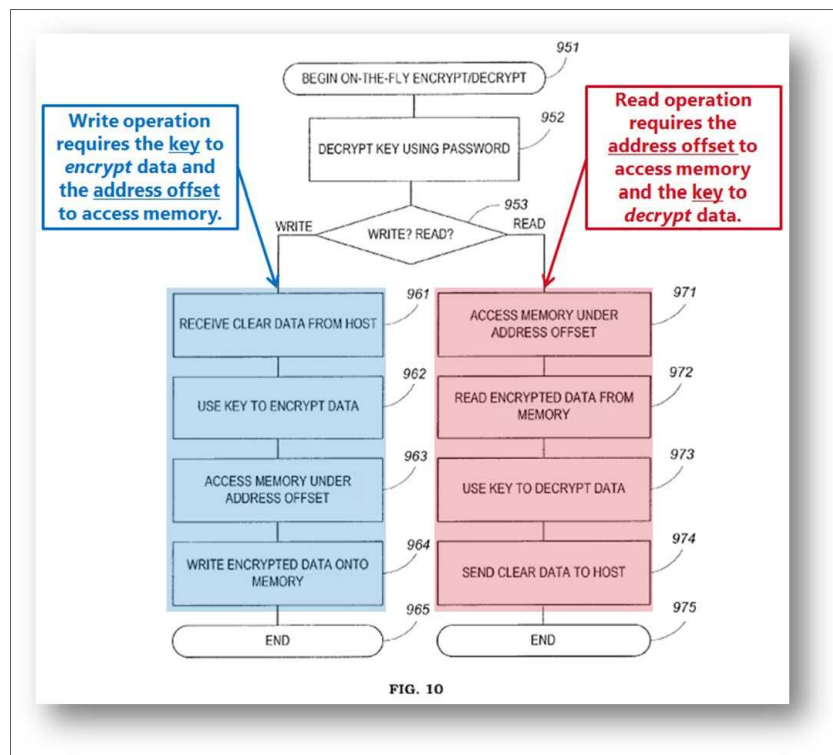
FIG. 10

Ex. 1004 at Fig. 10 (annotated).

After encrypting/decrypting the data and pointing to the proper memory address, a portion of the memory device (*i.e.*, secure area) is now configured according to the usage (*i.e.*, the host reading from or writing to the secure memory area).

Alternatively, *Vogt* discloses a configuration that occurs in accordance with a predefined access profile (*i.e.*, password) after receiving a read/write command (*i.e.*, a second command). Upon receiving a memory read or write signal that attempts to access a hidden storage area address, the controller configures the memory device to create a hidden storage read or write signal. Ex. 1005 at 3:45-

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4:6; 4:7-10; Ex. 1002 at ¶¶284-86. To create the hidden storage read/write signal, a Valid_HS_Access signal that accounts for a previously-entered, valid user password for the password-protected hidden storage area is logically "ANDed" with the received memory read/write signal. Ex. 1005 at 3:45-4:10. Moreover, in a read operation accessing a hidden storage, the controller configures the memory device to uniquely transfer data to a "hidden storage bus out" before transferring the data to an external data bus. *Id.* at 5:24-28.

Accordingly, the controller in *Vogt* configures a portion of memory accessed by the hidden read/write signal to properly perform the access operation to the hidden storage (*i.e.*, the usage) in accordance with the host-entered password (*i.e.*, predefined access profile).

In addition to the reasons to combine *Ziv* and *Vogt* described *supra* in Section IX.B.1(iii), a POSITA would have readily combined the read/write process for a hidden storage in *Vogt* with the read/write process in *Ziv* and seen benefits in doing so. Ex. 1002 at ¶258. *Vogt* discloses the "benefit from inclusion of security primitives in flash memory", confirming the desirability of combining *Vogt* with systems, such as *Ziv*, that involve secure access to data in a memory device. Ex. 1005 at 2:32-35; Ex. 1002 at ¶259. Moreover, a POSITA would look to implement *Vogt*'s known technique of allowing authorized access to password-protected areas to similarly improve the known memory device in *Ziv* that

performs access operations to a password-protected secure area. Ex. 1004 at 2:14-16; Ex. 1005 at 2:25-28; Ex. 1002 at ¶¶262-63.

2. Dependent Claims 3, 12

(i)   **The memory device of claim (1, 10) wherein at least one of the one or more predefined access profiles comprises a default access profile.**

The *Ziv-Vogt* combination discloses the memory device of Claim 1 as discussed above in Section IX.B.1. Furthermore, the *Ziv-Vogt* combination discloses the memory device of Claim 10 as discussed below in Section IX.B.4.

Ziv comprises a default access profile (*i.e.,* access to the clear user area) that is used to set up the memory device upon power up. Ex. 1004 at 6:2-4 ("By default, microprocessor 111 uses an address offset of zero, thus the host sees clear user area 121[.]"). The access to the clear user area does not require entry of a password. *Id.* at 6:4-7.

3. Dependent Claim 9

(i)   **The memory device of claim 1, wherein the one or more registers comprise a plurality of registers for storing a plurality of the predefined access profiles**.

The *Ziv-Vogt* combination discloses the memory device of Claim 1 as discussed above in Section IX.B.1.

Ziv discloses a plurality of predefined access profiles: (1) a default access profile (*i.e.*, access to the clear user area) that is used to set up the memory device

upon power up; and (2) a secure access profile (*i.e.*, password, address offset, and

key) that accesses the secure area (as discussed above in Section IX.B.1). *See* Ex.

1004 at 6:2-4 ("By default, microprocessor 111 uses an address offset of zero, thus

the host sees clear user area 121 via 'sector 0-A.'"); Figs. 4A-4B (shown below);

supra Section IX.B.1
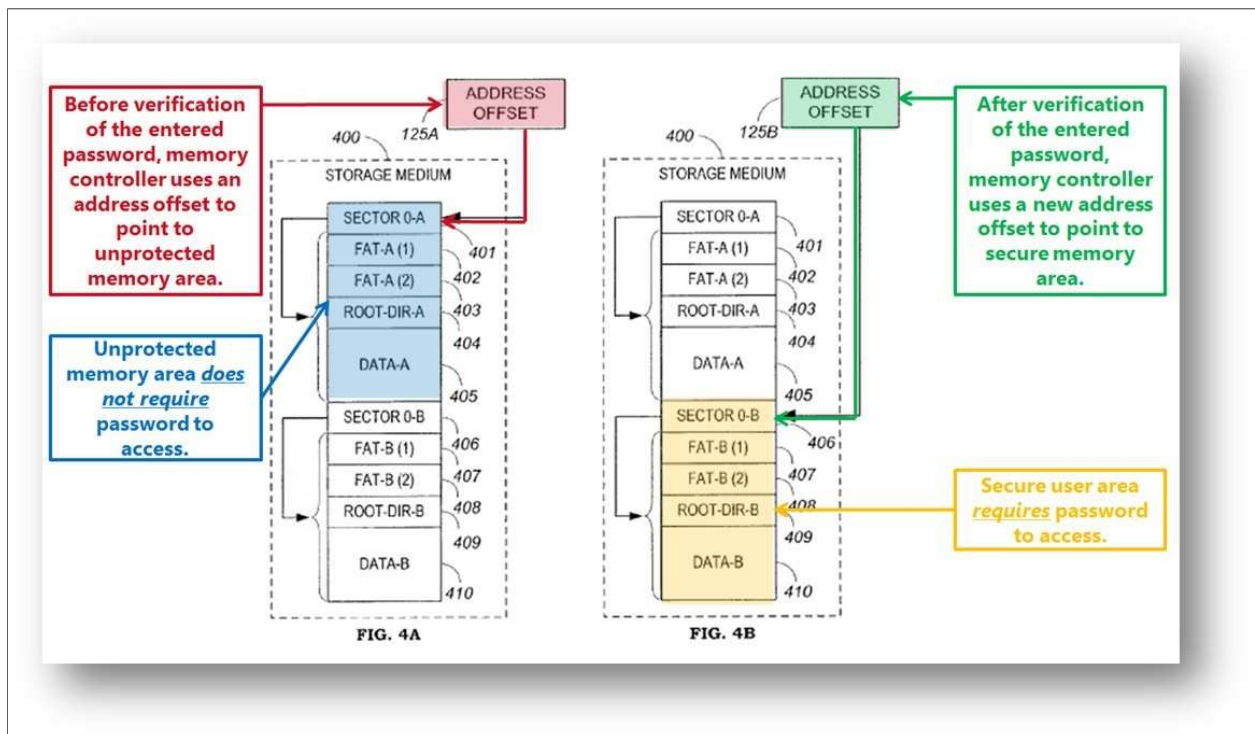
Ex. 1004 at Figs. 4A-B (annotated).

4. Independent Claim 10

(i) (Preamble) A memory device comprising:

See Section above at IX.B.1(i).

      (ii)   **one or more predefined access profiles to determine how access to the memory device is configured for at least one usage of the memory device;**

See Section above at IX.B.1(ii).

      (iii)   **a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles associated with the memory device; and**

See Section above at IX.B.1(iii).

      (iv)   **receive at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.**

See Section above at IX.B.1(iv).

     5.   **Independent Claim 19**

     (i)   **(Preamble) A method comprising:**

Ziv discloses at least a method for securing data on a portable storage device.

Ex. 1004, *Title* and *Abstract*.

      (ii)   **receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device,**

See Section above at IX.B.1(ii)-(iii).

> **(iii)** <u>the one or more predefined access profiles stored in one or more registers, the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and</u>

See Section above at IX.B.1(ii).

> **(iv)** <u>receiving at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.</u>

See Section above at IX.B.1(iv).

6. <u>Dependent Claim 21, 30</u>

> **(i)** <u>The method of claim (19, 28), wherein at least one of the one or more predefined access profiles comprises a default access profile.</u>

The *Ziv-Vogt* combination discloses the method of Claim 19 as discussed above in Section IX.B.5. Furthermore, the *Ziv-Vogt* combination discloses the method of Claim 28 as discussed below in Section IX.B.8.

See Section above at IX.B.2.

7. <u>Dependent Claim 27</u>

> **(i)** <u>The method of claim 19, wherein the one or more registers comprise a plurality of registers for storing a plurality of the predefined access profiles.</u>

The *Ziv-Vogt* combination discloses the method of Claim 19 as discussed above in Section IX.B.5.

See Section above at IX.B.3

8. Independent Claim 28

(i) (Preamble) A method comprising:

See Section above at IX.B.5(i).

(ii) receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device,

See Section above at IX.B.1(iii).

(iii) the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and

See Section above at IX.B.1(ii).

(iv) receiving at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the one or more predefined access profiles for the at least one usage.

See Section above at IX.B.1(iv).

C. GROUND 3: Claims 4, 13, 22, and 31 are unpatentable under 35 U.S.C. § 103(a) over *Ziv*, *Vogt*, and *eMMC*

As shown below, *Ziv*, *Vogt*, and *eMMC* render obvious Claims 4, 13, 22, and

31 of the '850 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶315-322.

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1. Dependent Claims 4 and 13

(i) The memory device of claim (1, 10), wherein the memory device comprises an embedded MultiMedia Card (eMMC) device.

Ground 2 in Section IX.B.1 and IX.B.4 applies *Ziv* and *Vogt* to independent Claims 1 and 10. Embedded MultiMedia Card devices were disclosed in eMMC. Ex. 1016.

Additionally, *Vogt* discloses embedding the flash memory within a device (*e.g.*, cell phone). *See* Ex. 1005 at 2:32-42. The "flash memory is ***embedded*** in the device, and cannot be easily reset or replaced." *Id.* at 11:16-19 (emphasis added).

A POSITA would combine the flash memory device in *Vogt* and/or eMMC with the storage medium described in *Ziv* and would see benefits in doing so. Ex. 1002 at ¶316. The flash memory device in eMMC and *Vogt* is a desirable type of storage medium that a skilled artisan would implement in the memory device in *Ziv* as an obvious design choice. Ex. 1002 at ¶317. For instance, eMMC specifically suggests that eMMC was a "versatile" technology and that embedding such a device in a host would give the host "access to all major classes of mass storage memory subsystems," making the "system architecture more flexible than that based upon other memory card-only standards." Ex. 1016. eMMC also notes that employing an eMMC device would make "it easy to embed" storage on a host system and would keep "technology complexity ... invisible to the host." Ex. 1016.

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Similarly, *Vogt* discloses the "benefit from inclusion of security primitives in flash memory," further confirming the desirability of combining *Vogt* with systems, such as *Ziv*, that involve secure access to data in a memory device. Ex. 1005 at 2:32-35.

Lastly, because the flash memory in *Vogt* suggests using a MMC card as the flash device, a POSITA would further understand that *Vogt*'s disclosure of "flash memory [that] is embedded in the device" is an embedded MMC (eMMC). Ex. 1002 at ¶¶315-38; Ex. 1005 at 11:16-19; Ex. 1016.

2. Dependent Claims 22 and 31

(i) The method of claim (19, 28), wherein the memory device comprises an embedded MultiMedia Card (eMMC) device.

Ground 2 in Section IX.B.5 and IX.B.8 applies *Ziv* and *Vogt* to independent Claims 19 and 28.

See Section above at IX.C.1(i).

D. GROUND 4: Claims 2, 11, 20, and 29 are unpatentable under 35 U.S.C. § 103(a) over *CompactFlash* and *Elhamias*

As shown below, *CompactFlash* and *Elhamias* render obvious Claims 2, 11, 20, and 29 of the '850 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶323-328.

1. Dependent Claim 2, 11

(i) The memory device of claim (1, 10) wherein the at least one first command activates two or more of the predetermined access profiles in parallel.

Ground 1 in Sections IX.A.1 and IX.A.4 applies *CompactFlash* to independent Claims 1 and 10. Non-volatile memory cards were disclosed in *Elhamias*. Ex. 1006 at ¶22.

Additionally, *Elhamias* discloses that a memory device may include predetermined access profiles that are activated in parallel. Ex. 1002 at ¶¶330-331. For example, *Elhamias* discloses that the disclosed storage device can utilize "memorize access sequences issued by the host under various predefined conditions, such as host reset or power on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to optimize operation for the expected commands." Ex. 1006 at ¶10. *Elhamias* further discloses that the "SD card 35 contains nine surface electrical contacts 10-18…Contact 12 receives commands (CMD) from the host and sends responses and status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2, DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its non-volatile memory and send data to the host in parallel from the memory. Ex. 1006 at ¶22. Thus, *Elhamias* discloses that

a memory device may include predetermined access profiles that are activated in parallel. Ex. 1002 at ¶¶329-31.

A POSITA would combine the memory device from *CompactFlash*, where the memory device receives commands from one or more predefined access profiles, with a memory card capable of conducting two or more memory access operations in parallel, as in *Elhamias*. Ex. 1002 at ¶¶323-328. Indeed, the memory device in *Elhamias* is a desirable type of storage medium that a POSITA would implement in the memory device of *CompactFlash* as an obvious design choice. Ex. 1002 at ¶324. For example, *Elhamias* specifically suggests that *Elhamias* is "removable non-volatile memory cards [that] include a memory array and a controller that performs as the memory control and the host interface function. These removable cards are plugged into a different of variety of devices[.]" Ex. 1008 at ¶7.

Further, *CompactFlash and Elhamia* are in a similar field, technology, and time frame. Ex. 1002 at ¶325.

Moreover, a POSITA would have especially been motivated to combine *CompactFlash* and *Elhamias*, as there are express motivations in the art for this combination, because *Elhamias* improves the efficiency of data transfer, and *CompactFlash* specifically introduced Ultra DMA modes to improve the efficiency of *CompactFlash* memory devices. Ex. 1002 at ¶326. Similarly, a POSITA would

have recognized that *Elhamias* also provides greater control for the *CompactFlash*

host to order its operations. *Id.* at ¶327. Using the advantages of *CompactFlash* of

performing read and write operations under a well-established standard, a POSITA

would have been motivated by the teachings of *Elhamias* to use host prioritization

of data to gain the advantage of meeting read and write operations in

CompactFlash. Id.

2. Dependent Claim 20, 29

(i) **The method of claim (19, 28) wherein receiving the at least one first command activates two or more access profiles in parallel.**

Ground 1 in Sections IX.A.5 and IX.A.8 applies to *CompactFlash* to

independent Claims 19 and 28.

See Section above at IX.D.1.(i).

E. GROUND 5: Claims 2, 11, 20, and 29 are unpatentable under 35 U.S.C. § 103(a) over *Ziv, Vogt,* and *Elhamias*

As shown below, *Ziv*, *Vogt*, and *Elhamias* render obvious Claims 2, 11, 20,

and 29 of the '850 Patent under 35 U.S.C. § 103. *See also* Ex. 1002 at ¶¶333-45.

1.   **Dependent Claim 2, 11**

(i)   **The memory device of claim (1, 10) wherein the at least one first command activates two or more of the predetermined access profiles in parallel.**

Ground 2 in Section IX.B.1 and IX.B.4 applies to *Ziv* and *Vogt* to independent Claims 1 and 10. Non-volatile memory cards were disclosed in *Elhamias.* Ex. 1006 at ¶22.

Additionally, *Vogt* discloses embedding the flash memory within a device (*e.g.*, cell phone). *See* Ex. 1005 at 2:32-42. The "flash memory is ***embedded*** in the device, and cannot be easily reset or replaced." *Id.* at 11:16-19 (emphasis added).

A POSITA would combine the flash memory device in *Vogt* and/or *Elhamias* with the storage medium described in *Ziv* and would see benefits in doing so. Ex. 1002 at ¶¶333-38, 39. The flash memory device in *Elhamias* and *Vogt* is a desirable type of storage medium that a POSITA would implement in the memory device in *Ziv* as an obvious design choice. Ex. 1002 at ¶333-40. For instance, *Elhamias* discloses that a memory device may include predetermined access profiles that are activated in parallel. For example, *Elhamias* discloses that the disclosed storage device can utilize "memorize access sequences issued by the host under various predefined conditions, such as host reset or power on boot sequence. As the sequence of host commands following these predefined conditions are usually the same, the storage device can use this information to

optimize operation for the expected commands." Ex. 1006 at ¶10. *Elhamias*

further discloses that the "SD card 35 contains nine surface electrical contacts 10-

18…Contact 12 receives commands (CMD) from the host and sends responses and

status signals back to the host. The remaining contacts 10, 11, 17 and 18 (DAT 2,

DAT 3, DAT 0, and DAT 1, respectively) receive data in parallel for storage in its

non-volatile memory and send data to the host in parallel from the memory.

Ex. 1006 at ¶22.

Similarly, *Vogt* discloses the "benefit from inclusion of security primitives in

flash memory", further confirming the desirability of combining *Vogt* with

systems, such as *Ziv*, that involve secure access to data in a memory device.

Ex. 1005 at 2:32-35.

2. **Dependent Claim 20, 29**

(i) **The method of claim (19, 28) wherein receiving the at least one first command activates two or more access profiles in parallel.**

Ground 1 in Sections IX.B.5 and IX.B.8 applies to *Ziv* and *Vogt* to

independent Claims 19 and 28.

See Section above at IX.E.1.(i).

F.   **GROUND 6: Claims 1, 3, 9, 10, 12, 13, 19, 21, 27, 28, and 30 are unpatentable under 35 U.S.C. § 102 over *Sinclair***

1.   **Independent Claim 1**

(i)   **(Preamble) A memory device, comprising:**

Sinclair discloses "the operation of re-programmable non-volatile memory systems such as semiconductor flash memory[.]" Ex. 1017 at 1:17-19, Fig. 1.
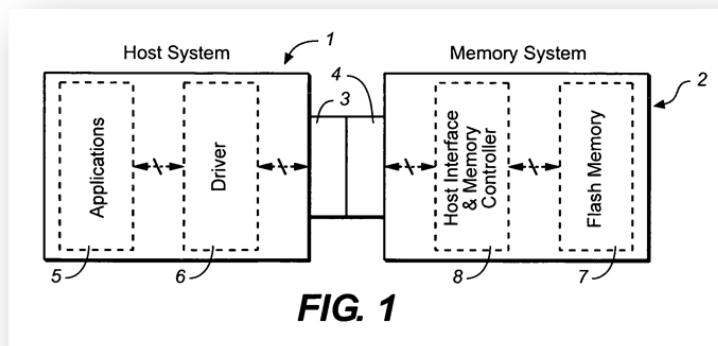
Id. at Fig. 1.

(ii)   **one or more registers to store one or more predefined access profiles associated with the memory device, the one or more predefined access profiles used to determine how access to the memory device is configured for at least one usage; and**

Sinclair discloses a Reclaim Normal mode that is a predefined access profile that optimally interrupts host write operations (*i.e.*, determine how access to the memory device is configured) based on an expected host activity (*i.e.*, usage). Ex. 1017 at 23:28-30. In this mode, the memory device calculates an optimal interleave ratio of reclaim operations such that a memory card will not run out of

writeable memory until there is no reclaimable memory left. *Id.* at Abstract. ("A memory controller ... schedules the reclaim operations to be evenly distributed between write operations until the memory is full."), 2:50-57, Fig. 19.

The selection of Reclaim Normal mode, for example, causes the memory controller to configure the device to optimally interleave memory access operations (*e.g.*, write/read) with reclaim operations. *Id.* at Abstract. ("A memory controller ... schedules the reclaim operations to be evenly distributed between write operations until the memory is full.").

Reclaim On mode and Reclaim Off mode similarly determine how access to the memory device is configured based on an expected host activity (*i.e.*, usage). In Reclaim On mode, the host sits "idle" by not sending additional commands as the memory device performs continuous reclaim operations. *Id.* at 23:38-44. In Reclaim Off mode, the memory device inhibits reclaim operations and only host operations are performed. *Id.* at 23:55-56.

Furthermore, *Sinclair* necessarily discloses one or more registers to store the one or more predefined access profiles associated with the memory device, as discussed above. Ex. 1002 at ¶¶ 353-55. For a host to select a reclaim mode, the host must first understand what modes are supported by the memory device by accessing the memory register for this information. *Id.* Without this information

stored in a register, the host would be unable to properly select a reclaim operation mode. *Id*.

The standardized memory technologies disclosed in *Sinclair* (*e.g.*, CompactFlash and MMC) each disclose a register that stores internal information. Ex. 1002 at ¶355. For example, CompactFlash discloses all host/card communication "is done using the Task File registers, which provide all the necessary registers for control and status information related to the storage medium." Ex. 1003 at 110 (emphasis supplied).

As another example, MMC teaches a standard approach for storing card parameters on a register. Ex. 1008 at 67-79. As shown in Fig. 4, the MMC card includes multiple registers (OCR, CID, CSD, RCA, and DSR) that store specific content or configuration parameters. Ex. 1008 at 67. For example, the Card-Specific Data register in MMC stores the supported card command classes for a MMC card. Ex. 1008 at 71.

Figure 4: MultiMediaCard Architecture
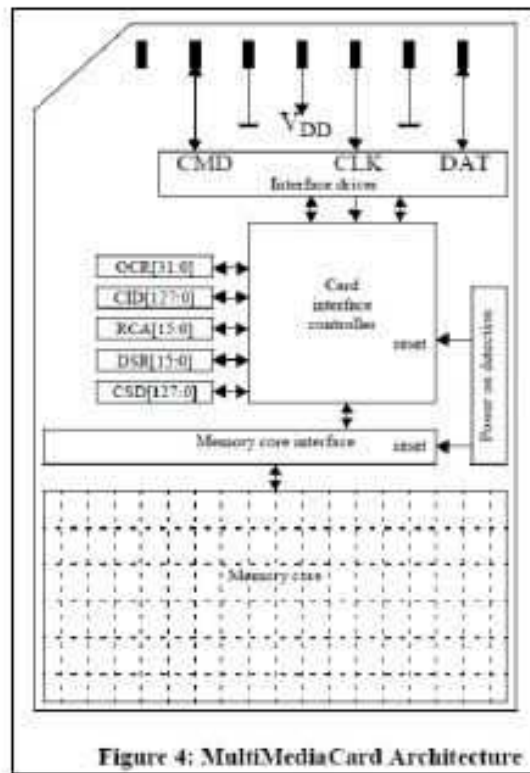
Ex. 1008 at Fig. 4.

Moreover, *Sinclair* discloses that a portion of the memory, like a register, should store operating firmware and data used by the memory controller. Ex. 1017 at 10:20-22 ("[a]t least one metablock 167 is usually allocated allocated as *a reserved block for storing operating firmware and data used by the memory controller*.") (emphasis added). Ex. 1002 at ¶ 357. The operating firmware and data used by the memory controller would include the reclaim operation modes available to the memory device. *Id.* The controller would need the firmware and data to store the available reclaim modes in order for the controller to perform the memory reclaim operations according to the currently-selected reclaim mode. *Id.* *Sinclair* thus

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discloses that a portion of the memory capable of storing information (*i.e.*, register) stores the operating firmware used by the memory controller, like the various supported reclaim modes, which are the predetermined access profiles, as discussed above. *Id*.

> **(iii)** **a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles associated with the memory device; and**

In *Sinclair*, the controller receives a command to select the appropriate reclaim mode. Ex. 1017 at 23:28-30 ("[T]he host may have commands to select the appropriate reclaim mode based on present host activity or expected host activity"); Ex. 1002 at ¶358. After receiving a reclaim mode command, such as the "Reclaim_normal" command, the controller begins reclaiming memory as specified by the selected profile. Ex. 1017 at 23:27-30. For instance, after receiving a "Reclaim_normal" command, the reclaiming occurs "according to an adaptive schedule" in Reclaim Normal mode. *Id.* at 24:1-3.

> **(iv)** **receive at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage**.

The memory controller in *Sinclair* receives a second command that optimally configures the performance of memory access operations (*e.g.,* write operations)

with reclaim operations (*i.e.*, usage) in accordance with the Reclaim Normal mode

(*i.e.*, predefined access profile).

When "triggered by a host command," the memory controller recalculates the

interleave ratio in the selected Reclaim Normal mode and configures the memory

device to the recalculated interleave ratio. Ex. 1017 at 18:23-26, 3:3-6 ("An

interleave ratio may be calculated at intervals or when there is a triggering event

such as the deletion of some stored data by a host. Thus, *the interleave ratio is*

updated as appropriate so that the ratio is adaptive to changing circumstances.")

(emphasis supplied); Ex. 1002 at ¶362. Accordingly, a portion of the memory device

(*i.e.*, the memory in the memory integrated circuit chip) is now configured to operate

according to the recalculated interleave ratio. Ex. 1017 at 18:17-23 ("The rate of

reclaiming is modified as a result [of recalculating the interleave ratio] and the rate

of programming valid data is also changed because the rate of reclaiming affects

the rate of programming valid data"); Ex. 1002 at 363. Specifically, the portion

of memory in the memory integrated circuit chip that is either being written to or

reclaimed is configured in accordance with the recalculated interleave ratio.

Ex. 1017 at 18:17-23; Ex. 1002 at ¶363.

Sinclair even depicts a scenario where the controller reconfigures the reclaim

operations for the memory device after receiving a host delete command. Ex. 1017

at 18:12-23; Ex. 1002 at ¶362. In Fig. 20 (shown below), when the host issues a

delete command to the memory device at time t10, the system alters the interleave

ratio such that all reclaimable space is reclaimed when the memory becomes full.

Ex. 1017 at 18:12- 26; Fig. 20 (shown below). Thus, the delete command configures

access to the memory device in accordance with the particular reclaim profile

selected for device access (*i.e.*, usage). Ex. 1002 at ¶¶362-63.
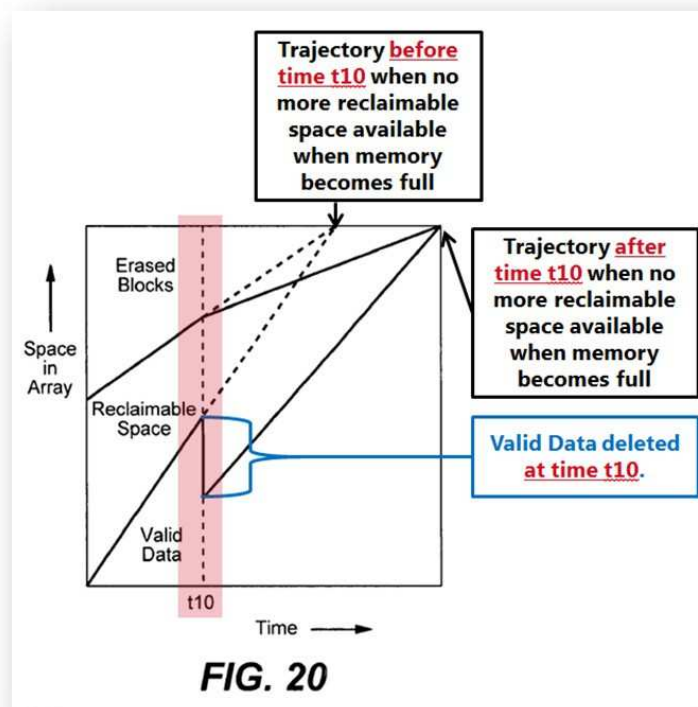
Ex. 1017 at Fig. 20 (annotated).

2. **Dependent Claims 3,12**

(i) **The memory device of claim (1, 10) wherein at least one of the one or more predefined access profiles comprises a default access profile**.

Sinclair discloses a default access profile, like the Reclaim Normal mode, that configures the memory device upon power up. Ex. 1017 at 23:47-48; Ex. 1002 at ¶364.

3. **Dependent Claim 9**

(i) **The memory device of claim 1, wherein the one or more predefined access profiles comprise a plurality of predefined access profiles.**

As discussed above, *Sinclair* discloses a Reclaim Normal mode, a Reclaim On mode, a Maximum Interleave mode, a Minimum Interleave mode, and a Reclaim Off mode that each constitute a predefined access profiles associated with the memory device. Ex. 1017 at 2:50-57; Ex. 1002 at ¶365. *Sinclair* thus discloses a plurality of predefined access profiles. *Id*.

4. **Dependent Claim 10**

(i) **(Preamble) A memory device comprising:**

See Section above at IX.F.1(i).

(ii) **one or more predefined access profiles to determine how access to the memory device is configured for at least one usage of the memory device;**

See Section above at IX.F.1(ii).

> **(iii)** **a controller configured to: receive at least one first command to activate at least one of the one or more predefined access profiles associated with the memory device; and**

See Section above at IX.F.1(iii).

> **(iv)** **receive at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.**

See Section above at IX.F.1(iv).

5. Dependent Claim 13

> **(i)** **The memory device of claim 10, wherein the memory device comprises an embedded MultiMedia Card (eMMC) device.**

The memory device in *Sinclair* may comprise an embedded MultiMediaCard. An exemplary memory device in *Sinclair* is a MultiMediaCard. Ex. 1017 at 4:28-32 ("There are currently many different flash memory cards that are commercially available, examples being the CompactFlash (CF), the MultiMediaCard (MMC), Secure Digital (SD), miniSD, Memory Stick, SmartMedia and TransFlash cards."). *Sinclair* further discloses that the MultiMediaCard may be embedded within the host. *Id.* at 4:25 ("[T]he flash memory can be embedded within the host[.]"). Accordingly, *Sinclair* discloses that an embedded Multimedia Card is an exemplary

memory device to implement the various reclaim operation modes. Ex. 1002 at

¶¶370-73.

6. Dependent Claim 19

(i) (Preamble) A method comprising:

Sinclair deals with "the operation of re-programmable non- volatile memory

systems such as semiconductor flash memory[.]" Ex. 1017 at 1:17-19; Fig. 1 (shown

below). A non-volatile memory system, such as a semiconductor flash memory, is

a memory device.
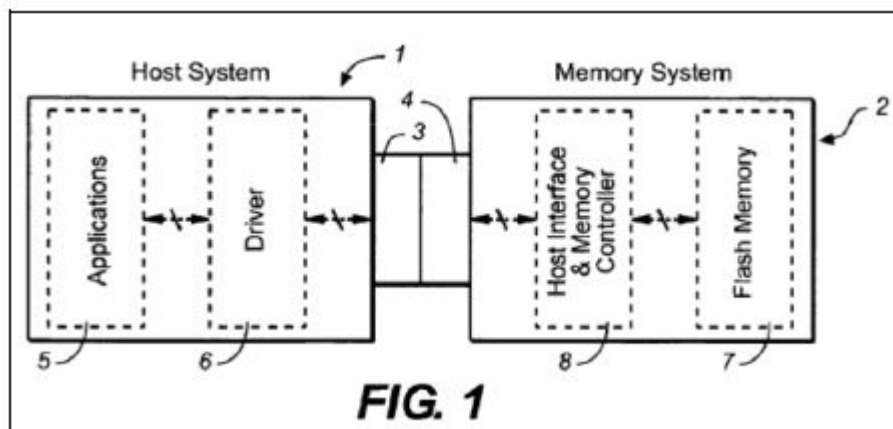
Ex. 1017 at Fig. 1.

Sinclair further discloses at least a "method for managing space in a non-

volatile memory." Ex. 1017 at Abstract, Claims 1-14.

(ii) receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device,

See Section above at IX.F.1(ii)-(iii).

(iii) **the one or more predefined access profiles stored in one or more registers, the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and**

See Section above at IX.F.1(ii).

(iv) **receiving at least one second command to designate the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the at least one of the one or more predefined access profiles for the at least one usage.**

See Section above at IX.F.1(iv).

7. **Dependent Claims 21 and 30**

(i) **The method of claim (19, 28), wherein at least one of the one or more predefined access profiles comprises a default access profile.**

See Section above at IX.F.2.

8. **Dependent Claim 27**

(i) **The method of claim 19, wherein the one or more registers comprise a plurality of registers for storing a plurality of the predefined access profiles.**

See Sections above at IX.F.1(ii) and IX.F.3.

9. **Dependent Claim 28**

(i) **(Preamble) A method comprising**:

See Section above at IX.F.6(i).

> **(ii)** <u>**receiving at least one first command to activate at least one of one or more predefined access profiles associated with a memory device**</u>,

See Section above at IX.F.6(iii).

> **(iii)** <u>**the one or more predefined access profiles determining how access to the memory device is configured for at least one usage of the memory device; and**</u>

See Section above at IX.F.6(ii).

> **(iv)** <u>**receiving at least one second command to configure access to the memory device in accordance with the at least one of the one or more predefined access profiles such that at least a portion of the memory device is configured according to the one or more predefined access profiles for the at least one usage**</u>.

See Section above at IX.F.6(iv).

G. <u>GROUND 7: Claim 13 is unpatentable under 35 U.S.C. § 103(a) over *Sinclair* and *eMMC*</u>

1. <u>Dependent Claim 13</u>

> **(i)** <u>**The memory device of claim 10, wherein the memory device comprises an embedded MultiMedia Card (eMMC) device.**</u>

Ground 6 applies *Sinclair* to Claim 10. If the Board concludes that *Sinclair's* disclosure of embedding an MMC device in a host is not an eMMC device, Claim 13 is obvious over *Sinclair* in view of eMMC. Use of eMMC to implement the memory device of *Sinclair* would be an obvious design choice in view of the explicit teachings in eMMC of the benefits of employing flash memory in the eMMC

standard format, as well as the teaching of *Sinclair* to embed the device in the host.

See Ex. 1016 ("eMMC™ makes it easy to embed mass-storage flash memory on host systems."); Ex. 1017 at 4:25-32; Ex. 1002 at ¶¶389-91; *supra* Section VIII.F.

X.   <u>CONCLUSION</u>

For the foregoing reasons, Petitioner respectfully requests that a trial for *inter partes* review of the '850 Patent be instituted and that Claims 1-4, 9-13, 19-22, and 27-31 be rejected and canceled.

Dated: January 31, 2019   Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

1.   The undersigned certifies that this brief complies with the type volume limitations of 37 CFR § 42.24(a)(1)(i). This brief contains 13,966 words (excluding the table of contents, the table of authorities, mandatory notices under 37 CFR § 42.8, the certificate of service, certificate of compliance, and appendix of exhibits), as calculated by the "Word Count" feature of Microsoft Word 2016, the word processing program used to create it.

2.   The undersigned further certifies that this brief complies with the typeface requirements of 37 CFR § 42.6(a)(2)(ii) and typestyle requirements of 37 CFR § 42.6(a)(2)(iii). This brief has been prepared in a proportionally spaced typeface using Microsoft Word 2016 in Times New Roman 14-point font.

Dated: January 31, 2019   Respectfully submitted,

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<u>CERTIFICATE OF SERVICE</u>

The undersigned hereby certifies that a true copy of the foregoing

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,063,850

and supporting materials (Exhibits 1001 - 1020 and Power of Attorney) have been

served in its entirety this 31st of January, 2019, by e-mail and Federal Express on

Patent Owner at the correspondence address for the attorney of record for the

9,063,850 Patent shown in USPTO PAIR, as well as on counsel for Patent Owner

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