Paper No. __
Filed: March 5, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,163,492

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,163,492

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 14-19 of U.S. Patent No. 6,163,492 ("the '492 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '492 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al*., No. 1:18-cv-00307-RGA (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 5,934,974 ("the '974 patent"), 6,099,386 ("the '386 patent"), 6,469,559 ("the '559 patent"), and 6,597,201 ("the '201 patent") in this action. Petitioner is concurrently filing two other IPR petitions challenging one or more claims of the '492 patent, as well as additional IPR petitions challenging certain claims of the '974, '386, '559, and '201 patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul

M. Anderson (Reg. No. 39,896), and (3) Chetan R. Bansal (Limited Recognition No. L0667). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the '492 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 14-19 ("challenged claims") of the '492 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following grounds:

Ground 1: Claims 14-19 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,457,656 ("Fu") (Ex. 1005).

Ground 2: Claims 14-19 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,621,346 ("McAdams") (Ex. 1006).

Ground 3: Claims 14-19 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious based on Fu and U.S. Patent No. 5,373,477 ("Sugibayashi") (Ex. 1011).

Ground 4: Claims 14-19 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over McAdams and Sugibayashi.

The '492 patent issued from U.S. Application No. 09/178,445 ("the '445 application") filed October 23, 1998. (Ex. 1001, Cover). The '445 application does not claim priority to any earlier-filed applications.

Fu issued on October 10, 1995. McAdams issued on November 04, 1986. Sugibayashi issued on December 13, 1994. Thus, Fu, McAdams, and Sugibayashi qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b) with respect to the '492 patent. Fu, McAdams, and Sugibayashi were not considered by the Patent Office during prosecution of the '492 patent. (*See generally* Ex. 1001 at References Cited.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '492 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including October 23, 1998, the filing date of the U.S. Application

maturing into the '492 patent), would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002 at ¶20.)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '492 PATENT AND PRIOR ART

A. The '492 Patent

The '492 patent is entitled "Programmable Latches that Include Non-volatile Programmable Elements." (Ex. 1001, Cover.) Consistent with the title, the '492 patent relates to "programmable latches that include non-volatile programmable elements" where "[e]xamples of non-volatile programmable elements are fuses." (*Id.*, 1:15-17; Ex. 1002 at ¶¶36-44; *see also* Ex.1002, ¶¶22-35 (citing Ex. 1015).)

As disclosed by the '492 patent, such programmable latches "are used in integrated circuits to enable modification of the circuits without changing the masks used for circuit fabrication." (Ex. 1001 at 1:18-20.) Programmable latches using non-volatile programmable elements such as fuses were known in the art before the alleged invention disclosed in the '492 patent. (*Id*. at 1:24-54.)

[1] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '492 patent. (Ex. 1002 at ¶¶5-15; Ex. 1003.)

As shown in figure 1 below, one prior art programmable latch includes a "[f]use F1 [] connected between the power supply VDD and the latch output terminal OUT." (*Id*. at 1:24-27.)

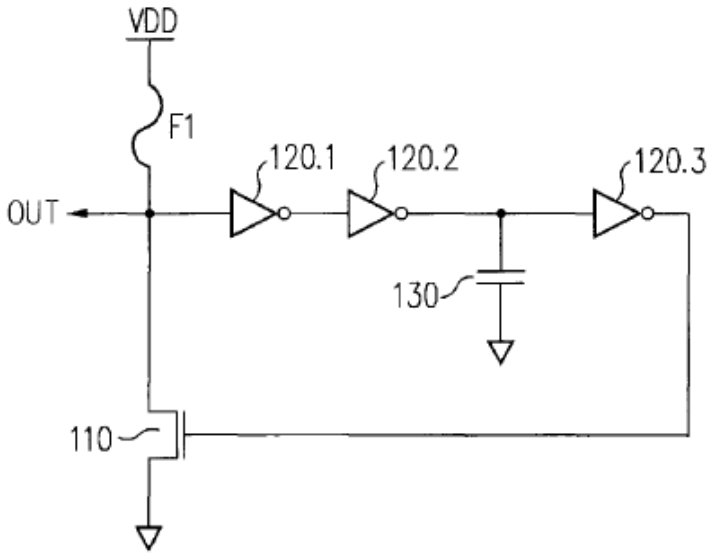


FIG. 1
(PRIOR ART)

(*Id*. at FIG. 1.)

According to the '492 patent, "[i]f the fuse F1 is intact, the terminal OUT is pulled to VDD" and the inverters 120.1, 120.2, and 120.3 keep the transistor 110 off. (*Id*. at 1:32-33.) In contrast, "[i]f fuse F1 is blown, the terminal OUT is at the ground voltage" and "[t]he inverters turn transistor 110 on to keep the terminal OUT at ground." (*Id*. at 1:33-35.)

Capacitor 130 is included in the circuit of figure 1 above to ensure proper initialization when power is supplied to the circuit. (*Id*. at 1:36-54.) Specifically,

when power is off, transistor 110 is off and the node OUT is floating. (*Id*. 1:38-40.) Because the node OUT is floating, there is a concern that OUT can inadvertently be raised to a logic "1" (high) by capacitive coupling or otherwise. (*Id*. at 1:40-44.) Therefore, even if the fuse F1 is blown when power is applied, the charge on OUT corresponding to the logic "1" (high) can keep the transistor 110 off, thereby preventing the charge on OUT from being drained away. (*Id*. at 1:44-46.) Therefore, even if the fuse has been blown, the output of the programmable latch, which should be a logic "0" (low), may remain high. (*Id*. at 1:46-47.) The '492 patent states that "capacitor 130 keeps the input of inverter 120.3 low sufficiently long to allow the inverter to turn on transistor 110 and discharge the terminal OUT to ground if the fuse is blown" such that OUT properly reflects the state of the fuse F1. (*Id*. at 1:48-54; Ex. 1002 at ¶¶40-41.)

The '492 patent acknowledges that the "[p]rior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch" and that "[t]he state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals." (Ex. 1001 at 2:22-26; *see also id.* at 1:24-54, FIG. 1; Ex. 1002 at ¶41.)

While the prior art programmable latch shown in figure 1 includes features to avoid an incorrect output on power up and does not require any initialization

signal, the '492 patent proposes an alternative programmable latch as shown in figure 2A below. (Ex. 1001 at 3:10-11.)

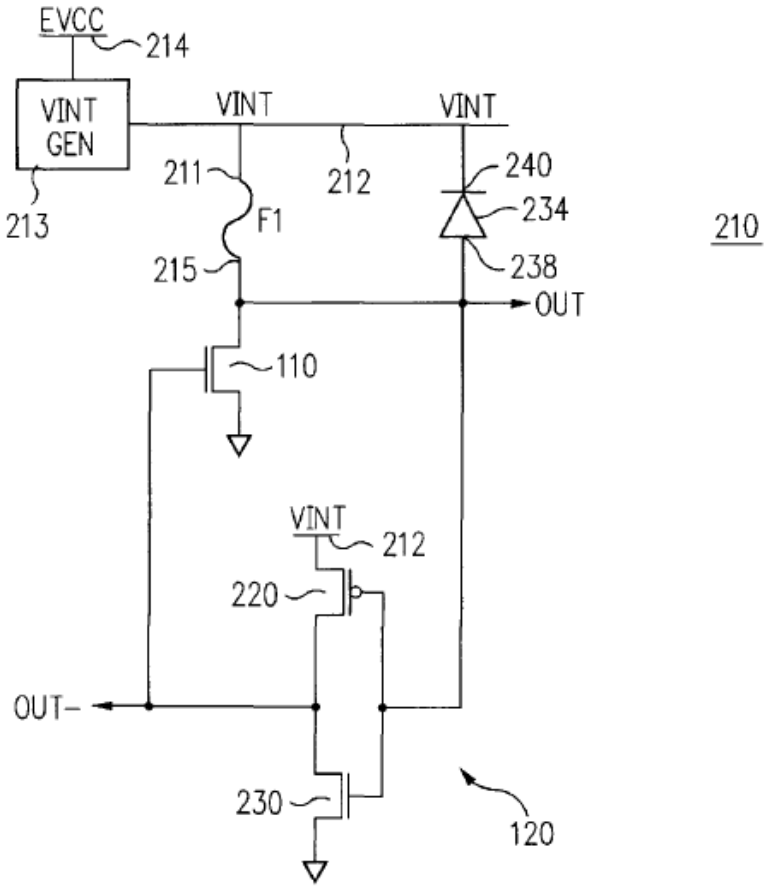


FIG. 2A

(*Id.* at FIG. 2A.)

The programmable latch shown in figure 2A above includes a fuse 211, an inverter 120 that includes transistors 220 and 230, and a transistor 110. (*Id.* at 3:10-33, FIG. 2A.) The programmable latch of figure 2A also includes a diode 234 that holds the OUT node at a voltage not higher than a threshold voltage of the

diode 234 when the VINT terminal is at ground. (*Id*. at 3:38-41.) According to the '492 patent, by maintaining the voltage on OUT low using the diode 234, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on and "connects the terminal OUT to ground," resulting in a correct output. (*Id*. at 3:41-49.) This happens because terminal OUT is held "not higher than one threshold voltage of diode 234," and at such a voltage, transistor 230 does not turn on because its threshold voltage (e.g., 1.2V) is greater than the threshold voltage of diode 234. (*Id.*) Per the '492 patent, the latch can operate correctly even if the diode is omitted. (*Id.* at 5:51-6:7; Ex. 1002 at ¶¶42-44.)

The above features were well known in the art, as discussed below at Sections VII.B, VII.C, and IX. (Ex. 1002 at ¶¶61-175.)

B. Fu

Fu relates to a "memory redundancy apparatus." (Ex. 1005 at Abstract.) Figure 2 of Fu, reproduced below, illustrates a memory redundancy circuitry 2, including a redundancy activation circuit 40. (*Id*. at 3:27-35, 3:47-48, FIG. 2.)

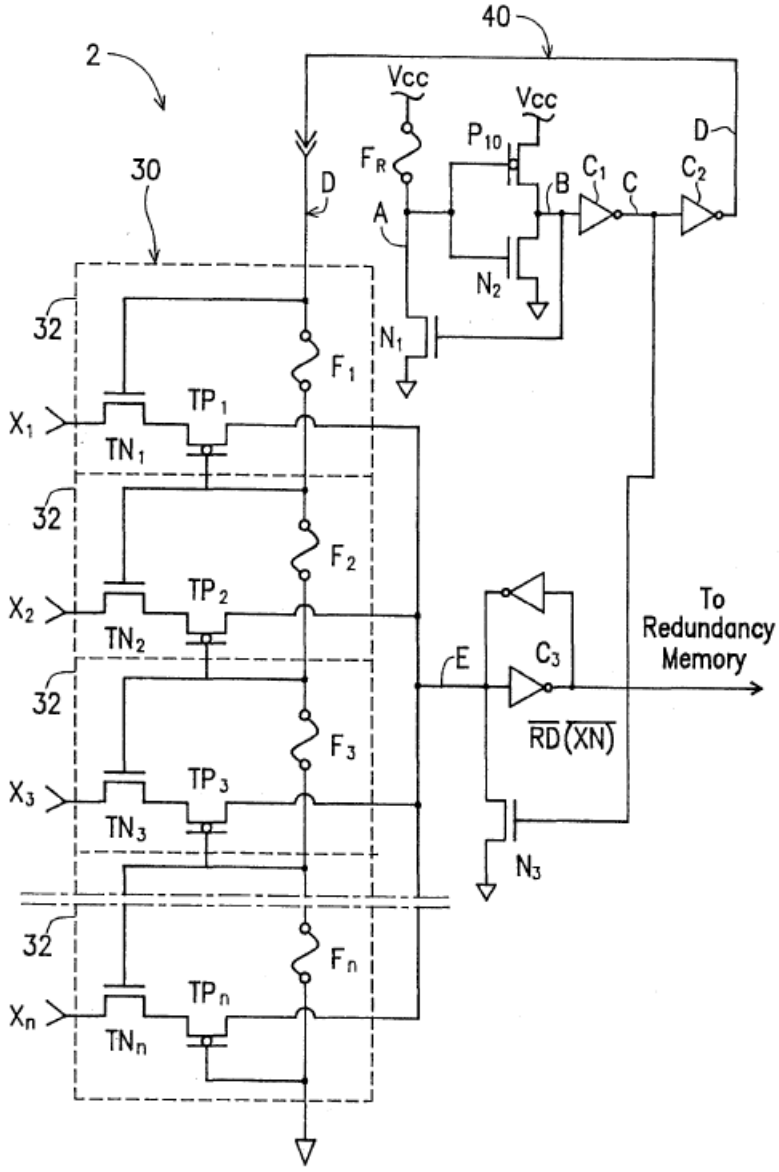


FIG. 2

(*Id*., FIG. 2.)

Fu discloses that the "redundancy activation circuit 40" shown in figure 2 is also depicted as a schematic diagram in figure 4, which is reproduced below. (*Id*. at 4:14-17, FIG. 4.)

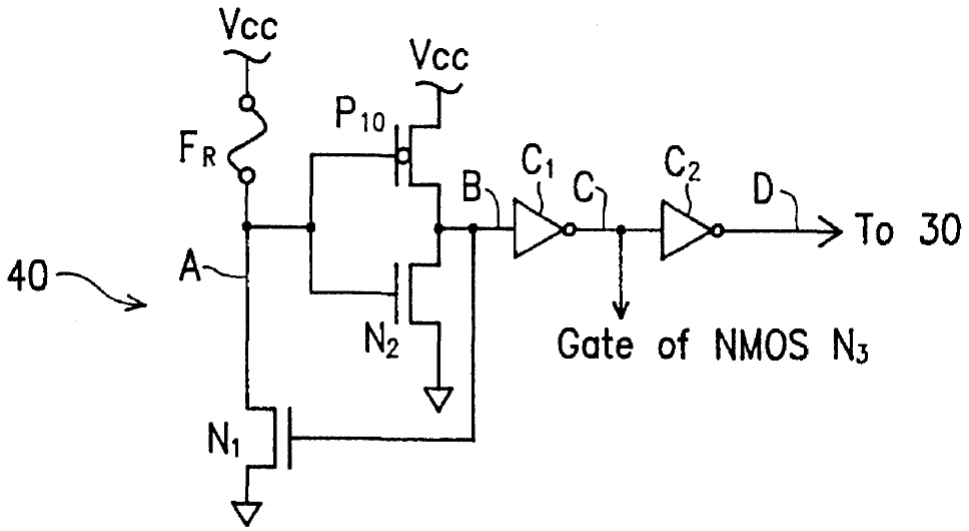


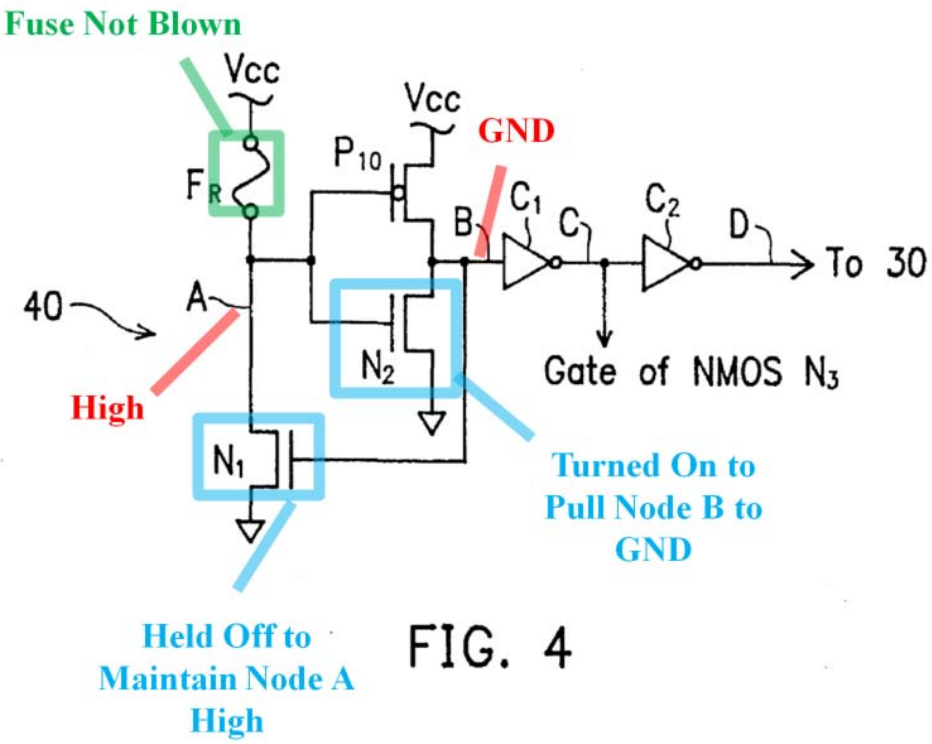
FIG. 4

(*Id*. at FIG. 4.)

In figure 4, "the fuse element F_R is connected in series with the NMOS transistor N_1, with the other end of fuse element tied to V_{CC}, and the transistor end tied to ground." (*Id*. at 4:20-23.) When the redundancy activation circuit 40 of figure 4 is operational, the voltage at node A is influenced by the electrical potentials applied on the V_{CC} and GND terminals and the state of the fuse F_R. (*Id*. at 4:67-5:29; Ex. 1002 at ¶¶47-50.)

In a first operational scenario depicted in annotated figure 4 below, the fuse F_R is not blown and therefore "the potential of node A is at the high level." (Ex. 1005 at 4:67-5:4.) Because node A is at the high level, NMOS transistor N_2 is turned on to "pull node B to the GND potential." (*Id*. at 5:4-6.) Fu further

discloses that "[m]eanwhile, the other NMOS transistor N_1 is maintained in non-conduction mode, helping to maintain the potential of node A at the high level." (*Id*. at 5:6-8; Ex. 1002 at ¶51.)



(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶51.)

In the alternate operational scenario depicted in the demonstrative below, the fuse has been blown and the node A is at a low potential. (Ex. 1005 at 5:19-25.) Because node A, which is coupled to the gate of PMOS transistor P_{10}, is low, PMOS transistor P_{10} is on and conducting. (*Id*. at 5:25-26.) In turn, "[t]he conduction of P_{10} brings node B to the high potential level, which also makes the

NMOS transistor N_1 conduct[], so that node A is ensured to be maintained at a low potential level." (*Id*. at 5:26-29; Ex. 1002 at ¶52.)

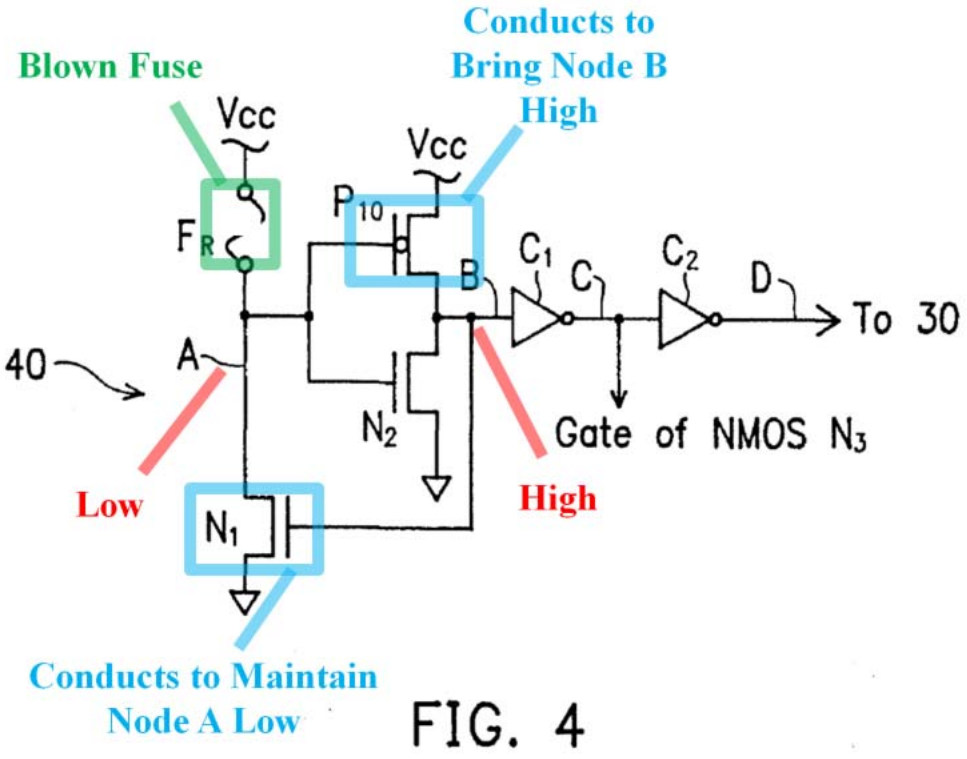


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶52.)

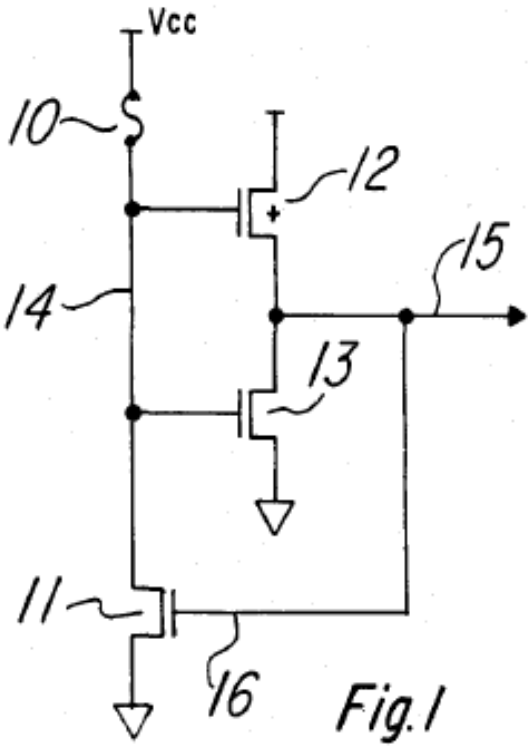
Therefore, based on whether or not the fuse F_R has been blown, node A will be held either high (V_{CC}) or low (GND). (Ex. 1005 at 4:67-5:29; Ex. 1002 at ¶53.) The state of node A is inverted by the inverter formed by transistors P_{10} and N_2 to produce the state at node B, which is fed back to the input of NMOS transistor N_1, thereby helping to maintain the state of nodes A and B. (Ex. 1002 at ¶53.)

Therefore, nodes A and B are latched at either V_{CC} or GND based on whether or not the fuse is blown. (*Id.*)

C. McAdams

McAdams relates to a "fuse circuit as used in self-repairing memory devices." (Ex. 1006, Abstract; Ex. 1002 at ¶54.) According to McAdams, "[i]n self-repairing semiconductor memory device, fuses are used to store the addresses of faulty locations, so redundant cells can be substituted" or "the fuse may be used to generate an enabling signal." (Ex. 1006 at 1:9-12.) McAdams further discloses that the "fuses are usually polysilicon conductor strips that are selectively blown by an indexed laser beam." (*Id*. 1:12-14.)

McAdams discloses operation of a particular fuse circuit in connection with figure 1. (*Id.*, FIG. 1; Ex. 1002 at ¶55.)



(Ex. 1006 at FIG. 1.)

The fuse circuit shown in figure 1 of McAdams includes "[a] fuse element 10," "an N-channel feedback transistor 11," and "[a] CMOS inverter [that] includ[es] a P-channel transistor 12 and an N-channel transistor 13." (*Id*. at 1:67-2:6.) The fuse circuit of figure 1 "produces an output 15" and "[f]eedback is provided from the output node 15 to the gate of the transistor 11." (*Id*. at 2:3-7; Ex. 1002 at ¶56.)

McAdams discloses how the fuse circuit operates when power-up occurs and Vcc goes from zero to +5v. (Ex. 1006 at 2:8-26; Ex. 1002 at ¶57.) For example, when power is applied, "if the fuse has not been blown, the node 14 follows Vcc."

(Ex. 1006 at 2:8-10.) If the fuse has been blown, node 14 is at Vss when power is applied, and transistor 12 turns on causing the output node 15 to follow Vcc. (*Id*. at 2:21-24.) As the output node 15 goes high, transistor 11 turns on, thereby keeping the node 14 at Vss. (*Id*. at 2:24-26.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express

constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002 at ¶46.)

IX. DETAILED EXPLANATION OF GROUNDS

As detailed below, the challenged claims are unpatentable based on Grounds 1-4. (Ex. 1002 at ¶¶61-175.)

A. Ground 1: Fu Anticipates Claims 14-19

1. Claim 14

a) A programmable latch comprising:

To the extent the preamble is limiting, Fu discloses this feature. (Ex. 1002 at ¶¶62-70.) For example, Fu discloses "memory redundancy circuitry 2, which comprises the redundancy activation circuit 40." (Ex. 1005 at 3:46-47.) Figure 2 (reproduced below) illustrates the memory redundancy circuitry 2, including the redundancy activation circuit 40. (*Id.* at 4:14-17, FIG. 2.)

[2] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '492 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

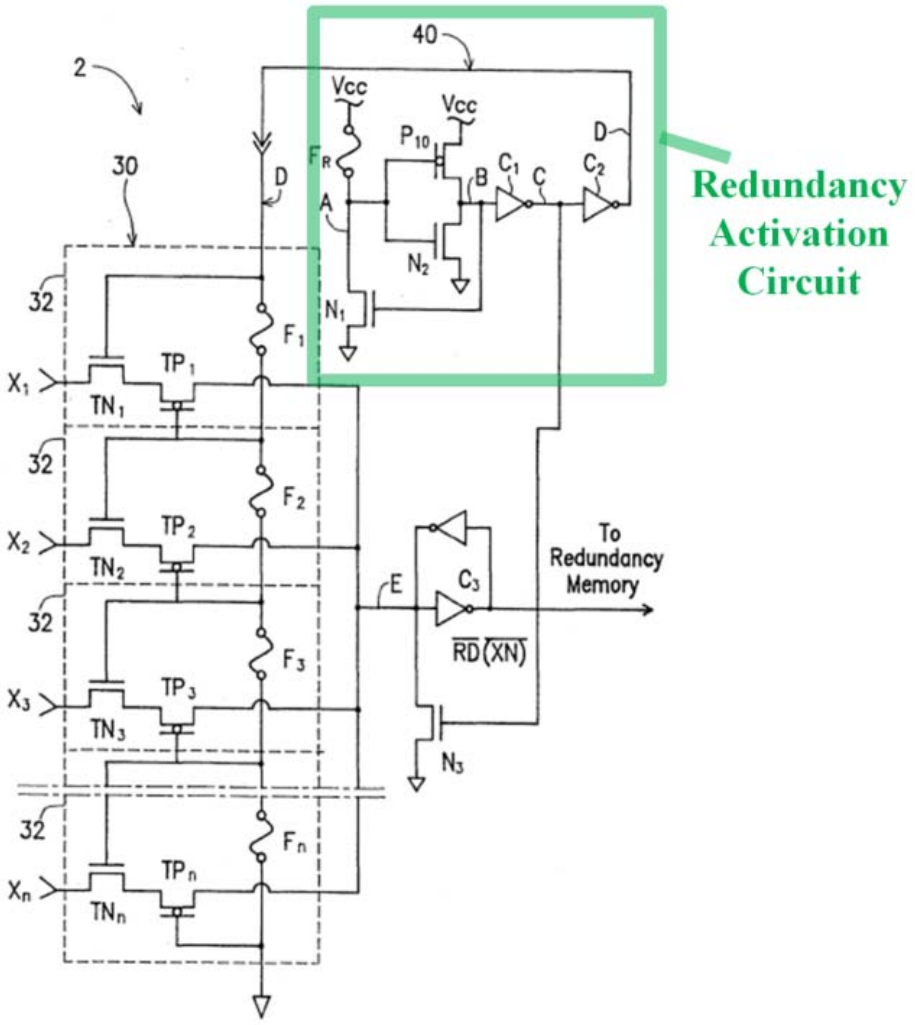


FIG. 2

(*Id*. at FIG. 2 (annotated); Ex. 1002 at ¶63.)

Fu further discloses that the "redundancy activation circuit 40" shown in figure 2 is also depicted in figure 4 (reproduced below). (Ex. 1005 at 4:14-17, FIG. 4.)

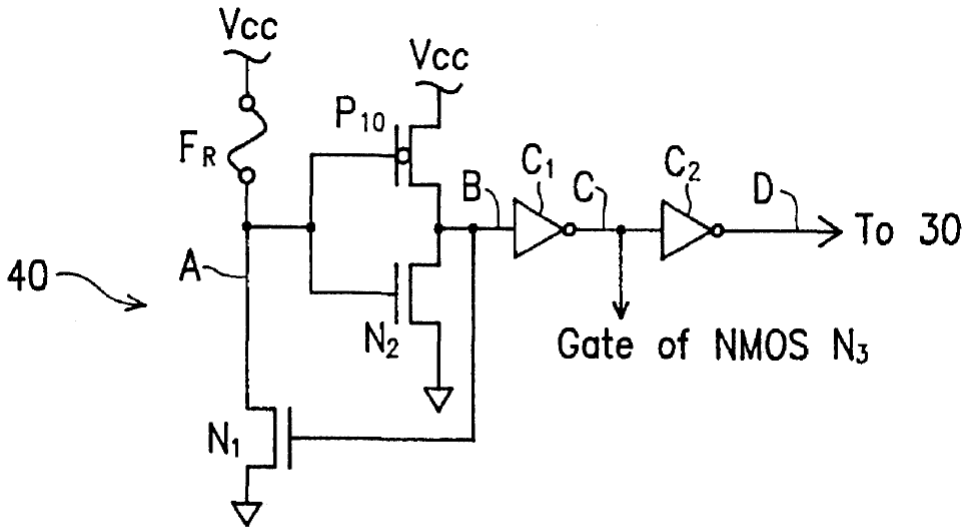


FIG. 4

(Ex. 1005 at FIG. 4.)

"The redundancy activation circuit 40 of figure 4 includes a fuse F_R, a PMOS transistor P_{10}, two NMOS transistors N_1 and N_2, and two inverters C_1 and C_2." (*Id*. at 4:17-19.) Fu discloses how the redundancy activation circuit 40 operates to provide control signals to the remainder of the memory redundancy circuitry 2 shown in FIG. 2. (*Id*. at 3:46-51, 4:64-5:37.) The circuitry operates between two electrical potentials, one of which is a logical high (V_{CC}) and the other is a logical low (GND). (*Id*. at 3:46-51; Ex. 1002 at ¶¶64-65.)

In a first operational scenario depicted in annotated figure 4 below, the fuse F_R is not blown and therefore "the potential of node A is at the high level." (Ex. 1005 at 4:67-5:4.) Because node A is at the high level, NMOS transistor N_2 is

turned on to "pull node B to the GND potential." (*Id*. at 5:4-6; Ex. 1002 at ¶66.) Fu further discloses that "[m]eanwhile, the other NMOS transistor N_1 is maintained in non-conduction mode, helping to maintain the potential of node A at the high level." (Ex. 1005 at 5:6-8.)

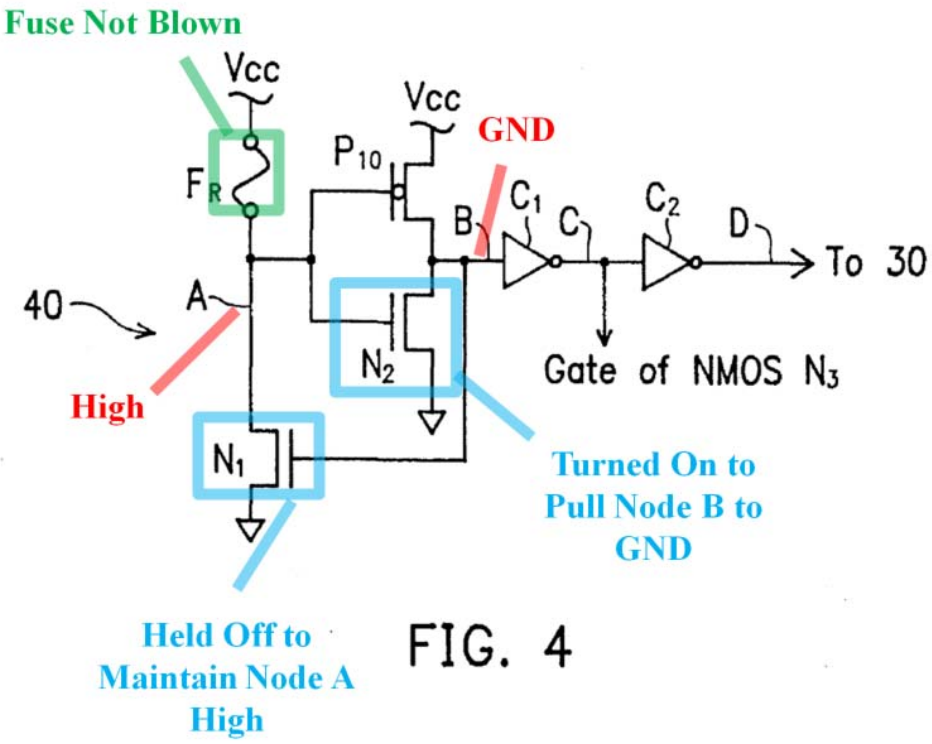


FIG. 4

(*Id*. at FIG. 4 (annotated); Ex. 1002 at ¶66.)

In the alternate operational scenario depicted in the demonstrative below, the fuse has been blown and the node A is at a low potential. (Ex. 1005 at 5:19-25.) Because node A, which is coupled to the gate of PMOS transistor P_{10}, is low, PMOS transistor P_{10} is on and conducting. (*Id*. at 5:25-26.) In turn, "[t]he conduction of P_{10} brings node B to the high potential level, which also makes the

NMOS transistor N_1 conduct[], so that node A is ensured to be maintained at a low potential level." (*Id*. at 5:26-29; Ex. 1002 at ¶67.)

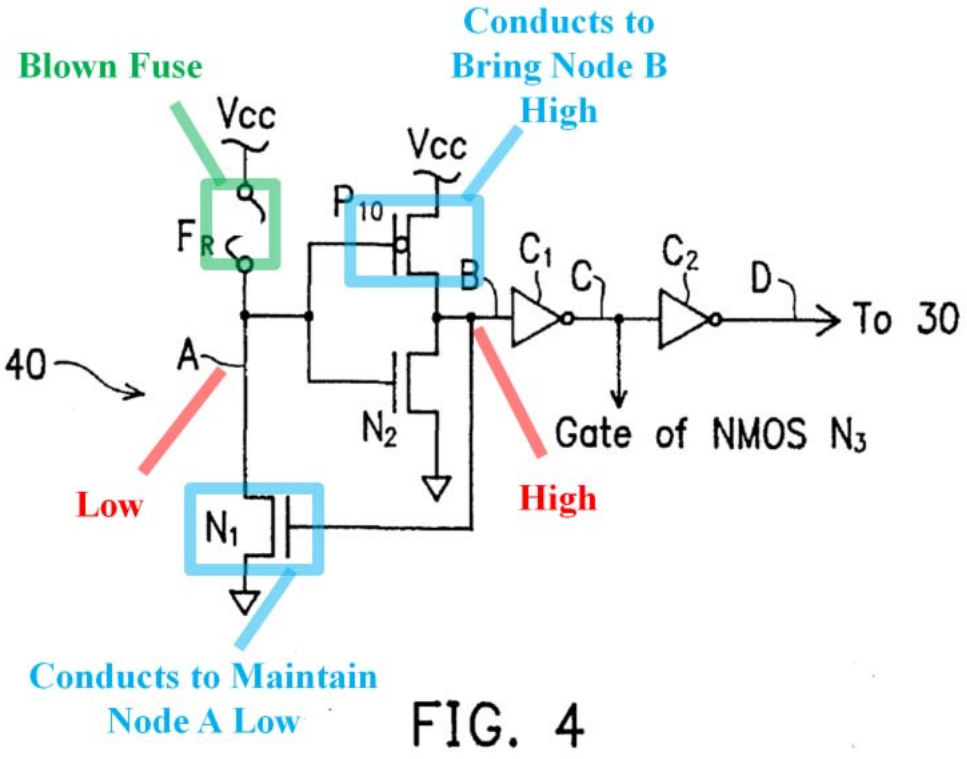


FIG. 4

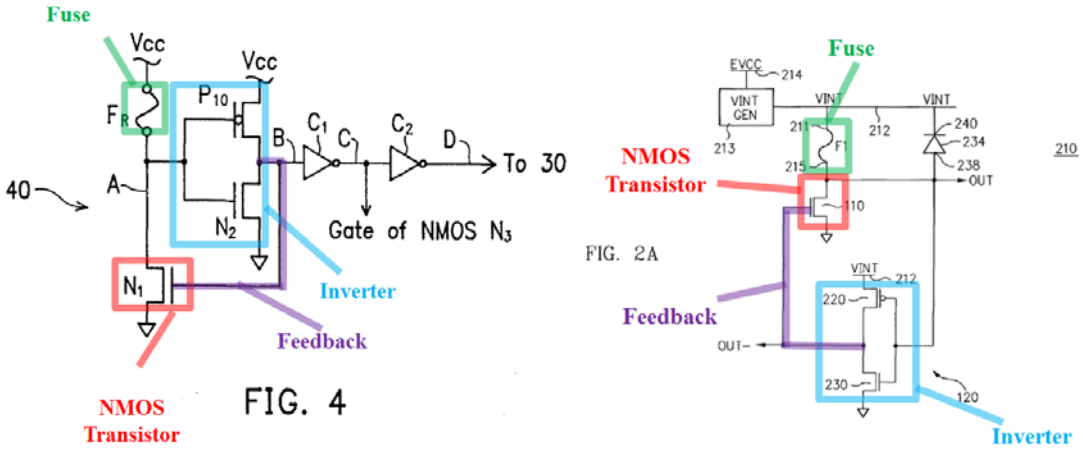
(Ex. 1005 at FIG.4 (annotated); Ex. 1002 at ¶67.)

Therefore, based on whether or not the fuse F_R has been blown, node A will be held either high (V_{CC}) or low (GND). (Ex. 1005 at 4:67-5:29; Ex. 1002 at ¶68.) The state of node A is inverted by the inverter formed by transistors P_{10} and N_2 to produce the state at node B, which is fed back to the input of NMOS transistor N_1, thereby helping to maintain the state of nodes A and B. (Ex. 1002 at ¶68.)

Therefore, nodes A and B are latched at either V_{CC} or GND based on whether or not the fuse is blown. (*Id.*)

The outputs of the redundancy activation circuit (i.e., the outputs of inverters C_1 and C_2) are inverted and non-inverted versions of the state of node B, respectively, where the state at node B is the inverse of the state at node A. (Ex. 1005 at FIG. 4.) A person of ordinary skill in the art would have recognized that the redundancy activation circuit shown in figure 4 of Fu is a "programmable latch" where the programming corresponds to the state of the fuse F_R, which determines the latched values at nodes A and B as well as at the outputs C and D. (Ex. 1002 at ¶69.)

Indeed, the circuit of figure 4 of Fu is a "programmable latch" in the same way that the figure 2A circuit of the '492 patent is a "programmable latch." As shown below, the circuit of figure 2A of the '492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the corresponding elements in the figure 4 circuit of Fu. (Ex. 1001 at FIG. 2A; Ex. 1002 at ¶70; *see infra* Sections IX.A.1(b)-(g) for analysis regarding remaining elements of claim 14.)



(Ex. 1005 at FIG. 4 (annotated); Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶70.)

b) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

Fu discloses this feature. (Ex. 1002 at ¶¶71-75.) As shown in annotated figure 4 below, the "fuse circuit" of Fu includes a "terminal" Vcc, where Vcc is a "high voltage level." (Ex. 1005 at 1:67.) Fu discloses that "[t]he memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (V_{CC}) and low (GND) levels together with its host main memory cell array of the entire memory device." (*Id*. at 3:46-51; Ex. 1002 at ¶¶71-73.) Fu further discloses that "[a]s can be seen in the drawing, the fuse element F_R is connected in series with the NMOS transistor N_1, with the other end of fuse element tied to V_{CC}, and the transistor end tied to ground." (Ex. 1005 at 4:20-23.) During "operation of the memory redundancy circuit 2," "node A is at its high

level (Vcc)" when the fuse is not blown. (*Id.* at 4:64-5:6.) Therefore, a high voltage V_{CC}, which is a constant non-ground voltage, is applied when the circuit of figure 4 operates. (Ex. 1002 at ¶74.) Accordingly, the terminal highlighted in blue below that receives V_{CC} is a "first terminal for receiving a constant non-ground voltage throughout operation of the latch" as recited in claim 14. (*Id.*)

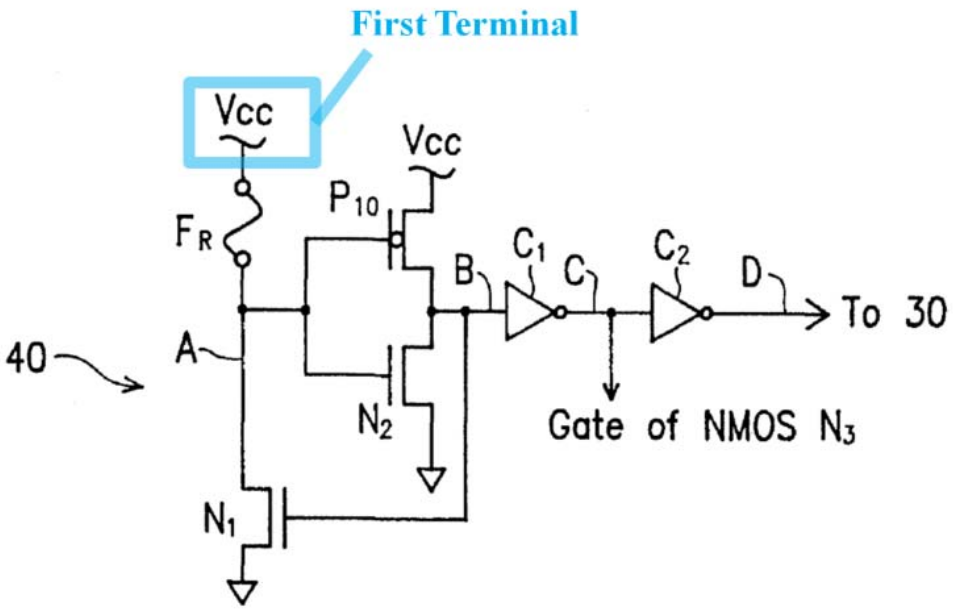


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶74.)

As shown in annotated figure 2A of the '492 patent below, the "first terminal" highlighted in figure 4 of Fu above is consistent with the "first terminal" disclosed by the '492 patent. (Ex.1002 at ¶75.)

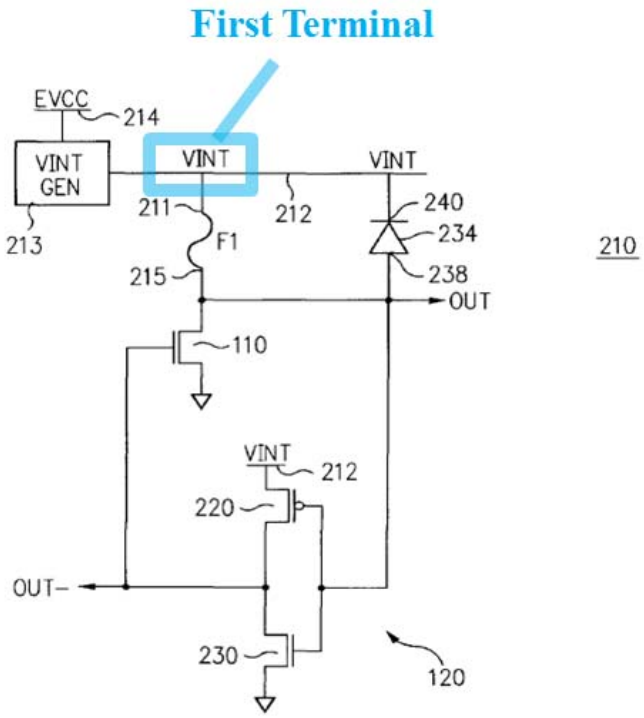


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶75.)

c) a second terminal for receiving a voltage;

Fu discloses this feature. (Ex. 1002 at ¶¶76-78.) For example, the programmable latch circuit in figure 4 of Fu includes a second terminal for receiving GND, which, in the example embodiment described in Fu, corresponds to a low voltage. (Ex. 1005 at 3:46-51, "The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (Vcc) and low (GND) levels together with its host main memory cell array of the entire memory device.", FIG. 4.) Fu discloses that "[a]s can be seen in the drawing, the fuse element F_R is connected in series with the NMOS transistor N_1,

with the other end of fuse element tied to V_{CC}, and *the transistor end tied to ground*." (*Id*. at 4:20-23, emphasis added.)

Therefore, the terminal highlighted in blue below that receives GND is a "second terminal for receiving a voltage" as recited in claim 14. (Ex. 1002 at ¶¶76-77.)

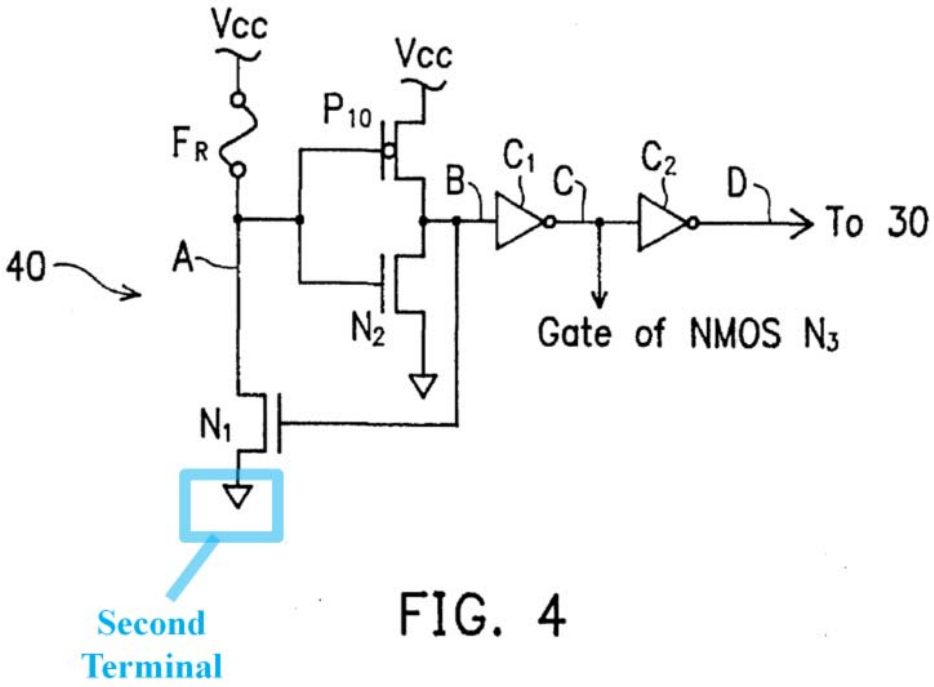


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶77.)

As shown in annotated figure 2A of the '492 patent below, the "second terminal" highlighted in figure 4 of Fu above is consistent with the "second terminal" disclosed by the '492 patent. (Ex.1002 at ¶78.)

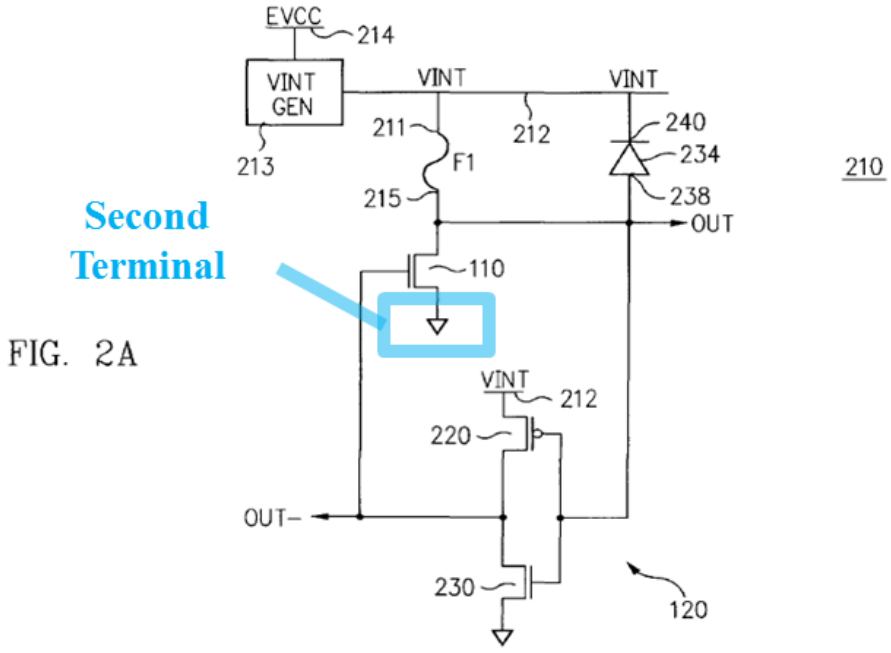


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶78.)

d) a terminal T1 for providing a signal indicating a state of the programmable latch;

Fu discloses this feature. (Ex. 1002 at ¶¶79-80.) For example, as shown in annotated figure 4 below, the node A indicates the state of the fuse, which corresponds to the state of the programmable latch ("a terminal T1 for providing a signal indicating a state of the programmable latch"). As discussed above with respect to claim element 14[a], during operation of the latch, if the fuse is intact, node A is at Vcc (high), but if the fuse is blown, node A is at GND (low). (*See* citations and discussion regarding the operation of the circuit in figure 5 of Fu at Section IX.A.1(a) *supra*.) Therefore, the voltage at node A indicates a "state of the

programmable latch" because it indicates whether the fuse is blown or not. (Ex. 1002 at ¶79.)

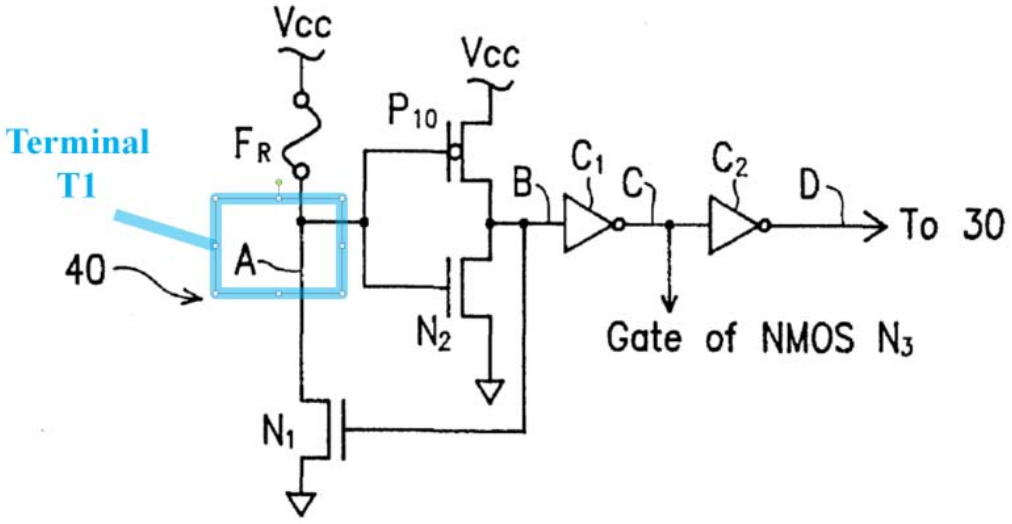
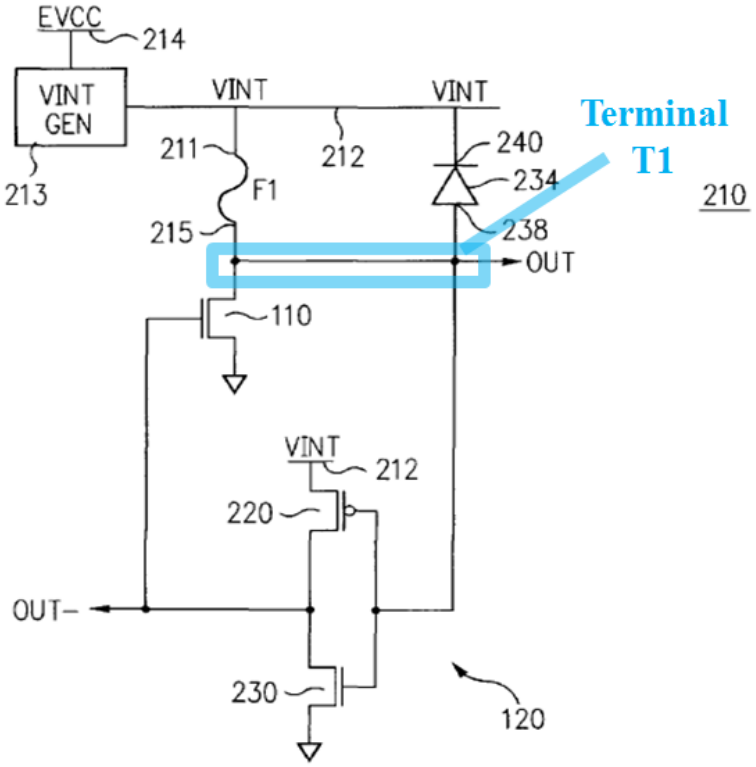


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶79.)

As shown in annotated figure 2A of the '492 patent below, the "terminal T1" highlighted in figure 4 of Fu above is consistent with the "terminal T1" disclosed by the '492 patent. (Ex.1002 at ¶80.)

FIG. 2A



(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶80.)

e) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

Fu discloses this feature. (Ex. 1002 at ¶¶81-85.) For example, the fuse F_R shown in annotated figure 4 of Fu below is a "non-volatile programmable element." Such an understanding is consistent with the disclosure of the '492 patent, which shows a fuse as the "non-volatile programmable element" in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 3:10-23, 7:24-36.) Indeed, the

specification explicitly states that F1 corresponds to the "non-volatile programmable element" and can be a "fuse." (Ex. 1001 at 7:24-36.) Moreover, claim 18, which depends from claim 14 recites "wherein the programmable element is a fuse," thereby demonstrating that a fuse is a "non-volatile programmable element" in the context of claim 14 and the '492 patent. (*Id.* at 10:38-39; Ex. 1002 at ¶81.)

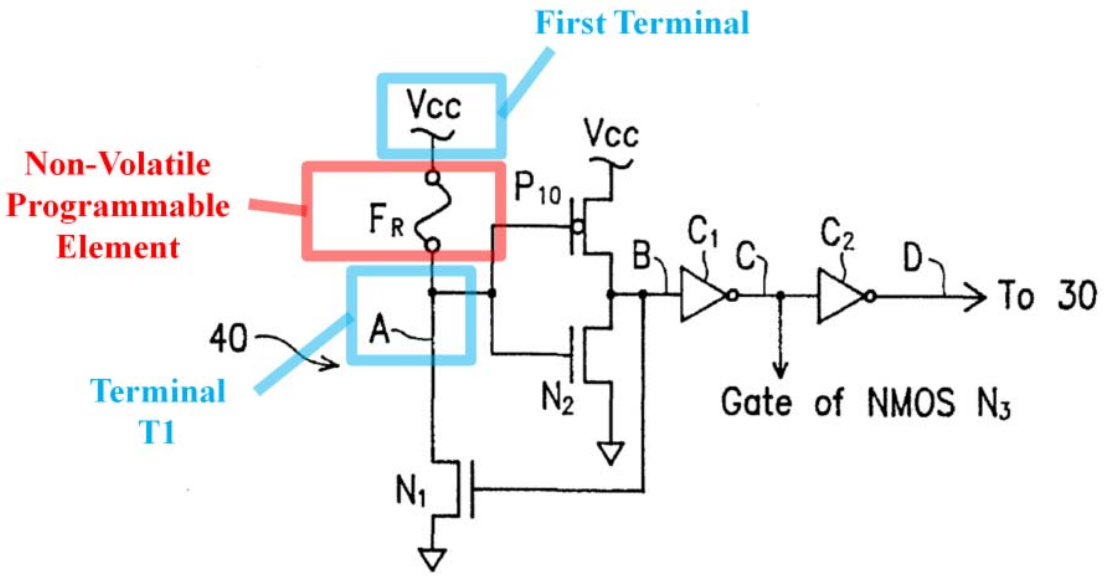


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶81.)

As shown in annotated figure 4 above, the fuse F_R ("non-volatile programmable element") is coupled between V_{CC} ("first terminal") and node A

("terminal T1") and therefore constitutes "a non-volatile programmable element connected to the terminal T1 and the first terminal." (Ex. 1002 at ¶82.)

If the fuse F_R is not blown and therefore "conductive," the fuse provides an electrical connection between V_{CC} ("first terminal") and node A ("terminal T1"). (Ex. 1005 at 5:4-5; s*ee* citations and discussion regarding the operation of the circuit in figure 5 of Fu at Section IX.A.1(a) *supra*.) Therefore, Fu discloses "the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive." (Ex. 1002 at ¶83.)

If the fuse F_R is blown and therefore "non-conductive," the fuse does not provide an electrical connection between V_{CC} ("first terminal") and node A ("terminal T1"), nor does any other circuit element. (Ex. 1005 at 5:19-25; s*ee* citations and discussion regarding the operation of the circuit in figure 5 of Fu at Section IX.A.1(a) *supra*; Ex. 1002 at ¶84.) Thus, "terminal T1" is isolated from the "first terminal." (Ex. 1002 at ¶84.) Therefore, Fu discloses "the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive."

As shown in annotated figure 2A of the '492 patent below, the "non-volatile programmable element" highlighted in figure 4 of Fu above is consistent with the

"non-volatile programmable element" disclosed by the '492 patent. (Ex.1002 at ¶85.)

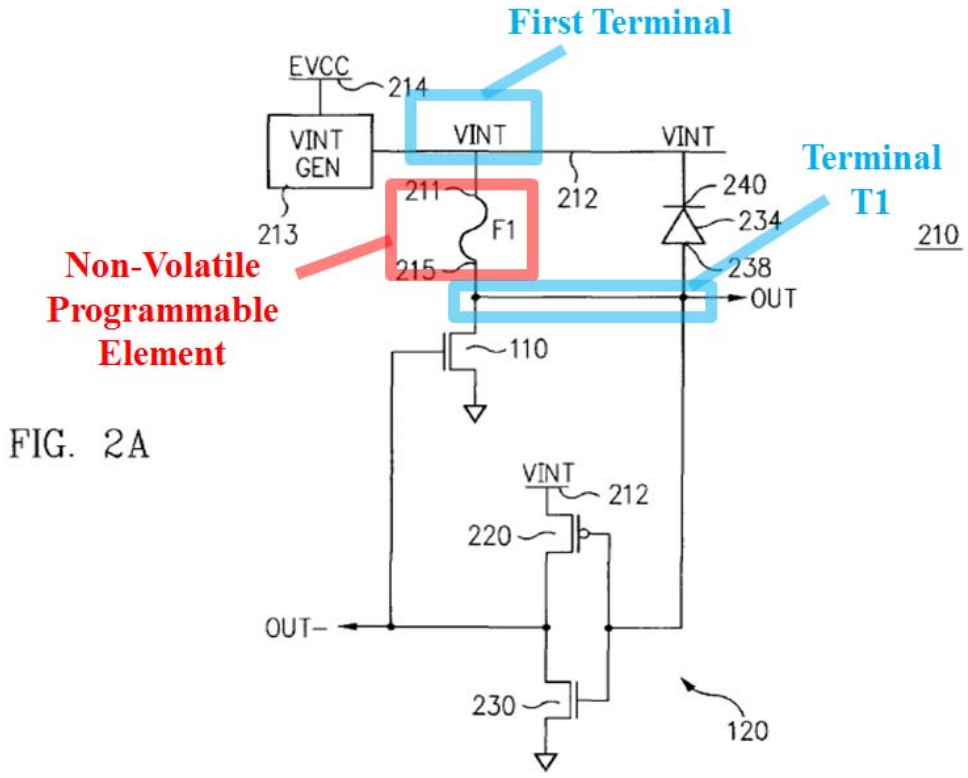


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶85.)

f) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and

Fu discloses this feature. (Ex. 1002 at ¶¶86-89.) For example, the NMOS transistor N_1 highlighted below in annotated figure 4 of Fu is a "variable-impedance electrical path." Such an understanding is consistent with the disclosure of the '492 patent, which shows an NMOS transistor as the "variable-impedance electrical path" in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A,

7:57-66.) Moreover, claim 19, which depends from claim 14 recites "wherein the variable-impedance electrical path is an NMOS transistor," thereby demonstrating that an NMOS transistor is a "variable-impedance electrical path" in the context of claim 14 and the '492 patent. (*Id*. at 10:38-39; Ex. 1002 at ¶86.)

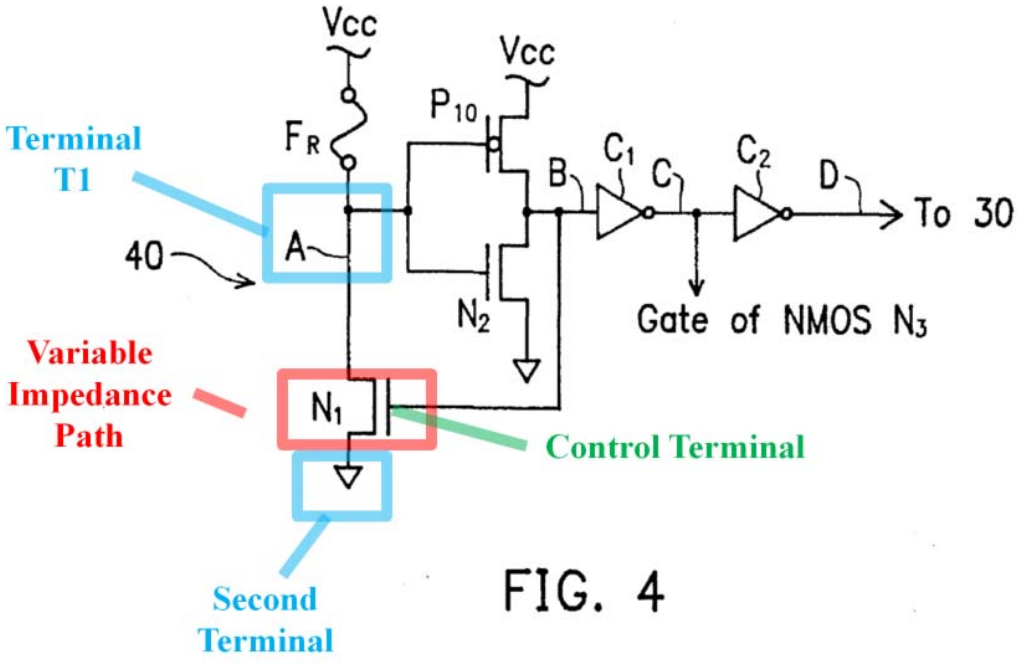


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶86.)

As shown in annotated figure 4 above, the NMOS transistor N_1 ("variable-impedance electrical path") is coupled between node A ("terminal T1") and GND ("second terminal") and therefore constitutes "variable-impedance electrical path connected between the terminal T1 and the second terminal." (Ex. 1002 at ¶87.)

The NMOS transistor N_1 ("variable impedance path") has a gate terminal ("having a control terminal") that determines whether the NMOS transistor is on or

off, where the impedance of the transistor is different when it is on as opposed to when it is off ("for controlling the impedance of the variable-impedance path"). (Ex. 1005 at 5:5-7, 5:26-28; Ex. 1002 at ¶88.)

As shown in annotated figure 2A of the '492 patent below, the "variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path" highlighted in figure 4 of Fu above is consistent with the "variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path" disclosed by the '492 patent. (Ex.1002 at ¶89.)

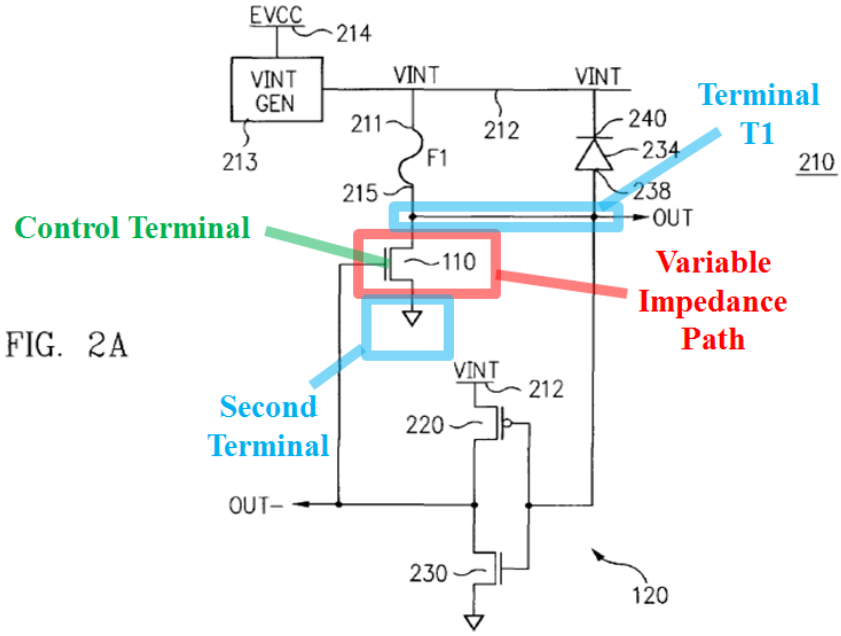


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶89.)

g) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

Fu discloses this feature. (Ex. 1002 at ¶¶90-95.) For example, annotated figure 4 of Fu below shows an inverter that includes transistors P_{10} and N_2. (Ex. 1005 at FIG. 4, 4:23-30, "The PMOS transistor P_{10} and the other NMOS transistor N_2 are also connected in series, with the PMOS end of this connection tied to V_{CC} and the NMOS end tied to ground. The gates of the P_{10} and N_2 transistors are tied together and are connected to the joint node A of the fuse element F_R and N_1 series connection. The gate of the transistor N_1 is connected to the joint node B of the P_{10} and N_2 transistor series connection. . . ."; Ex. 1002 at ¶90.) The gates of transistors P_{10} and N_2 ("the input of the inverter") are connected to the node A ("terminal T1"). (Ex. 1002 at ¶90.) The output of the inverter at node B is connected to the gate of the transistor N_1 ("an output connected to the control terminal of the variable-impedance path"). (*Id*. at ¶91.)

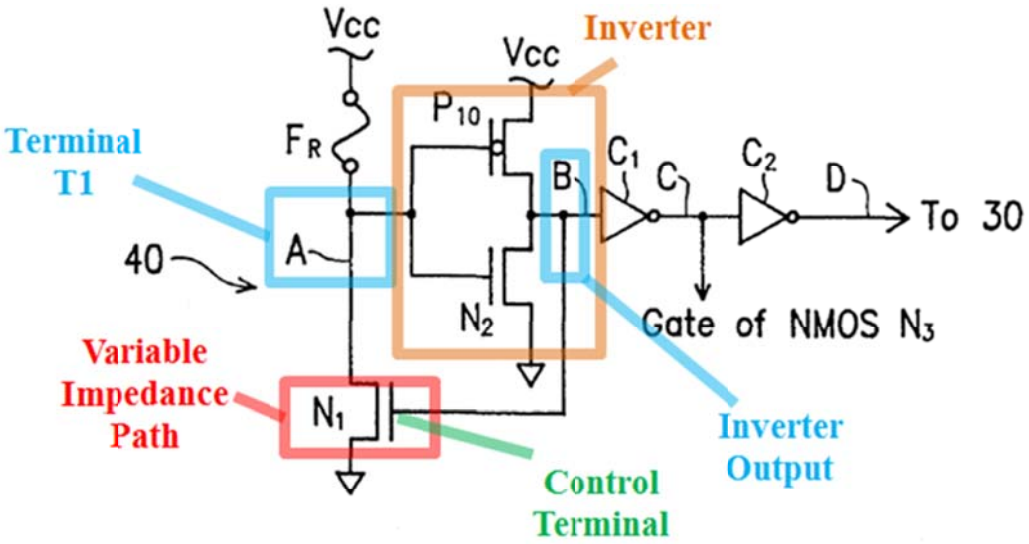


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶91.)

A POSITA would have understood that P_{10} and N_2 form an "inverter." (Ex. 1002 at ¶92.) Indeed, the circuit formed by P_{10} and N_2 is just like the "CMOS inverter 120 formed by pull-up transistor 220 and NMOS pull-down transistor 230" in the'492 patent. (Ex. 1001 at 3:24-32, FIG. 2A; Ex. 1002 at ¶92.)

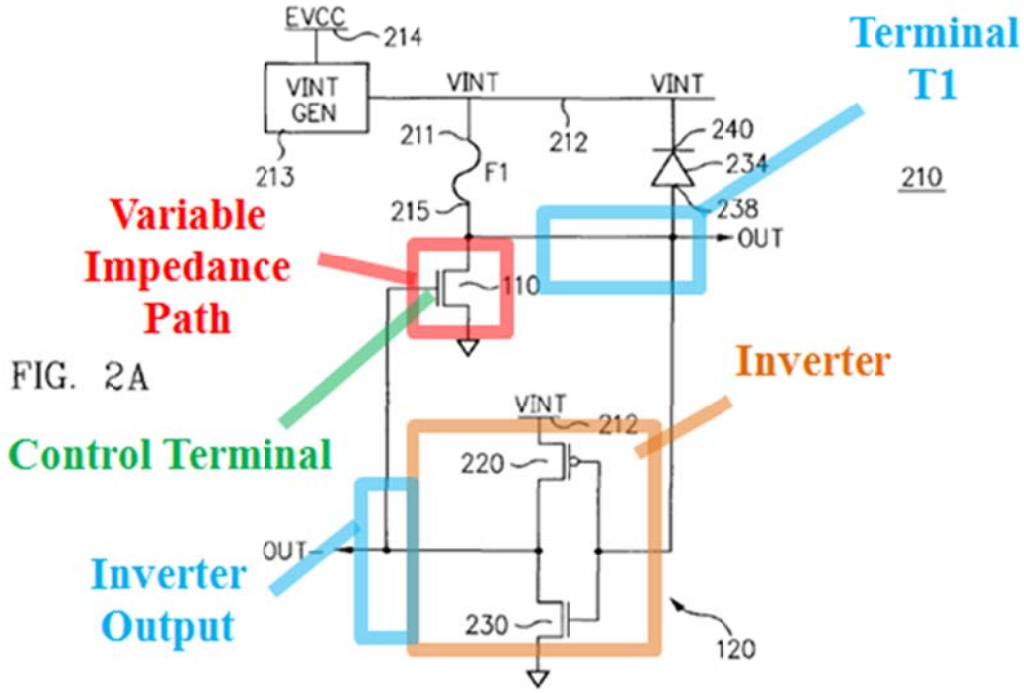


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶92.)

As shown in annotated figure 4 below, the inverter in Fu includes PMOS transistor P_{10} ("pull-up device") coupled between the inverter output node B and V_{CC}, where, when the PMOS transistor P_{10} is on, it pulls the voltage on the inverter output node B up to V_{CC} and therefore would be understood to operate as a "pull-up" transistor in the inverter. (Ex. 1005 at FIG. 4, 4:23-30; Ex. 1002 at ¶93.) Similarly, the inverter includes NMOS transistor N_2 ("pull-down device") coupled between the inverter output node B and GND, where, when the NMOS transistor N_2 is on, it pulls the voltage on the inverter output node 15 down to GND and therefore would be understood to operate as a "pull-down" transistor in the inverter. (*Id.*)

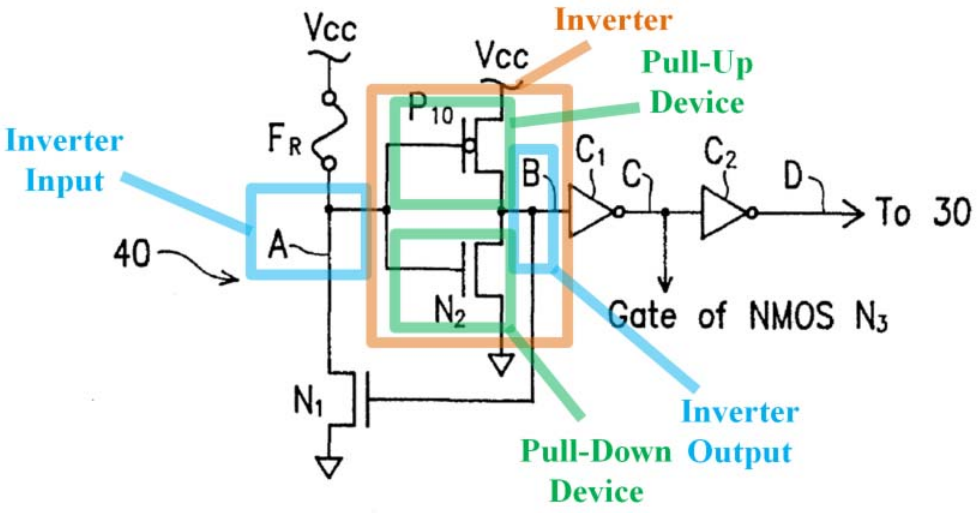


FIG. 4

(*Id*. at FIG. 4 (annotated); Ex. 1002 at ¶93.)

As shown in annotated figure 4 above, both the PMOS transistor P_{10} ("pull-up device") and the NMOS transistor N_2 ("pull-down device") are coupled to the inverter input at node A and the inverter output at node B ("at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output"). (Ex. 1005 at FIG. 4, 4:23-30; Ex. 1002 at ¶94.)

The disclosure of P_{10} and N_2 of Fu as "pull-up" and "pull-down" devices, respectively, is consistent with the disclosure of the '492 patent, which shows an inverter including PMOS transistor 220 ("pull-up device") and an NMOS transistor

("pull-down device") in figure 2A. (Ex. 1001 at 3:24-32, FIG. 2A; Ex. 1002 at ¶95.)

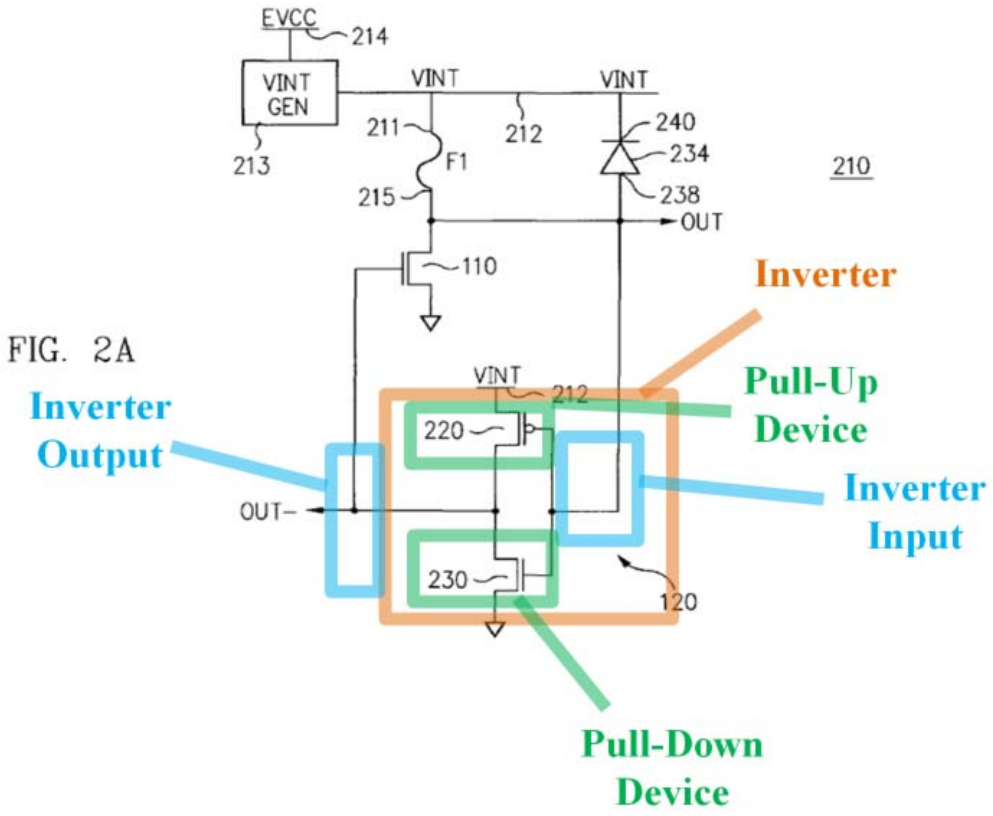


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶95.)

2. Claim 15

a) The programmable latch of claim 14 wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.

Fu discloses this feature. (Ex. 1002 at ¶¶96-98.) As shown in annotated figure 4 of Fu below, the "redundancy activation circuit" ("programmable latch") of Fu does not receive any inputs from outside of the circuit as illustrated. (Ex.

1005 at FIG. 4.) As discussed above with respect to claim feature 14[a], when the circuit of figure 4 is operational, the voltage at node A ("terminal T1") is only influenced by the electrical potentials applied on the Vcc and GND terminals ("first and second terminals") and the state of the fuse F_R ("programmable element"). (*Id*. at 4:67-5:29; *see supra* Section IX.A.1(a); Ex. 1002 at ¶96.) Specifically, if the fuse is not blown, node A is at Vcc and when the fuse is blown, node A is at GND. (*Supra* Section IX.A.1(a); Ex. 1005 at 4:67-5:29; Ex. 1002 at ¶97.)

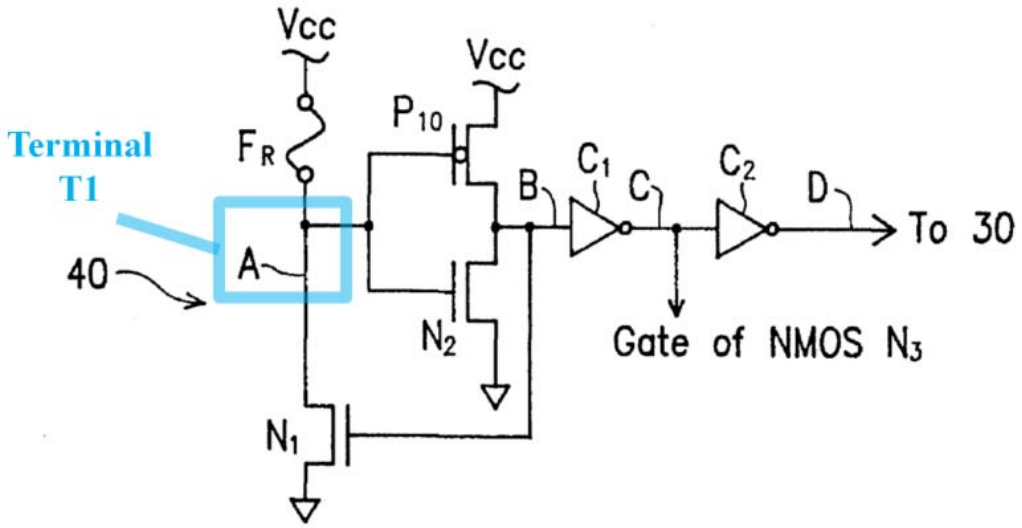


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶97.)

Therefore, Fu discloses "wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals." (Ex. 1002 at ¶98.)

3. Claim 16

a) The programmable latch of claim 14 wherein the latch does not receive any latch initialization signal from outside the latch.

Fu discloses this feature. (Ex. 1002 at ¶¶99-100.) As shown in figure 4 of Fu below, the "redundancy activation circuit" ("programmable latch") of Fu does not receive any inputs from outside of the circuit illustrated and the state of the latch is completely determined by the state of the fuse F_R and the voltages on the Vcc and GND terminals. (*See supra* Section IX.A.2; Ex. 1005 at 4:66-5:29, FIG. 4; Ex. 1002 at ¶99.)

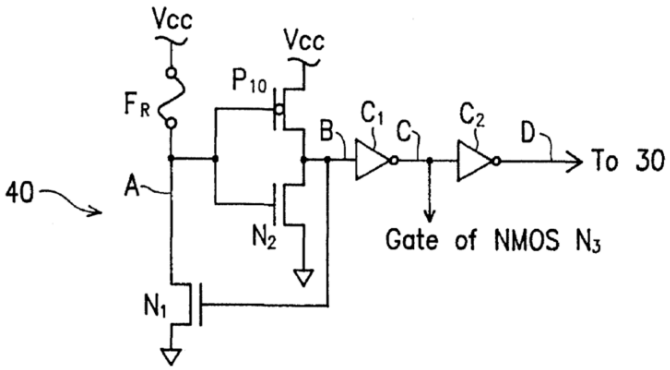


FIG. 4

(Ex. 1005 at FIG. 4.)

Therefore, Fu discloses "wherein the latch does not receive any latch initialization signal from outside the latch." (Ex. 1002 at ¶100.)

4. Claim 17

a) The programmable latch of claim 14 wherein the second terminal is to receive a ground voltage throughout operation of the latch.

Fu discloses this feature. (Ex. 1002 at ¶¶101-102.) As discussed above with respect to claim element 14[c], when the "redundancy activation circuit" ("programmable latch") is operational, the second terminal is connected to ground (GND). (Ex. 1005 at 3:46-51, "The memory redundancy circuitry 2, which comprises the redundancy activation circuit 40 and programmable redundancy decoder logic 30, operates between two electric potentials, i.e., the high (Vcc) and low (GND) levels together with its host main memory cell array of the entire memory device.", 4:20-23, "As can be seen in the drawing, the fuse element F_R is connected in series with the NMOS transistor N_1, with the other end of fuse element tied to V_{CC}, and the transistor end tied to *ground*.", emphasis added; *see supra* Section IX.A.1(c); Ex. 1002 at ¶101.)

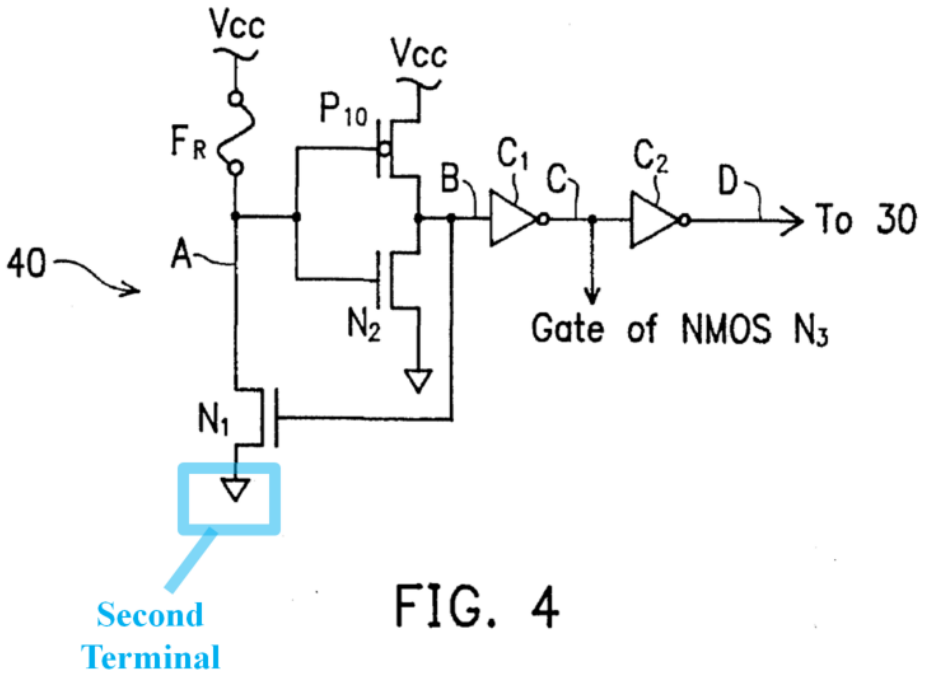


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶101.)

Therefore, Fu discloses that "the second terminal is to receive a ground voltage throughout operation of the latch" as recited in claim 17. (Ex. 1002 at ¶102.)

5. Claim 18

a) The programmable latch of claim 14 wherein the programmable element is a fuse.

Fu discloses this feature. (Ex. 1002 at ¶103.) As demonstrated above with respect to claim feature 14[e], the fuse F_R shown in annotated figure 4 below is a "non-volatile programmable element." (*See supra* Section IX.A.1(e).) Therefore, Fu discloses "wherein the programmable element is a fuse."

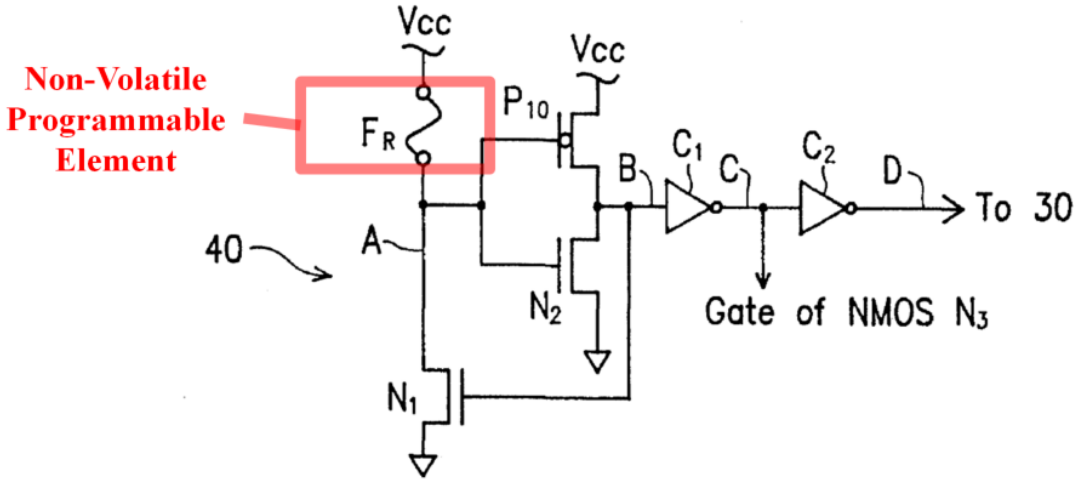


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶103.)

6. Claim 19

a) The programmable latch of claim 14 wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.

Fu discloses this feature. (Ex. 1002 at ¶¶104-105.) As demonstrated above with respect to claim feature 14[f], the NMOS transistor N_1 in annotated figure 4 below corresponds to the claimed "variable impedance electrical path." (*See supra* Section IX.A.1(f).) Therefore, Fu discloses "wherein the variable-impedance path is an NMOS transistor." (Ex. 1002 at ¶104.)

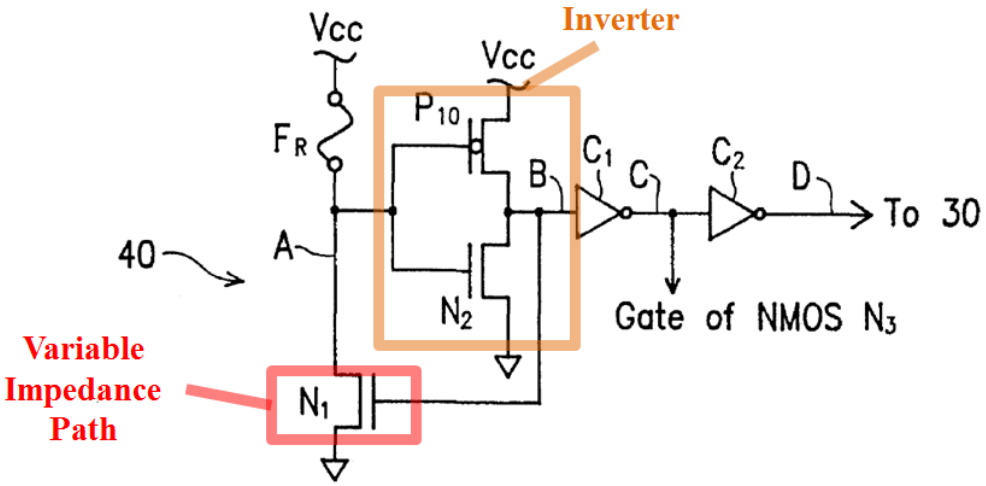


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶104.)

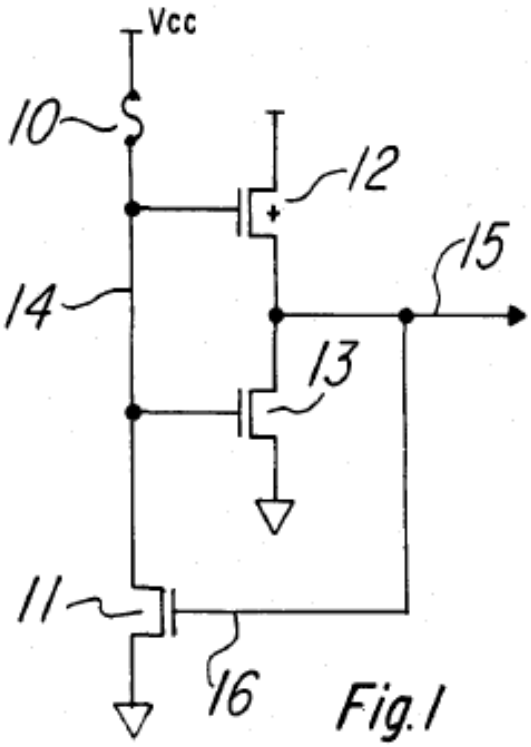
Similarly, as demonstrated above with respect to claim feature 14[g], PMOS transistor P_{10} and NMOS transistor N_2 together disclose the claimed "inverter." (*See supra* Section IX.A.1(g).) The inverter formed by PMOS transistor P_{10} and NMOS transistor N_2 is a "CMOS inverter" as it includes both NMOS and PMOS transistors (i.e., complementary MOS "CMOS" transistors). (Ex. 1002 at ¶105.) Such an understanding is consistent with the disclosure of the '492 patent. (*Id.*; Ex. 1001 at 3:24-26, "Terminal OUT is connected to the input of CMOS inverter 120 formed by PMOS pull-up transistor 220 and NMOS pull-down transistor 230.") Therefore, Fu discloses "wherein . . . the inverter is a CMOS inverter" as recited in claim 19. (Ex. 1002 at ¶105.)

B. Ground 2: McAdams Anticipates Claims 14-19

1. Claim 14

a) A programmable latch comprising:

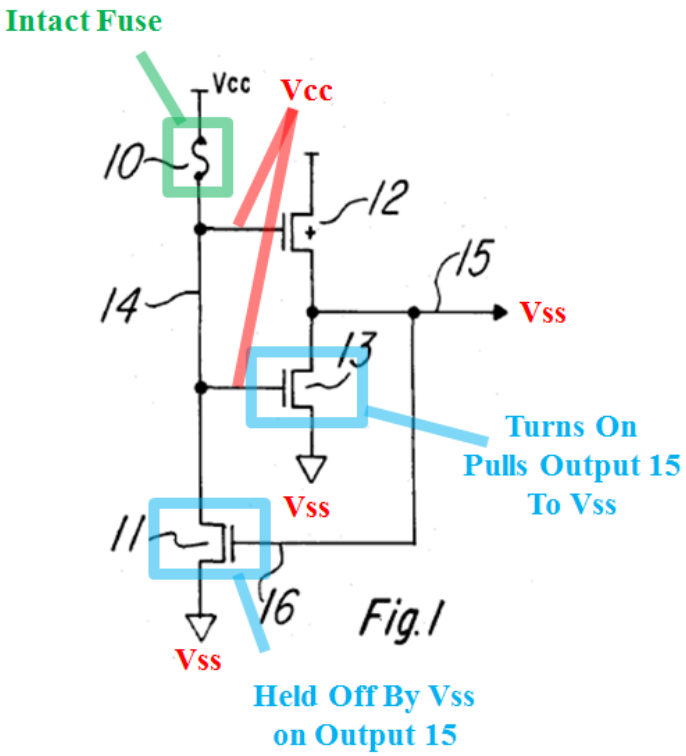
To the extent the preamble is limiting, McAdams discloses this feature. (Ex. 1002 at ¶¶107-113.) For example, McAdams discloses a fuse circuit depicted in figure 1.



(Ex. 1006 at FIG. 1.)

The fuse circuit of figure 1 includes a fuse 10, a feedback transistor 11, and an inverter that includes P-channel transistor 12 and N-channel transistor 13. (*Id.* at 1:67-2:7.) The fuse circuit of figure 1 produces an output 15, which is fed back to the gate of the transistor 11. (*Id.* at 2:3-7.)

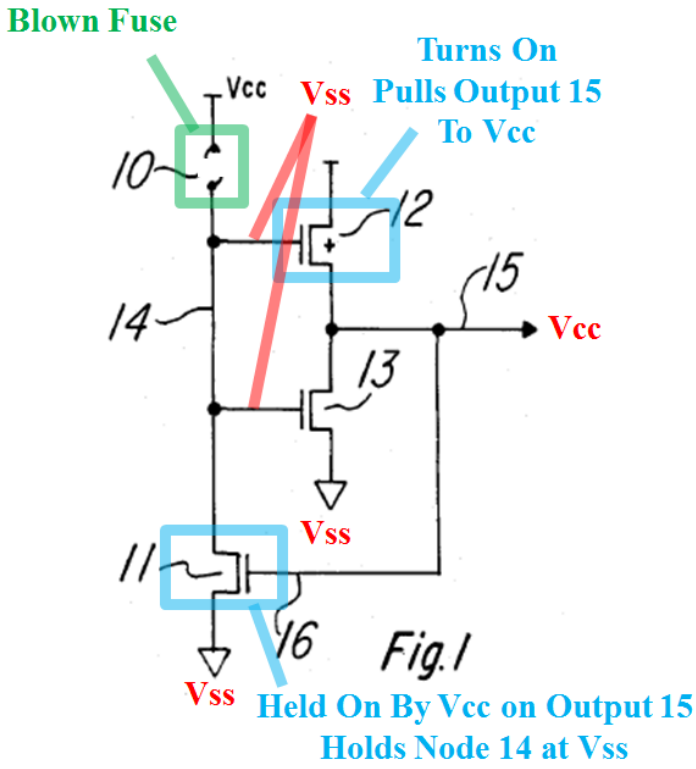
In the operational scenario depicted in annotated figure 1 below, if the fuse 10 is intact and has not been blown when power is applied to the circuit, the node 14 follows the power supply Vcc, which turns on transistor 13. (*Id*. at 2:8-15.) When transistor 13 turns on, any charge on the output node 15 is discharged, pulling the output 15 to Vss. (*Id*.) The Vss voltage on the output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state. (*Id*. at 2:8-18; Ex. 1002 at ¶¶109-110.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶110.)

In the alternate operational scenario where the fuse has been blown, which is depicted in the demonstrative below, the node 14 is at Vss when power is applied.

(Ex. 1006 at 2:21-22; Ex. 1002 at ¶111.) Because the gate of P-channel transistor 12 is at Vss, transistor 12 turns on and the output node 15 is pulled to Vcc. (Ex. 1006 at 2:22-24.) The Vcc voltage on the output is fed back to the gate of transistor 11, which turns transistor 11 on and holds the node 14 at Vss. (*Id.* at 2:24-26; Ex. 1002 at ¶111.) Holding node 14 at Vss ensures that the P-channel transistor 12 remains on and the output 15 is held is Vcc. (Ex. 1006 at 21-26.)

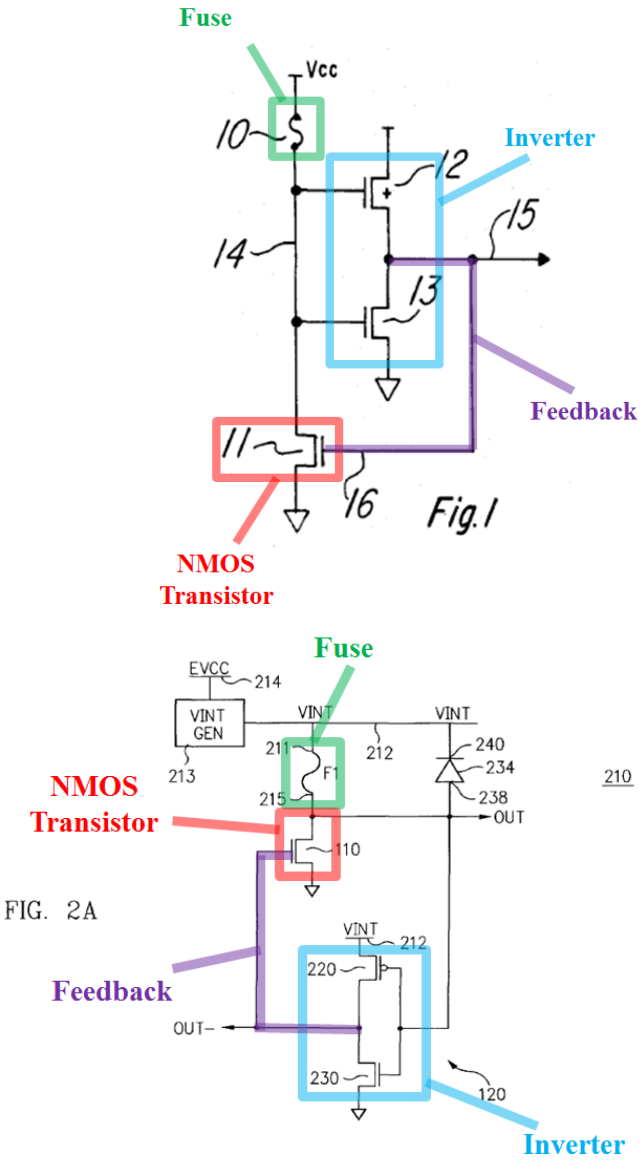


(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶111.)

Therefore, based on whether the fuse 10 has been blown or is intact, the output 15 of the fuse circuit shown in figure 1 will be held at either Vcc or Vss. (Ex. 1006 at 2:8-26; 1002 at ¶112.) The feedback of the output of the inverter to

the transistor 11 holds that output at Vcc or Vss. (Ex. 1002 at ¶112.) Therefore, the output is latched at either Vcc or Vss based on whether or not the fuse is blown. (*Id*.) A person of ordinary skill in the art would have recognized that the fuse circuit constitutes a "programmable latch" where the programming corresponds to the state of the fuse, which determines the latched value at the output. (*Id*.)

Indeed, the fuse circuit of McAdams corresponds to a "programmable latch" in the same manner as that disclosed in the figure 2A of the '492 patent. (*Id.* at ¶113.) As shown below, the programmable latch shown in figure 2A of the '492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the fuse circuit in figure 1 of McAdams. (Ex. 1001 at FIG. 2A; Ex. 1006 at FIG. 1; *see infra* Sections IX.B.1(b)-(g) for analysis regarding remaining elements below of claim 14.)

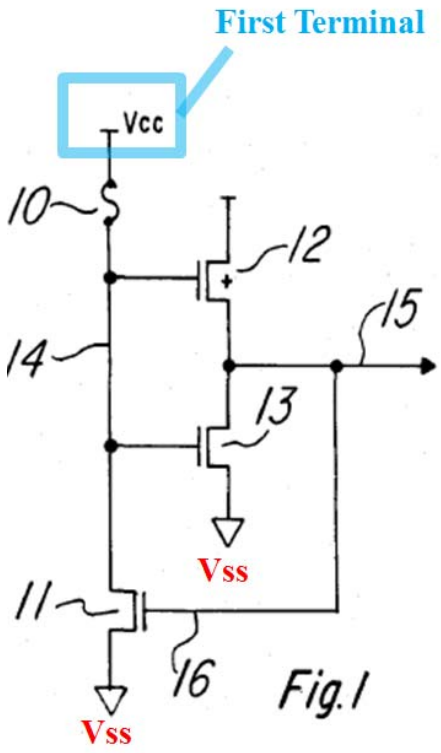


(Ex. 1006 at FIG. 1 (annotated) (top); Ex. 1001 at FIG. 2A (annotated) (bottom); Ex. 1002 at ¶113.)

b) a first terminal for receiving a constant non-ground voltage throughout operation of the latch;

McAdams discloses this feature. (Ex. 1002 at ¶¶114-115.) As shown in annotated figure 1 below, the "programmable latch" of McAdams includes a

"terminal" Vcc, where Vcc is a "supply voltage" that is applied when power is applied to the circuit of figure 1. (Ex. 1006 at 2:2-3, "series circuit is connected between a supply voltage Vcc and Vss", 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v", 3:24-26, "wherein said one of the first and second terminals of said power supply is a positive voltage and said other is ground", 4:20-22, "a power supply having a first terminal at a positive voltage and a second terminal at a ground potential".) In the example embodiment of McAdams, Vcc is at +5 v after power up of the latch and therefore constitutes "a constant non-ground voltage throughout operation of the latch." (Ex. 1002 at ¶114.) Therefore, the terminal highlighted in blue below constitutes a "first terminal for receiving a constant non-ground voltage throughout operation of the latch." (*Id.*)



(*Id*. at FIG. 1 (annotated); Ex. 1002 at ¶114.)

As shown in annotated figure 2A of the '492 patent below, the "first terminal" highlighted in figure 1 of McAdams above is consistent with the "first terminal" disclosed by the '492 patent. (Ex.1002 at ¶115.)

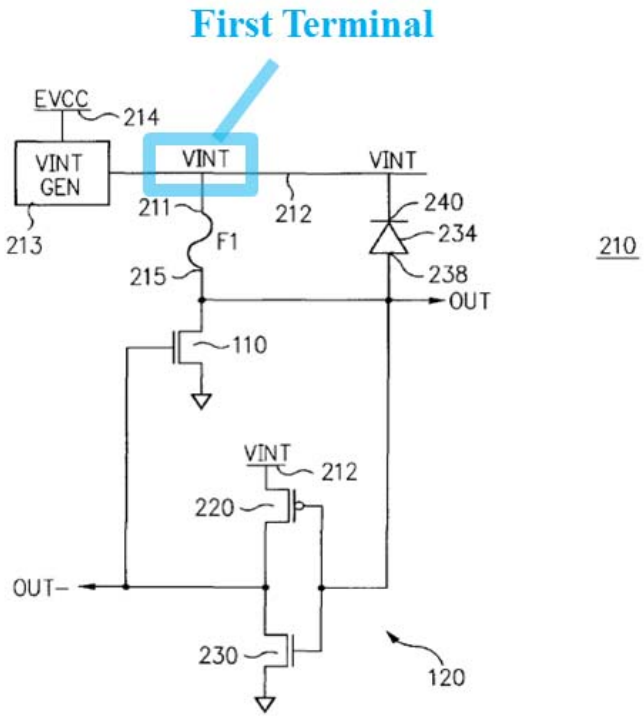
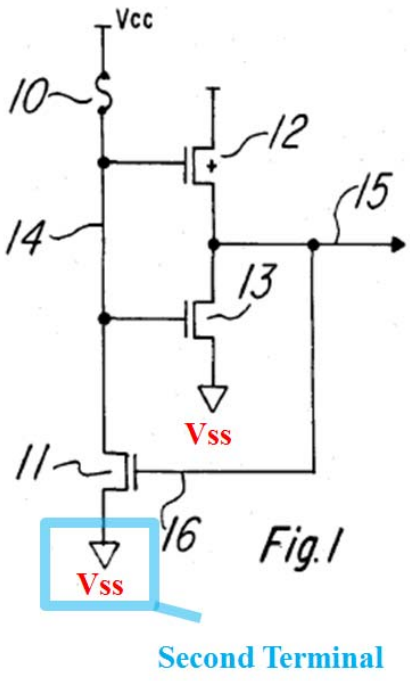


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶115.)

c) a second terminal for receiving a voltage;

McAdams discloses this feature. (Ex. 1002 at ¶¶116-117.) For example, the programmable latch circuit in figure 1 of McAdams includes a terminal ("second terminal") for receiving Vss ("a voltage"). (Ex. 1006 at 2:2-3, "series circuit is connected between a supply voltage Vcc and Vss", 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v", 2:14-17, "[T]he transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to Vcc transition.) Therefore, McAdams discloses "a second terminal for receiving a voltage." (Ex. 1002 at ¶116.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶116.)

As shown in annotated figure 2A of the '492 patent below, the "second terminal" highlighted in figure 1 of McAdams above is consistent with the "second terminal" disclosed by the '492 patent. (Ex.1002 at ¶117.)

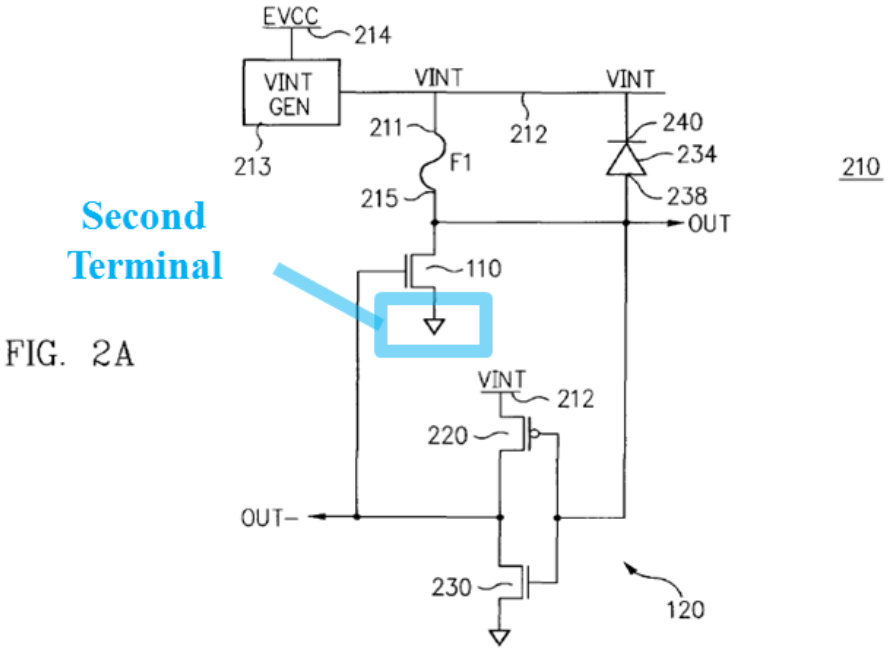


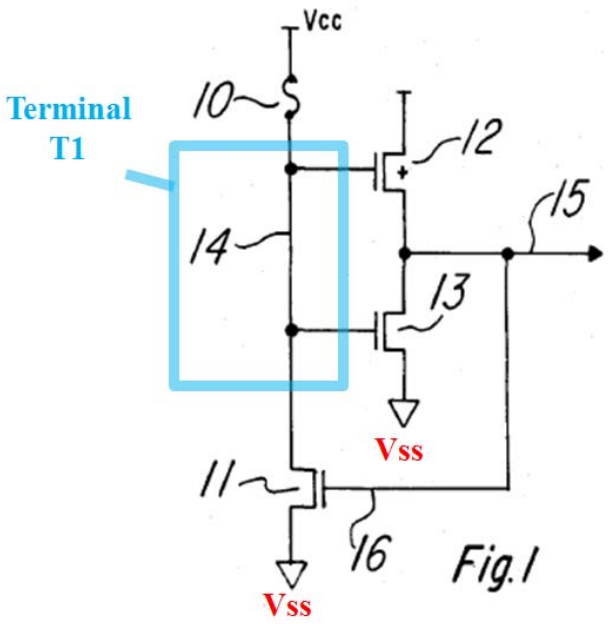
FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶117.)

d) a terminal T1 for providing a signal indicating a state of the programmable latch;

McAdams discloses this feature. (Ex. 1002 at ¶¶118-119.) For example, as shown in annotated figure 1 below, the node 14 indicates the state of the fuse, which corresponds to the state of the programmable latch ("a terminal T1 for providing a signal indicating a state of the programmable latch"). (*Id.*) As discussed above with respect to claim element 14[a], when power is applied to the latch, if the fuse is intact, node 14 is at Vcc (high), but if the fuse is blown, node 14 is at Vss (low). (*See* citations and discussion regarding the operation of the circuit in figure 1 of McAdams at Section IX.B.1(a) *supra*.) Therefore, the voltage at

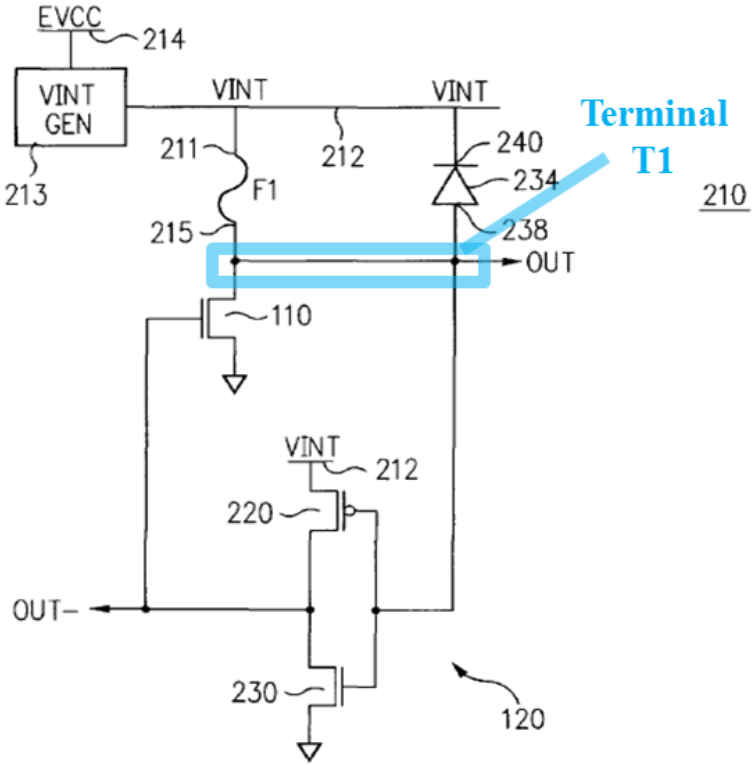
node 14 indicates a "state of the programmable latch" because it indicates whether the fuse is blown or not. (Ex. 1002 at ¶118.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶118.)

As shown in annotated figure 2A of the '492 patent below, the "terminal T1" highlighted in figure 1 of McAdams above is consistent with the "terminal T1" disclosed by the '492 patent. (Ex.1002 at ¶119.)

FIG. 2A

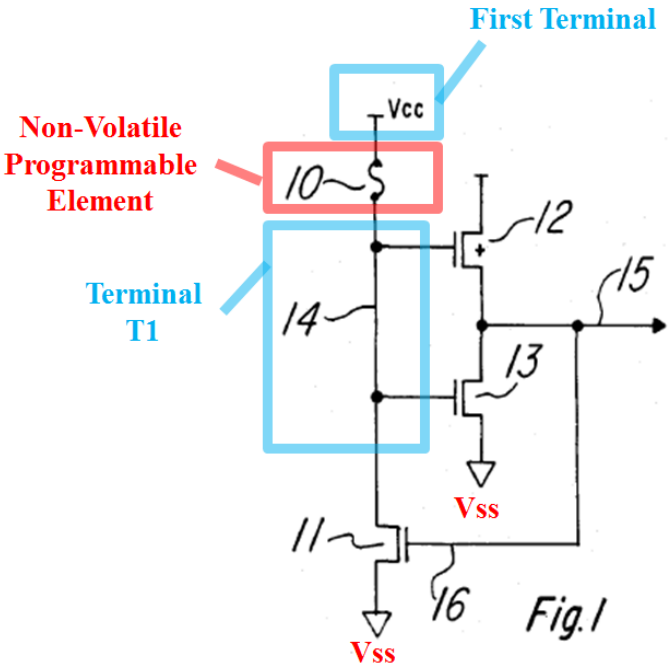


(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶119.)

e) a non-volatile programmable element connected to the terminal T1 and the first terminal, the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive, the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive;

McAdams discloses this feature. (Ex. 1002 at ¶¶120-124.) For example, the fuse 10 shown in annotated figure 1 below is a "non-volatile programmable element." (*Id.*) Such an understanding is consistent with the disclosure of the '492 patent, which shows a fuse as the "non-volatile programmable element" in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 3:10-23, 7:24-36.) Moreover,

claim 18, which depends from claim 14 recites "wherein the programmable element is a fuse," thereby demonstrating that a fuse is a "non-volatile programmable element" in the context of claim 14 and the '492 patent. (*Id.* at 10:38-39; Ex. 1002 at ¶120.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶120.)

As shown in annotated figure 1 above, the fuse 10 ("non-volatile programmable element") is coupled between Vcc ("first terminal") and node 14 ("terminal T1") and therefore constitutes "a non-volatile programmable element connected to the terminal T1 and the first terminal." (Ex. 1002 at ¶121.)

If the fuse 10 is intact and therefore "conductive," the fuse provides an electrical connection between Vcc ("first terminal") and node 14 ("terminal T1").

(Ex. 1006 at 2:8-11; *see* citations and discussion regarding the operation of the circuit in figure 5 of McAdams at Section IX.B.1(a) *supra*.) Therefore, *McAdam*s discloses "the programmable element providing a conductive path between the terminal T1 and the first terminal when the programmable element is conductive." (Ex. 1002 at ¶122.)

If the fuse 10 is blown and therefore "non-conductive," the fuse does not provide an electrical connection between Vcc ("first terminal") and node 14 ("terminal T1"), nor does any other circuit element. (Ex. 1006 at 2:21-24 (explaining that even though Vcc is powered up, node 14 remains at Vss); *see* citations and discussion regarding the operation of the circuit in figure 5 of McAdams at Section IX.B.1(a) *supra*.) Thus, "terminal T1" is isolated from the "first terminal." (Ex. 1002 at ¶¶123.) Therefore, McAdams discloses "the programmable element isolating the terminal T1 from the first terminal when the programmable element is non-conductive." (*Id.*)

As shown in annotated figure 2A of the '492 patent below, the "non-volatile programmable element" highlighted in figure 1 of McAdams above is consistent with the "non-volatile programmable element" disclosed by the '492 patent. (Ex.1002 at ¶124.)

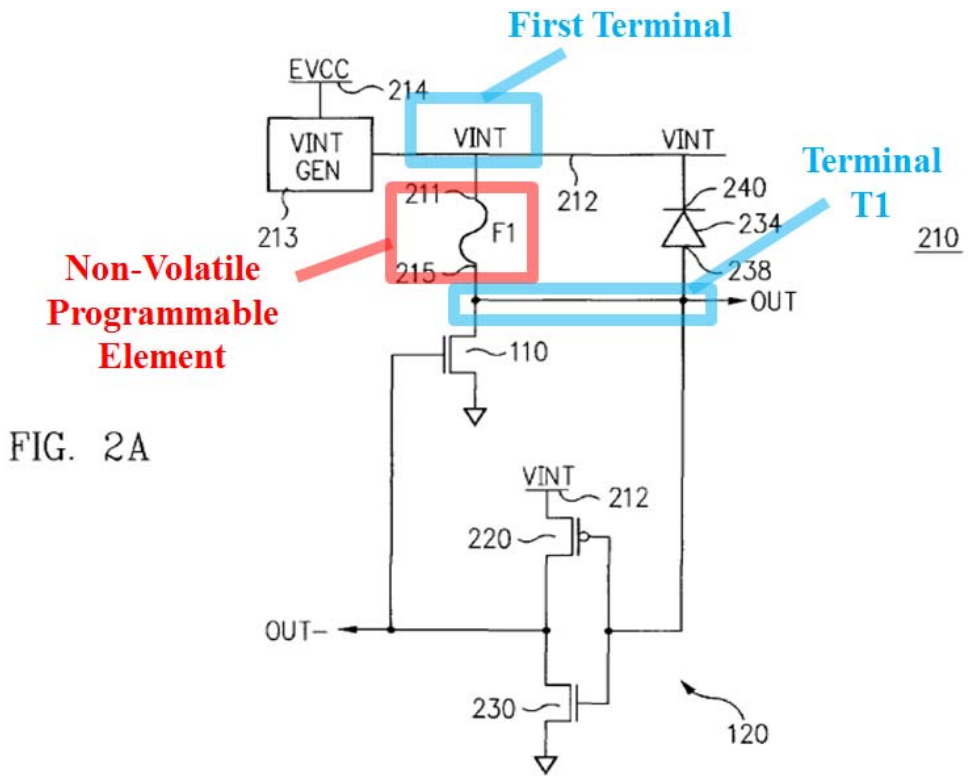


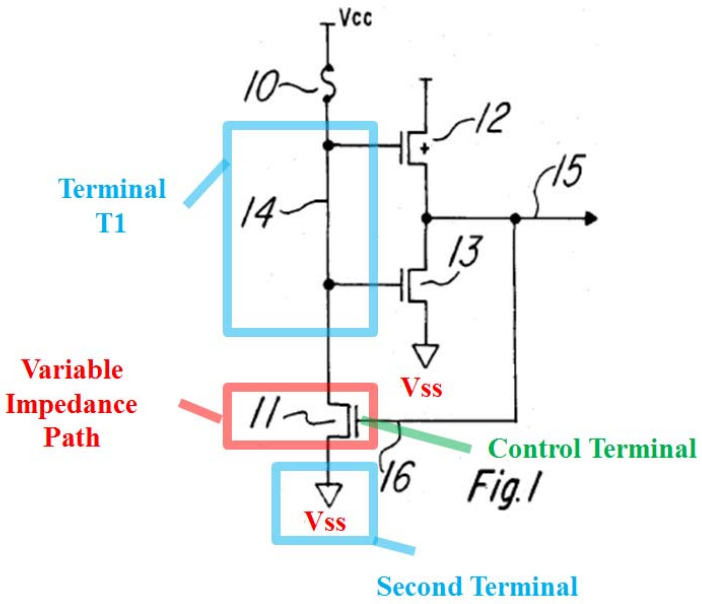
FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶124.)

f) a variable-impedance electrical path connected between the terminal T1 and the second terminal, the variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path; and

McAdams discloses this feature. (Ex. 1002 at ¶¶125-128.) For example, the N-channel (NMOS) transistor 11 highlighted below in annotated figure 1 is a "variable-impedance electrical path." (*Id.* at ¶125.) Such an understanding is consistent with the disclosure of the '492 patent, which shows an NMOS transistor as the "variable-impedance electrical path" in the embodiment of figure 2A. (Ex. 1001 at FIG. 2A, 7:57-66.) Moreover, claim 19, which depends from claim 14 recites "wherein the variable-impedance electrical path is an NMOS transistor,"

thereby demonstrating that an NMOS transistor is a "variable-impedance electrical path" in the context of claim 14 and the '492 patent. (*Id*. at 10:38-39; Ex. 1002 at ¶125.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶125.)

As shown in annotated figure 1 above, the NMOS transistor 11 ("variable-impedance electrical path") is coupled between node 14 ("terminal T1") and Vss ("second terminal") and therefore constitutes a "variable-impedance electrical path connected between the terminal T1 and the second terminal." (Ex. 1002 at ¶126.)

As shown in annotated figure 1 of McAdams above, the NMOS transistor 11 ("variable impedance path") has a gate terminal ("having a control terminal") that determines whether the NMOS transistor is on or off ("for controlling the

impedance of the variable-impedance path"). (Ex. 1006 at 2:14-18, 2:24-26; Ex. 1002 at ¶¶126-127.)

As shown in annotated figure 2A of the '492 patent below, the "variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path" highlighted in figure 1 of McAdams above is consistent with the "variable-impedance path having a control terminal for controlling the impedance of the variable-impedance path" disclosed by the '492 patent. (Ex. 1002 at ¶128; *see* Ex. 1001 at 3:31-32, 3:46-51.)

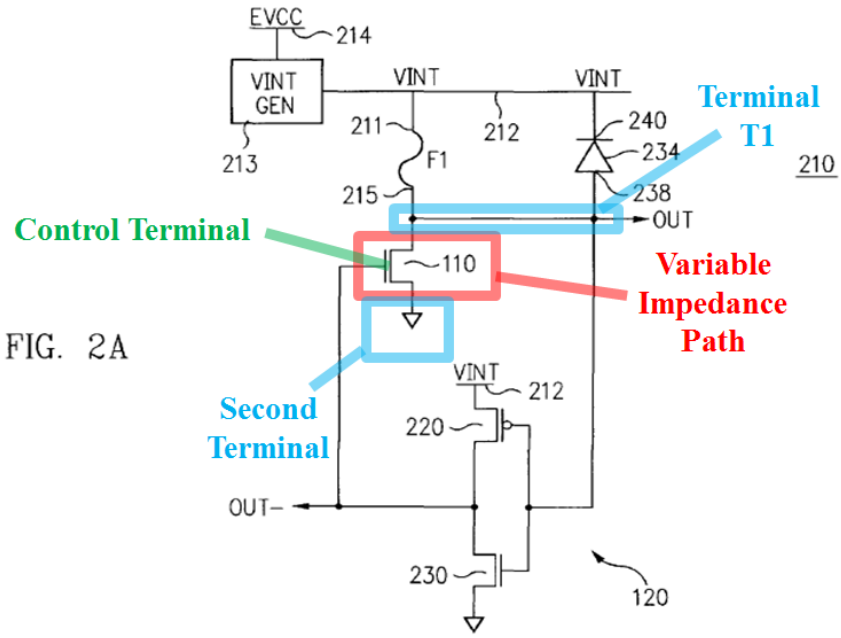
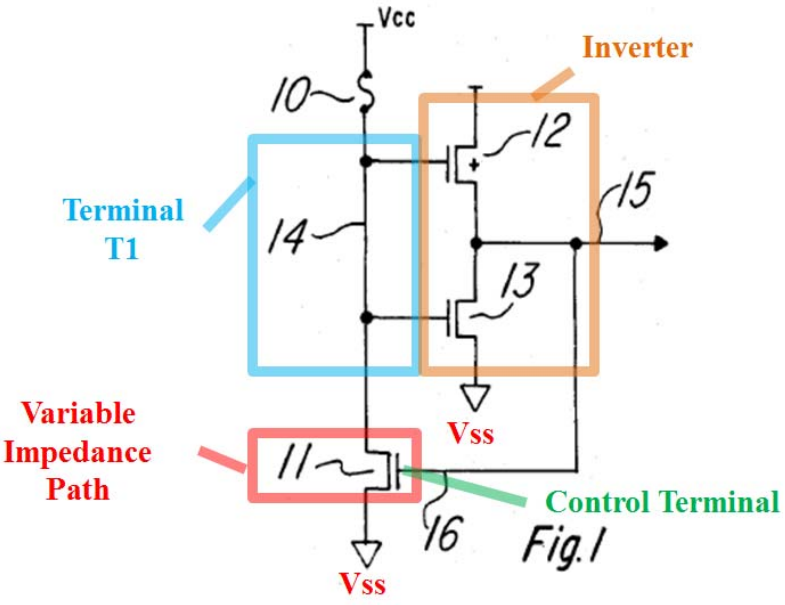


FIG. 2A

(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶128.)

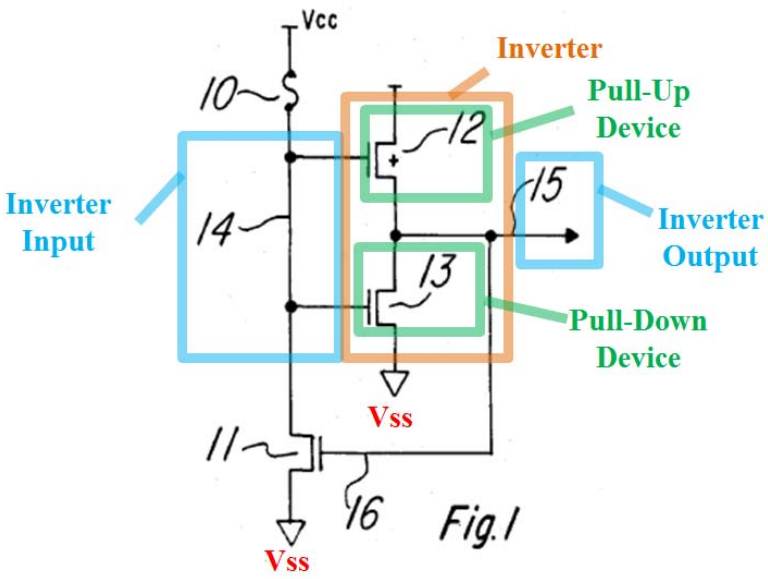
g) an inverter having an input connected to the terminal T1 and an output connected to the control terminal of the variable-impedance path, wherein the inverter has a pull-up device and a pull-down device, at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

McAdams discloses this feature. (Ex. 1002 at ¶¶129-132.) For example, annotated figure 1 of McAdams below shows an inverter that includes transistors 12 and 13. (Ex. 1006 at FIG. 1, 2:3-6, "A CMOS inverter including a P-channel transistor 12 and an N-channel transistor 13 has the node 14 as an input and produces an output 15.") The gates of transistors 12 and 13 ("the input of the inverter") are connected to the node 14 ("terminal T1"). (*Id*. at FIG. 1, 2:3-6.) The output 15 of the inverter is connected to the gate of the transistor 11 ("an output connected to the control terminal of the variable-impedance path"). (*Id*. at 2:6-7.)



(*Id*. at FIG. 1 (annotated); Ex. 1002 at ¶129.)

As shown in annotated figure 1 below, the inverter of McAdams includes P-channel transistor 12 ("pull-up device") coupled between the output 15 and Vcc, where, when the P-Channel transistor 12 is on, it pulls the voltage on output node 15 up to 5V and therefore would have been understood to operate as a "pull-up" transistor in the inverter. (Ex. 1002 at ¶130.) Similarly, the inverter includes N-channel transistor 13 ("pull-down device") coupled between the output 15 and Vss, where, when the N-Channel transistor 13 is on, it pulls the voltage on output node 15 down to Vss and therefore would have been understood to operate as a "pull-down" transistor in the inverter. (Ex. 1006 at FIG. 1, 2:3-6; Ex. 1002 at ¶130.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶130.)

As shown in annotated figure 1 above, both the P-channel transistor 12 ("pull-up device") and the N-channel transistor 13 ("pull-down device") are coupled to inverter input at node 14 and the inverter output 15 ("at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output"). (Ex. 1006 at FIG. 1, 2:3-6; Ex. 1002 at ¶131.)

The disclosure of transistors 12 and 13 of McAdams being "pull-up" and "pull-down" devices, respectively, is consistent with the disclosure of the '492 patent, which shows the inverter including PMOS transistor 220 ("pull-up device") and an NMOS transistor ("pull-down device") in figure 2A. (Ex. 1001 at 3:24-32, FIG. 2A; Ex. 1002 at ¶132.)

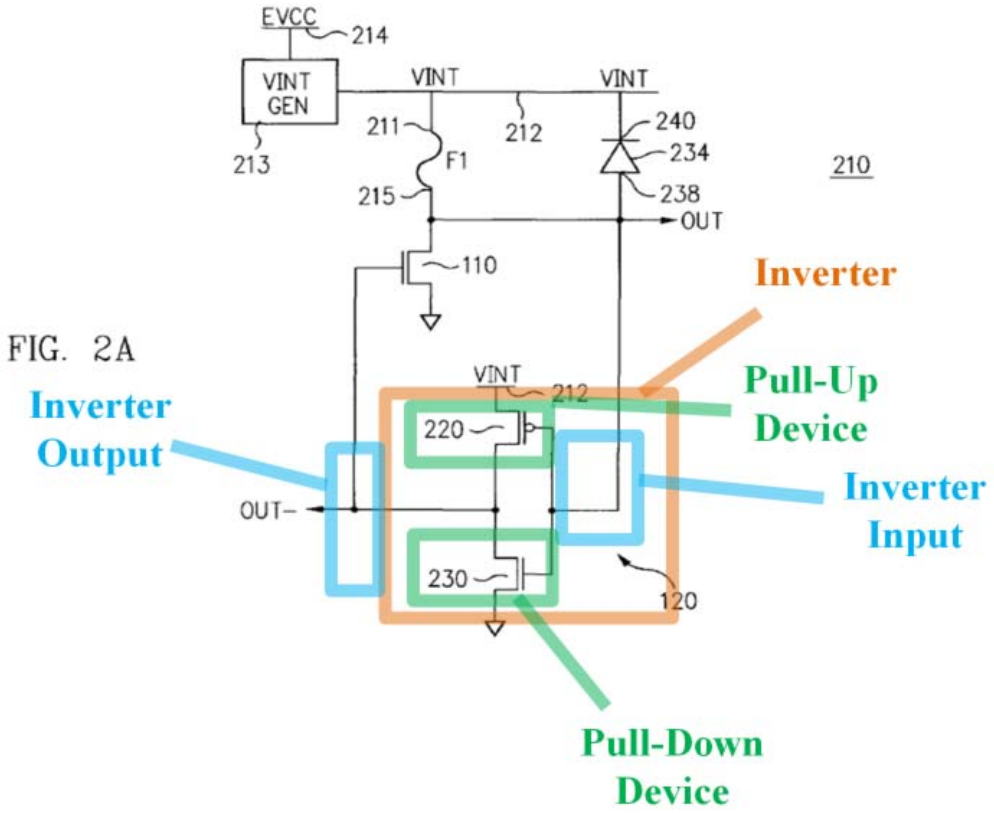


FIG. 2A

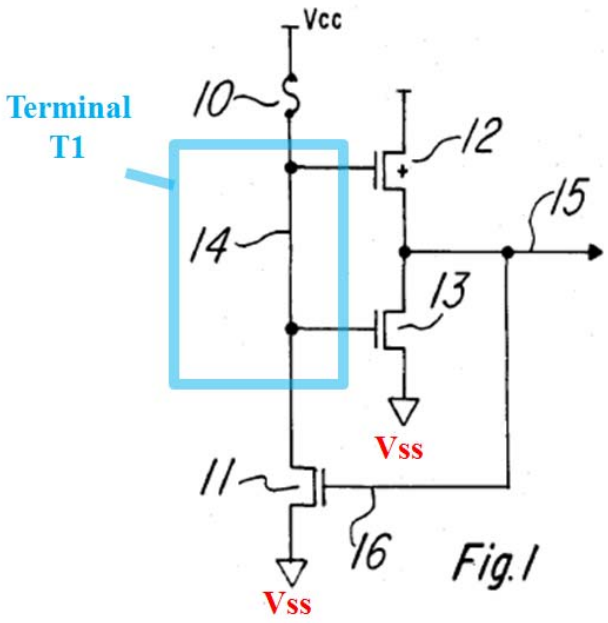
(Ex. 1001 at FIG. 2A (annotated); Ex. 1002 at ¶132.)

2. Claim 15

a) The programmable latch of claim 14 wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals.

McAdams discloses this feature. (Ex. 1002 at ¶¶133-134.) As shown in annotated figure 1 of McAdams below, the fuse circuit ("programmable latch") of McAdams does not receive any inputs from outside of the circuit illustrated. (Ex. 1006 at FIG. 1; Ex. 1002 at ¶133.) As discussed above with respect to claim feature 14[a], when power is applied, the voltage at node 14 ("terminal T1") is

only influenced by the power supply voltage Vcc and Vss terminals ("first and second terminals") and the state of the fuse 10 ("programmable element"). (*See supra* Section IX.B.1(a); *id*. at 1:67-2:33.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶133.)

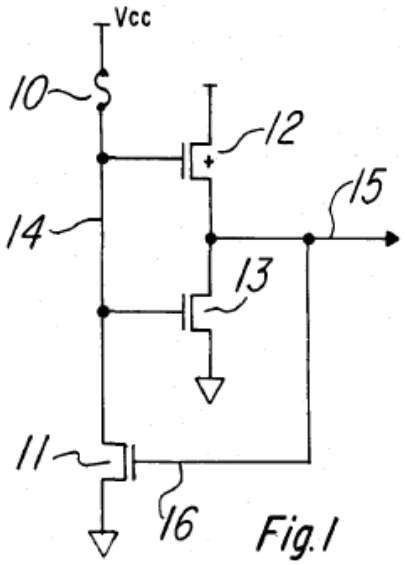
Therefore, McAdams discloses "wherein during operation the voltage on the terminal T1 is completely determined by the state of the programmable element and the voltages on the first and second terminals." (Ex. 1002 at ¶134.)

3. Claim 16

a) The programmable latch of claim 14 wherein the latch does not receive any latch initialization signal from outside the latch.

McAdams discloses this feature. (Ex. 1002 at ¶¶135-136.) As shown in figure 1 of McAdams below, the fuse circuit ("programmable latch") of McAdams

does not receive any inputs from outside of the circuit illustrated and the state of the latch is completely determined by the state of the fuse 10 and the voltages on the Vcc and Vss terminals. (*See supra* Section IX.B.2; Ex. 1006 at FIG. 1; Ex. 1002 at ¶135.)



(Ex. 1006 at FIG. 1.)

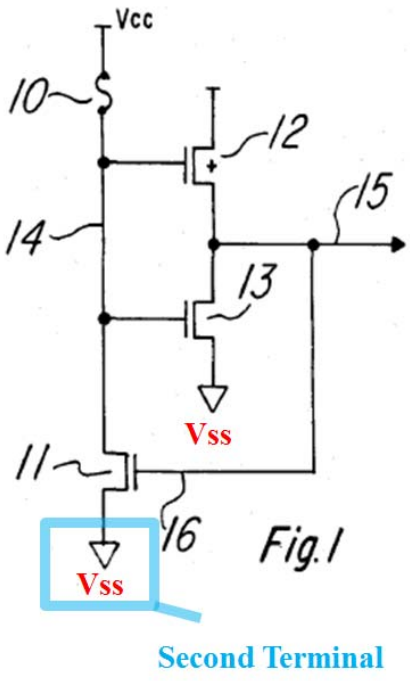
Therefore, McAdams discloses "wherein the latch does not receive any latch initialization signal from outside the latch." (Ex. 1002 at ¶136.)

4. Claim 17

a) The programmable latch of claim 14 wherein the second terminal is to receive a ground voltage throughout operation of the latch.

McAdams discloses this feature. (Ex. 1002 at ¶¶137-138.) As discussed above with respect to claim element 14[c], when power is applied to the fuse circuit ("programmable latch"), the second terminal is connected to Vss throughout

operation of the latch. (*See supra* Section IX.B.1(c).) McAdams confirms that Vss is a ground voltage because it states that when node 15 is pulled low to Vss, the voltage thereon is zero volts. (Ex. 1006 at 2:14-17, "[T]he transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to Vcc transition.") The claims of McAdams further confirm this because they describe the circuit of figure 1 and state that "one of the first and second terminals of said power supply is a positive voltage and said other is *ground*" (emphasis added). (Ex. 1006 at 3:24-26; Ex. 1002 at ¶137; *see also* Ex. 1006 at 4:20-22, "a power supply having a first terminal at a positive voltage and a *second terminal at a ground potential*" (emphasis added), 2:2-3 (explaining that Vss and Vcc are the two terminals of the supply voltage).)



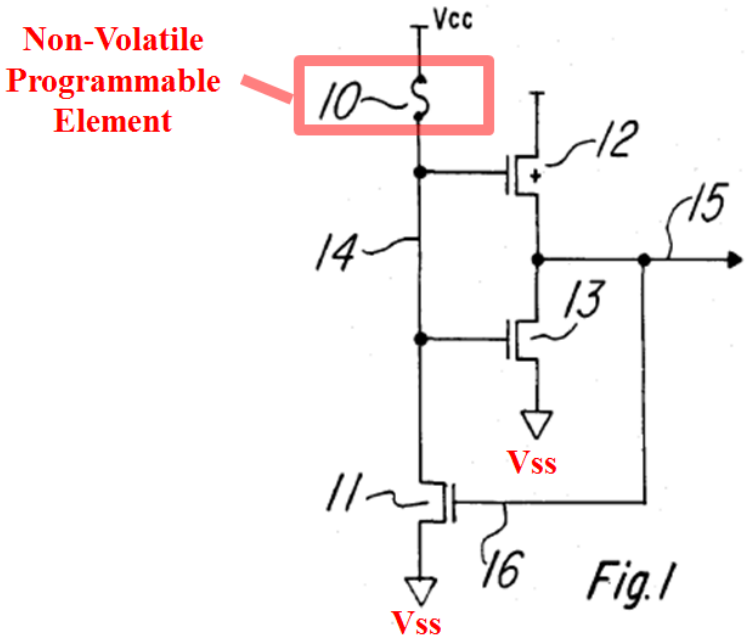
(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶137.)

Therefore, McAdams discloses that "the second terminal is to receive a ground voltage throughout operation of the latch" as recited in claim 17. (Ex. 1002 at ¶138.)

5. Claim 18

a) The programmable latch of claim 14 wherein the programmable element is a fuse.

McAdams discloses this feature. (Ex. 1002 at ¶139.) As demonstrated above with respect to claim feature 14[e], the fuse 10 shown in annotated figure 1 below is a "non-volatile programmable element." (*See supra* Section IX.B.1(e).) Therefore, McAdams discloses "wherein the programmable element is a fuse." (Ex. 1002 at ¶¶139.)

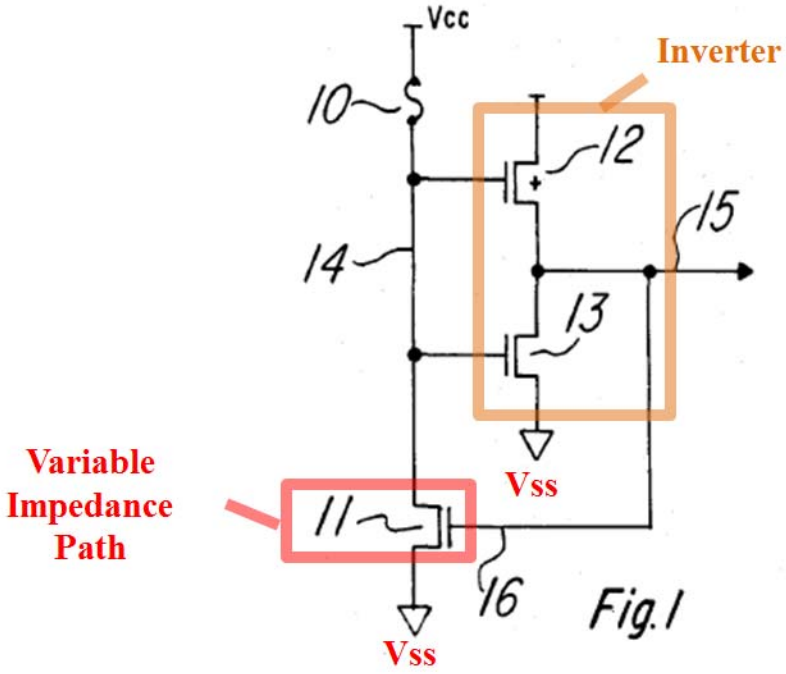


(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶139.)

6. Claim 19

a) The programmable latch of claim 14 wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter.

McAdams discloses this feature. (Ex. 1002 at ¶140.) As demonstrated above with respect to claim features 14[f] and 14[g], the N-channel (NMOS) transistor 11 in annotated figure 1 below corresponds to the claimed "variable impedance electrical path" and the CMOS inverter that includes PMOS transistor 12 and NMOS transistor 13 corresponds to the claimed "inverter." (*See supra* Sections IX.B.1(f)-(g).) Therefore, McAdams discloses "wherein the variable-impedance electrical path is an NMOS transistor, and the inverter is a CMOS inverter." (Ex. 1002 at ¶140.)



(Ex. 1006 at FIG. 1 (annotated); Ex. 1002 at ¶140.)

C. Ground 3: Fu In View of Sugibayashi Renders Claims 14-19 Obvious

1. Claim 14

As demonstrated above in Section IX.A, Fu discloses all of the features of claim 14. For example, as discussed above, the circuit of figure 4 of Fu includes a "first terminal" to which a constant non-ground voltage (Vcc) is applied when the circuit of figure 4 operates. (*Supra* Section IX.A.1(b).)

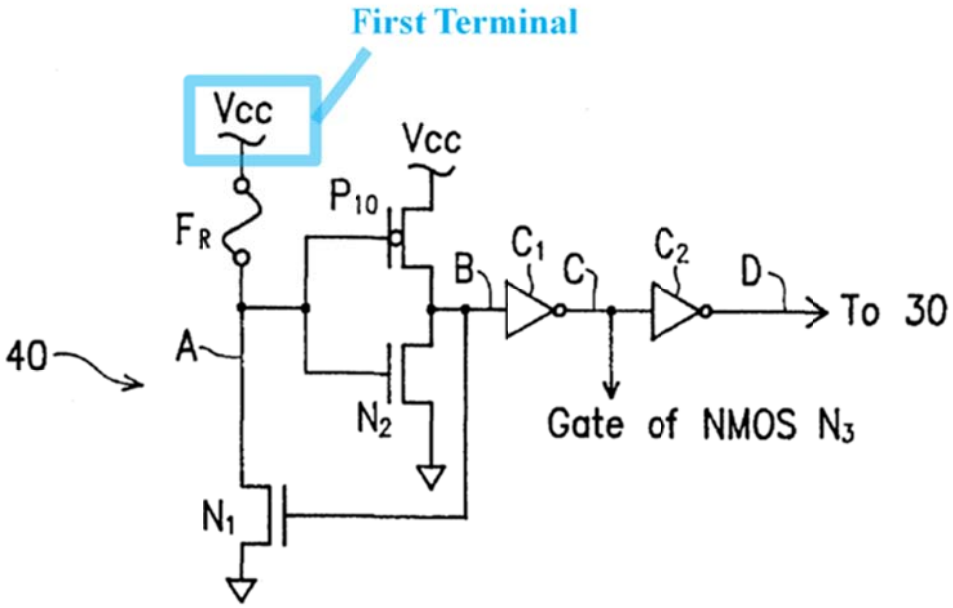


FIG. 4

(Ex. 1005 at FIG. 4 (annotated); Ex. 1002 at ¶142.)

However, to the extent that Patent Owner argues or the Board finds the voltage on the Vcc terminal in Fu is not "a *constant* non-ground voltage throughout operation of the latch," as recited in claim element 14(b) (*supra* Section IX.A.1(b)), it would have been obvious in view of Sugibayashi to provide the supply voltage Vcc in a manner that ensures it is constant throughout the operation of the memory in which the latch is included. (Ex. 1002 at ¶¶141-161.) As discussed below, in view of Sugibayashi, a POSITA would have found it obvious to include an internal voltage supply generating circuit in the semiconductor

memory as disclosed in Fu to ensure that the voltage on the terminal Vcc is constant throughout the operation of the latch. (*Id.*)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007). Under this flexible approach, "it important to identify "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements" in the way claimed. *Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356–57 (Fed. Cir. 2007). Such reason may be found "explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill." *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (internal quotations and citations omitted); *see also KSR*, 550 U.S. at 419-20. Moreover, "'if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.'" *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (quoting *KSR*, 550 U.S. at 417).

Under the law of obviousness, including the above principles, the combination of Fu with Sugibayashi would have been obvious to a POSITA. This is because, *inter alia*, at the time of the alleged invention there existed a known problem in memory devices (such as Fu) that the power supply (e.g., Vcc) provided to circuits in the memory device fluctuated, thereby causing malfunction of the circuit components. (Ex. 1002 at ¶¶145-146.) As explained below, Sugibayashi provided a known solution to this known problem by disclosing an internal voltage supply generator that generated a constant voltage for the circuit components of the memory chip. (Ex. 1002 at ¶¶147-153.)

A POSITA would have known that fluctuations in the power supply voltage used within a memory device can negatively impact the functionality of a memory device. (Ex. 1002 at ¶146; Ex. 1011 at 2:33-38, 2:58-3:24, 7:5-15.) Therefore, a POSITA would have known that it was desirable to provide a stable (i.e., constant) supply voltage to the circuitry on the memory device to ensure proper operation. (Ex. 1002 at ¶147.) A POSITA also knew that, from the perspective of the semiconductor memory device itself (e.g. a memory chip), the external voltage supplied to the memory device is not under control of the memory device. (*Id.*) Therefore, at the time of the alleged invention, it was routine for memory chip designers to include an internal voltage supply generator in the memory chip, where the internal voltage supply generator receives an external voltage supply and

generates an internal supply for the circuits on the memory chip. (*Id.* at ¶¶147-148; Ex. 1011 at 1:16-22; Ex. 1012 at 1:19-23 ("[B]y installing on-chip an internal power-supply voltage supplier, regardless of the external power-supply voltage a constant voltage is applied to the interior of the memory device.").) As explained below, Sugibayashi provides an example of a well-known internal power-supply generator that was capable of providing a constant internal power supply to the circuits of the memory chip. (Ex. 1002 at ¶¶149-153.)

Sugibayashi discloses "a dynamic random access memory device embodying the present invention is fabricated on a single semiconductor chip 11, and largely comprises an internal power supply system 12 for producing a step-down power voltage Vint …." (Ex. 1011 at 4:40-45.) Sugibayashi discloses that the disclosed "internal power supply system [] does not produce any overshoot upon fluctuation of an external power supply" (*id.* at 3:28-31), where the internal power supply "keep[s] the step-down power voltage constant" (*id.* at 3:55; *see also id.* at 3:39-68).

According to Sugibayashi, while internal voltage supply generators for memory devices such as DRAMs were known, such prior art voltage supply generators could result in malfunctions in the internal component circuits of the memories as a result of the loss of voltage margin caused by an overshoot (OS) condition. (*Id.* at 2:58-3:24.) The overshoot condition in Sugibayashi is shown in

figure 4, where the overshoot (OS) corresponds to when the internal voltage supply generated (Vint) exceeds the target voltage level (Vreg). (*Id.*; *id.* at FIG. 4.)

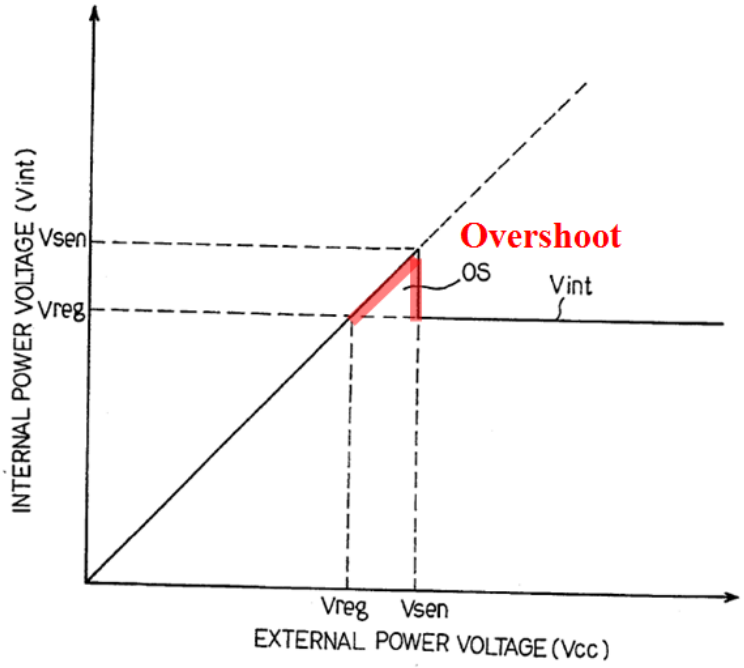
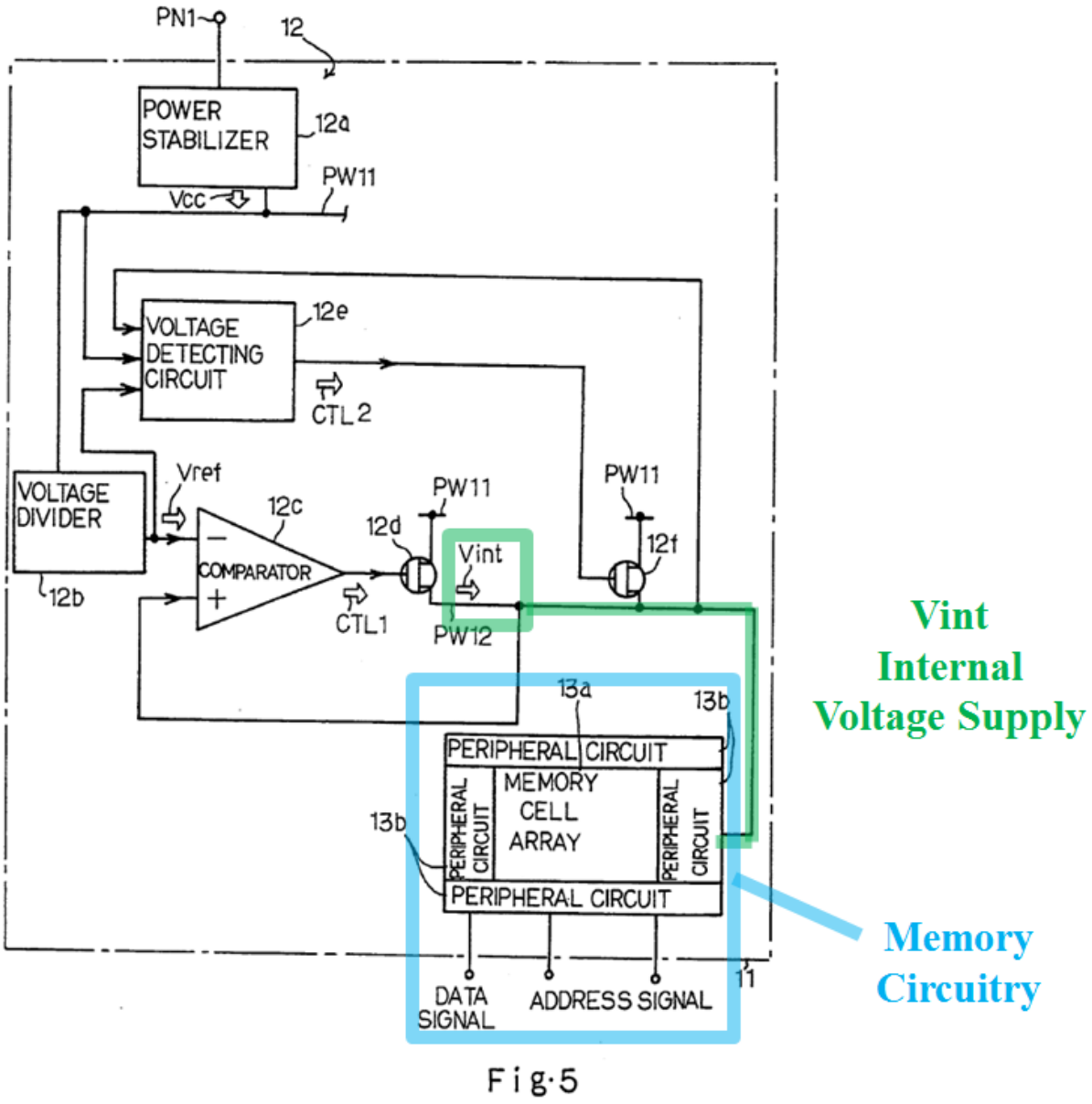


Fig. 4
PRIOR ART

(Ex. 1011 at FIG. 4 (annotated); Ex. 1002 at ¶151.)

In order to avoid the malfunctions that could result from the overshoot on the internal voltage (Vint), Sugibayashi discloses an internal power supply system 12 depicted in annotated figure 5 below. (Ex. 1011 at 4:40-52, FIG. 5; Ex. 1002 at ¶152.)



Fig·5

(Ex. 1011 at FIG. 5 (annotated); Ex. 1002 at ¶152.)

As shown in annotated figure 5 above, a comparator 12c compares the internal voltage Vint with a reference voltage Vref, and, based on whether the internal voltage Vint is greater or less than Vref, comparator 12c controls the transistor 12d to keep Vint at the desired reference voltage level Vref. (Ex. 1011 at

5:7-31, FIG. 5.) The internal power supply system 12 shown above also includes voltage detecting circuit 12e, which, in combination with variable load transistor 12f, ensures that variations in the external power voltage Vcc do not result in similar variations on the internal voltage supply Vint. (*Id.* at 6:48-68 (describing that when there is "turbulence in an external supply system" the "step-down power voltage Vint is *kept constant* as shown in FIG. 8") (emphasis added); Ex. 1002 at ¶153.)

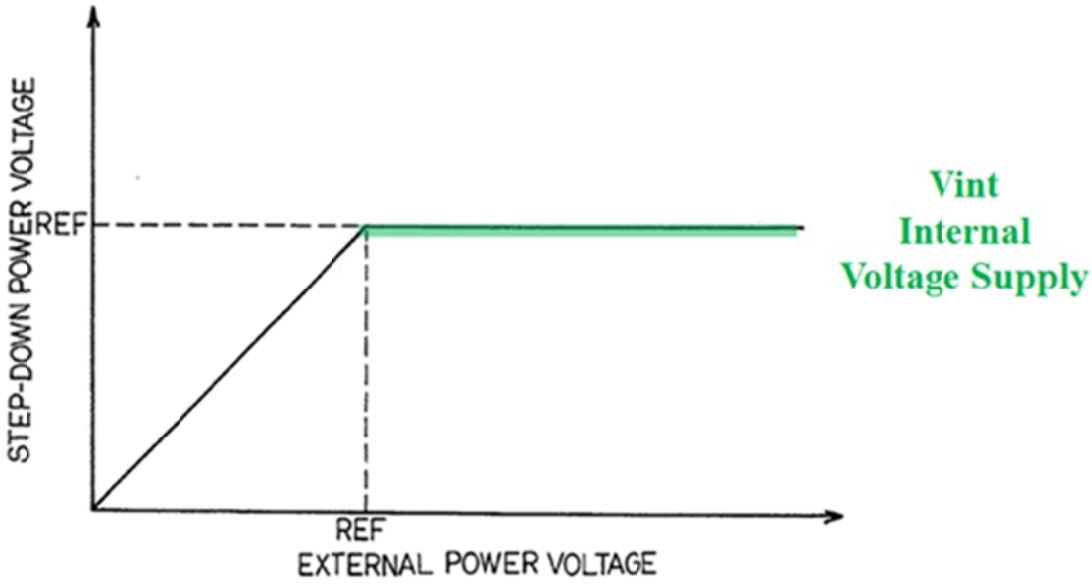


Fig.8

(Ex. 1011 at FIG. 8 (annotated); Ex. 1002 at ¶153.)

Based on the teachings of Sugibayashi, a POSITA would have been motivated to modify the circuit of figure 4 in Fu such that the Vcc supply voltage in Fu is provided by an internal voltage supply generator similar to the one

disclosed in Sugibayashi *in order to ensure a constant internal supply voltage and avoid malfunctions in internal component circuits of the memory*. (Ex. 1002 at ¶154.) A POSITA would have looked to Sugibayashi because, *inter alia*, like Fu, Sugibayashi is related to integrated circuit memory devices. (Ex. 1005 at 3:27-35; Ex. 1011 at 1:9-13 ("This invention relates to an integrated circuit device, and more particularly to … a dynamic random access memory device equipped with an internal step-down circuit."), 4:40-48; Ex. 1002 at ¶154.)

Having looked to Sugibayashi, a POSITA would have found it obvious to combine the teachings of Sugibayashi with Fu to implement an internal voltage supply generator (like in Sugibayashi) to generate the voltage supply Vcc that is provided to the internal component circuits of Fu's memory, including the latch circuit shown in figure 4 of Fu. (Ex. 1002 at ¶155.) First, such a modification of Fu would have been within the capabilities of one of ordinary skill because Sugibayashi discloses how such an internal supply voltage generator is included in a semiconductor memory device and explains how the internal supply voltage generator operates to ensure a *constant* internal voltage in spite of variations in the external voltage supply. (*Id*. at ¶156.) Second, as explained above, a POSITA would have recognized a benefit to making such a modification because it would have resulted in a memory device that is less likely to suffer malfunctions due to variations in the external power supply voltage. (*Id*. at ¶157.) *See Unwired*

Planet, 841 F.3d at 1004 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"); *KSR*, 550 U.S. at 424 ("the proper question to have asked was whether a pedal designer of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to upgrading Asano with a sensor").

Indeed, combining the teachings of Sugibayashi with Fu would have been obvious because a POSITA would have recognized that applying Sugibayashi's technique (e.g., generating a constant internal voltage from an external power supply voltage) to Fu's memory device would have improved Fu's device in the same way Sugibayashi's technique improves Sugibayashi's memory device (e.g., prevents malfunctioning of the circuits within the memory device), and such application was within the level of ordinary skill. (Ex. 1002 at ¶158.) *See Katz Interactive Call Processing Patent Litig. v. Am. Airlines, Inc.*, 639 F.3d 1303, 1323 (quoting *KSR*, 550 U.S. at 417 and affirming a finding of obviousness because "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill"); *see also In re Schwemberger*, 410 Fed. Appx. 298, 304 (Fed. Cir. 2010).

Moreover, including the internal supply voltage generator as disclosed by Sugibayashi with the circuit of figure 4 of Fu would not have negatively impacted the disclosed circuit in Fu and would have solved a known problem of circuit malfunction in memory devices like Fu. (Ex. 1002 at ¶159.) *See ZUP*, 896 F.3d at 1371-72 (solving a problem or need that was well-known in the prior art provides a motivation to combine); *KSR* at 419-20 (a patent claim "can be proved obvious [] by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the . . . [claim]"). Therefore, the combined Fu-Sugibayashi circuit discloses or suggests "a constant non-ground voltage throughout operation of the latch" because in the combination, Vcc ("non-ground voltage") is produced by an internal voltage generator that produces a constant voltage. (Ex. 1002 at ¶160.)

Fu in combination with Sugibayashi discloses or suggests the remaining limitations of claim 14 for the reasons discussed above for claim 14 in Ground 1, with the only modification to the analysis for claim 14 being that discussed above. (*Supra* Sections IX.A.1(a)-(g); Ex. 1002 at ¶161.)

2. Claims 15-19

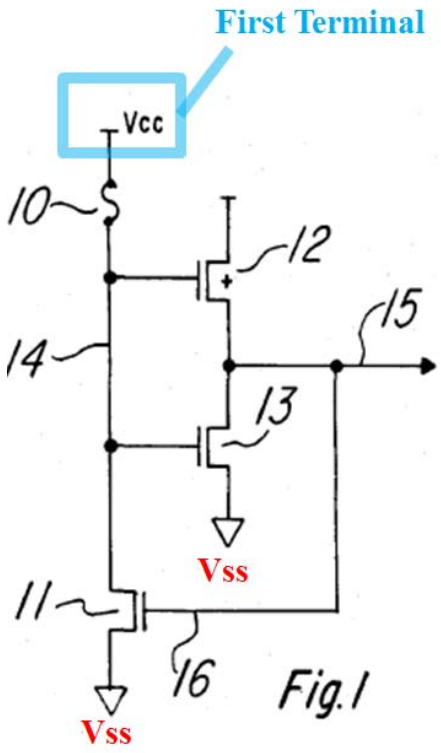
Fu in combination with Sugibayashi discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.A.2-6; Ex. 1002 at ¶162.) The same analysis presented above for these claims in Ground 1 is also

applicable for the Fu-Sugibayashi combination discussed above in Section IX.C.1. (Ex. 1002 at ¶162.) The combination of Sugibayashi with Fu does not affect the analysis for these claims in Section IX.A.

D. Ground 4: McAdams In View of Sugibayashi Renders Claims 14-19 Obvious

1. Claim 14

As demonstrated above in Section IX.A.1, McAdams discloses all of the features of claim 14. For example, as discussed above in Section IX.B.1(b), McAdams includes a "first terminal" Vcc, where Vcc is a "supply voltage" that is applied when power is applied to the circuit of figure 1. (Ex. 1006 at 2:2-3, 2:8-9, 3:24-26, 4:20-22.) As further discussed above in Section IX.B.1(b), Vcc is at +5 v after power up of the latch and therefore constitutes "a constant non-ground voltage throughout operation of the latch." (*Supra* Section IX.B.1(b); Ex. 1002 at ¶164.) Therefore, the terminal highlighted in blue below constitutes a "first terminal for receiving a constant non-ground voltage throughout operation of the latch." (Ex. 1002 at ¶164.)



(Ex. 1001 at FIG. 1 (annotated); Ex. 1002 at ¶164.)

However, to the extent that Patent Owner argues or the Board finds the voltage on the Vcc terminal in McAdams is not "a *constant* non-ground voltage throughout operation of the latch," as recited in claim element 14(b) (*supra* Section IX.B.1(b)), it would have been obvious in view of Sugibayashi to provide the supply voltage Vcc in a manner that ensures it is constant throughout the operation of the memory in which the latch is included. (Ex. 1002 at ¶¶163-174.) As discussed below, in view of Sugibayashi, a POSITA would have found it obvious to include an internal voltage supply generating circuit in the semiconductor

memory as disclosed in McAdams to ensure that the voltage on the terminal Vcc is constant throughout the operation of the latch. (*Id.*)

As explained above in Section IX.C.1, at the time of the alleged invention there existed a known problem in memory devices (such as McAdams) that the power supply (e.g., Vcc) provided to circuits in the memory device fluctuated, thereby causing malfunction of the circuit components. (*Supra* Section IX.C.1; Ex. 1002 at ¶167.) As also explained above in Section IX.C.1, Sugibayashi provided a known solution to this known problem by disclosing an internal voltage supply generator that generated a constant voltage for the circuit components of the memory chip. (*Id.*)

Based on the teachings of Sugibayashi, a POSITA would have been motivated to modify the circuit of figure 1 in McAdams such that the Vcc supply voltage in McAdams is provided by an internal voltage supply generator similar to the one disclosed in Sugibayashi *in order to ensure a constant internal supply voltage and avoid malfunctions in internal component circuits of the memory*. (Ex. 1002 at ¶168.) A POSITA would have looked to Sugibayashi because, *inter alia*, like McAdams, Sugibayashi is related to integrated circuit memory devices. (Ex. 1006 at 1:5-12; Ex. 1011 at 1:9-13 ("[t]his invention relates to an integrated circuit device, and more particularly to … a dynamic random access memory device equipped with an internal step-down circuit."), 4:40-48; Ex. 1002 at ¶168.)

Having looked to Sugibayashi, a POSITA would have found it obvious to combine the teachings of Sugibayashi with McAdams to implement an internal voltage supply generator (like in Sugibayashi) to generate the voltage supply Vcc that is provided to the internal component circuits of McAdams's memory, including the latch circuit shown in figure 1 of McAdams. (Ex. 1002 at ¶169.) First, such a modification of McAdams would have been within the capabilities of one of ordinary skill because Sugibayashi discloses how such an internal supply voltage generator is included in a semiconductor memory device and explains how the internal supply voltage generator operates to ensure a *constant* internal voltage in spite of variations in the external voltage supply. (*Id*. at ¶170.) Second, as explained above, a POSITA would have recognized a benefit to making such a modification because it would have resulted in a memory device that is less likely to suffer malfunctions due to variations in the external power supply voltage. (*Id*. at ¶171.) *See Unwired Planet*, 841 F.3d at 1003 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"); *KSR*, 550 U.S. at 424 ("the proper question to have asked was whether a pedal designer of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to upgrading Asano with a sensor.")

Indeed, combining the teachings of Sugibayashi with McAdams would have been obvious because a POSITA would have recognized that applying Sugibayashi's technique (e.g., generating a constant internal voltage from an external power supply voltage) to McAdams's memory device would have improved McAdams's device in the same way Sugibayashi's technique improves Sugibayashi's memory device (e.g., prevents malfunctioning of the circuits within the memory device), and such application was within the level of ordinary skill. (Ex. 1002 at ¶172.) *See Katz Interactive Call Processing Patent Litig.*, 639 F.3d at 1323 (quoting *KSR*, 550 U.S. at 417 and affirming a finding of obviousness because "if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill"); *see also In re Schwemberger*, 410 Fed. Appx. at 304.

Moreover, including the internal supply voltage generator as disclosed by Sugibayashi with the circuit of figure 1 of McAdams would not have negatively impacted the disclosed circuit in McAdams and would have solved a known problem of circuit malfunction in memory devices like McAdams. (Ex. 1002 at ¶173.) *See ZUP*, 896 F.3d at 1371-72 (solving a problem or need well-known in the prior art provides a motivation to combine); *KSR* at 419-20 (a patent claim "can be proved obvious [] by noting that there existed at the time of invention a known

problem for which there was an obvious solution encompassed by the . . . [claim]"). Therefore, the combined McAdams-Sugibayashi circuit discloses or suggests "a constant non-ground voltage throughout operation of the latch" because in the combination, Vcc ("non-ground voltage") is produced by an internal voltage generator that produces a constant voltage. (Ex. 1002 at ¶173.)

McAdams in combination with Sugibayashi discloses or suggests the remaining limitations of claim 14 for the reasons discussed above for claim 14 in Ground 2 with the only modification to the analysis for claim 14 being that discussed above. (*Supra* Sections IX.B.1(a)-(g); Ex. 1002 at ¶174.)

2. Claims 15-19

McAdams in combination with Sugibayashi discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.B.2-6; Ex. 1002 at ¶175.) The same analysis presented above for these claims in Ground 2 is also applicable for the McAdams-Sugibayashi combination discussed above in Section IX.D.1. (Ex. 1002 at ¶175.) The combination of Sugibayashi with McAdams does not affect the analysis for these claims in Section IX.B.

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 14-19 of the '492 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 5, 2019 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 contains, as measured by the word-processing system used to prepare this paper, 12,501 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 5, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

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