Paper No. __
Filed: March 5, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,163,492

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,163,492

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Ex. 1015	Taur *et al.*, Fundamentals of Modern VLSI Devices, 2009 ("Taur")
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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-13 of U.S. Patent No. 6,163,492 ("the '492 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '492 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al*., No. 1:18-cv-00307-RGA (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 5,934,974 ("the '974 patent"), 6,099,386 ("the '386 patent"), 6,469,559 ("the '559 patent"), and 6,597,201 ("the '201 patent") in this action. Petitioner is concurrently filing two other IPR petitions challenging one or more claims of the '492 patent, as well as additional IPR petitions challenging certain claims of the '974, '386, '559, and '201 patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul

M. Anderson (Reg. No. 39,896), and (3) Chetan R. Bansal (Limited Recognition No. L0667). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the '492 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-13 ("challenged claims") of the '492 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following grounds:

Ground 1: Claims 1-5, 8-10, and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 4,621,346 ("McAdams") (Ex. 1006) in view of U.S. Patent No. 5,519,658 ("Uda") (Ex. 1007).

Ground 2: Claims 5-7 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over McAdams in view of Uda and U.S. Patent No. 5,552,739 ("Keeth") (Ex. 1008).

Ground 3: Claims 11 and 12 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over McAdams in view of Uda and Neil Weste *et al.*, *Principles of CMOS VLSI Design: A Systems Perspective*, 2d. ed. 1993 ("Weste") (Ex. 1009).

Ground 4: Claim 9 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over McAdams in view of Uda and U.S. Patent No. 5,604,710 ("Tomishima") (Ex. 1013).

The '492 patent issued from U.S. Application No. 09/178,445 ("the '445 application") filed October 23, 1998. (Ex. 1001, Cover). The '445 application does not claim priority to any earlier-filed applications.

McAdams issued on November 04, 1986. Uda issued on September 03, 1996. Keeth issued on May 21, 1996. Tomishima issued on February 18, 1997.

Weste published at least by 1994. Dr. Hsieh-Yee, an expert on library cataloging and classification, considered numerous facts relating to Weste (e.g.,

bibliographic and MARC records, a date stamp, copyright registration information, and pre-filing date citations to Weste) and explains on the basis of such evidence that Weste was accessible to the public by September 16, 1993. (Ex. 1016, ¶27; *see also id.*, ¶¶12-26.)[1] Additionally, Dr. Hsieh-Yee explains that several pre-critical-date publications cite to Weste, including one as early as December 1994. (*Id.*, ¶26.)

Thus, McAdams, Uda, Keeth, Weste, and Tomishima qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b) with respect to the '492 patent. None of McAdams, Uda, Keeth, Weste, and Tomishima was considered by the Patent Office during prosecution of the '492 patent. (*See generally* Ex. 1001, References Cited.)

[1] Dr. Hsieh-Yee cites to Exhibit 1014 in her analysis regarding the public availability of the Weste textbook (Exhibit 1009). (*See, e.g.*, Ex. 1016, ¶¶12-13.) Exhibit 1014 is a copy of Weste's relevant portions (e.g., cover, title page, copyright page, back cover, etc.) that Dr. Hsieh-Yee personally made and which match the corresponding portions of Exhibit 1009 being cited in this petition. (*Compare, e.g.*, Ex. 1009, 1-22, 745-46 *with* Ex. 1014 at 1-22, 23-24.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA at the time of the alleged invention of the '492 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including October 23, 1998, the filing date of the U.S. Application maturing into the '492 patent), would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶20.)[2] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '492 PATENT AND PRIOR ART

A. The '492 Patent

The '492 patent is entitled "Programmable Latches that Include Non-volatile Programmable Elements." (Ex. 1001, Cover.) Consistent with the title, the '492 patent relates to "programmable latches that include non-volatile programmable elements" where "[e]xamples of non-volatile programmable elements are fuses." (*Id.,* 1:15-17; Ex. 1002, ¶¶40-48; *see also* Ex.1002 at ¶¶22-39 (citing Ex. 1015).)

The '492 patent acknowledges that the "[p]rior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal

[2] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '492 patent. (Ex. 1002, ¶¶5-15; Ex. 1003.)

from outside the latch" and that "[t]he state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals." (Ex. 1001, 2:22-26; *see also id.,* 1:24-54, FIG. 1; Ex. 1002, ¶41.)

While the prior art programmable latch shown in figure 1 includes features to avoid an incorrect output on power up and does not require any initialization signal, the '492 patent proposes an alternative programmable latch as shown in figure 2A below. (Ex. 1001, 3:10-11.)

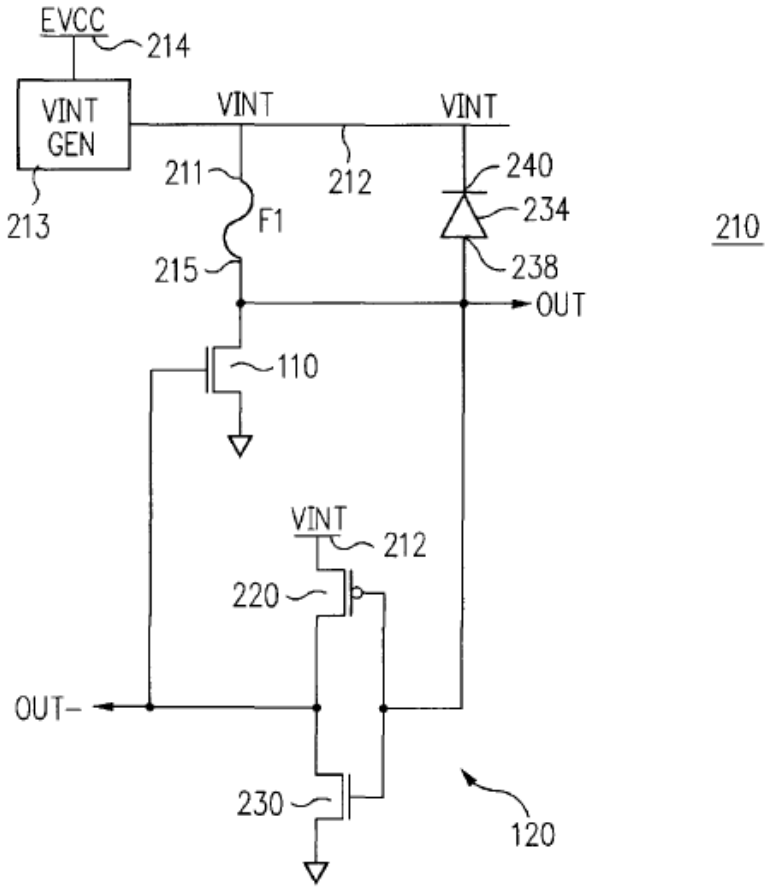


FIG. 2A

(*Id.*, FIG. 2A.)

The programmable latch shown in figure 2A above includes a fuse 211, an inverter 120 that includes transistors 220 and 230, and a transistor 110. (*Id.*, 3:10-33, FIG. 2A.) The programmable latch of figure 2A also includes a diode 234 that holds the OUT node at a voltage not higher than a threshold voltage of the diode 234 when the VINT terminal is ground. (*Id.*, 3:38-41.) According to the '492 patent, by maintaining the voltage on OUT low using the diode 234, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on and

"connects the terminal OUT to ground," resulting in a correct output. (*Id.*, 3:41-49.) This happens because terminal OUT is held "not higher than one threshold voltage of diode 234," and at such a voltage, transistor 230 does not turn on because its threshold voltage (e.g., 1.2V) is greater than the threshold voltage of diode 234. (*Id.*) Per the '492 patent, the latch can operate correctly even if the diode is omitted. (*Id.*, 5:51-6:7; Ex. 1002, ¶¶46-48.)

The above features were well known as discussed below in Section IX. (Ex. 1002, ¶¶66-195.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.,* 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior

art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[3] (Ex. 1002, ¶50.)

IX. DETAILED EXPLANATION OF GROUNDS

As detailed below, the challenged claims are unpatentable based on Grounds 1-4. (Ex. 1002, ¶¶66-195.)

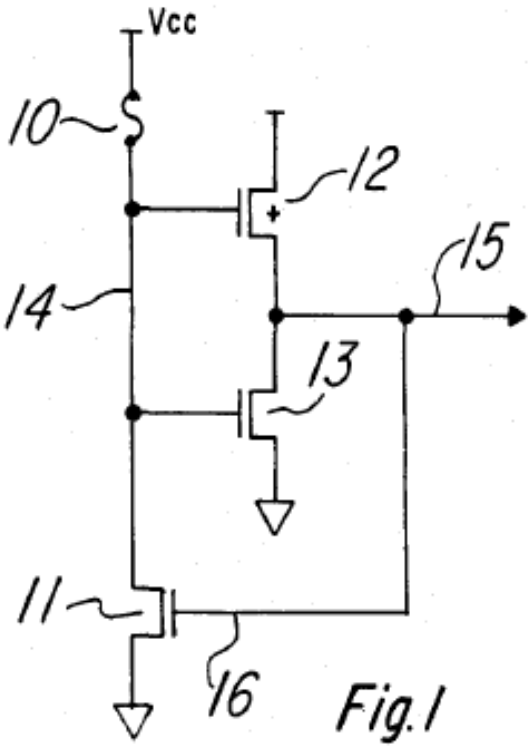
A. Ground 1: McAdams and Uda Render Obvious Claims 1-5, 8-10, and 13

1. Claim 1

a) A programmable latch comprising:

To the extent the preamble is limiting, McAdams discloses this feature. (Ex. 1002, ¶¶67-73.) For example, McAdams discloses a fuse circuit depicted in figure 1.

[3] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '492 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

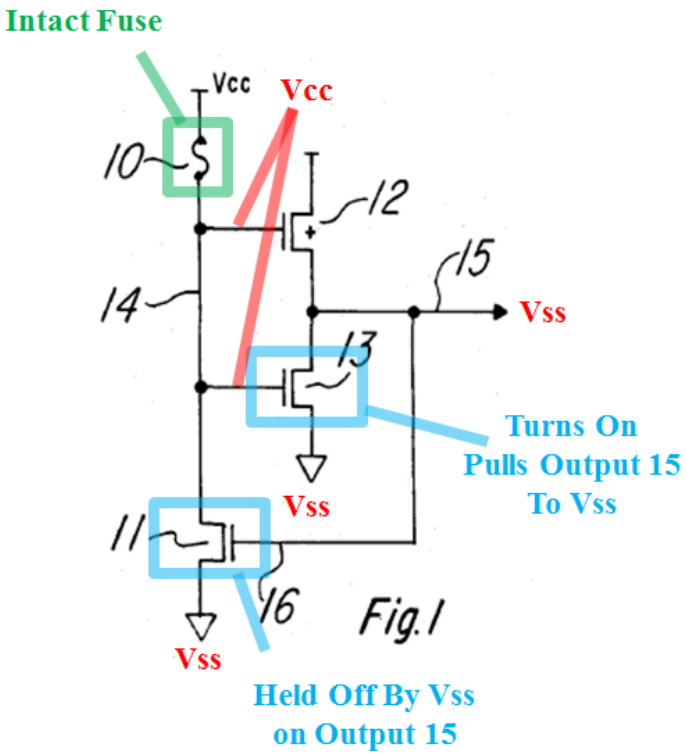


(Ex. 1006, FIG. 1.)

The fuse circuit of figure 1 includes a fuse 10, a feedback transistor 11, and an inverter that includes P-channel transistor 12 and N-channel transistor 13. (*Id.,* 1:67-2:7; Ex. 1002, ¶68.) The fuse circuit of figure 1 produces an output 15, which is fed back to the gate of the transistor 11. (Ex. 1006, 2:3-7.)

In the operational scenario depicted in annotated figure 1 below, if the fuse 10 is intact and has not been blown when power is applied to the circuit, the node 14 follows the power supply Vcc, which turns on transistor 13. (*Id.,* 2:8-15; Ex. 1002, ¶69.) When transistor 13 turns on, any charge on the output node 15 is discharged, pulling the output 15 to Vss. (Ex. 1002, ¶70.) The Vss voltage on the

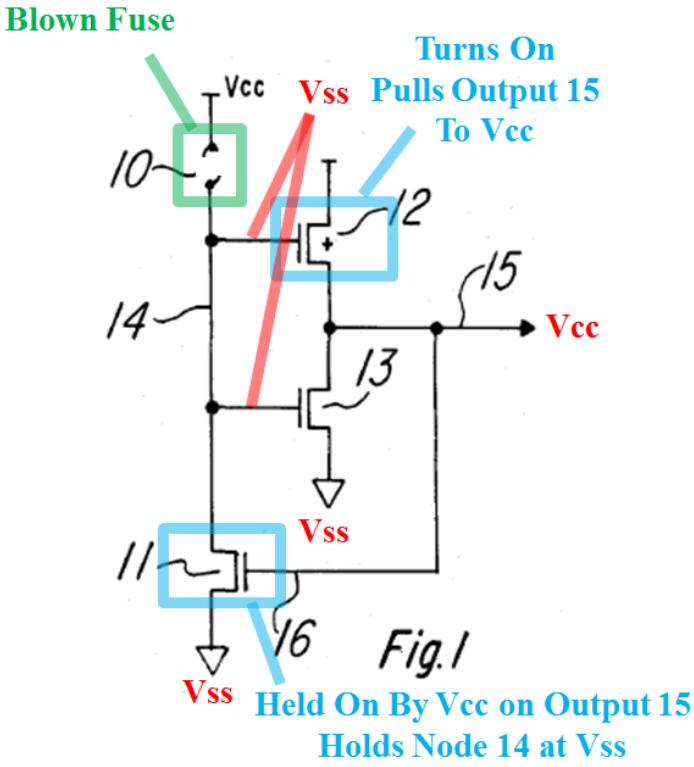
output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state. (Ex. 1006, 2:8-18; Ex. 1002, ¶70.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶70.)

In the alternate operational scenario where the fuse has been blown, which is depicted in the demonstrative below, the node 14 is at Vss when power is applied. (Ex. 1006, 2:21-22; Ex. 1002, ¶71.) Because the gate of P-channel transistor 12 is at Vss, transistor 12 turns on and the output node 15 is pulled to Vcc. (Ex. 1006, 2:22-24.) The Vcc voltage on the output is fed back to the gate of transistor 11, which turns transistor 11 on and holds the node 14 at Vss. (*Id.*, 2:24-26.) Holding

node 14 at Vss ensures that the P-channel transistor 12 remains on and the output 15 is held is Vcc. (*Id.*, 2:21-26.)

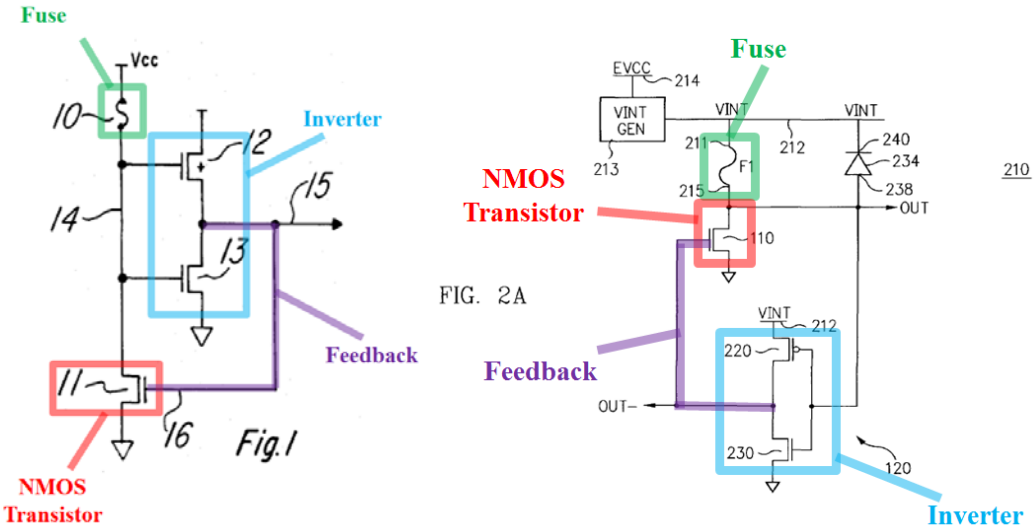


(Ex. 1002, ¶71.)

Therefore, based on whether the fuse 10 has been blown or is intact, the output 15 of the fuse circuit shown in figure 1 will be held at either Vcc or Vss. (*Id.*, ¶72.) The feedback of the output of the inverter to the transistor 11 holds that output at Vcc or Vss. (*Id.*) Therefore, the output is latched at either Vcc or Vss based on whether or not the fuse is blown. (*Id.*) A POSITA would have recognized that the fuse circuit constitutes a "programmable latch" where the

programming corresponds to the state of the fuse, which determines the latched value at the output. (*Id.*)

Indeed, the fuse circuit of McAdams corresponds to a "programmable latch" in the same manner as that disclosed in the figure 2A of the '492 patent. As shown below, the programmable latch shown in figure 2A of the '492 patent includes a fuse 211, inverter 120 that includes transistors 220 and 230, and transistor 110 that are intercoupled in the same manner as the fuse circuit in figure 1 of McAdams. (Ex. 1001, FIG. 2A; *see* analysis regarding remaining claim elements below; Ex. 1002, ¶73.)

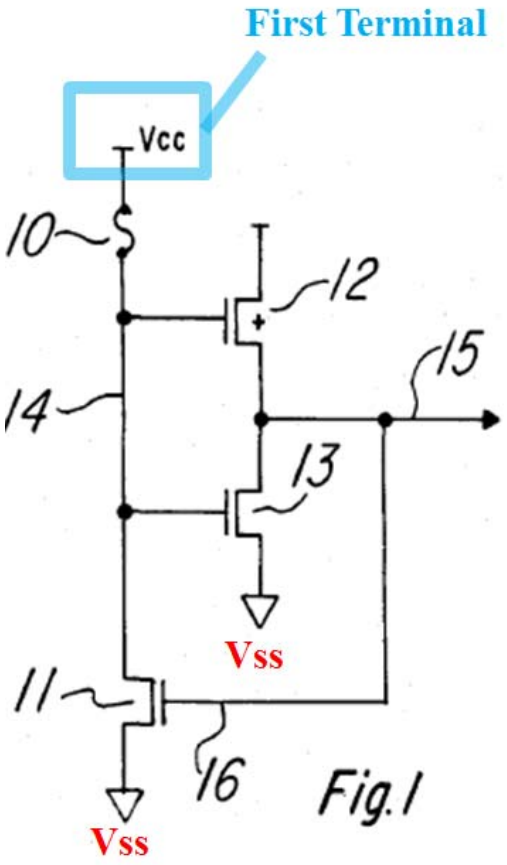


(Ex. 1006, FIG. 1 (annotated); Ex. 1001, FIG. 2A (annotated); Ex. 1002, ¶73.)

b) a first terminal for receiving a first voltage;

McAdams discloses this feature. (Ex. 1002, ¶¶74-75.) As shown in annotated figure 1 below, the "programmable latch" of McAdams includes a

"terminal" Vcc, where Vcc is a "supply voltage" that is applied when power is applied to the circuit of figure 1. (Ex. 1006, 2:2-3, "series circuit is connected between a supply voltage Vcc and Vss"; *id.,* 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v"; *id.,* 3:24-26, "wherein said one of the first and second terminals of said power supply is a positive voltage and said other is ground"; *id.,* 4:20-22, "a power supply having a first terminal at a positive voltage and a second terminal at a ground potential".) In the example embodiment of McAdams, Vcc is at +5 v after power up of the latch and therefore constitutes "a first voltage." (*Id*.; Ex. 1002, ¶74.) Therefore, the terminal highlighted in blue below constitutes a "first terminal for receiving a first voltage." (*Id*.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶74.)

As shown in annotated figure 2A of the '492 patent below, the "first terminal" highlighted in figure 1 of McAdams above is consistent with the "first terminal" disclosed by the '492 patent. (Ex. 1002, ¶75.)

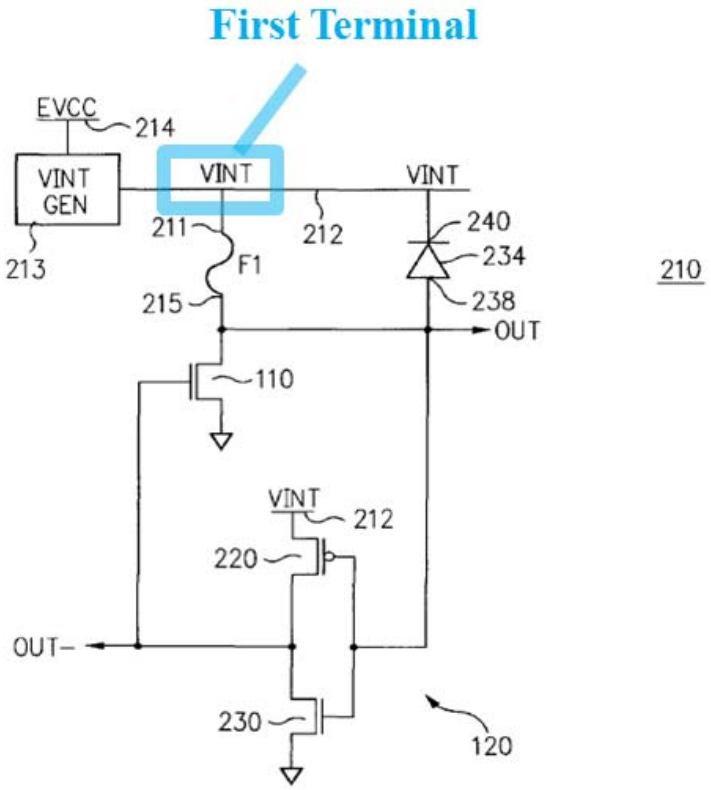


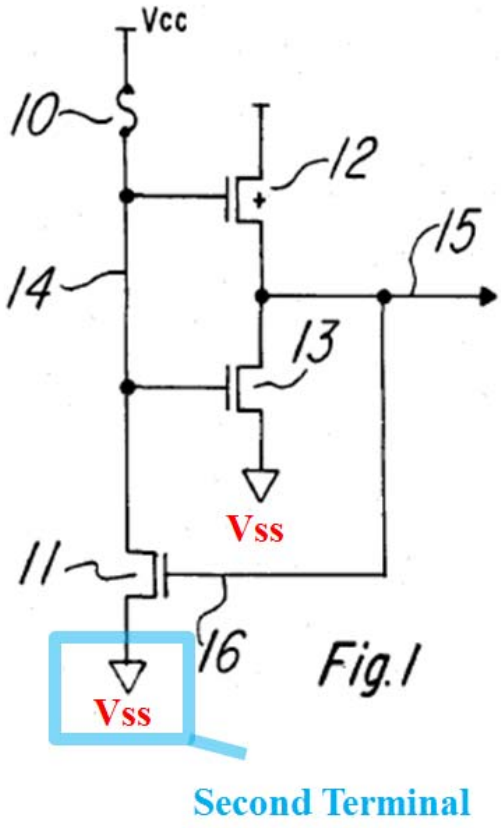
FIG. 2A

(Ex. 1001, FIG. 2A (annotated); Ex. 1002, ¶75.)

c) a second terminal for receiving a second voltage;

McAdams discloses this feature. (Ex. 1002, ¶¶76-77.) For example, the programmable latch circuit in figure 1 of McAdams includes a terminal ("second terminal") for receiving Vss ("a second voltage"). (Ex. 1006, 2:2-3, "series circuit is connected between a supply voltage Vcc and Vss"; *id.*, 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v"; *id.*, 2:14-17, "[T]he transistor 13 turns on, holding the output node 15 at Vss. This quickly discharges to zero any capacitive coupling of voltage to the output node 15 at power-on due to

Vcc transition.) Therefore, McAdams discloses "a second terminal for receiving a second voltage." (Ex. 1002, ¶76.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶76.)

As shown in annotated figure 2A of the '492 patent below, the "second terminal" highlighted in figure 1 of McAdams above is consistent with the "second terminal" disclosed by the '492 patent. (Ex. 1002, ¶77.)

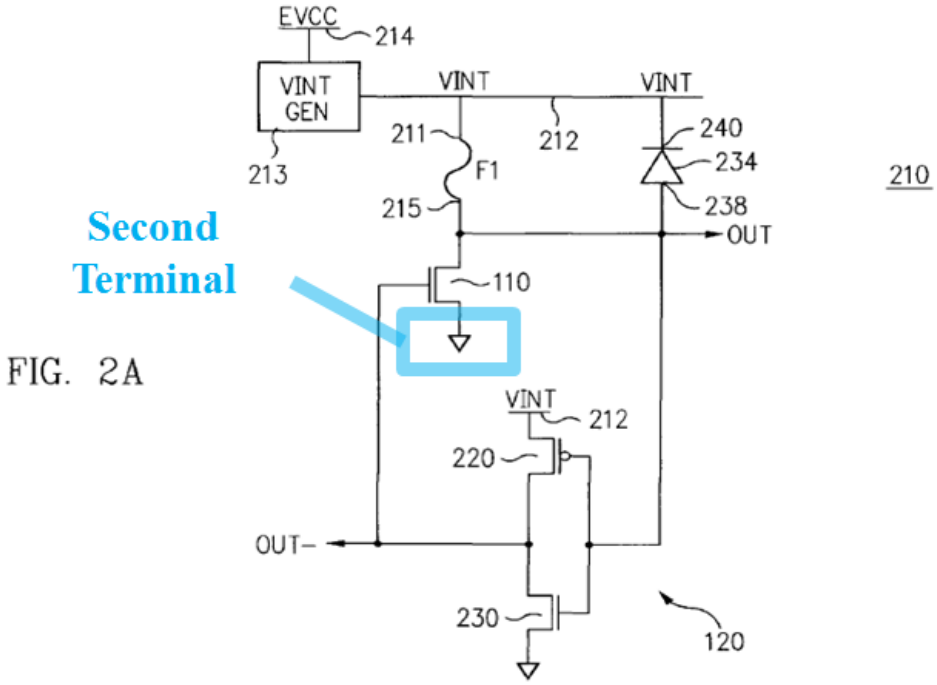
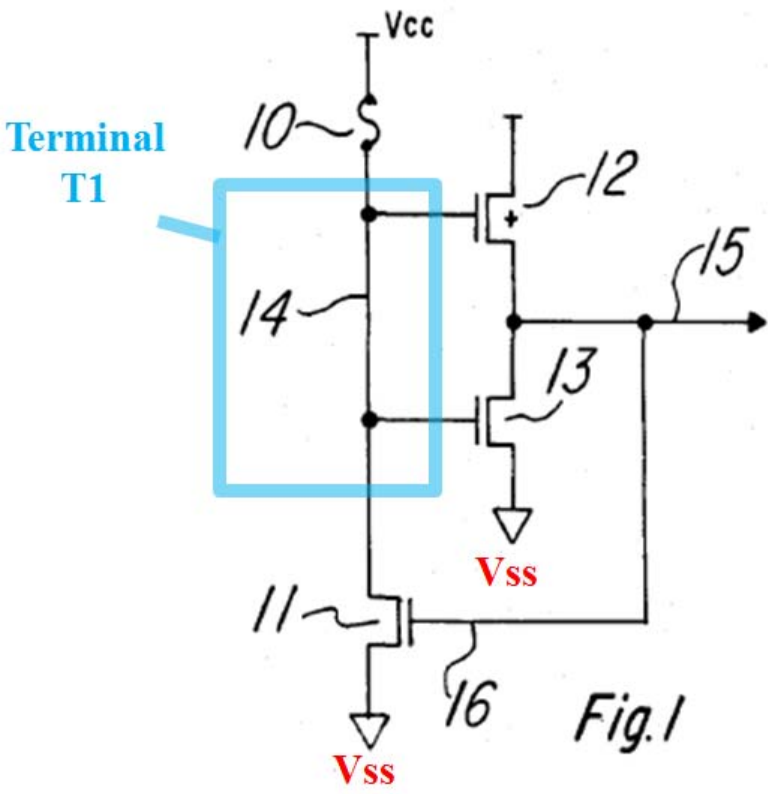


FIG. 2A

(Ex. 1001, FIG. 2A (annotated); Ex. 1002, ¶77.)

d) a terminal T1 for providing a signal indicating a state of the programmable latch;

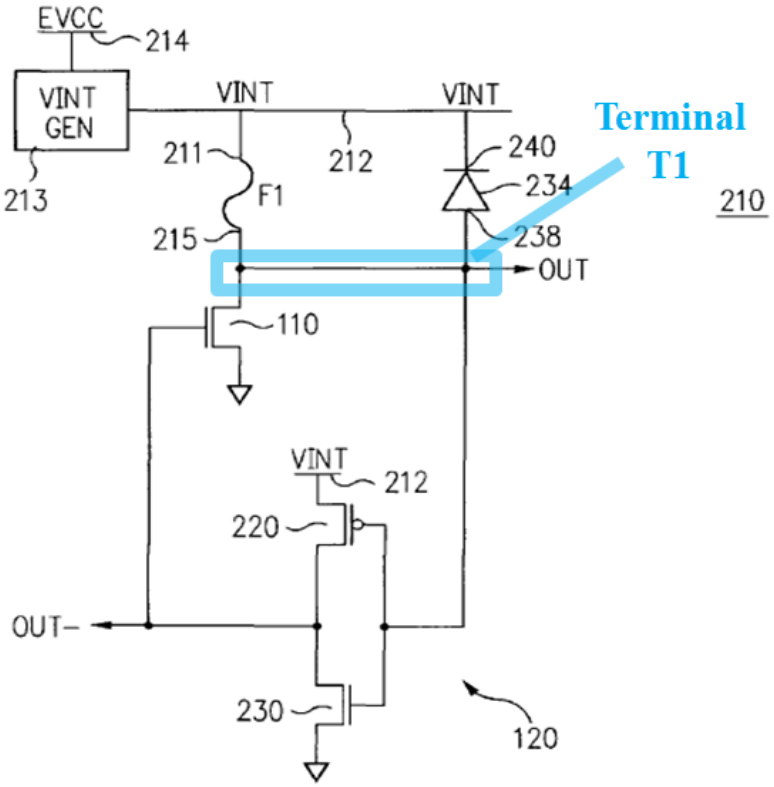
McAdams discloses this feature. (Ex. 1002, ¶¶78-79.) For example, as shown in annotated figure 1 below, the node 14 indicates the state of the fuse, which corresponds to the state of the programmable latch ("a terminal T1 for providing a signal indicating a state of the programmable latch"). (*Id.*, ¶78.) As discussed above with respect to claim element 1[a], when power is applied to the latch, if the fuse is intact, node 14 is at Vcc (high), but if the fuse is blown, node 14 is at Vss (low). (*See* Section IX.A.1(a) *supra*.) Therefore, the voltage at node 14 indicates a "state of the programmable latch" because it indicates whether the fuse is blown or not. (Ex. 1002, ¶78.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶78.)

As shown in annotated figure 2A of the ’492 patent below, the “terminal T1” highlighted in figure 1 of McAdams above is consistent with the “terminal T1” disclosed by the ’492 patent. (Ex. 1002, ¶79.)

FIG. 2A

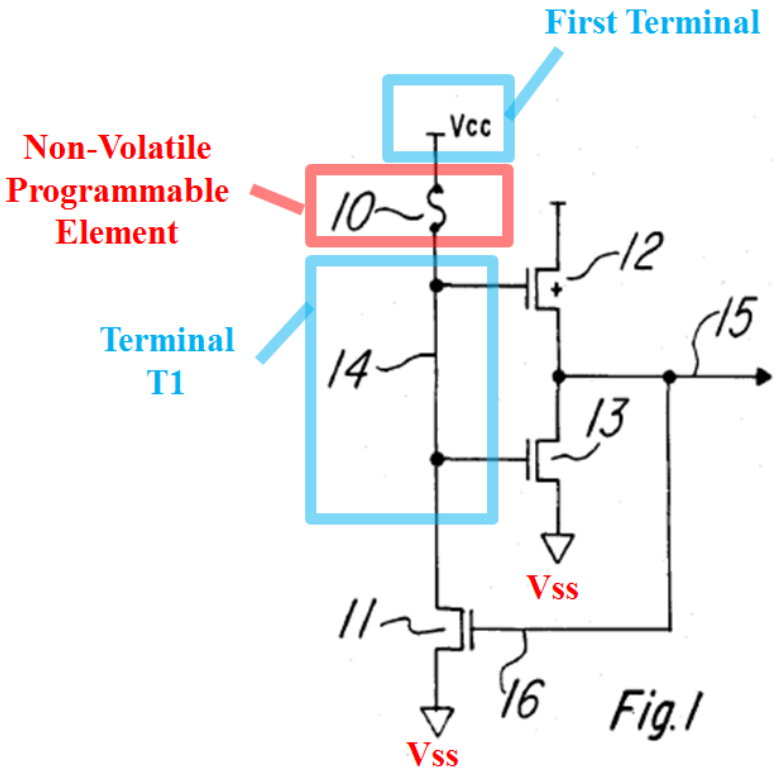


(Ex. 1001, FIG. 2A (annotated); Ex. 1002, ¶79.)

e) a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;

McAdams discloses this feature. (Ex. 1002, ¶¶80-83.) For example, the fuse 10 shown in annotated figure 1 below is a "non-volatile programmable element." (*Id.*, ¶80.) Such an understanding is consistent with the disclosure of the '492 patent, which shows a fuse as the "non-volatile programmable element" in the embodiment of figure 2A. (Ex. 1001, FIG. 2A, 3:10-23, 7:24-36; Ex. 1002,

¶80.) Moreover, claim 10, which depends from claim 1, recites "wherein the programmable element is a fuse," thereby demonstrating that a fuse is a "non-volatile programmable element" in the context of claim 1 and the '492 patent. (Ex. 1001, 9:25-27; Ex. 1002, ¶80.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶80.)

Further, as shown in annotated figure 1 above, the fuse 10 ("non-volatile programmable element") is coupled between Vcc ("first terminal") and node 14 ("terminal T1"), thereby forming an "electrical path" between Vcc ("first terminal") and node 14 ("terminal T1"). When the fuse 10 is intact and therefore "conductive," the fuse connects Vcc ("first terminal") to node 14 ("terminal T1").

(Ex. 1006, 2:8-11; *See* citations and discussion regarding the operation of the circuit in figure 1 of McAdams at Section IX.A.1(a) *supra*.) Therefore, McAdams discloses "when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal." (Ex. 1002, ¶81.)

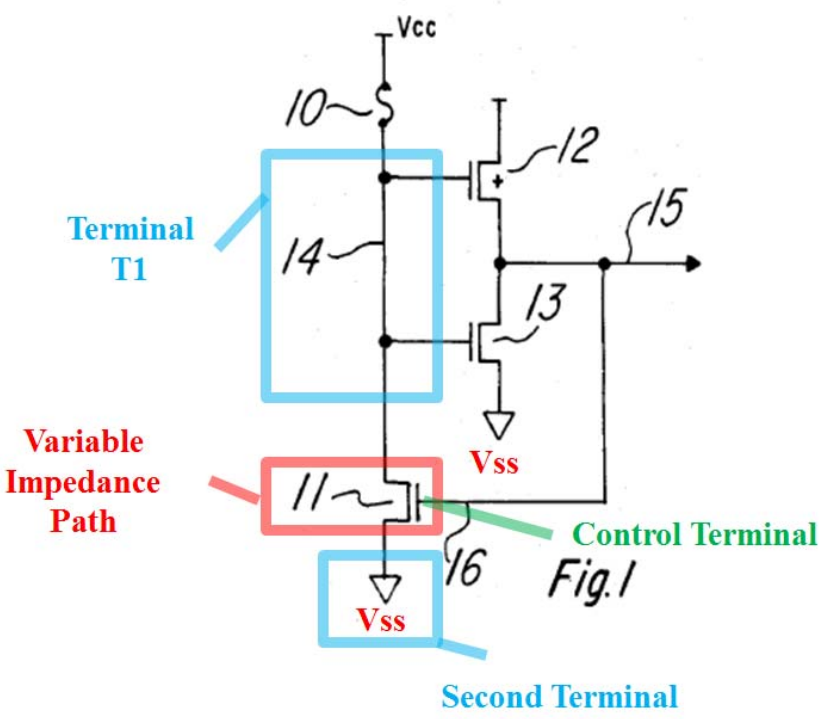
When the fuse 10 is blown and therefore "non-conductive," the fuse does not connect Vcc ("first terminal") to node 14 ("terminal T1"). (Ex. 1006, 2:21-24 (explaining that even though Vcc is powered up, node 14 remains at Vss when the fuse is blown); *see also* citations and discussion regarding the operation of the circuit in figure 1 of McAdams at Section IX.A.1(a) *supra*; Ex. 1002, ¶82.) Therefore, McAdams discloses "when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal." (Ex. 1002, ¶82.)

Because the state of the fuse may be modified or programmed to determine whether the electrical path connects Vcc ("first terminal") to node 14 ("terminal T1"), McAdams discloses a "programmable electrical path" having the features recited in claim element 1[e]. (*Id.,* ¶83.)

> f) a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and

McAdams discloses this feature. (Ex. 1002, ¶¶84-88.) For example, the N-channel (NMOS) transistor 11 highlighted below in annotated figure 1 is a

"variable-impedance electrical path." (*Id.*, ¶84.) Such an understanding is consistent with the disclosure of the '492 patent, which shows an NMOS transistor as the "variable-impedance electrical path" in the embodiment of figure 2A. (Ex. 1001, FIG. 2A; Ex. 1002, ¶84.) Moreover, claim 10, which depends from claim 1 recites "the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal," thereby demonstrating that a transistor is a "variable-impedance electrical path" in the context of claim 1 and the '492 patent. (Ex. 1001, 9:28-30; Ex. 1002, ¶85.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶85.)

As shown in annotated figure 1 above, the NMOS transistor 11 ("variable-impedance electrical path") is coupled between node 14 ("terminal T1") and Vss

("second terminal") and therefore constitutes a "variable-impedance electrical path connected between the terminal T1 and the second terminal." (Ex. 1002, ¶86.)

McAdams further discloses that "the impedance of the electrical path is controlled by a signal on the terminal T1," as recited in claim element 1(f). For instance, as shown in annotated figure 1 above, the signal on node 14 ("terminal T1") is inverted by the CMOS inverter collectively formed by transistors 12 and 13, and the output of the inverter at node 15 is coupled to the gate of the NMOS transistor 11. (*See* Ex. 1006, FIG. 1.) A POSITA would have understood that the voltage on the gate terminal of the NMOS transistor 11 controls whether the transistor 11 is on or off. (Ex. 1002, ¶87.)

If the NMOS transistor 11 is on, it has a lower impedance than when the NMOS transistor 11 is off. (*Id.,* ¶88.) Therefore, the signal at node 14 ("terminal T1") determines the signal at node 15, which in turn determines whether the NMOS transistor 11 is on or off, i.e., has a low or high impedance ("the impedance of the electrical path[4] is controlled by a signal on the terminal T1"). (*Id*.; Ex. 1006, 2:12-26.)

[4] For purposes of this proceeding, Petitioner assumes that "the electrical path" refers to the "variable-impedance electrical path" recited in claim 1 and not the

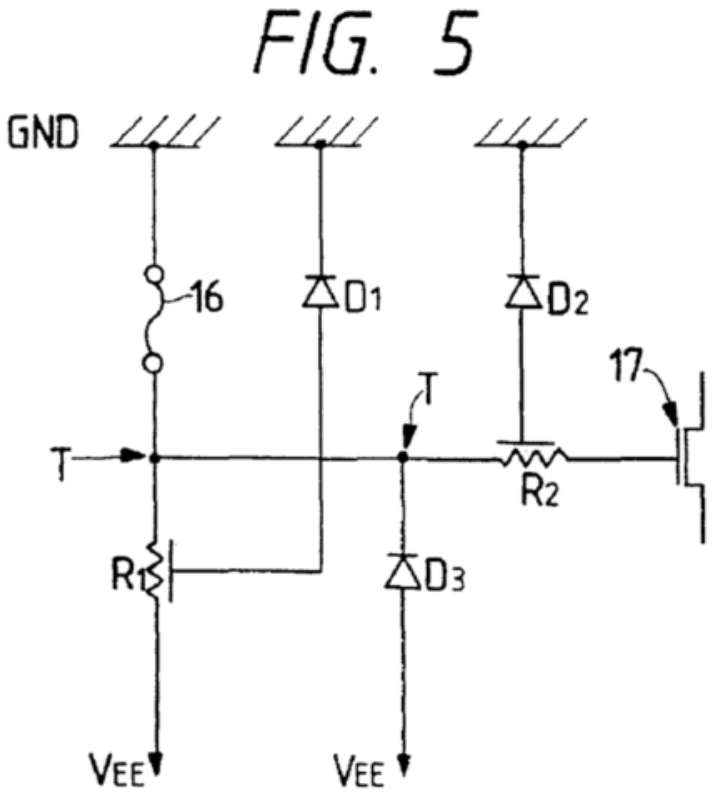
g) a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶89-115.) McAdams does not explicitly disclose "a diode" for keeping the voltage on the terminal T1 within a predetermined range of values as recited in claim element 1[g]. But Uda discloses such a feature. (*Id.,* ¶89.) In view of Uda, a POSITA would have been motivated to include a diode in McAdams for keeping the voltage on node 14 ("terminal T1") within a predetermined range of values. (*Id.,* ¶¶89-108.)

Uda, like McAdams, is in the field of semiconductor integrated circuit devices, including redundancy circuits for memory devices that use fuses to enable such redundancy circuits. (Ex. 1006, 1:5-12, 1:41-51, FIG. 1; Ex. 1007, 1:10-17, 3:15-19, 3:32-37, FIG. 5; Ex. 1002, ¶90.) Therefore, a POSITA implementing the circuit of McAdams would have had reason to look to Uda. (Ex. 1002, ¶90.)

Uda discloses "[a] fuse arrangement that acts to replace a defective cell with the corresponding backup cell," where figure 5 depicts "how the fuse arrangement is connected" in one embodiment. (Ex. 1007, 9:21-29.)

"programmable electrical path" that is also recited in claim 1. Petitioner, however, does not concede that claim 1 is not indefinite under 35 U.S.C. § 112.



(*Id.*, FIG. 5.)

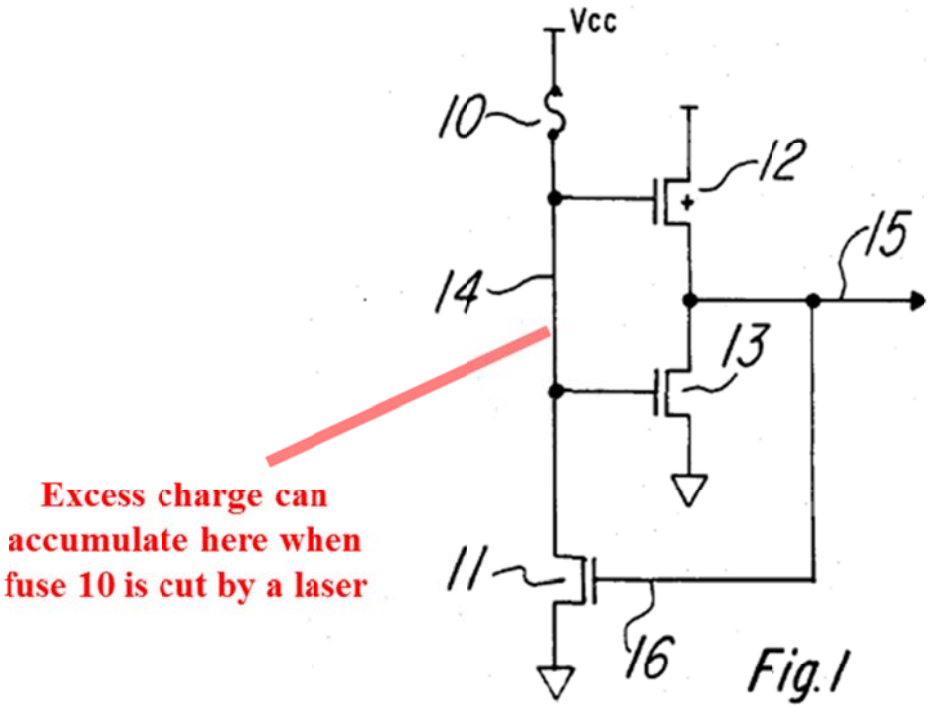
Uda discloses that "[t]he fuses are melted, illustratively, by use of a laser means or electrical means." (*Id.*, 1:38-42.) Uda further discloses that "[t]he purpose of furnishing diodes D1 through D3 and the resistor R2 is to prevent gate destruction that would otherwise occur if an excess charge stemming from laser cutting reaches the NMOS gate." (*Id.*, 9:44-47.) Specifically, Uda discloses that "[i]f a positive charge develops, the charge is led to the ground line GND via the diodes D1 and D2," which contributes to protecting the NMOS gate 17 from

destruction. (*Id.,* 9:47-53.) As discussed below, in view of Uda's teachings, a POSITA would have found it obvious to include a diode like that disclosed in Uda, in McAdams' figure 1 circuit. (Ex. 1002, ¶¶91-93.)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007). Under this flexible approach, it important to identify "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements" in the way claimed. *Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356–57 (Fed. Cir. 2007). Such a reason may be found "explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill." *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (internal quotations and citations omitted); *see also KSR*, 550 U.S. at 419-20.

Under the law of obviousness, including the above principles, the combination of McAdams with Uda would have been obvious to a POSITA. (Ex. 1002, ¶¶92-105.) This is because, *inter alia*, implementing a diode in McAdams'

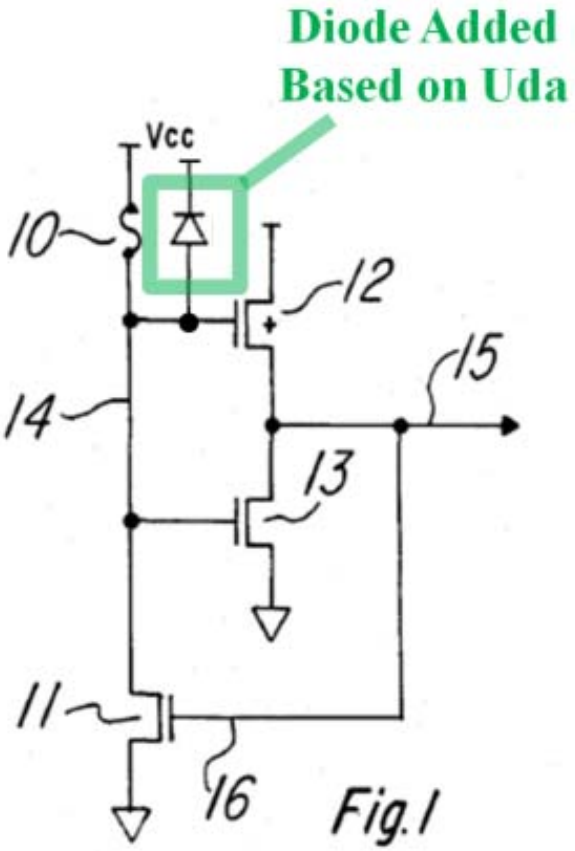
circuit would have solved a potential problem that could arise in McAdams' circuit. (Ex. 1002, ¶92.) Specifically, McAdams, like Uda, discloses that a laser can be used to program the fuse 10 shown in figure 1 of McAdams. (Ex. 1006, 1:12-14 ("These fuses are usually polysilicon conductor strips that are selectively blown by an indexed laser beam.").) A POSITA would have recognized that when a laser is used to blow a fuse (i.e., program the fuse), charge from the laser can accumulate at various points in the circuit. (Ex. 1007, 9:44-47; Ex. 1002,¶¶93-94.) As shown below, just like in Uda, one place in the McAdams' circuit where excess charge can accumulate is node 14, which is connected to the gates of transistors 12 and 13. (Ex. 1002, ¶94.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶94.) This excess charge must be removed because otherwise the gates of transistors 12 and 13 could be damaged. (Ex. 1007, 9:44-47; Ex. 1002, ¶¶96-97 (explaining that excess charge on the gate could result in the voltage on the gate exceeding a permissible value).)

Including a diode, like in Uda, would have been a straightforward way of solving this problem, which a POSITA would have recognized based on Uda's teachings. (Ex. 1002, ¶98.) Therefore, based on the teachings of Uda, a POSITA would have been motivated to modify the circuit of figure 1 in McAdams to implement a diode like that disclosed in Uda in order to provide protection for the

transistors 12 and 13, the gates of which are connected to node 14. (*Id.*, ¶¶95-103.) For example, in view of Uda, a POSITA would have been motivated to implement, *inter alia*, a diode connected between the node 14 and the power supply voltage V_{CC} such that when the fuse 10 is programmed using a laser, any excess charge on node 14 stemming from the laser cutting of the fuse would be led to the power supply node V_{CC} thereby limiting the maximum voltage experienced by the gates of transistors 12 and 13. (*Id.*) As a non-limiting example, a demonstrative is provided below showing certain aspects of the combined McAdams-Uda circuit that a POSITA would have found to be consistent with the modification of the circuit of FIG. 1 of McAdams based on Uda. (*Id.*, ¶95.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶95.)

Accordingly, a POSITA would have found it obvious to combine the teachings of McAdams and Uda as described above to implement a fuse-based redundancy circuit that is more robust in that potential damage to transistors 12 and 13 is avoided when the fuse in the circuit is blown using a laser. (*Id.*, ¶¶104-105.)

First, such a modification of McAdam's disclosed circuit would have been within the capabilities of a POSITA because of the similarities between figure 1 of McAdams and figure 5 of Uda, and because Uda discloses how such a diode is included in a fuse-based circuit and explains how the diode allows excess charge

on a node coupled to one end of the fuse to be led to a supply voltage. (*Id.*, ¶104.) For example, the McAdams circuit is similar to Uda's circuit because, just like Uda includes a fuse between the gate of transistor 17 and a power supply terminal,[5] McAdams, includes a fuse connected between node 14 and a power supply terminal (V_{CC}), where the node 14, also like Uda, is used to provide a signal to the gate of a transistor. (*Id.*) Moreover, a POSITA would have known from Uda that the diode must be connected between node 14 and Vcc to ensure that any charge resulting from laser-cutting that builds up on node 14, which corresponds to the gates of transistors 12 and 13, is removed. (*Id.*, ¶¶99-101(explaining why the diode would not be connected between node 14 and ground in McAdams).) A POSITA would have thus had the capability to modify McAdams based on Uda as noted above. (*Id.*, ¶¶102-103.)

[5] In Uda, the power supply terminal is GND. (Ex. 1007, FIG. 5.) But Uda's power supply terminal (GND) is analogous to Vcc in McAdams because both terminals receive the highest voltage in the circuit. (Ex. 1002, ¶104, n.7.) Specifically, in Uda, the GND terminal receives 0V whereas the VEE terminal receives -4V. (Ex. 1007, 9:28-36.) In McAdams, the Vcc node goes from 0V to 5V and Vss is at ground (i.e., 0V). (Ex. 1006, FIG. 1, 2:8-11, claim 4.)

Second, as discussed above, a POSITA would have recognized that adding the diode in the McAdams circuit would have provided protection for the transistors 12 and 13 in the event that any excess charge is deposited on node 14 during laser cutting of the fuse 10. (*Id.*, ¶104.) Adding the diode in the McAdams circuit would have made the McAdams circuit more robust, and therefore, a POSITA would have been motivated to, and would have found it obvious to, make the above noted modification of the McAdams circuit based on Uda. (*Id.*) *See v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"); *KSR*, 550 U.S. at 424 ("the proper question to have asked was whether a pedal designer of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to upgrading Asano with a sensor").

Moreover, including the diode similar to that disclosed by Uda in the circuit of figure 1 of McAdams would not have negatively impacted the disclosed circuit and would have solved a known problem arising from charge accumulation in fuse-based circuits like McAdams. (Ex. 1002, ¶105.) *See ZUP*, 896 F.3d at 1371-72 (solving a problem or need well-known in the prior art provides a motivation to combine); *KSR* at 419-20 (a patent claim "can be proved obvious [] by noting that there existed at the time of invention a known problem for which there was an

obvious solution encompassed by the . . . [claim].") Indeed, the above modification of McAdams based on Uda would have been a predictable combination of known components according to known methods (e.g., replication of Uda's transistor-protecting diode in the fuse-based redundancy circuit disclosed by McAdams), and would have been consistent with the expected result that it would be less likely that transistors 12 and 13 would be damaged when the laser is used to blow fuse 10. (Ex. 1002, ¶105.) *KSR*, 550 U.S. at 416.

The circuit illustrated in the demonstrative above for the McAdams-Uda combination discloses claim element 1[g], as explained below. (Ex. 1002, ¶106.) McAdams discloses that before power is supplied to the latch shown in figure 1, the supply voltage V_{CC} is at 0V (ground). (Ex. 1006, 2:8-9 ("During power-up of the supply voltage V_{CC}, as V_{CC} goes from zero to +5 v ….").) A POSITA would have understood that when V_{CC} is at 0V (i.e., "before power is supplied to the latch"), the diode in the combined McAdams-Uda circuit would not allow the voltage at node 14 to exceed 0 volts by more than a threshold voltage of the diode. (Ex. 1002, ¶107.) Such an understanding is consistent with the disclosure of the '492 patent. (Ex. 1001, 2:1-12; Ex. 1002, ¶107.)

Therefore, the combined McAdams-Uda circuit discloses "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch." (Ex. 1002, ¶108.) That is, the diode keeps the

voltage on terminal T1 below the diode threshold ("predetermined range of values") before power is supplied to the latch. (*Id*.) The "predetermined range" within which the McAdams-Uda circuit keeps the voltage at node 14 ("terminal T1") is consistent with a "predetermined range" as understood by the '492 patent as claim 13, which depends from claim 1, recites "said predetermined range consists of all voltages below a predetermined value." (Ex. 1001, 9:50-52; Ex. 1002, ¶108.) As discussed above, in the McAdams-Uda combination, the diode keeps the voltage on terminal T1 below the diode threshold and therefore "within a predetermined range of values," consistent with claim 13. (Ex. 1002, ¶108.)

A POSITA would also have understood that the addition of the diode would not only keep the voltage on node 14 ("terminal T1") "within a predetermined range of values before power is supplied to the latch," but the diode would also "**prevent the latch from assuming an incorrect state when power is supplied to the latch,**" as recited in claim element 1[g] (emphasis added). (Ex. 1002, ¶¶109-115.) Specifically, a POSITA would have understood that in the correct state of the latch, the voltage on node 14 is Vcc (+5V) if the fuse 10 is not blown and Vss (0V) if the fuse 10 is blown. (*Id.,* ¶109.) The diode in the McAdams-Uda combination would have ensured the latch circuit operates correctly when power is supplied thereto (e.g. V_{CC} goes from 0 v to +5 v). (*Id*.) For instance, consider the situation in which the fuse 10 is blown. If the latch assumes a correct state when

power is supplied to the latch, the voltage on node 14 should be 0V, as discussed above. (*Id.,* ¶110.) Based on the discussion in the background of the '492 patent, in the absence of the diode, node 14 would be floating when power is applied. (Ex. 1001, 1:36-47; *Id.,* ¶110.) As also discussed in the '492 patent, there is some concern that in such a situation there may be excess charge on node 14. (*Id.*) If such a situation exists, as the '492 patent suggests, and power was supplied to the latch of McAdams, the voltage on node 14 could be high enough that transistor 13 would turn ON, pulling down the gate of transistor 11. (*Id.,* ¶110.) This would result in transistor 11 remaining OFF. (*Id.*) As a result, node 14 would continue to remain at a high voltage as the excess charge on node 14 would not be drained to Vss by transistor 11 even though fuse 10 is blown. (*Id.*) That is, the latch would have assumed an *incorrect* state when power is supplied to the latch. (*Id.*)

But the diode included in the McAdams-Uda combination to protect the transistors 12 and 13 from damage during laser-programming also ensures that any excess charge on node 14 bleeds away such that if the fuse 10 has been blown, PMOS transistor 12 (and not NMOS transistor 13) will turn ON as soon as V_{CC} becomes high enough so that the threshold voltage for transistor 12 is reached. (Ex. 1006, 2:21-24; Ex. 1002, ¶111.) Specifically, before power is supplied to the latch, the Vcc node in the McAdams-Uda combination is at 0V. (Ex. 1006, 2:8-9 ("During power-up of the supply voltage V_{CC}, as V_{CC} goes from zero to +5 v

….").) Therefore, before power is supplied to the latch the voltage on the node 14 will be held at or below the threshold voltage of the diode included in the McAdams-Uda circuit. (Ex. 1002, ¶112; *see* Ex. 1001, 2:33-50 (explaining that if the cathode of the diode is at ground, the anode can go no higher than a threshold of the diode (e.g., +0.65V).) Accordingly, when power is supplied to the circuit, the voltage on node 14 is necessarily near zero because of the presence of the diode, and therefore the gate-to-source voltage for the PMOS transistor 12 will quickly surpass the threshold voltage as V_{CC} goes from 0 v to +5 v. (Ex. 1002, ¶113.) As disclosed by McAdams, when transistor 12 turns on, it pulls the output node 15 high, thereby turning on NMOS transistor 11, which keeps the node 14 at V_{SS} and ensures that the output of the latch correctly reflects the state of the fuse 10. (Ex. 1006, 2:21-26.) Therefore, the diode in the McAdams-Uda combination "**prevents the latch from assuming an incorrect state when power is supplied to the latch**" because it ensures that if the fuse is blown and power is then supplied, the voltage on node 14 is quickly pulled down to Vss, which is the correct state of the latch if the fuse is blown. (Ex.1002 at ¶113.) Indeed, the diode in the McAdams-Uda circuit works just like diode 234 in the '492 patent. (*Id.*; Ex. 1001, FIG. 2A, 2:33-50.)

Notably, if the fuse 10 is not blown when power is applied, the node 14 will rise with V_{CC} as it goes from 0 v to +5 v, and the diode will remain off as the same

voltage (V_{CC}) is at the anode and the cathode of the diode. (Ex. 1002, ¶114.) The high voltage on the node 14 turns on transistor 13 pulling node 15 low and maintaining transistor 11 in the off state. Thus, the diode does not interfere with the operation of the circuit when the fuse is not blown. (*Id*.)

For the above reasons, the combined McAdams-Uda circuit discloses or suggests "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied, to the latch to prevent the latch from assuming an incorrect state when power is supplied to the latch." (*Id.*, ¶¶89-115.)

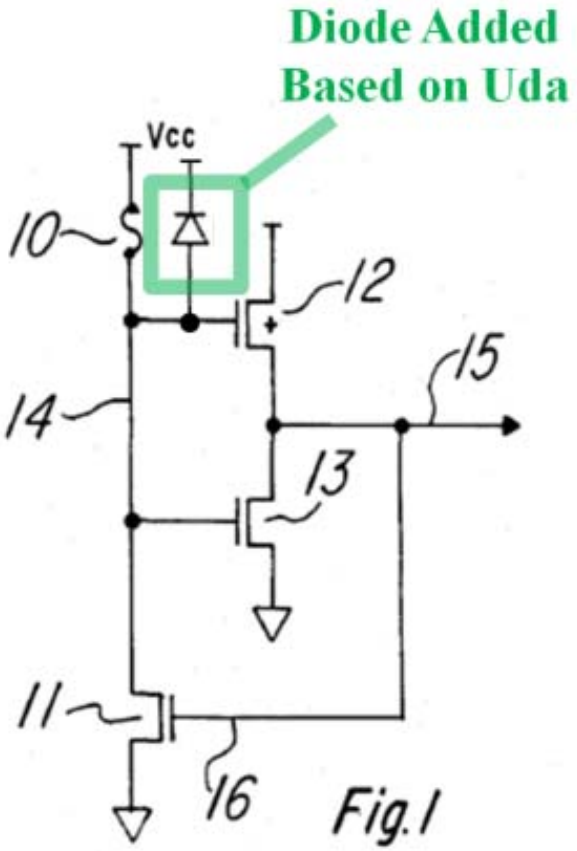
2. Claim 2

a) The programmable latch of claim 1 wherein during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltages.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶116-118.) As discussed above with respect to claim element 1[a], when power is applied, the voltage at node 14 ("terminal T1") is only influenced by the power supply voltage Vcc and Vss ("first and second voltage") and the state of the fuse 10 ("programmable element"). (*See supra* Section IX.A.1(a); Ex. 1006, 1:67-2:34.) If the fuse 10 is not blown, node 14 is pulled to Vcc when power is supplied (i.e., during operation of the latch). (*See supra* Section IX.A.1(a); Ex. 1006, 1:67-2:34.) If the fuse is blown, node 14 is pulled to Vss when power is supplied (i.e., during operation of the latch). (*See supra* Section IX.A.1(a); Ex. 1006, 1:67-2:34.) No

outside signals are provided to the fuse circuit in McAdams and therefore, "during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltages." (Ex. 1002, ¶116.)

As shown in the demonstrative below, the inclusion of the diode in the circuit of McAdams based on Uda does not cause the circuit in the McAdams-Uda combination to receive any inputs from outside of the circuit illustrated. (*Id.*, ¶117.) As further discussed above with respect to claim element 1[g], the inclusion of the diode ensures the same operation discussed above when power is supplied to the latch (i.e., node 14 is at VCC if fuse 10 is not blown, whereas node 14 is at VSS if fuse 10 is blown). (*Id*.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶117.)

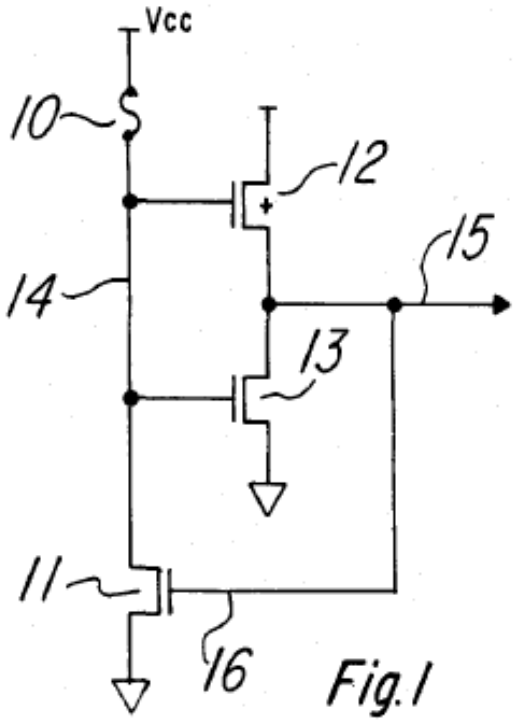
Therefore, the McAdams-Uda combination discloses or suggests claim 2. (Ex. 1002, ¶118.)

3. Claim 3

a) The programmable latch of claim 1 wherein the latch does not receive any latch initialization signal from outside the latch.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶119-120.) As shown in figure 1 of McAdams below, the fuse circuit ("programmable latch") of McAdams does not receive any inputs from outside of

the circuit illustrated and the state of the latch is completely determined by the state of the fuse 10 and the voltages on the Vcc and Vss terminals. (*See supra* Section IX.A.2; Ex. 1006, FIG. 1; Ex. 1002, ¶119.)

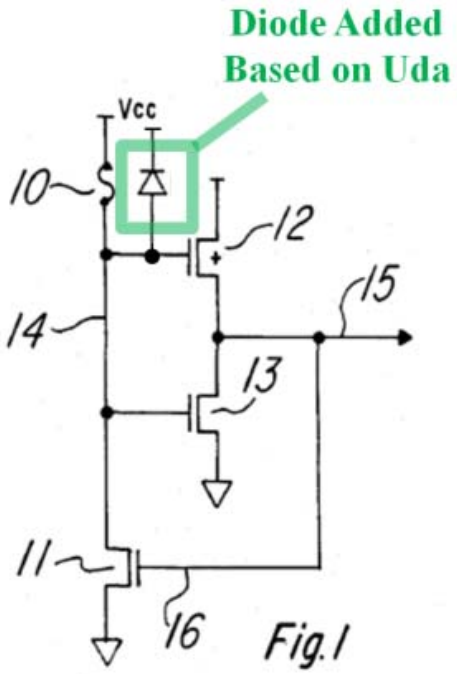


(Ex. 1006, FIG. 1.)

Therefore, McAdams discloses "wherein the latch does not receive any latch initialization signal from outside the latch." (Ex. 1002, ¶120.)

Further, as shown in the demonstrative below, the inclusion of the diode in the circuit of McAdams based on Uda does not cause the circuit in the McAdams-Uda combination to receive any inputs from outside of the circuit illustrated. (*Id.*, ¶120.) Therefore, the McAdams-Uda combination discloses or suggests "wherein the latch does not receive any latch initialization signal from outside the latch" for

the same reasons discussed above with respect to claim 2. (*Id.*; *see supra* Section IX.A.2.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶120.)

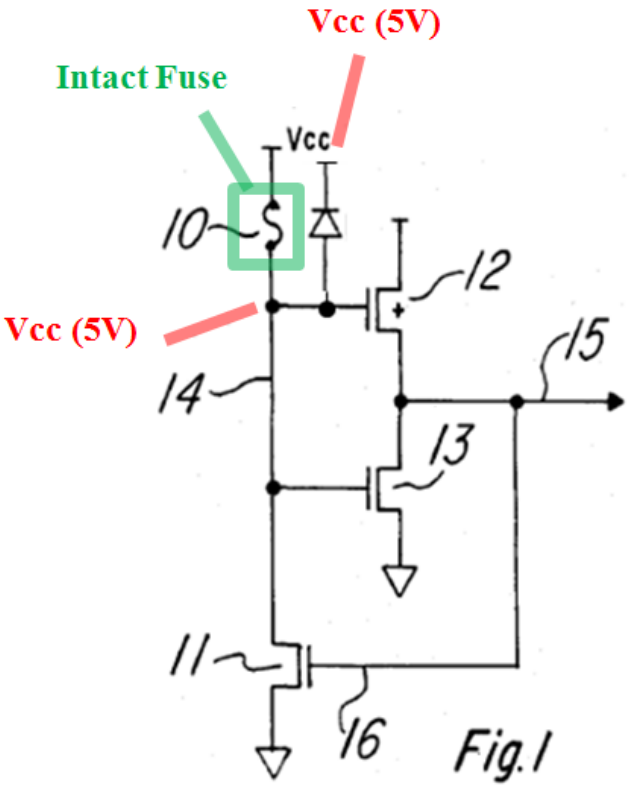
4. Claim 4

a) The programmable latch of claim 1 wherein no current flows through the diode during normal operation of the latch, but when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶121-126.) In order for current to flow through the diode included in the McAdams-Uda combination, the diode must be in the "forward bias" state, i.e., the

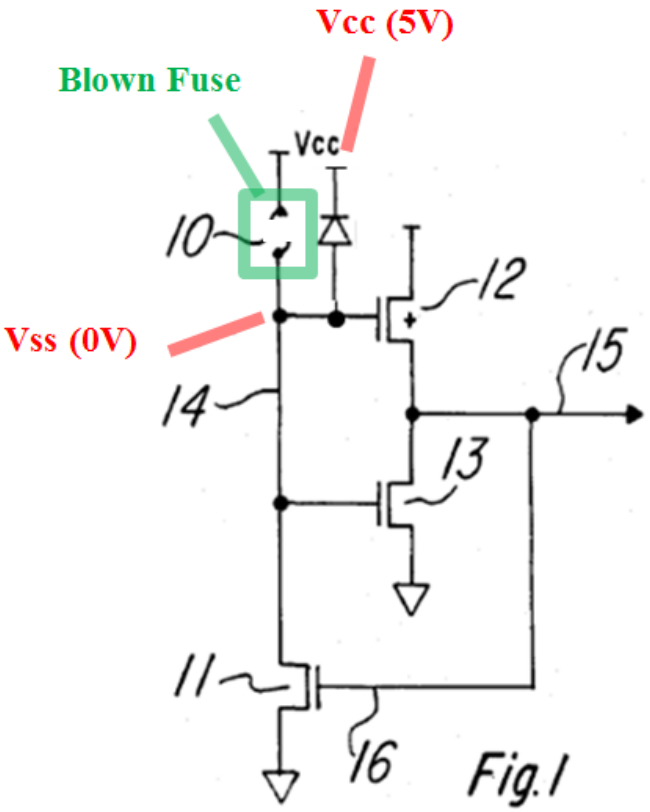
voltage on the anode of the diode must be greater than the voltage on the cathode of the diode by at least the threshold voltage of the diode. (*Id.,* ¶121.)

When power is applied to the fuse circuit ("programmable latch") during normal operation of the latch in the McAdams-Uda combination, the first terminal is connected to Vcc, which corresponds to 5V. (Ex. 1006, 2:2-3, 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v".) In this scenario, the diode is not in a "forward bias" state and thus no current flows through the diode. (Ex. 1002, ¶122.) In particular, as shown in the demonstrative below, when the fuse 10 is intact, the fuse provides an electrical path from the "first terminal" (Vcc) to the node 14 and therefore the voltage at node 14 is also at Vcc (5V). As such, the voltage at both the anode (node 14) and the cathode (first terminal) of the diode is Vcc or 5V. Therefore, the voltage at the anode of the diode (5V) does not exceed the voltage at the cathode of the diode (also 5V) by at least a threshold voltage of the diode and no current flows through the diode. (Ex. 1002, ¶122.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶122.)

Similarly, during operation of the latch when the fuse has been blown, node 14 is pulled low to ground (Vss) by the transistor 11. (*See supra* Section IX.A.1(a); Ex. 1002, ¶123.) As such, the voltage on the anode of the diode (node 14) is Vss (0V) and the voltage on the cathode of the diode (first terminal) is Vcc (5V). Therefore, the voltage at the anode of the diode (0V) does not exceed the voltage at the cathode of the diode (5V) by at least a threshold voltage of the diode and no current flows through the diode. (Ex. 1002, ¶123.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶123.)

As demonstrated above, when power is applied to the programmable latch of the McAdams-Uda combination (i.e., during normal operation), no current flows through the diode regardless as to whether or not the fuse has been blown. (Ex. 1002, ¶124.) Therefore, the McAdams-Uda combination discloses "wherein no current flows through the diode during normal operation of the latch." (*Id.*)

As disclosed by McAdams, when the power is off, the power supply voltage Vcc is at 0V. (Ex. 1006, 2:8-9 ("During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v".)) As discussed above with respect to claim element

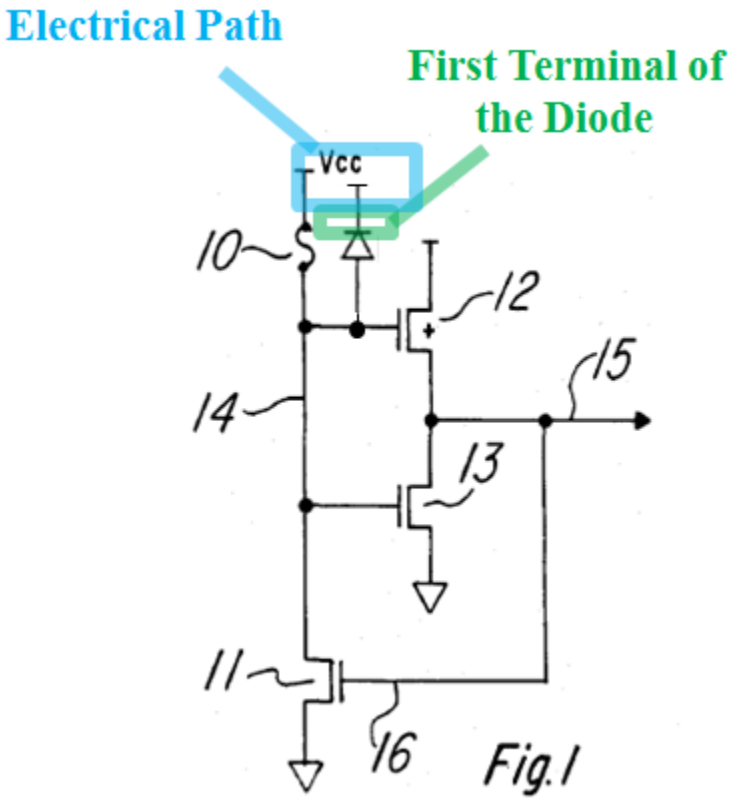
1[g], when the power is off, the diode in the combined McAdams-Uda circuit will not allow the voltage at node 14 to exceed 0V by more than a threshold voltage of the diode. (Ex. 1002, ¶125.) This is because if the voltage on the anode of the diode (node 14) were more than a threshold voltage above the voltage at the cathode of the diode (0V), the threshold voltage of the diode would be exceeded and the diode would turn on, thereby causing current to flow through the diode from node 14 to ground. (*Id.*). Such current flow would continue until the voltage across the diode becomes less than the threshold voltage and the diode turns off. (*Id.*).

Therefore, the combined McAdams-Uda circuit discloses or suggests that when the power is off, Vcc is at 0V, and current flows through the diode if the voltage on node 14 ("terminal T1") exceeds the threshold voltage of the diode ("when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values"). (*See supra* Section IX.A.1(g) describing that the "predetermined range of values" is the range of voltages less than the diode threshold voltage; Ex. 1002, ¶126.)

5. Claim 5

a) The programmable latch of claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶127-130.) As shown in the demonstrative below, the diode of the McAdams-Uda combination has a first terminal corresponding to the cathode of the diode. (*Id.*, ¶127.) As disclosed by McAdams, when power is not applied to the fuse circuit, the power supply node Vcc is at 0V. (Ex. 1006, 2:8-9 ("During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v").) Therefore, McAdams necessarily discloses an electrical path from the terminal marked as Vcc to a ground terminal because the voltage at the terminal marked Vcc is at 0V when power is not supplied to the fuse circuit. (Ex. 1002, ¶127.) Accordingly, when power is not supplied to the fuse circuit, there is an electrical path from the cathode of the diode ("first terminal of the diode") to a "ground terminal" because the voltage on the cathode of the diode is 0V. (*Id*.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶127.)

Further, as shown in the demonstrative above, the first terminal of the diode is coupled to Vcc, and therefore, there is necessarily "a first electrical path interconnecting a first terminal of the diode and a ground terminal" as McAdams discloses that the terminal Vcc is at ground when power is not supplied to the fuse circuit. (Ex. 1002, ¶128.)

The McAdams-Uda combination also discloses or suggests "wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode." (*Id.*, ¶129.) As disclosed by McAdams, during normal operation

(e.g. when power is supplied to the fuse circuit), Vcc is at 5V. (Ex. 1006, 2:8-9, "During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v".) As discussed above with respect to claim 4, when the voltage at the cathode of the diode is at +5V during normal operation, the diode is off as the anode of the diode is either at 0V or +5V depending on the state of the fuse. (*See supra* Section IX.A.4.) As such, the McAdams-Uda combination discloses that during normal operation the cathode of the diode ("first terminal of the diode") is charged to +5V ("is charged to a voltage that turns off the diode"). (Ex. 1002, ¶129.)

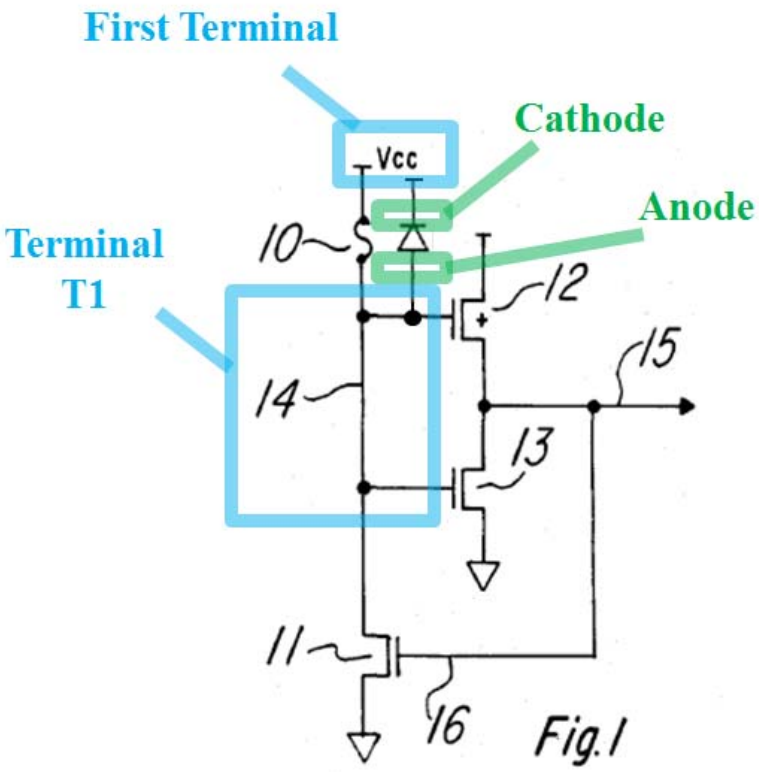
Additionally, as discussed above, when the power is off in the McAdams-Uda combination, the Vcc node is at 0V, and therefore there is necessarily a "first electrical path" that connects the Vcc node to a ground terminal. (*Id.,* ¶130.) Because the Vcc node is grounded and the cathode of the diode is coupled to Vcc, the first terminal of the diode (i.e., the cathode of the diode) will be discharged to ground through the electrical path (i.e., the path that connects the cathode to ground through the Vcc node) when the power is off. (*Id*.) Therefore, the McAdams-Uda combination also discloses or suggests that "when the power is off the first terminal of the diode is discharged through said first electrical path" as recited in claim 5. (*Id*.)

6. Claim 8

a) The programmable latch of claim 1 wherein the diode has one terminal connected to the terminal T1, and the diode

has another terminal connected to the first terminal.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶131-132.) As shown in the demonstrative below, the diode in the McAdams-Uda combination has one terminal (the anode) connected to node 14, which corresponds to "terminal T1." (*See supra* Section IX.A.1(d), (g); Ex. 1002, ¶131.) The diode also has another terminal (the cathode) connected to Vcc, which corresponds to the "first terminal" recited in claim 1 above. (*See supra* Section IX.A.1(b); Ex. 1002, ¶131.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶131.)

Therefore, the McAdams-Uda combination discloses or suggests claim 8. (Ex. 1002, ¶132.)

7. Claim 9

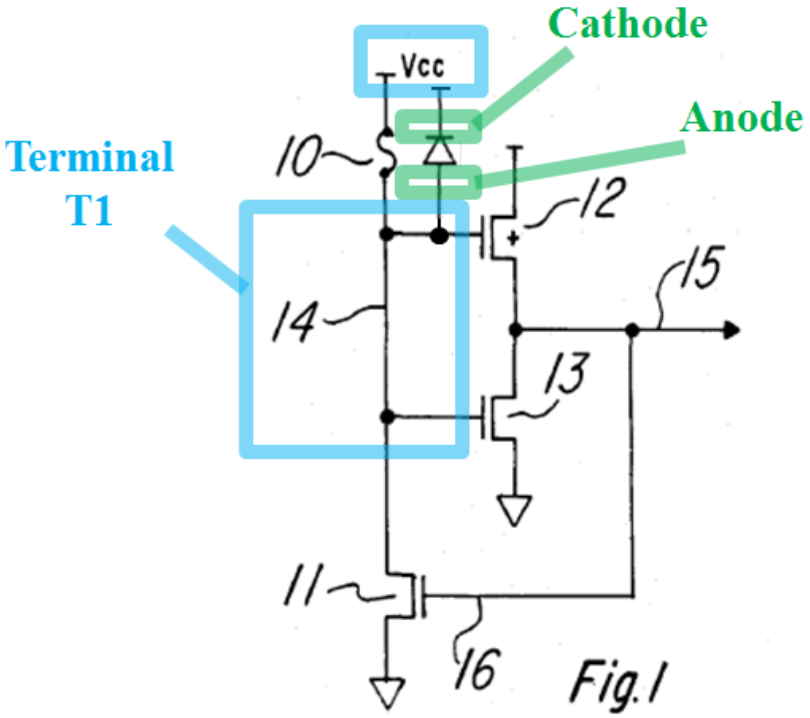
a) The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶133-134.) For example, McAdams discloses that "the principal object of this invention [is] to provide improved fuse circuits exhibiting a low current drain for use in semiconductor integrated circuits such as memory or microcomputer devices, particularly CMOS devices with low standby power dissipation and minimum complexity." (Ex. 1006, 1:33-38.) McAdams further discloses that "[t]his invention relates to semiconductor integrated circuit devices, and more particularly to fuse circuits of the type used in VLSI CMOS semiconductor memory devices or the like." (*Id.,* 1:5-8.)

Therefore, McAdams discloses that the disclosed fuse circuit ("latch") (*see supra* Section IX.A.1(a)) is used in an integrated circuit device such as a memory device ("the latch is an integrated circuit or part of an integrated circuit"). (Ex. 1002, ¶¶133-134.)

b) wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶135-139.) For example, as shown in the demonstrative below, the anode ("one terminal") of the diode in the McAdams-Uda combination is connected to node 14 ("terminal T1") and the cathode ("another terminal") of the diode is connected to Vcc. (*Id.*, ¶135.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶135.)

As discussed above with respect to claim element 1[b], Vcc is a "supply voltage" that is supplied when power is applied to the circuit of figure 1. (Ex. 1006, 2:2-3 ("series circuit is connected between a supply voltage Vcc and Vss"), 2:8-9 ("During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v"), 3:24-26 ("wherein said one of the first and second terminals of said power

supply is a positive voltage and said other is ground"), 4:20-22 ("a power supply having a first terminal at a positive voltage and a second terminal at a ground potential").) In the example embodiment of McAdams, Vcc is at +5 V after power-up of the latch and therefore constitutes "non-ground power-supply voltage." (Ex. 1002, ¶136.) A POSITA would have understood that a power supply voltage for an integrated circuit is typically provided via an external pin and therefore would have understood that the Vcc power-supply voltage in McAdams would have been received "from an external pin of the integrated circuit" on which the fuse circuit is located. (*Id.*)

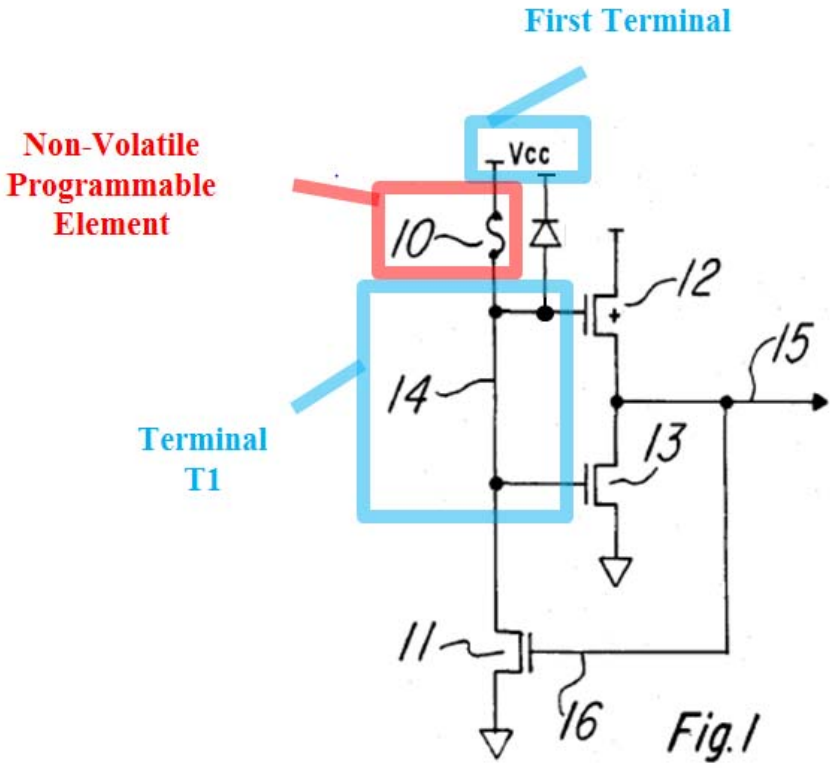
To the extent that McAdams does not disclose that the Vcc terminal receives the non-ground supply voltage from an external pin, it would have been obvious to provide the +5V supply voltage Vcc from an external pin. McAdams discloses that the power supply has a first terminal and a second terminal, where one of the first and second terminals is a positive voltage and the other is ground. (Ex. 1006, 3:3, 3:24-29.) A POSITA would have understood that supply voltages for integrated circuits are commonly supplied via pins on the integrated circuit that permit connectivity to circuitry and voltage sources outside of the integrated circuit. (Ex. 1002, ¶¶137-139.) Therefore, the McAdams-Uda combination discloses or suggests "the diode has one terminal connected to the terminal T1 and

the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit." (*Id*.)

8. Claim 10

a) The programmable latch of claim 1 wherein: the programmable element is a fuse connected to and between the terminal T1 and the first terminal;

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶140.) As demonstrated above with respect to claim element 1[e], McAdams discloses a fuse 10 that constitutes a "programmable element," where the fuse 10 is connected between node 14 ("terminal T1") and Vcc ("the first terminal").) (*See supra* Section IX.A.1(e).) Therefore, the McAdams-Uda combination discloses or suggests "the programmable element is a fuse connected to and between the terminal T1 and the first terminal." (Ex. 1002, ¶140.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶140.)

b) the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal;

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶141-142.) As demonstrated with respect to claim element 1[f] above, the NMOS transistor 11 highlighted in the McAdams-Uda combination below is a "variable-impedance electrical path." (*See supra* Section IX.A.1(f); Ex. 1002, ¶141.)

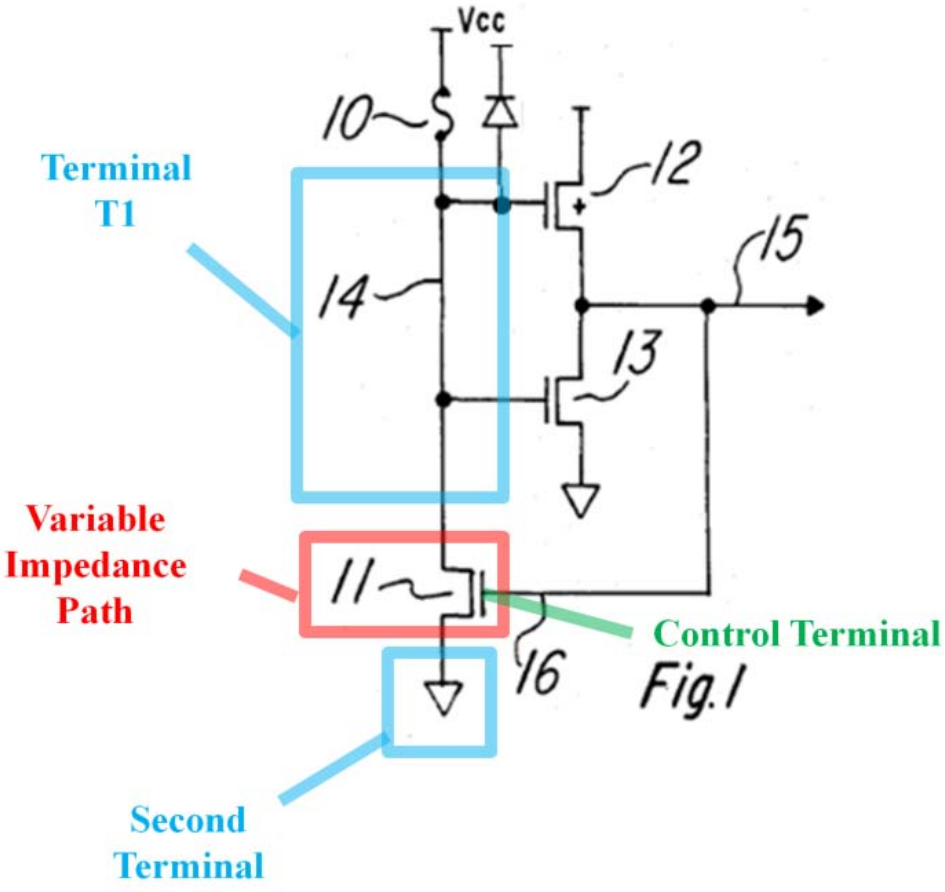


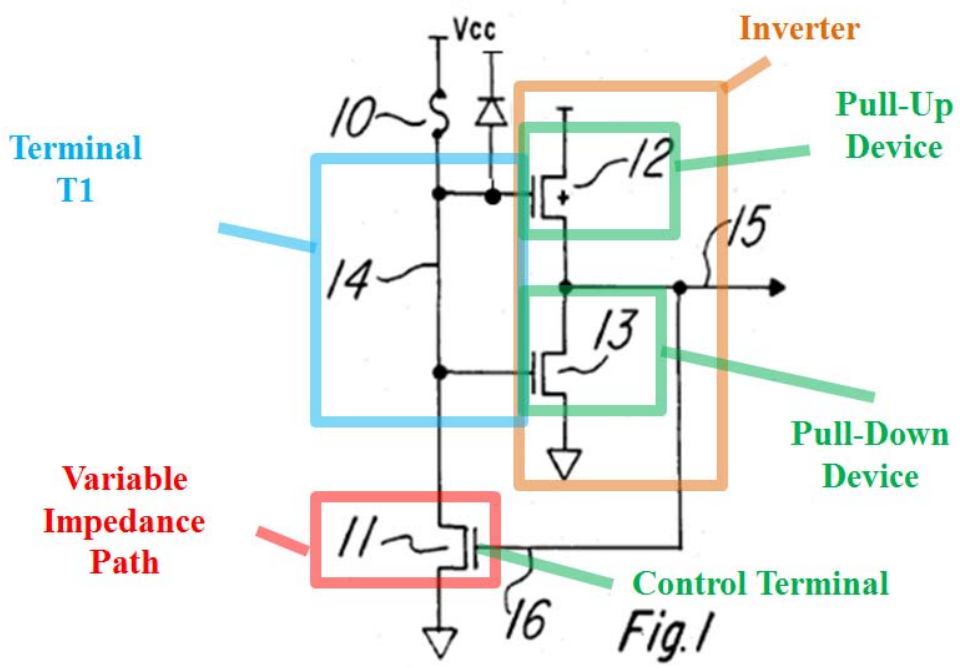
Fig. 1

(Ex. 1002, ¶141.)

As shown in the demonstrative above, the NMOS transistor 11 ("variable-impedance electrical path") is coupled between node 14 ("terminal T1") and Vss ("second terminal") and therefore is "connected to and between the terminal T1 and the second terminal." Furthermore, the gate of transistor 11 is used to control whether the transistor 11 is on or off, and therefore the gate of transistor 11 is a "control terminal." (*See supra* Section IX.A.1(f); Ex. 1002, ¶142.)

c) the programmable latch further comprises an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶143-146.) For example, the McAdams-Uda combination discloses a programmable latch that includes an inverter, where the inverter is highlighted in orange in the demonstrative below.



(Ex. 1002, ¶143.)

As shown in the demonstrative above, the inverter includes P-channel transistor 12 ("pull-up device") coupled between output 15 and Vcc, where, when the P-channel transistor 12 is on, it pulls the voltage at output node 15 up to 5V and therefore would be understood to operate as a "pull-up" transistor in the inverter. (Ex. 1002, ¶144.) Similarly, the inverter includes N-channel transistor 13 ("pull-down device") coupled between output 15 and Vss, where, when the N-channel transistor 13 is on, it pulls the voltage at output node 15 down to V_{ss} and therefore would be understood to operate as a "pull-down" transistor in the inverter. (Ex. 1006, FIG. 1, 2:3-6; Ex. 1002, ¶144.)

As also shown in the demonstrative above, both the P-channel transistor 12 ("pull-up device") and the N-channel transistor 13 ("pull-down device") are coupled to inverter input at node 14, which corresponds to "terminal T1" ("an inverter whose input is connected to the terminal T1"). (Ex. 1006, FIG. 1, 2:3-6; Ex. 1002, ¶145.) Both the P-channel transistor 12 ("pull-up device") and the N-channel transistor 13 ("pull-down device") are also coupled to inverter output at node 15, which corresponds to the input of the gate of transistor 11 ("an inverter … whose output is connected to the control terminal of said transistor"). (Ex. 1002, ¶145.) As is evident from the demonstrative above, both transistors 12 and 13 are connected to the inverter input at node 14 ("at least one of the pull-up and pull-down devices is connected to the inverter input"), and both transistors 12 and 13

are connected to the inverter output at node 15 ("both of the pull-up and pull-down devices are connected to the inverter output"). (*Id.*)

Therefore, the McAdams-Uda combination discloses or suggests "an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output." (Ex. 1002, ¶146.)

9. Claim 13

a) The programmable latch of claim 1 wherein: said predetermined range consists of all voltages below a predetermined value; and

McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶147.) As discussed above with respect to claim element 1[g], the McAdams-Uda combination discloses "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch." (*See supra* Section IX.A.1(g).) Specifically, a POSITA would have understood that when V_{CC} is at 0V (i.e., "before power is supplied to the latch"), the diode in the combined McAdams-Uda circuit would not allow the voltage at node 14 to exceed 0 volts by more than a threshold voltage of the diode. (Ex. 1002, ¶147.) Therefore, the McAdams-Uda combination discloses that the "predetermined range consists of all

voltages below a predetermined value" where the predetermined value is the threshold voltage of the diode. (*Id*.)

b) when the programmable element is conductive, the variable-impedance path is non-conductive.

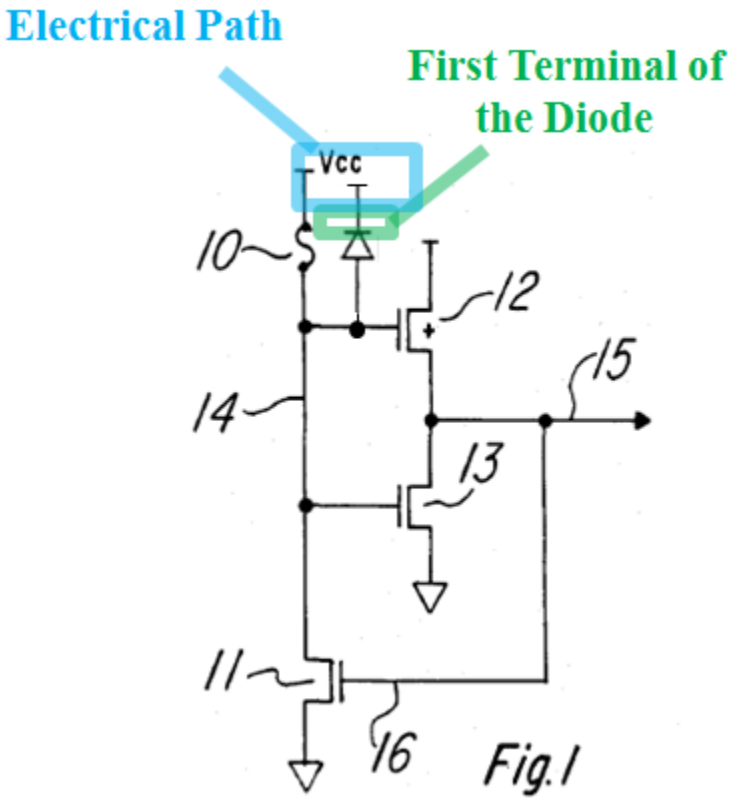
McAdams in view of Uda discloses or suggests this feature. (Ex. 1002, ¶¶148-149.) As discussed above in claim element 1[a], if the fuse in McAdams is not blown ("programmable element is conductive") when power is applied to the circuit, the node 14 follows the power supply Vcc, which turns on transistor 13. (Ex. 1006, 2:8-15; *see supra* Section IX.A.1(a).) When transistor 13 turns on, any charge on the output node 15 is discharged, pulling the output to Vss. (Ex. 1002, ¶148.) The Vss voltage on the output 15 is fed back to the gate of transistor 11 and holds that transistor in the off state ("the variable-impedance path is non-conductive"). (Ex. 1006, 2:8-18.) The inclusion of the diode in the circuit of McAdams based on Uda does not alter this aspect of the operation of the fuse circuit in McAdams. (Ex. 1002, ¶149.) Therefore, the McAdams-Uda combination discloses that the "when the programmable element is conductive, the variable-impedance path is non-conductive." (*Id*.)

B. Ground 2: McAdams, Uda and Keeth Render Obvious Claims 5-7

1. Claim 5

a) The programmable latch of claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.

As explained above with respect to claim 5 in Section IX.A, the McAdams-Uda combination discloses or suggests the features of claim 5. (Ex. 1002, ¶151.) Specifically, the McAdams-Uda combination discloses an electrical path connecting the cathode of the diode ("first terminal of the diode") with a ground terminal when power is not supplied to the fuse circuit because the terminal marked as Vcc in figure 1 of McAdams is 0V (i.e., ground voltage) when power is not supplied to the fuse circuit. (*See supra* Section IX.A.5; Ex. 1006, 2:8-9 ("During power-up of the supply voltage Vcc as Vcc goes from zero to +5 v.").)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶151.)

However, to the extent that PO argues or the Board finds that the combination of McAdams and Uda does not explicitly or necessary disclose or suggest "*a first electrical path interconnecting a first terminal of the diode and a ground terminal*, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path" (emphasis added), such a feature would have been obvious to a POSITA in view of McAdams, Uda, and Keeth. (Ex. 1002, ¶¶152-161.) Specifically, as discussed below, a

POSITA would have been motivated to provide the Vcc voltage (as shown in the McAdams-Uda demonstrative above) from a power supply circuit, which would include a path from the Vcc terminal to a ground terminal. (*Id*.)

At the time of the alleged invention of the '492 patent, it was well-known that memory devices could include an internal power supply generator that would generate an internal power supply from an external voltage supply. (Ex. 1002, ¶153; Ex. 1008, 1:17-35 (explaining that an integrated circuit memory (e.g., a DRAM) "conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts" that is then converted to an internal voltage V_{CCR}); Ex. 1012, 1:19-23.) When implementing the McAdams-Uda system, a POSITA would have understood that McAdams and Uda do not expressly disclose details of the voltage supplies (e.g., Vcc) used therein. (Ex. 1002, ¶153.) But because McAdams and Uda disclose semiconductor memory devices (Ex. 1006, Abstract; Ex. 1007, 1:10-18), a POSITA would have understood that the voltages in their respective circuits (e.g., Vcc in figure 1 of McAdams and V_{EE} in figure 5 of Uda) could be provided from an internal power-supply generator. (Ex. 1002, ¶153.) Therefore, a POSITA looking to implement the McAdams-Uda combination would have looked to references that disclose an internal power-supply generator. (*Id.*)

A POSITA would have therefore looked to Keeth because, as discussed below, Keeth discloses an internal power-supply generator for a memory device

and also explains how its novel internal power-supply generator overcomes several problems of conventional designs for such circuits. (Ex. 1002, ¶153.) Like McAdams and Uda, Keeth relates to memory circuits. (*See, e.g.,* Ex. 1008, 1:11-60; Ex. 1006, Abstract; Ex. 1007, 1:10-18; Ex. 1002, ¶154.) Keeth discloses that an integrated circuit memory (e.g., a DRAM) "conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts." (Ex. 1008, 1:17-19.) This externally applied voltage (V_{CCX}) is converted by a power supply circuit to "an internal voltage V_{CCR}," which is used as the power supply for the memory circuits. (*Id.,* 1:31-34; *see also id.,* Abstract ("internal operating voltage, designated V_{CCR}"), 6:19 ("Signal V_{CCR} . . . powers circuit 30," where circuit 30 includes DRAM, SRAM, etc. (*id.,* 4:12-22).) But the conventional power supply circuits for converting an external power supply voltage to an internal power supply voltage suffered from several problems. (*Id.,* 1:31-60; Ex. 1002, ¶154-155.)

To overcome these deficiencies, Keeth discloses a novel circuit (voltage reference 100) in FIG. 3 that receives an external power signal V_{CCX} and provides the internal power supply voltage V_{CCR}. (*See, e.g.,* Ex. 1008, 1:17-19, 5:58-62, FIG. 3; Ex. 1002, ¶156.) The voltage reference 100 achieves a "piecewise linear relationship between V_{CCX} and V_{CCR}" that alleviates shortcomings of similar prior art circuits. (Ex. 1008, 4:37-5:62.) Specifically, the voltage reference 100 operates over three segments (i.e., three ranges of input values for V_{CCX}) and "[w]hen used

in a dynamic random access memory integrated circuit, operation in the first segment provides data retention at low power consumption. Operation in the second segment supports speed grading individual devices with a margin for properly stating memory performance specifications. Operation in the third segment supports screening at elevated temperatures for identifying weak and defective memory devices." (*Id.,* Abstract; *see also id.,* 4:37-5:62.) According to Keeth, the voltage reference 100 prevents the "useful life of the IC" from being shortened, increases "[s]ystem reliability," and allows "improved integrated circuit testing and screening." (*Id.,* 5:51-54, Abstract; *see also id.,* 4:37-5:62; Ex. 1002, ¶157.)

The voltage reference 100 is shown in FIG. 3 of Keeth.

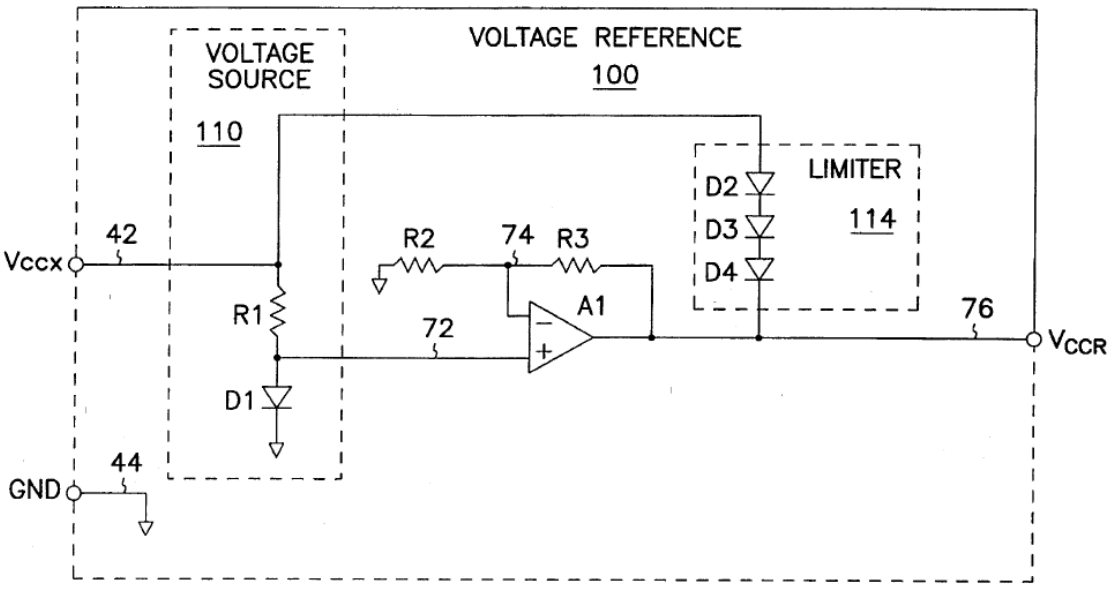


FIG. 3

(*Id.,* FIG. 3.)

Given the above-noted advantages associated with the voltage reference 100, a POSITA would have been motivated to combine the teachings of McAdams, Uda, and Keeth such that the power supply Vcc in figure 1 of McAdams is provided by a circuit similar to voltage reference 100, which receives an external power supply V_{CCX} and converts it to an internal power supply voltage V_{CCR}. (Ex. 1002, ¶158.) When implementing the McAdams-Uda system, a POSITA would have looked to teachings associated with internal power supply circuits, such as those disclosed by Keeth, given that McAdams and Uda do not expressly disclose details of the voltage supplies used therein. (*Id*.) Having looked to Keeth, a POSITA would have found it obvious to combine its teachings with the McAdams-Uda combination because, *inter alia*, the voltage reference 100 prevents the "useful life of the IC" from being shortened, increases "[s]ystem reliability," and allows "improved integrated circuit testing and screening." (*Id*.; Ex. 1008, 5:51-54, Abstract; *see also id.,* 4:37-5:62.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016).

Indeed, the combination of Keeth's voltage reference 100 and the McAdams-Uda circuit would have been nothing more than the combination of familiar elements (e.g. the voltage reference 100 of Keeth and the McAdams-Uda memory device) according to known methods (providing an electrical connection

between the Vcc node in the McAdams-Uda circuit and the V_{CCR} node in the voltage reference 100) that yields an expected result (the power supply in the McAdams-Uda circuit is provided by the voltage reference 100 of Keeth) and therefore, obvious to one of ordinary skill in the art. (Ex. 1002, ¶158.) *KSR*, 550 U.S. at 416.

The combined McAdams-Uda-Keeth system discloses or suggests claim 5. (Ex. 1002, ¶¶159-161.) Specifically, as discussed above, the Vcc terminal in figure 1 of McAdams would be connected to the V_{CCR} terminal in figure 3 of Keeth that is further connected to the ground terminal through a resistor network R2, R3. (Ex. 1008, FIG. 3; Ex. 1002, ¶159.) Accordingly, the McAdams-Uda-Keeth combination discloses an electrical path connecting the cathode of the diode ("first terminal of the diode") in the McAdams-Uda combination with a ground terminal through a resistor network (R2 and R3 like in Keeth). (Ex. 1002, ¶¶159-160.)

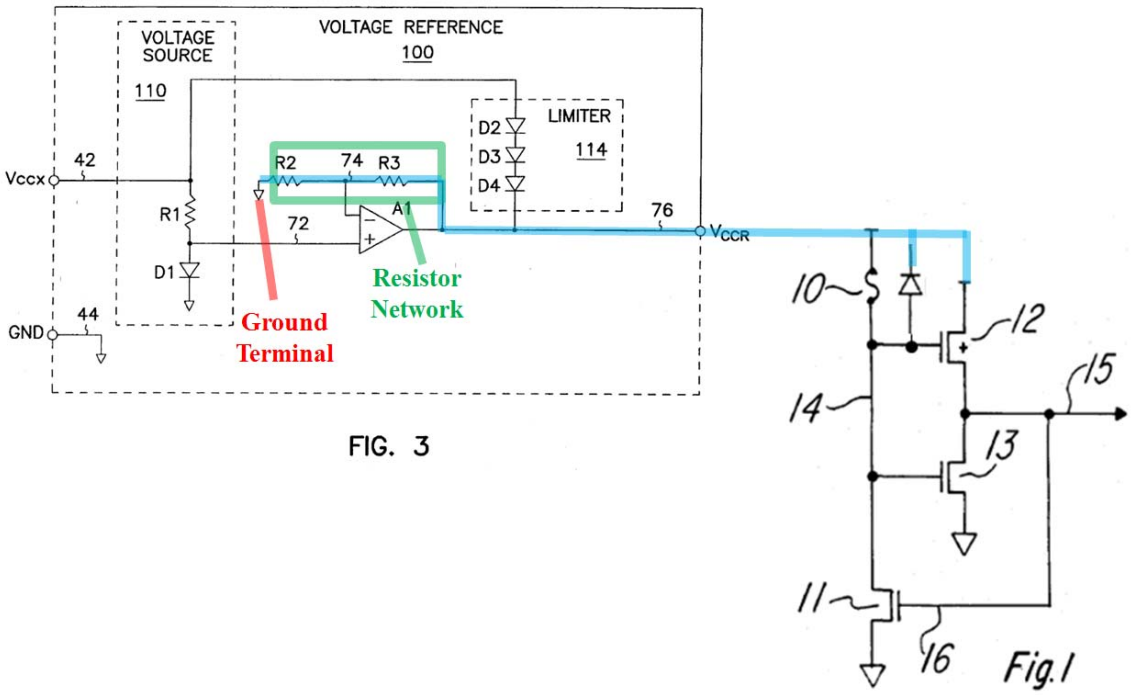


FIG. 3

(Ex. 1002, ¶159 (illustrating a non-limiting configuration of the McAdams-Uda-Keeth combination).)

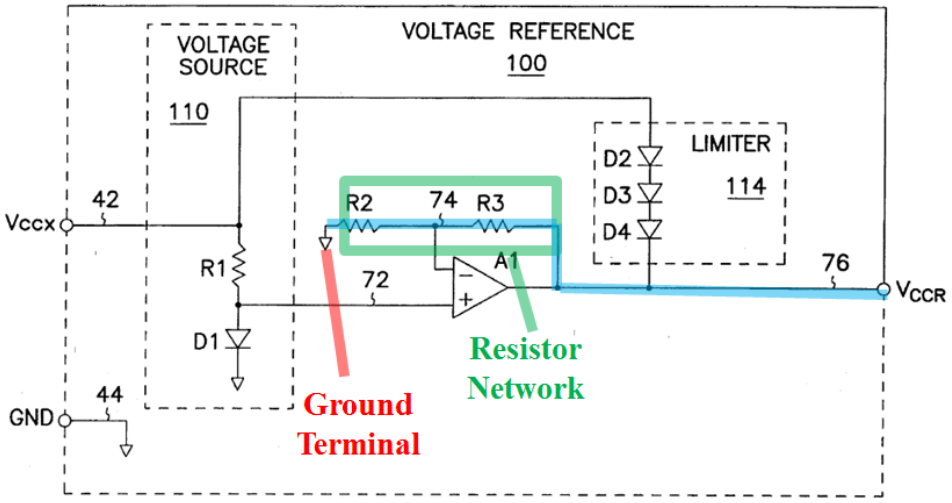


FIG. 3

(Ex. 1008, FIG. 3 (annotated); Ex. 1002, ¶160.)

Additionally, as discussed above, when the power is off in the McAdams-Uda-Keeth combination, the Vcc node remains connected to ground via the "first electrical path" highlighted in blue in the demonstrative above. Because the Vcc node is grounded and the cathode of the diode is coupled to Vcc (and hence coupled to ground as well), the first terminal of the diode (i.e., the cathode of the diode) will be discharged to ground through the electrical path (highlighted in blue above) when the power is off. (Ex. 1002, ¶161.)

2. Claim 6

a) The combination of claim 5 wherein the first electrical path is a resistor or a resistor network.

The combined McAdams-Uda-Keeth system discloses or suggests this limitation. (Ex. 1002, ¶162.) As discussed above in claim 5, in the modified system the disclosed "first electrical path" includes resistors R2 and R3, and thus includes "a resistor or a resistor network." (*Id.*; s*ee supra* Section IX.B.1.)

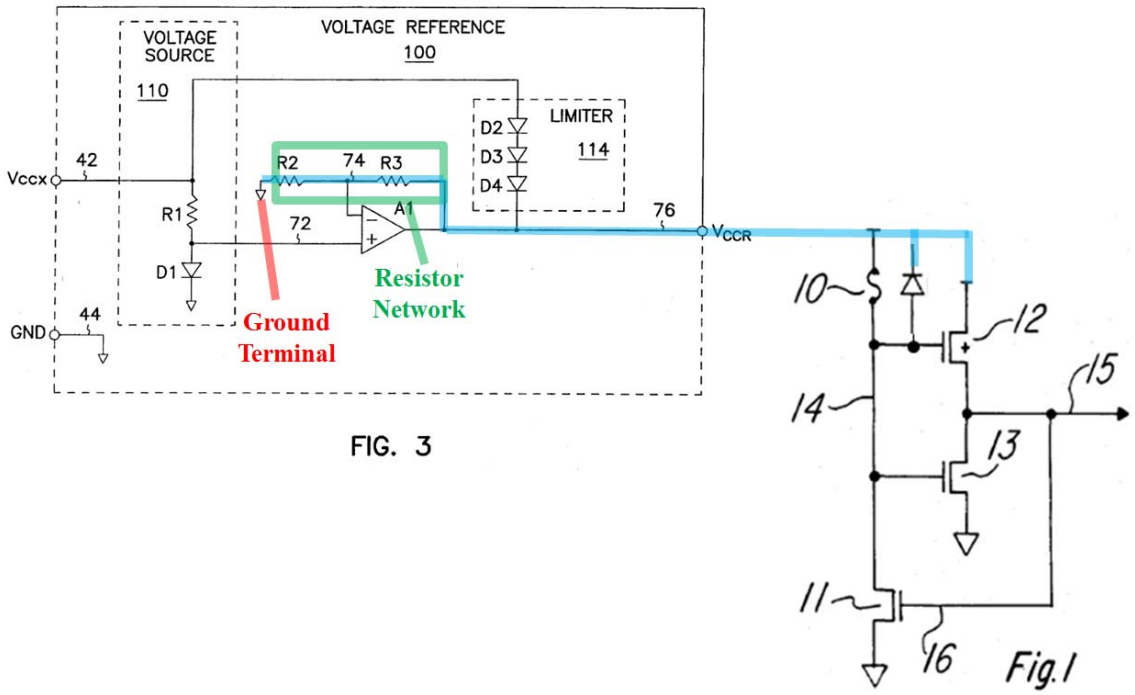


FIG. 3

(Ex. 1002, ¶162.)

3. Claim 7

a) The combination of claim 5 wherein the first electrical path is part of a reference voltage generator whose output is connected to the diode's first terminal.

The combined McAdams-Uda-Keeth system discloses or suggests this limitation. (Ex. 1002, ¶163.) As discussed above with respect to claim 5, the modified system discloses that the output V_{CCR} of voltage reference 100 ("reference voltage generator") is connected to the cathode of the diode ("the diode's first terminal") in the McAdams-Uda combination. (*See supra* Section IX.B.1.) Therefore, the "first electrical path" (annotated in blue below) is part of a reference voltage generator (voltage reference 100). (Ex. 1002, ¶163.)

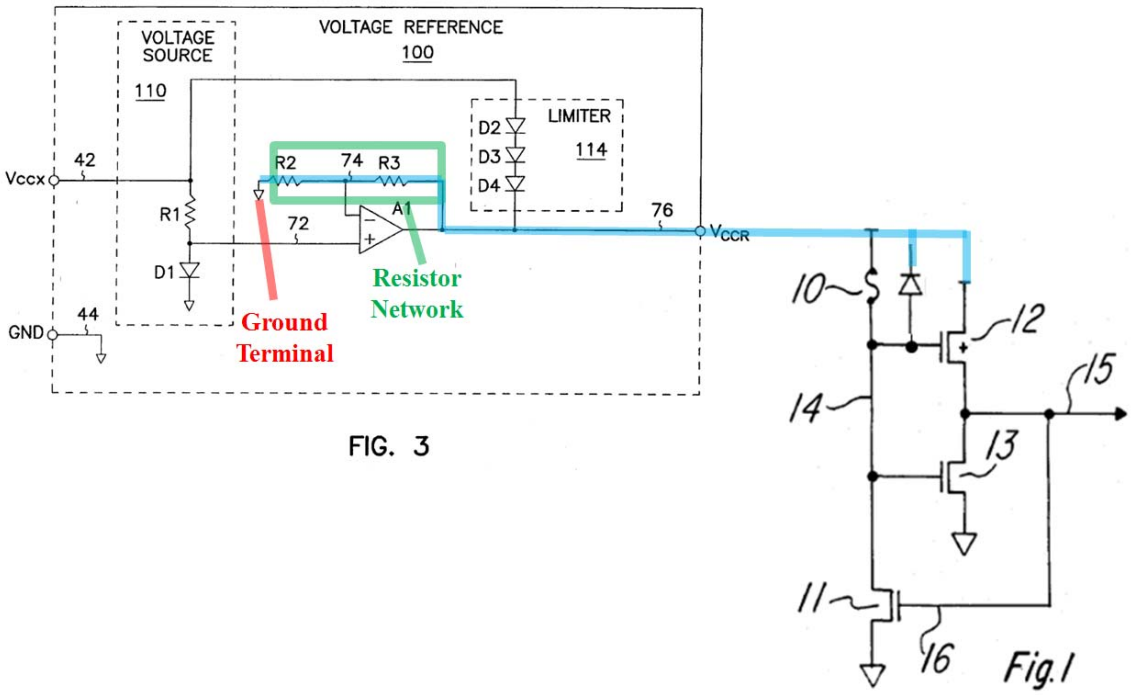


FIG. 3

(Ex. 1002, ¶163.)

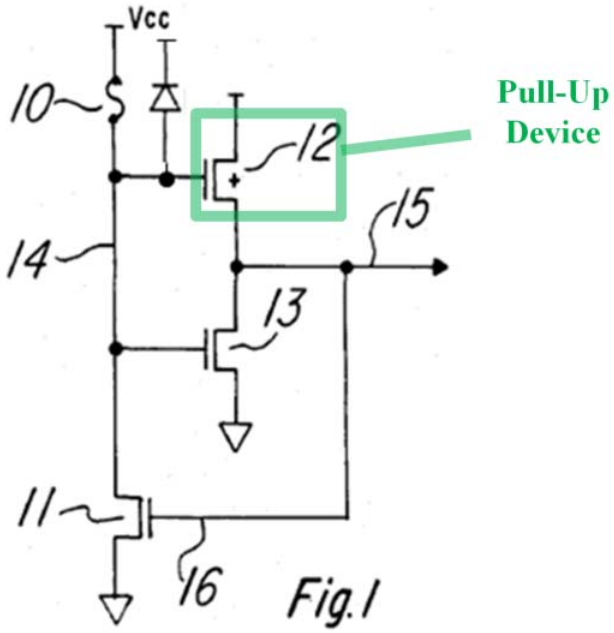
C. Ground 3: McAdams, Uda and Weste Render Obvious Claims 11-12

1. Claim 11

a) The programmable latch of claim 10 wherein one of the pull-up and pull-down devices is a MOS transistor formed in a first semiconductor region of a first conductivity type, and the diode comprises a second semiconductor region of a second conductivity type forming a junction with the first semiconductor region, the second region being connected to the terminal T1.

McAdams in view of Uda and Weste discloses or suggests this feature. (Ex. 1002, ¶¶165-179.) As shown in the demonstrative below, the "pull-up device" in the inverter of the McAdams-Uda combination is a P-channel (PMOS) transistor. (Ex. 1006, 1:67-2:7; *supra* Section IX.A.8(c).) Therefore, the McAdams-Uda

combination discloses that "one of the pull-up and pull-down devices is a MOS transistor." (Ex. 1002, ¶165.)

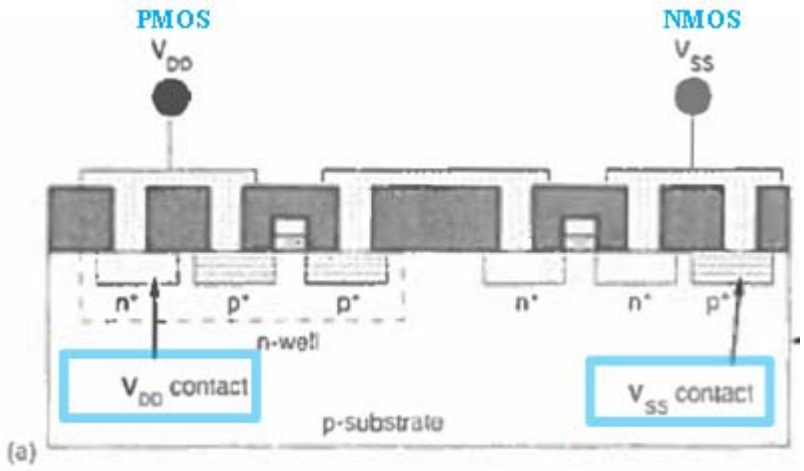


(Ex. 1002, ¶165 (illustrating a non-limiting implementation of the McAdams-Uda combination).)

While neither McAdams nor Uda discloses how the P-channel transistor 12 is formed, a POSITA would have known that P-channel transistors are formed such that the source and drain are P-type doped regions in an N-type substrate or N-well. (*Id.*, ¶166.) Weste, which is a treatise in the field of semiconductor integrated circuit devices, provides specific disclosure as to how such transistors are formed. (Ex. 1009, 1, 379, 625.) Weste describes the technology and construction of semiconductor circuit elements used in McAdams and Uda, such as

NMOS and PMOS transistors, diodes, latches, and fusible links. (*See, e.g.*, *id.*, 19-21, 41-51, 91-93, 117-130, 318-322, 395-400.)

When building circuits that include both PMOS and NMOS transistors, CMOS technology is used as it is "the leading VLSI systems technology." (Ex. 1009, 117; Ex. 1002, ¶169.) The most commonly used CMOS process is the n-well CMOS process in which the NMOS transistors are built in the native p-substrate but a separate n-well is created inside the p-substrate to mimic the function of an n-substrate for the PMOS transistors. (Ex. 1002, ¶169.) In such an n-well CMOS process, an inverter (which includes an NMOS transistor and a PMOS transistor sharing their drain terminals) would be constructed as shown below:



(*Id.*, 124 (FIG. 3.9, annotated); *see id.*, 122-23; Ex. 1002, ¶169.)

As seen from figure 3.9 of Weste, the NMOS transistor is formed by two n+ regions formed inside a p-substrate while the PMOS transistor is formed by two p+

regions formed inside an n-well. (Ex. 1002, ¶170.) The above construction for an inverter was so well-known and routine that another well-known treatise (Taur, Ex. 1015) shows the identical construction for a CMOS inverter where the PMOS transistor is formed inside an n-well next to an NMOS transistor in the p-substrate:

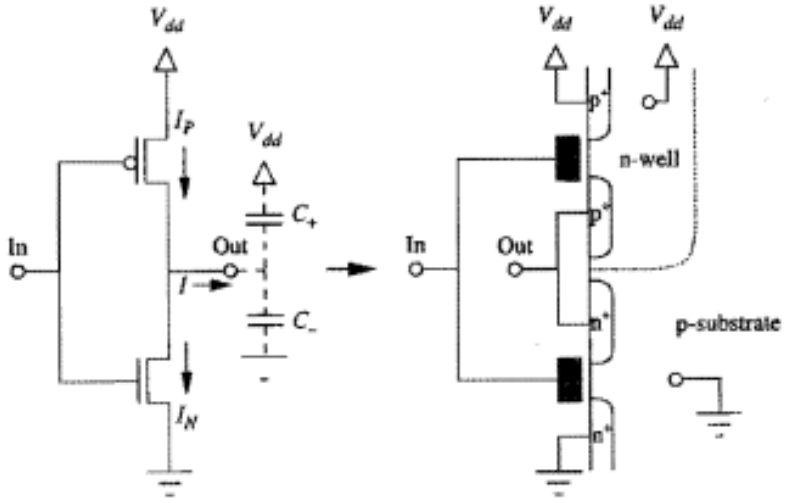
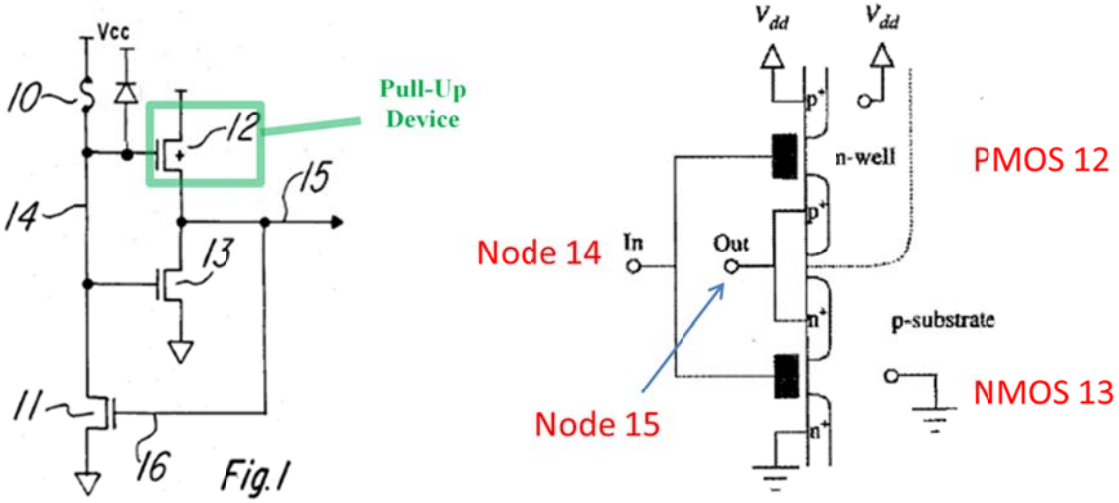


Figure 5.2. Circuit diagram and schematic cross section of a CMOS inverter.

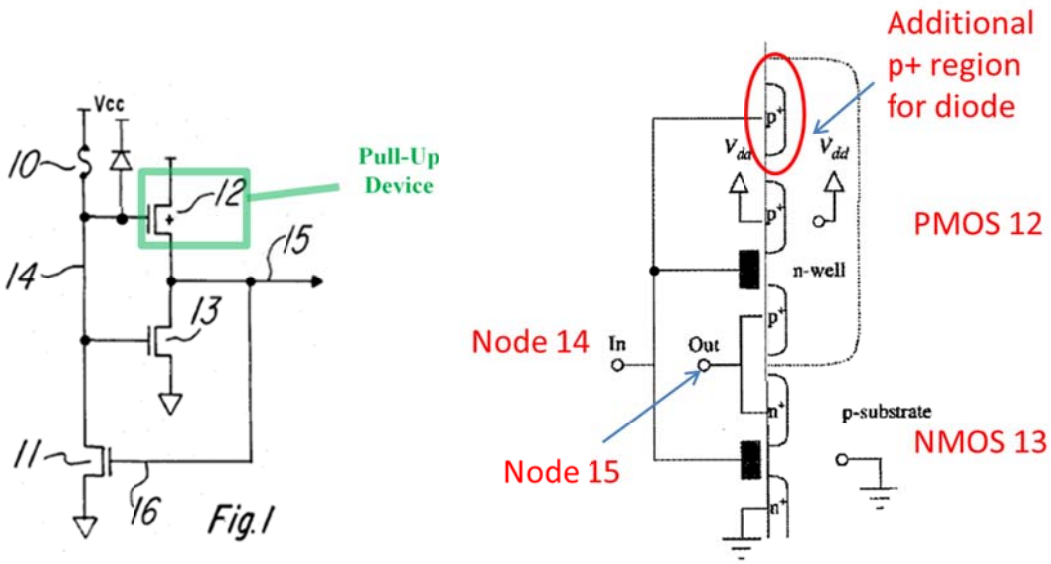
(Ex. 1015 at 257; Ex. 1002, ¶171.)

In view of the above, a POSITA would have understood that the inverter in the McAdams-Uda combination, i.e., the combination of PMOS transistor 12 and NMOS transistor 13 would be constructed as discussed in Weste and Taur:



(Ex. 1006, FIG. 1 (annotated); Ex. 1015 at 257 (FIG. 5.2, annotated); Ex. 1002, ¶¶172-173.)

But because the McAdams-Uda combination also includes a diode, an additional p+ region would have been included in the n-well region so that a p-n diode would be formed by the p+ region and the n-well:



(Ex. 1002, ¶¶174-176; *see also* Ex. 1009, 232 (FIG. 4.35) (explaining how a diode is formed between a p+ region and an n-well).)

The above construction discloses the features of claim 12. (Ex. 1002, ¶177.) For instance, the PMOS transistor 12 is formed in the n-well ("first semiconductor region of a first conductivity type") as shown in the demonstrative above. Further, the diode is formed by a p+ region ("the diode comprises a second semiconductor region of a second conductivity type") forming a junction with the n-well ("forming a junction with the first semiconductor region"). The p+ region of the diode would be connected to node 14 in the combination ("the second region being connected to the terminal T1") as shown in the demonstrative above. (*Id.*)

A POSITA would have been motivated to look to a treatise like Weste when implementing the McAdams-Uda combination and would have chosen the CMOS process for implementing the combination because the CMOS process "is the leading VLSI systems technology" (Ex. 1009, 117) and McAdams states that the inverter that includes transistors 12 and 13 is a "CMOS" inverter. (Ex. 1006, 2:3-7; Ex. 1002, ¶178.) A POSITA would have had reason to combine the teachings of the McAdams-Uda combination with Weste because while the McAdams-Uda combination discloses a circuit diagram (i.e., a schematic like figure 1 of McAdams), the combination does not disclose how to actually implement the components of the circuit in silicon. (Ex. 1002, ¶178.) Weste discloses well-

known CMOS fabrication techniques that have been used to form transistors such as those in the McAdams-Uda combination for several decades. (*Id.*) Therefore, a POSITA would have implemented the McAdams-Uda combination using the CMOS fabrication techniques disclosed in Weste. (*Id.*)

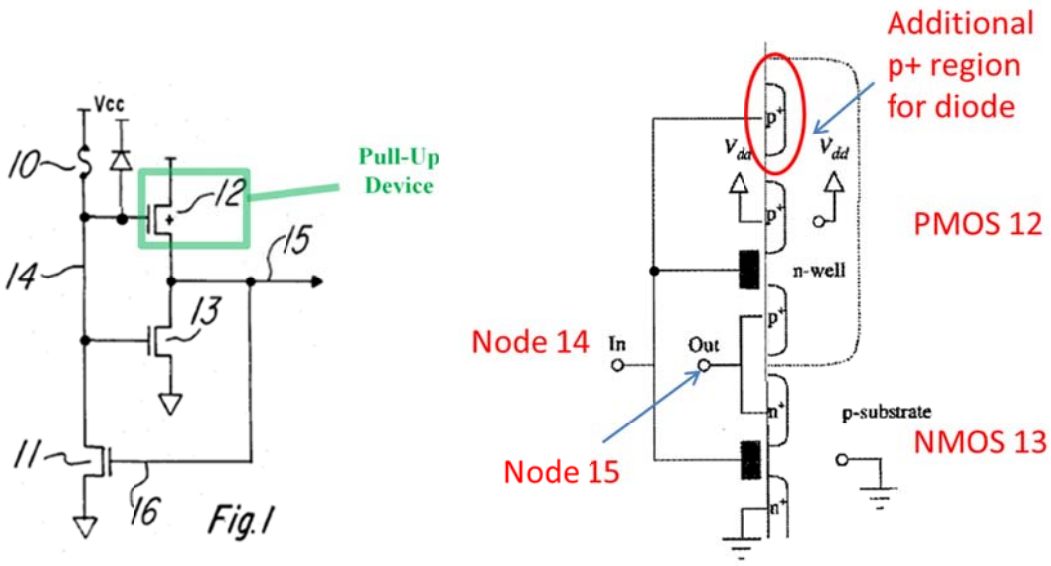
Indeed, the Federal Circuit has found obviousness under very similar circumstances. For example, the Federal Circuit has explicitly considered an earlier version of the Weste treatise and found it to be a resource that a POSITA would have consulted for guidance regarding implementing a circuit component disclosed in another reference. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1262 (Fed. Cir. 2007) (affirming a finding of obviousness based on a reference disclosing multiplexer circuits in view of an earlier edition of the Weste treatise disclosing a well-known option within a POSITA's technical grasp for implementing multiplexer circuits).

Having chosen the CMOS fabrication process, a POSITA would have naturally arrived at the layout set forth in the demonstrative above because that is most the logical way of implementing the relevant portions (inverter and diode) of the McAdams-Uda circuit. (Ex. 1002, ¶179.)

2. Claim 12

a) The programmable latch of claim 11 wherein the MOS transistor is a PMOS transistor, the first conductivity type is type N, the second conductivity type is type P, and the first semiconductor region is to receive a positive voltage.

McAdams in view of Uda and Weste discloses or suggests this feature. (Ex. 1002, ¶¶180-183.) As discussed above with respect to claim 11 (*supra* Section IX.C.1), a POSITA would have found it obvious to implement the inverter and diode in the McAdams-Uda circuit using the layout in the right side of demonstrative below:



(Ex. 1006, FIG. 1 (annotated); Ex. 1015 at 257 (FIG. 5.2, annotated); Ex. 1002, ¶180.)

As seen from the above layout, the MOS transistor formed in the n-well is a PMOS transistor (*supra* Section IX.C.1), the n-well ("first semiconductor region") is of conductivity type n ("the first conductivity type is type N"), the p+ region ("second semiconductor region") is of a conductivity type p ("the second conductivity type is type P"). (Ex. 1002, ¶181.) Moreover, as is evident from the demonstrative above, the n-well is tied to Vdd, which is a positive voltage (+5V) in

the McAdams-Uda circuit ("the first semiconductor region is to receive a positive voltage"). (*Id.*) A POSITA would have understood that the n-well is tied to the highest voltage in the circuit to ensure proper operation of the circuit. (Ex. 1009, 122-23; Ex. 1002, ¶181-183.)

D. Ground 4: McAdams, Uda, and Tomishima Render Obvious Claim 9

As discussed above in Ground 1, claim 9 is obvious in view of McAdams and Uda. (*See supra* Section IX.A.7.). However, to the extent Patent Owner contends or the Board finds that McAdams and Uda do not disclose or suggest that the Vcc terminal of the combined McAdams-Uda fuse circuit is received "from an external pin of the integrated circuit" as recited in claim element 9[b], such a feature would have been obvious in further view of Tomishima as demonstrated below. (Ex. 1002, ¶¶184-195.)

1. Claim 9

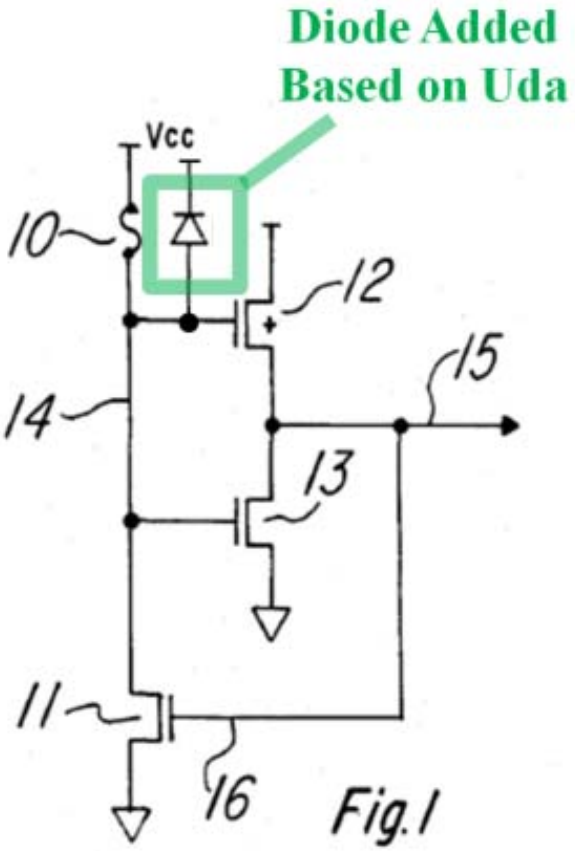
a) The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,

As discussed above in Section IX.A.7(a), McAdams in combination with Uda discloses or suggests this feature because the combined McAdams-Uda circuit is used in an integrated circuit device such as a memory device. (*See supra* Section IX.A.7(a); Ex. 1002, ¶185.)

b) wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is

to receive a non-ground power supply voltage from an external pin of the integrated circuit.

As discussed above in Section IX.A.7(b), McAdams in combination with Uda discloses or suggests this feature. (*See supra* Section IX.A.7(b).) However, to the extent Patent Owner contends or the Board finds that McAdams and Uda do not disclose or suggest that the Vcc terminal of the combined McAdams-Uda fuse circuit shown below ("programmable latch") is received "from an external pin of the integrated circuit" as recited in claim element 9[b], it would have been obvious in view of Tomishima (Ex. 1013) to configure the combined McAdams-Uda fuse circuit to receive the power supply Vcc from an external pin of the integrated circuit. (Ex. 1002, ¶¶186-195.)



(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶95.)

As discussed above in Section IX.D.1(a), the McAdams-Uda circuit is implemented in an integrated circuit. A POSITA would have understood that it was common practice for the integrated circuit device to receive power on an external pin of the integrated circuit and for the circuits inside the integrated circuit to use the received power either directly from the pin or through an intermediate circuit (e.g., an internal power supply generator). (*See supra* Sections IX.A.7(b), IX.B.1; Ex. 1002, ¶188.) Indeed, providing power to integrated circuits using external pins was so routine and well-known to a POSITA, that patents such as

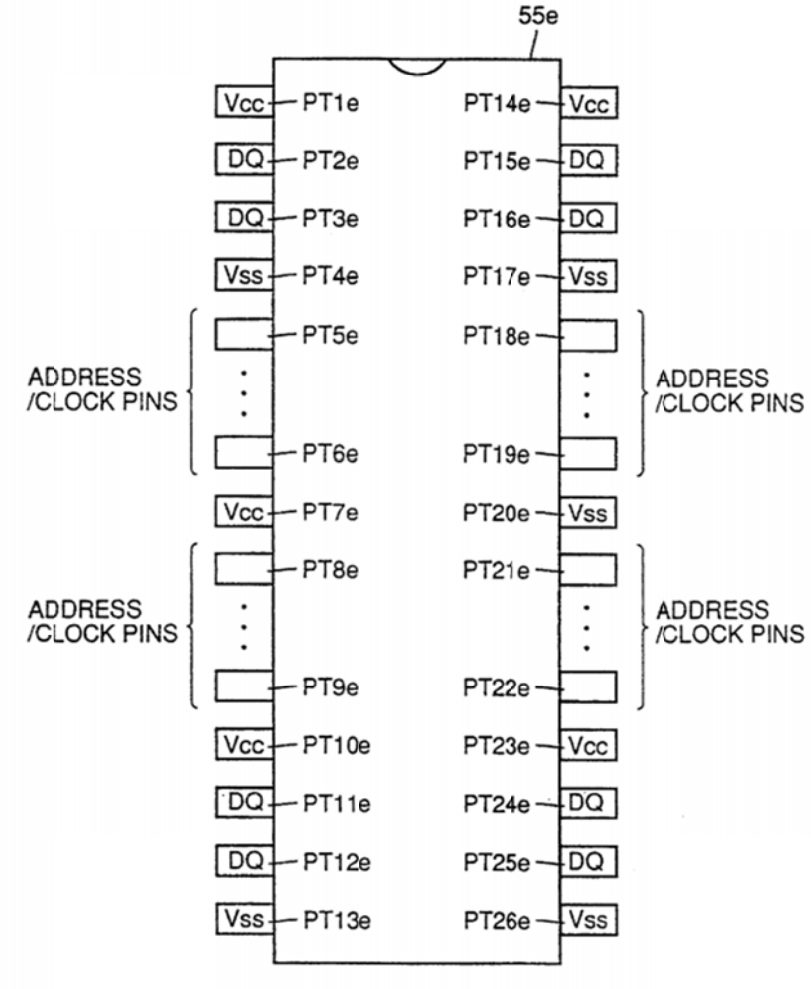
McAdams and Uda did not provide specifics as to the origin of the power supply inside the chip (e.g., Vcc in figure 1 of McAdams). (Ex. 1002, ¶188.) As demonstrated below, Tomishima discloses specifics as to an integrated circuit device receiving the power supply voltage on an external pin, thereby demonstrating that it was within the knowledge of a POSITA at the time of the alleged invention of the '492 patent. (*Id*.) As also discussed below, a POSITA would have been motivated to provide the Vcc voltage (as shown in the McAdams-Uda demonstrative above) from a power supply pin such as that disclosed in Tomishima. (*Id.*, ¶¶188-195.)

Like McAdams and Uda, Tomishima relates to memory circuits. (*See, e.g.*, Ex. 1013, 1:12-19; Ex. 1006, Abstract ("A fuse circuit as used in self-repairing memory devices or the like…."); Ex. 1007, 1:10-18 ("the invention relates to a semiconductor integrated circuit device having a redundancy circuit arrangement such as a static RAM (random access memory)…."); Ex. 1002, ¶189.) Tomishima discloses that in an integrated circuit memory (e.g., a DRAM), a center region is conventionally designed to have "pads for receiving external power supply voltage and ground voltage and for input/output of signals." (Ex. 1013, 1:31-35.) Tomishima discloses that such a configuration, however, does not allow all structures in the memory device to operate stably at high speed. (*Id.*, 2:40-41.) To overcome these deficiencies, Tomishima discloses a specific arrangement of power

supply pads that receive power from a source external to the integrated circuit. (*Id.*, 4:6-14; Ex. 1002, ¶190.)

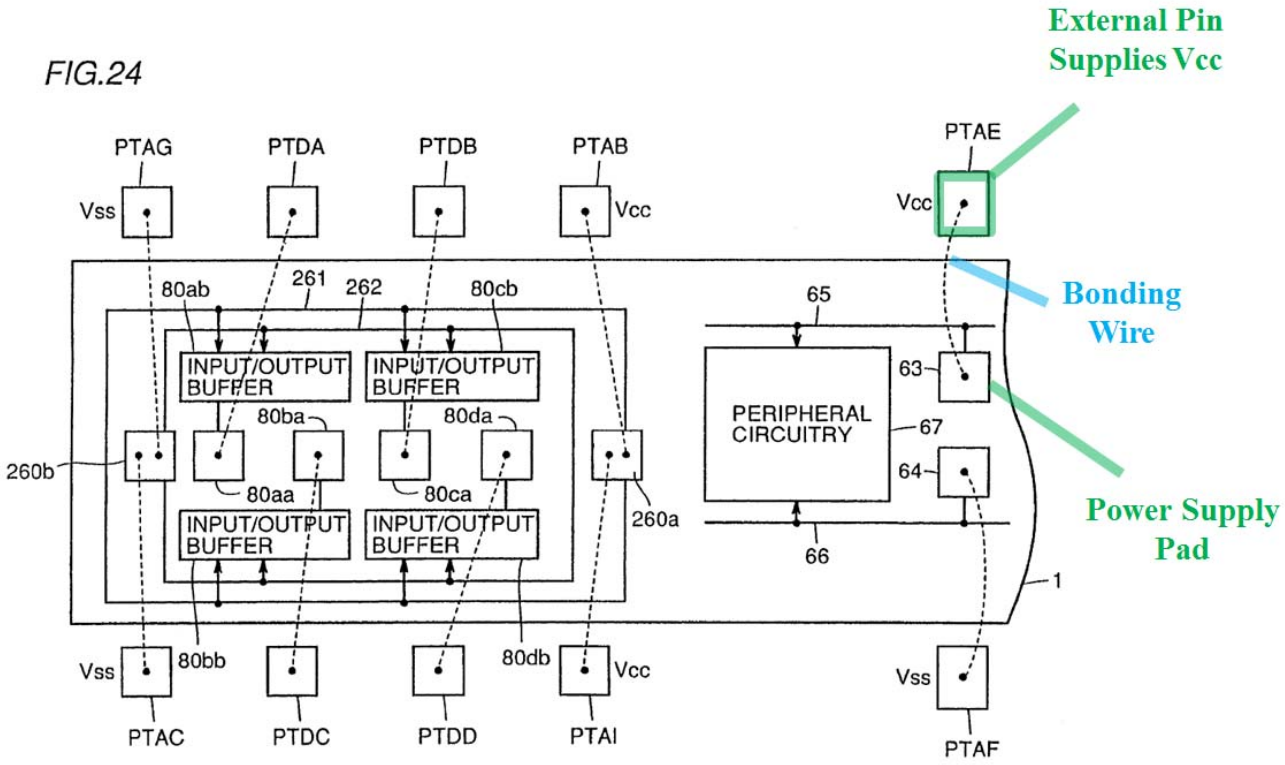
An example configuration of external power supply pins is shown below in figure 23 of Tomishima. (Ex. 1002, ¶191.)

FIG.23



(Ex. 1013, FIG. 23.) Tomishima explains that "power supply pin terminals and ground pin terminals are arranged on each respective side of package 55e." (*Id.*, 24:32-40.) "The voltages Vcc and Vss supplied to pin terminals PT7e and PT20e

are used by peripheral circuitry operating on the signals received through address/clock pin terminals …." (*Id.,* 24:56-59.) Figure 24 of Tomishima, annotated below, shows an inner pad layout of the semiconductor memory device in the package of figure 23. (*Id.,* 6:21-22, 24:60-61; Ex. 1002, ¶192.)



(*Id.,* FIG. 24 (annotated); Ex. 1002, ¶192.)

As shown in figure 24 above, bonding wires (broken lines) are used to connect the power supply pins to power supply pads (e.g. 260a) on the integrated circuit memory device. (Ex. 1013, 24:65-25:1; Ex. 1002, ¶193.)

Given the above-noted disclosure associated with how Vcc is supplied to a memory device in Tomishima, a POSITA would have been motivated to combine the teachings of McAdams, Uda, and Tomishima such that the power supply (Vcc)

in the McAdams-Uda combination is provided by an external pin of the integrated circuit. (Ex. 1002, ¶194.) Neither McAdams nor Uda provides specific disclosure as to how the power supply (e.g., Vcc as shown in figure 1 of McAdams) is configured for the integrated circuits disclosed therein or from where the power supply is received. (*Id.*) Therefore, a POSITA would have looked to teachings associated with external power supply connections, such as those disclosed by Tomishima, so that Vcc in the McAdams-Uda combination could be provided with the necessary voltage. (*Id.*; Ex. 1006, 2:8-9 ("During power-up of the supply voltage V_{CC}, as V_{CC} goes from zero to +5 v ….").) Accordingly, a POSITA would have combined the teachings of the McAdams-Uda combination and Tomishima because Tomishima explains how a power supply can be received by an external pin of an integrated circuit (e.g., the memory device including the McAdams-Uda) and such a power supply can be used to power circuits inside an integrated circuit. (Ex. 1002, ¶195; Ex 1013 at 24:56-59.) *See Unwired Planet*, 841 F.3d at 1003.

Therefore, for these reasons in addition to those presented above in Section IX.A.7(b), the McAdams-Uda-Tomishima system discloses or suggests the features of claim 9, including "the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit." (Ex. 1002, ¶¶186-195.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-13 of the '492 patent based on the ground specified in this petition.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 contains, as measured by the word-processing system used to prepare this paper, 13,735 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 5, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

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