Paper No. __
Filed: March 5, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,163,492

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,163,492

TABLE OF CONTENTS

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 6,163,492
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	Prosecution History of U.S. Patent No. 6,163,492
Ex. 1005	RESERVED
Ex. 1006	RESERVED
Ex. 1007	RESERVED
Ex. 1008	U.S. Patent No. 5,552,739 ("Keeth")
Ex. 1009	Weste *et al.*, Principles of CMOS VLSI Design: A Systems Perspective, 2d. ed. 1993 ("Weste")
Ex. 1010	U.S. Patent No. 5,619,469 ("Joo")
Ex. 1011	RESERVED
Ex. 1012	U.S. Patent No. 5,592,121 ("Jung")
Ex. 1013	U.S. Patent No. 5,604,710 ("Tomishima")
Ex. 1014	Weste *et al.*, Principles of CMOS VLSI Design: A Systems Perspective, 2d. ed. 1993, including cover, series title page, title page, copyright page, about the author page, preface, table of contents, last numbered page, back cover, and spine
Ex. 1015	Taur *et al.*, Fundamentals of Modern VLSI Devices, 2009 ("Taur")
Ex. 1016	Declaration of Dr. Ingrid Hsieh-Yee

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1, 2, and 4-13 of U.S. Patent No. 6,163,492 ("the '492 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '492 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al*., No. 1:18-cv-00307-RGA (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 5,934,974 ("the '974 patent"), 6,099,386 ("the '386 patent"), 6,469,559 ("the '559 patent"), and 6,597,201 ("the '201 patent") in this action. Petitioner is concurrently filing two other IPR petition challenging one or more claims of the '492 patent, as well as additional IPR petitions challenging certain claims of the '974, '386, '559, and '201 patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul

M. Anderson (Reg. No. 39,896), and (3) Chetan R. Bansal (Limited Recognition No. L0667). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the '492 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1, 2, and 4-13 ("challenged claims") of the '492 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following grounds:

Ground 1: Claims 1, 2, 4, and 8-13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Joo in view of Weste.

Ground 2: Claims 1, 2, 4-8, and 10-13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Joo in view of Weste and Keeth.

Ground 3: Claim 9 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Joo in view of Weste and Tomishima.

The '492 patent issued from U.S. Application No. 09/178,445 ("the '445 application") filed October 23, 1998. (Ex. 1001, Cover). The '445 application does not claim priority to any earlier-filed applications.

Joo issued on April 8, 1997. Keeth issued on May 21, 1996. Tomishima issued on February 18, 1997. Weste published at least by 1994. Dr. Hsieh-Yee, an expert on library cataloging and classification, considered numerous facts relating to Weste (e.g., bibliographic and MARC records, a date stamp, copyright registration information, and pre-filing date citations to Weste) and explains on the basis of such evidence that Weste was accessible to the public by September 16, 1993. (Ex. 1016, ¶27; *see also id.,* ¶¶12-26.)[1] Additionally, Dr. Hsieh-Yee

[1] Dr. Hsieh-Yee cites to Exhibit 1014 in her analysis regarding the public availability of the Weste textbook (Exhibit 1009). (*See, e.g.*, Ex. 1016 at ¶¶12-13.) Exhibit 1014 is a copy of Weste's relevant portions (e.g., cover, title page, copyright page, back cover, etc.) that Dr. Hsieh-Yee personally made and which match the corresponding portions of Exhibit 1009 being cited in this petition. (*Compare, e.g.*, Ex. 1009, 1-22, 745-46 *with* Ex. 1014 at 1-22, 23-24.)

explains that several pre-critical-date publications cite to Weste, including one as early as December 1994. (*Id.*, ¶26.)

Thus, Joo, Keeth, Weste, and Tomishima qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b) with respect to the '492 patent. None of them were considered by the Patent Office during prosecution of the '492 patent. (*See generally* Ex. 1001, References Cited.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person having ordinary skill in the art at the time of the alleged invention of the '492 patent ("POSITA"), which for purposes of this proceeding is the mid-to-late 1990s (including October 23, 1998, the filing date of the U.S. Application maturing into the '492 patent), would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶¶20.)[2] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '492 PATENT AND PRIOR ART

A. The '492 Patent

The '492 patent is entitled "Programmable Latches that Include Non-volatile Programmable Elements." (Ex. 1001, Cover.) Consistent with the title, the '492

[2] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '492 patent. (Ex. 1002, ¶¶5-15; Ex. 1003.)

patent relates to "programmable latches that include non-volatile programmable elements" where "examples of non-volatile programmable elements are fuses." (*Id.*, 1:15-17; Ex. 1002, ¶¶40-48; *see also* Ex.1002, ¶¶23-39 (citing Ex. 1015).)

The '492 patent acknowledges that the "[p]rior art latch of FIG. 1 has an advantage that a latch initialization does not require a latch initialization signal from outside the latch" and that "[t]he state of the latch is completely determined by the state of fuse F1 and the voltages on the VDD and ground terminals." (Ex. 1001, 2:22-26, FIG. 1; Ex. 1002, ¶¶45.)

While the prior art programmable latch shown in figure 1 includes features to avoid an incorrect output on power up and does not require any initialization signal, the '492 patent proposes an alternative programmable latch as shown in figure 2A below. (Ex. 1001, 3:10-11.)

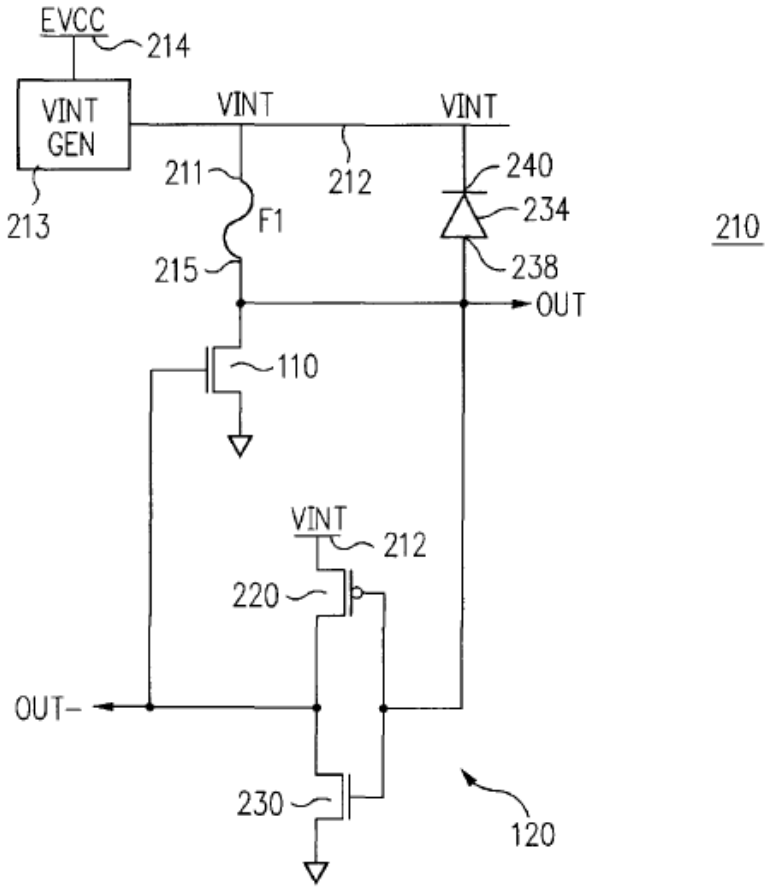


FIG. 2A

(*Id.*, FIG. 2A.)

The programmable latch shown in figure 2A above includes a fuse 211, an inverter 120 that includes transistors 220 and 230, and a transistor 110. (*Id.*, 3:10-33, FIG. 2A.) The programmable latch of figure 2A also includes a diode 234 that holds the OUT node at a voltage not higher than a threshold voltage of the diode 234 when the VINT terminal is ground. (*Id.*, 3:38-41.) According to the '492 patent, by maintaining the voltage on OUT low using the diode 234, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on and

"connects the terminal OUT to ground," resulting in a correct output. (*Id.*, 3:41-49.) This happens because terminal OUT is held "not higher than one threshold voltage of diode 234," and at such a voltage, transistor 230 does not turn on because its threshold voltage (e.g., 1.2V) is greater than the threshold voltage of diode 234. (*Id.*) Per the '492 patent, the latch can operate correctly even if the diode is omitted. (*Id.*, 5:51-6:7; Ex. 1002, ¶¶46-48.)

The above features were well known as discussed below in Section IX. (Ex. 1002, ¶¶63-169; *see also id.*, ¶¶51-62 (describing the prior art).)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.,* 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). For purposes of this proceeding, Petitioner believes that no express

constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[3] (Ex. 1002, ¶50.)

IX. DETAILED EXPLANATION OF GROUNDS

As detailed below, the challenged claims are unpatentable based on Grounds 1-3. (Ex. 1002, ¶¶63-169.)

A. Ground 1: Joo and Weste Render Obvious Claims 1, 2, 4, and 8-13

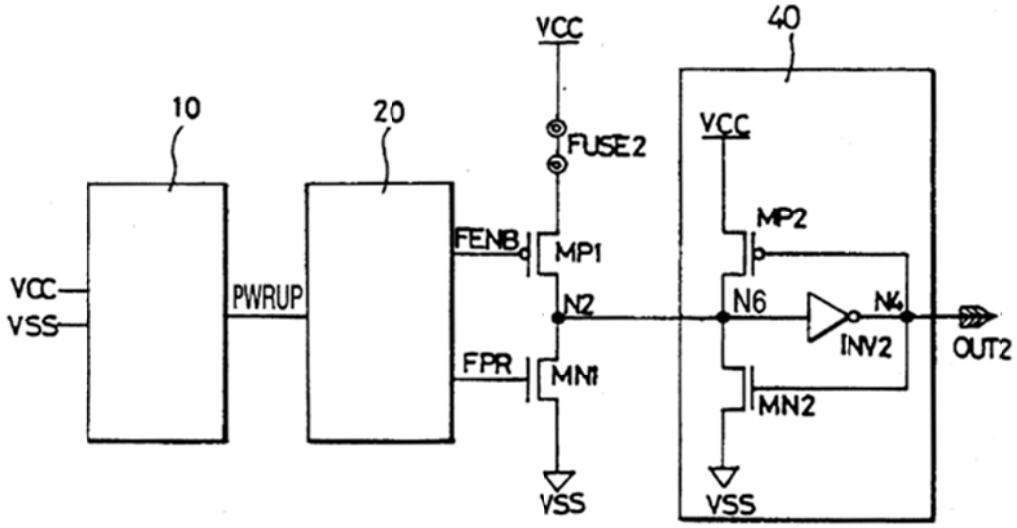
1. Claim 1

a) A programmable latch comprising:

To the extent the preamble is limiting, Joo discloses this feature. (Ex. 1002, ¶¶65-69.) For example, Joo discloses a fuse circuit depicted in figure 2.

[3] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '492 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

FIG.2

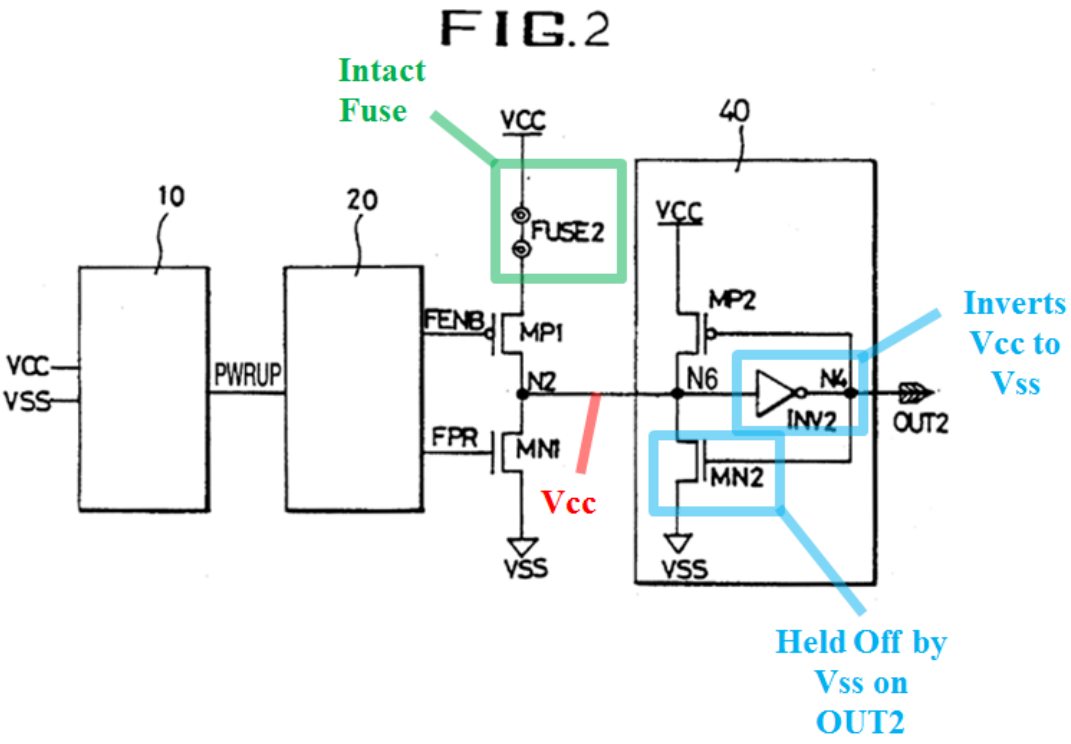


(Ex. 1010, FIG. 2.)

The fuse circuit of figure 2 includes a fuse ROM with fuse FUSE2, PMOS transistor MP1, NMOS transistor MN1, gate control section 20, and power supply detecting circuit 10. (*Id.,* 2:49-62.) Latching section 40 includes feedback transistors MP2 and MN2, and an inverter INV2. (*Id.,* 2:63-3:4.) The fuse ROM and latching section 40 of figure 2 produce an output OUT2, which is fed back to the gate of transistors MP2 and MN2. (*Id.,* 3:4-11.) Thus, the fuse ROM (*i.e.*, programmable ROM) outputs a value to the latching section 40 at node N2, which is latched and output from the programmable ROM cell. (*Id.,* 2:63-3:12; Ex. 1002, ¶66.)

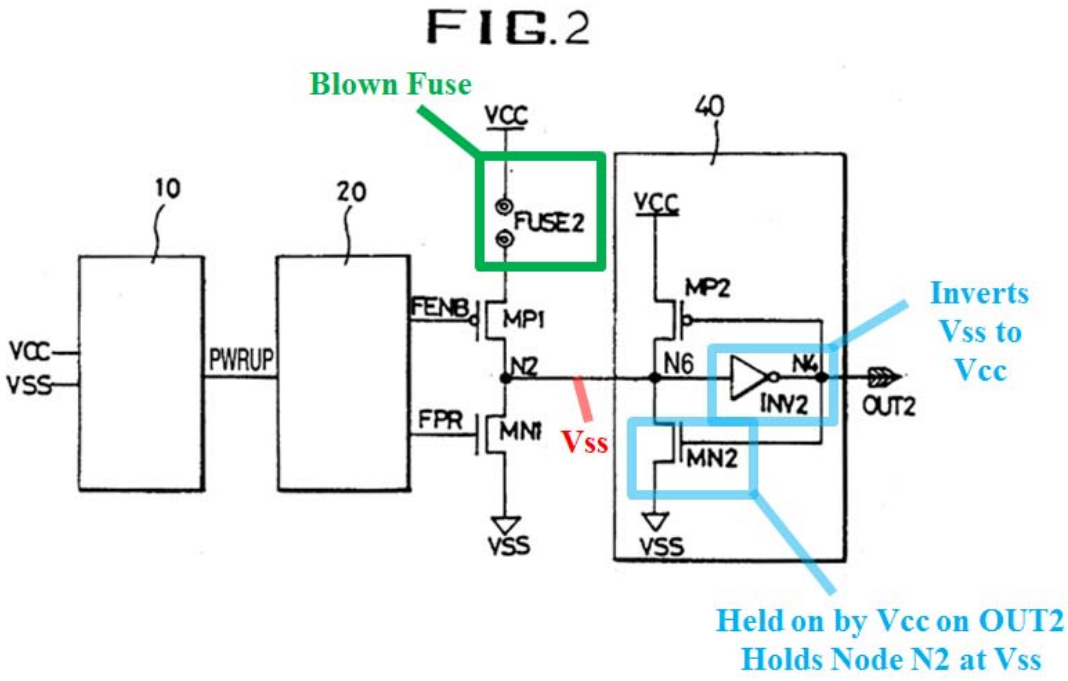
In the exemplary operational scenario depicted in annotated figure 2 below, Joo discloses that if fuse FUSE2 is intact when power is applied to the circuit, node

N2 follows the power supply Vcc. (Ex. 1010, 3:36-40.) Consequently, output OUT2 is maintained at a low level (Vss) by latching section 40, which turns off transistor MN2 and turns on transistor MP2. (*Id.*, 3:56-61; Ex. 1002, ¶67.)



(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶67.)

In an alternate operational scenario where the fuse is blown, as depicted in the demonstrative below, node N2 remains at ground voltage Vss. (Ex. 1010, 3:36-40.) Consequently, output OUT2 is maintained at a high level (Vcc) by latch section 40. (*Id.*, 4:1-4.) Because inverter INV2 outputs a high value, NMOS transistor MN2 is turned on, thereby maintaining node N2 at Vss. (*Id.*; Ex. 1002, ¶68.)

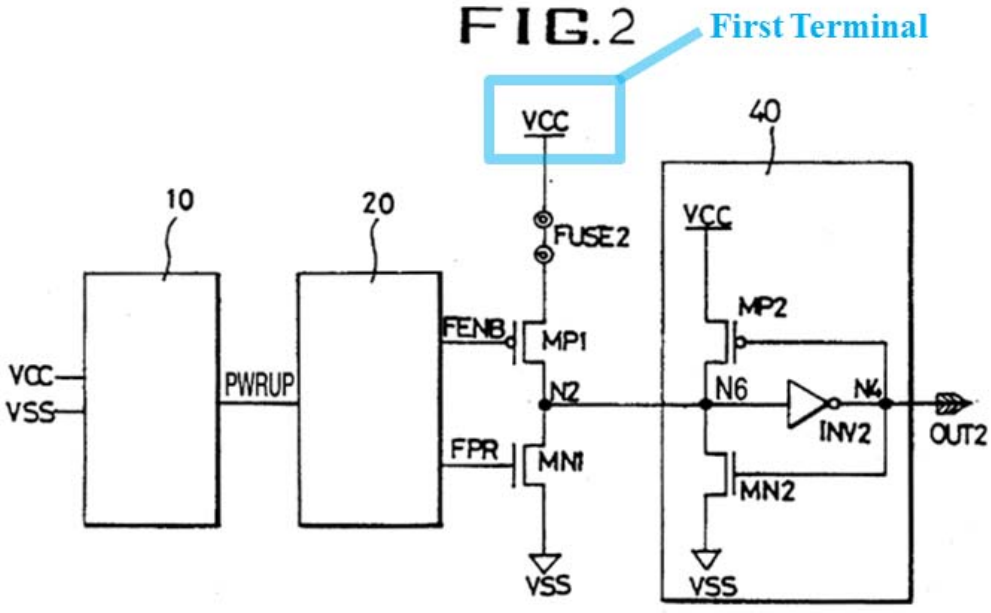


(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶68.)

Therefore, based on whether fuse FUSE2 is open (*i.e.*, blown) or remains intact, output OUT2 of the fuse circuit shown in FIG. 2 is held at either Vcc or Vss. (Ex. 1010, 3:36-40.) The feedback of the output of the inverter INV2 to transistors MN2 and MP2 holds that output at Vcc or Vss. Therefore, the output is latched at either Vcc or Vss based on whether or not the fuse is blown. A POSITA would have recognized that the circuit of FIG. 2 constitutes a "programmable latch" where the programming corresponds to the state of the fuse, *i.e.*, open or intact, which determines the latched value at the output OUT2. (Ex. 1002, ¶69.)

b) a first terminal for receiving a first voltage;

Joo discloses this feature. (Ex. 1002, ¶¶70-72.) As shown in annotated figure 2 below, the "programmable latch" of Joo includes a "terminal" V_{CC}, where V_{CC} is a "supply voltage" that is applied when power is applied to the circuit of figure 2. (Ex. 1010, 2:51-53 ("fuse FUSE2, a PMOS transistor MP1, and an NMOS transistor MN1 are connected in series between a power source Vcc and a ground voltage Vss"), 3:15-17 ("[w]hen power is supplied to the circuit, the power source voltage is gradually stepped up until the level Vcc is reached"), 3:36-40 ("in accordance with the state of the fuse FUSE2 . . . node N2 is pulled up to the power supply voltage Vcc (if the fuse FUSE2 is connected)").) Therefore, Vcc constitutes "a first voltage." (Ex. 1002, ¶70.) Thus, the terminal highlighted in blue below constitutes a "first terminal for receiving a first voltage." (*Id.*)

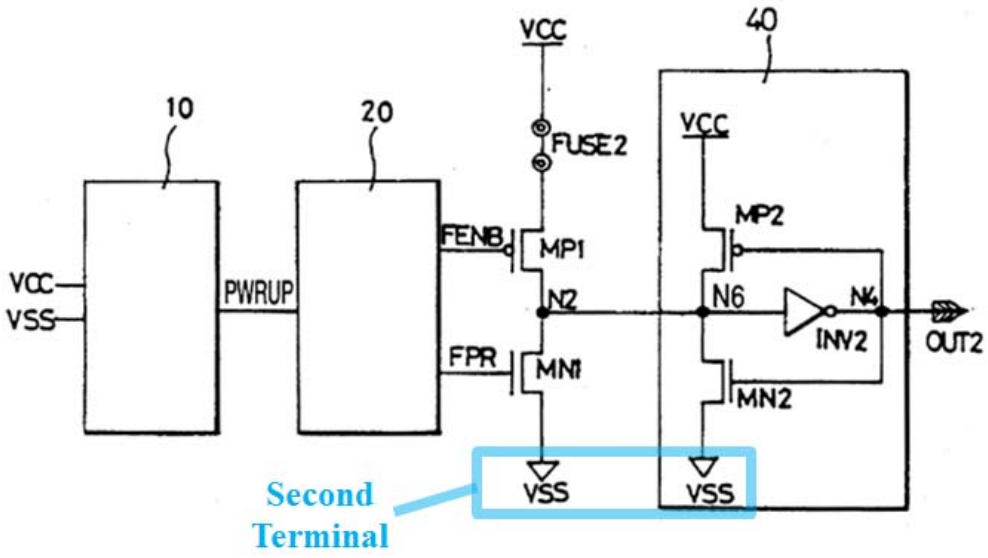


(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶70.)

c) a second terminal for receiving a second voltage;

Joo discloses this feature. (Ex. 1002, ¶71.) For example, the programmable latch circuit in FIG. 2 of Joo includes a second terminal for receiving a ground voltage Vss ("second voltage"). (Ex. 1010, 2:51-53 ("fuse FUSE2, a PMOS transistor MP1, and an NMOS transistor MN1 are connected in series between a power source Vcc and a ground voltage Vss"), 3:36-38 ("in accordance with the state of the fuse FUSE2 . . . the level of the first node N2 is maintained at the ground voltage Vss (if the fuse FUSE2 is open)"), 2:64-66 ("Two MOS transistors MP2 and MN2 of different conductivity types are connected in series between the power source voltage Vcc and the ground voltage Vss"), 4:1-4 ("[t]he high output turns on the NMOS transistor MN2 of the latching section 40, so that the input to the inverting device INV2 is maintained at a low level").) Therefore, Joo discloses "a second terminal for receiving a second voltage." (Ex. 1002, ¶71.)

FIG.2



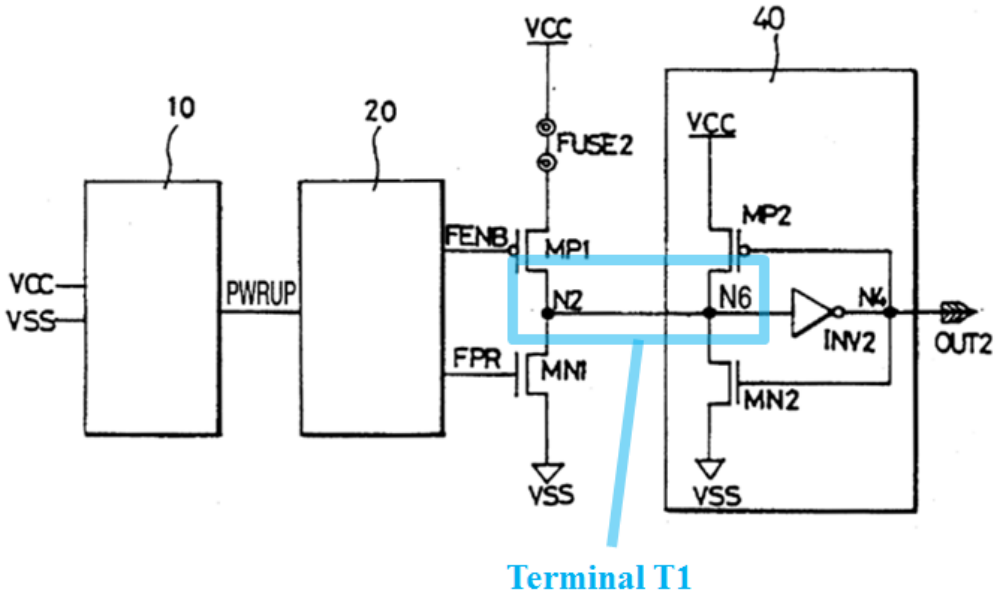
(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶71.)

d) a terminal T1 for providing a signal indicating a state of the programmable latch;

Joo discloses this feature. (Ex. 1002, ¶72.) For example, as shown in annotated figure 2 below, the node N2 indicates the state of the fuse, which corresponds to the state of the programmable latch ("a terminal T1 for providing a signal indicating a state of the programmable latch"). (*Id.*) As discussed above with respect to claim element 1[a], when power is applied to the latch, if the fuse is intact, node N2 is at Vcc (high), but if the fuse is blown, node N2 is at Vss (low). (*See* citations and discussion regarding the operation of the circuit in figure 2 of Joo at Section IX.A.1(a) *supra*.) Furthermore, "node N2 is connected to a connection point N6." (Ex. 1010, 2:66-67.) The voltage level at node N6 is the

same as the voltage level at node N2, and therefore, node N2 and node N6 both indicate the state of the programmable latch. (Ex. 1002, ¶72.) Therefore, the voltage at node N2/N6 indicates a "state of the programmable latch" because it indicates whether the fuse is blown or not. (*Id.*)

FIG.2

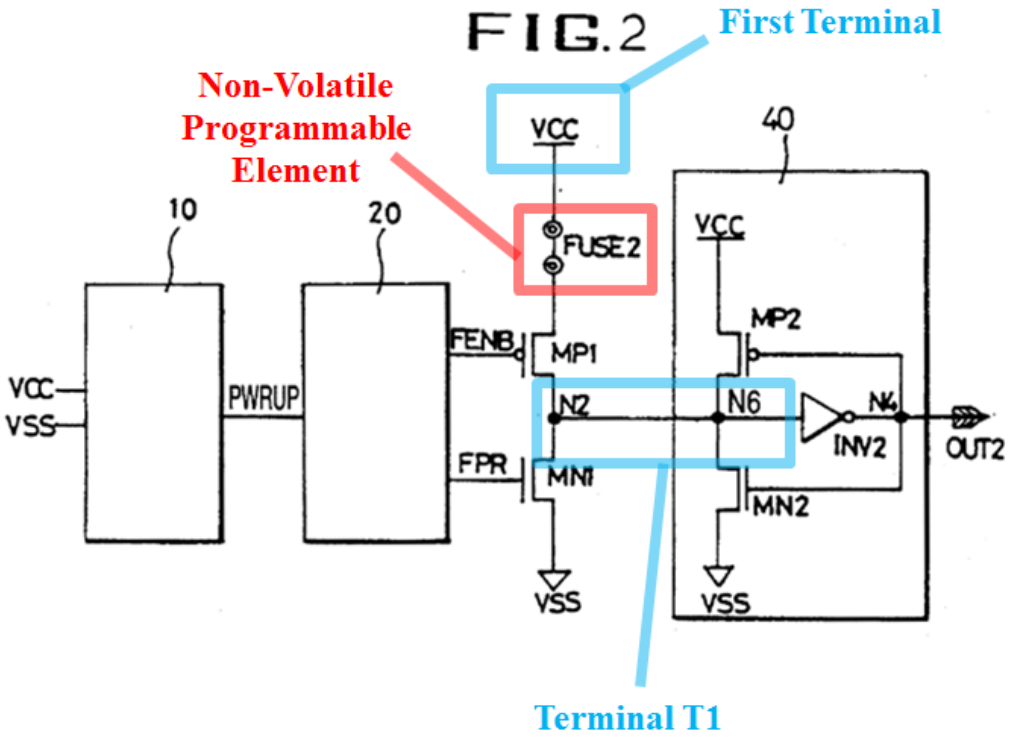


(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶72.)

e) a programmable electrical path including a non-volatile programmable element such that when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal, and when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal;

Joo discloses this feature. (Ex. 1002, ¶¶73-76.) For example, Joo discloses "a programming section using a fuse according to the present invention." (Ex.

1010, 2:45-46.) The programming section may be "programmed," for example, by cutting the fuse using a laser. (*Id.*, 1:14-16, 1:24-27.) Thus, the fuse FUSE2 shown in annotated figure 2 below is a "programmable electrical path including a non-volatile programmable element." (Ex. 1002, ¶73.) Such an understanding is consistent with the disclosure of the '492 patent, which shows a fuse in the embodiment of figure 2A and states that "[e]xamples of non-volatile programmable elements are fuses" (Ex. 1001, 1:16-17), where such fuses can be "electrically programmable fuses." (*Id.*, 2:41-45.) Moreover, claim 10, which depends from claim 1 recites "wherein the programmable element is a fuse," thereby demonstrating that a fuse is a "non-volatile programmable element" in the context of claim 1 and the '492 patent. (*Id.*, 9:25-27; Ex. 1002, ¶122.)



(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶73.)

Further, as shown in annotated figure 2 above, the fuse FUSE2 ("non-volatile programmable element") is coupled between Vcc ("first terminal") and node N2 ("terminal T1"), thereby forming an "electrical path" between Vcc ("first terminal") and node N2 ("terminal T1"). When the fuse 10 is intact and therefore "conductive," the fuse connects Vcc ("first terminal") to node N2 ("terminal T1"). (Ex. 1010, 3:36-40; *see* citations and discussion regarding the operation of the circuit in figure 2 of Joo at Section IX.A.1(a) *supra*.) Even though PMOS transistor MP1 is between fuse FUSE2 and node N2, FUSE2 "connects" terminal N2 to Vcc. Such an understanding is consistent with the disclosure of the '492

patent, which explains that "[i]n some embodiments, other circuit elements (such as resistors, perhaps variable-impedance resistors) are included between the terminal OUT and the ground or VINT terminals." (Ex. 1001, 7:63-66.) Therefore, Joo discloses "when the programmable element is conductive, the programmable path connects the terminal T1 to the first terminal." (Ex. 1002, ¶74.)

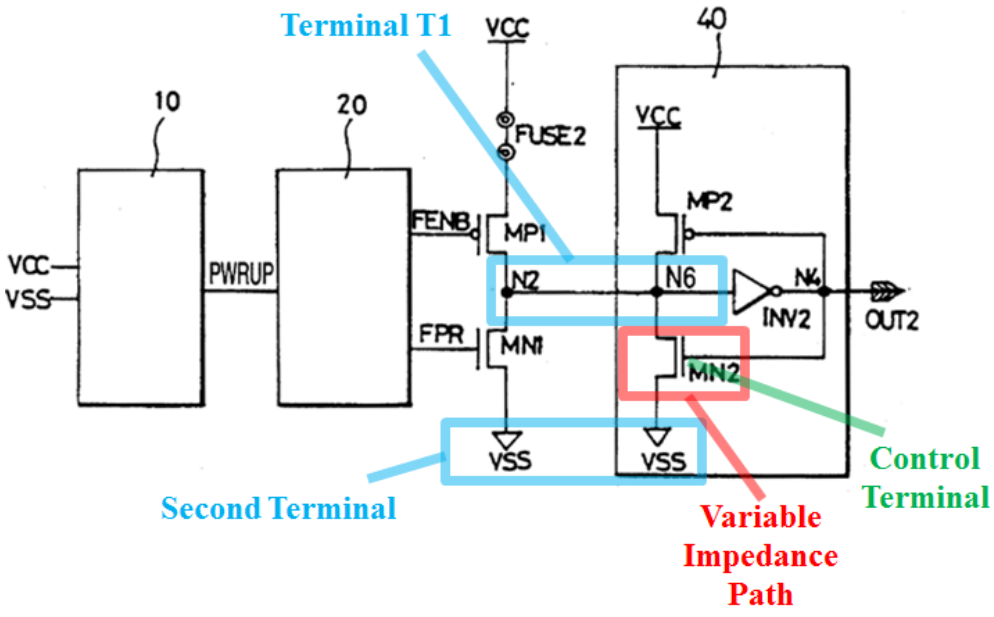
When the fuse 10 is open and therefore "non-conductive," the fuse does not connect Vcc ("first terminal") to node N2 ("terminal T1"). (Ex. 1010, 3:36-40 (explaining that even though Vcc is powered up, node N2 remains at Vss when the fuse is open); *see also* citations and discussion regarding the operation of the circuit of figure 2 of Joo in Section IX.A.1(a) *supra*.) Therefore, Joo discloses "when the programmable element is non-conductive, the programmable path does not connect the terminal T1 to the first terminal." (Ex. 1002, ¶75.)

Because the state of the fuse may be modified or programmed to determine whether the electrical path connects Vcc ("first terminal") to node N2 ("terminal T1"), Joo discloses a "programmable electrical path" having the features recited in claim element 1[e]. (*Id.*, ¶76.)

f) a variable-impedance electrical path between the terminal T1 and the second terminal, wherein the impedance of the electrical path is controlled by a signal on the terminal T1; and

Joo discloses this feature. (Ex. 1002, ¶¶77-81.) For example, the NMOS transistor MN2 highlighted below in annotated figure 2 is a "variable-impedance electrical path." (*Id.*, ¶77.) Such an understanding is consistent with the disclosure of the '492 patent, which shows an NMOS transistor as the "variable-impedance electrical path" in the embodiment of figure 2A. (Ex. 1001, FIG. 2A.) Moreover, claim 10, which depends from claim 1 recites "the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal," thereby demonstrating that a transistor is a "variable-impedance electrical path" in the context of claim 1 and the '492 patent. (*Id.*, 9:28-30; Ex. 1002, ¶¶77-78.)

FIG.2



(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶78.)

As shown in annotated figure 1 above, the NMOS transistor MN2 ("variable-impedance electrical path") is coupled between node N2/N6 ("terminal T1") and Vss ("second terminal") and therefore constitutes a "variable-impedance electrical path connected between the terminal T1 and the second terminal." (*Id.*, ¶79.)

Joo further discloses that "the impedance of the electrical path is controlled by a signal on the terminal T1," as recited in claim element 1(f). For instance, as shown in annotated figure 2 above, the signal on node N2/N6 ("terminal T1") is inverted by the inverter INV2, and the output of the inverter at node N4 is coupled to the gate (i.e., control terminal) of the NMOS transistor MN2. (*See* Ex. 1010, FIG. 2, 3:3-9.) A POSITA would have understood that the voltage on the gate terminal of the NMOS transistor MN2 controls whether the transistor MN2 is on or off. (*Id.*, 3:3-9; Ex. 1002, ¶80.) If the NMOS transistor MN2 is on, it has a lower impedance than when the NMOS transistor MN2 is off. (Ex. 1002, ¶81.) Therefore, the signal at node N2/N6 ("terminal T1") determines the signal at node N4, which in turn determines whether the NMOS transistor MN2 is on or off, i.e., has a low or high impedance ("the impedance of the electrical path[4] is controlled by a signal on the terminal T1"). (*Id.*; Ex. 1010, 3:51-4:4.)

[4] For purposes of this proceeding, Petitioner assumes that "the electrical path" refers to the "variable-impedance electrical path" recited in claim 1 and not the

g) a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶82-108.) Joo does not explicitly disclose "a diode for keeping the voltage on the terminal T1 within a predetermined range of values" as recited in claim element 1[g]. However, it would have been obvious to a POSITA to construct the PMOS transistor MP1 in figure 2 of Joo in such a way as to provide a diode as recited. (*Id.*, ¶82.) As discussed in more detail below, in view of Weste, a POSITA would have been motivated to construct the transistors in Joo's figure 2 circuit according to conventional CMOS (Complementary Metal-Oxide-Semiconductor) fabrication techniques, such as those disclosed in Weste. Conventional construction of PMOS transistors include body diodes corresponding to each of the source and drain for the PMOS device, where the anode of each body diode corresponds to the source/drain and the cathode of each body diode corresponds to the n-substrate or n-well in which the PMOS transistor is formed. When constructed according to conventional CMOS processing techniques, the body diode included in the PMOS transistor MP1 would maintain the voltage on node N2 ("terminal T1") "within a

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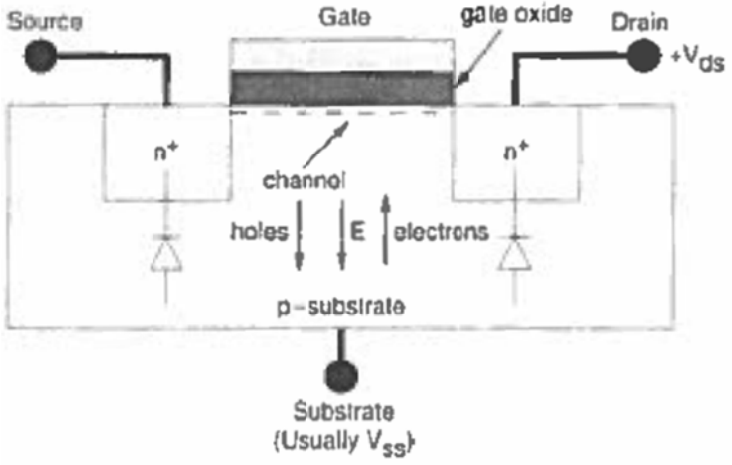
"programmable electrical path" that is also recited in claim 1. Petitioner, however, does not concede that claim 1 is not indefinite under 35 U.S.C. § 112.

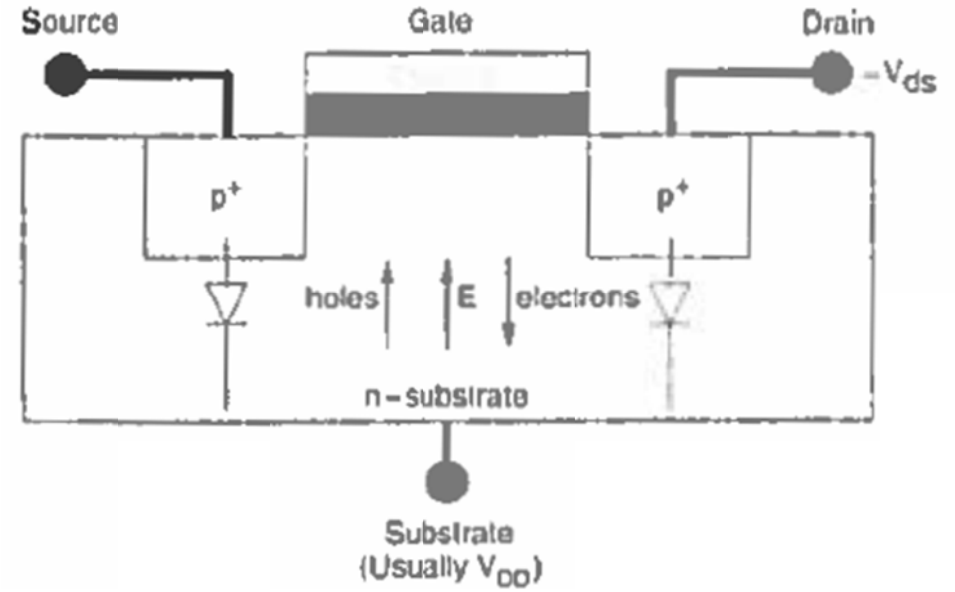
predetermined range of values before power is supplied to the latch." (Ex. 1002, ¶83.)

Weste is a treatise in the field of semiconductor integrated circuit devices, specifically CMOS technology. (Ex. 1009, 1, 379, 625.) Weste describes the operation and construction of semiconductor circuit elements that are used in Joo, such as NMOS and PMOS transistors, diodes, latches, and fusible links. (*Id.,* 19-21, 41-51, 91-93, 117-130, 318-322, 395-400.) For example, Weste discloses how both NMOS and PMOS transistors are constructed on a semiconductor substrate, as shown below. Weste explains that an NMOS transistor is formed by forming two n+ doped regions (corresponding to the source and drain) in a moderately doped p-type region (e.g., a p-substrate). (*Id.,* 43, FIG. 2.3.)



(*Id.,* FIG. 2.3 (showing an NMOS device).)

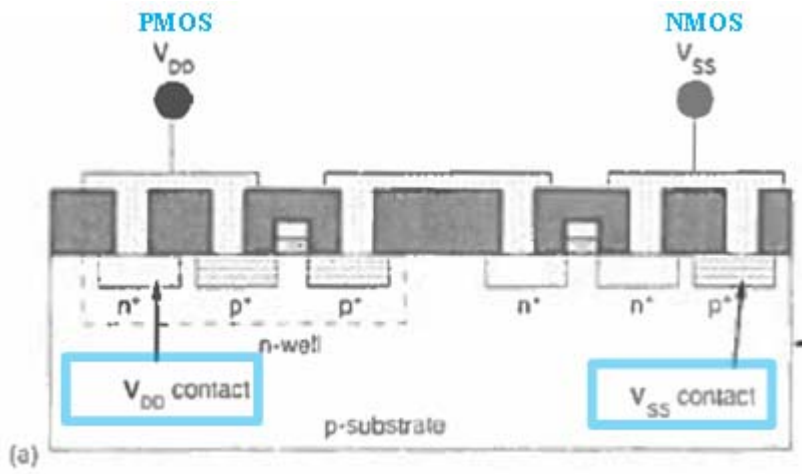
Similarly, a PMOS transistor is formed by forming two p+ regions (corresponding to the source and drain) into a moderately doped n-type region (e.g., an n-substrate). (*See id.*, 47, FIG. 2.6.)



(*Id.,* FIG. 2.6 (showing a PMOS device).)

As shown in figures 2.3 and 2.6 of Weste above, the NMOS and PMOS transistors each have a body (referred to as "substrate" in FIGs. 2.3 and 2.6 of Weste) connected to a voltage (Vss or low for NMOS, and Vdd or high for PMOS), and each have intrinsic diodes between the source/drain and the body. (Ex. 1002, ¶¶84-86.) For the diodes in the NMOS device, the anode corresponds to the body (p-type) and the cathode corresponds to the source/drain region (n-type). (*Id.*; Ex. 1009, FIG. 2.3.) For the diodes in the PMOS device, the anodes correspond to the source/drain region (p-type) and the cathodes correspond to the

body (n-type). (Ex. 1002, ¶¶85-86; Ex. 1009, FIG. 2.6.) These diodes are intrinsic to the construction of a MOS device and result from the p-n junctions that exist in the respective transistor structures. (Ex. 1002, ¶86.) As shown in figures 2.3 and 2.6, the body for an NMOS device is typically connected to V_{SS} (ground), and the body for a PMOS device is typically connected to V_{DD} (the positive power supply). (*Id.*, ¶87; Ex. 1009, 122-23, 231-32.) These body connections are also shown in FIG. 3.9 of Weste below, which illustrates an inverter formed with a PMOS transistor and an NMOS transistor, where the drains of the two transistors are coupled together. (Ex. 1009, 122-24.)



(Ex. 1009, FIG. 3.9 (annotated); *see id.*, 122-24; Ex. 1002, ¶87.)

As seen from the inverter structure shown in figure 3.9 of Weste, the NMOS transistor is formed by two n+ regions formed inside a p-substrate while the PMOS transistor is formed by two p+ regions formed inside an n-well, which is deposited

in the p-substrate. (Ex. 1002, ¶88.) The intrinsic diodes resulting from the numerous p-n junctions for such a CMOS inverter are shown in FIG. 4.35 of Weste below. (Ex. 1009, FIG. 4.35.)

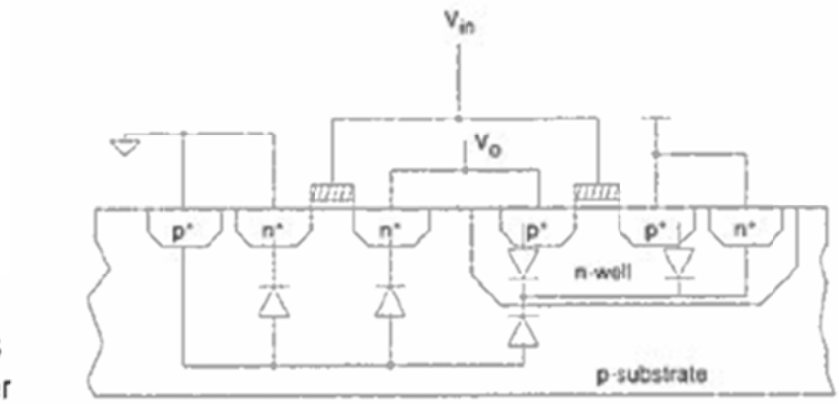
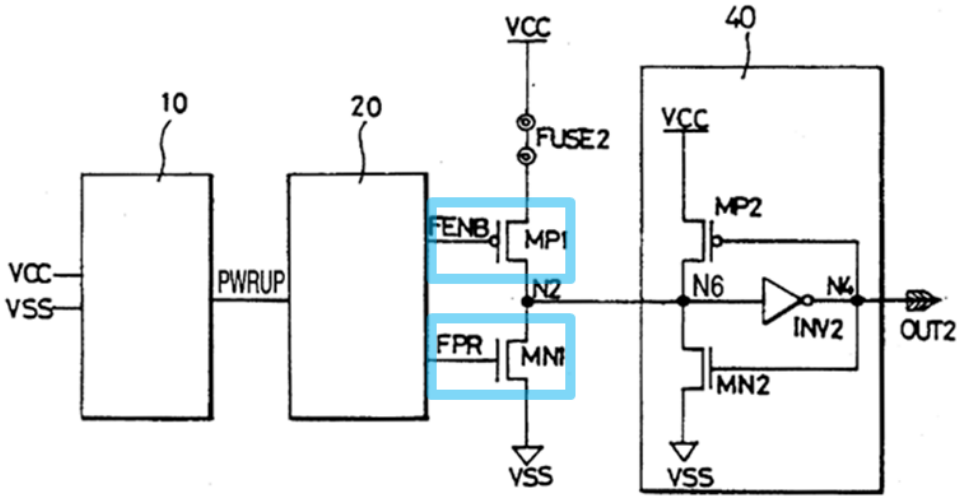


FIGURE 4.35 Model describing parasitic diodes present in a CMOS inverter

(Ex. 1009, 232 (FIG. 4.35).)

As shown in figure 2 of Joo below, similar to a CMOS inverter, transistors MP1 and MN1 are connected in series such that their drains are connected at node N2. (Ex. 1002, ¶89.)

FIG.2

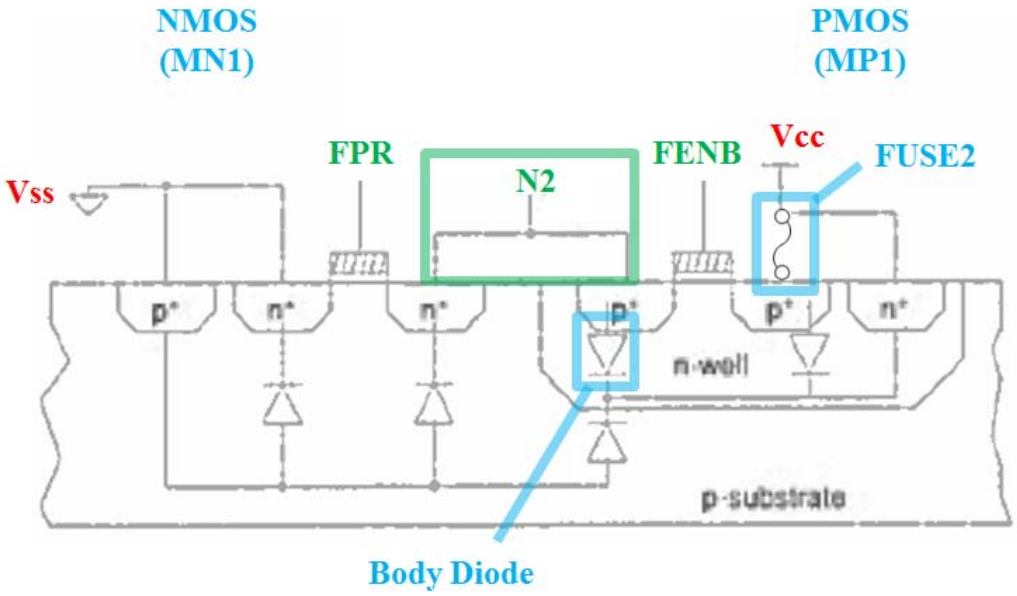


(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶89.)

Joo does not disclose how the PMOS transistor MP1 and the NMOS transistor MN1 are constructed. Weste, however, discloses how such transistors are constructed, and a POSITA would have found it obvious to construct the PMOS transistor MP1 and NMOS transistor MN1 such that they have the well-known structures disclosed in Weste. (*Id.*, ¶90.) The result would have been PMOS and NMOS transistors that have well-known semiconductor structures and operate as known in the art. (*Id.*)

A POSITA would also have recognized that, because the drains of MP1 and MN1 are connected at node N2 in the same manner as the drains of the PMOS and NMOS transistors in the inverter of Weste, MP1 and MN1 would be constructed on a common substrate in the same manner used for a CMOS inverter. (*Id.*, ¶91.)

The demonstrative below shows transistors MP1 and MN1 as they would have been implemented in the Joo-Weste combination, where the fuse FUSE2 of figure 2 is also included in schematic form.

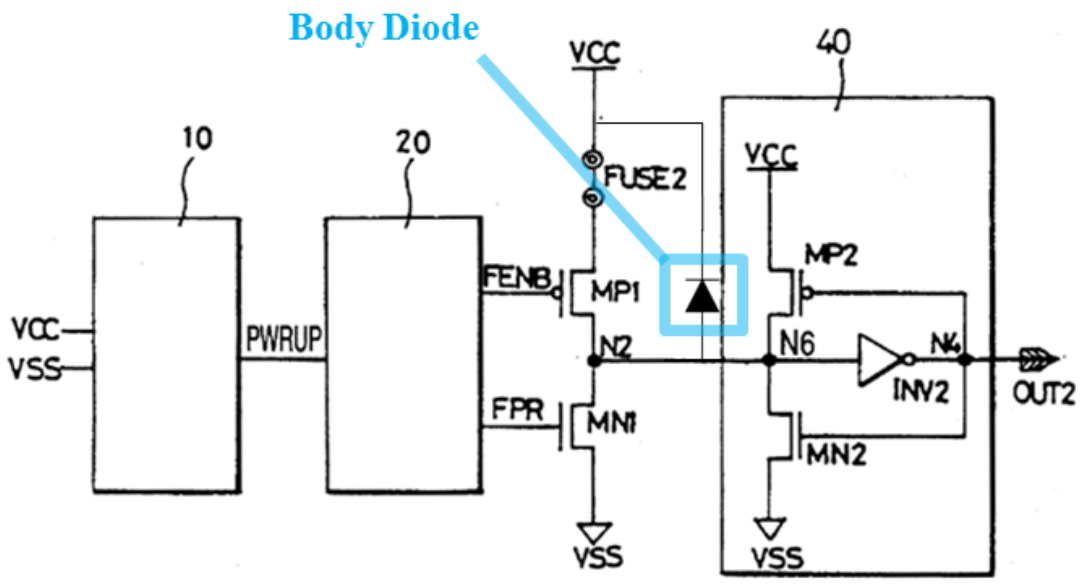


(Ex. 1009, 232 (FIG. 42.5 (annotated); Ex. 1002, ¶91.)

As can be seen in the demonstrative above, the construction of transistor MP1 in the manner well-known to a POSITA inherently forms body diodes between the p-type and n-type semiconductor regions. Specifically, the body diode that is highlighted in blue is between the p+ drain of the PMOS transistor MP1 and the n-well in which the PMOS transistor MP1 is formed. The n-well is tied to V_{CC} by the n+ ohmic contact formed in the n-well. (Ex. 1002, ¶92.) Therefore, the highlighted body diode has its anode at terminal N2 of the Joo-Weste combination

("Terminal T1") and the cathode of the diode is at Vcc. (*Id.*) The highlighted body diode above *that is included in PMOS transistor MP1* is represented in schematic form in the demonstrative below, which shows the body diode connected between node N2 and Vcc as described above.

FIG.2



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶92.)

A POSITA would have been motivated to look to a treatise like Weste when implementing the Joo circuit and would have chosen the CMOS process for implementing the combination because the CMOS process "is the leading VLSI systems technology." (Ex. 1009, 117). A POSITA would have had reason to

combine the teachings of Joo with Weste because while Joo discloses a circuit diagram (i.e., a schematic like figure 2), Joo does not disclose how to actually implement the components of the circuit in silicon. (Ex. 1002, ¶¶93-94.) Weste discloses well-known CMOS fabrication techniques that have been used to form transistors such as those in Joo for several decades. (*Id.*) Therefore, a POSITA would have implemented the Joo circuit of figure 2 using the CMOS fabrication techniques disclosed in Weste. (*Id.*)

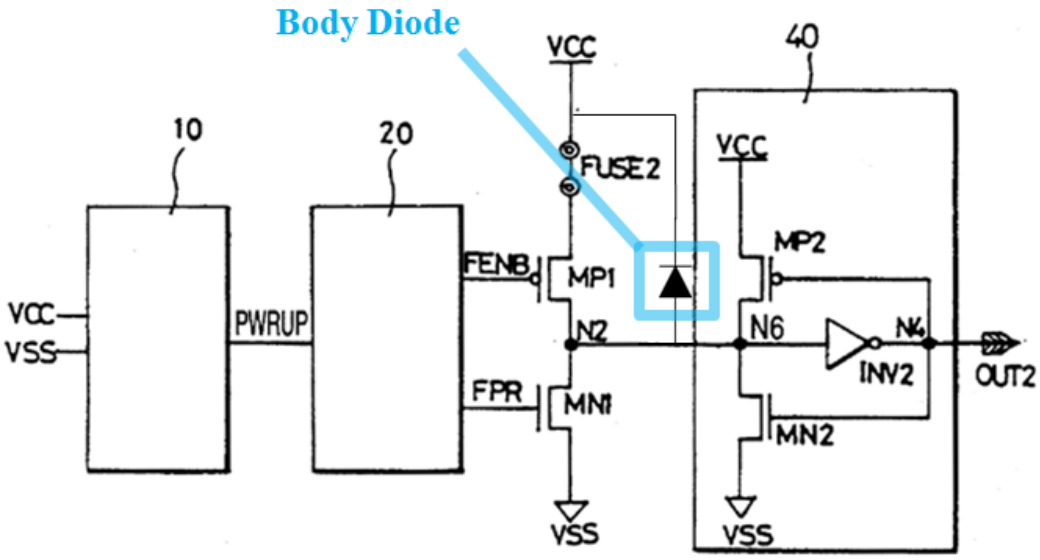
Indeed, the Federal Circuit has found obviousness under very similar circumstances. For example, the Federal Circuit has explicitly considered an earlier version of the Weste treatise and found it to be a resource that a POSITA would have consulted for guidance regarding implementing a circuit component disclosed in another reference. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1262 (Fed. Cir. 2007) (affirming a finding of obviousness based on a reference disclosing multiplexer circuits in view of an earlier edition of the Weste treatise disclosing a well-known option within a POSITA's technical grasp for implementing multiplexer circuits).

The presence of the body diodes disclosed by Weste in the circuit of FIG. 2 of Joo would not have negatively impacted the functionality of the circuit. Indeed, such body diodes are inherent to CMOS transistors, including both PMOS and NMOS transistors, and a POSITA would have understood that they would be

necessarily present in the circuit of Joo based on the conventional structure of NMOS and PMOS transistors. (Ex. 1002, ¶95.)

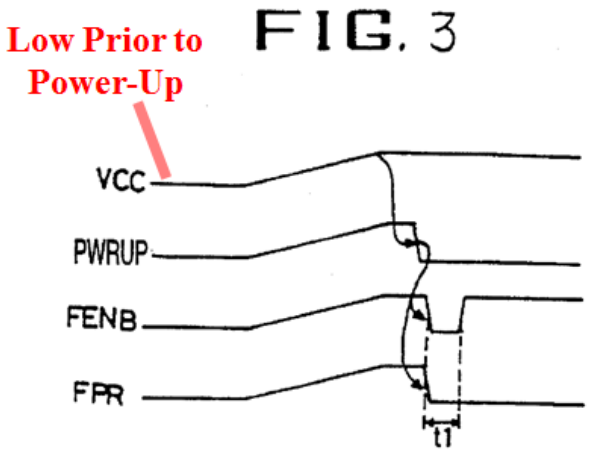
The circuit illustrated in the demonstrative above for the Joo-Weste combination discloses claim element 1[g], as explained below. For instance, the Joo-Weste combination discloses or suggests "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch." (Ex. 1002, ¶¶96-100.) As discussed above, the Joo-Weste combination includes a diode that is inherent to the PMOS transistor MP1. This diode is shown in the figure below connected between node N2 and terminal VCC:

FIG.2



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶96.)

As shown in figure 3 below, Joo discloses that before power is supplied to the circuit shown in figure 2, the supply voltage that is applied to the V_{CC} node ("first terminal") is low. (Ex. 1010, FIG. 3, 3:15-17 ("When power is supplied to the circuit, the power source voltage is gradually stepped up until the level Vcc is reached"); Ex. 1002, ¶¶97-98.)



(Ex. 1010, FIG. 3 (annotated); Ex. 1002, ¶97.)

A POSITA would have understood that when V_{CC} is low (*i.e.*, before power is supplied), the diode in the combined Joo-Weste circuit would not allow the voltage at node N2 to exceed the voltage on the Vcc terminal by more than a threshold voltage of the body diode. (Ex. 1002, ¶99.) Such an understanding is consistent with the disclosure of the '492 patent. (Ex. 1001, 2:1-12.)

Therefore, the Joo-Weste combination discloses or suggests "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before

power is supplied to the latch" because the body diode clamps the voltage on node N2 ("terminal T1") such that the voltage on node N2 cannot be higher than the diode threshold above the voltage on the Vcc node before power is supplied to the latch. (Ex. 1002, ¶100.) Stated differently, if the Vcc node is at voltage "X" before power is supplied to the latch, the body diode would not allow the voltage on node N2 to exceed "X" plus a diode threshold. Therefore, the body diode keeps the voltage at node N2 "within a predetermined range of values," where the "predetermined range of values" is voltages less than "X" (voltage level of Vcc node before power is supplied) plus a diode threshold. (*Id.*)

Claim element 1[g] further recites "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, *to prevent the latch from assuming an incorrect state when power is supplied to the latch*" (emphasis added). As discussed below, the body diode in the Joo-Weste combination functions in a similar manner to the diode 234 in the '492 patent. Therefore, for the same reasons that the diode 234 in the '492 patent "prevent[s] the latch from assuming an incorrect state when power is supplied to the latch," the body diode in the Joo-Weste combination also "prevent[s] the latch from assuming an incorrect state when power is supplied to the latch." (Ex. 1002, ¶¶101-108.)

For example, figure 2A of the '492 patent (reproduced below) shows one embodiment of a programmable latch according to the '492 patent. (Ex. 1001, 2:64-65, FIG. 2A.)

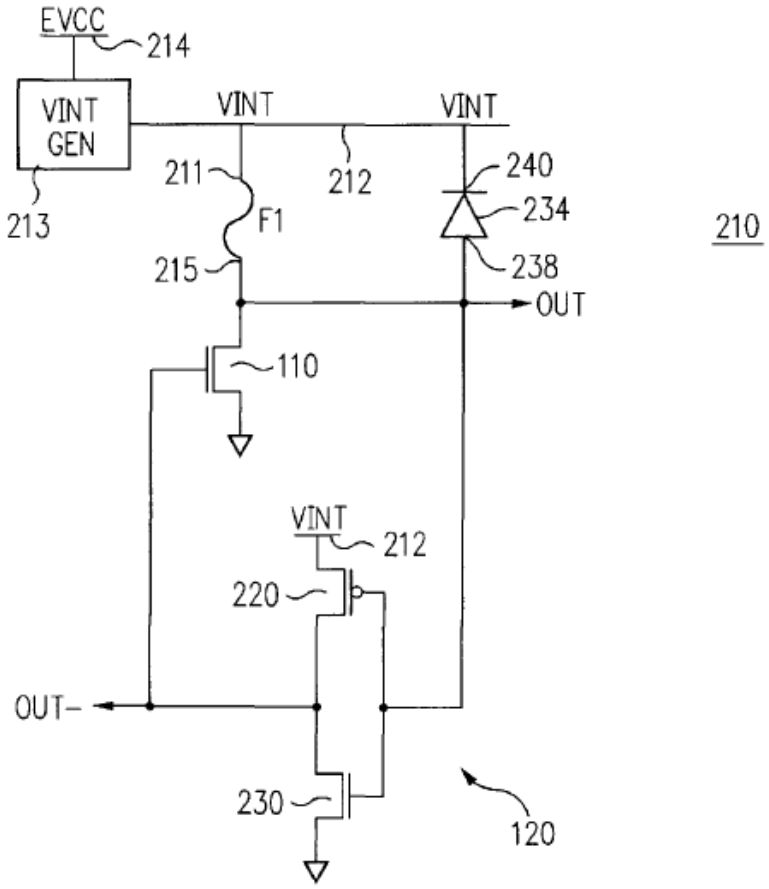


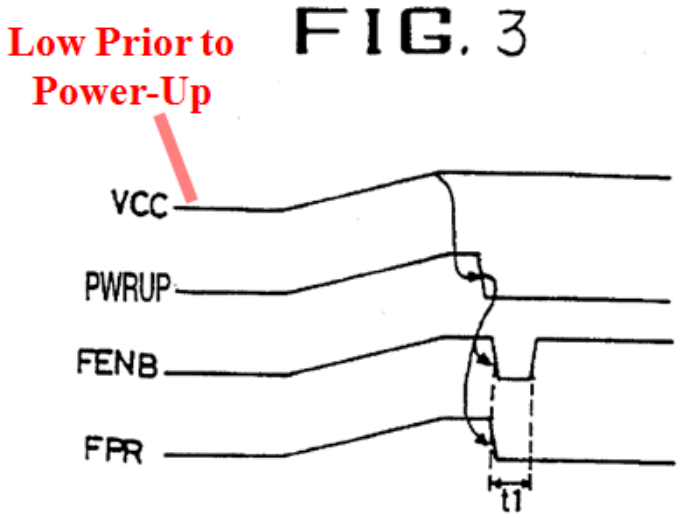
FIG. 2A

(*Id.*, FIG. 2A.)

The programmable latch of figure 2A includes a diode 234 that holds the OUT node at a voltage not higher than a threshold voltage of the diode 234 when the VINT terminal is ground. (*Id.*, 3:38-41.) According to the '492 patent, if the fuse F1 has been blown and power is applied to the circuit, transistor 110 turns on

and "connects the terminal OUT to ground," *resulting in a correct output.* (*Id.,* 3:41-49.) This happens because terminal OUT is held "not higher than one threshold voltage of diode 234," and at such a voltage, transistor 220 (and not transistor 230) turns on, which turns on transistor 110 that connects the terminal OUT to ground. (*Id.*) Stated differently, the correct output is achieved in the figure 2A latch of the '492 patent because the diode 234 drains away any excess charge on node OUT (i.e., "terminal T1" in the context of claim 1) and keeps the voltage on node OUT to a low level (e.g., not higher than a diode threshold above ground) before power is supplied to the latch. (Ex. 1002, ¶103.)

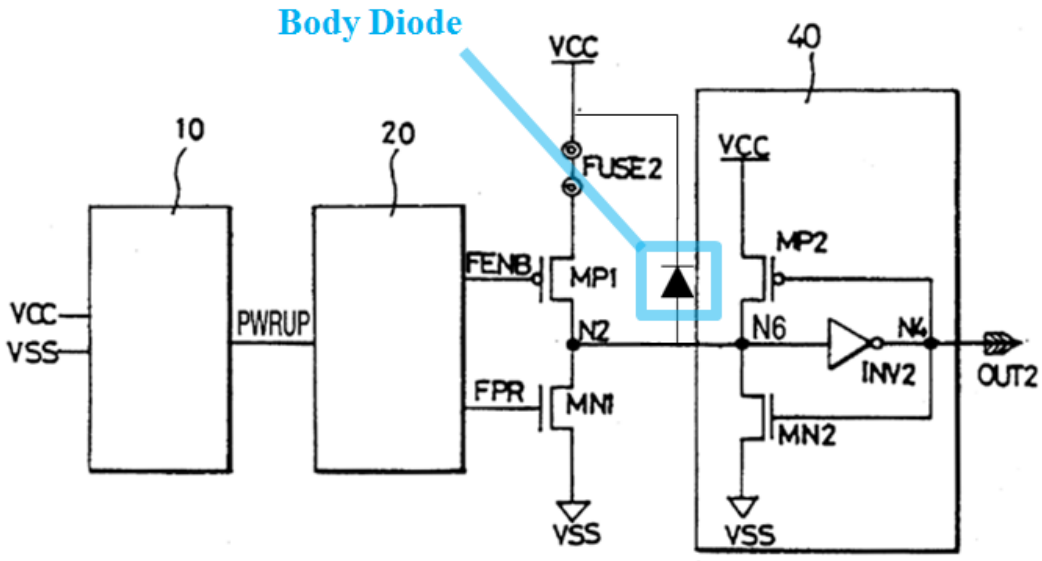
The body diode in the Joo-Weste combination works in a similar manner as diode 234 in the '492 patent because it drains away any excess charge on node N2 and keeps N2 to a low level before power is supplied to the latch. (*Id.,* ¶104.) As explained above, the Vcc node in the Joo circuit is at a low voltage before power is supplied. Because the body diode in the Joo-Weste combination has its anode at node N2 and cathode at the Vcc node, the body diode maintains node N2 at a low voltage (at most a diode threshold voltage above the low voltage on Vcc when power is not supplied) before power is supplied to the circuit. (*Id*.)



(Ex. 1010, FIG. 3 (annotated); Ex. 1002, ¶104.)

Under the scenario in which the fuse is blown, because the voltage on N2 is maintained at a low voltage by the body diode before power is applied, the output of inverter INV2 will be a high voltage that will turn off MP2 and turn on MN2 when power is ultimately applied to the circuit. (Ex. 1002, ¶105.) As a result, N2 will remain at a low level because MP2 will not pull N2 high, and in fact, MN1 will pull N2 low to VSS. When the fuse is blown, N2 being at a low voltage is the correct state of the latch. (*Id.*; Ex. 1010, 3:36-40.)

FIG.2



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶105.)

As such, the body diode in the Joo-Weste circuit "prevent[s] the latch from assuming an incorrect state when power is supplied to the latch" when the fuse is blown in a similar manner to the diode 234 shown in figure 2A of the '492 patent. (Ex. 1002, ¶106.)

When the fuse is intact, while the node N2 has been pulled to no higher than a threshold voltage above the low voltage on Vcc prior to power being supplied, after power is supplied and transistor MP1 turns on, a large current flows through MP1, which causes node N2 to be pulled high to Vcc. (*Id.*, 107; Ex. 1010, 3:51-56.) Because Vcc is high when the node N2 is pulled high, the diode is not

forward biased as it has the same voltage at the anode (node N2) and cathode (Vcc). (Ex. 1002, ¶107.) Therefore, the body diode does not affect node N2 being pulled high once power is applied. As node N2 is pulled high, inverter INV2 outputs a low voltage on OUT2. The low voltage on OUT2 turns on the PMOS transistor MP2, which latches the high voltage at node N2, and the correct state of the fuse is reflected in the output of the circuit. (*Id.*)

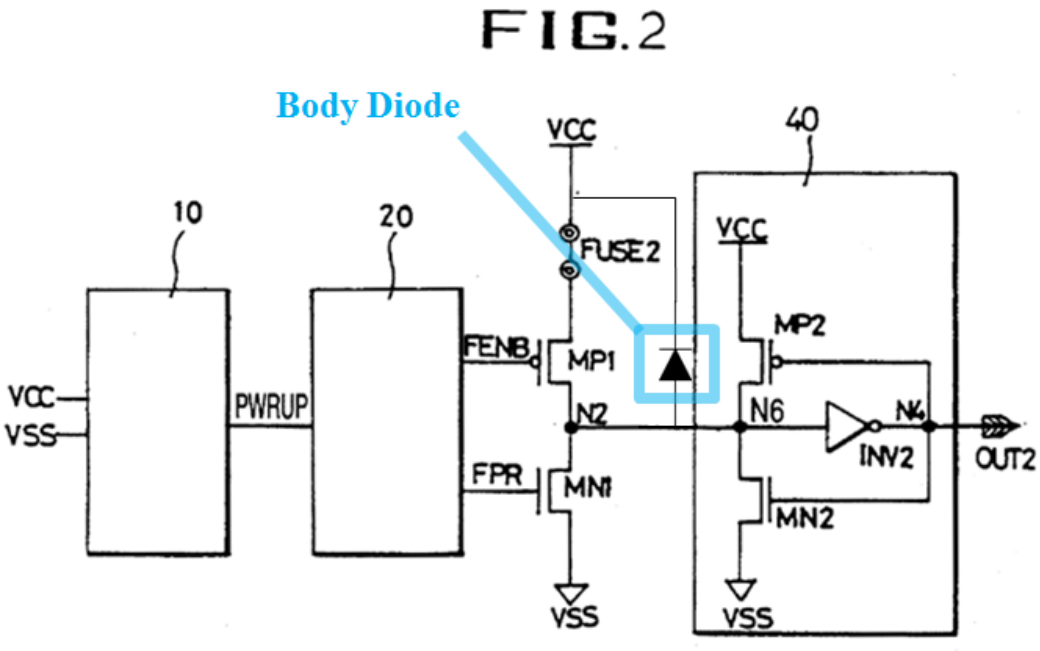
For at least these reasons, the Joo-Weste combination discloses or suggests "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch" as recited in claim 1. (*Id.*, ¶108.)

2. Claim 2

a) The programmable latch of claim 1 wherein during operation of the latch the signal on the terminal T1 is completely determined by the state of the programmable element and the first and second voltages.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶109.) As discussed above with respect to claim element 1[a], during operation of the latch, the voltage at node N2 ("terminal T1") is only influenced by the power supply voltages Vcc and Vss ("first and second voltages") and the state of the fuse FUSE2 ("programmable element"). (*See supra* Section IX.A.1(a).) Specifically, based on whether fuse FUSE2 is open (*i.e.*, blown) or remains intact, output OUT2

of the fuse circuit shown in FIG. 2 is held at either Vcc or Vss. (Ex. 1010, 3:36-40; Ex. 1002, ¶109; *see supra* Section IX.A.1(a).)



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶109.)

3. Claim 4

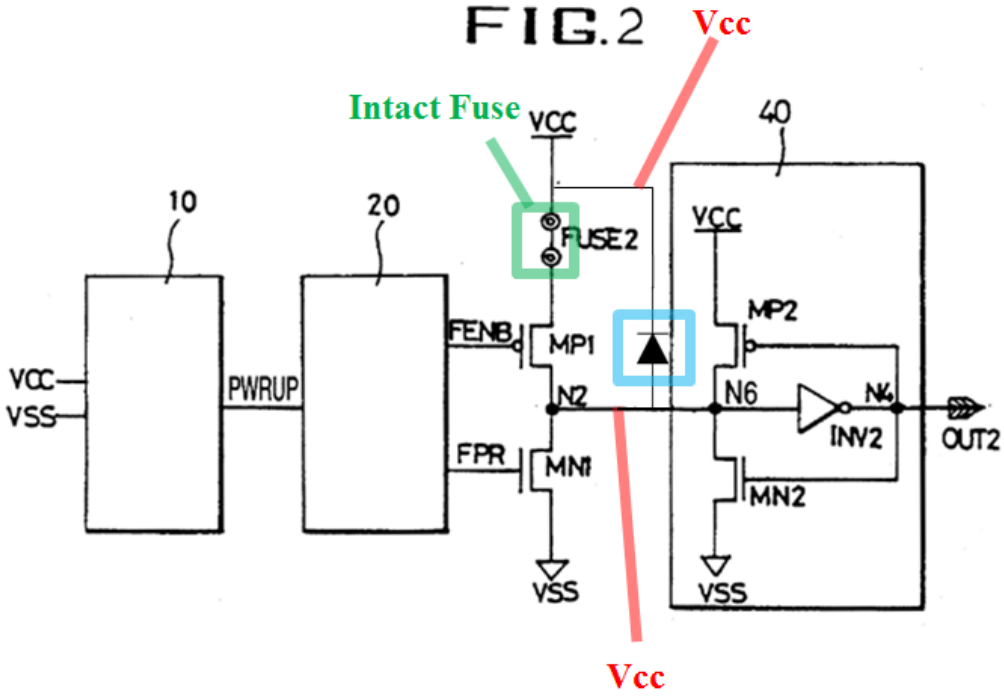
a) The programmable latch of claim 1 wherein no current flows through the diode during normal operation of the latch, but when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶110-115.) In order for current to flow through the body diode included in the Joo-Weste combination, the diode must be in the "forward bias" state, i.e., the voltage

on the anode of the diode must be greater than the voltage on the cathode of the diode by at least the threshold voltage of the diode. (*Id.,* ¶¶37-38, 110.)

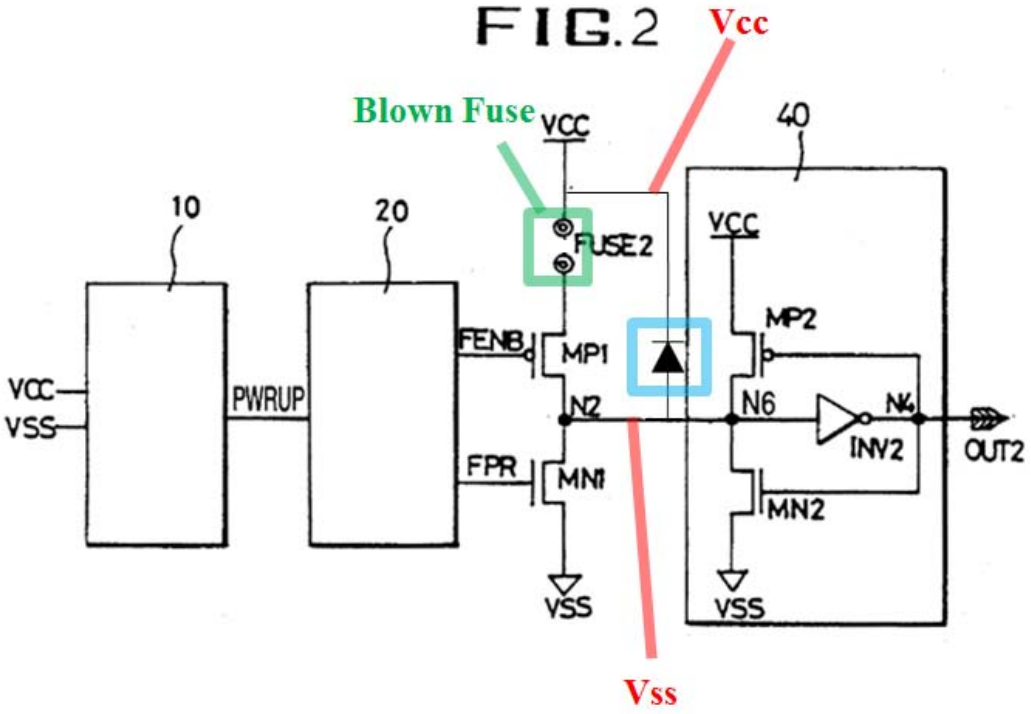
When power is applied to the fuse circuit ("programmable latch") during normal operation of the latch in the Joo-Weste combination, the first terminal is connected to Vcc, which corresponds to the high power supply voltage. (*Id.,* ¶111; Ex. 1010, 3:15-17, 3:36-40.) In this scenario, the diode is not in a "forward bias" state and thus no current flows through the diode. (Ex. 1002, ¶111.) In particular, as shown in the demonstrative below, when the fuse FUSE2 is intact, the fuse pulls up the node N2, which is held high by the PMOS transistor MP2. (*Id.*; Ex. 1010, 3:46-40, "Consequently, in accordance with the state of the fuse FUSE2, either the level of the first node N2 is maintained at the ground level Vss (if the fuse FUSE2 is open), or the level of the first node N2 is pulled up to the power supply voltage Vcc (if the fuse FUSE2 is connected)."; *id.,* 3:44-47, "When the fuse FUSE2, which is part of the programmable ROM cell, is connected, the latching section 40 pulls up the level of the node N2 to the power supply level Vcc.") Therefore, when the fuse FUSE2 is intact, the voltage at node N2 is the same as the voltage on the power supply Vcc. (Ex. 1002, ¶111.) As such, the voltage at both the anode (node N2) and the cathode (first terminal) of the diode is Vcc. (*Id.*) Therefore, the voltage at the anode of the diode (Vcc) does not exceed the voltage at the cathode

of the diode (also Vcc) by at least a threshold voltage of the diode and no current flows through the diode. (*Id.*)



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶111.)

Similarly, during operation of the latch when the fuse has been blown, node N2 is pulled low to ground by the transistor MN2. (*See supra* Section IX.A.1(a); Ex. 1002, ¶112.) As such, the voltage on the anode of the diode (node N2) is Vss (low) and the voltage on the cathode of the diode (first terminal) is Vcc (high). Therefore, the voltage at the anode of the diode (low) does not exceed the voltage at the cathode of the diode (high) by at least a threshold voltage of the diode and no current flows through the diode. (Ex. 1002, ¶112.)



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶112.)

As demonstrated above, when power is applied to the programmable latch of the Joo-Weste combination (i.e., during normal operation), no current flows through the diode regardless as to whether or not the fuse has been blown. (*Id.*, ¶113.) Therefore, the Joo-Weste combination discloses or suggests "wherein no current flows through the diode during normal operation of the latch." (*Id.*)

As disclosed by Joo, when the power is off, the power supply voltage Vcc is low. (Ex. 1010, FIG. 3, 3:15-17 ("[w]hen power is supplied to the circuit, the power source voltage is gradually stepped up until the level Vcc is reached").) As

discussed above with respect to claim element 1[g], when the power is off, the diode in the combined Joo-Weste circuit will not allow the voltage at node N2 to exceed the low voltage on Vcc by more than a threshold voltage of the diode. (Ex. 1002, ¶114.) This is because if the voltage on the anode of the diode (node N2) were more than a threshold voltage above the voltage at the cathode of the diode (the low voltage on Vcc), the threshold voltage of the diode would be exceeded and the diode would turn on, thereby causing current to flow through the diode from node N2 to the low voltage on Vcc. (*Id.*). Such current flow would continue until the voltage across the diode becomes less than a threshold voltage above the low voltage on the Vcc node, and the diode turns off. (*Id.*)

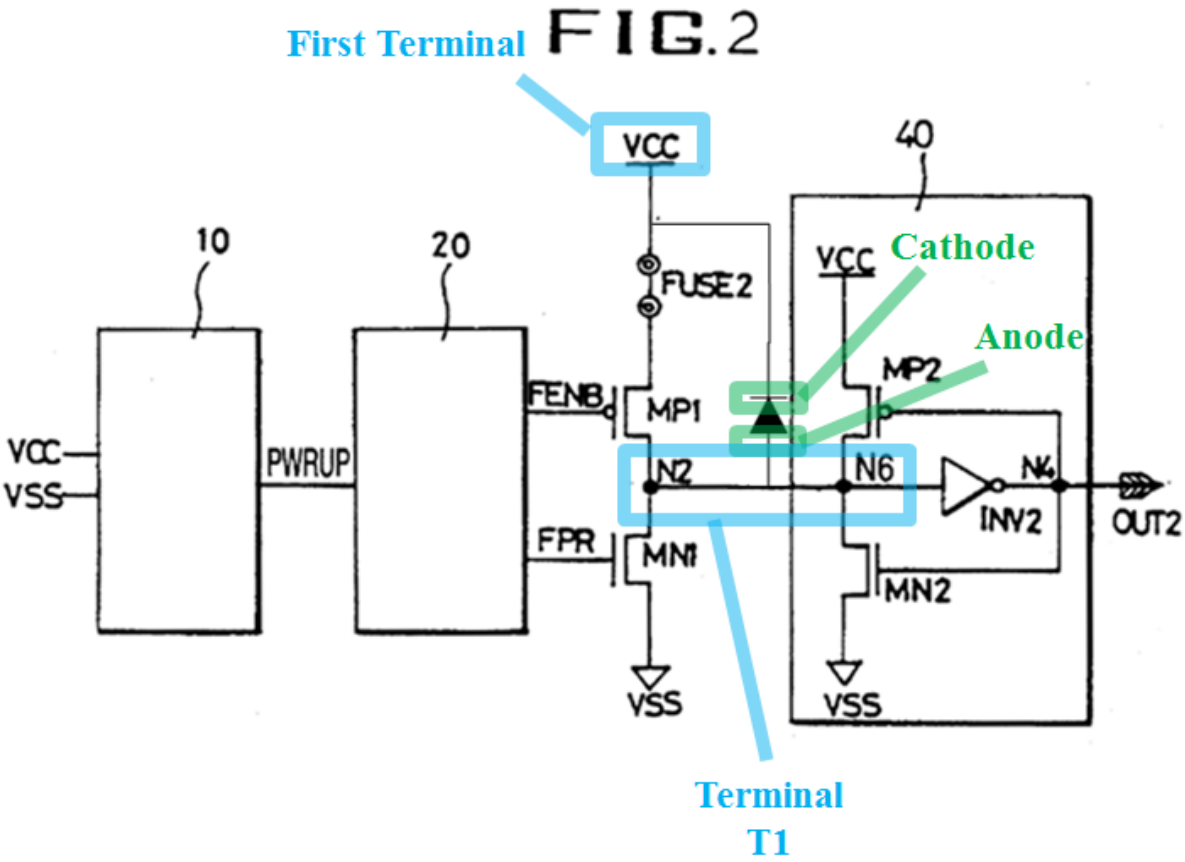
Therefore, the combined Joo-Weste circuit discloses or suggests that when the power is off, Vcc is low, and current flows through the diode if the voltage on node N2 ("terminal T1") exceeds the low voltage on Vcc by the threshold voltage of the diode ("when the power is off then current flows through the diode if the voltage on the terminal T1 is outside the predetermined range of values").) (*See supra* Section IX.A.1(g) describing that the "predetermined range of values" is the range of voltages less than a diode threshold voltage above the low voltage on Vcc when power is not supplied; Ex. 1002, ¶115.)

4. Claim 8

a) The programmable latch of claim 1 wherein the diode has one terminal connected to the terminal T1, and the diode

has another terminal connected to the first terminal.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶116-117.) As shown in the demonstrative below, the diode in the Joo-Weste combination has one terminal (the anode) connected to node N2, which corresponds to "terminal T1." (*See supra* Sections IX.A.1(d), (g); Ex. 1002, ¶116.) The diode also has another terminal (the cathode) connected to Vcc, which corresponds to the "first terminal" recited in claim 1 above. (*Id.*)



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶116.)

Therefore, the Joo-Weste combination discloses or suggests a programmable latch "wherein the diode has one terminal connected to the terminal T1, and the diode has another terminal connected to the first terminal" as recited in claim 8. (Ex. 1002, ¶117.)

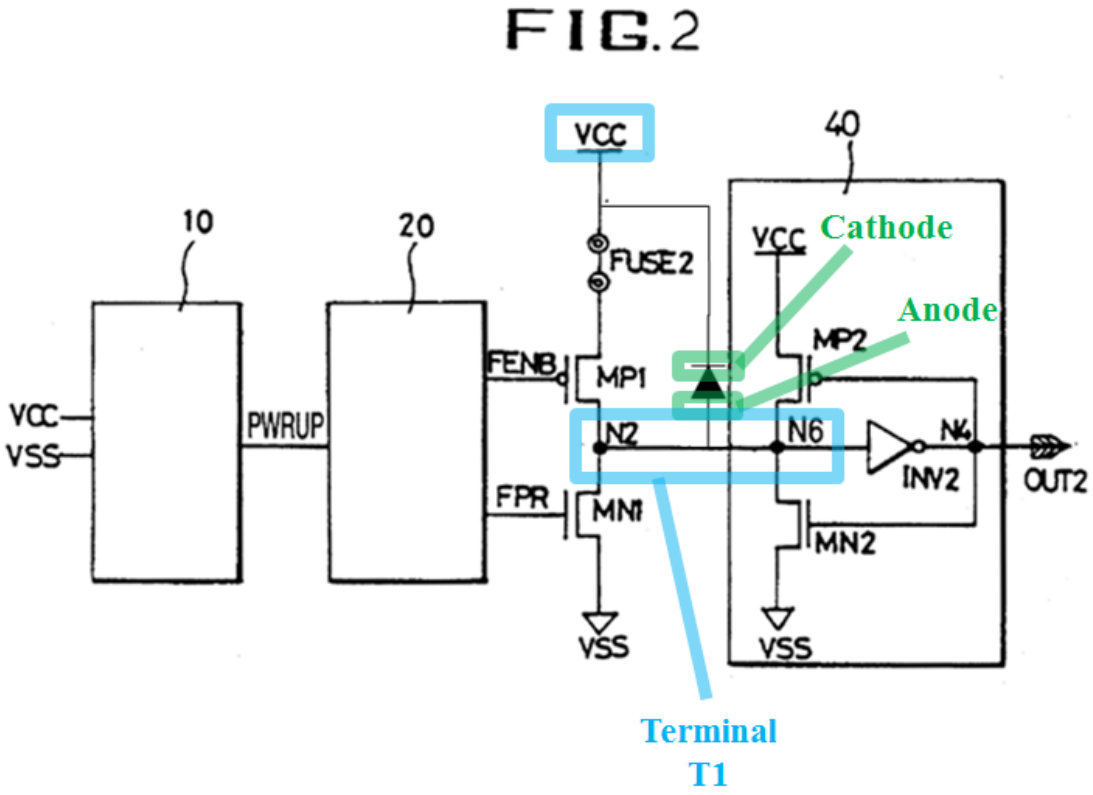
5. Claim 9

a) The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶118.) For example, Joo discloses that "[t]he present invention relates to a semiconductor memory device, and more particularly, to a programming section of a semiconductor memory device having a fuse read only memory (fuse ROM)." (Ex. 1010, 1:7-10.) As further disclosed by Joo, "FIG. 2 illustrates a circuit of a semiconductor memory device having a fuse ROM in accordance with the present invention." (*Id.,* 2:49-51.) A POSITA would have understood that a "semiconductor memory device" as described in Joo is an integrated circuit device. (Ex. 1002, ¶118.) Therefore, the latch of figure 2 of Joo, as modified by Weste, (*see supra* Sections IX.A.1(a), (g)) is "part of an integrated circuit." (Ex. 1002, ¶118.)

b) wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶119-121.) For example, as shown in the demonstrative below, the anode ("one terminal") of the diode in the Joo-Weste combination is connected to node N2 ("terminal T1") and the cathode ("another terminal") of the diode is connected to Vcc. (*Id.*, ¶119.)



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶119.)

As discussed above with respect to claim element 1[b], Vcc is a "supply voltage" that is supplied when power is applied to the circuit of figure 2. (Ex. 1010, 2:51-53 ("fuse FUSE2, a PMOS transistor MP1, and an NMOS transistor

MN1 are connected in series between a power source Vcc and a ground voltage Vss"), 3:15-17 ("[w]hen power is supplied to the circuit, the power source voltage is gradually stepped up until the level Vcc is reached"), 3:36-40 ("in accordance with the state of the fuse FUSE2 . . . node N2 is pulled up to the power supply voltage Vcc (if the fuse FUSE2 is connected").) In the example embodiment of Joo, Vcc is at a high voltage after power up of the latch and therefore constitutes "non-ground power-supply voltage." (Ex. 1002, ¶120.) A POSITA would have understood that a power supply voltage for an integrated circuit is typically provided via an external pin and therefore would have understood that the Vcc power-supply voltage in Joo would have been received "from an external pin of the integrated circuit" on which the fuse circuit is located. (*Id*.)

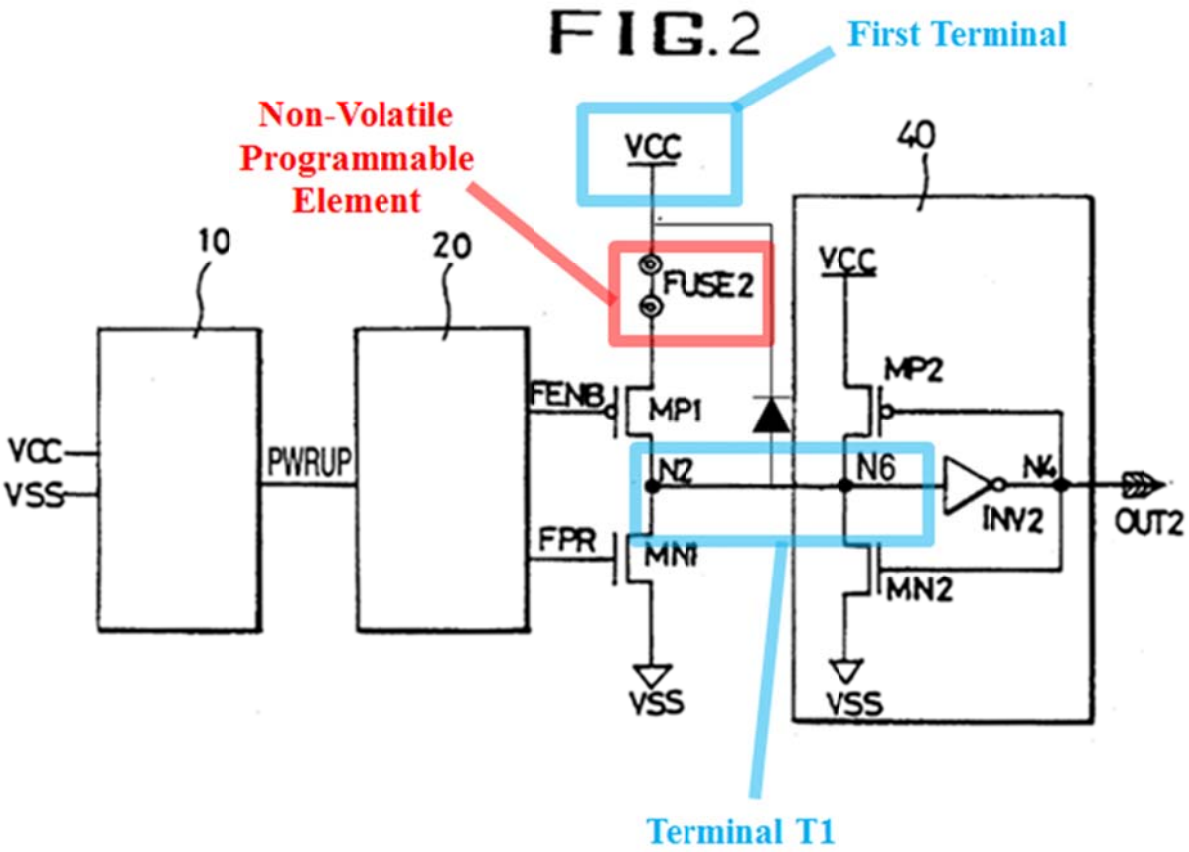
To the extent that Joo does not disclose that the Vcc terminal receives the non-ground supply voltage from an external pin, it would have been obvious to provide the non-ground power supply voltage Vcc from an external pin. (*Id.,* ¶121.) Joo discloses that the power supply has a first terminal and a second terminal, where one of the first and second terminals is a positive voltage and the other is ground. (Ex. 1010, 2:51-53, 3:15-17, 3:36-40.) A POSITA would have understood that supply voltages for integrated circuits are commonly supplied via pins on the integrated circuit that permit connectivity to circuitry and voltage sources outside of the integrated circuit. (Ex. 1002, ¶121.) Therefore, the Joo-

Weste combination discloses or suggests "the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit." (*Id*.)

6. Claim 10

a) The programmable latch of claim 1 wherein: the programmable element is a fuse connected to and between the terminal T1 and the first terminal;

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶122.) As demonstrated above with respect to claim element 1[e], Joo discloses a fuse FUSE2 that constitutes a "programmable element," where the fuse FUSE2 is connected between node N2 ("terminal T1") and Vcc ("the first terminal").) (*See supra* Section IX.A.1(e).) In addition, the fuse FUSE2 is connected to node N2 ("terminal T1") via PMOS transistor MP1 and connected to Vcc ("the first terminal").) (*See supra* Section IX.A.1(e).) Therefore, the Joo-Weste combination discloses or suggests "the programmable element is a fuse connected to and between the terminal T1 and the first terminal." (Ex. 1002, ¶122.)

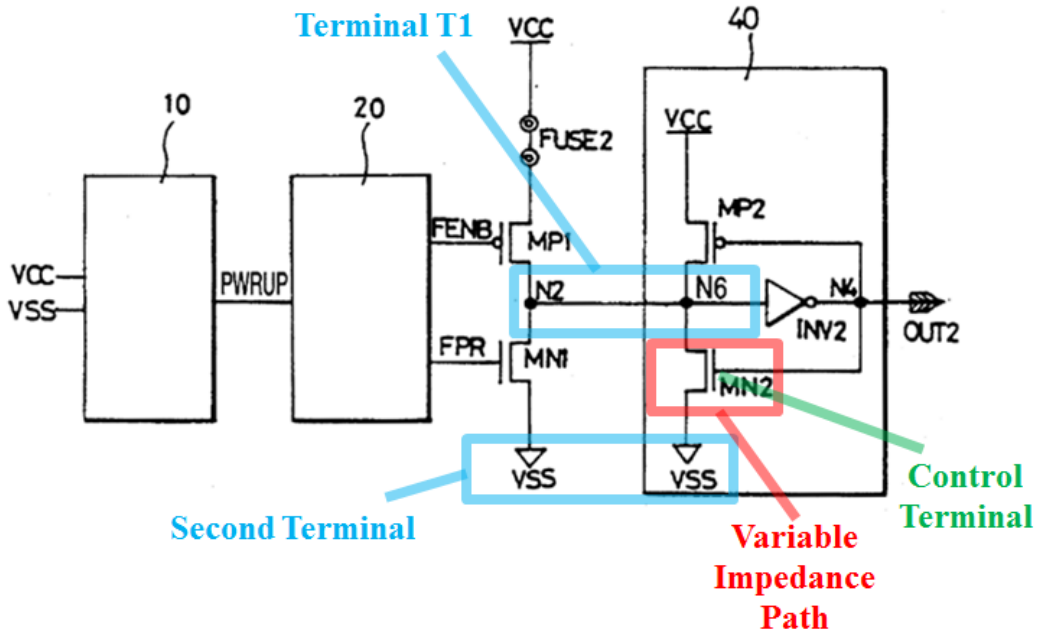


(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶122.)

b) the variable-impedance path is a transistor connected to and between the terminal T1 and the second terminal and having a control terminal;

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶123-124.) As demonstrated with respect to claim element 1[f] above, the NMOS transistor MN2 highlighted in the Joo-Weste combination below is a "variable-impedance electrical path." (*Id.*, ¶123; *see supra* Section IX.A.1(f).)

FIG.2



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶123.)

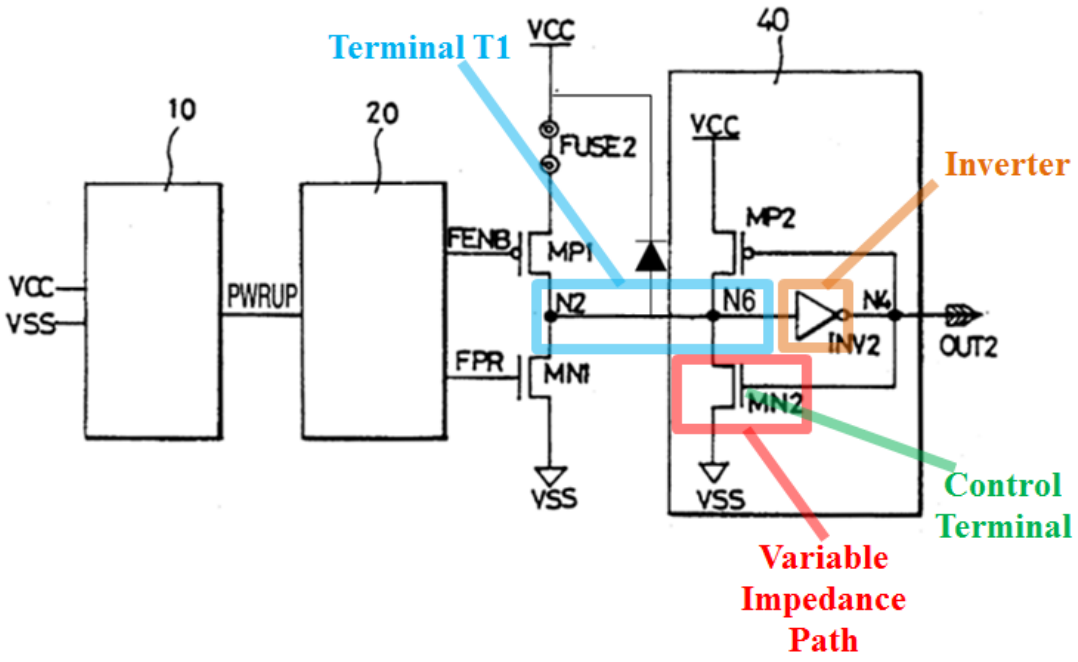
As shown in the demonstrative above, the NMOS transistor MN2 ("variable-impedance electrical path") is coupled between node N2/N6 ("terminal T1") and Vss ("second terminal") and therefore is "connected to and between the terminal T1 and the second terminal." Furthermore, the gate of transistor MN2 is used to control whether the transistor MN2 is on or off, and therefore the gate of transistor MN2 is a "control terminal." (*See supra* Section IX.A.1(f); Ex. 1002, ¶¶124.)

c) the programmable latch further comprises an inverter whose input is connected to the terminal T1 and whose output is connected to the control terminal of said transistor, the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-

down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶125-129.) For example, the Joo-Weste combination discloses a programmable latch that includes an inverter, where the inverter is highlighted in orange in the demonstrative below. (*Id.*, ¶125.)

FIG.2



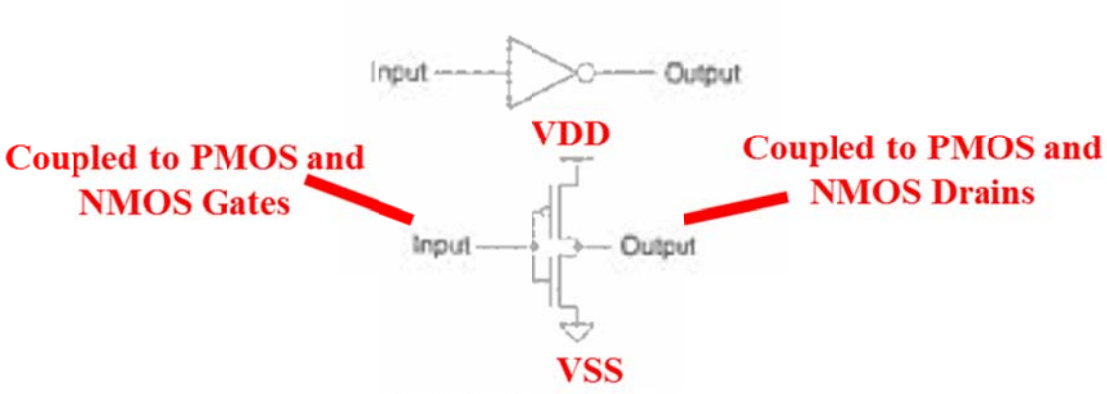
(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶125.)

As shown in the demonstrative above, the input of the inverter INV2 is connected to node N2/N6 ("an inverter whose input is connected to the terminal

T1"), and the output of the inverter INV2 is connected to the gate of transistor MN2 ("inverter … whose output is connected to the control terminal of said transistor"). (Ex. 1002, ¶126.)

Joo does not explicitly disclose that the "inverting device" (inverter) INV2 includes a pull-up device and a pull-down device, nor does it specifically disclose how the inverter INV2 is constructed. (*Id.,* ¶127.) But a POSITA would have understood that INV2 would have been constructed using a PMOS transistor ("pull-up" device) and an NMOS transistor ("pull-down" device) that are connected with each other like MP2 and MN2 in figure 2 of Joo. (*Id*.) This is because MP2 and MN2 also constitute an "inverter" and the symbol used for inverter INV2 typically indicates a configuration like MP2 and MN2 where a PMOS and an NMOS share the drain region (which is the output of the inverter) and receive a common input at their gates. (*Id.*) Therefore, Joo's inverter INV2 discloses "the inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output" because, as discussed above, an inverter constructed like MP2 and MN2 has a PMOS transistor ("pull up" device) and NMOS transistor ("pull down" device) that have a common output and a common input. (*Id.*) This is further confirmed by Weste, which discloses a transistor level schematic of an inverter that includes an

NMOS transistor (bottom) and a PMOS transistor (top) just like MN2 and MP2 in figure 2 of Joo. The PMOS in Weste's figure 1.4 is a "pull up" device because it pulls the output high (i.e., to VDD) when it is on and the NMOS is a "pull down" device because it pulls the output low (i.e., to VSS) when it is on. (*Id.*; Ex. 1009, 9.)



(Ex. 1009, 10 (FIG. 1.4) (annotated); Ex. 1002, ¶127.)

To the extent Patent Owner contends a POSITA would not have understood from Joo that inverter INV2 has the typical configuration of an inverter, a POSITA would have found it obvious, in view of Weste, to form inverter INV2 like MP2 and MN2. (Ex. 1002, ¶128.) Specifically, based on the above teachings of Weste, which are consistent with a POSITA's understanding of the circuit structure of an "inverter," a POSITA would have been motivated to form INV2 ("inverter") with a PMOS transistor and an NMOS transistor, where the drains of the two transistors are coupled together at the inverter output and the gates of the two transistors

receive a common input. (*Id.*) A POSITA would have found it obvious to do so because such a configuration was the widely-known configuration of a CMOS inverter like INV2 and it was typical to implement inverters in such a manner. (*Id.*) Indeed, the Federal Circuit has found obviousness under very similar circumstances. For example, the Federal Circuit has explicitly considered an earlier version of the Weste treatise and found it to be a resource that a POSITA would have consulted for guidance regarding implementing a circuit component disclosed in another reference. *In re Translogic Tech., Inc.*, 504 F.3d at 1262 (affirming a finding of obviousness based on a reference disclosing multiplexer circuits in view of an earlier edition of the Weste treatise disclosing a well-known option within a POSITA's technical grasp for implementing multiplexer circuits).

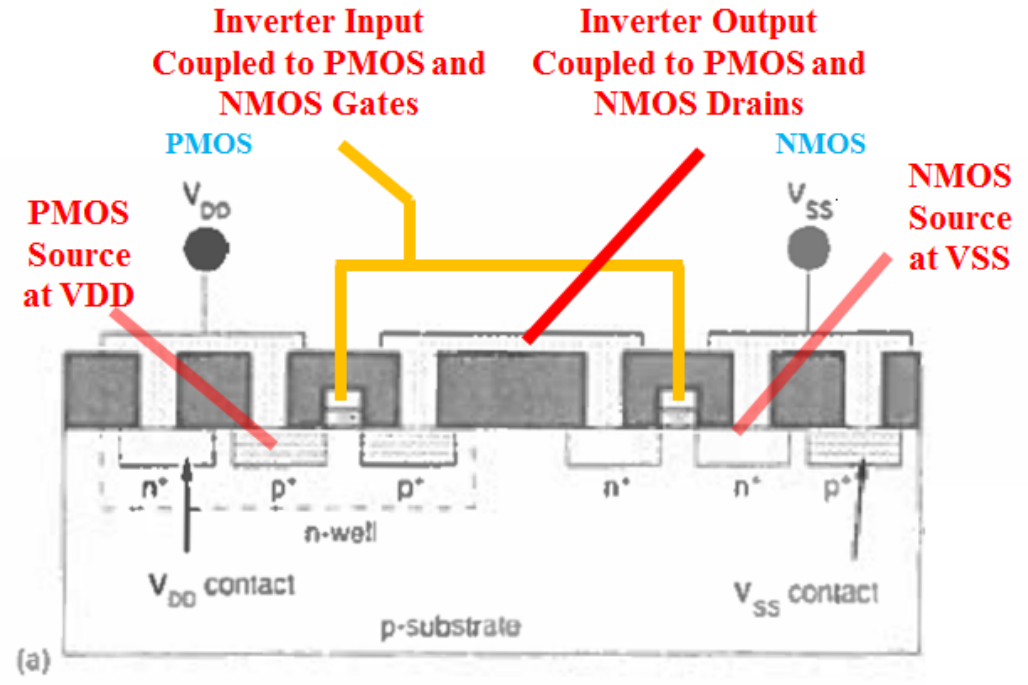
Therefore, the Joo-Weste combination discloses or suggests an "inverter having a pull-up device and a pull-down device, wherein at least one of the pull-up and pull-down devices is connected to the inverter input, and both of the pull-up and pull-down devices are connected to the inverter output." (Ex. 1002 at ¶129.)

7. Claim 11

a) The programmable latch of claim 10 wherein one of the pull-up and pull-down devices is a MOS transistor formed in a first semiconductor region of a first conductivity type, and the diode comprises a second semiconductor region of a second conductivity type forming a junction with the first semiconductor region, the second region being connected to the terminal T1.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶130-136.) As discussed above with respect to claim 10, it would have been obvious to implement the inverter INV2 in Joo such that INV2 includes a PMOS and an NMOS. (*See supra* Section IX.A.6.)

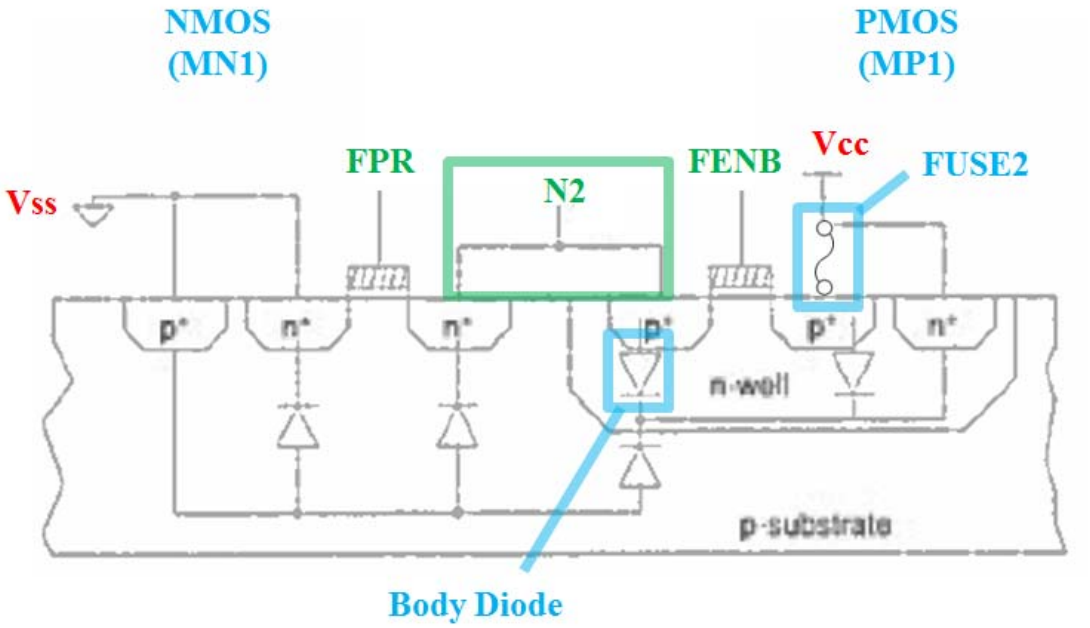
As discussed above with respect to claim element 1[g], figure 3.9 of Weste illustrates the layout for an inverter formed with a PMOS transistor and an NMOS transistor, where the drains of the two transistors are coupled together at the inverter output. (Ex. 1009, 122-23, FIG. 3.9; *see supra* Section IX.A.1(g); Ex. 1002, ¶131.)



(Ex. 1009, FIG. 3.9 (annotated); *see id.*, 122-23; Ex. 1002, ¶131.)

As seen from the inverter structure shown in figure 3.9 of Weste, the NMOS transistor is formed by two n+ regions formed inside a p-substrate while the PMOS transistor is formed by two p+ regions formed inside an n-well, which is deposited in the p-substrate. (Ex. 1009, FIG. 3.9; Ex. 1002, ¶132.) As is also shown in figure 3.9 above, the gates of the PMOS and NMOS transistors are coupled to the input of the inverter, and the source of the PMOS transistor is coupled to VDD while the source of the NMOS transistor is coupled to VSS. (*Id*.)

As shown in annotated figure 3.9 above, the PMOS transistor ("one of the pull-up and pull down devices is a MOS transistor") is formed in the n-well ("formed in a first semiconductor region of a first conductivity type"). As further discussed above with respect to claim element 1[g], a POSITA would have formed transistors MP1 and MN1 in figure 2 of Joo according to the teachings of Weste. (*See supra* Section IX.A.1(g).) The resulting structure for the transistors MP1 and MN1 in the Joo-Weste combination is shown in the demonstrative below. (Ex. 1002, ¶133.)



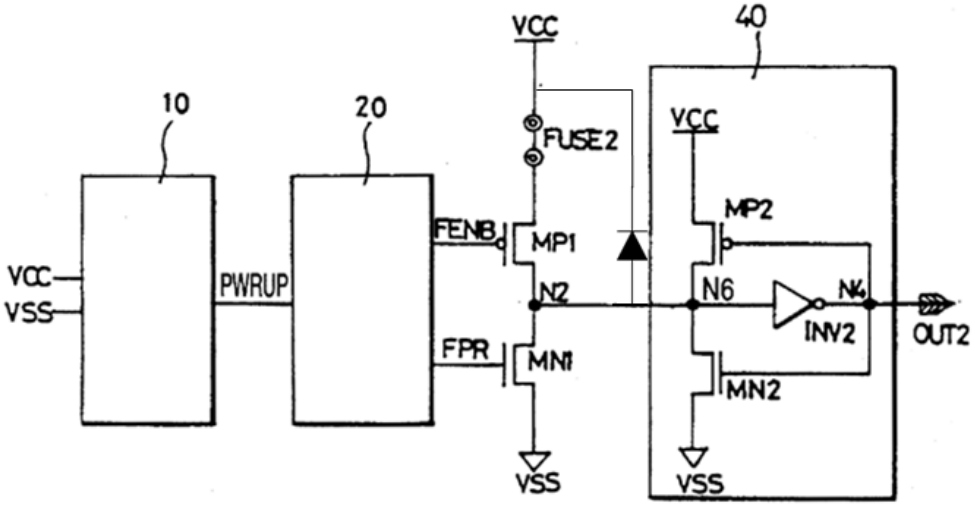
(Ex. 1009, 232 (FIG. 4.35) (annotated); Ex. 1002, ¶133.)

As shown in the demonstrative above, the highlighted body diode, which corresponds to the diode recited in claims 1 and 11, is formed by a p-n junction, where the p+ region is the drain of PMOS transistor MP1 and the n-type material is the n-well formed in the p-substrate. (Ex. 1002, ¶134; *See supra* Section IX.A.1(g).) A POSITA would have understood that transistors MP1 and MP2, both of which are PMOS transistors, would be formed in the same n-well. (Ex. 1002, ¶134.) A POSITA would also have understood that the PMOS transistor included in the inverter INV2 would also be constructed in the same n-well. (*Id.*)

In an n-well process, the NMOS transistors are formed in the p-substrate, while the PMOS transistors are formed in an n-well. (Ex. 1009, 117-23.) For

example, Weste describes an n-well process where "[t]he first mask defines the n-well (or n-tub); p-channel transistors will be fabricated in this well." (*Id.,* 118; Ex. 1002, ¶135.) While more than one n-well can be included in the p-substrate, a POSITA would have recognized that the PMOS transistor in inverter INV2 and PMOS transistors MP1 and MP2 would logically be formed in the same n-well as, as illustrated in the annotated figure 2 below, they are located in close proximity in the circuit and share points of connectivity. (Ex. 1002, ¶135.) Moreover, a POSITA would have understood that having multiple n-wells for multiple transistors would require additional chip area as design rules only allow certain structures to be placed within a certain distance of an n-well, and including multiple n-wells would force the circuitry to be spread across a larger chip area. (*Id*.)

FIG.2



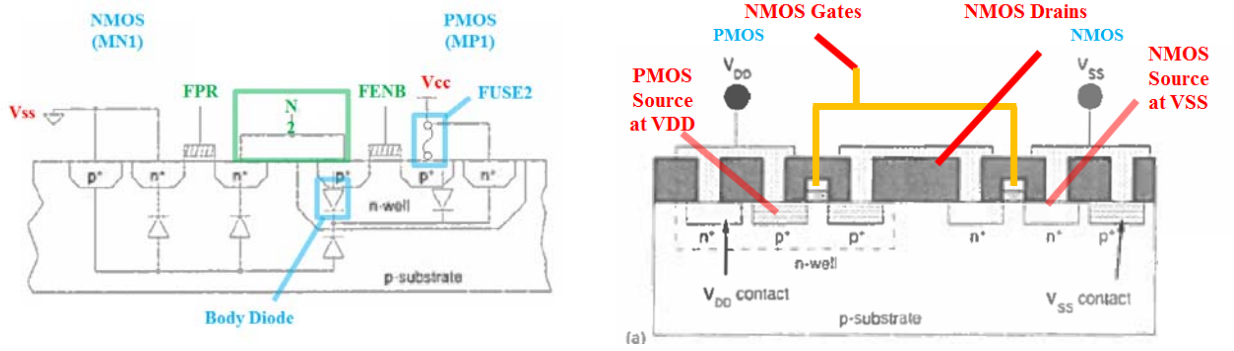
(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶135.)

Therefore, the diode includes a p-type region ("diode comprises a second semiconductor region of a second conductivity type") that forms a junction with the same n-well in which the PMOS transistor ("pull-up" device) of the inverter INV2 is formed ("forming a junction with the first semiconductor region"), where the p-type region ("second region") of the diode (i.e. the anode of the diode which corresponds to the drain of the PMOS transistor) is connected to the node N2 ("terminal T1"). (Ex. 1002, ¶136.) For at least these reasons, the Joo-Weste combination discloses or suggests "the diode comprises a second semiconductor region of a second conductivity type forming a junction with the first semiconductor region, the second region being connected to the terminal T1." (*Id*.)

8. Claim 12

a) The programmable latch of claim 11 wherein the MOS transistor is a PMOS transistor, the first conductivity type is type N, the second conductivity type is type P, and the first semiconductor region is to receive a positive voltage.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶¶137-138.) As discussed above with respect to claim 11, a POSITA would have found it obvious to implement the inverter and diode in the Joo-Weste circuit according to the following layouts, where it is understood that the PMOS transistors would be formed in the same n-well. (Ex. 1002, ¶137; *See supra* Section IX.A.7.)



(Ex. 1009, FIG. 4.35 (annotated), FIG. 3.9 (annotated); Ex. 1002, ¶137.)

As seen from the above layout, the MOS transistor (the PMOS transistor of the inverter INV2 shown on the right) is formed in the n-well ("first semiconductor region"), which is of conductivity type n ("the first conductivity type is type N"), the p+ region ("second semiconductor region") is of a conductivity type p ("the second conductivity type is type P"). (Ex. 1002, ¶138.) Moreover, as is evident from the demonstrative above, the n-well is tied to Vdd, which is a positive voltage in the Joo-Weste circuit ("the first semiconductor region is to receive a positive voltage"). (*Id.*) A POSITA would have understood that the n-well is tied to the highest voltage in the circuit to ensure proper operation of the circuit. (*Id.*; Ex. 1009, 122-23.)

9. Claim 13

a) The programmable latch of claim 1 wherein: said predetermined range consists of all voltages below a predetermined value; and

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶139.) As discussed above with respect to claim element 1[g], the Joo-Weste combination discloses "a diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch." (*See supra* Section IX.A.1(g).) Specifically, a POSITA would have understood that when V_{CC} is at a low voltage as shown in figure 3 of Joo (i.e., "before power is supplied to the latch"), the diode in the combined Joo-Weste circuit would not allow the voltage at node N2 to exceed that low voltage by more than a threshold voltage of the diode. (Ex. 1002, ¶139.) Therefore, the Joo-Weste combination discloses or suggests that the "predetermined range consists of all voltages below a predetermined value" where the predetermined value is the threshold voltage of the diode. (Ex. 1002, ¶139.)

b) when the programmable element is conductive, the variable-impedance path is non-conductive.

Joo in view of Weste discloses or suggests this feature. (Ex. 1002, ¶140.) As discussed above in claim element 1[a], if the fuse in Joo is not blown ("programmable element is conductive") when power is applied to the circuit, the node N2 follows the power supply Vcc, which results in the voltage on OUT2 shifting to a low level. (Ex. 1010, 3:44-57; *see supra* Section IX.A.1(a).) The low voltage on OUT2 is fed back to the gate of transistor MN2 and holds that transistor in the off state ("the variable-impedance path is non-conductive"). (Ex. 1002,

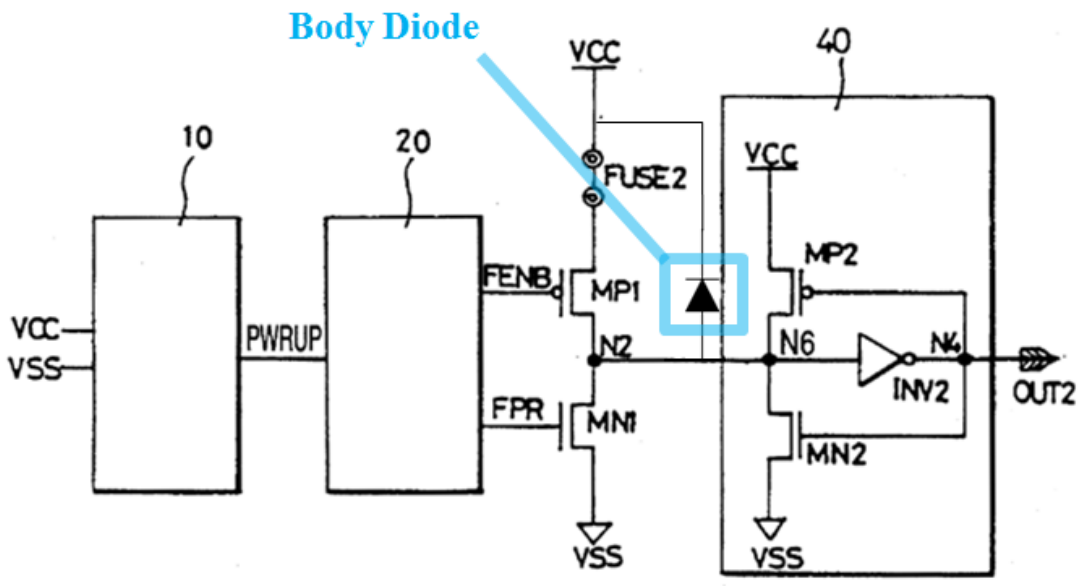
¶140.) The inclusion of the diode in the circuit of Joo based on Weste does not alter this aspect of the operation of the fuse circuit in Joo. (*Id*.) Therefore, the Joo-Weste combination discloses or suggests that the "when the programmable element is conductive, the variable-impedance path is non-conductive." (*Id*.)

B. Ground 2: Joo, Weste, and Keeth Render Obvious Claims 1, 2, 4-8, and 10-13

1. Claims 1, 2, 4, 8, and 10-13

As demonstrated above in Section IX.A.1, Joo in view of Weste discloses or suggests all of the features of claim 1. For example, as discussed above, the circuit of figure 2 of the Joo-Weste combination includes a body diode that functions in a manner similar to diode 234 in figure 2 of the '492 patent. (Ex. 1002, ¶142; *Supra* Section IX.A.1(g).) Therefore, for the same reasons that the '492 patent discloses a "diode for keeping a voltage on the terminal T1 within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch," the Joo-Weste combination also discloses or suggests this limitation. (*Id.*)

FIG.2



(Ex. 1010, FIG. 2 (annotated to provide a non-limiting illustration of the Joo-Weste combination); Ex. 1002, ¶142.)

However, to the extent that Patent Owner disputes this similarity by arguing that the Vcc terminal (and hence the cathode of the body diode highlighted above) in the Joo-Weste combination is not disclosed as being at the ground voltage like the VINT terminal coupled to the cathode of the diode 234 in the '492 patent (*see* Ex. 1001, FIG. 2A, 3:35-36), it would have been obvious in view of Keeth to make the voltage on the Vcc terminal in the Joo-Weste combination 0V (i.e. ground) when power is not supplied to the circuit. (Ex. 1002, ¶¶143-152.) Specifically, as discussed below, a POSITA would have been motivated to provide the Vcc voltage

(as shown in the Joo-Weste demonstrative above) from a power supply circuit such as that disclosed in Keeth, where, as also disclosed in Keeth, the power supply circuit would maintain the Vcc node in the Joo-Weste combination at ground when power is not supplied to the circuit. (*Id*.)

At the time of the alleged invention of the '492 patent, it was common for memory devices to include an internal power supply generator that would generate an internal power supply from an external voltage supply. (Ex. 1002, ¶144; Ex. 1008, 1:17-35 (explaining that an integrated circuit memory (e.g., a DRAM) "conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts" that is then converted to an internal voltage V_{CCR}); Ex. 1012, 1:19-23 ("by installing on-chip an internal power-supply voltage supplier, regardless of the external power-supply voltage a constant voltage is applied to the interior of the memory device.").) When implementing the Joo-Weste combination, a POSITA would have understood that Joo does not expressly disclose details regarding how the voltage supply (Vcc) is generated in Joo's figure 2 circuit. (*Id.*, ¶¶144.) But because Joo discloses a semiconductor memory device (Ex. 1010, 2:48-50 ("FIG. 2 illustrates a circuit of a semiconductor memory device having a fuse ROM in accordance with the present invention.")), a POSITA would have understood that the Vcc voltage in figure 2 of Joo could be provided from an internal power-supply generator. (Ex. 1002, ¶144.) Therefore, a POSITA looking to implement the Joo-

Weste combination would have looked to references that disclose an internal power-supply generator. (*Id.*)

A POSITA would have therefore looked to Keeth because, as discussed below, Keeth discloses an internal power-supply generator for a memory device and also explains how its novel internal power-supply generator overcomes several problems of conventional designs for such circuits. (Ex. 1002, ¶144.) Like Joo, Keeth relates to memory circuits. (*See e.g.,* Ex. 1008, 1:11-60; Ex. 1002, ¶145.) Keeth discloses that an integrated circuit memory (e.g., a DRAM) "conventionally accepts an externally applied power signal (V_{CCX}) on one of its contacts." (Ex. 1008, 1:17-19.) This externally applied voltage (V_{CCX}) is converted by a power supply circuit to "an internal voltage V_{CCR}," which is used as the power supply for the memory circuits. (*Id.,* 1:31-34, Abstract ("internal operating voltage, designated V_{CCR}"), 6:19 ("Signal V_{CCR} . . . powers circuit 30," where circuit 30 includes DRAM, SRAM, etc. (*id.,* 4:12-22).) But the conventional power supply circuits for converting an external power supply voltage to an internal power supply voltage suffered from several problems. (*Id.,* 1:31-60.)

To overcome these deficiencies, Keeth discloses a novel circuit (voltage reference 100) in FIG. 3 that receives power signal V_{CCX} and provides the internal power supply voltage V_{CCR}. (*See, e.g., id.,* 5:58-62, FIG. 3; Ex. 1002, ¶146.) The voltage reference 100 achieves a "piecewise linear relationship between V_{CCX} and

V_{CCR}" that alleviates shortcomings of similar prior art circuits. (Ex. 1008, 4:37-5:62.) Specifically, the voltage reference 100 operates over three segments (i.e., three ranges of input values for V_{CCX}) and "[w]hen used in a dynamic random access memory integrated circuit, operation in the first segment provides data retention at low power consumption. Operation in the second segment supports speed grading individual devices with a margin for properly stating memory performance specifications. Operation in the third segment supports screening at elevated temperatures for identifying weak and defective memory devices." (*Id.,* Abstract, 4:37-5:62.) According to Keith, the voltage reference 100 prevents the "useful life of the IC" from being shortened, increases "[s]ystem reliability," and allows "improved integrated circuit testing and screening." (*Id.,* Abstract, 4:37-5:62; Ex. 1002, ¶146.)

The voltage reference 100 is shown in FIG. 3 of Keith. (Ex. 1002, ¶147.)

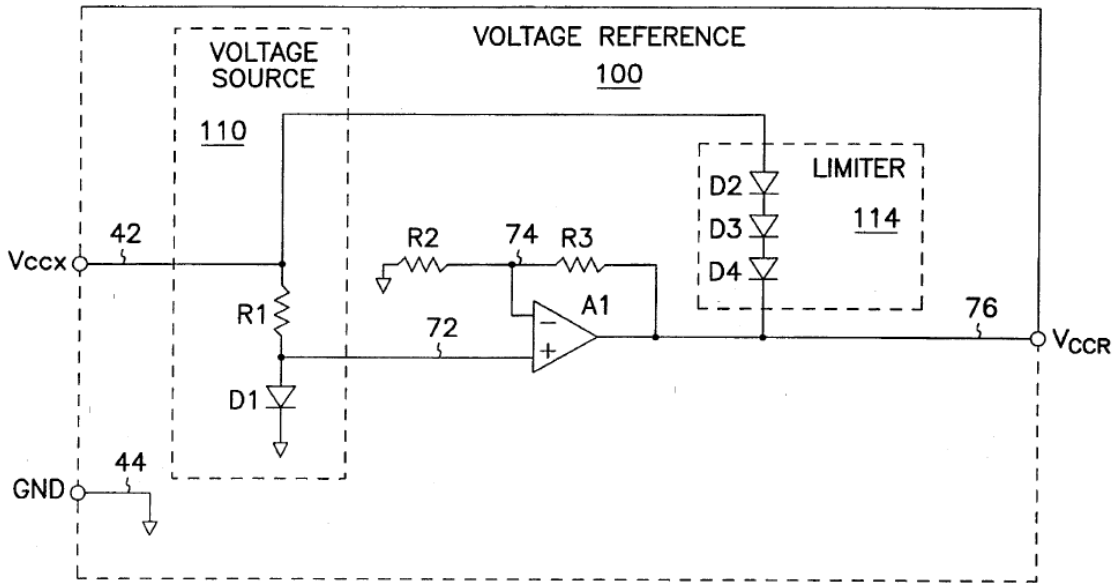


FIG. 3

(*Id.*, FIG. 3.)

Given the above-noted advantages associated with the voltage reference 100, a POSITA would have been motivated to combine the teachings of Joo, Weste, and Keeth such that the power supply Vcc in figure 2 of Joo is provided by a circuit similar to voltage reference 100, which receives an external power supply V_{CCX} and converts it to an internal power supply voltage V_{CCR}. (Ex. 1002, ¶¶148-152.) When implementing the Joo-Weste system, a POSITA would have looked to teachings associated with internal power supply circuits, such as those disclosed by Keeth, given that Joo does not expressly disclose details of the voltage supplies used therein. (*Id.*, ¶148.) Having looked to Keith, a POSITA would have found it obvious to combine its teachings with the Joo-Weste combination because, *inter*

alia, the voltage reference 100 prevents the "useful life of the IC" from being shortened, increases "[s]ystem reliability," and allows "improved integrated circuit testing and screening." (*Id.*; Ex. 1008, Abstract, 4:37-5:62.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 424 (2007) ("the proper question to have asked was whether a pedal designer of ordinary skill, facing the wide range of needs created by developments in the field of endeavor, would have seen a benefit to upgrading Asano with a sensor").

Indeed, the combination of Keith's voltage reference 100 and the Joo-Weste combination would have been nothing more than the combination of familiar elements (e.g. the voltage reference 100 of Keeth and the Joo-Weste memory device) according to known methods (providing an electrical connection between the Vcc node in Joo's figure 2 circuit and the V_{CCR} node in the voltage reference 100) that yields an expected result (the power supply in the Joo-Weste combination is provided by the voltage reference 100 of Keeth) and therefore, obvious to one of ordinary skill in the art. (*Id.*, ¶149.) *KSR*, 550 U.S. at 416.

The combined Joo-Weste-Keeth system discloses or suggests claim 1. (*Id.*, ¶¶150-152.) Specifically, as discussed above and as shown in the demonstrative

below, the Vcc terminal would be connected to the V_{CCR} terminal in figure 3 of Keeth that is further connected to the ground terminal through a resistor network R2, R3. (Ex. 1008, FIG. 3; Ex. 1002, ¶150.)

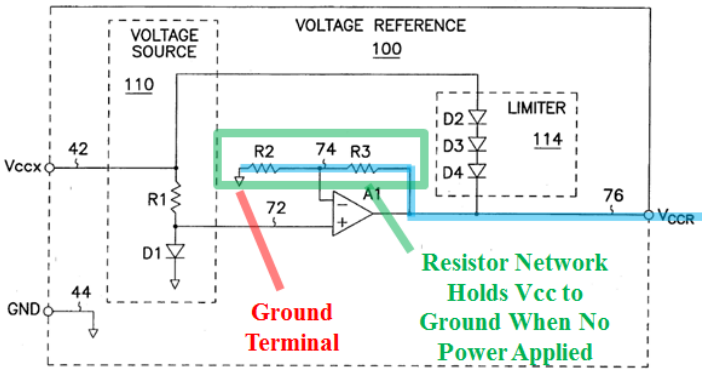
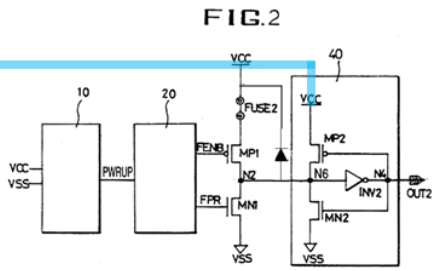


FIG. 3



(Ex. 1008, FIG. 3 (annotated); Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶150 (illustrating a non-limiting configuration of the Joo-Weste-Keeth combination).)

Accordingly, when power is not supplied to the resulting circuit in the Joo-Weste-Keeth combination (i.e., a positive external power supply signal Vccx is not provided to the circuit), the Vcc node (highlighted in blue) coupled to the diode in the latch circuit shown above will be at ground (0V). (Ex. 1002, ¶151.) Therefore, the body diode in the Joo-Weste-Keith combination will discharge the node N2 to a voltage no greater than one threshold voltage of the diode above ground (0V) in a similar manner as diode 234 in figure 2a of the '492 patent. (*Id.*; *see* Ex. 1001, 3:33-49.) As discussed above in section IX.A.1(g), the resulting circuit in the Joo-Weste-Keeth therefore includes "a diode for keeping a voltage on the terminal T1

within a predetermined range of values before power is supplied to the latch, to prevent the latch from assuming an incorrect state when power is supplied to the latch" that operates in a similar manner as the diode 234 in the '492 patent. (Ex. 1002, ¶151.)

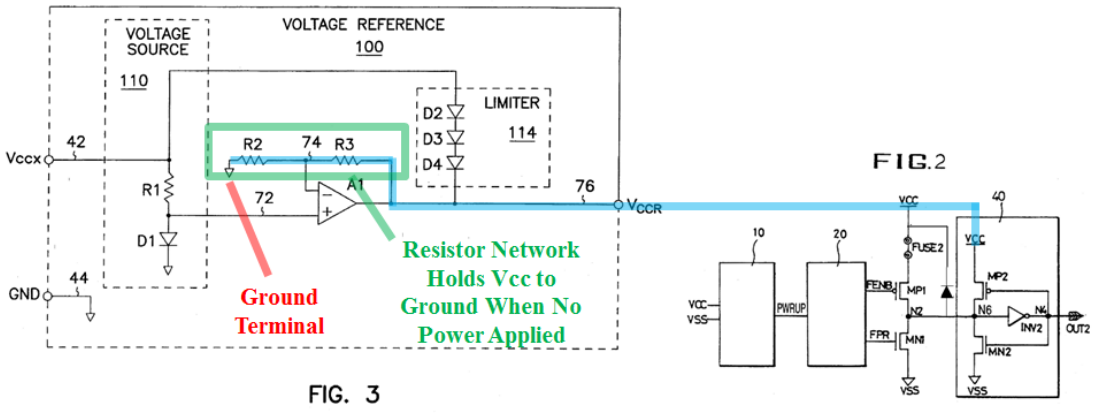
The addition of the power supply circuit of Keeth does not affect the operation of the Joo-Weste combination that discloses or suggests the remainder of claim 1 or that discloses or suggests the operation of claims 2, 4, 8, and 10-13. (*Id.*, ¶152.) For at least these reasons, claims 1, 2, 4, 8, and 10-13 are rendered obvious by Joo in view of Weste and Keeth.

2. Claim 5

a) The programmable latch of claim 1 in combination with a first electrical path interconnecting a first terminal of the diode and a ground terminal, wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode, but when the power is off the first terminal of the diode is discharged through said first electrical path.

Joo in view of Weste and Keeth discloses or suggests this feature. (Ex. 1002, ¶¶153-156.) As explained above with respect to claim 1 in Section IX.B.1, the Joo-Weste-Keeth combination discloses or suggests the features of claim 1. (*See supra* Section IX.B.1; Ex. 1002, ¶153.) Specifically, the Joo-Weste-Keeth combination discloses providing the VCC voltage to the programmable latch

circuit using an internal voltage generation circuit as shown in the demonstrative below. (Ex. 1002, ¶153.)



(Ex. 1008, FIG. 3 (annotated); Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶153 (illustrating a non-limiting configuration of the Joo-Weste-Keeth combination).)

As shown in the demonstrative above, the Joo-Weste-Keeth combination discloses a first terminal of the diode, namely the cathode which is connected to the VCC terminal, connected to the ground terminal (highlighted in red) via the resistor network that includes resistors R2 and R3 (highlighted in green). (Ex. 1002, ¶154.) Therefore, the Joo-Weste-Keeth combination discloses or suggests "a first electrical path interconnecting a first terminal of the diode and a ground terminal." (*Id.*)

The Joo-Weste-Keeth combination also discloses or suggests "wherein during normal operation the first terminal of the diode is charged to a voltage that turns off the diode." (*Id.*, ¶155.) As disclosed by Joo, during normal operation

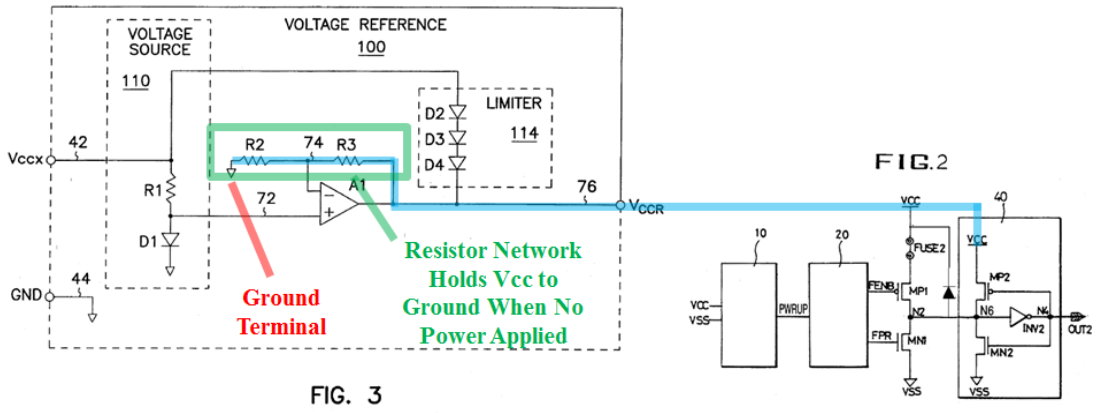
(e.g. when power is supplied to the fuse circuit), Vcc is at a high voltage level. (Ex. 1010, 2:51-53, 3:15-17, 3:36-40, FIG. 3.) As discussed above with respect to claim 4, when the voltage at the cathode of the diode is high during normal operation, the diode is off as the anode of the diode is either low or high depending on the state of the fuse. (*See supra* Section IX.A.3.) As such, the Joo-Weste-Keeth combination discloses or suggests that during normal operation the cathode of the diode ("first terminal of the diode") is charged to high voltage ("is charged to a voltage that turns off the diode"). (Ex. 1002, ¶155.)

Additionally, as discussed above, when the power is off in the Joo-Weste-Keeth combination, the Vcc node remains connected to ground via the "first electrical path" highlighted in blue in the demonstrative above. Because the Vcc node is grounded and the cathode of the diode is coupled to Vcc, the first terminal of the diode (i.e., the cathode of the diode) will be discharged to ground through the electrical path (highlighted in blue above) when the power is off. (*Id.*, ¶156.) Therefore, the Joo-Weste-Keeth combination also discloses or suggests that "when the power is off the first terminal of the diode is discharged through said first electrical path" as recited in claim 5. (*Id.*)

3. Claim 6

a) The combination of claim 5 wherein the first electrical path is a resistor or a resistor network.

The combined Joo-Weste-Keeth system discloses or suggests this limitation. (Ex. 1002, ¶157.) As discussed above in claim 5, in the modified system the disclosed "first electrical path" includes resistors R2 and R3, and thus includes "a resistor or a resistor network." (*See supra* Section IX.B.2.)



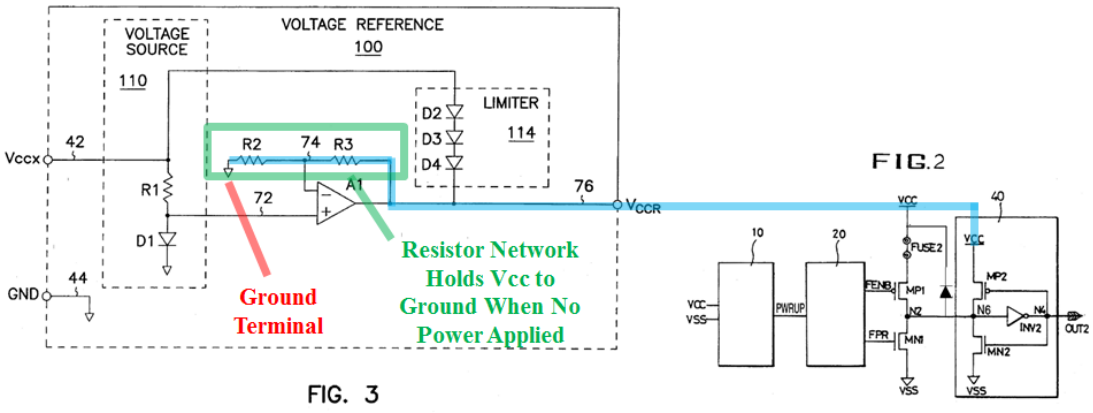
(Ex. 1002, ¶157 (illustrating a non-limiting configuration of the Joo-Weste-Keeth combination).)

4. Claim 7

a) The combination of claim 5 wherein the first electrical path is part of a reference voltage generator whose output is connected to the diode's first terminal.

The combined Joo-Weste-Keeth system discloses or suggests this limitation. (Ex. 1002, ¶158.) As discussed above with respect to claims 1 and 5, the modified system discloses or suggests that the output V_{CCR} of voltage reference 100 ("reference voltage generator") is connected to the cathode of the diode ("the diode's first terminal") in the Joo-Weste-Keeth combination. (*See supra* Sections

IX.B.1-2.) Therefore, the "first electrical path" (annotated in blue below) is part of a reference voltage generator (voltage reference 100). (Ex. 1002, ¶158.)



(Ex. 1002, ¶158 (illustrating a non-limiting configuration of the Joo-Weste-Keeth combination).)

C. Ground 3: Joo, Weste, and Tomishima Render Obvious Claim 9

As discussed above in Ground 1, claim 9 is obvious in view of Joo and Weste. (*See supra* Section IX.A.5.). However, to the extent Patent Owner contends or the Board finds that the Joo-Weste combination does not disclose or suggest that the Vcc terminal of the combined Joo-Weste circuit is received "from an external pin of the integrated circuit" as recited in claim element 9[b], such a feature would have been obvious in further view of Tomishima as demonstrated below. (Ex. 1002, ¶¶159-169.)

1. Claim 9

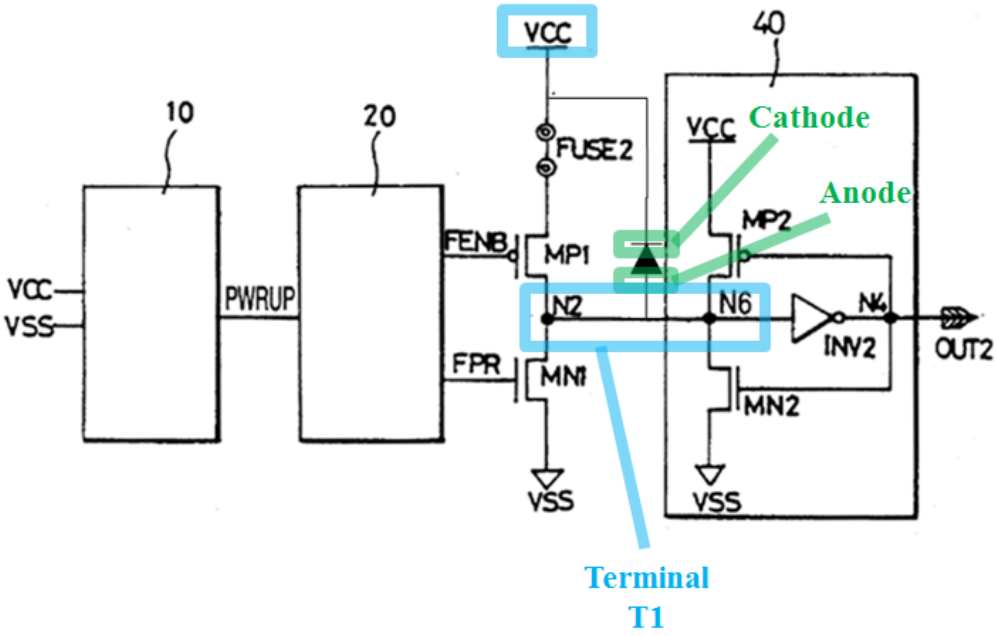
a) The programmable latch of claim 1 wherein the latch is an integrated circuit or a part of an integrated circuit,

As discussed above in Section IX.A.5(a), the Joo-Weste combination discloses or suggests this feature because the combined Joo-Weste circuit is used in an integrated circuit device such as a memory device. (*See supra* Section IX.A.5(a); Ex. 1002, ¶159;)

> b) wherein the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit.

As discussed above in Section IX.A.5(b), the Joo-Weste combination discloses or suggests this feature. (*See supra* Section IX.A.5(b).) However, to the extent Patent Owner contends or the Board finds that the Joo-Weste combination does not disclose or suggest that the Vcc terminal of the combined Joo-Weste fuse circuit shown below ("programmable latch") is received "from an external pin of the integrated circuit" as recited in claim element 9[b], it would have been obvious in view of Tomishima (Ex. 1013) to configure the combined Joo-Weste fuse circuit to receive the power supply Vcc from an external pin of the integrated circuit. (Ex. 1002, ¶¶161-169.)

FIG.2



(Ex. 1010, FIG. 2 (annotated); Ex. 1002, ¶161.)

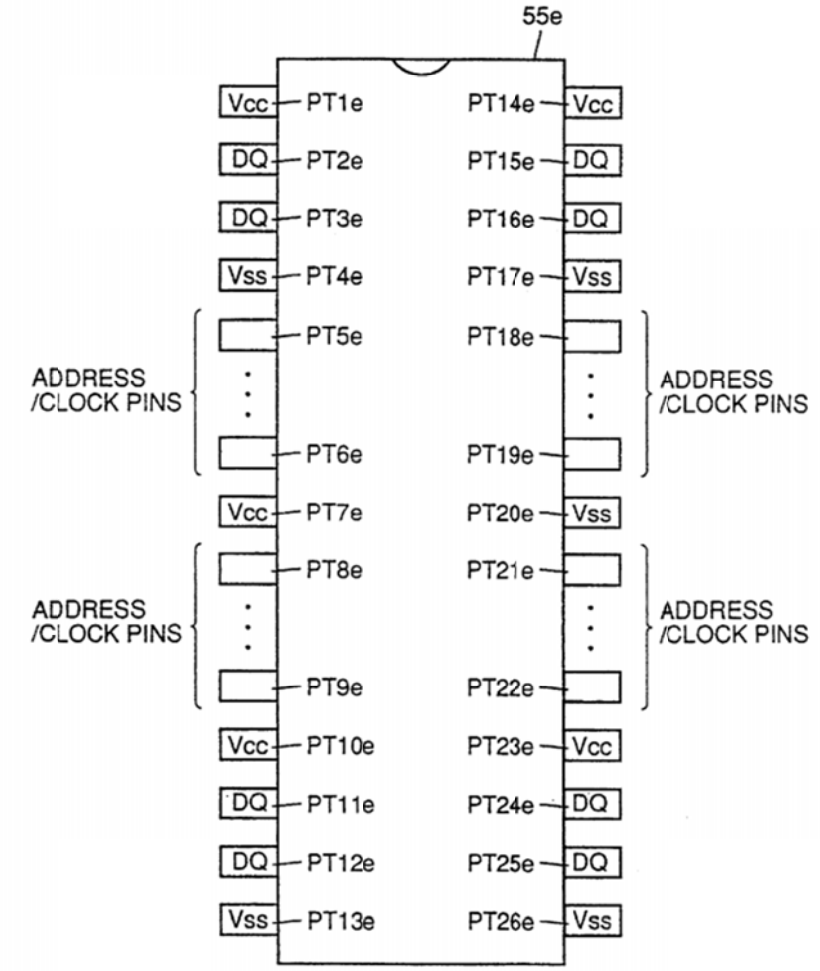
As discussed above in Section IX.C.1(a), the combined Joo-Weste circuit is implemented in an integrated circuit. (*See supra* Section IX.C.1(a).) A POSITA would have understood that it was common practice for the integrated circuit device to receive power on an external pin of the integrated circuit and for the circuits inside the integrated circuit to use the received power either directly from the pin or through an intermediate circuit (e.g., an internal power supply generator). (*See supra* Section IX.A.5(b); *see supra* Section IX.B.1; Ex. 1002, ¶163.) Indeed, providing power to integrated circuits using external pins was so routine and well-known to a POSITA, that a patent such as Joo did not provide specifics as to the

origin of the power supply inside the chip (e.g., Vcc in figure 2 of Joo). (Ex. 1002, ¶163.) As demonstrated below, Tomishima discloses specifics as to an integrated circuit device receiving the power supply voltage on an external pin, thereby demonstrating that receiving power from an external pin was within the knowledge of a POSITA at the time of the alleged invention of the '492 patent. As also discussed below, a POSITA would have been motivated to provide the Vcc voltage (as shown in the Joo-Weste demonstrative above) from a power supply pin such as that disclosed in Tomishima. (*Id.*, ¶¶163-169.)

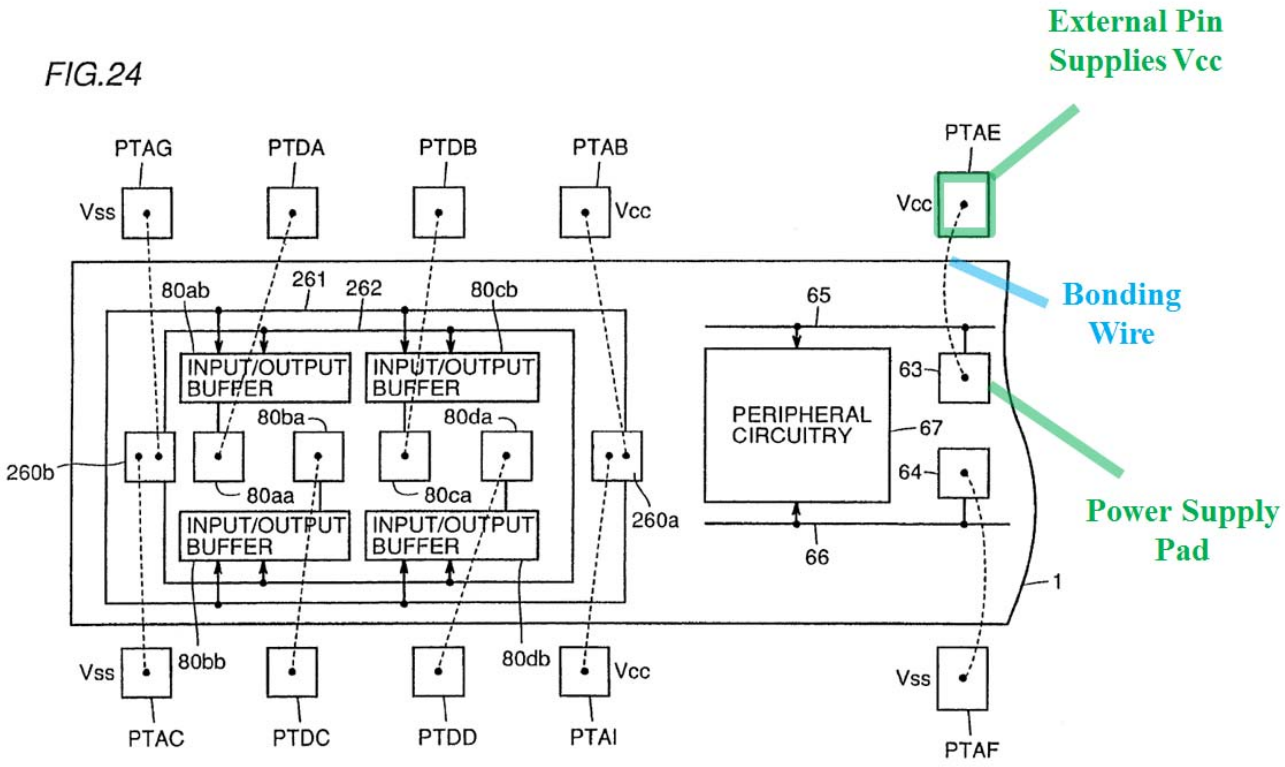
Like Joo, Tomishima relates to memory circuits. (*See e.g.,* Ex. 1013, 1:12-19; Ex. 1002, ¶164.) Tomishima discloses that in an integrated circuit memory (e.g., a DRAM), a center region is conventionally designed to have "pads for receiving external power supply voltage and ground voltage and for input/output of signals." (Ex. 1013, 1:31-35.) Tomishima discloses that such a configuration, however, does not allow all structures in the memory device to operate stably at high speed. (*Id.,* 2:40-41.) To overcome these deficiencies, Tomishima discloses a specific arrangement of power supply pads that receive power from a source external to the integrated circuit. (*Id.,* 4:6-14; Ex. 1002, ¶164.)

An example configuration of external power supply pins is shown below in figure 23 of Tomishima. (Ex. 1002, ¶165)

FIG.23



(Ex. 1013, FIG. 23.) Tomishima explains that "power supply pin terminals and ground pin terminals are arranged on each respective side of package 55e." (*Id.,* 24:32-40.) "The voltages Vcc and Vss supplied to pin terminals PT7e and PT20e are used by peripheral circuitry operating on the signals received through address/clock pin terminals …." (*Id.,* 24:56-59.) Figure 24 of Tomishima, replicated below, shows an inner pad layout of the semiconductor memory device in the package of figure 23. (*Id.,* 6:21-22, 24:60-61; Ex. 1002, ¶165.)



(*Id.*, FIG. 24 (annotated); Ex. 1002, ¶165.)

As shown in figure 24 above, bonding wires (broken lines) are used to connect the power supply pins to power supply pads (e.g. 260a) on the integrated circuit memory device. (Ex. 1013, 24:65-25:1; Ex. 1002, ¶166.)

Given the above-noted disclosure associated with how Vcc is supplied to a memory device in Tomishima, a POSITA would have been motivated to combine the teachings of the Joo-Weste combination and Tomishima such that the power supply (Vcc) in the Joo-Weste combination is provided by an external pin of the integrated circuit. (Ex. 1002, ¶167.) Joo does not provide a specific disclosure as to how the power supply (e.g., Vcc) is configured for its memory device or from where the power supply is received. (*Id.*) Therefore, a POSITA would have

looked to teachings associated with external power supply connections, such as those disclosed by Tomishima so that Vcc in the Joo-Weste combination can be provided with the necessary voltage. (*Id.*; Ex. 1010, 3:15-17 ("[w]hen power is supplied to the circuit, the power source voltage is gradually stepped up until the level Vcc is reached").) Accordingly, a POSITA would have combined the teachings of the Joo-Weste combination and Tomishima because Tomishima explains how a power supply can be received by an external pin of an integrated circuit (e.g., the memory device including the combined Joo-Weste circuit) and such a power supply can be used to power circuits inside an integrated circuit. (Ex. 1002, ¶167; Ex 1013 at 24:56-59.) *See Unwired Planet*, 841 F.3d at 1003.

Indeed, using an external power supply received on an external pin of the integrated circuit in the Joo-Weste combination, based on Tomishima, would have been nothing more than the combination of familiar elements (receiving a power supply voltage Vcc in the Joo-Weste combination) according to known methods (using an external pin as in Tomishima to receive a power supply (e.g., Vcc)) that yields an expected result (a functional memory device that receives a power supply needed for operation) and therefore, obvious to one of ordinary skill in the art. (*Id.*, ¶168.) *KSR*, 550 U.S. at 416.

Therefore, for these reasons in addition to those presented above in Section IX.A.5(b), the Joo-Weste-Tomishima system discloses or suggests the features of

claim 9, including "the diode has one terminal connected to the terminal T1 and the diode has another terminal which is to receive a non-ground power supply voltage from an external pin of the integrated circuit." (Ex. 1002, ¶169.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1, 2 and 4-13 of the '492 patent based on the grounds specified in this petition.

Respectfully submitted,

Dated: March 5, 2019 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 contains, as measured by the word-processing system used to prepare this paper, 13,695 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 5, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,163,492 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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