Paper No. __
Filed: March 5, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PROMOS TECHNOLOGIES, INC.
Patent Owner

U.S. Patent No. 6,469,559

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,469,559

TABLE OF CONTENTS

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 6,469,559
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	Prosecution History of U.S. Patent No. 6,469,559
Ex. 1005	Prosecution History of U.S. Patent No. 6,339,354
Ex. 1006	Certified English Translation of Japanese Patent Publication JP2000-022510 to Ogiwara *et al.*("Ogiwara"), Japanese Language Version of JP2000-022510, and Translation Certificate
Ex. 1007	Dally, W. *et al.*, Digital Systems Engineering, 1998, including title page, copyright page, and chapters 4 and 12 ("Dally")
Ex. 1008	U.S. Patent No. 5,095,352 ("Noda")
Ex. 1009	Dunlop et al., "A Procedure for Placement of Standard-Cell VLSI Circuits," IEEE Transactions on Computer-Aided Design, Vol. Cad-4, No. 1, January 1985 ("Dunlop")
Ex. 1010	Declaration of Dr. Ingrid Hsieh-Yee
Ex. 1011	Taur *et al.*, Fundamentals of Modern VLSI Devices, 2009
Ex. 1012	U.S. Patent No. 5,459,422 ("Behrin")
Ex. 1013	First Amended Complaint dated November 21, 2018 in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al.*, No. 1:18-cv-00307-RGA (D. Del.)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-17 of U.S. Patent No. 6,469,559 ("the '559 patent") (Ex. 1001), which, according to PTO records, is assigned to ProMOS Technologies, Inc. ("Patent Owner"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC.

Related Matters: Patent Owner has asserted the '559 patent against Petitioner in *ProMOS Technologies, Inc. v. Samsung Electronics Co., Ltd., et al*., No. 1:18-cv-00307-RGA (D. Del.). Patent Owner has also asserted U.S. Patent Nos. 5,934,974; 6,099,386; 6,163,492; and 6,597,201 in this action. Petitioner is concurrently filing petitions challenging one or more claims in these patents.

Counsel and Service Information: Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Chetan R. Bansal (Limited Recognition No. L0667). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-

Samsung-ProMOS3-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.104(a)

Petitioner certifies that the '559 patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED UNDER 37 C.F.R. § 42.104(b)

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-17 ("challenged claims") of the '559 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable in view of the following ground:

Ground 1: Claims 5, 8, 12-14, and 16 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Japanese Patent Publication JP2000-022510

to Ogiwara et al. ("Ogiwara") (Ex. 1006)[1] and U.S. Patent No. 5,095,352 ("Noda") (Ex. 1008).

Ground 2: Claims 1-4, 6, 7, 9, 10, 11, 15, and 17 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Ogiwara (Ex. 1006) in view of Dally, W. et al., Digital Systems Engineering, 1998, ("Dally") (Ex. 1007) and Noda (Ex. 1008).

The '559 patent issued from U.S. Application No. 10/007,875 filed November 08, 2001, which claims priority to U.S. Application No. 09/542,511 filed on April 03, 2000. (Ex. 1001, Cover). Ogiwara (Exhibit 1006) was published on January 01, 2000, and thus is prior art to the '559 patent at least under pre-AIA 35 U.S.C. § 102(a).

Dr. Hsieh-Yee, an expert on library cataloging and classification, considered numerous facts relating to Dally (e.g., bibliographic and MARC records, a date stamp, and pre-filing date citations to Dally) and explains on the basis of such evidence that Dally was accessible to the public by October 22, 1998. (Ex. 1010, ¶24; *see also id.,* ¶¶12-23.) Additionally, Dr. Hsieh-Yee explains that several pre-

[1] Ex. 1006 is a compilation containing the English-language translation of Ogiwara (*id*., pp. 1-19), followed by its Japanese language version (*id*., pp. 20-38). The affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) follows the Japanese-language version.

critical-date publications cite to Dally, including one as early as March 1999. (*Id.*, ¶23.) Thus, Dally is prior art under pre-AIA 35 U.S.C. § 102(b).

Noda (Exhibit 1008) issued on March 10, 1992, and thus is prior art to the '559 patent under pre-AIA 35 U.S.C. § 102(b). None of Ogiwara, Dally, or Noda was considered by the Patent Office during prosecution of the '559 patent. (*See generally* Ex. 1001, References Cited.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the alleged invention of the '559 patent ("POSITA"), which for purposes of this proceeding is the late 1990s-early 2000s (including April 3, 2000) would have had a bachelor's degree in electrical engineering or a similar field, and at least two to three years of experience in integrated circuit design. (Ex. 1002, ¶¶20-21.) More education can supplement practical experience and vice versa. (*Id.*)[2]

VII. OVERVIEW OF THE '559 PATENT AND PRIOR ART

A. The '559 Patent

The '559 patent is entitled "System and Method for Eliminating Pulse Width Variations in Digital Delay Lines." (Ex. 1001, Cover.) Consistent with the title, the '559 patent relates to the "preservation of the width of pulses propagated

[2] Petitioner submits the declaration of R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '559 patent. (Ex. 1002, ¶¶5-14; Ex. 1003.)

through relatively long delay voltage controlled delay lines of particular utility in conjunction with delay locked loops ('DLL')." (*Id.,* 1:26-28; Ex. 1002, ¶¶36-44.) As disclosed by the '559 patent, such delay locked loops include "those utilized in double data rate ('DDR') dynamic random access memory ('DRAM') devices, processors and other integrated circuit ('IC') devices and semiconductor processes." (Ex. 1001, 1:29-32.)

The utility of variable delay lines in DLLs is recognized by the '559 patent as being well-known at the time of the alleged invention. (*Id.,* 1:22-45.) For example, the '559 patent recognizes in the Background of the Invention that it was known to use DLL circuitry to increase the bandwidth in DDR DRAMs. In such DRAMs, the DLL circuitry is used to achieve synchronization of data accesses to enable reading of data on both the rising and falling edge of each clock cycle. (*Id.,* 1:34-39.)

According to the '559 patent, figure 2 shows "a voltage controlled delay inverter circuit" that forms a portion of the voltage controlled delay line circuit used in a DLL. (*Id.,* 3:3-5.)

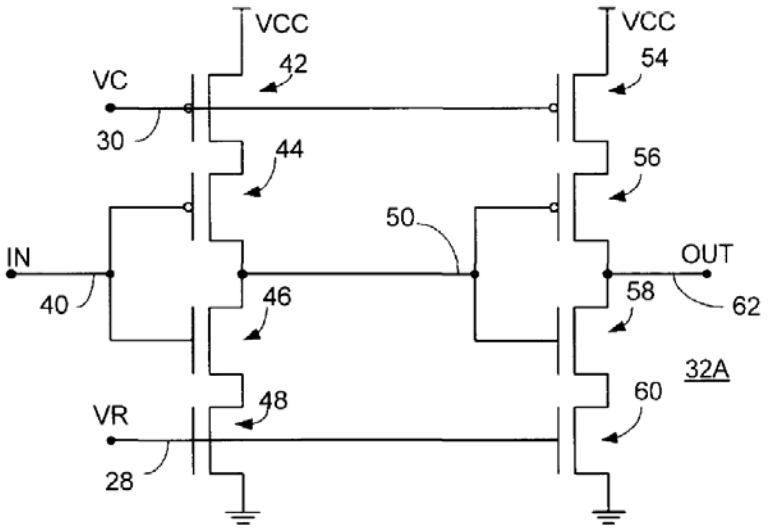


Fig. 2

(*Id.*, FIG. 2.)

The '559 patent acknowledges that the voltage controlled delay inverter circuit of figure 2 was known and used in prior art delay lines such as the delay line 32 illustrated in figure 3. (*Id.*, 3:3-7, 4:8-15, FIGs. 2-3.)

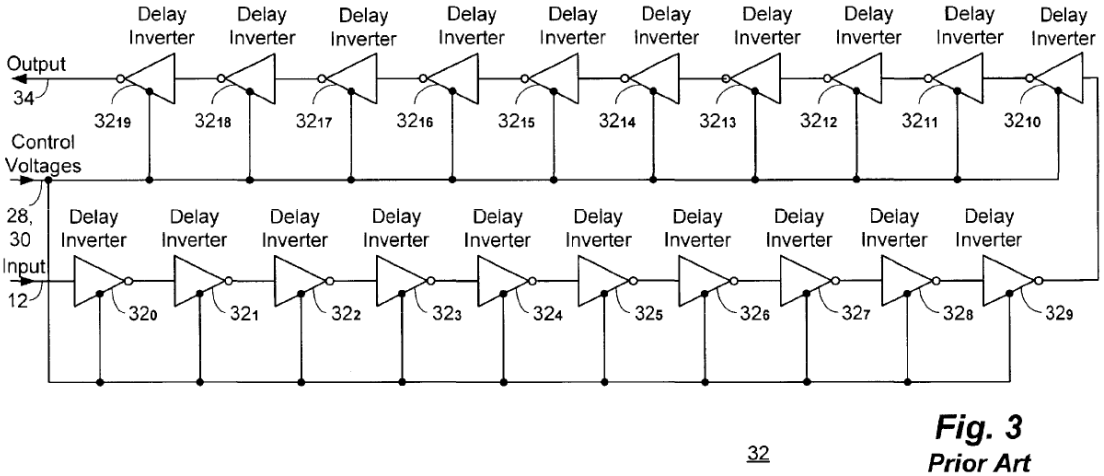
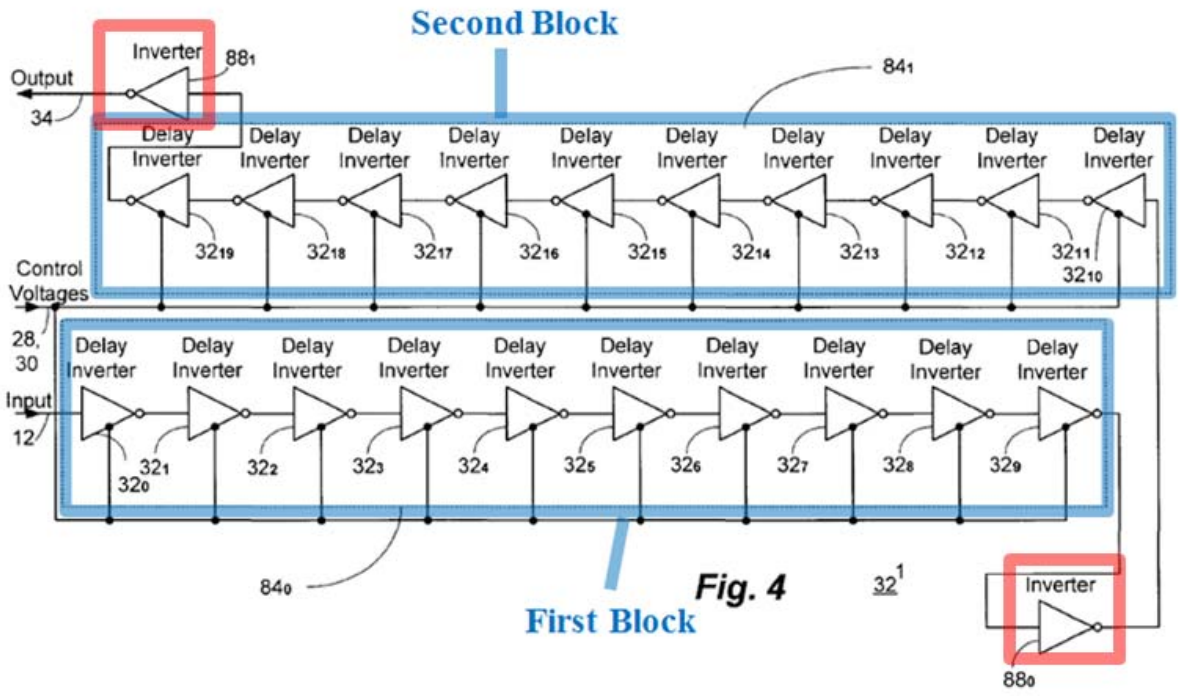


Fig. 3
Prior Art

(*Id.*, FIG. 3.)

As noted above, the ’559 patent is directed to ensuring that the width of a pulse going through the delay line is maintained. (*Id.,* 1:22-32, 1:56-57.) According to the ’559 patent, there are two ways to preserve the width of a pulse in such a delay line: “1) the propagation delays for both the rising inputs and falling inputs must be made identical for each individual inverter; or 2) the delay for rising edge inputs are made identical on an odd-even basis and the delay for falling edge inputs are made identical on an odd-even basis.” (*Id.,* 1:56-62.) The ’559 patent indicates that there are problems with both approaches, as the first is “very difficult to achieve because of the variations in the pull-up or pull-down devices” in the inverters and the second “requires that each odd-even pair of delay inverters be made identical and that the parasitic loading between all inverters also be the same.” (*Id.,* 1:64-2:2.)

The solution proposed by the ’559 patent is to modify the prior art delay line shown in figure 3 by partitioning the delay line into two substantially identical bocks of delay inverters with a first inverter being inserted between the two blocks and a second inverter being added at the output of the second block. (*Id.,* 2:11-15.) Annotated figure 4 of the ’559 patent below shows the first and second blocks of delay elements (e.g. inverters), with a first inverter 88_0 between the two blocks and a second inverter 88_1 at the output of the second block.



(Ex. 1001, FIG. 4 (annotated); Ex. 1002, ¶42.)

According to the '559 patent:

> Since the rising edge input to the first block becomes a falling edge input to the second block as it propagates through the delay line, the rising and falling input edges will encounter an identical set of transitions as they propagate through the two blocks. If the loading of the inverter at the output of the first block and that of the inverter at the output of the second block are identical, the pulse width will be perfectly preserved.

(Ex. 1001, 2:24-31.)

In other words, a rising edge transition entering the first block is inverted to become a falling edge transition that enters the second block and vice-versa. (Ex. 1002, ¶42.) Therefore both rising and falling edges of the signal being delayed will experience the same amount of delay even if there is a lack of balance between the delay applied to a rising edge versus a falling edge in an individual one of the delay blocks. (*Id.*)

The above features were well known as discussed below in Sections VII.B and IX. (Ex. 1002, ¶¶48-176; *see also id.*, ¶¶22-34.)

B. Ogiwara

Ogiwara relates to an "RC delay circuit formed in an integrated circuit having a MOS structure used, for example, in memory such as DRAM and SRAM." (Ex. 1006, ¶[0001]; Ex. 1002, ¶¶48-52.) Ogiwara indicates that because the PMOS and NMOS transistor thresholds can vary in opposite directions, the delay time through the delay circuit can vary, which is undesirable. (Ex. 1006, ¶¶[0042]-[0043].)

In order to address this problem, Ogiwara proposes to provide "an odd number of CMOS inverter circuit 13 stages between two delay circuits so that the direction in which second delay circuit 12 I/O signal logic levels transition is opposite the direction in which the first delay circuit 11 I/O signal logic levels

transition." (*Id.*, ¶[0068].) Ogiwara's first embodiment is depicted in figure 1 below.

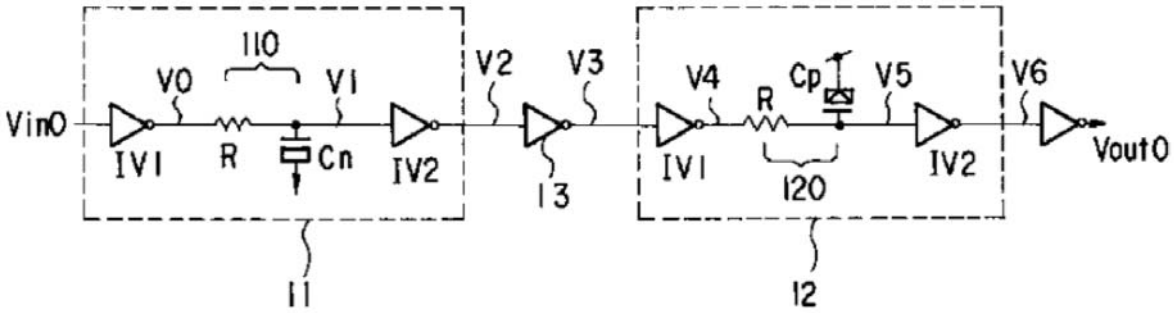


FIG. 1

(*Id.*, FIG. 1.)

As shown in figure 1 above, the "odd number of CMOS inverter circuit 13 stages" is shown as a single inverter 13 that is positioned between the first delay circuit 11 and the second delay circuit 12. (*Id.*, ¶ [0068], FIG. 1.) Ogiwara teaches that by inverting the signal being delayed after it has propagated through the first block of delay elements 11, any transitions in the signal provided to the second block of delay elements 12 will be in the opposite direction as compared to the corresponding transitions in the signal provided to the first block. (*Id.*, ¶¶ [0068], [0078].) As such, a rising edge that is input to block 11 will result in a falling edge being input to block 12 and vice versa. (*Id.*)

Ogiwara's second embodiment is shown in figure 4 below. (*Id.*, ¶ [0077], FIG. 4.)

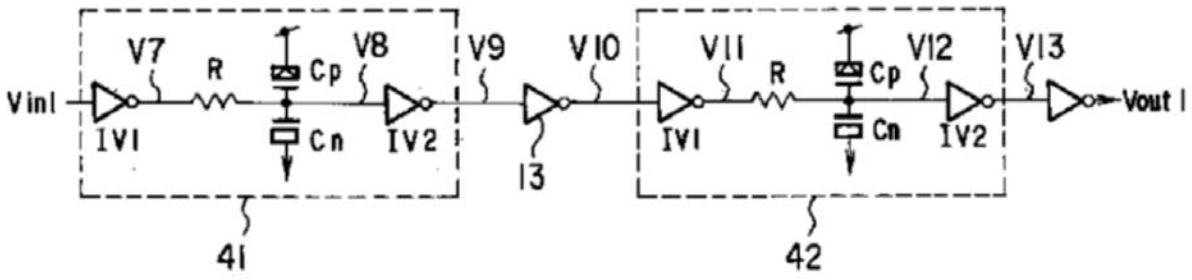


FIG. 4

(*Id.*, FIG. 4.)

The "RC delay circuit" of Ogiwara's second embodiment builds on Ogiwara's first embodiment shown in figure 1. (*Id.*, ¶[0078], FIGs. 1, 4.) Like the RC delay circuit depicted in figure 1, the RC delay circuit depicted in figure 4 of Ogiwara includes an inverter 13 between the delay circuits 41 and 42. (*Id.*, ¶¶ [0068], [0078].) According to Ogiwara, "in the second embodiment RC delay circuit, as in the first embodiment RC delay circuit, changes in the two delay circuit delay times cancel one another even if the threshold absolute values for the PMOS transistor and NMOS transistor included in the circuit vary in opposite directions, so that overall delay time variability can be minimized." (*Id.*, ¶[0087].)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a

POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.,* 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that, except for claim 6 below, no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[3] (Ex. 1002, ¶46.)

A. "means for varying the delay of the input signal"

Claim 6 recites, *inter alia*, "means for varying the delay of the input signal," which is a means-plus-function term under 35 U.S.C. §112(f). As discussed below,

[3] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '559 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

this claim term recites the function of "varying the delay of the input signal" where the corresponding structure is "voltage controlled delay inverter circuit."

According to the '559 patent, the variable delay line of figure 4 has "delay inverters 32_0 through 32_9 and 32_{10} through 32_{19}" where each of the delay inverters "may be formed in accordance with the configuration of the delay inverter 32A shown in FIG. 2." (Ex. 1001, 4:46-55.) The delay inverter 32A is a "voltage controlled delay inverter circuit." (*Id.,* 3:42-46.) A POSITA would have understood that a voltage controlled delay inverter circuit varies the delay of the input signal provided to the inverter input. (Ex. 1002, ¶47.) Accordingly, the corresponding structure for "means for varying the delay of the input signal" in the '559 patent is a "voltage controlled delay inverter circuit or equivalents thereof." (*Id*.)

IX. DETAILED EXPLANATION OF GROUNDS

As detailed below, the challenged claims are unpatentable based on Grounds 1 and 2. (Ex. 1002, ¶¶57-176.)

A. Ground 1: Ogiwara and Noda Render Obvious Claims 1, 5, 8, 12-14, and 16

1. Claim 5

a) A delay line for delaying an input signal between input and output lines thereof, the delay line comprising:

To the extent the preamble is limiting, Ogiwara discloses this feature. (Ex. 1002, ¶¶59-65.) For example, Ogiwara's second embodiment discloses an "RC delay circuit" that is shown in figure 4 below. (Ex. 1006, ¶ [0077], FIG. 4.)

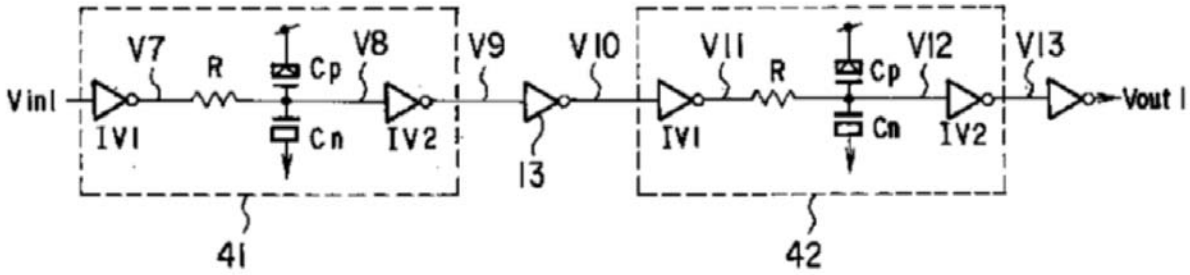


FIG. 4

(*Id.*, FIG. 4.)

The "RC delay circuit" of Ogiwara's second embodiment builds on a similar circuit in Ogiwara's first embodiment that is shown in figure 1 below. (*Id.*, ¶[0078], FIGs. 1, 4.)

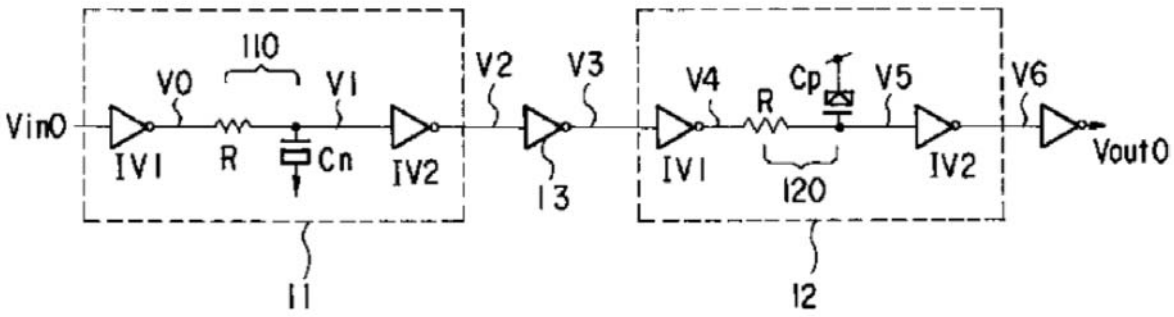


FIG. 1

(*Id.,* FIG. 1.)

According to Ogiwara, the difference between the first and second embodiments depicted in figures 1 and 4, respectively, is that the delay circuits 41 and 42 in figure 4 include additional capacitors in comparison to the delay circuits 11 and 12 of figure 1. (*Id.*, ¶[0078].) Specifically, figures 1 and 4 are the same except that in figure 4, both delay circuits (i.e., 41 and 42) include the same capacitor combination of Cp and Cn. (*Id.,* FIGS. 1, 4.) Therefore, much of Ogiwara's description of the first embodiment of figure 1 is also applicable to the description of the second embodiment depicted in figure 2. (Ex. 1002, ¶62.)

Like the RC delay circuit depicted in figure 1, the RC delay circuit depicted in figure 4 of Ogiwara includes delay circuits "connected in series via an odd number (in this example, one) of stages of a CMOS inverter circuit 1." (Ex. 1006, ¶¶ [0050], [0078].) The output Vout1 of the "RC delay circuit" of figure 4 is a delayed version of input signal Vin1. (*Id.*, Figs. 4, 5(a), ¶ [0079].) Therefore, as

illustrated in annotated figure 4 below, the RC delay circuit of figure 4 forms a "delay line," where the delay line delays the input signal Vin1 between the input and output lines of the delay line ("delay line for delaying an input signal between input and output lines thereof"). (Ex. 1002, ¶¶63-65.)

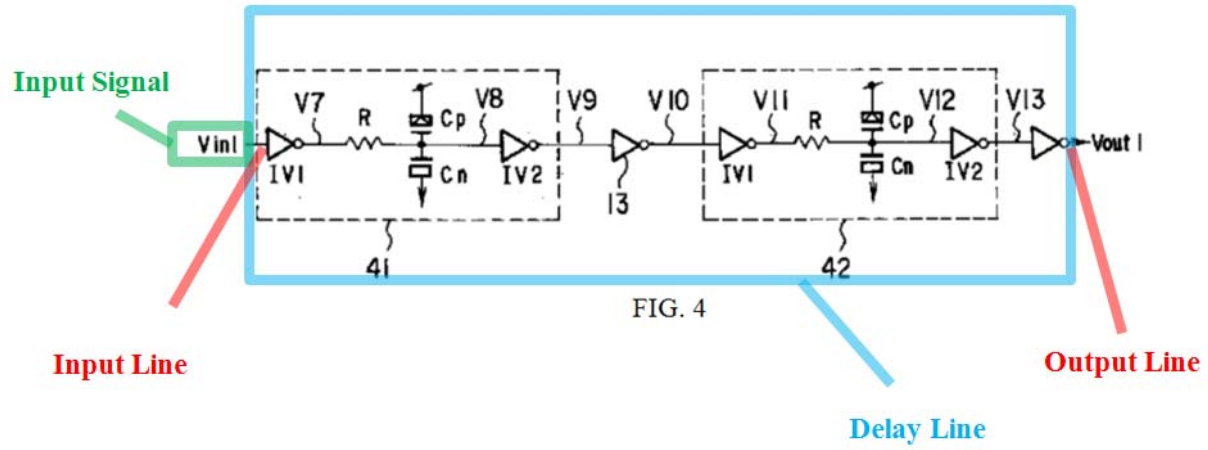


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶65.)

b) first and second blocks of delay elements coupled to receive said input signal on said input line,

Ogiwara discloses this feature. (Ex. 1002, ¶¶66-67.) The "delay line" of figure 4 includes a first delay circuit 41 ("first block of delay elements") and a second delay circuit 42 ("second block of delay elements"), where the "delay elements" in each of the blocks include a first delay element, inverter IV1, and a second delay element, the combination of the RC circuit (R, Cp, and Cn) with inverter IV2. (Ex. 1006, ¶¶ [0051], [0078], FIG. 4.)

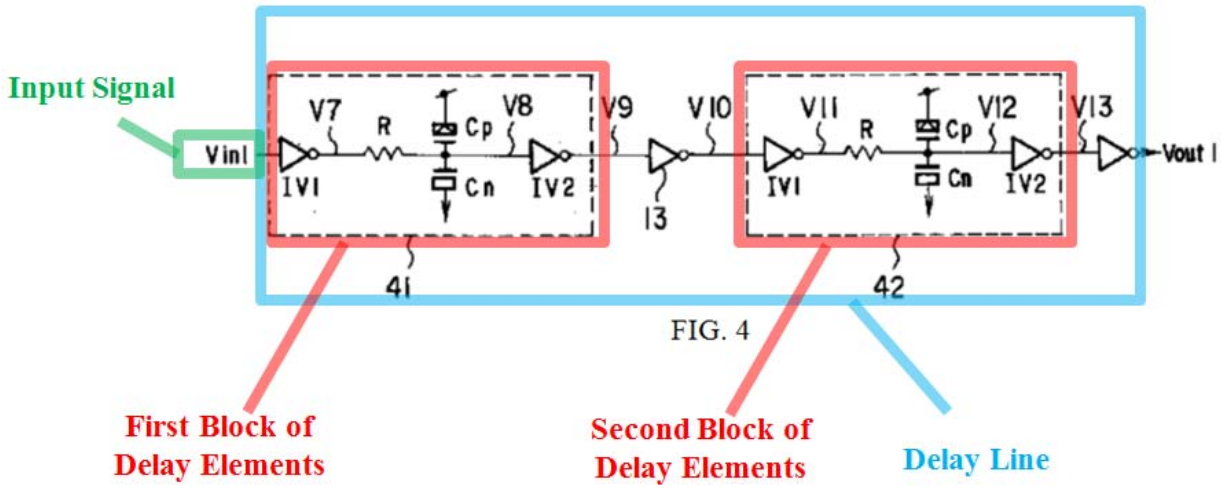


FIG. 4

(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶66.)

The first delay circuit 41 is coupled in series with the second delay circuit 42, and the input signal Vin1 is provided to the input of the first delay circuit 41. (Ex. 1006, ¶¶ [0050], [0078], FIG. 4.) Therefore, Ogiwara discloses "first and second blocks of delay elements coupled to receive said input signal on said input line." (Ex. 1002, ¶67.) Indeed, Ogiwara's delay circuits 41 and 42 are coupled to input signal Vin1 in the same manner that blocks 84_0 and 84_1 are coupled to the input signal 12 in figure 4 of the '559 patent. (*Id.*; Ex. 1001, FIG. 4.)

c) wherein the propagation delay of individual delay elements in each of said first and second blocks is at least partially unequal and

Ogiwara discloses this feature. (Ex. 1002, ¶¶68-79.) As explained in detail below, in each of the delay circuits 41 and 42 ("said first and second blocks"), the propagation delay of the first delay element, (i.e., inverter IV1), is different than

the propagation delay of the second delay element (i.e., the combination of the RC circuit that includes R, Cp, and Cn with IV2). Therefore, Ogiwara discloses that "the propagation delay of the individual delay elements in each of the first and second blocks is at least partially unequal."

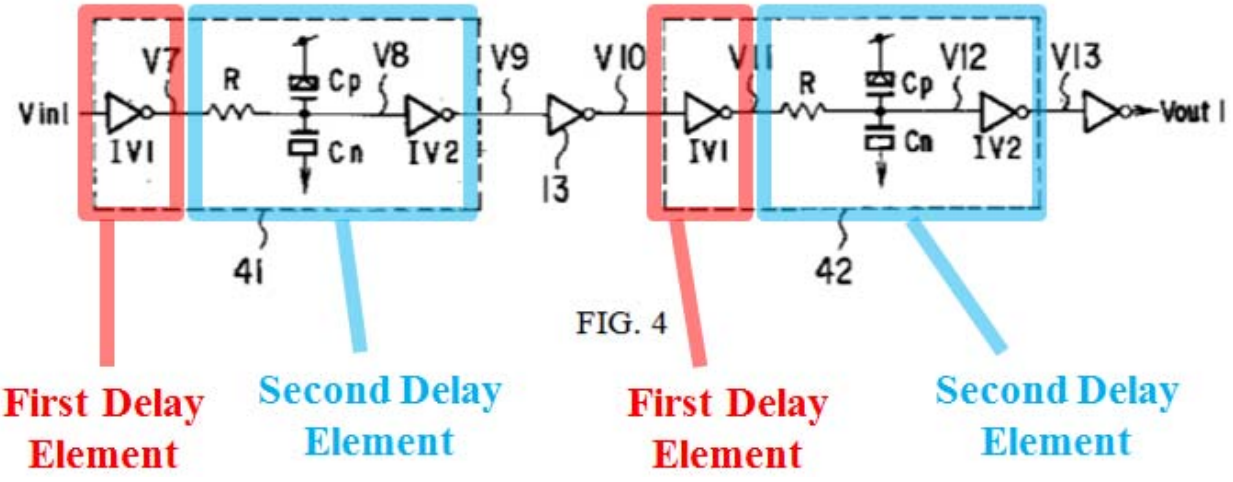


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶68.)

The "first delay element" and "second delay element" in Ogiwara (as shown above) have unequal propagation delays because the second delay element has an additional RC circuit (formed from R, Cp, and Cn) compared to the first delay element. (Ex. 1002, ¶69.) A POSITA would have understood that the presence of this additional RC circuit would result in different delays through the "first delay element" and the "second delay element" because of the additional delay imposed by the RC circuit formed by R, Cp, and Cn in the "second delay element." (*Id.*) This is explained in further detail below.

Ogiwara discloses that each of inverters IV1 and IV2 "have a normal constitution in which, as shown in FIG. 25, for example, the PMOS transistor TP and NMOS transistor TN gates are connected to one another." (Ex. 1006, ¶[0051]; *supra* Section IX.A.1(a) (explaining that the description of the first embodiment in Ogiwara also applies to the second embodiment (i.e., the FIG. 4 embodiment)).) Therefore, each of the inverters IV1 and IV2 in each of the blocks of delay elements 41 and 42 is a CMOS (complementary MOS) inverter that includes a PMOS and NMOS transistor as shown in figure 25. (Ex. 1002, ¶70.)

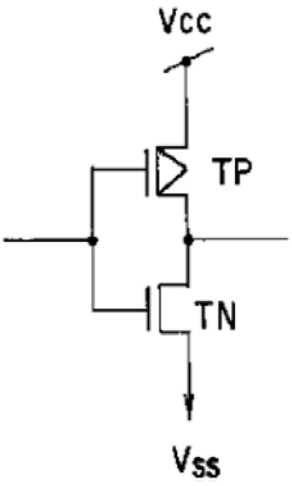


FIG. 25

(Ex. 1006, FIG. 25).

Ogiwara further discloses that inverters IV1 and IV2 have PMOS transistors of approximately the same size and NMOS transistors of approximately the same size. (*Id.*, ¶ [0076], "the first delay circuit 11 PMOS transistor size and the second

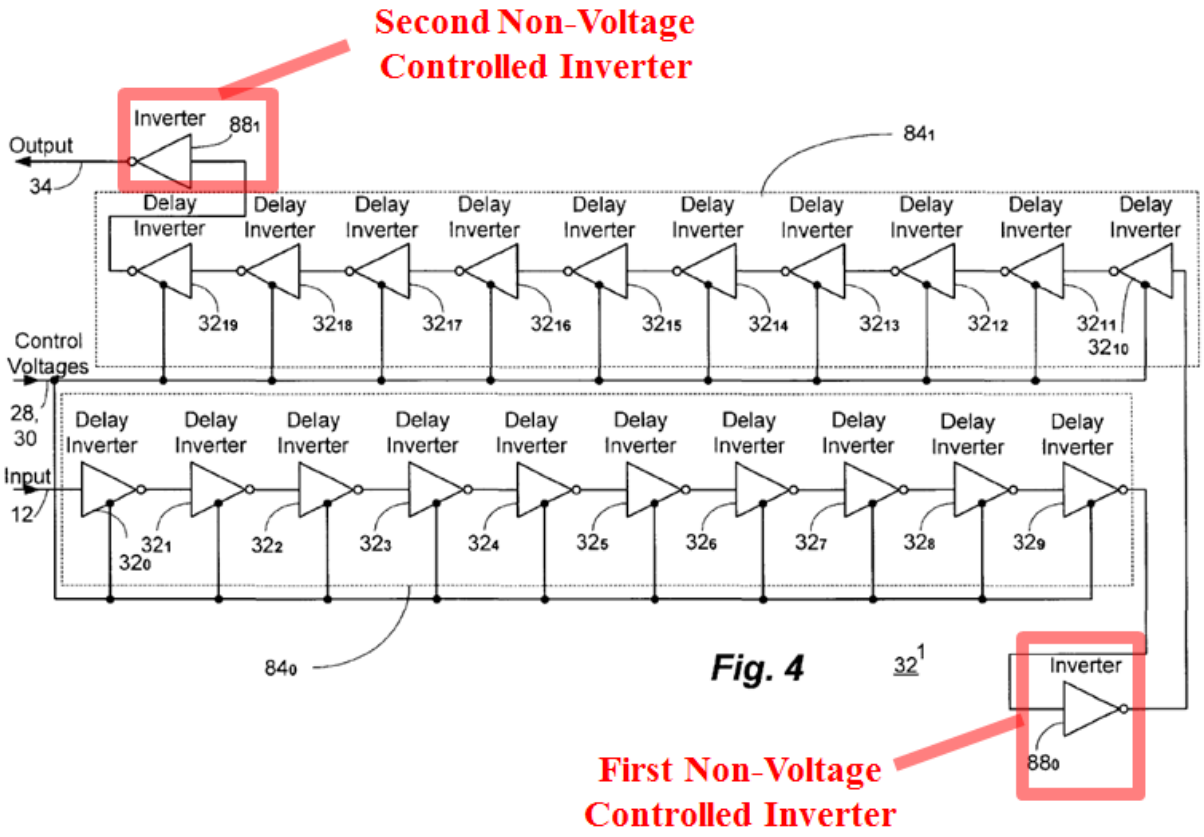
delay circuit 12 PMOS transistor size are approximately equal, and the first delay circuit 11 NMOS transistor size and the second delay circuit 12 NMOS transistor size are approximately equal.") Accordingly, Ogiwara discloses that the inverters IV1 and IV2 are the same, both with respect to each other and with respect to their counterparts in the other delay circuit in the delay line (i.e., IV1 and IV2 in delay circuit 41 have the same PMOS and NMOS transistor sizes, and those same PMOS and NMOS transistor sizes are also used in IV1 and IV2 of delay circuit 42). (Ex. 1002, ¶¶71-72; *see also id.*, ¶72, n.5.)

While both the "first delay element" and the "second delay element" have a similar inverter (IV1 and IV2), the "second delay element" also includes an RC circuit (R, Cp, and Cn) that will add additional delay for a signal passing through it. That is, while a signal passing through the "first delay element" will face a delay equal to that offered by inverter IV1, a signal passing through the "second delay element" will not only face a delay offered by inverter IV2 (which has the same structure has IV1) but also additional delay offered by the RC circuit (R, Cp, and Cn). Accordingly, Ogiwara discloses that "the propagation delay of individual delay elements in each of said first and second blocks is at least partially unequal." (*Id.*, ¶73.)

Moreover, the above conclusion that Ogiwara discloses that "the propagation delay of individual delay elements in each of said first and second

blocks is at least partially unequal" is also consistent with the '559 patent disclosure. As explained below, the '559 patent provides some explanation regarding what is required for two non-voltage controlled inverters (like inverters IV1 and IV2 in Ogiwara) to have the *same* propagation delay. (*Id.*, ¶74.)

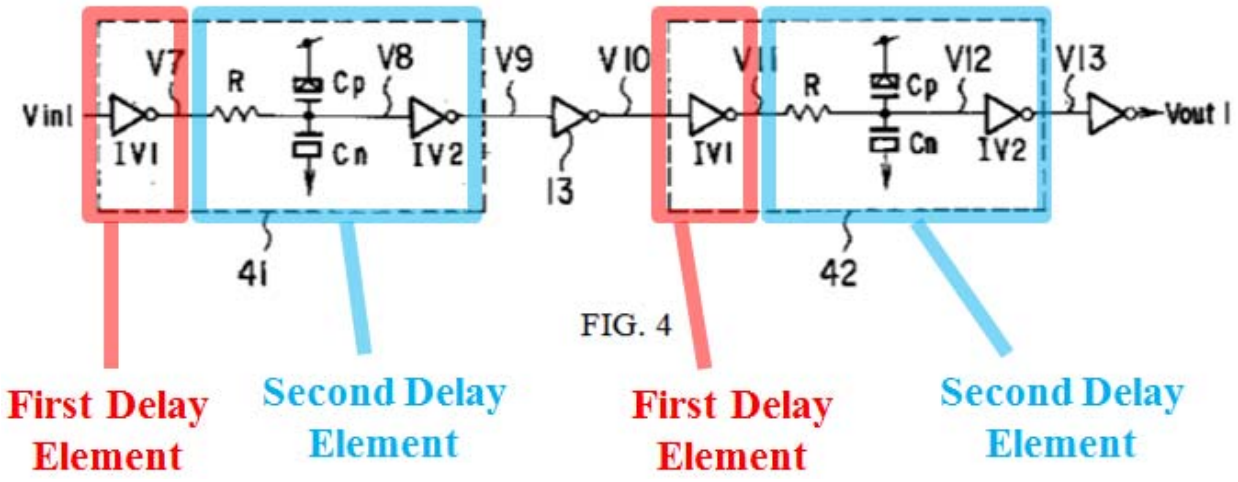
Specifically, claim element 5[g] of the '559 patent states that "the propagation delay of said first and second inverters is equal," where the first and second inverters are "non-voltage controlled." (Ex. 1001, 6:16-26.) Therefore, the claimed "first and second inverters" must correspond to non-voltage controlled inverters 88_0 and 88_1 depicted below in figure 4 of the '559 patent. (Ex. 1002, ¶75.)



(Ex. 1001, FIG. 4 (annotated); Ex. 1002, ¶75.)

While the '559 patent does not explicitly disclose how the propagation delay through the inverters 88_0 and 88_1 is made equal, the '559 patent indicates that "[t]he only requirement is that the inverter 88_0 and inverter 88_1 be identical and have the same parasitic loading." (Ex. 1001, 5:4-6.) The '559 patent further discloses that "[m]atching of these inverters is relatively easy to effectuate since the same inverter layout can be used in both cases *and the input drive to each is identical*." (*Id.*, 5:6-8, emphasis added.)

As is apparent from figure 4 of Ogiwara, while the inverters IV1 and IV2 are approximately the same, *the input drive to each inverter is different*. The presence of the RC circuit, which includes resistor R and capacitors Cp and Cn, at the input of the inverter IV2 in each of the delay blocks presents different loading on the input drive to the inverter IV2 than is present for the inverter IV1. (Ex. 1002, ¶¶76-77.) As such, a POSITA would have recognized that the propagation delay through the second delay element that includes R, Cp, Cn, and the inverter IV2 is different than the propagation delay of the first delay element that only includes inverter IV1. Because the propagation delay of the first and second delay elements ("individual delay elements") in figure 4 of Ogiwara is different, the propagation delay of those delay elements is "at least partially unequal" as recited in claim 5. (*Id.*)



(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶77.)

The prosecution history of U.S. Patent 6,339,354 ("the '354 patent), which is the parent patent to the '559 patent, further confirms that the inclusion of the RC circuit between the inverters in each of the delay blocks in Ogiwara results in non-identical delay elements. For example, during prosecution of the '354 patent, Applicant argued that "Claim 1 calls for a delay line with first and second blocks of delay elements in which odd-even pairs of said delay elements are at least partially non-identical." (Ex. 1005, 127, emphasis omitted.) Applicant further noted that "[i]n prior art devices, control over pulse width for a signal propagated through a delay line was achieved typically by attempting to fabricate each odd-even pair of delay inverters to be identical and *with parasitic loading between all inverters being the same*." (*Id*., emphasis added.) Applicant further argued that "[t]he claimed invention overcomes the need for matching at the individual inverter level by not requiring odd-even matching." (*Id*.) Therefore, in the prosecution of the parent '354 patent, Applicant's arguments were premised on the assertion that "matching at the individual inverter level" included both identical inverters and the same parasitic loading for the inverters.

As is apparent from figure 4 of Ogiwara, the loading of the first inverter IV1 and the second inverter IV2 is not the same, and therefore there is no even-odd pair matching within the delay block. Based on the disclosure of the '559 patent and corresponding prosecution histories, the lack of even-odd pair matching that is

shown in figure 4 of Ogiwara establishes that the "propagation delay of individual delay elements in each of said first and second blocks is at least partially unequal." (Ex. 1002, ¶79.)

d) said first and second blocks have substantially identical block level integrated circuit layouts;

Ogiwara in combination with Noda discloses or suggests this feature. (Ex. 1002, ¶¶80-90.) Figure 4 of Ogiwara shows that the first and second blocks of delay elements 41 and 42 each include the same circuit components (IV1, R, Cp, Cn, IV2) that are interconnected in an identical manner. (*See* Ex. 1006, FIG. 4).

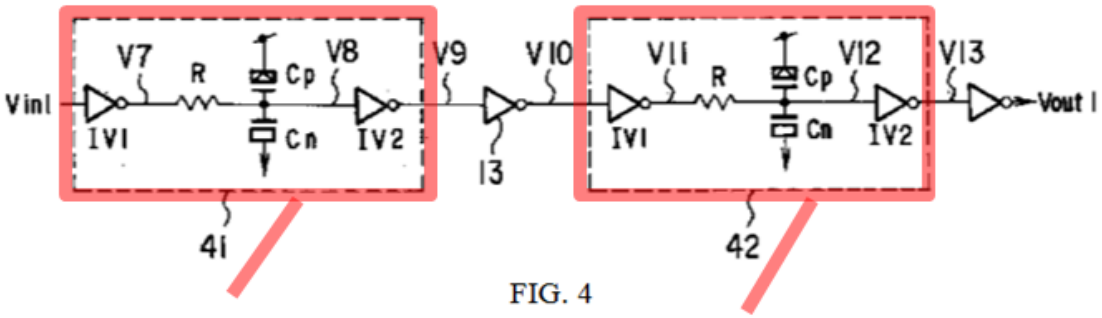


FIG. 4

(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶80.)

While Ogiwara does not explicitly state that the identical "layout" is necessarily used when implementing delay circuits 41 and 42 on a wafer, a POSITA would have found it obvious to use the same layout (e.g. the same patterns for the various layers of the components in the integrated circuit) for delay

circuits 41 and 42. (Ex. 1002, ¶81.) Using the same layout for circuit constructs like those depicted in figure 4 reduces design effort and is consistent with Ogiwara's desire to simplify the design of the delay circuit disclosed. (Ex. 1006, ¶[0076].) Such reduced design effort is realized because portions of the design of the integrated circuit are reused to create other portions. Indeed, it would have been common sense for a POSITA to first perform a layout for one of the delay circuits (e.g., delay circuit 41) and use that same layout for the other delay circuit (e.g., delay circuit 42) because the two delay circuits are identical and reusing the layout would shorten design time. (Ex. 1002, ¶¶82-83 (citing Ex. 1008, 1:16-36; Ex. 1009 at 93.) *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1328-30 (Fed. Cir. 2009) (noting that "[c]ommon sense has long been recognized to inform the analysis of obviousness if explained with sufficient reasoning" and concluding that it would have been nothing more than common sense to repeat process steps when "common sense dictates" such repetition.)

Indeed, additional reasons support the above conclusion that a POSITA would have found it obvious to use the same layout for the two delay circuits. For example, Ogiwara further discloses that "it is particularly desirable from the standpoint of simplifying design to set" the values of the resistance of the resistor R and capacitance of the capacitors Cp, Cn the same in both delay circuits 41 and 42. (Ex. 1006, ¶[0076].) A POSITA would have understood that using the same

respective layout for the resistors R and for each of the capacitors Cp and Cn shown in figure 4 would have provided a simple way to accomplish the desired matching of resistance and capacitance values. (Ex. 1002, ¶¶84-86.) A POSITA would also have understood that such re-use would also simplify design of the circuit while achieving the goal of matching the device characteristics. (*Id*.)

Moreover, a POSITA would have understood that the representation of IV1 and IV2 with the same label in each of the delay circuits indicates that the inverter IV1 is the same in each delay block and that the inverter IV2 is also the same in each block. (Ex. 1002, ¶86; *supra* Section IX.A.1(c) (explaining that the size of the PMOS and NMOS transistors in inverters IV1 and IV2 is approximately the same[4]).) A POSITA would also have understood that the same layout would have been used for these inverters in the delay blocks 41 and 42 because doing so would be consistent with Ogiwara's desire of "simplifying design" of the circuit. (Ex. 1002, ¶86.)

As discussed above, a POSITA would have found it obvious to implement identical block level layouts for the first and second delay blocks 41 and 42.

[4] *See* Ex. 1002, ¶72, n.5 (explaining that when Ogiwara describes circuit elements as "approximately equal," a POSITA would have understood Ogiwara's description to refer to circuit elements that would be identical but for fabrication variations that are inherent to the manufacturing process).

Moreover, such a feature would also have been obvious based on the teachings of Ogiwara in combination with Noda.

Noda "relates to a semiconductor device and, more particularly, to a semiconductor integrated circuit device of a standard cell system . . . ." (Ex. 1008, 1:10-12.) Noda explains that as the number of circuit components on a chip has increased over the years, "the period required for designing" such a chip "has been undesirably increased." (*Id.,* 1:16-21.) Noda discloses that "to shorten the design period, a method of designing a standard cell system has been widely employed." (*Id.,* 1:21-23.) In such a standard cell system, a layout is created for various circuit components (e.g., inverter, NAND gate, flip-flop) and saved as a cell in a cell library. (*Id.,* 1:24-30.) The cell is then instantiated when the corresponding circuit component is encountered in the circuit. (*Id.,* 1:24-36.) In view of the above, a POSITA would have understood that Noda discloses that the same layout can be reused for identical circuit components. (Ex. 1002, ¶88.)

A POSITA would have found it obvious to combine the teachings of Ogiwara with Noda such that the same layout is used for delay circuits 41 and 42. (Ex. 1002, ¶89.) A POSITA would have looked to Noda because, like Ogiwara, Noda also discloses semiconductor integrated circuits with repetitious circuit components. (Ex. 1006, ¶[0001]; Ex. 1008, 1:10-12.) Having looked to Noda, a POSITA would have been motivated to use the same layout for delay circuits 41

and 42 because circuits 41 and 42 have identical components interconnected in an identical manner and using the same layout for both circuits 41 and 42 would have shortened the design time for implementing Ogiwara's circuit on a semiconductor wafer. (Ex. 1002, ¶89; Ex. 1008, 1:16-36; Ex. 1009 at 93.) *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]").

Therefore, the Ogiwara-Noda combination discloses or suggests that "the first and second blocks have substantially identical block level integrated circuit layouts." (Ex. 1002, ¶90.)

e) a first non-voltage controlled inverter coupled to an output of said first block of delay elements for providing an inverted delayed signal to said second block of delay elements,

The Ogiwara-Noda combination discloses or suggests this feature. (Ex. 1002, ¶¶91-95.) For example, figure 4 of Ogiwara shows inverter 13 coupled in series between the first and second blocks of delay elements 41 and 42. (Ex. 1006, ¶ [0068], FIG. 4.)

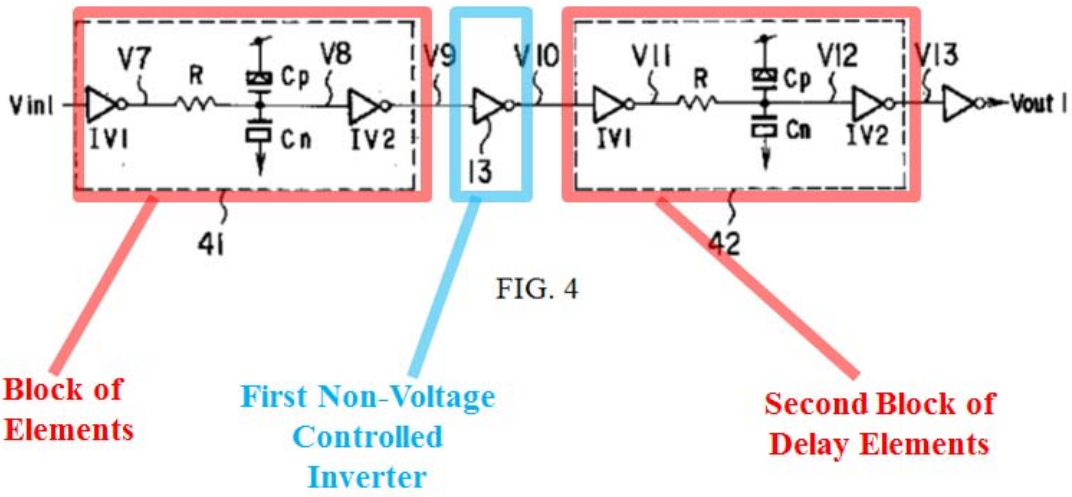
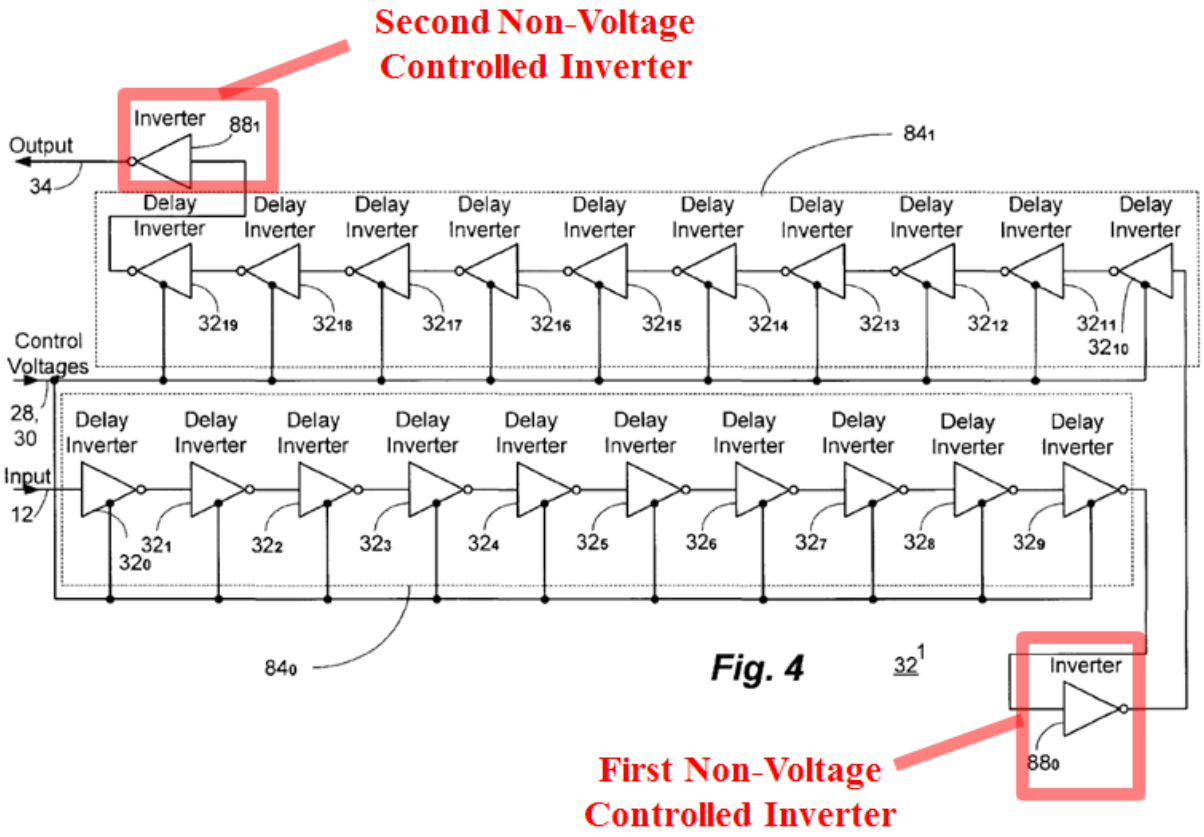


FIG. 4

(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶91.)

The inverter 13 is coupled to the output of the first block of delay elements 41, which corresponds to node V9. (Ex. 1006, FIG. 4.) The output of the inverter 13, which corresponds to node V10, is provided to the input of the second block of delay elements 42. (Ex. 1006, ¶[0068], ¶[0078], FIGs. 1, 4.) The output of the inverter 13 is a delayed version of the signal Vin1 that is input to the second block of delay elements 42, where the delay applied to the signal Vin1 is the sum of the delay through the first block of delay elements 41 and the delay through the inverter 13. (Ex. 1002, ¶92.) Therefore, the Ogiwara-Noda combination discloses or suggests an "inverter coupled to an output of said first block of delay elements for providing an inverted delayed signal to said second block of delay elements" as recited in claim 5. (*Id.*)

The ’559 patent distinguishes between voltage-controlled inverters and non-voltage controlled inverters in that one or more additional control signals are applied to a voltage controlled inverter in order to control the delay through the voltage controlled inverter. (Ex. 1001, 3:42-56, 4:50-56, 4:60-62.) A non-voltage controlled inverter does not receive such a control voltage. (*Id.*, 4:56-58, “The inverters 88_0 and 88_1 may be conventional CMOS inverters or comprise any other suitable inverter structure or process.”) For example, the delay inverters 32_0-32_{19} shown in annotated figure 4 of the ’559 patent below are voltage controlled inverters that receive control voltages 28. Inverters 88_0 and 88_1 do not receive the control voltages 28, and are non-voltage controlled inverters.

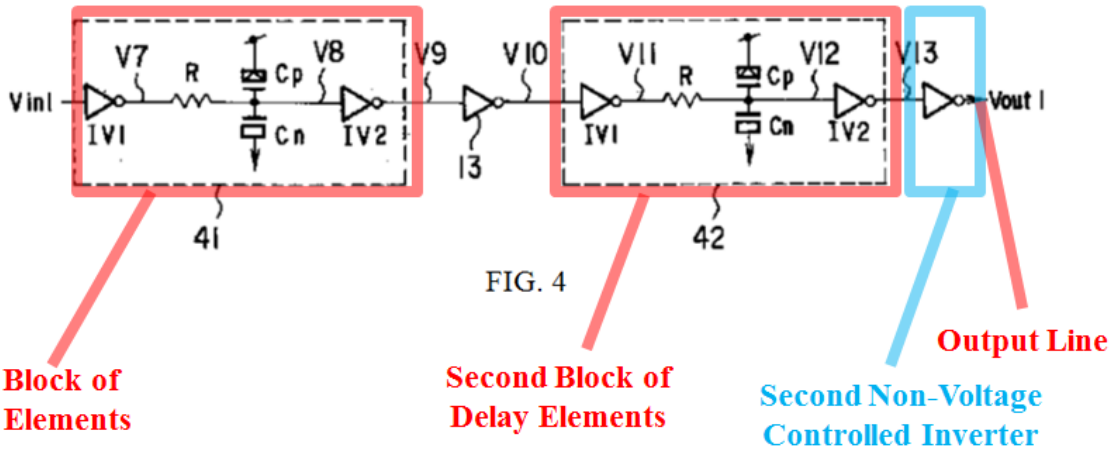


(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶94.)

The inverter 13 shown in figure 4 of Ogiwara does not receive a control voltage that varies the delay through the inverter, and therefore, a POSITA would have recognized that inverter 13 is a "non-voltage controlled inverter" as that term is used in the context of the '559 patent. (Ex. 1002, ¶95.) Therefore, the Ogiwara-Noda combination discloses or suggests "a first non-voltage controlled inverter coupled to an output of said first block of delay elements for providing an inverted delayed signal to said second block of delay elements" as recited in claim element 5[e]. (*Id.*)

f) a second non-voltage controlled inverter coupled to an output of said second block of delay elements for providing a re-inverted delayed signal on said output line; and

The Ogiwara-Noda combination discloses or suggests this feature. (Ex. 1002, ¶¶96-98.) For example, annotated figure 4 of Ogiwara below shows an inverter coupled to the output of the second block of delay elements at the node labeled V13. (Ex. 1006, FIG. 4.)



(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶96.)

For the same reasons discussed above with respect to inverter 13 in claim element 5[e] above, the inverter coupled to the output of the second block of delay elements highlighted in annotated figure 4 above is also a "non-voltage controlled inverter" as that term is used in the '559 patent. (*See supra* Section IX.A.1[e]; Ex. 1002, ¶97.) The output of the second non-voltage controlled inverter is coupled to the output line Vout1, where the inverter provides a re-inverted delayed signal on the output line. The inverter 13 inverts the input signal between the blocks of

delay elements, and the inverter that provides the output signal Vout1 re-inverts that inverted signal provided by the first non-voltage controlled inverter 13 to the second block of delay elements. (Ex. 1006, FIG. 4.)

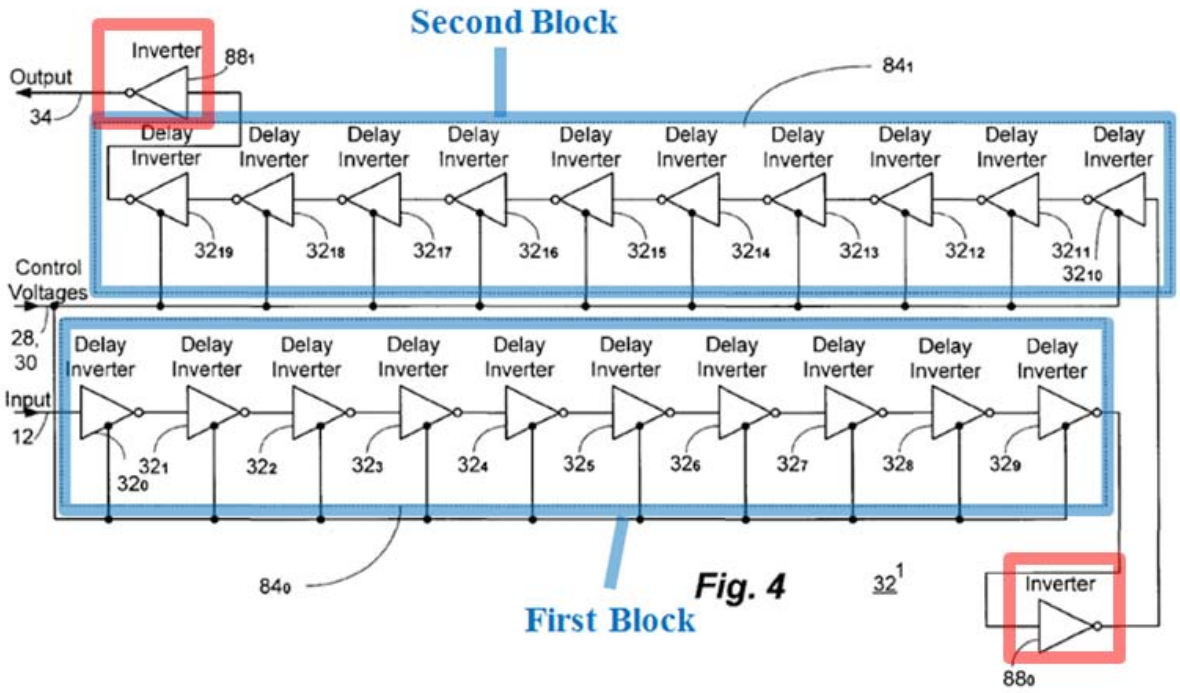
The delay of the output signal Vout1 in comparison to the input signal Vin1 includes the delay through both of the first and second blocks of delay elements as well as the delay through both of the non-voltage controlled inverters. (Ex. 1002, ¶98.) Therefore, the output signal Vout1 is a "delayed signal." For at least these reasons, the Ogiwara-Noda combination discloses or suggests "a second non-voltage controlled inverter coupled to an output of said second block of delay elements for providing a re-inverted delayed signal on said output line," as recited in claim element 5[f]. (*Id*.)

g) wherein the propagation delay of said first and second inverters is equal.[5]

The Ogiwara-Noda combination discloses or suggests this feature. (Ex. 1002, ¶¶99-108.) As explained below, Ogiwara discloses this feature in a manner that is consistent with the '559 patent. Specifically, the '559 patent suggests that inverter 88_0 and inverter 88_1 (which correspond to the claimed "first and second

[5] The "first and second inverters" recited in claim element 5[g] are assumed to be "first and second non-voltage controlled inverters" recited in claim elements 5[e] and 5[f].

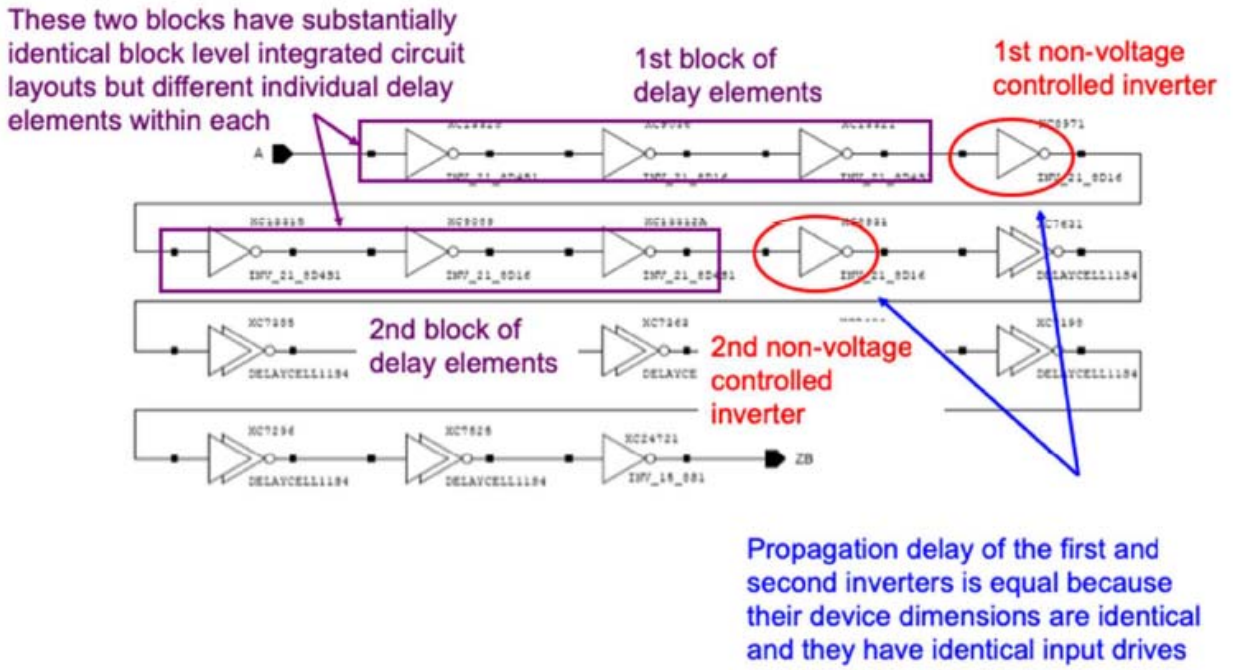
inverters") have the same propagation delay because they are identical and have identical input drives (i.e., the same block of elements provides the input signal to the inverters). (Ex. 1002, ¶99; Ex. 1001, FIG. 4 (reproduced below).) For example, the '559 patent indicates that "[t]he only requirement is that the inverter 88_0 and inverter 88_1 be identical and have the same parasitic loading." (Ex. 1001, 5:4-6.) The '559 patent further discloses that "[m]atching of these inverters is relatively easy to effectuate since the same inverter layout can be used in both cases and the input drive to each is identical." (*Id.*, 5:6-8.)



(Ex. 1001, FIG. 4 (annotated); Ex. 1002, ¶99.)

Indeed, in its infringement allegations in an Amended Complaint filed in district court litigation, Patent Owner argues that two inverters have the same

propagation delay "because their device dimensions are identical and they have identical input drives." (Ex. 1013, 15-16.)



(*Id.*)

Just like the '559 patent, the input drive of the two inverters outside of blocks 41 and 42 is the same. (*See* demonstrative below annotating the "first non-voltage controlled inverter" and "second non-voltage controlled inverter"; *see also supra* Sections IX.A.1(e), (f).) Specifically, as shown in the annotated figure below, the first inverter is driven by block 41 and the second inverter is driven by block 42. As discussed above, blocks 41 and 42 are identical as they have identical components. (*Supra* Section IX.A.1(c); Ex. 1006, FIG. 4, ¶¶ [0075]-[0076].)

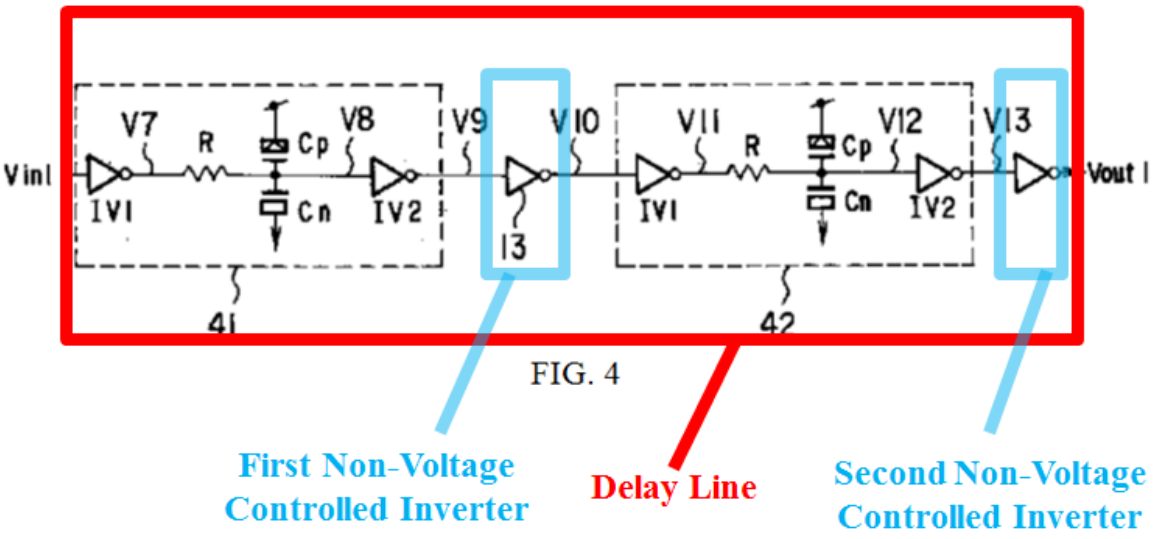


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶100.)

While Ogiwara discloses that inverters IV1 and IV2 are identical across blocks 41 and 42 (*see supra* Section IX.A.1(c)), it is not explicitly stated in Ogiwara that the inverters outside blocks 41 and 42 are identical. (Ex. 1002, ¶101.) But a POSITA would have used identical inverters outside blocks 41 and 42 for at least the following reasons.

First, the two inverters simply serve the role of inverting and reinverting the input signal and therefore, a POSITA would have no reason to choose different dimensions for them as using the same dimensions would have simplified the design of Ogiwara's circuit. (Ex. 1002, ¶102.) Specifically, in the circuit of figure 4 of Ogiwara, inverter 13 is inserted between delay circuits 41 and 42 so that the two delay circuits receive input signals with opposite logic level transitions. (Ex. 1006, ¶[0068].) Stated differently, inverter 13 ensures that a rising edge input to

delay circuit 41 is a falling edge input to the delay circuit 42. (Ex. 1002, ¶102.) Therefore, an inverter is added at the output of delay circuit 42 to reinvert the signal that was inverted by inverter 13 because Vin1 has the same polarity as Vout1. (*Id.*; *see* Ex. 1006, FIG. 5.) Accordingly, the only role of the two inverters is to invert and reinvert a signal. As such a POSITA would have used the same circuit dimensions for the two inverters because Ogiwara explains that design can be simplified by using identical circuit components. (Ex. 1006, ¶[0076], explaining that design is simplified by, for example, using the same value for resistance "R" in the two delay circuits 11 and 12 in figure 1, which are analogous to delay circuits 41 and 42 in figure 4 as explained in Section IX.A.1(a).) Indeed, using the same circuit dimensions for the two inverters would not have negatively impacted Ogiwara's circuit. (Ex. 1002, ¶102.)

Second, using identical inverters in Ogiwara would have been obvious because there are only two choices: either use identical inverters or use inverters having different dimensions. (*Id.*, ¶104.) Thus, choosing identical inverters would have been one of two choices available to a POSITA. Accordingly, using identical inverters would have been obvious because it would have been one of a "finite number of identified, predictable solutions." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d at 1331 (finding that a claimed step was obvious when it was one of three available choices.) Indeed, using identical inverters would have been

consistent with Ogiwara's use of identical inverters IV1 and IV2 across blocks 41 and 42. (*Supra* Section IX.A.1(c).)

Third, using identical inverters would have been consistent with Ogiwara's desire to minimize the overall variability in delay time through the delay circuit shown in figure 4. (Ex. 1006, ¶¶ [0069], [0078].) A POSITA would have recognized that, just as the transitions of the signal being delayed would be opposite in the second block of delay elements 42 in comparison to the corresponding transitions in the first block of delay elements (e.g. a rising edge input to the first block is a falling edge input to the second block), the transitions presented at the input of the second non-voltage controlled inverter would be opposite to the transitions presented to the input of the first non-voltage controlled inverter. (Ex. 1002, ¶103.) Therefore, just as the variations in delays through the blocks of delay elements are cancelled by matching the circuitry of the first block with the second block, matching the two non-voltage controlled inverters outside blocks 41 and 42 would result in any variations in delay through those inverters being cancelled out. (*Id.*) Hence, using identical inverters would have been consistent with Ogiwara's desire to minimize the overall variability in delay time through the delay circuit shown in figure 4. (*Id.*)

Furthermore, in view of Noda, a POSITA would have found it obvious to use the same dimensions and *the same layout* for the two inverters outside blocks

41 and 42 in Ogiwara. (Ex. 1002, ¶105.) For example, Noda discloses that an "inverter" is a "basic gate[]" that can be used as a "standard cell" when designing integrated circuits to shorten the design time. (Ex. 1008, 1:24-36.) A layout is created for the inverter and stored as a "standard cell," which is then instantiated whenever an inverter is encountered in the circuit. (*Id.*)

In view of Noda, a POSITA would have been motivated to use a standard cell layout for the two inverters because doing so would have saved design time and effort. (Ex. 1002, ¶106; Ex. 1008, 1:16-36; Ex. 1009 at 93.) In order for a POSITA to be able to use a standard cell for the two inverters, the two inverters would need to have the same circuit dimensions because only then can the same cell layout be applied for those inverters. (Ex. 1002, ¶106.)

Therefore, in view of the above, a POSITA would have found it obvious to use Noda's teachings of standard cell design in Ogiwara to shorten design time and effort for Ogiwara's circuit. *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). As such, a POSITA would have used the same circuit dimensions and layout for the two inverters. (Ex. 1002, ¶107.) Doing so would have been within the capabilities of a POSITA as evidenced by Noda. (*Id.*)

The Ogiwara-Noda combination therefore discloses or suggests claim element 5[g]. (Ex. 1002, ¶108.) First, as discussed above, the input drive for the two inverters outside blocks 41 and 42 is the same. Second, as also discussed above, the two inverters would have had identical circuit dimensions and layout. Therefore, consistent with the disclosure in the '559 patent, the two inverters would have the same propagation delay. (*See* discussion above regarding the '559 patent's disclosure at column 5, lines 4-10.)

2. Claim 8

a) The delay line as in claim 5 in which the first and second blocks each comprises an even number of CMOS delay inverters.

Ogiwara in view of Noda discloses or suggests this feature. (Ex. 1002, ¶¶109-110.) As shown in figure 4 of Ogiwara, the first delay circuit 41 ("first block of delay elements") and the second delay circuit 42 ("second block of delay elements") each include two delay inverters IV1 and IV2.

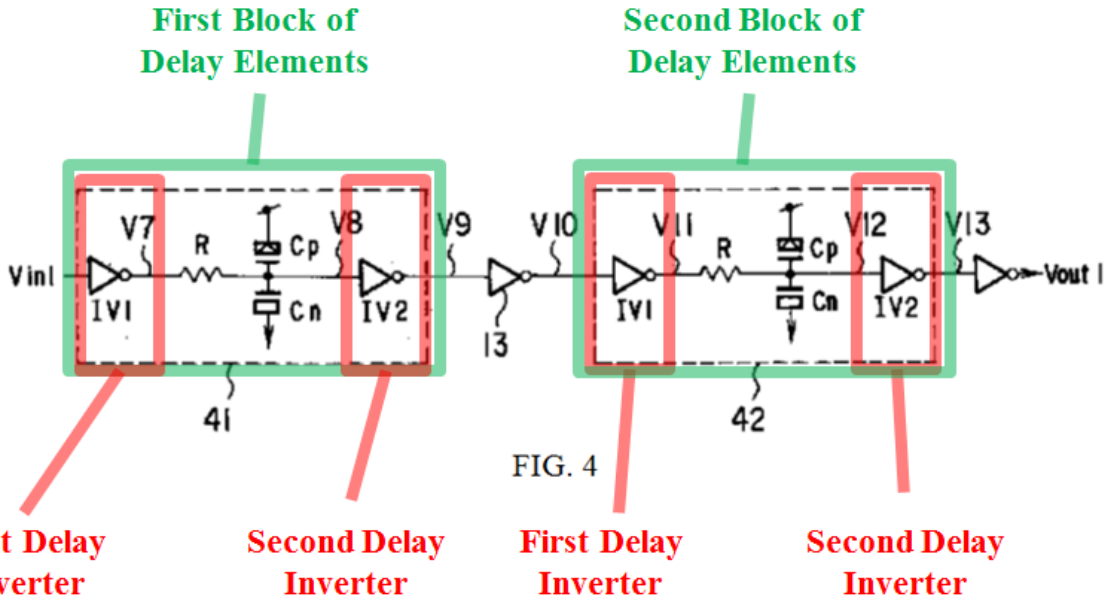


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶109.)

As discussed above with respect to claim element 5[c], Ogiwara discloses that the inverters IV1 and IV2 are CMOS (complimentary MOS) inverters as they include both PMOS and NMOS transistors. (*See supra* Section IX.A.1[c]; Ex. 1002, ¶110; *see also* Ex. 1006 at ¶¶[0070] ("CMOS inverter IV1"), [0084] ("CMOS inverter IV2").) Because each of the first and second blocks of delay elements includes two delay inverters IV1 and IV2, Ogiwara discloses that "the first and second blocks each comprises an even number of CMOS delay inverters" as recited in claim 8. (*Id.*, ¶110.)

3. Claim 12

a) The delay line as in claim 5 in which the first and second inverters each has substantially equivalent parasitic loading.

Ogiwara in view of Noda discloses or suggests this feature. (Ex. 1002, ¶¶111-115.) As discussed above with respect to claim element 5[g], it would have been obvious for the non-voltage controlled inverters (i.e., the inverters outside blocks 41 and 42 in figure 4 of Ogiwara) to have the same dimensions and the same layout. (*Supra* Section IX.A.1(g).)

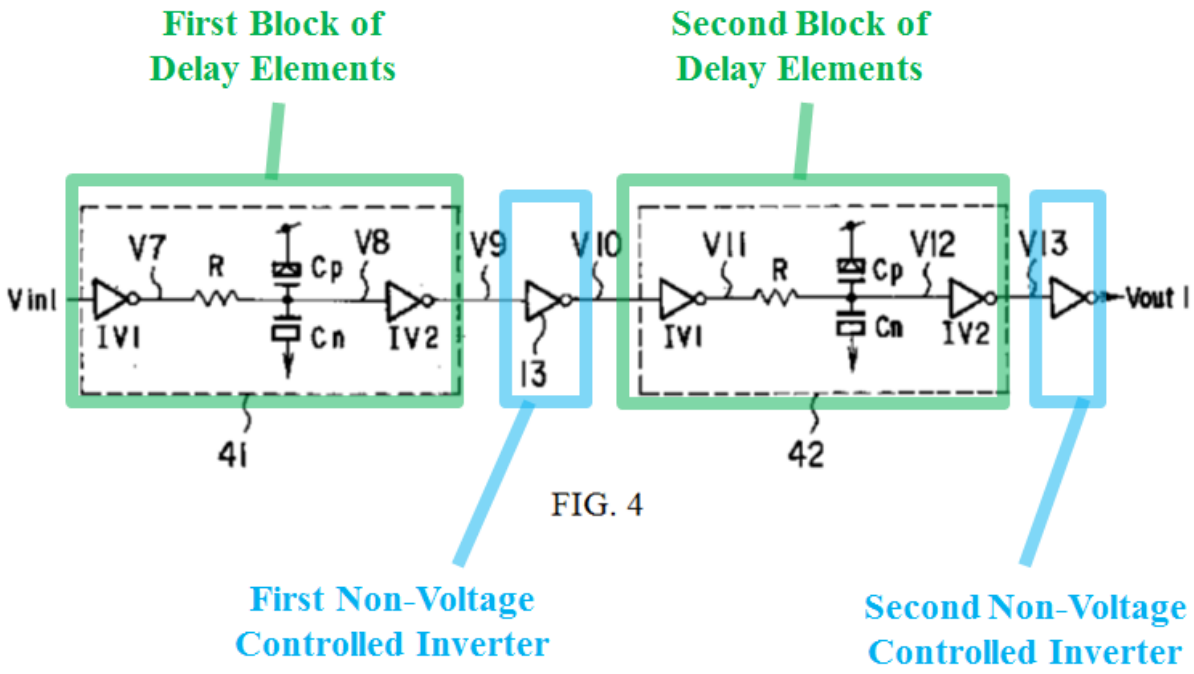


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶111.)

Furthermore, as is apparent from annotated figure 4 above, the input drive to the first and second non-voltage controlled inverters is the same. (Ex. 1006, FIG.

4.) Specifically, each of the first and second non-voltage controlled inverters is driven by the output of a corresponding one of the first and second blocks of delay elements. (*Id*.) Because the first and second blocks of delay elements (i.e., delay circuits 41 and 42) have identical components and would have the same layout (*supra* Section IX.A.1(d)) in the Ogiwara-Noda combination, the outputs of those blocks of delay elements, which constitute the input drive to the non-voltage controlled inverters, are the same. (Ex. 1002, ¶112; Ex. 1006, FIG. 4.)

In view of the above, in the Ogiwara-Noda combination, the two inverters in figure 4 of Ogiwara outside blocks 41 and 42 have "substantially equivalent parasitic loading," as recited in claim 12 because the inverters are identical, have the same layout, and have the same input drive. Such a conclusion is consistent with the '559 patent, as explained below. (Ex. 1002, ¶113.)

The '559 patent discloses that "[t]he only requirement is that the inverter 88_0 and inverter 88_1 be identical and have the same parasitic loading." (Ex. 1001, 5:4-6.) The '559 patent further explains that "[m]atching of these inverters is relatively easy to effectuate since the same inverter layout can be used in both cases and the input drive to each is identical." (*Id.,* 5:6-8.) According to the '559 patent, "[i]f the loading of the inverter 88_0 at the output of the first block and 88_1 at the output of the second block is identical, the pulse width will be perfectly preserved." (*Id.,* 5:15-18.) Therefore, based on the disclosure of the '559 patent, a POSITA would

have understood that each of the first and second non-voltage controlled inverters would have the same parasitic loading if the same layout is used for both inverters and the input drive to each is the same. (Ex. 1002, ¶114.)

Therefore, the Ogiwara-Noda combination discloses or suggests "the first and second inverters each has substantially equivalent parasitic loading" as recited in claim 12. (Ex. 1002, ¶115.)

4. Claim 13

a) The delay line as in claim 5 in which the first and second inverters each has the same inverter layout.

Ogiwara in view of Noda discloses or suggests this feature. (Ex. 1002, ¶116.) As discussed above with respect to claim element 5[g], a POSITA would have been motivated to implement the first and second non-voltage controlled inverters in figure 4 of Ogiwara such that they have the same layout and the same propagation delay. (*See supra* Section IX.A.1(g); Ex. 1002, ¶116.)

5. Claim 14

a) A delay line for delaying an input signal between input and output lines thereof, the delay line comprising:

Ogiwara discloses this feature for the same reasons as those discussed above for claim element 5[a]. (Ex. 1002, ¶117; *supra* Section IX.A.1(a).)

b) first and second blocks of delay elements coupled to receive said input signal on said input line,

Ogiwara discloses this feature for the same reasons as those discussed above for claim element 5[b]. (Ex. 1002, ¶118; *supra* Section IX.A.1(b).)

c) wherein the propagation delay of individual delay elements in each of said first and second blocks is unequal and

While claim element 14[c] recites that the "propagation delay of individual delay elements in each of said first and second blocks is *unequal*" and claim element 5[c] recites that the "propagation delay of individual delay elements in each of said first and second blocks is at least *partially unequal*," a POSITA would have understood that if the propagation delays are "partially unequal" then such propagation delays are not equal and therefore necessarily "unequal." Nothing in the '559 patent distinguishes between delays that are "partially unequal" or "unequal." (Ex. 1002, ¶119.) Therefore, for the same reasons provided above with respect to claim element 5[c], the Ogiwara-Noda combination discloses or suggests that "the propagation delay of individual delay element in each of said first and second blocks is unequal" as recited in claim 14.

d) said first and second blocks have substantially identical propagation delays;

Ogiwara in view of Noda discloses or suggests this feature. (Ex. 1002, ¶¶120-123.) The '559 patent does not provide any specific disclosure as to how

the blocks 84_0 and 84_1 (which correspond to the claimed "first and second blocks") shown in annotated figure 4 below have "substantially identical propagation delays."

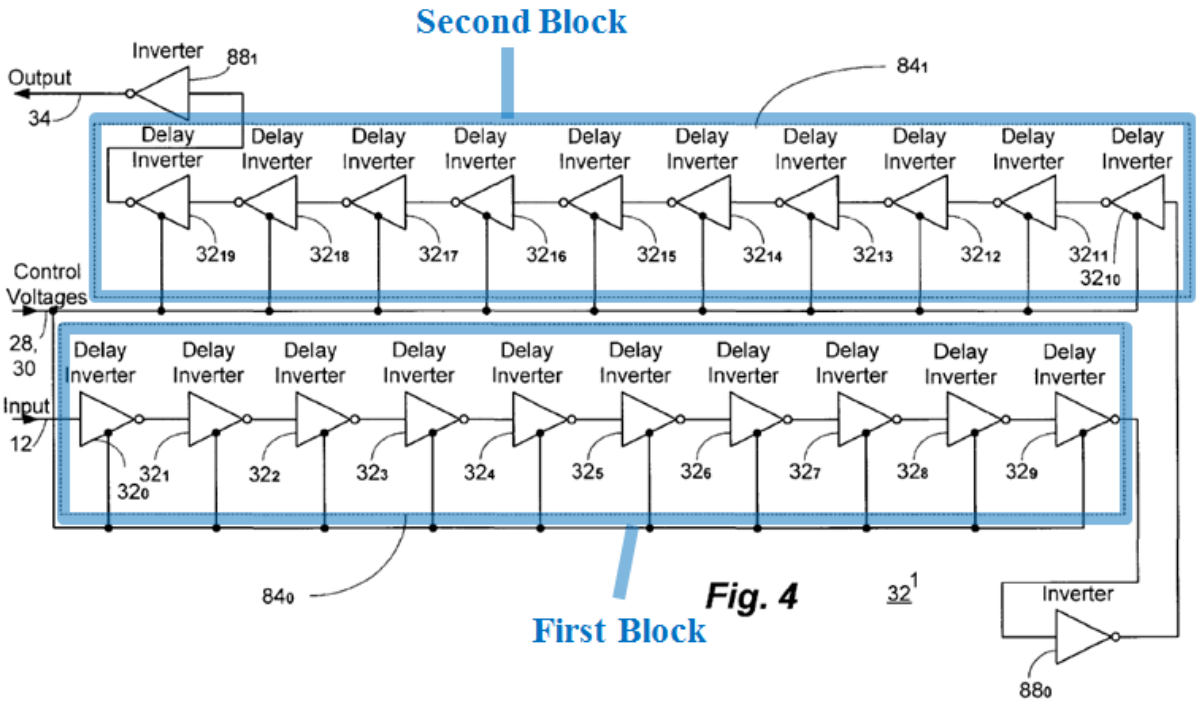


Fig. 4

(Ex. 1001, FIG. 4 (annotated); Ex. 1002, ¶120.)

The '559 patent characterizes the blocks 84_0 and 84_1 as "two identical blocks of inverters." (Ex. 1001, 4:66-67.) Further, claim element 5[d] states that "said first and second blocks have substantially identical block level integrated circuit layouts." (*Id.*, 6:14-15.) Moreover, a non-voltage controlled inverter 88_0 is inserted between blocks 84_0 and 84_1 "so that the rising edge input to the first block 84_0 becomes a falling edge input to the second block 84_1 . . . ." (*Id.*, 5:11-15; Ex. 1002, ¶121.)

The Ogiwara-Noda combination discloses each of the above aspects of the '559 patent and therefore, discloses claim element 14[d] for the same reasons as the '559 patent specification supports disclosure of claim element 14[d]. (Ex. 1002, ¶122.) For example, as discussed above in section IX.A.1(d), each of the delay blocks 41 and 42 ("first and second blocks") shown in figure 4 of Ogiwara includes identical components (R, Cp, Cn, IV1, and IV2) interconnected in an identical manner. (*Supra* Section IX.A.1(d).) As further discussed above in Section IX.A.1(d), it would have been obvious to use the same layout for blocks 41 and 42 consistent with Ogiwara's objective of simplifying design. (*Id.*) Moreover, a non-voltage controlled inverter (like the non-voltage controlled inverter 88_0 in the '559 patent) is inserted between the two blocks (i.e., delay circuit elements 41 and 42) so that a rising edge input to the first block is input to the second block as a falling edge. (Ex. 1006, ¶[0068].)

Therefore, the Ogiwara-Noda combination discloses or suggests that delay circuit blocks 41 and 42 "have substantially identical propagation delays" consistent with the disclosure in the '559 patent. (Ex. 1002, ¶123.)

e) a first non-voltage controlled inverter coupled to an output of said first block of delay elements for providing an inverted delayed signal to said second block of delay elements,

The Ogiwara-Noda combination discloses or suggests this feature for the same reasons as those discussed above for claim element 5[e]. (Ex. 1002, ¶124; *supra* Section IX.A.1(e).)

f) a second non-voltage controlled inverter coupled to an output of said second block of delay elements for providing a re-inverted delayed signal on said output line; and

The Ogiwara-Noda combination discloses or suggests this feature for the same reasons as those discussed above for claim element 5[f]. (Ex. 1002, ¶125; *supra* Section IX.A.1(f).)

g) wherein the inverter layout of said first and second inverters is the same.

The Ogiwara-Noda combination discloses or suggests this feature for the same reasons as those discussed above for claim element 5[g]. (*See supra* Section IX.A.1(g); Ex. 1002, ¶126.)

6. Claim 16

a) The delay line as in claim 14 in which the first and second blocks each comprises an even number of CMOS delay inverters.

The Ogiwara-Noda combination discloses or suggests this feature for the same reasons as discussed above for claim 8. (Ex. 1002, ¶127; *supra* Section IX.A.2.)

B. Ground 2: Ogiwara, Noda, and Dally Render Obvious Claims 1-4, 6, 7, 9-11, 15, and 17

1. Claim 6

a) The delay line as in claim 5 in which the delay line further comprises means for varying the delay of the input signal.

Ogiwara in view of Noda and Dally discloses or suggests this feature. (Ex. 1002, ¶¶128-139.) As discussed above in Section VIII.A, the "means for varying the delay of the input signal" disclosed in the '559 patent corresponds to a voltage controlled delay inverter circuit such as that shown in figure 2 of the '559 patent.

The Ogiwara-Noda combination discussed above for claim 5 does not disclose a "means for varying the delay of the input signal" in the delay line shown in figure 4 of Ogiwara. For example, inverters IV1 and IV2 in blocks 41 and 42 are not voltage controlled CMOS inverters. (Ex. 1006, FIG. 4.) However, as discussed below, it would have been obvious to modify the delay line of Ogiwara such that a voltage controlled delay inverter circuit is utilized for inverters IV1 and

IV2, thereby providing a "means for varying the delay of the input signal." (*Id.*, ¶130.)

Dally recognizes that "[a] CMOS inverter can be used as a simple delay element and a delay line can be built by cascading a number of inverters." (Ex. 1007, 589.[6]) Such an understanding is consistent with the delay line shown in figure 4 of Ogiwara, where each delay block 41 and 42 includes two inverters that are cascaded. (Ex. 1002, ¶131.)

Dally further discloses that an adjustable delay line can be constructed using delay elements with an analog control input. (Ex. 1007, 589-590; Ex. 1002, ¶132.) Dally also discloses a technique for modifying an inverter to provide a variable delay element used in a delay line. (*Id.*) According to Dally, "the most obvious way to add a voltage-mode control input is to add current control transistors in series with the switching transistors in the inverters." (*Id.*) Such an implementation is depicted in figure 12-27 of Dally, which is similar to the voltage controlled delay inverter shown in figure 2 of the '559 patent. (*Id.*, ¶133.) Indeed, the '559 patent acknowledges that the circuit of figure 2 was known and used in prior art delay lines in delay locked loops (DLLs). (Ex. 1001, 3:3-7, 4:8-15, FIGs. 2-3.)

[6] All citations to Dally are to the actual page numbers in the book.

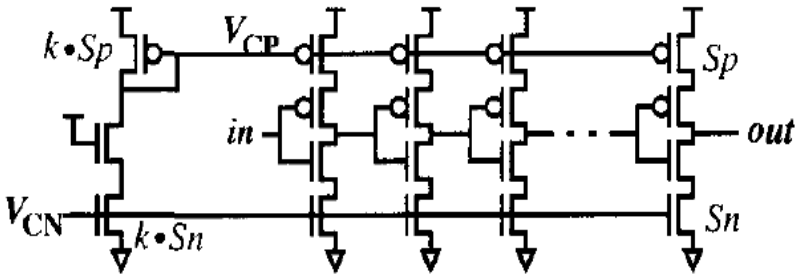


FIGURE 12-27 Current-Starved Inverter Delay Line

(Ex. 1007, FIG. 12-27.)

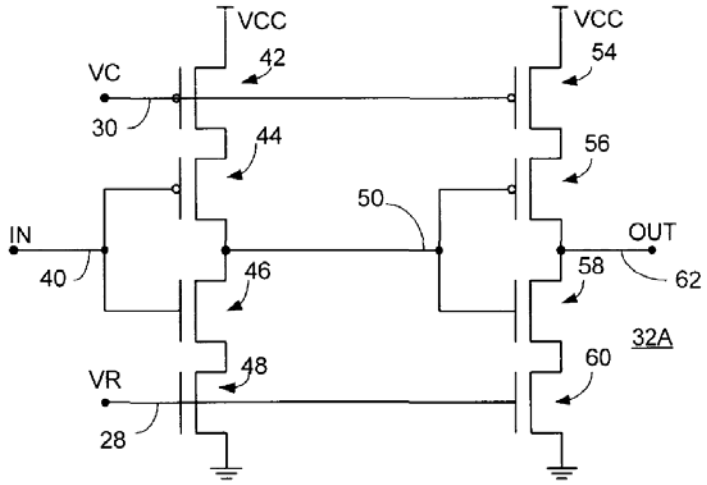


Fig. 2

(Ex. 1001, FIG. 2.)

In view of Dally, a POSITA would have found it obvious to modify the CMOS inverters IV1 and IV2 in the delay line shown in figure 4 of Ogiwara to make the delay through those inverters variable. (Ex. 1002, ¶134.) As a result, the delay line in figure 4 of Ogiwara would have included voltage controlled inverters that would have provided a means for varying the delay of the input signal applied to the delay line. (*Id.*) A POSITA reading Dally would have understood how to

make the delay through the inverters IV1 and IV2 variable. (*Id.*) For example, such a POSITA would have added current control transistors in series with the switching transistors in the CMOS inverters IV1 and IV2 in a manner similar to that shown in figure 12-27 of Dally. (*Id.*)

A POSITA would have looked to Dally because Dally is a well-known book in the field of integrated circuit design and both references disclose delay circuits and techniques for achieving delays for signals propagating on integrated circuits. (*Id.,* ¶135; Ex. 1006, ¶ [0001], "The present invention pertains to a semiconductor circuit, and more particularly to an RC delay circuit formed in an integrated circuit having a MOS structure used, for example, in memory such as DRAM and SRAM, or in logic gates, CPUs and the like."; Ex. 1007, 583-585, 595-596.) Having looked to Dally, a POSITA would have been motivated to make the above modification because it would have allowed the figure 4 delay line of Ogiwara to be used in applications requiring a variable delay line, thereby enhancing the utility of the Ogiwara's delay line. (Ex. 1002, ¶135.) *Unwired Planet, LLC*, 841 F.3d at 1003 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). For example, a delay locked loop (DLL), which requires a variable delay line, could be implemented with the variable delay line resulting from the modified delay line of Ogiwara. The utility of such DLLs is recognized

by Dally, which describes DLLs that include voltage-controlled delay lines (VCDLs) being used in applications such as clock aligners. (Ex. 1007, (635-639.) Figure 12-96 from Dally, replicated below, shows such a DLL-based clock aligner, where the DLL includes a voltage-controlled delay line labeled "VCDL."

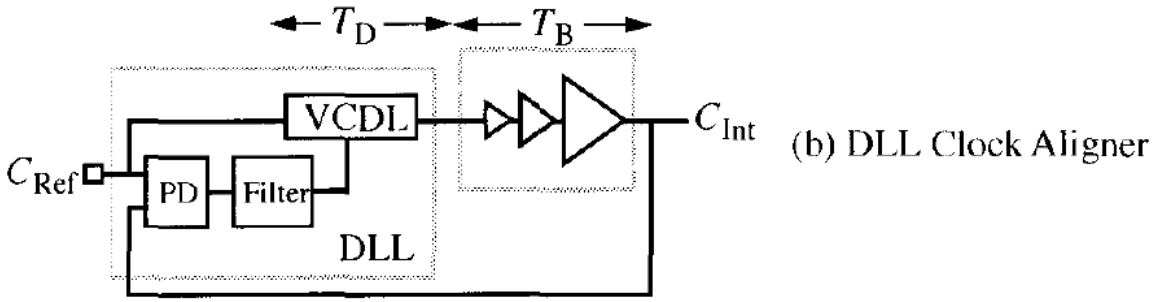


FIGURE 12-96 Clock Aligner Implementations

(*Id.,* FIG. 12-96.)

Indeed, the utility of variable delay lines in DLLs is also recognized by the '559 patent as being well-known at the time of the alleged invention. (Ex. 1001, 1:22-45.) For example, the '559 patent recognizes in the Background of the Invention that DLL circuits are used to improve throughput in DRAMs, where a digital pulse or steam of pulses can be delayed in such a DLL circuit where "a string of an even number of series coupled inverters is often used." (Ex. 1001, 1:22-49.) The '559 patent also recognizes that it was known that the delay in a delay line made up of inverters could be made variable. (*Id.,* 1:49-52, "If it is desired to make the delay variable, the inverters may include some means of

adjusting the delay through the inverter with an applied external voltage level."; Ex. 1002, ¶¶136-137.)

A POSITA would have recognized that the above modification of the Ogiwara delay line based on Dally's disclosure of voltage controlled inverters used in delay lines would have been merely the result of combining prior art elements (e.g., Ogiwara's figure 4 delay line and Dally's voltage-controlled delay modifications) according to known methods (e.g., adding current-limiting transistors to the inverters in the delay blocks of Ogiwara's delay line) to yield predictable results (e.g., delay elements with voltage-controllable delays). *KSR*, 550 U.S. at 416-21 (Ex. 1002, ¶138.)

Notably, modifying the inverters IV1 and IV2 in figure 4 of Ogiwara to be variable-delay inverters as disclosed in Dally does not negatively impact the disclosure of the other claim elements by the Ogiwara-Noda-Dally combination. (Ex. 1002, ¶139.) For example, in the Ogiwara-Noda-Dally combination, a POSITA would have understood that each of the inverters IV1 and IV2 in each of the delay blocks 41 and 42 is modified in the same manner such that the layouts and propagation delays through the inverters as modified remain the same. (*Id.*) Therefore, after modification to add voltage-controlled variable delay as disclosed by Dally, the layout of the delay block 41 is still the same as the layout of delay

block 42 and the propagation delay through the delay blocks 41 and 42 as modified by Dally would have been the same. (*Id*.)

2. Claim 7

a) The delay line as in claim 5 in which the delay elements of the first and second blocks each further comprises a control terminal for receiving a control signal.

Ogiwara in view of Noda and Dally discloses or suggests this feature. (Ex. 1002, ¶¶140-141.) As discussed above with respect to claim 6, it would have been obvious to modify inverters IV1 and IV2 in blocks 41 and 42 to be voltage controlled inverters as disclosed in Dally by adding current control transistors in series with the PMOS and NMOS transistors in IV1 and IV2. (*See supra* Section IX.B.1; Ex. 1002, ¶140.) Therefore, each of the modified inverters IV1 and IV2 would have included "a control terminal for receiving a control signal" because each of the current control transistors include a gate ("control terminal") that receives a control voltage. This is shown in Dally, which discloses that the control signal VCN is provided at the gate of a transistor to control how much current is allowed to flow between the switching transistors and the power supply. (Ex. 1007, 590 (FIG. 12-27).)

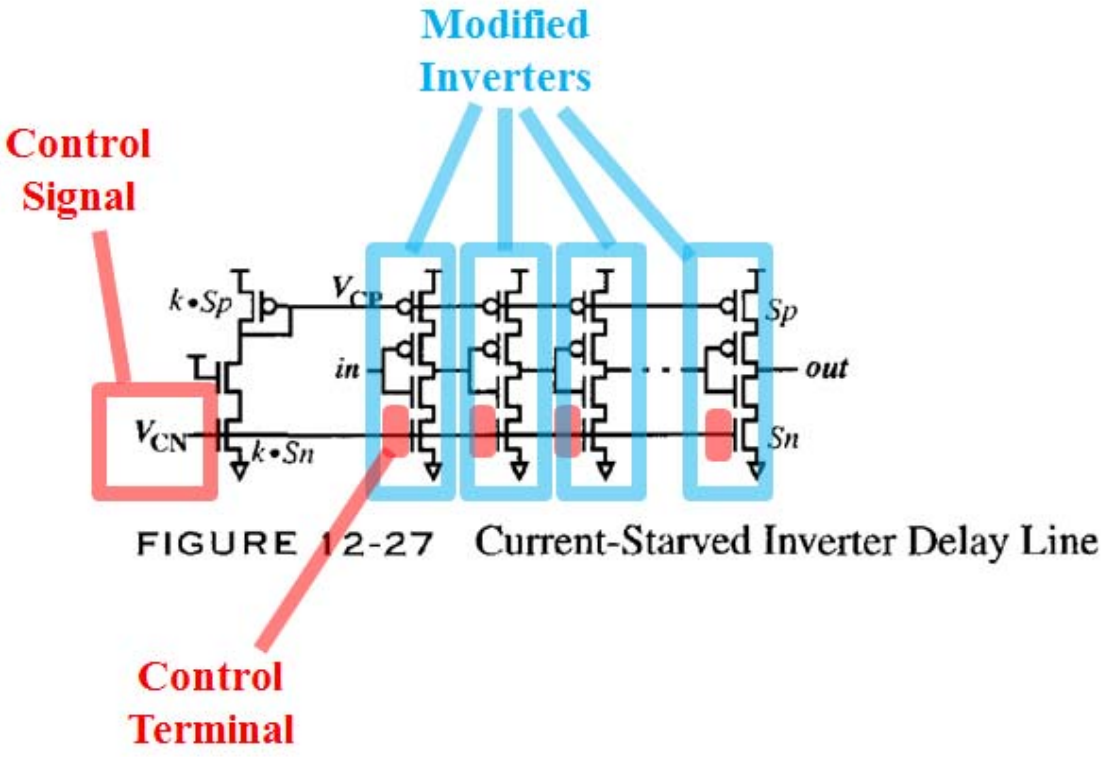


FIGURE 12-27 Current-Starved Inverter Delay Line

(Ex. 1007, FIG. 12-27 (annotated); Ex. 1002, ¶140.)

Therefore in the variable delay line of the Ogiwara-Noda-Dally combination, the inverter in each of the delay elements in the delay blocks 41 and 42 includes a control terminal for receiving a control signal that allows the delay through the delay element to be controlled. As explained above, the gate of the current limiting transistors for each of the inverters would be the "control terminal" for each delay element, where an increased voltage applied to the gates of the current-limiting transistors will reduce the delay through the delay element. (Ex. 1002, ¶141.) Therefore, the Ogiwara-Noda-Dally combination discloses or suggests this feature for the reasons discussed above for claim 6 regarding

modifying the inverters IV1 and IV2 in figure 4 of Ogiwara to be variable-delay inverters. (Ex. 1002, ¶141; *supra* Section IX.B.1.)

3. Claim 9

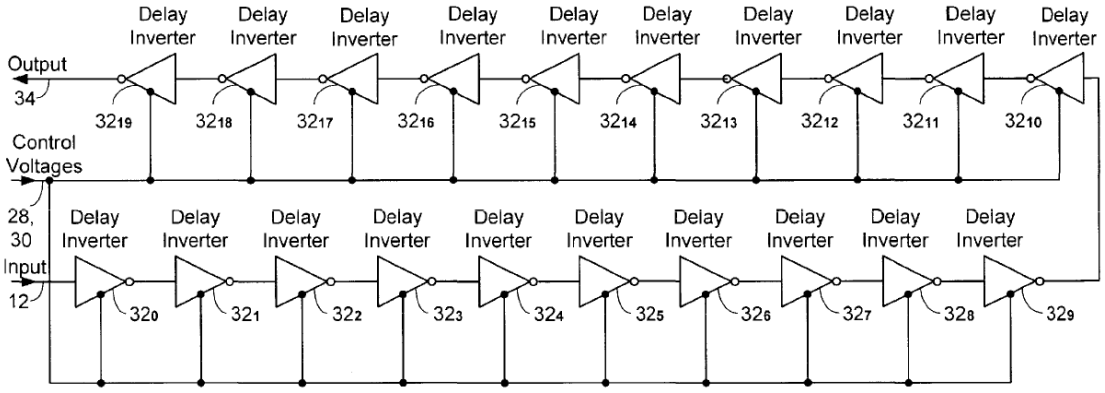
a) The delay line as in claim 5 in which the first and second blocks each comprises at least ten CMOS delay inverters.

Ogiwara in view of Noda and Dally discloses or suggests this feature. (Ex. 1002, ¶¶142-148.) As discussed above with respect to claim 8, each of the delay circuits 41 and 42 include two CMOS delay inverters. (Ex. 1006 at FIG. 6; *supra* Section IX.A.2.) But the number of CMOS delay inverters inside a block is a "result-effective variable" because changing the number of inverters changes the total delay through the delay circuit. (Ex. 1002, ¶142.) Therefore, if "at least ten CMOS delay inverters" is an optimum number per claim 9, claim 9 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '559 patent provides no evidence that "at least ten" CMOS inverters produces a new or unexpected result, and thus the claimed range cannot form the basis of patentability given that the number of CMOS inverters in a block is a result-effective variable. (Ex. 1002, ¶143.) *In re Boesch*, 617 F.2d at 276; *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990). Indeed, there is no criticality

associated with "at least ten" CMOS delay inverters given that the '559 patent admits that prior art delay lines had twenty or more inverters (and therefore, a block had ten or more inverters). (Ex. 1002, ¶143, citing Ex. 1001, 1:52-55, FIG. 3; *see also id.*, ¶144 (citing Ex. 1012).)

Furthermore, as discussed above with respect to claim 6, it would have been obvious to modify the delay line of Ogiwara to provide a variable delay through the delay elements by making the CMOS inverters of the delay elements variable-delay inverters as disclosed in Dally. (*See supra* Section IX.B.1; Ex. 1002, ¶145.) As also discussed above with respect to claim 6, a well-known application for the variable delay line achieved by the combination of Ogiwara and Dally is a clock alignment circuit such as a delay locked loop. (*See supra* Section IX.B.1.) A well-known use for such delay locked loops was in double-data rate (DDR) synchronous dynamic random access memories (SDRAMs). Indeed, such an application is acknowledged as being well-known by the '559 patent. (Ex. 1001, 1:34-55.) Specifically, in the Background of the Invention, the '559 patent states that "[o]ne particular application of relatively long delay voltage controlled delay lines is in conjunction with DDR DRAMs." (*Id.,* 1:34-35.) The '559 patent also notes that "[i]f comparatively long delays are required, such as those often used in DLLs, the number of inverters in the chain can be relatively high, e.g. on the order of twenty or more." (*Id.,* 1:52-55.)

It would have been obvious to modify the delay blocks 41 and 42 in figure 4 of Ogiwara to each include at least ten CMOS delay inverters as modified based on Dally. As discussed above with respect to claim 6, providing voltage control of the delay for the inverters increases the utility of the delay line shown in figure 4 of Ogiwara as such a voltage controlled delay line can be used in a DLL, which in turn can be used in a DRAM. (*See supra* Section IX.B.1.) As acknowledged by the '559 patent, such DLLs require comparatively long delays, which are achieved by using a large number of inverters in the chain of inverters making up the delay line. (Ex. 1002, ¶¶146-147.) Indeed, such a configuration is shown in figure 3 of the '559 patent, which illustrates a "prior art" voltage-controlled delay line that includes 20 voltage-controlled inverters.



(Ex. 1001, FIG. 3.)

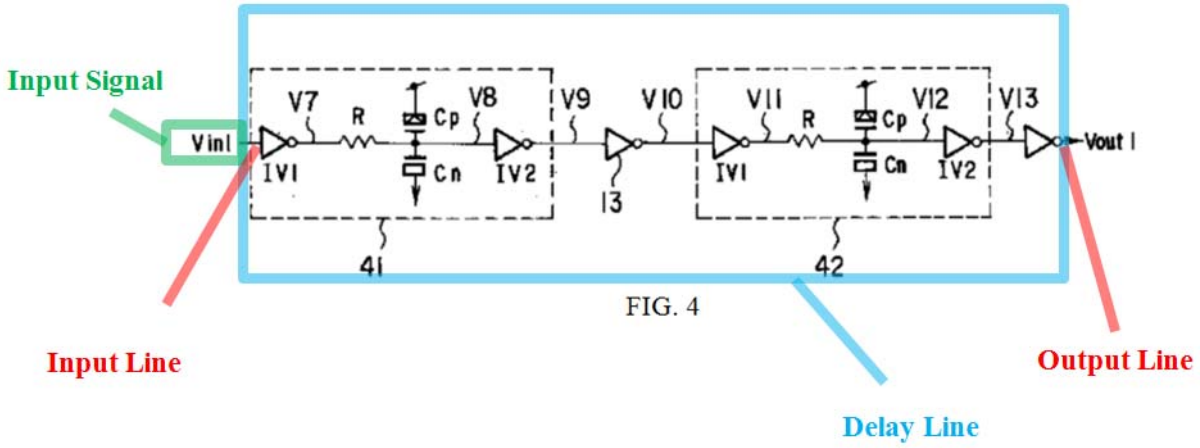
A POSITA would have understood that different numbers of CMOS delay inverters could be included in each of the delay blocks in order to adapt the amount of delay through the delay blocks to suit the application in which the variable delay line was used. (Ex. 1002, ¶148.) For example, while a small number of variable delay inverters would be adequate for certain applications, other applications requiring longer delays would require more delay inverters. Therefore, a POSITA would have understood that selecting the number of CMOS delay inverters to include in the delay line is nothing more than a design choice, where the number of inverters is chosen in order to provide the appropriate amount of delay for the application in which the delay line is used. (*Id*.) A POSITA would also have recognized that no special adaptations or additional design effort is required in order to modify the number of CMOS delay inverters included in the delay line, thereby making the design choice and implementation of that choice within the capabilities of a person of ordinary skill in the art. (*Id.*, ¶142)

Because it would have been obvious to modify the delay blocks 41 and 42 in figure 4 of Ogiwara to each include at least ten CMOS delay inverters as modified based on Dally, the Ogiwara-Noda-Dally combination discloses or suggests the features of claim 9. (Ex. 1002, ¶147.)

4. Claim 10

a) The delay line as in claim 5 in which the input signal comprises an input clock signal.

Ogiwara in view of Noda and Dally discloses or suggests this feature. (Ex. 1002, ¶¶149-153.) As discussed above with respect to claim 5, Ogiwara discloses a delay line that delays the input signal Vin1. (*See, e.g., supra* Section IX.A.1(a).)



(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶149.)

Ogiwara does not explicitly disclose that input signal Vin1 is a "clock signal." However, it would have been obvious in view of Dally to provide a "clock signal" as the input signal to the delay line of figure 4 of Ogiwara. (Ex. 1002, ¶150.)

As discussed above with respect to claim 6, it would have been obvious to modify the delay line of Ogiwara to make the delay through the delay elements variable as disclosed in Dally so that the delay line can be used in a delay locked loop (DLL), which was a well-known application for the variable delay line achieved by such a modification. (*See supra* Section IX.B.1; Ex. 1007, 635-639;

Ex. 1002, ¶150.) As disclosed by Dally, one use for such a DLL is a clock alignment circuit. (Ex. 1007, 635-639.) Figure 12-96 of Dally, replicated below, shows such a DLL-based clock aligner, where the DLL includes a voltage-controlled delay line labeled "VCDL."

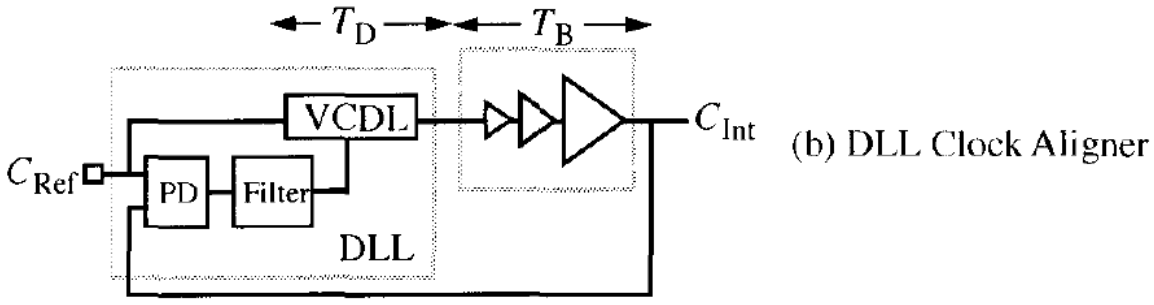


FIGURE 12-96 Clock Aligner Implementations

(*Id.,* FIG. 12-96.)

As shown in figure 12-96 of Dally, the input to the voltage controlled delay line (VCDL) is the signal CREF, which is a reference **clock**. (*Id.,* 635-639.) For example, Dally states "[i]n a simple DLL-based clock aligner, a variable delay is inserted between the reference clock and the chip's internal clock buffer; its purpose is actually to shift the phase of the reference clock to cancel the phase shift in the buffer." (*Id.,* 638; Ex. 1002, ¶151.)

Indeed, the utility of variable delay lines in DLLs to perform phase alignment of clock signals as disclosed by Dally is recognized by the '559 patent as being well-known at the time of the alleged invention. (Ex. 1001, 1:22-45.) In that context, the '559 patent states, "the DLL is operational to adjust one or more

control voltages applied to a voltage controlled delay line until the two clock signals are perfectly in phase." (*Id.*, 1:43-46; Ex. 1002, ¶152.)

Therefore, the Ogiwara-Noda-Dally combination discloses using the Ogiwara-Noda-Dally variable delay line as a voltage-controlled delay line (VCDL) in a DLL-based clock aligner. In such a configuration, the input Vin1 is a clock signal. (Ex. 1002, ¶153.)

5. Claim 11

a) The delay line as in claim 5 in which each of the delay elements comprises a voltage-controlled CMOS inverter.

Ogiwara in view of Noda and Dally discloses or suggests this feature. (Ex. 1002, ¶154.) As discussed above with respect to claim 6, a POSITA would have been motivated to modify the delay line shown in figure 4 of Ogiwara based on Dally to make the delay through the delay line variable. (*See supra* Section IX.B.1.) As detailed in the analysis for claim 6, a POSITA would have been motivated to modify the CMOS inverters IV1 and IV2 shown in the delay blocks 41 and 42 of Ogiwara to be voltage-controlled CMOS inverters as disclosed in Dally. (*Supra* Section IX.B.1.) Therefore, the Ogiwara-Noda-Dally combination discloses or suggests a delay line where "each of the delay elements comprises a voltage-controlled CMOS inverter" as recited in the claim 11.

6. Claim 15

a) The delay line as in claim 14 in which the delay line further comprises means for varying the delay of the input signal.

The Ogiwara-Noda-Dally combination discloses or suggests this feature for the same reasons as those discussed above for claim 6. (Ex. 1002, ¶155; *supra* Section IX.B.1.)

7. Claim 17

a) The delay line as in claim 14 in which each of the delay elements comprises a voltage-controlled CMOS inverter.

The Ogiwara-Noda-Dally combination discloses or suggests this feature for the same reasons as those discussed above for claim 11. (Ex. 1002, ¶156; *supra* Section IX.B.5.)

8. Claim 1

a) A variable delay line for delaying an input clock signal between input and output lines thereof, the delay line comprising:

To the extent the preamble is limiting, Ogiwara in view of Dally discloses or suggests this feature. (Ex. 1002, ¶¶157-158.) As discussed above with respect to claim element 5[a], Ogiwara discloses a "delay line for delaying an input . . . signal between input and output lines thereof." (*See supra* Section IX.A.1(a).)

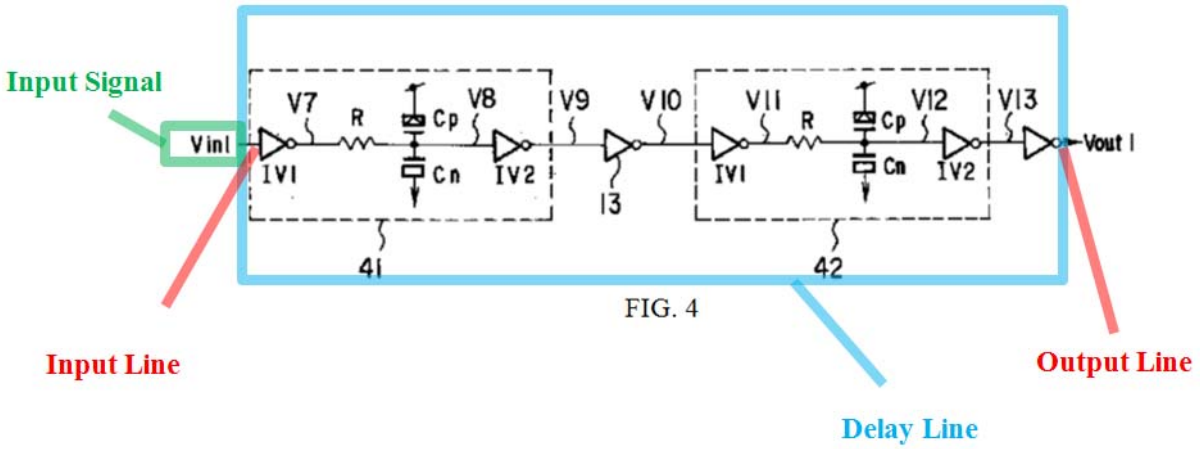


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶157.)

But Ogiwara does not disclose that the delay line is a "variable" delay line or that the input signal is a "clock" signal, as recited in the preamble of claim 1. (Ex. 1002, ¶158.) However, as discussed above with respect to claim 6, it would have been obvious to make the delay line of Ogiwara a "variable" delay line by modifying the inverters IV1 and IV2 in each of the delay blocks 41 and 42 to have a variable delay. (*See supra* Section IX.B.1.) Specifically, as discussed above with respect to claim 6, a POSITA would have found it obvious to combine the teachings of Ogiwara and Dally to use voltage controlled inverters for inverters IV1 and IV2 so that the inverters have a variable delay like in Dally. (*See supra* Section IX.B.1.) Furthermore, as discussed above with respect to claim 10, it would have been obvious to use the combined Ogiwara-Dally variable delay line in a DLL in which the input signal is a "clock" signal. (*See supra* Section IX.B.4.)

Therefore, the Ogiwara-Dally combination discloses or suggests claim element 1[a] for reasons similar to those discussed above with respect to claims 6 and 10. (*Id.*, ¶158.)

b) first and second separate blocks of voltage-controlled CMOS delay inverters coupled in series to receive said input clock signal on said input line

The Ogiwara-Dally combination discloses or suggests claim element 1[b]. (Ex. 1002, ¶¶159-162.) As discussed above with respect to claim element 5[b], Ogiwara discloses "first and second blocks of delay elements" to receive the input signal VIN1 on the input line. (*See supra* Section IX.A.1(b).) The first and second blocks of delay elements are "separate" and "coupled in series." (*Id.*, Ex. 1006, FIG. 4.)

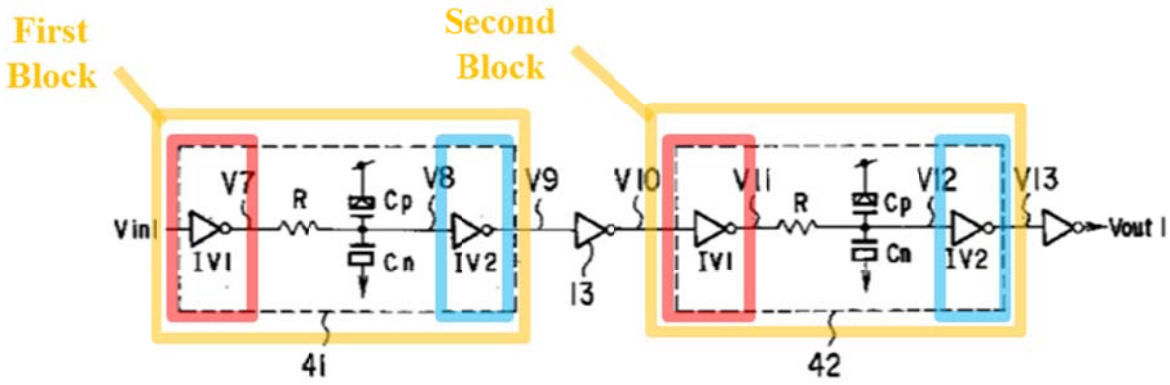


FIG. 4

(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶159.)

Each of the first and second blocks of delay elements includes CMOS delay inverters IV1 and IV2. (*Supra* Section IX.A.2 (analysis for claim 8).) As discussed above with respect to the preamble of claim 1, it would have been obvious to combine Ogiwara and Dally to make the CMOS inverters IV1 and IV2 voltage controller inverters that have a delay that can be varied by changing a control voltage. (*See supra* Sections IX.B.8(a), IX.B.1, IX.B.2, and IX.B.5.) Therefore, Ogiwara's "first and second blocks" (as shown in the annotated figure above) in the Ogiwara-Dally combination are "first and second separate blocks of voltage-controlled CMOS delay inverters" because they include voltage-controlled CMOS delay inverters.

Moreover, as discussed above with respect to the preamble, it would have been obvious to use the combined Ogiwara-Dally variable delay line in a DLL in which the input signal is a "clock" signal. (*See supra* Section IX.B.8(a).)

Therefore, the Ogiwara-Dally combination discloses claim element 1[b]. (Ex. 1002, ¶162.)

> c) wherein the propagation delay of individual said delay inverters in each of said first and second blocks are at least partially non-identical and

The Ogiwara-Dally combination discloses or suggests this feature. (Ex. 1002, ¶¶163-167.) For example, in each of the blocks of delay elements, the propagation delay of the first delay inverter, inverter IV1 (as modified in view of

Dally), is different than the propagation delay of the second delay inverter, IV2 (as modified in view of Dally) ("propagation delay of individual said delay inverters in each of said first and second blocks are at least partially non-identical"). As discussed in detail below, the propagation delay of the inverters is non-identical at least in part because the input drive to each of the inverters IV1 and IV2 is different.

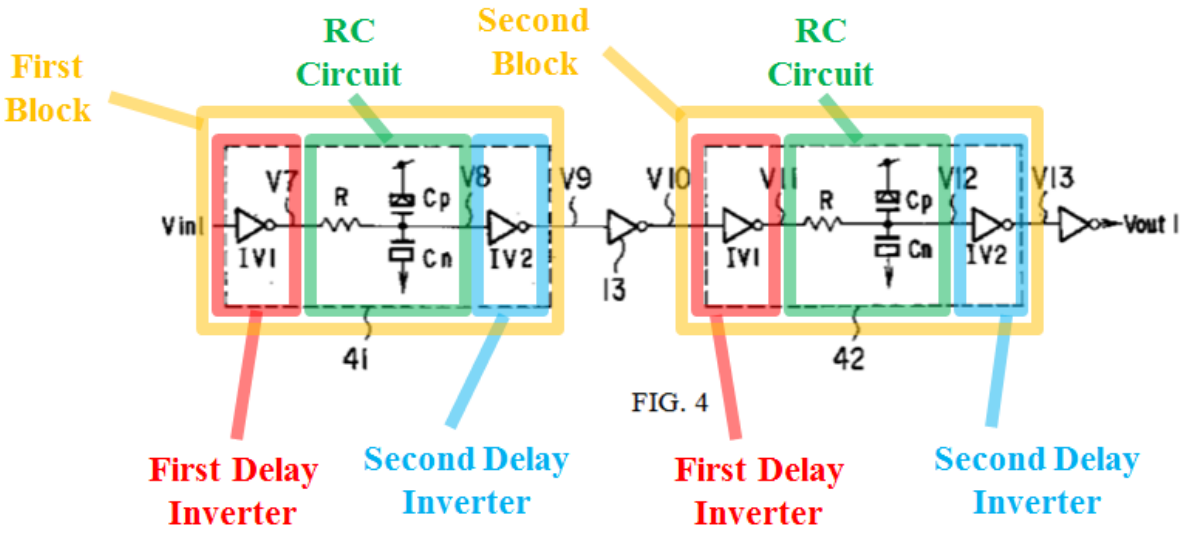


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶163.)

The specification of the '559 patent is not explicit as to how the propagation delay of the individual delay inverters in the blocks of delay elements are "at least partially non-identical." However, as discussed above with respect to claim element 5[c], the '559 patent indicates that circuit elements with the same input drive and same layout will have the same propagation delay. (*See supra* Section IX.A.1(c).)

As is apparent from figure 4 of Ogiwara, while the layout of the inverters IV1 and IV2 may be the same, the input drive to each inverter is different. The presence of the RC circuit, which includes resistor R and capacitors Cp and Cn, at the input of IV2 in each of the delay blocks presents different loading on the input drive to IV2 than is present for IV1. As such, a POSITA would have recognized that, consistent with the disclosure of the '559 patent, the propagation delay through inverter IV2, which has more input loading than inverter IV1, is different than the propagation delay of inverter IV1. Because the propagation delay of first and second delay inverters ("individual said delay inverters") in figure 4 of Ogiwara as modified by Dally are different, the propagation delay of those delay inverters is "at least partially non-identical" as recited in claim element 1[c]. (Ex. 1002, ¶165.) Moreover, the '559 patent confirms that it is extremely difficult for two voltage-controlled inverters inside a block to have identical propagation delays. (Ex. 1001, 4:22-32.)

The prosecution history of U.S. Patent 6,339,354 ("the '354 patent), which is the parent patent to the '559 patent, confirms that the inclusion of the RC circuit between the inverters in each of the delay blocks in Ogiwara results in non-identical delay through the inverters. For example, during prosecution of the '354 patent, Applicant argued that "Claim 1 calls for a delay line with first and second block so delay elements in which odd-even pairs of said delay elements are at least

partially non-identical." (Ex. 1005, 127, emphasis omitted.) Applicant further noted that "[i]n prior art devices, control over pulse width for a signal propagated through a delay line was achieved typically by attempting to fabricate each odd-even pair of delay inverters to be identical and with parasitic loading between all inverters being the same." (*Id*., emphasis added.) Applicant further argued that "[t]he claimed invention overcomes the need for matching at the individual inverter level by not requiring odd-even matching." (*Id*.) As is apparent from figure 4 of Ogiwara, the loading of the first and second inverters is not the same, and therefore there is not even-odd pair matching within the delay block. Based on the disclosure of the '559 patent and corresponding prosecution histories, the "propagation delay of individual said delay inverters in each of said first and second blocks are at least partially non-identical" is established by the lack of even-odd pair matching that is shown in figure 4 of Ogiwara.

Notably, modifying the inverters IV1 and IV2 to be variable-delay inverters as disclosed in Dally does not impact the propagation delay of the inverters being non-identical as discussed above. In the Ogiwara-Dally combination, each of the inverters IV1 and IV2 in each of the delay blocks 41 and 42 is modified in the same manner such that the layouts and propagation delays through the inverters as modified are changed in the same manner. (Ex. 1002, ¶167.)

d) said first and second blocks have substantially identical block level integrated circuit layouts;

Ogiwara in combination with Dally and Noda discloses or suggests this feature. (Ex. 1002, ¶¶168-169.) As discussed above with respect to claim element 5[d], the delay circuit elements 41 and 42 have "substantially identical block level integrated circuit layouts." (*Supra* Section IX.A.1(d).) Even though inverters IV1 and IV2 in delay circuit elements 41 and 42 are modified to make them voltage controlled inverters in view of Dally, (*supra* Section IX.B.8(a)), the analysis for claim element 5[d] is still applicable here because each of the inverters IV1 and IV2 in each of the delay blocks 41 and 42 is modified in the same manner to make the inverters voltage-controlled CMOS inverters. Indeed, to simplify design as set forth in Ogiwara, a POSITA would have ensured, given such a person's knowledge and Noda, that the modification of IV1 and IV2 based on Dally still results in blocks 41 and 42 (modified based on Dally) having the same circuit components interconnected in the identical manner and having the same layout. (*See supra* Section IX.A.1(d) (explaining that it would have been obvious in view of a POSITA's knowledge and Noda to use the same layout for blocks 41 and 42).)

e) a first inverter coupled to an output of said first block of delay inverters for providing an inverted delayed signal to said second block of delay inverters;

The Ogiwara-Dally-Noda combination discloses or suggests this feature for reasons similar to that discussed above with respect to claim element 5[e]. (*Supra* Section IX.A.1(e); Ex. 1002, ¶170.)

f) a second inverter coupled to an output of said second block of delay inverters for providing a re-inverted delayed signal on said output line; and

The Ogiwara-Dally-Noda combination discloses or suggests this feature for reasons similar to that discussed above with respect to claim element 5[f]. (*Supra* Section IX.A.1(f); Ex. 1002, ¶171.)

g) wherein said first and second inverters are non-voltage controlled inverters having substantially equivalent parasitic loading and the same inverter layout.

The Ogiwara-Dally-Noda combination discloses or suggests this feature. (Ex. 1002, ¶172.) As explained above with respect to claim elements 5[e] and 5[f], the two inverters outside of the delay blocks 41 and 42 are "non-voltage controlled inverters." (*Supra* Section IX.A.1(e), (f).) Furthermore, as discussed above with respect to claims 12 and 13, it would have been obvious to configure the two inverters to have substantially equivalent parasitic loading and the same inverter layout. (*Supra* Sections IX.A.3, IX.A.4.) While the analysis for claims 12 and 13 is presented in the context of the Ogiwara-Noda combination, the addition of Dally

to this combination does not affect the analysis for those claims and the analysis for claims 12 and 13 applies equally for claim element 1[g].

9. Claim 2

a) The variable delay line as in claim 1 in which the CMOS delay inverters each further comprises a control terminal for receiving a control signal.

The Ogiwara-Dally-Noda combination discloses or suggests this feature for the same reasons as discussed above for claim 7. (Ex. 1002, ¶173; *supra* Section IX.B.2.)

10. Claim 3

a) The variable delay line as in claim 1 in which the first and second blocks each comprises an even number of CMOS delay inverters.

The Ogiwara-Dally-Noda combination discloses or suggests this feature. (Ex. 1002, ¶¶174-175.) As shown in figure 4 of Ogiwara, the first delay circuit 41 ("first block of delay elements") and the second delay circuit 42 ("second block of delay elements") each include two delay inverters IV1 and IV2, which in the Ogiwara-Dally-Noda combination are modified to have variable delay. (*Supra* Section IX.B.8.)

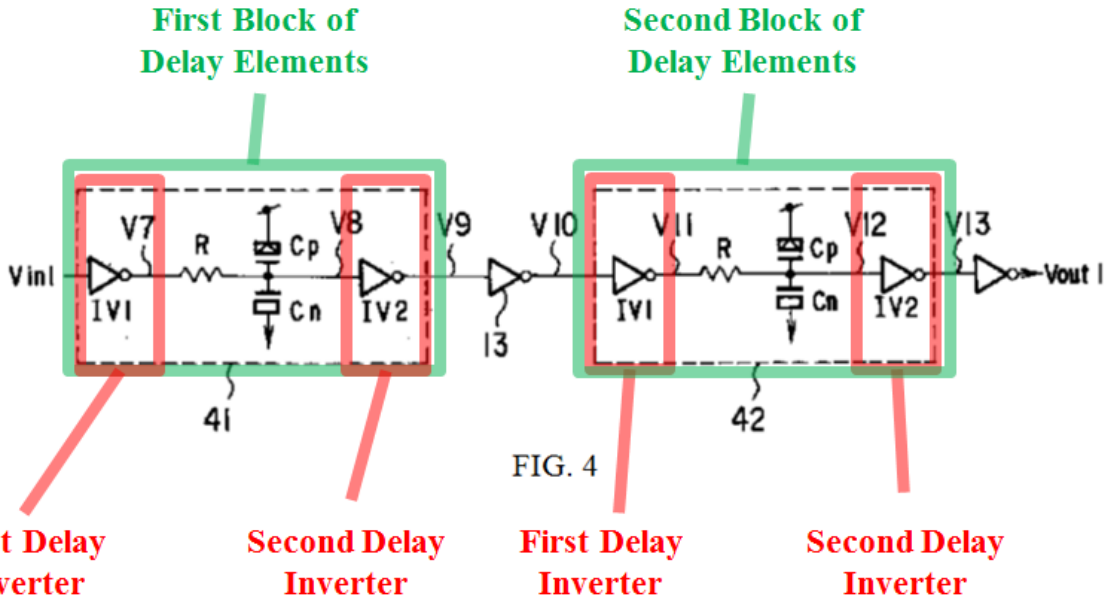


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶174.)

As discussed above with respect to claim element 1[b], as modified, inverters IV1 and IV2 are "voltage-controlled CMOS delay inverters." (*See supra* Section IX.B.8[b].) Therefore, each of the first and second blocks of delay elements (i.e., blocks 41 and 42 in the Ogiwara-Noda-Dally combination) includes two ("an even number") of CMOS delay inverters. (*Id.*, ¶175.)

11. Claim 4

a) The variable delay line as in claim 1 in which the first and second blocks each comprises at least ten CMOS delay inverters.

The Ogiwara-Dally-Noda combination discloses or suggests this feature for the same reasons as discussed above for claim 9. (Ex. 1002, ¶176; *supra* Section IX.B.3.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-17 of the '559 patent based on the ground specified in this petition.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(b)(1), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,469,559 contains, as measured by the word-processing system used to prepare this paper, 13,879 words. This word count excludes the Table of Contents, Table of Authorities, List of Exhibits, Certificate of Compliance, and Certificate of Service.

Respectfully submitted,

Dated: March 5, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 5, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,469,559 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

Hogan Lovells US LLP – Colorado Springs
Two North Cascade Avenue
Suite 1300
Colorado Springs, CO 80903

A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

Craig Kaufman (ckaufman@tklg-llp.com)
Jerry Chen (jchen@tklg-llp.com)
Tom Gray (tgray@tklg-llp.com)
Kevin Jones (kjones@tklg-llp.com)
Kai Tseng (ktseng@tklg-llp.com)
TechKnowledge Law Group LLP
100 Marine Parkway, Suite 200
Redwood Shores, CA 94065

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner