UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

NUCURRENT, INC.,
Patent Owner

Patent No. 8,680,960

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,680,960

TABLE OF CONTENTS

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 8,680,960
Ex. 1002	Declaration of Dr. Steven Leeb
Ex. 1003	Curriculum Vitae of Dr. Steven Leeb
Ex. 1004	Prosecution History of U.S. Patent No. 8,680,960
Ex. 1005	U.S. Patent Application Publication No. 2007/0267718 A1 ("Lee")
Ex. 1006	Semat and Katz, *Physics*, Chapters 29-32 (1958)
Ex. 1007	RESERVED
Ex. 1008	RESERVED
Ex. 1009	U.S. Patent Application Publication No. 2009/0096413 A1 ("Partovi")
Ex. 1010	IEEE Standard Dictionary of Electrical and Electronics Terms, Sixth Edition (1996)
Ex. 1011	U.S. Patent Application Publication No. 2007/0089773 A1 ("Koester")
Ex. 1012	U.S. Patent Application Publication No. 2012/0280765A1 ("Kurs")
Ex. 1013	U.S. Patent No. 6,432,497
Ex. 1014	U.S. Patent No. 6,083,842
Ex. 1015	Reinhold et al., *Efficient Antenna Design of Inductive Coupled RFID-Systems with High Power Demand* (2007)
Ex. 1016	U.S. Patent No. 4,549,042
Ex. 1017	U.S. Patent No. 5,812,344
Ex. 1018	Wheeler, *Formulas for the Skin Effect* (1942)
Ex. 1019	U.S. Patent No. 7,236,080 ("Kyriazidou")

Ex. 1020	Alldred *et al.*, "A 1.2 V, 60 GHz radio receiver with onchip transformers and inductors in 90 nm CMOS," *Proc. IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 51-54, Nov. 2006 ("Alldred")
Ex. 1021	RESERVED
Ex. 1022	RESERVED
Ex. 1023	RESERVED
Ex. 1024	RESERVED
Ex. 1025	U.S. Patent Application Publication No. 2007/0126544 A1 ("Wotherspoon")
Ex. 1026	RESERVED
Ex. 1027	RESERVED
Ex. 1028	RESERVED
Ex. 1029	RESERVED
Ex. 1030	RESERVED
Ex. 1031	U.S. Patent No. 7,030,725 ("Ahn")
Ex. 1032	RESERVED
Ex. 1033	RESERVED
Ex. 1034	RESERVED
Ex. 1035	IEEE Xplore web page
Ex. 1036	Kraemer *et al.*, "Architecture Considerations for 60 GHzPulse Transceiver Front-Ends," CAS 2007 Proceedings Vol. 2, 2007 Int'l Semiconductor Conference (2007)

Ex. 1037	Varonen *et al.*, "V-band Balanced Resistive Mixer in 65-nm CMOS," *Proceedings of the 33rd European Solid-State Circuits Conference* (2007)

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-8, 10, 12-13, 15-22, and 24-30 ("the challenged claims") of U.S. Patent No. 8,680,960 ("the '960 patent") (Ex. 1001), which, according to PTO records, is assigned to NuCurrent, Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claim should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Related Matters: The '960 patent is at issue in *NuCurrent, Inc. v. Samsung Electronics Co. Ltd.* and *Samsung Electronics America, Inc.*, Case No. 1:19-cv-00798-DLC (S.D.N.Y.). The '960 patent shares the same specification as U.S. Patent No. 8,698,591 ("the '591 patent"); U.S. Patent No. 8,710,948 ("the '948 patent"); and U.S. Patent No. 9,300,046 ("the '046 patent"). Petitioner is concurrently filing petitions challenging these patents. Moreover, Patent Owner has also asserted U.S. Patent No. 9,941,729 ("the '729 patent") in the above litigation.

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel is (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan

R. Bansal (Limited Recognition No. L0667), and (3) Howard Herr (*pro hac vice* admission to be requested). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-NuCurrent-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '960 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-8, 10, 12-13, 15-22, and 24-30 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-8, 10, 15-22, and 24-30 are unpatentable under pre-AIA 35 U.S.C. § 102 as anticipated by U.S. Patent Application Publication No. 2007/0267718 A1 to Lee ("Lee") (Ex. 1005); and

Ground 2: Claim 12 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent No. 7,030,725 to Ahn ("Ahn") (Ex. 1031); and

Ground 3: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent No. 7,236,080 ("Kyriazidou") (Ex. 1019); and

Ground 4: Claim 24 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") (Ex. 1009); and

Ground 5: Claims 1-8, 10, 15-22, and 25-30 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee and Alldred *et al.*, "A 1.2 V, 60 GHz radio receiver with onchip transformers and inductors in 90 nm CMOS," *Proc. IEEE Compound Semiconductor Integrated Circuits Symp.*, pp. 51-54, Nov. 2006 ("Alldred") (Ex. 1020); and

Ground 6: Claim 12 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee, Alldred, and Ahn; and

Ground 7: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Lee, Alldred, and Kyriazidou.

The '960 patent issued from U.S. patent application no. 13/797,387 (the '387 application"), filed March 12, 2013. (Ex. 1001, Cover.) The '960 claims priority to a series of related applications, including Provisional Application No. 61/158,688, filed March 9, 2009. For purposes of this proceeding only, Petitioner assumes the earliest effective filing date of the '960 patent is March 9, 2009.

Lee was published November 22, 2007. (Ex. 1005, Cover.) Kyriazidou was issued on June 26, 2007 (Ex. 1019, Cover.). Ahn issued on April 18, 2006 (Ex. 1031, Cover.)

Therefore, Lee, Kyriazidou, and Ahn are prior art under pre-AIA 35 U.S.C. § 102(b). Partovi was filed May 7, 2008. (Ex. 1009, Cover). Therefore, Partovi is prior art under pre-AIA 35 U.S.C. § 102(e).

Alldred is an IEEE publication that was publicly available to persons interested and skilled in the art in 2006, and at a minimum before March 9, 2009. The Board has routinely held that IEEE publications like Lee are printed publications. For example, "[t]he Board has previously observed that 'IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on the information published on the copyright line of IEEE publications.'" *Power Integrations, Inc., v. Semiconductor Components Industries, LLC*, IPR2018-00377, Paper No. 10 at 10 (July 17, 2018) (quoting *Ericsson, Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 11 (May 18, 2015)). Indeed, in *Ericsson*, the Board "accept[ed] the publication information on the IEEE copyright line on page 1 of [the IEEE reference] as evidence of its date of publication and public accessibility." *Ericsson*, IPR2014-00527, Paper 41, 10-11; *see also Coriant (USA)*

Inc. v. Oyster Optics, LLC, IPR2018-00258, Paper 13 at 11 (June 6, 2018); *Microsoft Corp. v. Bradium Techs. LLC*, IPR2016-00449, Paper 9 at 13 (PTAB July 27, 2016) (noting generally that "IEEE publications, such as the one in which Reddy appeared, are distributed widely and intended to be accessible to the public").

Here, Alldred bears the marking "©2006 IEEE" at the top of the title page (page 1) and the footer of the first page of the article, and the copyright page bears the marking "Copyright © 2006 by The Institute of Electrical and Electronics Engineers, Inc." (Ex. 1020, title page (page 1), copyright page (page 3); *see also* Ex. 1035 at 1 ("Published in: 2006 IEEE Compound Semiconductor Integrated Circuit Symposium" and "Date Added to IEEE Xplore: 26 February 2007" and "Publisher: IEEE").) With such markings, Alldred is similar to a reference that the Board recently found is a printed publication in *Microsoft Corp. v. Koninklijke Philips N.V.*, IPR 2017-00890, Paper 49 at 19 (Sept. 6, 2018). Moreover, several IEEE publications that were published before the alleged invention date of the '960 patent, and that do not have any co-authors in common with Alldred, cite to Alldred, demonstrating that Alldred was publicly accessible before March 9, 2009. (Ex. 1036 at copyright page (page 3) ("Copyright © 2007 by the Institute of Electrical and Electronics Engineers."), 428 (citation [9] is to Alldred and includes a date of "2006"); Ex. 1037 at ii ("Copyright © 2007 by the Institute of Electrical

and Electronics Engineers, Inc."), 363 (citation [3] is to Alldred and includes a date of "Nov. 2006").)

Therefore, for all of the foregoing reasons, Alldred is a printed publication and qualifies as prior art under pre-AIA 35 U.S.C. § 102(b) by virtue of its publication in 2006, or at least under pre-AIA 35 U.S.C. § 102(a) by virtue of its publication before March 9, 2009 (e.g., as demonstrated by citations in various other references to Alldred as discussed above).

None of these references were considered by the Patent Office during prosecution of the '960 patent. (*See*, *e.g.*, Ex. 1001, Cover ("References Cited"); Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '960 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering, or a similar discipline and at least two years additional relevant experience with power electronics, including design or manufacturing of inductors. (Ex. 1002, ¶¶15-16.)[1] More education can supplement practical experience and vice versa. (*Id.*)

[1] Petitioner submits the declaration of Dr. Steven Leeb (Ex. 1002), an expert in the field of the '960 patent. (Ex. 1002, ¶¶1-16; Ex. 1003.)

VII. OVERVIEW OF THE '960 PATENT AND THE PRIOR ART

A. The '960 Patent

The '960 patent, titled "Multi-layer-multi-turn structure for high efficiency inductors," is directed to "an inductor having a plurality of conductor layers separated by insulator layers," "for incorporation within electric circuits." (Ex. 1001, Abstract, 1:36-39, 4:22-23; *see also id.* at 4:24:25 (disclosing the inductor described is "most notably" for "electrical circuits that operate within and above the radio frequency range of at least 3 kHz"); Ex. 1002, ¶¶30-34.) The '960 patent discloses that one of its objectives is "reducing resistance loss . . . of the inductor structure" with a "multi-layer wire configuration." (Ex. 1001, 4:15-21.)

With reference to figure 1, the '960 patent discloses "a high-level diagram of an inductor 100 for use in an electronic or electrical circuit . . . compris[ing] a coil 102 and a multi-layer wire 104, that "may have a plurality of turns 122 . . . around a central axis point 124." (*Id.*, 15:8-11, 16:32-37.)

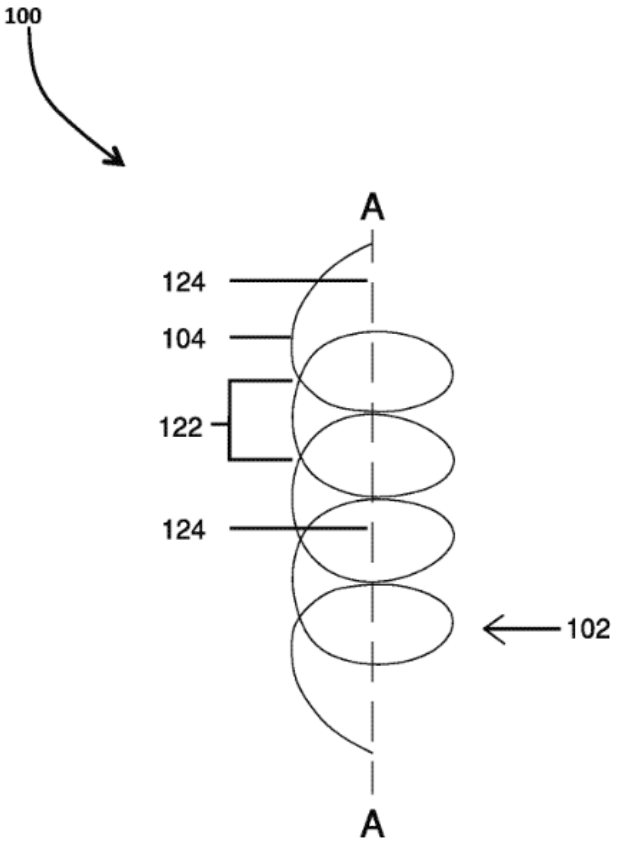


FIG. 1

(*Id.*, FIG. 1.)

The ’960 patent further discloses various embodiments including “a double turn circular spiral-solenoidal coil” in figure 3B “where each turn has N layers,” and “where ‘N’ is a number equal to or greater than one.” (*Id.*, FIG. 3B, 12:34-36, 16:40-47.)

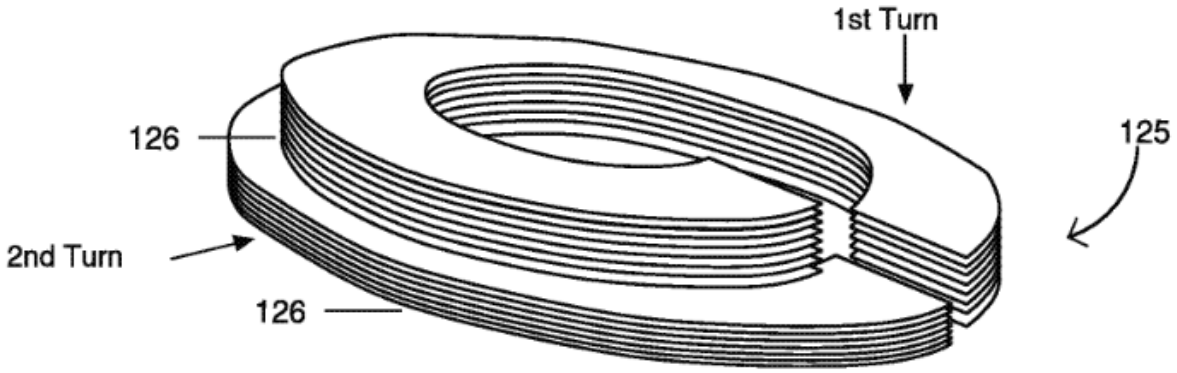


FIG. 3B

(*Id.*, FIG. 3B.)

The '960 patent admits that many properties of inductors were known. (Ex. 1002, ¶33; Ex. 1001, 1:54-64, 14:17-27; *see also* Ex. 1002, ¶¶17-25.) The '960 patent also admits that impacts of the "skin depth" phenomenon on current distribution within conductors is well known, and explains that the skin depth "defines the electrical current cross-sectional area that is [sic] carries most of the current (is active) in the conducting wire of an inductor." (*Id.*, 2:49-53.) And that "[w]ith higher frequencies, current that normally flows through the entire cross section of the wire comprising the inductor becomes restricted to its surface," thereby increasing resistance. (Ex. 1001, 2:60-66; Ex. 1002, ¶34.)

B. Lee

Lee relates to "a multilayer winding inductor" with "a plurality of looped conductive traces overlapping and separated from each other" and "a multi-level interconnect structure." (Ex. 1005, Abstract, ¶[0004]; Ex. 1002, ¶¶36-39.)

Lee discloses a top-down view of an embodiment of a multilayer winding inductor in figure 4A and a cross-section along line 4C-C' in figure 4C, which reveals the multilayer structure inside. (*Id.*, ¶[0031]; Ex. 1002, ¶37.)

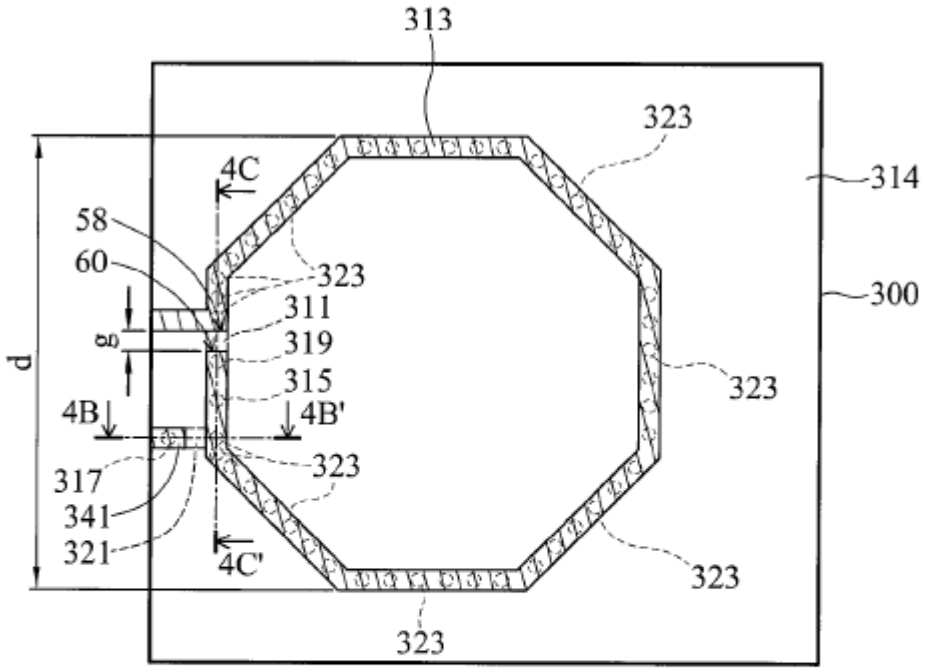


FIG. 4A

(Ex. 1005, FIG. 4A.)

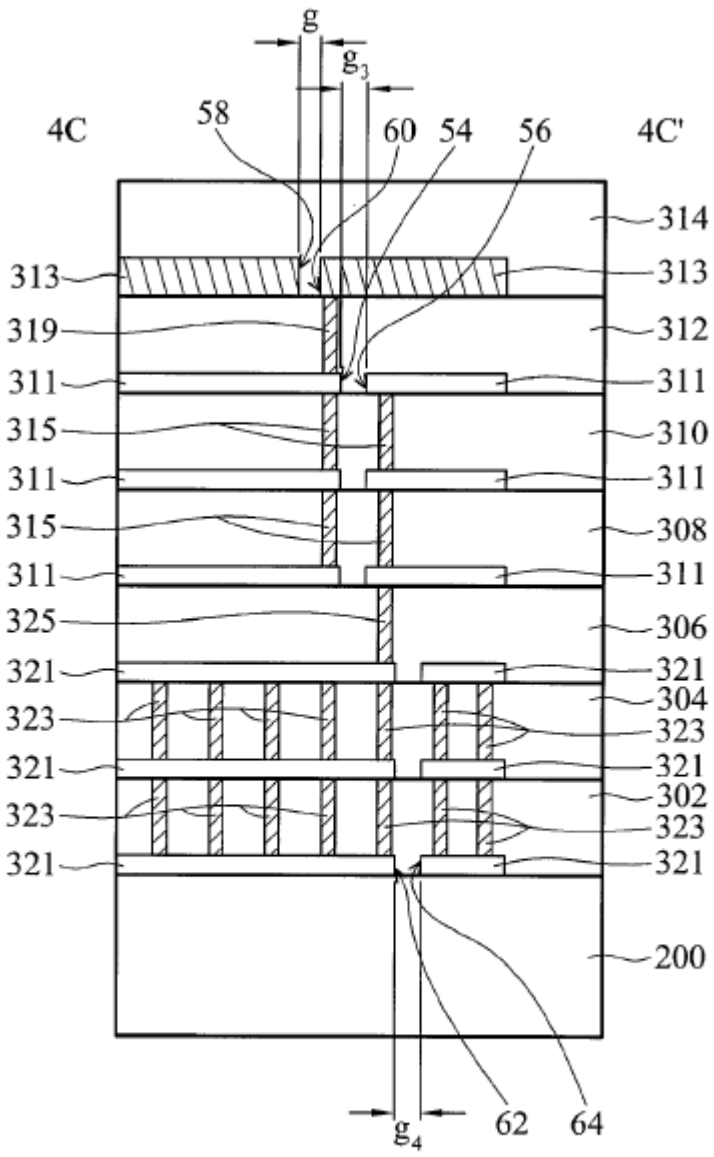


FIG. 4C

(Ex. 1005, FIG. 4C.)

Lee discloses that the inductor "includes two multi-level interconnect structures . . . embedded in an insulating layer on a substrate." (*Id.*, ¶[0031].) The interconnect structures further include "looped conductive traces" 311 and 321, and conductive plugs 323 and 325. (*Id.*, ¶[0031].) The conductive traces and plugs "may be copper, aluminum, or a combination thereof." (*Id.*, ¶[0033].) Lee also discloses that the insulating layer "may be dielectric layers 302, 304, 306, 308, 310, 312, and 314 successively deposed on the substrate." (*Id.*)

Lee further discloses that "external or internal circuits provide a current passing through the lower multi-level interconnect structure . . . and utilize the inductance induced by the inductor. (*Id.*, ¶[0034].) And "since the inductor includes two overlapping lower conductive traces, higher inductance can be obtained." (*Id.*, ¶[0035].)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the

claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002, ¶35.)

[2] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '960 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

IX. DETAILED EXPLANATION OF GROUNDS

As discussed below, claims 1-8, 10, 12, 13, 15-22, and 24-30 are unpatentable in view of the prior art. (Ex. 1002, ¶¶40-146.)

A. Ground 1: Lee Anticipates Claims 1-8, 10, 15-22, and 24-30

1. Claim 1

Preamble: An inductor comprising:

Lee discloses this limitation. (Ex. 1002, ¶41.) For example, Lee discloses a multi-layer "winding inductor." (*See*, *e.g.*, Ex. 1005, ¶[0031], FIGS. 4A-4C; Ex. 1002, ¶41; *see also supra* Section VII.B.) A plan view of the inductor is illustrated in figure 4A (reproduced below), showing the uppermost looped conductive trace 313 and other components. (Ex. 1005, ¶¶[0020]-[0022], [0031]-[0034], FIG. 4A.)

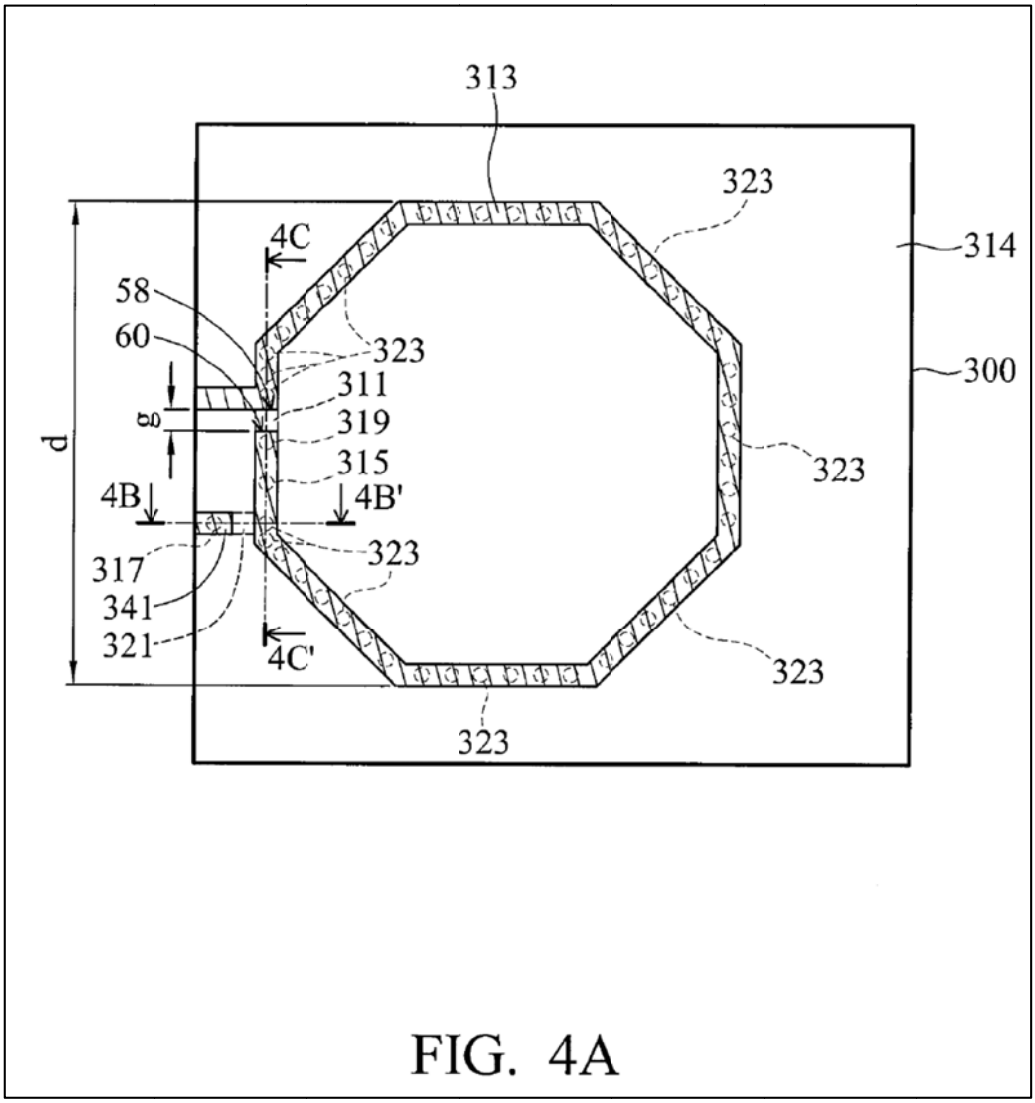


FIG. 4A

(Ex. 1005, FIG. 4A (annotated); Ex. 1002, ¶41.)

a) a first conductor layer;

Lee discloses this limitation. (Ex. 1002, ¶42.) For instance, as shown in annotated figure 4C below, Lee discloses that the inductor includes a looped conductive trace 311 ("first conductor layer"). (Ex. 1005, FIG. 4C, ¶[0031].)

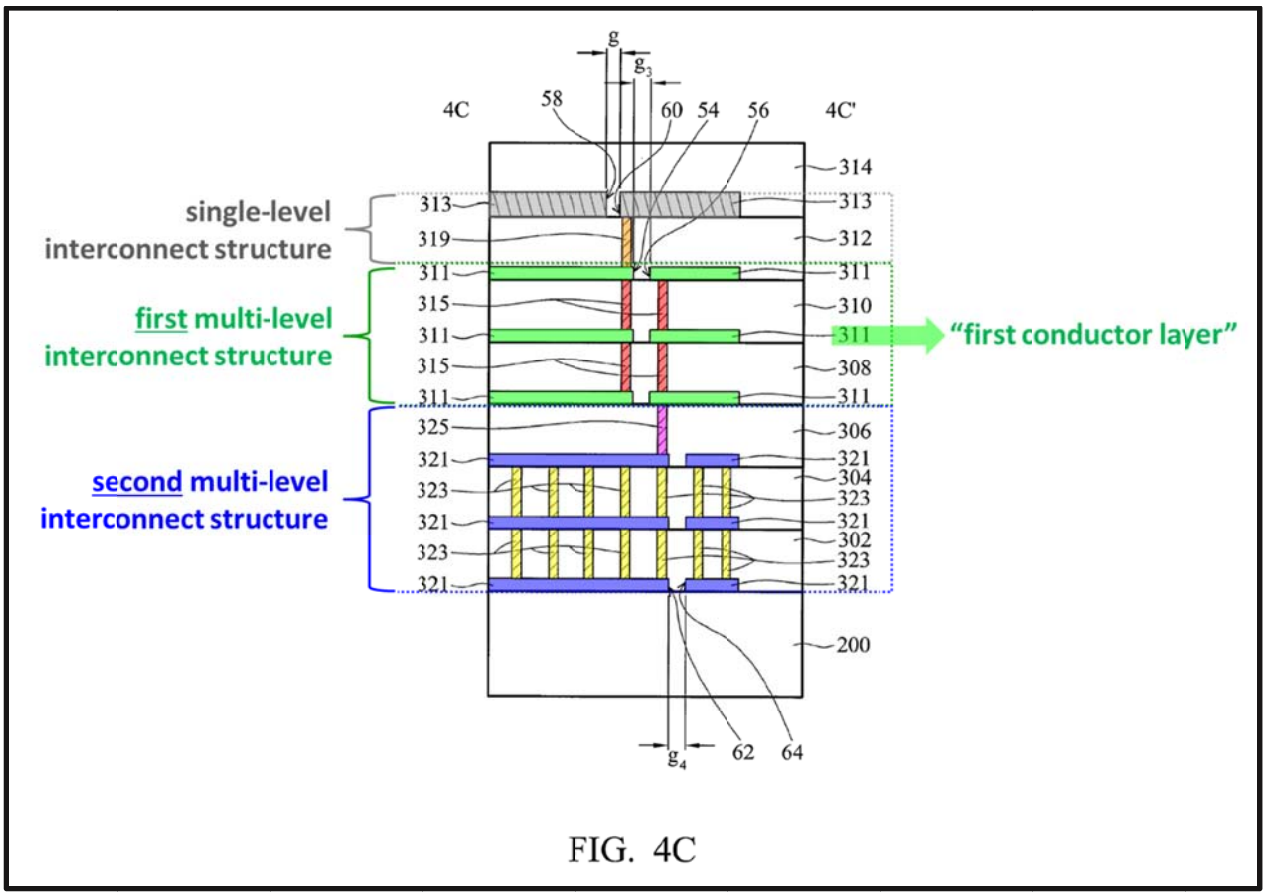


FIG. 4C

(*Id.*, FIG. 4C (annotated); Ex. 1002, ¶42.)

b) a second conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive;

Lee discloses this limitation. (Ex. 1002, ¶¶43-45.) For example, as illustrated in annotated figure 4C below, Lee discloses that the inductor includes a looped conductive trace 311 ("second conductor layer") that is embedded in dielectric layer 308. (Ex. 1005, ¶¶[0024]-[0025], [0029], [0031]; *see also id.* at ¶¶ [0026]-[0028], [0032]-[0033]; Ex. 1002, ¶43.)

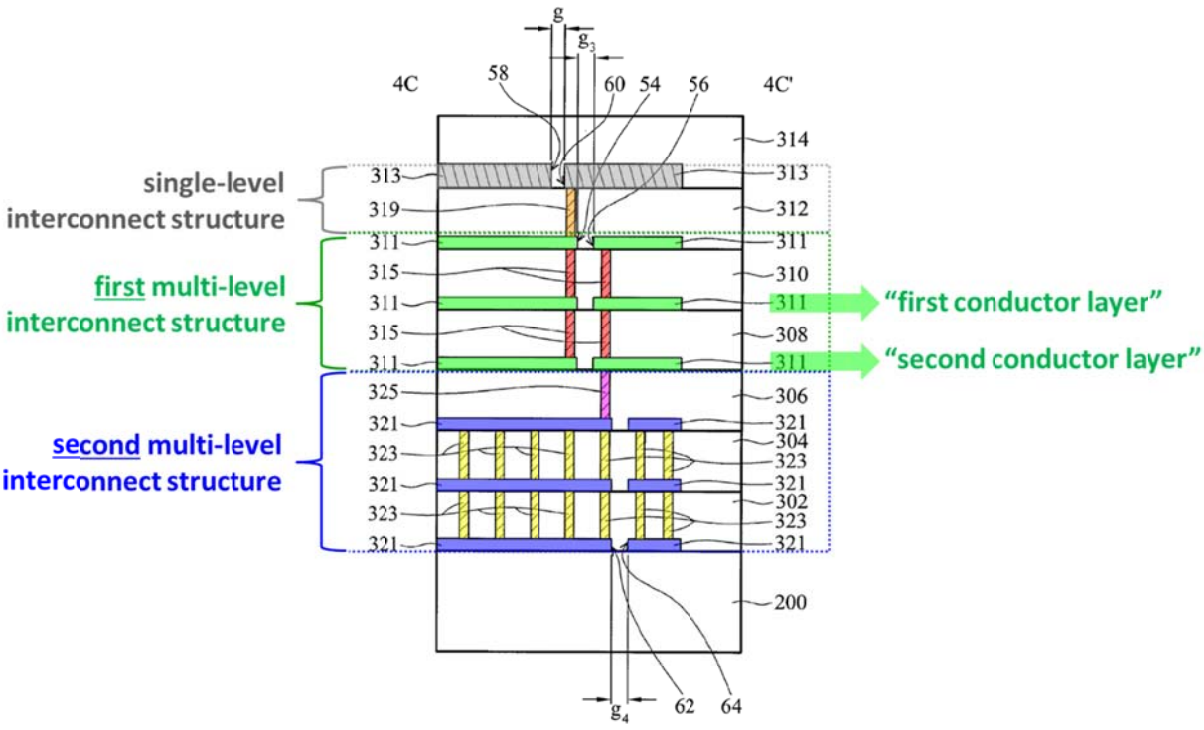


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶43.)

Furthermore, Lee discloses that the conductive traces 311 (i.e., "first conductor layer" embedded in dielectric layer 310 and "second conductor layer" embedded in dielectric layer 308) are "separated from each other." (Ex. 1005, ¶[0025][3]; *see also id*. at Abstract (disclosing "a plurality of looped conductive traces overlapping and separated from each other"), ¶[0010], claim 1; Ex. 1002,

[3] The embodiment of figures 4A-4C incorporates the disclosure of the embodiment of figures 3A-3C. (Ex. 1005, ¶[0031].)

¶44.) Indeed, a conductive plug 315 connects the two traces and provides an electrical connection between them. (Ex. 1005, FIG. 4C (annotated above), ¶[0026]; Ex. 1002, ¶44.)

Lee also discloses that these conductive traces 311 ("first conductor layer" and "second conductor layer") are electrically conductive at least because Lee describes these traces 311 as **conductive** traces formed from "copper, aluminum or combinations thereof," and further discloses a **current** may pass through these conductive traces to utilize the inductance. (*See*, *e.g.*, Ex. 1005, ¶¶[0025], [0026], [0034].) Accordingly, Lee discloses "a second conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive." (Ex. 1002, ¶45.)

c) an insulator layer positioned in the space between the first conductor layer and the second conductor layer;

Lee discloses this limitation. (Ex. 1002, ¶46.) For example, as shown in the annotated figure 4C below, Lee discloses a dielectric layer 308 ("insulator layer") positioned in the space between two conductive traces 311 ("the first conductor layer and the second conductor layer"). (Ex. 1005, ¶[0025][4] (disclosing that "[t]he multi-level interconnect is embedded in the dielectric layers 308, 310 and 312,

[4] The embodiment of figures 4A-4C incorporates the disclosure of the embodiment of figures 3A-3C. (Ex. 1005, ¶[0031].)

comprising a plurality of looped conductive traces 311 formed in the dielectric layers" and that "looped conductive traces 311 . . . are separated from each other"); Ex. 1002, ¶46.)

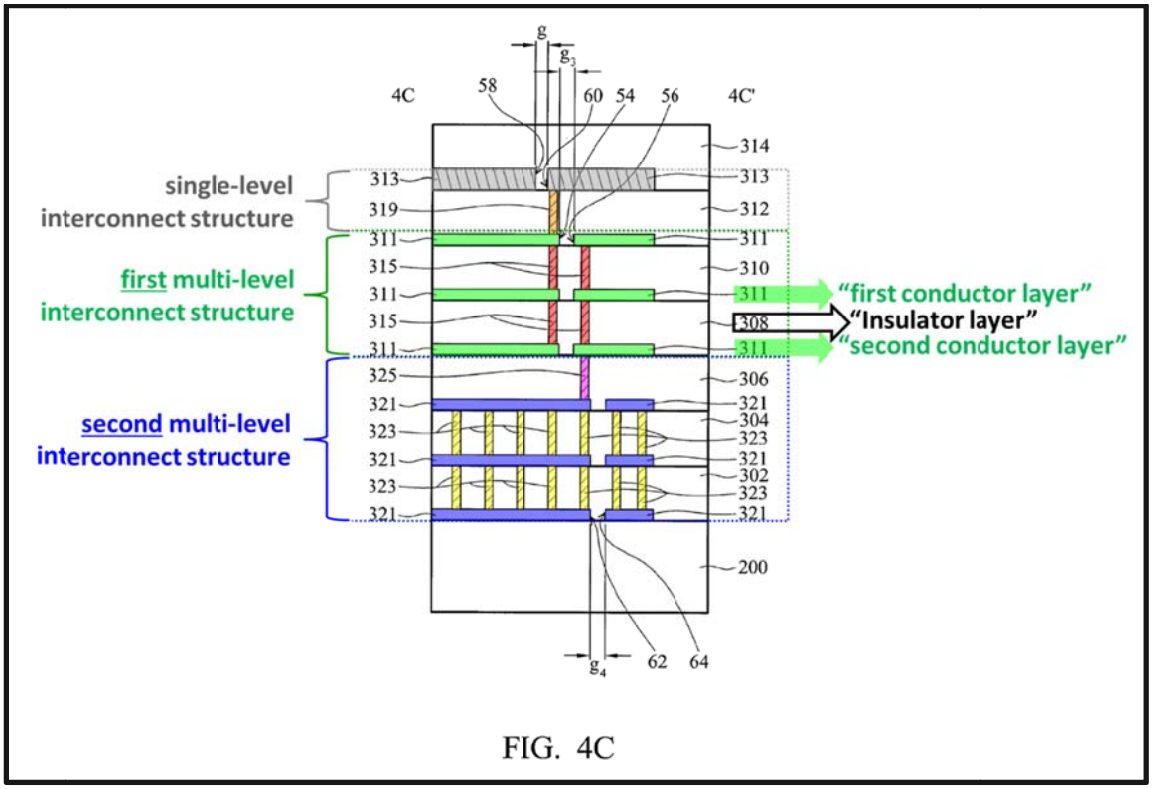


FIG. 4C

(Ex. 1005, FIG. 4C (annotated to show that dielectric layer 308 is positioned in the space between two conductive traces 311); Ex. 1002, ¶46.) It was well known to those of ordinary skill in the art that dielectric materials are electrical insulators. (Ex. 1002, ¶46.) Furthermore, Lee reflects this understanding and discloses that dielectric layer 308 is an "insulator" layer, as claimed. (Ex. 1005, ¶[0031] ("the **insulating** layer may be dielectric layers 302, 304, 306, 308, 310, 312 and 314

successively disposed on the substrate 300.") (emphasis added); *see also id*. ¶[0024]; Ex. 1002, ¶46.)

d) at least one connector electrically connecting the first conductor layer and the second conductor layer; and

Lee discloses this limitation. (Ex. 1002, ¶47.) For example, referring to the annotated figure 4C below, Lee discloses multiple conductive plugs 315 ("at least one connector") electrically connect conductive traces 311 ("the first conductor layer and the second conductor layer") that are separated by dielectric layer 308. (Ex. 1005, ¶[0026] ("The conductive plugs 315 are disposed between the looped conductive traces 311 to serve as **an electrical connection therebetween**, in which at least two conductive plugs 315 are disposed between the neighboring looped conductive traces 311.") (emphasis added); Ex. 1002, ¶47.)

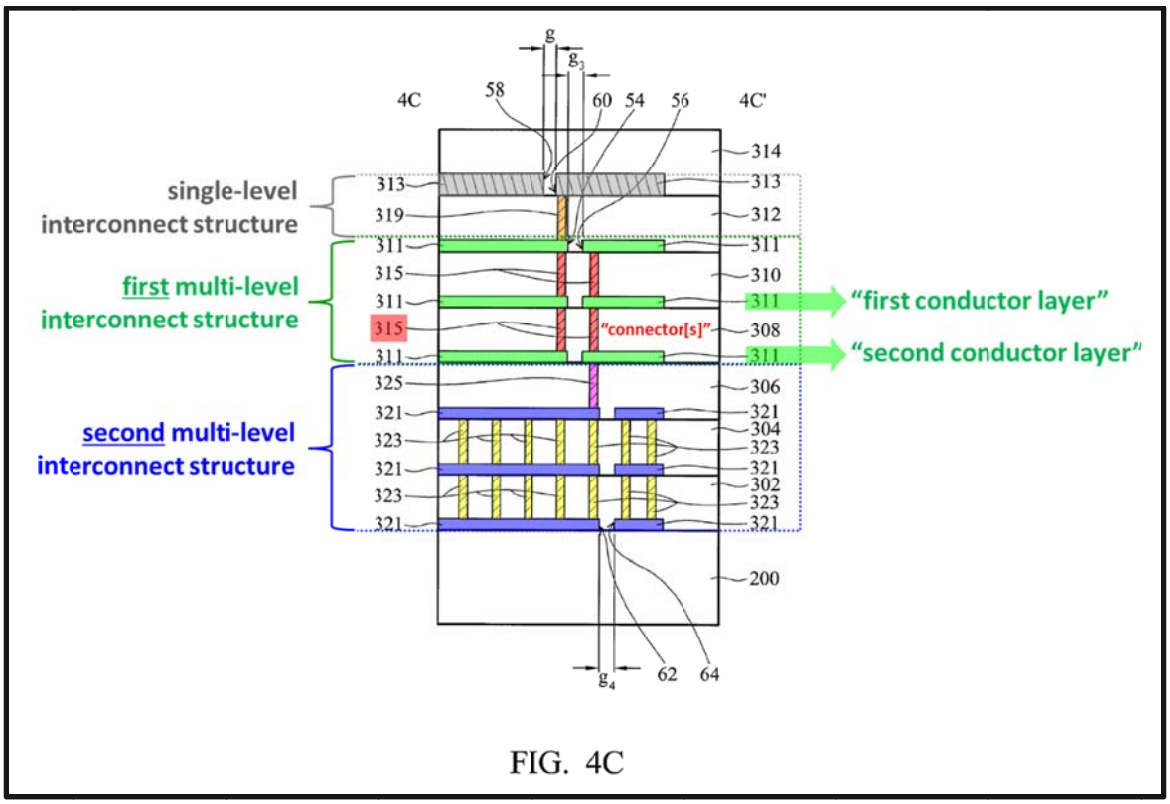


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶47.)

e) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor; and

Lee discloses this limitation in at least two ways. (Ex. 1002, ¶¶48-50.) **First**, Lee discloses that a current passes through the entire inductor of figure 4A including the "upper multi-level interconnect structure (i.e., upper conductive trace)." (Ex. 1005, ¶[0034].) The "upper conductive trace" refers to the conductive traces 311 (Ex. 1002, ¶48), which as discussed above disclose the claimed "first" and "second" conductor layer. (*Supra* Sections IX.A.1(a), (b).) A POSITA would have understood and readily recognized that the propagation of

electrical current through the inductor (including the "first conductor layer") would necessarily result in generation of magnetic flux within the inductor because that is an inherent physical property of an inductor. (Ex. 1002, ¶48.) The '960 patent reflects this understanding, and acknowledges that electric current traveling through a conductive coil will generate a magnetic flux. (Ex. 1001, 1:54-56 ("In an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current."); Ex. 1002, ¶48.)

Second, a POSITA would have understood that according to Ampère's law (also known as Ampère's circuital law, a basic and well-known physics theory), when a current passes through Lee's inductor (including a looped conductive trace 311 ("first conductor layer")), a magnetic field is generated within the inductor. (Ex. 1002, ¶49; Ex. 1006 at 566-567 (disclosing a magnetic field is generated inside a solenoid that carries a current); *see also id.*at 557-558 (explaining that it has been known since the 19th century that a magnetic field is generated by a wire carrying current), 559 (disclosing that "[i]f the current in the loop is counterclockwise when viewed from the positive x axis, the direction of the **magnetic field at the center of the loop** is perpendicular to the plane of the loop and in the positive x direction" and that the magnetic field "**inside**" a coil is "uniform and parallel to the axis of the coil") (emphases added), 560-565 (disclosing using Ampère's law to calculate the magnetic field intensity around a

current-carrying wire and a coil), 604 ("In the process of establishing a current in the circuit, a magnetic field is established in the inductor.").) The generation of a magnetic field is associated with generation of magnetic flux. (Ex. 1002, ¶49; Ex. 1006 at 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil."); *id.* at 554-555; Ex. 1009 at ¶[0212] (disclosing that a coil constructed with two or more layers can achieve a higher magnetic flux density than a single layer coil), FIG. 18.)

Accordingly, Lee discloses "when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor." (Ex. 1002, ¶50.)

f) wherein when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated.

To begin, as admitted by the '960 patent, the claimed limitation is an inherent property of an inductor. (Ex. 1002, ¶51.) For example, the '960 patent admits that

> In an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current. **A change in electrical current elicits a corresponding magnetic flux proportional to the amount of current, which in turn, generates an electromotive force**

> **(EMF), measured in volts, that opposes the change in current. Inductance is a measure of the amount of EMF generated per unit change in current.**

(Ex. 1001, 1:54-64 (emphases added).)

> An inductor is generally an electrical component or circuit that **introduces inductance into a circuit**. . . . **Inductance is generally a property of an electric circuit** by which an electromotive force is induced as the result of a changing magnetic flux.

(*Id.*, 14:17-27 (emphases added); Ex. 1002, ¶51.) As admitted in the '960 patent, inductance is a property of an inductor, as might be formed by one or more turns of an electrical conductor. (Ex. 1001, 1:54-64; Ex. 1002, ¶52.) Therefore, when there is a change in the frequency, magnitude, or waveform shape of a current flowing through an inductor, a changing magnetic flux is created. (Ex. 1002, ¶52.) This in turn generates an electromagnetic force or voltage across the inductor through self-inductance. (*Id.*) Thus, when a change in frequency, magnitude, or waveform shape of the propagated electrical current occurs, an inductance, including at least a self-inductance, is necessarily generated. (*Id.*) Accordingly, Lee necessarily discloses this feature because Lee discloses an inductor in figures 4A-4C. (*Id.*)

Lee discloses this limitation for additional reasons. (Ex. 1002, ¶53.) **First**, Lee discloses generating an "inductance" when a current passes through an inductor. (Ex. 1005, ¶[0034] (disclosing that "the external or internal circuits provide a current passing through" the inductor "and utilize the **inductance induced by the inductor**") (emphasis added).) "Inductance" is defined by the IEEE Standard Dictionary of Electrical and Electronics Terms as "the property of an electric circuit by virtue of which a **varying current** induces an electromotive force in that circuit or in a neighboring circuit." (Ex. 1010 at 517 (emphasis added); Ex. 1002, ¶53.) Thus, given that Lee discloses the inductor induces "inductance" when an electric current passes through it, a POSITA would have understood that the current necessarily has "a change in at least one of a frequency, a magnitude, or a waveform shape" because such a change in necessary to induce an inductance. (Ex. 1002, ¶53.)

This understanding is consistent with Lee's disclosure that its inductors are "[c]onventionally . . . employed **in integrated circuits designed for radio frequency (RF) band**." (Ex. 1005, ¶[0005] (emphasis added); Ex. 1002, ¶54.) A POSITA would have understood that an RF circuit is an electrical circuit includes a current that **oscillates** at a frequency other than zero and is associated with circuits that can operate at very high frequencies (for example, frequencies as high as 100 GHz. (Ex. 1010 at 860 ("The present practicable limits of radio frequency are

roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz)"); Ex. 1020, 1 (disclosing a 60 GHz RF signal).) Therefore, the current in an RF circuit necessarily **changes in magnitude** because it is oscillating. (Ex. 1002, ¶54.)

Second, a POSITA would have understood that any change in current passing through Lee's inductor, including turning the circuit on for the first time, would necessarily create a transient event or transient period. (*Id.*, ¶55.) For instance, a current passing through Lee's circuit in response to the abrupt application of a DC voltage would necessarily take a finite amount of time, known as the transient period, to reach a steady-state value. (Ex. 1006 at 604; *see also id.* at 603, 605; Ex. 1002, ¶55.) During this transient interval, at least the magnitude of current passing through the inductor would change (from zero to a value determined primarily by the series resistance in the circuit), and an electromotive force (EMF, measured in Volts) would therefore be induced in the inductor. (Ex. 1006 at 604 (explaining that, at the beginning of the transient interval, "the rate of change of current is very large, and the [EMF] induced in the inductor limits the flow of current," and that "[w]hen the current reaches a steady value and is no longer changing, there is no induced [EMF]…."); Ex. 1002, ¶55.) An inductance (measured in Henrys) is a measure of EMF generated in response to a change in current (measured in Amperes) per unit time. (*Id.*; *see also* Ex. 1006 at 601 ("a coil has an inductance of 1 [H]enry if an [EMF] of 1 volt is induced in the coil

when the current through it is changing at the rate of 1 amp/sec."); Ex. 1010 at 517.) As such, an "inductance," including at least a self-inductance, is necessarily generated when current passes through Lee's inductor—at least during the transient period. (Ex. 1002, ¶55.) Accordingly, Lee discloses "when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated." (*Id.*)

2. Claim 2

a) The inductor of claim 1 wherein an electromotive force is generated when at least one of the frequency, the magnitude, or the waveform shape of the propagated electrical current is changed.

Lee discloses this limitation because the claimed feature is merely an inherent property of an inductor, where **any** change in the current flowing through the inductor results in the generation of an EMF (electromotive force) across the inductor that opposes this change in current. (Ex. 1002, ¶56; Ex. 1001, 1:54-64, 14:17-27.) Therefore, because Lee discloses an inductor, an electromotive force will necessarily be generated when there is change in "at least one of the frequency, the magnitude, or the waveform shape" of electrical current flowing through the inductor (and therefore, through the "first conductor layer"). (Ex. 1002, ¶56.)

Moreover, as discussed above in Section IX.A.1(f), Lee discloses passing a current through its inductor to generate an inductance. (*See supra* Section

IX.A.1(f); Ex. 1005, ¶[0034] ("the external or internal circuits provide a current passing through" the inductor "and utilize the **inductance induced by the inductor**") (emphasis added).) Given that inductance is a measure of EMF generated in response to a change in current per unit time, (*see* Ex. 1006 at 601; Ex. 1010 at 517), an "electromotive force" is necessarily generated in Lee's inductor when there is a change in current through the inductor ("when at least one of the frequency, the magnitude, or the waveform shape of the propagated electrical current is changed"), as would occur with excitation of Lee's inductor by RF currents. (Ex. 1002, ¶57.)

Furthermore, as discussed in Section IX.A.1(f), the current through Lee's inductor necessarily changes (e.g., from zero to a finite, steady-state value) in response to an abruptly applied DC voltage, and such a change in current would necessarily generate an EMF in the inductor. (Ex. 1002, ¶58.)

3. Claim 3

a) The inductor of claim 2 wherein a magnitude of the magnetic flux is proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current.

Lee discloses this limitation. (Ex. 1002, ¶¶59-61.) As admitted by the '960 patent, the claimed limitation is an inherent property of an inductor. (*Id.*, ¶59.) For example, the '960 patent admits that "[i]n an inductor, electric current travels

through the metallic coil **generating a magnetic flux that is proportional to the amount of electric current**" and that "**[a] change in electrical current elicits a corresponding magnetic flux proportional to the amount of current**." (Ex. 1001, 1:54-60 (emphases added); Ex. 1002, ¶59.) Therefore, Lee necessarily discloses claim 3 because figures 4A-4C of Lee disclose an inductor. (Ex. 1002, ¶59.)

Furthermore, because Lee at least discloses a change in the magnitude of the current in its inductor (e.g., in response to current oscillating at an RF frequency and during the transient period following application of DC voltage) as discussed above in Section IX.A.1(f), Lee necessarily discloses "a magnitude of the magnetic flux is proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current." (*See supra* Section IX.A.1(f); Ex. 1002, ¶60.)

Furthermore, as discussed above in Section IX.A.1(e), a magnetic flux is a measure of magnetic field that passes through a specific area (Ex. 1002, ¶61; Ex. 1006 at 554-555.) Accordingly, a POSITA would have recognized that Lee discloses "a magnitude of the magnetic flux is proportional to the amount of change of…the magnitude…of the electrical current," given that the magnetic field that passes through a specific area is also proportional to the change in electrical current through the inductor. (Ex. 1002, ¶61; *see also* Ex. 1006 at 592-593, 601

("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil.").)

4. Claim 4

a) The inductor of claim 1 wherein, an electrical resistance of at least one of the first conductor layer is reducable when a cross-sectional area of a conducting skin depth within at least the first conductor layer is increased.

Lee discloses this limitation. (Ex. 1002, ¶¶62-64.) A POSITA would have understood that the claimed "conducting skin depth," as admitted by the '960 patent, is an inherent material property, which defines an outer portion of a conductor extending to a certain depth below a conductor's surface where most of the current flows. (Ex. 1002, ¶62; Ex. 1001, 2:36-54, 2:61-63, 17:28-46.) As explained below, a POSITA would have understood that as the conducting skin depth of a conductor (e.g., conductive trace 311 embedded in dielectric layer 310, i.e., "first conductor layer") increases, cross-sectional area of the conducting skin depth of a conductor also necessarily increases, leading to a reduction of electrical resistance of the conductor. (Ex. 1002, ¶63.) As such, Lee discloses "an electrical resistance of at least one of the first conductor layer is reducable when a cross-sectional area of a conducting skin depth within at least the first conductor layer is increased." (*Id.*)

A POSITA would have understood that the skin depth of a given conductor decreases as the frequency of the current passing through it is increased, and increases as the frequency is decreased. (*Id.*, ¶64; *see also id.* at ¶¶26-29.) Indeed, as was well known in the art, when a high frequency current flows through a conductor, the current flow is negligible at the interior core of the conductor. (*Id.*, ¶27.) Rather, the current is substantially confined to a cross-sectional area that is defined by the skin depth at a given frequency near the surface of the conductor, thereby reducing the effective conductivity (or increasing the effective resistance) of the conductor. (*Id.*; Ex. 1015 at 16 ("the skin effect influences the effective area of the cross section" of a conductor); Ex. 1016 at 1:11-21.)

Conversely, as the frequency is reduced, the skin depth increases. (Ex. 1002, ¶28.) The increased skin depth also increases the cross-sectional area available for current flow, thereby increasing the effective conductivity (or reducing the effective resistance) of the conductor. (*Id.*) This phenomenon was widely known and well-understood in the art at the time of the claimed invention. (*Id.*)

The skin depth effect occurs in any conductive medium, including Lee's looped conductive trace 311 ("first conductor layer"), which can be made of copper, aluminum, or a combination thereof. (Ex. 1005, ¶[0026]; Ex. 1016 at 1:11-18; Ex. 1017 at 7:5-10, 8:12-28; Ex. 1002, ¶64.) Accordingly, a POSITA would

have understood that when the frequency of the current passing through Lee's inductor is increased, the electrical resistance of the looped conductive trace 311 ("first conductor layer") in Lee's inductor increases as the cross-sectional area of a conducting skin depth of the inductor decreases. (Ex. 1002, ¶64.) Similarly, a POSITA would have also understood that when the frequency of the current decreases, the electrical resistance of the looped conductive trace 311 in Lee's inductor ("first conductor layer") decreases as the cross-sectional area of a conducting skin depth of the inductor increases. (*Id.*) Accordingly, Lee discloses "an electrical resistance of at least one of the first conductor layer is reducable when a cross-sectional area of a conducting skin depth within at least the first conductor layer is increased." (*Id.*)

5. Claim 5

a) The inductor of claim 1 wherein a thickness of at least the first conductor layer is about equal to or greater than a thickness of a skin depth of the first conductor layer at a given frequency.

Lee discloses this limitation. (Ex. 1002, ¶¶65-67.) Lee discloses that "[f]or example, . . . the looped conductive layer 311 has a thickness of about 0.53 μm. (Ex. 1005, ¶[0027].) Lee also discloses that the conductive layer 311 is formed of copper. (*Id.,* ¶[0026].) Lee further discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (*Id.,* ¶[0005].) The RF band includes several frequencies, including high

frequencies such as 30 GHz and 100 GHz. (Ex. 1002, ¶67; Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz).").) Therefore, at certain operating frequencies in the RF band, Lee's conductive layer 311 ("first conductor layer") has a "thickness . . . about equal to or greater than a thickness of" its skin depth at that frequency. (*Id.*) For example, at 30 GHz, which is a frequency within the RF band, the skin depth of copper (with a resistivity of 1.678 10^{-8} ohm-metres and relative permeability of 1) is 0.3764 μm. (*Id.* (citing https://chemandy.com/calculators/skin-effect-calculator.htm).) Similarly, at 100 GHz, the skin depth of copper is 0.2062 μm, which is less than half the thickness of Lee's conductive layer 311. (*Id.*) At such frequencies, the thickness of looped conductive layer 311 (i.e., 0.53 μm) is more than the skin depth (i.e., 0.3764 μm at 30 GHz or 0.2062 μm at 100 GHz) of conductive layer 311. (*Id.*; (Ex. 1002, ¶67.)

6. Claim 6

a) The inductor of claim 1 wherein a thickness of the first conductor layer ranges from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency.

As discussed above for claim 5, the thickness of the looped conductive layer 311 is 0.53 μm and the skin depth is 0.3764 μm at 30 GHz. (*See supra* Section IX.A.5.) Therefore, Lee discloses claim 6 because 0.53 μm is about 1.4 times 0.3764 μm. (Ex. 1002, ¶68.) Similarly, as described above in Section 5, the skin

depth is 0.2062 μm at 100 GHz, which is about 2.6 times the conductor layer thickness of 0.53 μm, also disclosing the limitations of claim 6. (*See supra* Section IX.A.5.)

7. Claim 7

a) The inductor of claim 1 wherein a thickness of the second conductor layer ranges from about 1.25 times to about 4 times a thickness of a skin depth of the second conductor layer at a given frequency.

Lee discloses this feature for the same reasons as it discloses claim 6. (Ex. 1002, ¶69.) Specifically, the "second conductor layer" in Lee is one of the three conductive traces 311. (*See supra* Section IX.A.1(b).) Therefore, the analysis for claim 6 applies to the "second conductor layer" as well.

8. Claim 8

a) The inductor of claim 1 wherein a first conductor layer thickness is about the same as a second conductor layer thickness.

Lee discloses this limitation. (Ex. 1002, ¶70.) For example, as discussed above in Sections IX.A.1(a) and (b), looped conductive traces 311 discloses the "first conductor layer" and the "second conductor layer." (*See supra* Sections IX.A.1(a) and (b).) Furthermore, because Lee discloses that "the looped conductive trace 321 may have the same thickness as the looped conductive traces 311" (Ex. 1005, ¶[0032]), Lee discloses that each of the looped conductive traces 311 have the same thickness. (Ex. 1002, ¶70.)

9. Claim 10

a) The inductor of claim 1 wherein a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer.

Lee discloses this limitation. (Ex. 1002, ¶71.) As discussed above in Section IX.A.4(a), a skin depth for a conductor, e.g, Lee's inductor, is determined based on the frequency of the current propagating through the conductor, and intrinsic properties of the conductor, including conductivity and permeability. (*See supra* Section IX.A.4(a).) At least because Lee discloses that traces 311 ("the first conductor layer" and "the second conductor layer") "may be copper, aluminum or a combination thereof," Lee discloses that an embodiment that these traces are made of the same material and, in that embodiment, the traces necessarily share the same conductivity and permeability. (Ex. 1005, [0026]; Ex. 1002, ¶71.) Lee also discloses that the first and second conductor layers share the same thickness and geometry. (Ex. 1005, ¶[0032]; Ex. 1002, ¶71.) Furthermore, because traces 311 belong to the same inductor, they are subject to the same excitation current and therefore the same excitation frequency. (Ex. 1002, ¶71.) Accordingly, each of traces 311 has about the same skin depth because they have the same current, frequency, conductivity, permeability, and geometry. (*Id.*) Thus, Lee discloses "a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer." (*Id.*)

10. Claim 15

a) The inductor of claim 1 wherein the frequency is at least 3 kHz.

Lee discloses this limitation. (Ex. 1002, ¶72.) Lee discloses that inductors are "[c]onventionally…employed **in integrated circuits designed for radio frequency (RF) band**." (Ex. 1005, ¶[0005] (emphasis added); Ex. 1002, ¶72.) As discussed above, RF band includes frequencies such as 30 GHz and 100 GHz (*supra* Section IX.A.1(f)), and thus Lee's inductor would be operated at RF frequencies (including 30 GHz and 100 GHz). (Ex. 1002, ¶72.)

11. Claim 16

a) The inductor of claim 1 wherein at least one of the first and second conductor layers is formed from a thermally conductive material.

Lee discloses this limitation. (Ex. 1002, ¶73.) Lee discloses that the looped conductive traces 311 ("the first and second conductor layers") may be copper, which a POSITA would have understood as thermally conductive. (*Id.,* ¶73; Ex. 1005, ¶[0026]; Ex. 1011 at ¶[0039] (describing copper as "thermally conductive material"); Ex. 1013 at 4:37-39 (disclosing copper has "having a high thermal conductivity").)

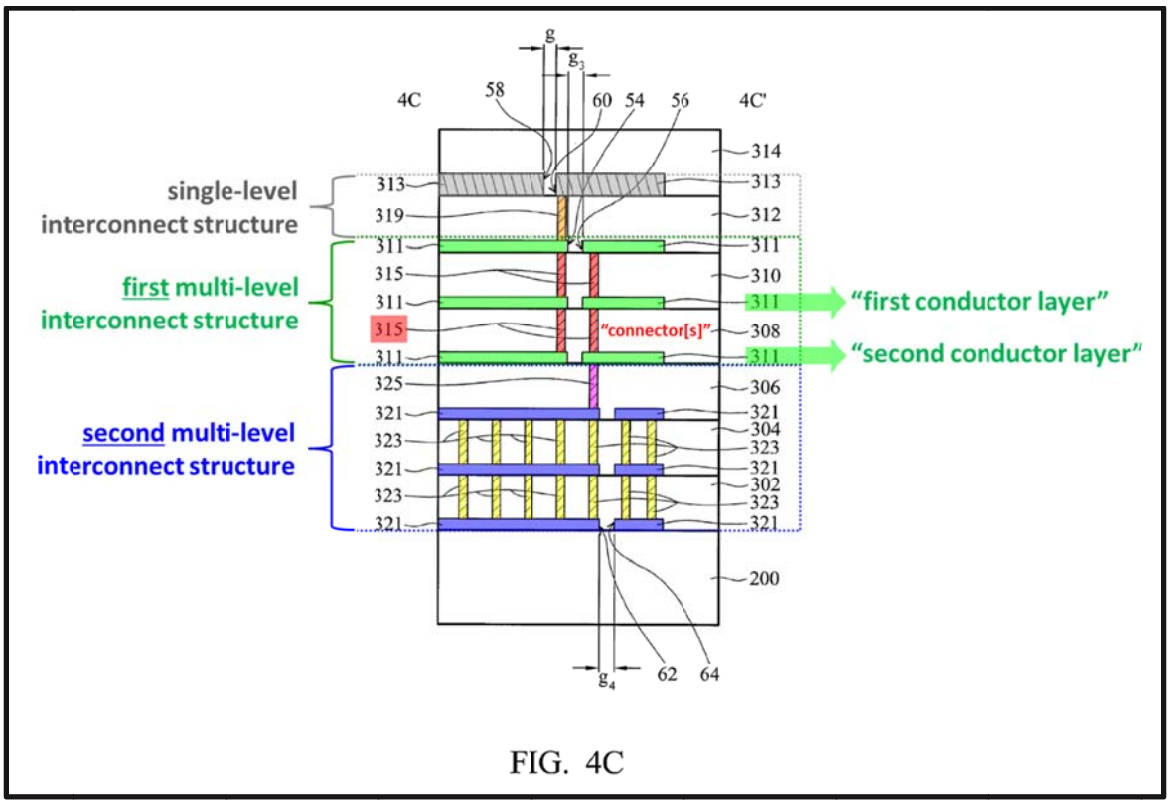
12. Claim 17

a) The inductor of claim 1 wherein the connector is selected from the group consisting of a via, a solder, a tab, a wire, a pin, a rivet, a filled mesh structure, a conductive polymer, a conductive composite, a

conductive adhesive, a liquid metal, a foamed metal, and combinations thereof.

Lee discloses this limitation in at least two ways. (Ex. 1002, ¶¶74-76.)

First, Lee discloses the claimed "connector" being conductive plugs 315, which may be "copper, aluminum or a **combination thereof**." (Ex. 1005, ¶[0026] (emphasis added).) Accordingly, any of conductive plugs 315 in Lee ("connector") disclose the claimed "conductive composite." (Ex. 1002, ¶74.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶74; *supra* Section IX.A.1(d).)

Second, a POSITA would have understood that conductive plugs 315, connecting the looped conductive traces 311 ("the first and second conductor layers"), disclose the claimed "via[s]." (Ex. 1014 at 2:2-4 (describing that a "**via**

plug…is comprised of a conductive material and is disposed within a **via hole**…"), 2:18-20 ("**a copper plug within a via hole** may contact the insulating layer surrounding the via hole.") (emphases added); Ex. 1002, ¶75.)

A "via" is well-known in the electrical engineering field as an electrical connection between adjacent layers of, for example, a multi-layer printed circuit board, or PCB. (Ex. 1002, ¶76.) Indeed, the '960 patent admits that a via is "an electrically conductive connection from one layer to another." (Ex. 1001, 15:1-3; 16:13-20.) Just as the vias 144 of figure 4F in the '960 patent provide an electrical connection between conductive layers 138 and 140, the conductive plugs 315 as disclosed by Lee electrically connect the conductive traces 311 ("first conductor layer" and "second conductor layer"). (Ex. 1005, ¶[0026]; Ex. 1002, ¶76.) Accordingly, any of conductive plugs 315 in Lee ("connector") discloses the claimed "via." (Ex. 1002, ¶76.)

13. Claim 18

a) The inductor of claim 1 wherein at least one connector electrically connects the first conductor layer and the second conductor layer in parallel.

Lee discloses this limitation. (Ex. 1002, ¶77.) For example, Lee discloses at least two conductive plugs 315 ("at least one connector") electrically connect ends of conductive traces 311 (the first conductor layer and the second conductor layer) such that "one of the conductive traces 311 is coupled with other conductive traces

311 **in parallel**." (Ex. 1005, ¶[0026] (emphasis added), ¶[0010] ("The first conductive plug is disposed between the looped conductive traces to **electrically connect** the looped conductive traces, in which at least two first conductive plugs are disposed between the neighboring looped conductive traces.") (emphasis added); *see also id.* at claim 1 (disclosing conductive plugs "electrically connecting" looped conductive traces), claim 11 ("first looped conductive traces coupled in parallel"), claim 15 ("at least one pair of first conductive plugs connecting the first looped conductive traces in parallel"), claim 17; Ex. 1002, ¶77.)

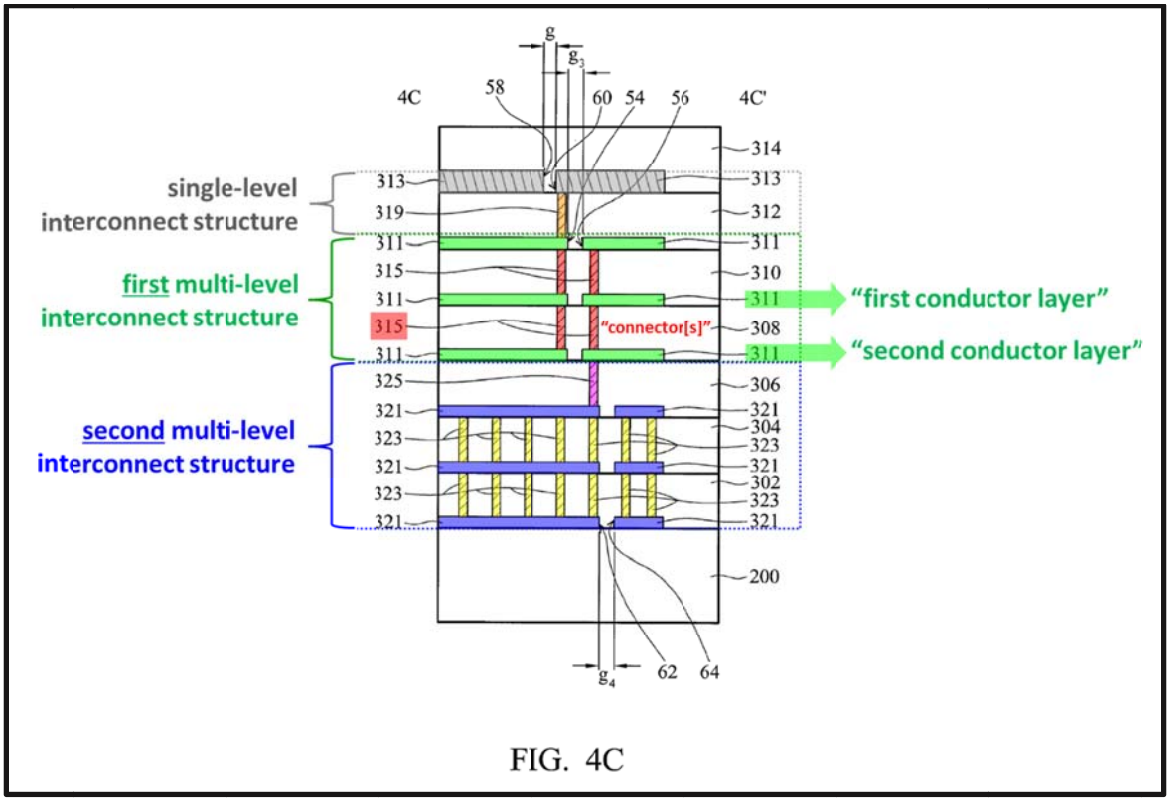


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶77.)

14. Claim 19

a) The inductor of claim 1 wherein the first conductor layer and the second conductor layer form a structure in which the first and second conductor layers are positioned in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other.

Lee discloses this limitation. (Ex. 1002 ¶¶78-79.) For example, Lee discloses that looped conductive traces 311 ("the first and second conductor layers") "overlap and are separated from each other." (Ex. 1005, ¶[0025]; *see also id.* at FIG. 4C.) Thus, a POSITA would have understood that traces 311 are positioned "in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other" because they are in different planes. (Ex. 1002, ¶79.)

15. Claim 20

a) The inductor of claim 1 comprising a third conductor layer and a fourth conductor layer electrically connected in parallel or series and wherein the first and second conductive layers are connected electrically in series or parallel with the third and fourth conductor layers.

Lee discloses this limitation. (Ex. 1002, ¶¶80-85.)

First, Lee discloses "a third conductor layer and a fourth conductor layer electrically connected in parallel or series." (*Id.,* ¶81.) For example, as shown in the annotated figure 4C below, Lee's second multi-level interconnect structure

includes a looped conductive trace 321 ("third conductor layer") embedded in a dielectric layer 306 and another looped conductive trace 321 ("fourth conductor layer") embedded in dielectric layer 304. (Ex. 1005, ¶[0032]; *see also id.* at ¶[0031].)

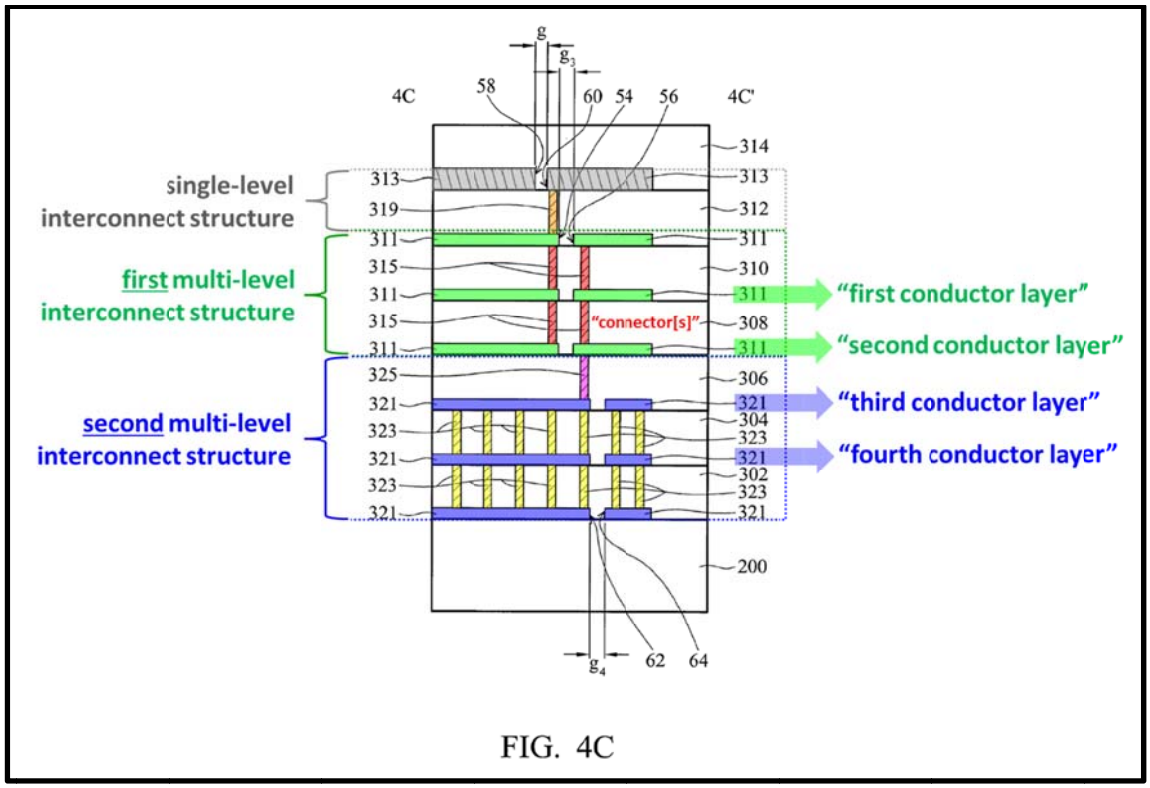


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶81.)

Furthermore, Lee discloses that looped conductive traces 321 ("third conductor layer" and "fourth conductor layer") are electrically connected in parallel by conductive plugs 323. (Ex. 1005, ¶[0035] ("since the **lower conductive trace** includes multilayer winding structure in which each conductive trace is connected **in parallel**, the series resistance can be reduced to maintain the Q value

of the inductor.") (emphasis added); ¶[0034] (disclosing that "the multi-level interconnect structure formed by **the looped conductive traces 321 serves as another lower conductive trace of the inductor**") (emphasis added); *see also id.* at ¶[0033] ("The conductive plugs 323 are disposed between the looped conductive traces 321 to serve as an electrical connection therebetween…thereby reducing the resistance of the multi-level interconnect structure to further reduce the series resistance."), *id*. at claim 20 ("the third looped conductive traces are coupled in parallel"); Ex. 1002, ¶82.)

Indeed, a POSITA would have also understood that looped conductive traces 321 are electrically connected in parallel based on figure 4C. (Ex. 1002, ¶83.) For example, as shown in the annotated figure 4C above, conductive plugs 323 connect the **same ends** of traces 321 ("third conductor layer" and "fourth conductor layer"), rather than **different ends** of the traces. (*Id.*) As such, a POSITA would have also understood that traces 321 ("third conductor layer" and "fourth conductor layer") are connected in parallel. (*Id.*)

Second, Lee discloses "the first and second conductive layers are connected electrically in series or parallel with the third and fourth conductor layers." (*Id.,* ¶84.) For example, Lee discloses with reference to figure 4C that traces 311 (first and second conductive layers) and traces 321 ("third and fourth conductor layers") are electrically connected in series by conductive plug 325. (Ex. 1005, ¶[0033];

see also id. at claim 20 ("the third looped conductive traces, the first looped conductive traces and the second conductive trace are connected **in series**.") (emphasis added).)

Indeed, a POSITA would have also understood that looped conductive traces 311 ("first and second conductive layers") and 321 (the third and fourth conductor layers) are electrically connected in series based on figure 4C. (Ex. 1002, ¶85.) For example, as shown in the annotated figure 4C above, conductive plug 325 connects different ends of traces 311 and 321 ("second conductor layer" and "third conductor layer"), rather than the same ends of the traces. (*Id.*; *see also* Ex. 1005, ¶[0033].) As such, a POSITA would have also understood that traces 311 and 321 ("the first and second conductive layers" and "the third and fourth conductor layers") are connected in series. (*Id.*, ¶85.)

16. Claim 21

a) The inductor of claim 1 wherein the inductor is electrically connectable with an electrical circuit operating at about 100 kHz or greater.

Lee discloses this limitation. (Ex. 1002, ¶86.) Because the claim says that an electrical circuit is "electrically connectable" and not "electrically connected" to the inductor, the claim only requires that the inductor be capable of having an electrical connection with an electrical circuit operating at about 100 kHz or greater. (*Id.*) Lee discloses that "[c]onventionally, the on-chip inductor is . . .

employed in integrated circuits designed for radio frequency (RF) band." (*Id.*, ¶[0005].) The RF band includes frequencies above 100 kHz. (Ex. 1002, ¶86; *supra* Section IX.A.1(f).) Therefore, Lee's figures 4A-4C inductor is "electrically connectable with an electrical circuit operating at about 100 kHz or greater."

17. Claim 22

a) The inductor of claim 21 wherein the electrical circuit is selected from the group consisting of a mixer circuit, an impedance matching circuit, an upconverting mixer circuit, a downconverting mixer circuit, a modulator, a demodulator, a synthesizing circuit, a PLL synthesizing circuit, an amplifying circuit, an electrical driver circuit, an electrical detecting circuit, an RF log detector, an RF RMS detector, an electrical transceiver, a power controller, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, ¶87.) As discussed above with respect to claim 21, Lee discloses that the on-chip inductor can be employed in RF circuits but does not limit the RF circuits to any particular circuit. (*Supra* Section IX.A.16.) Therefore, Lee's inductor is connectable, for example, to a low noise amplifier ("amplifying circuit"), which is an electrical circuit that is employed in RF circuits. (*See, e.g.,* Ex. 1020, FIG. 1.)

18. Claim 24

a) The inductor of claim 1 wherein a control circuit is electrically connectable to the inductor.

Lee discloses this limitation. (Ex. 1002, ¶88.) Because the claim says that a control circuit is "electrically connectable" and not "electrically connected" to the inductor, the claim only requires that the inductor be capable of having an electrical connection with a control circuit. (*Id.*) As discussed above with respect to claim 21, Lee discloses that the on-chip inductor can be employed in RF circuits (*supra* Section IX.A.16), which a POSITA would have known includes a control circuit. (Ex. 1002, ¶88.) Therefore, Lee's inductor is electrically connectable to a control circuit (e.g., a control circuit in an RF integrated circuit).

19. Claim 25

a) The inductor of claim 1 wherein at least the first and second conductor layers has at least a partial revolution.

Lee discloses this limitation. (Ex. 1002, ¶¶89-90.) For example, as shown in the annotated figure 4C below, Lee discloses that each of looped conductive traces 311 ("the first and second conductor layers") is separated by a gap g3. (Ex. 1005, ¶¶[0025], [0031], FIGs. 4A, 4C.)

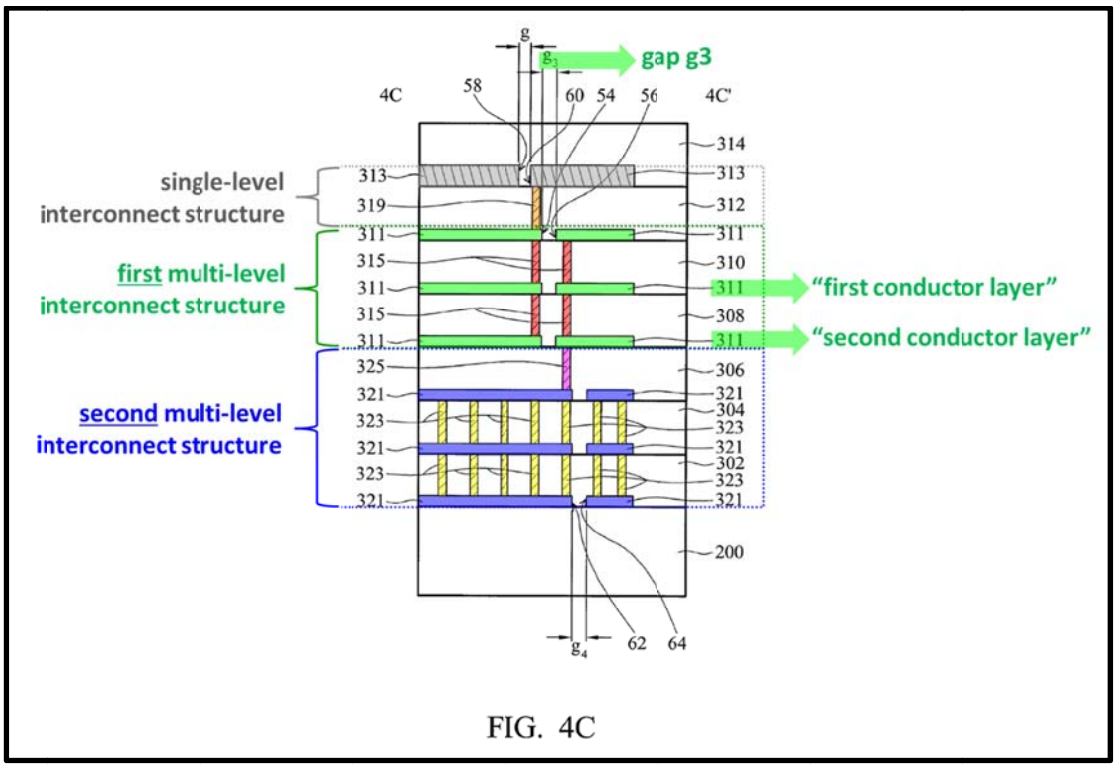


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶89.)

Because Lee discloses that each of conducive traces 311 ("first and second conductor layers") is looped and separated by gap g3, Lee discloses that "at least the first and second conductor layers has at least a partial revolution." (Ex. 1002, ¶90.)

20. Claim 26

a) The inductor of claim 1 wherein the first conductor layer or the second conductor layer comprises a material selected from the group consisting of copper, titanium, platinum, platinum and iridium alloys, tantalum, niobium, zirconium, hafnium, nitinol, cobalt-chromium-nickel alloys, stainless steel, gold, a gold alloy, palladium, carbon, silver, a noble metal, a conductive polymer, a conductive adhesive, a conductive composite, a liquid metal, a foamed metal, a conductive tape, a conductive ribbon, a conductive foil, a conductive leaf, a wire, a deposited metal, a biocompatible material, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, ¶91.) For example, Lee discloses that traces 311 ("first conductor layer" and "second conductor layer") "may be copper, aluminum or a combination thereof." (Ex. 1005, ¶[0026].)

21. Claim 27

a) The inductor of claim 1 wherein at least one insulator layer is formed from an electrically insulative material.

Lee discloses this limitation. (Ex. 1002, ¶92.) For example, Lee discloses that dielectric layer 308 ("insulator layer") may be an "insulating layer" such as "silicon oxide, silicon nitride or low k dielectric material." (Ex. 1005, ¶[0024].) A POSITA would have understood that at least silicon oxide and silicon nitride are "electrically insulative material" because dielectric layer 308 is an insulating layer. (Ex. 1002, ¶92.)

22. Claim 28

a) The inductor of claim 1 wherein the insulator layer comprises an electrically insulative material selected from the group consisting of air, polystyrene, silicon dioxide, a biocompatible ceramic, a conductive dielectric material, a non-conductive dielectric material, a piezoelectric material, a pyroelectric material, a ferrite material, and combinations thereof.

Lee discloses this limitation. (Ex. 1002, ¶93.) For example, Lee discloses that dielectric layer 308 ("insulator layer") may be "silicon oxide, silicon nitride or low k dielectric material." (Ex. 1005, ¶[0024].) Further, each of the insulators Lee discloses at least a "non-conductive dielectric material." (Ex. 1002, ¶93.)

23. Claim 29

Preamble An inductor comprising:

Lee discloses this limitation, for at least the same reasons as presented above for preamble of claim 1. (*Supra* Section IX.A.1(preamble); Ex. 1002, ¶94; *see also infra* Sections IX.A.23(a)-(d) for the remaining elements of this claim.)

a) a first inductor subassembly comprising:

Lee discloses this limitation. (Ex. 1002, ¶95.) For example, as shown in annotated figure 4C below, Lee's first multi-level interconnect structure discloses the claimed "first inductor subassembly." (Ex. 1005, ¶[0025]; *see also* analysis below for claim limitations 29(a)(1)-(4).)

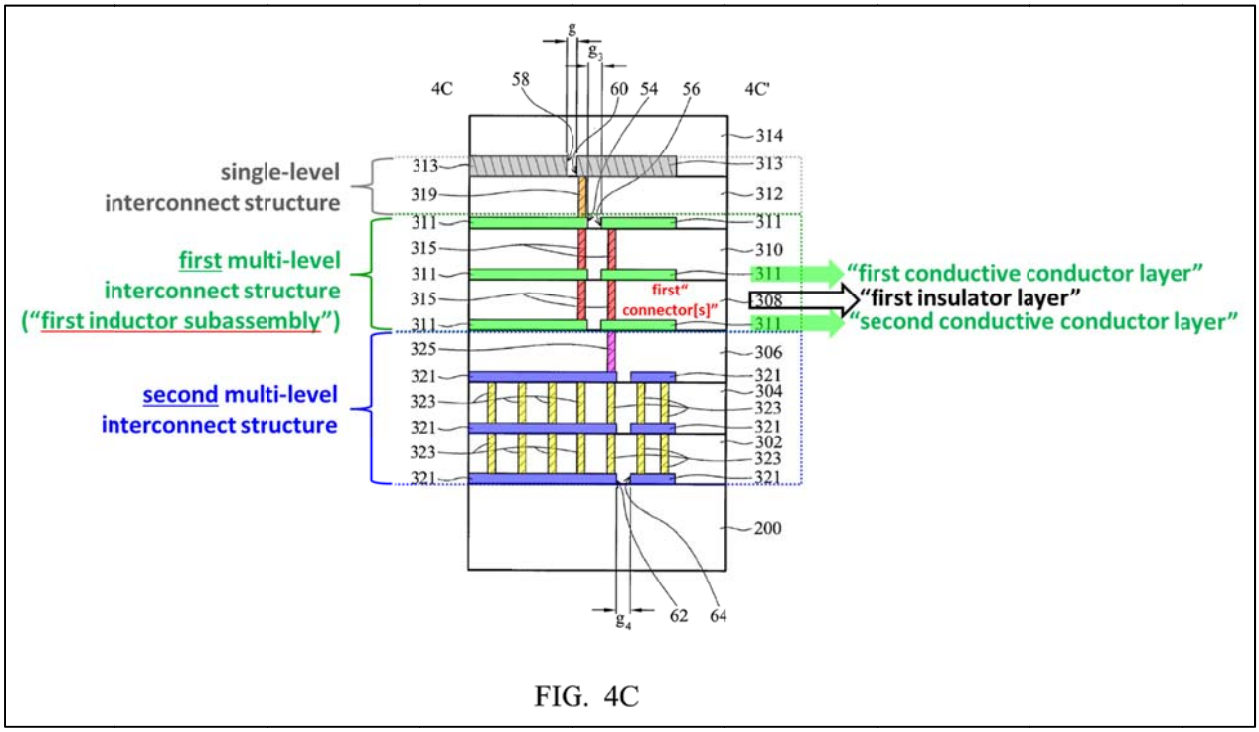


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶95.)

(1) i) a first conductive conductor layer;

Lee discloses this limitation for at least the same reasons as presented above for limitation 1(a). (*Supra* Section IX.A.1(a); Ex. 1002, ¶96.)

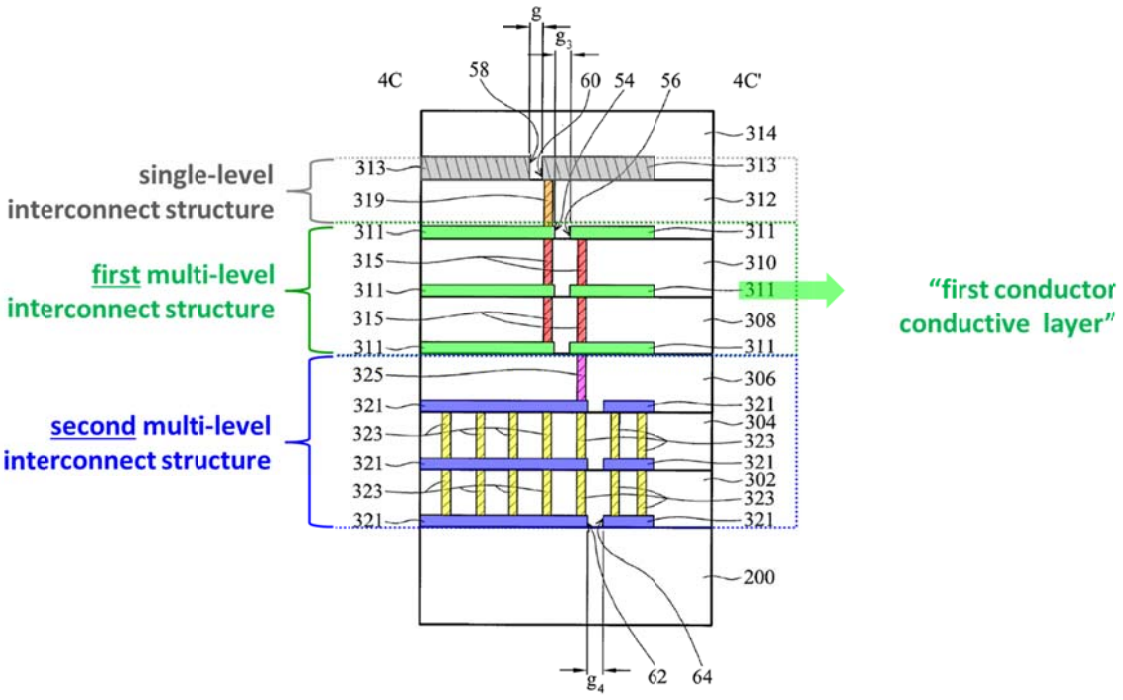


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶96.)

(2) ii) a second conductive conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive;

Lee discloses this limitation for at least the same reasons as presented above for limitation 1(b). (*Supra* Section IX.A.1(b); Ex. 1002, ¶97.)

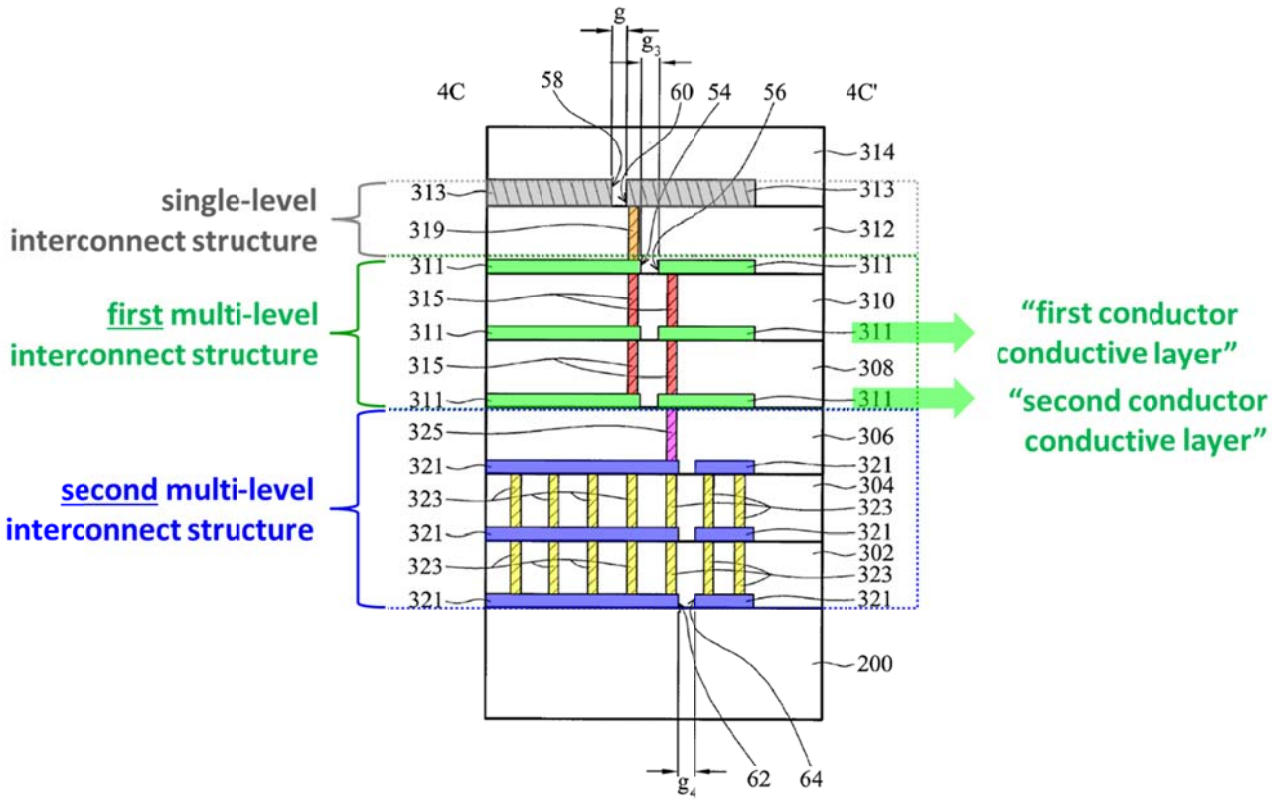


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶97.)

(3) ii) a first insulator layer positioned in the space between the first conductor layer and the second conductor layers, and

Lee discloses this limitation for at least the same reasons as presented above for limitation 1(c). (*Supra* Section IX.A.1(c); Ex. 1002, ¶98.)

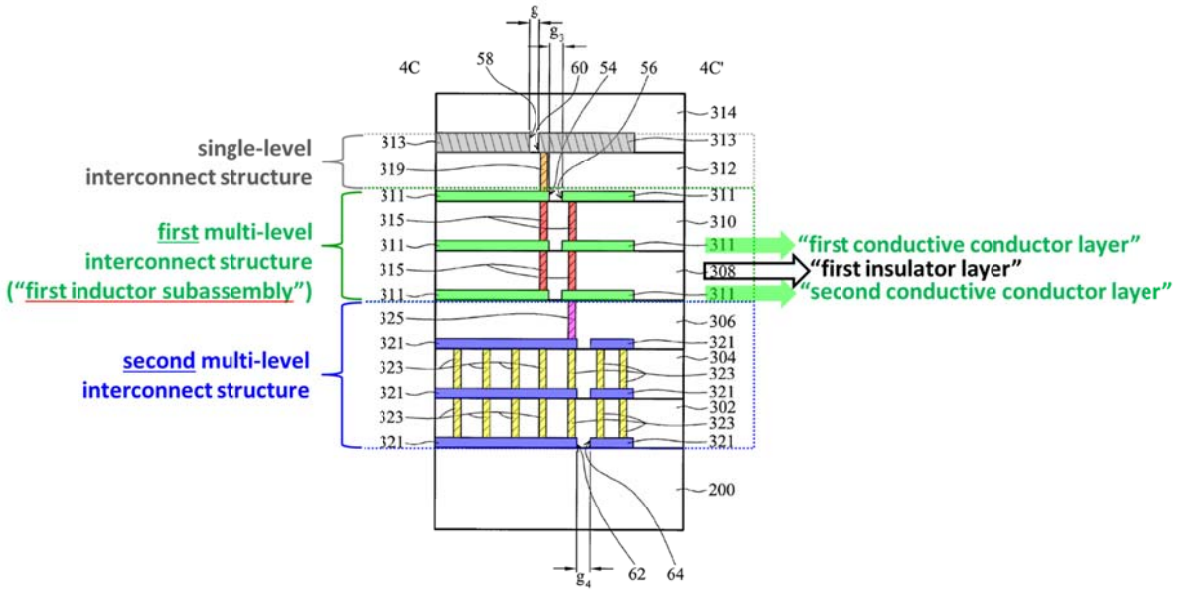


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶98.)

(4) iii) a first connector electrically connecting the first conductor layer and the second conductor layer in parallel;

Lee discloses this limitation for at least the same reasons as presented above for limitations 1(d) and claim 18. (*Supra* Sections IX.A.1(d) and IX.A.13; Ex. 1002, ¶99.)

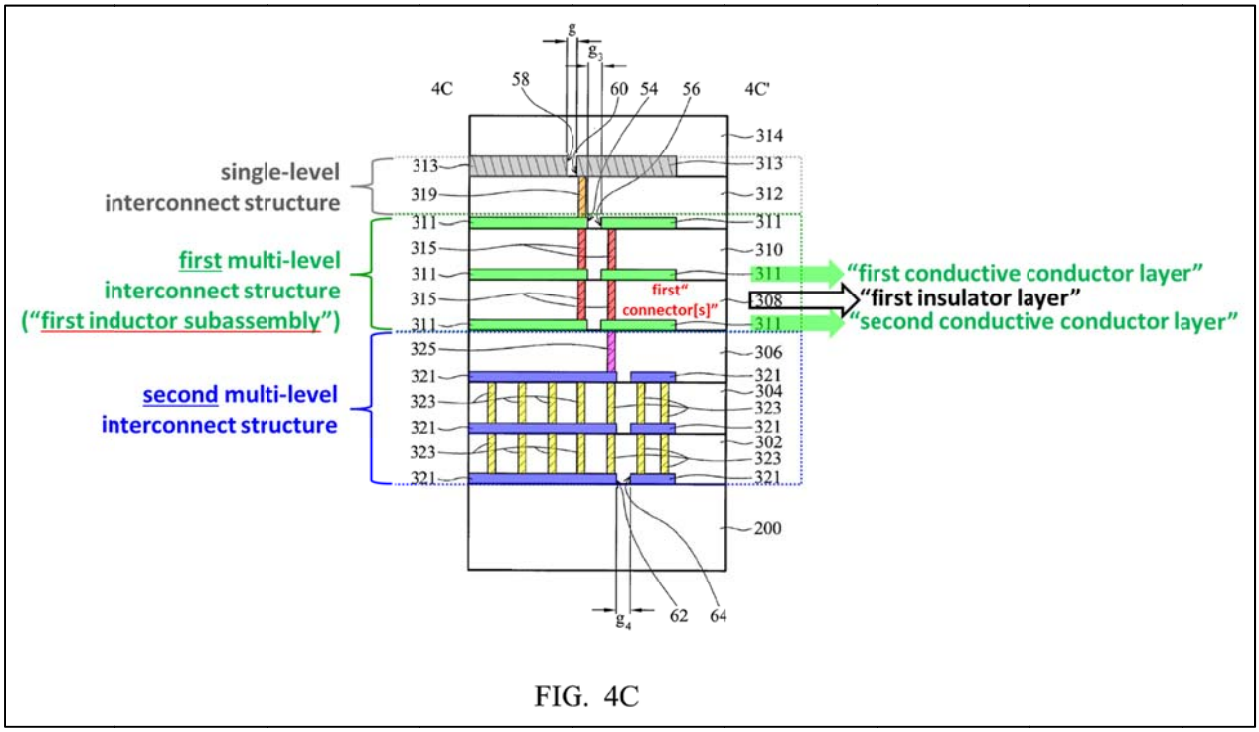


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶99.)

b) a second inductor subassembly comprising:

Lee discloses this limitation. (Ex. 1002, ¶100.) For example, as shown in the annotated figure 4C below, Lee's second multi-level interconnect structure discloses the claimed "second inductor subassembly." (Ex. 1005, ¶[0031]; *see infra* Sections IX.A.23(b)(1)-(4) for the remaining elements of the claimed "second inductor subassembly.")

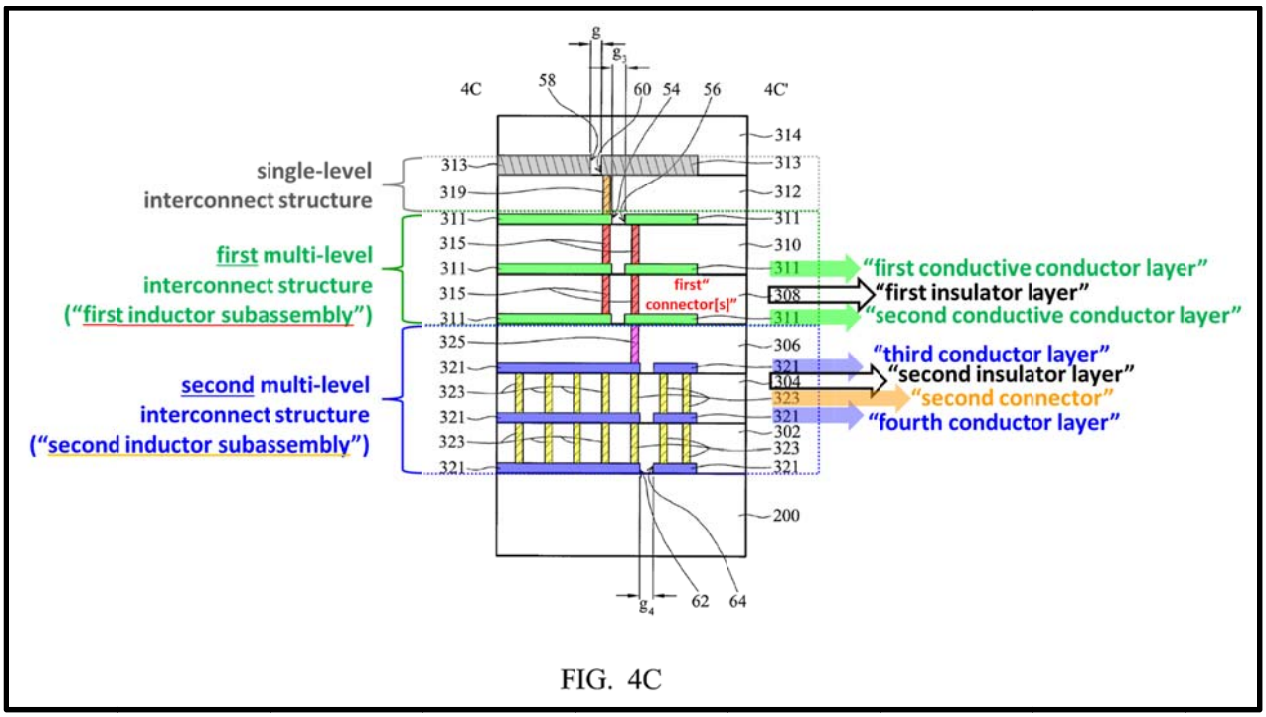


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶100.)

(1) i) a third conductor layer;

Lee discloses this limitation for at least the same reasons as presented above for claim 20. (*Supra* Section IX.A.15(a); Ex. 1002, ¶101.)

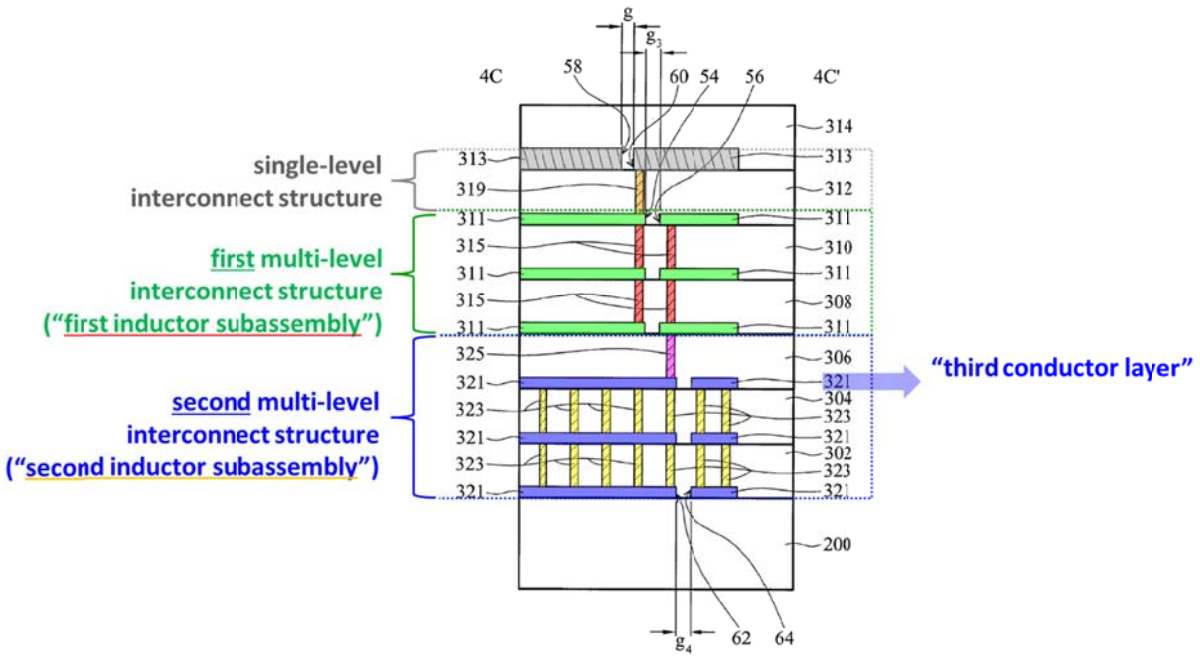


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶101.)

(2) ii) a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive;

Lee discloses this limitation. (Ex. 1002, ¶¶102-104.) For example, as illustrated in annotated figure 4C below, Lee's inductor, in its second multi-level interconnect structure, includes another looped conductive trace 321 ("fourth conductor layer") that is embedded in dielectric layer 304, in addition to looped conductive trace 321 ("third conductor layer") that is embedded in dielectric layer 306. (Ex. 1005, ¶[0032]; *see also id.* at ¶¶[0031], [0033]-[0034]; Ex. 1002, ¶102.)

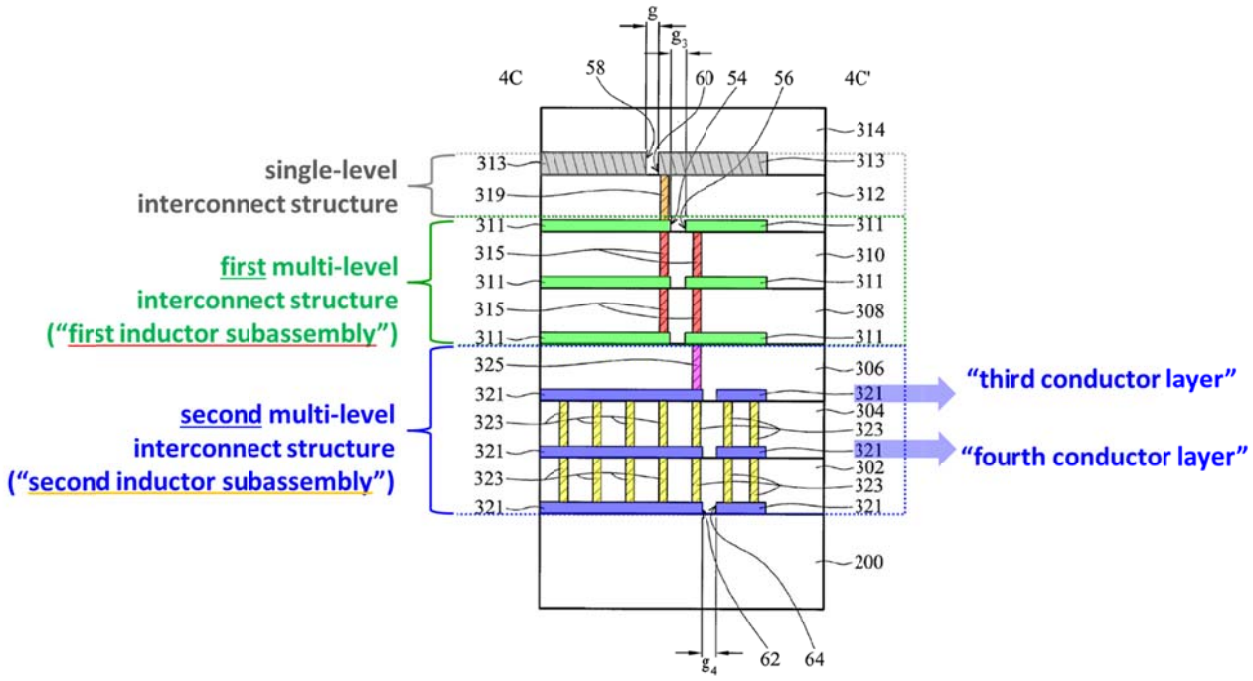


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶102.)

Furthermore, Lee discloses that these conductive traces 321 ("third conductor layer" and "fourth conductor layer") are "separated from each other." (Ex. 1005, ¶[0032]; *see also id.* at Abstract (disclosing "a plurality of looped conductive traces overlapping and separated from each other"), ¶[0010], claim 2.) Thus, Lee discloses "a fourth conductor layer spaced apart from the third conductor layer." (Ex. 1002, ¶103.)

Lee also discloses that these conductive traces 321 ("third conductor layer" and "second conductor layer") are electrically conductive at least because Lee describes these traces 321 as **conductive** and that a **current** may pass through

these conductive traces to induce inductance. (*See*, *e.g.*, Ex. 1005, ¶[0034].) Accordingly, Lee discloses "a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive." (Ex. 1002, ¶104.)

(3) iii) a second insulator layer positioned in the space between the third conductor layer and the fourth conductor layers; and

Lee discloses this limitation. (Ex. 1002, ¶105.) For example, as shown in the annotated figure 4C below, Lee discloses dielectric layer 304 ("second insulator layer") that is positioned in the space between two conductive traces 321 ("the third conductor layer and the fourth conductor layers"). (Ex. 1005, ¶[0032] (disclosing that "the looped conductive layers 321 may be correspondingly disposed in the dielectric layers 302, 304 and 306" and that "[t]he looped conductive traces 321…are separated from each other.").)

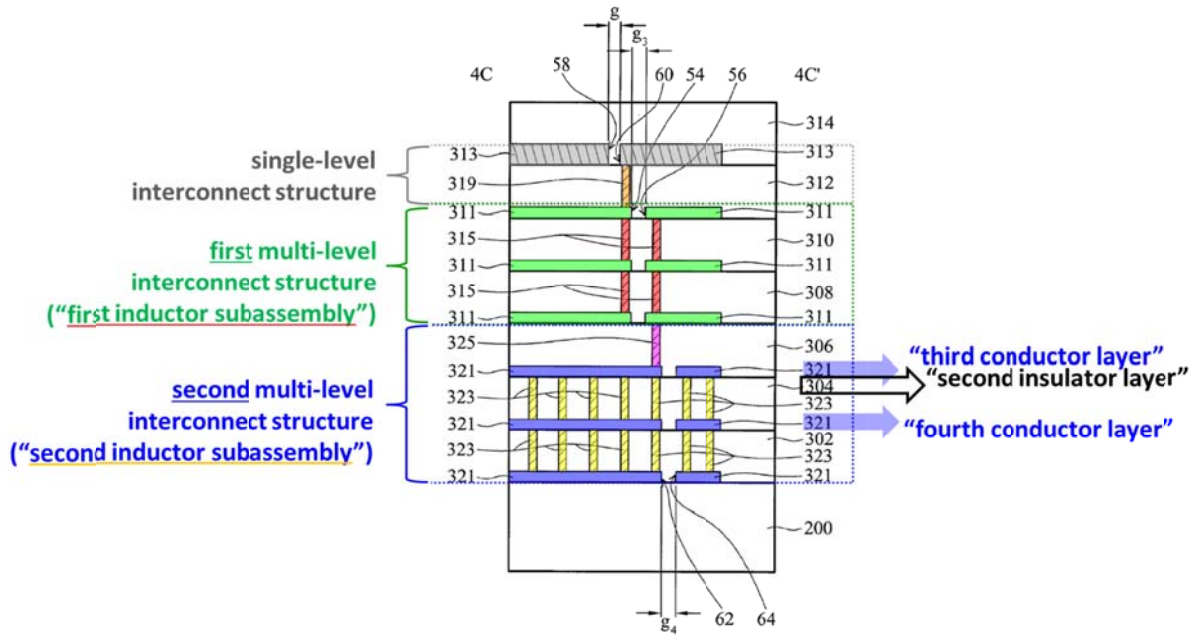


FIG. 4C

(Ex. 1005, FIG. 4C (annotated to show that dielectric layer 304 is positioned in the space between two conductive traces 321); Ex. 1002, ¶105.) Furthermore, Lee discloses that dielectric layer 304 is an "insulator layer," as claimed. (Ex. 1005, ¶[0031] ("the **insulating** layer may be dielectric layers 302, 304, 306, 308, 310, 312 and 314 successively disposed on the substrate 300.") (emphasis added); Ex. 1002, ¶105.)

(4) iv) a second connector electrically connects the third conductor layer and the fourth conductor layer in parallel or series, wherein the first inductor subassembly is electrically connected in series or parallel to the second inductor subassembly; and

Lee discloses this limitation. (Ex. 1002, ¶¶106-109.) For clarity, this limitation is discussed in two parts. (*Id.,* ¶106.)

First, Lee discloses "a second connector electrically connects the third conductor layer and the fourth conductor layer in parallel or series." (*Id.,* ¶107.) For example, as shown in the annotated figure 4C below, Lee discloses that at least two conductive plugs 323 ("second connector") electrically connect two conductive traces 321 ("the third conductor layer and the fourth conductor layer") in parallel. (Ex. 1005, ¶[0035] ("since the lower conductive trace includes multilayer winding structure in which each conductive trace is **connected in parallel**, the series resistance can be reduced to maintain the Q value of the inductor") (emphasis added); ¶[0034] (disclosing that "the multi-level interconnect structure formed by **the looped conductive traces 321 serves as another lower conductive trace of the inductor**") (emphasis added); *see also id.* at ¶[0033] ("The conductive plugs 323 are disposed between the looped conductive traces 321 to serve as an electrical connection therebetween…thereby reducing the resistance of the multi-level interconnect structure to further reduce the series resistance.");

claim 20 ("the third looped conductive traces are coupled **in parallel**") (emphasis added); Ex. 1002, ¶107.)

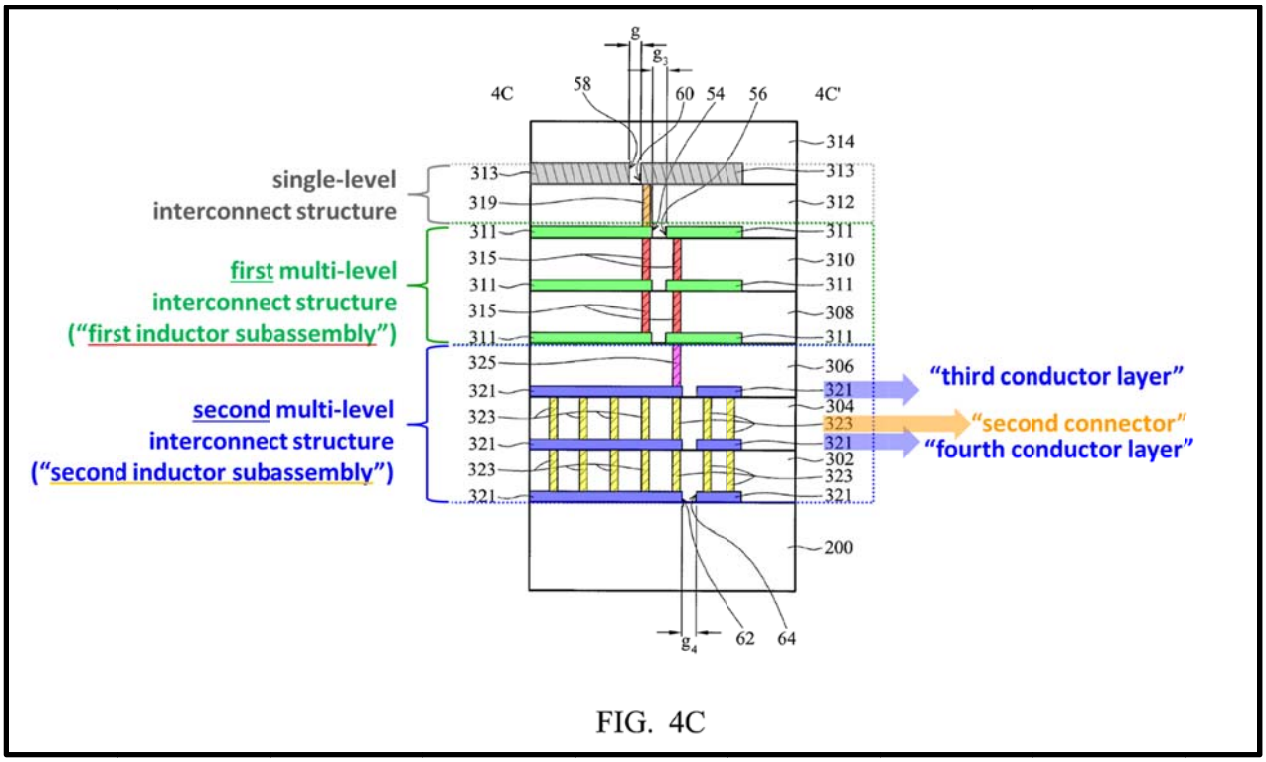


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶107.)

Second, Lee discloses "the first inductor subassembly is electrically connected in series or parallel to the second inductor subassembly." (Ex. 1002, ¶108.) For example, as shown in the annotated figure 4C below, Lee discloses that "the first inductor subassembly" (including traces 311 that are separated by dielectric layer 308, and conductive plugs 315) and "the second inductor subassembly" (including traces 321 that are separated by dielectric layer 304, and conductive plugs 323) are electrically connected in series by conductive plug 325. (Ex. 1005, FIG. 4C, ¶[0033]; *see also id.* at claim 20 ("the third looped conductive

traces, the first looped conductive traces and the second conductive trace are connected **in series**," where the third looped traces correspond to traces 321s in figure 4C, the first looped traces correspond to traces 311s in figure 4C) (emphasis added); Ex. 1002, ¶108.)

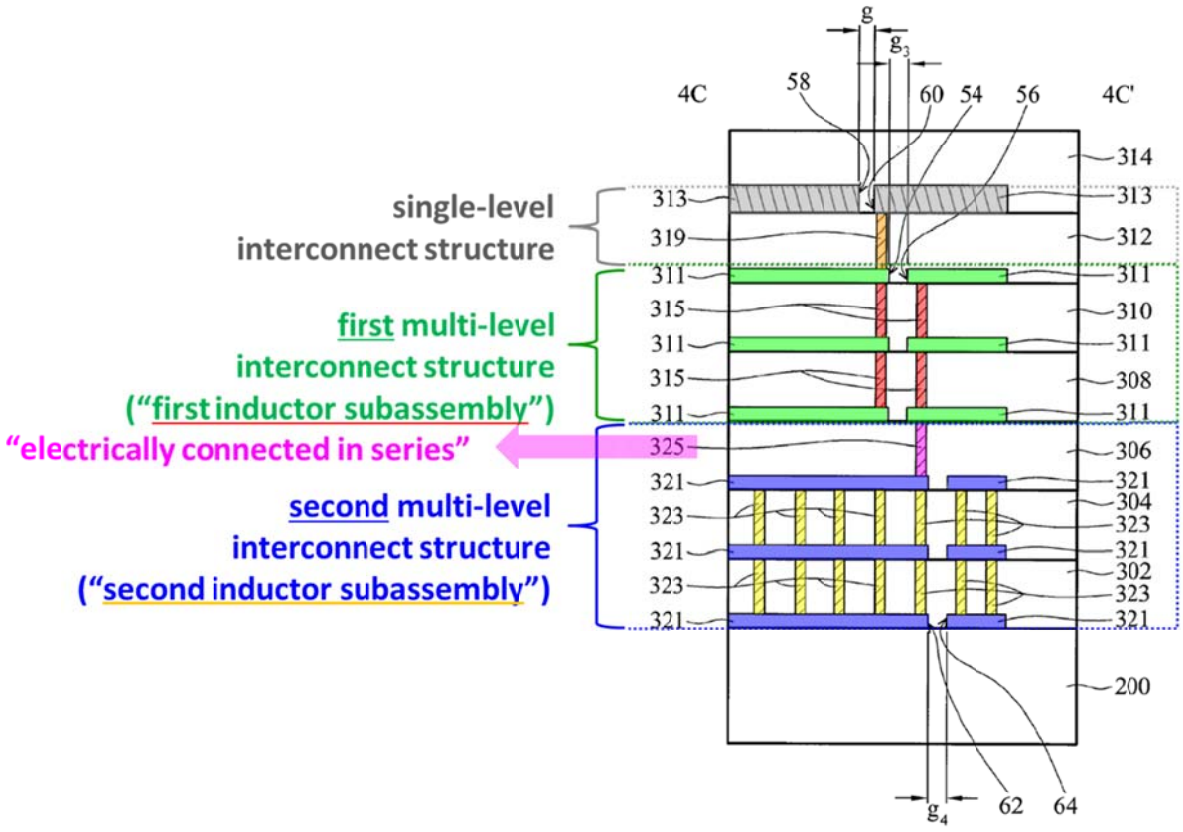


FIG. 4C

(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶108.)

Indeed, a POSITA would have also understood based on figure 4C that the "first inductor subassembly" and "second inductor subassembly" are electrically connected in series. (Ex. 1002, ¶109.) For example, as shown in the annotated

figure 4C above, unlike plugs 315, which connects both ends of traces 311, conductive plug 325 connects only one end of adjacent traces 311 and 321 (respectively being a part of "first inductor subassembly" and a part of "second inductor subassembly"). (*Id.*; *see also* Ex. 1005, ¶[0033].) As such, a POSITA would have also understood that "first inductor subassembly" and "second inductor subassembly" are connected in series. (*Id.,* ¶109.)

c) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor; and

Lee discloses this limitation for at least the same reasons as presented above for limitation 1(e). (*Supra* Section IX.A.1(e); Ex. 1002, ¶110.)

d) wherein when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated.

Lee discloses this limitation for at least the same reasons as presented above for limitation 1(f). (*Supra* Section IX.A.1(f); Ex. 1002, ¶111.)

24. Claim 30

a) The inductor of claim 29 wherein the first inductor subassembly and the second inductor subassembly are oriented such that the first and second inductor subassemblies are positioned about parallel, about perpendicular, or at an angular relationship with respect to each other.

Lee discloses this limitation. (Ex. 1002 ¶112.) For example, Lee discloses that the first and second inductor subassemblies (*supra* Section IX.23 (analysis for

claim 29) are separated from each other because "a conductive plug 325" connects the two assemblies. (Ex. 1005, ¶[0033]; *see also id.* at FIG. 4C.) Thus, a POSITA would have understood that the two subassemblies are positioned "in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other," as the subassemblies are in different planes. (Ex. 1002, ¶78, 79, 112.)

B. Ground 2: Claim 12 is Obvious over Lee in View of Ahn

1. Claim 12

a) The inductor of claim 1 wherein a thickness of the insulating layer is less than about 5 cm.

Lee in combination with Ahn discloses or suggests this limitation. (Ex. 1002, ¶¶113-119.) Lee discloses a "multilayer winding inductor formed in a semiconductor chip" where conductive traces 311 ("first conductor layer" and "second conductor layer") are separated by insulating dielectric layers, including layer 308 ("insulating layer"). (Ex. 1005, ¶[0031]; Ex. 1002, ¶114.) Lee further discloses that its insulating layers may be silicon oxide or dielectric material. (Ex. 1005, ¶[0024].) A POSITA would have understood that the scale of semiconductor components is in the micron range (1 micron is equal to 1/10000 cm) and that the thickness of layers, e.g. conductor layers or insulator layers, in semiconductor devices would be orders of magnitude smaller than 5 cm. (Ex. 1002, ¶114.) Indeed, Lee discloses conductor layer (311) is less than 1 micron.

(Ex. 1005, ¶[0027].) As such, while Lee does not expressly disclose the thickness of its insulating layer, a POSITA would have understood the thickness of the insulating layer in Lee's inductor would have been much less than about 5cm. (Ex. 1002, ¶114.)

Like Lee, Ahn discloses "an integrated circuit structure" formed in a semiconductor substrate comprising spiral-shape inductors separated by insulating or dielectric layers. (Ex. 1031, 1:15-17, 42-45, FIG. 1; *see also id.* at 5:33-6:2.) Just like Lee, Ahn discloses that insulating layers can be a dielectric or oxide. (*Id.,* 5:35-38.) Indeed, Ahn states that an oxide is "typically used for such purposes." (*Id.*; Ex. 1002, ¶115.)

In particular, Ahn discloses an embodiment in figure 4, reproduced below, with insulating layers 53 and 530 ("insulating layer") separating inductors 302 ("first conductor layer") and 312 ("second conductor layer"). (Ex. 1031, 5:45-6:2; *see also id.* at 5:26-32 (describing the inductor layers as conductors).)

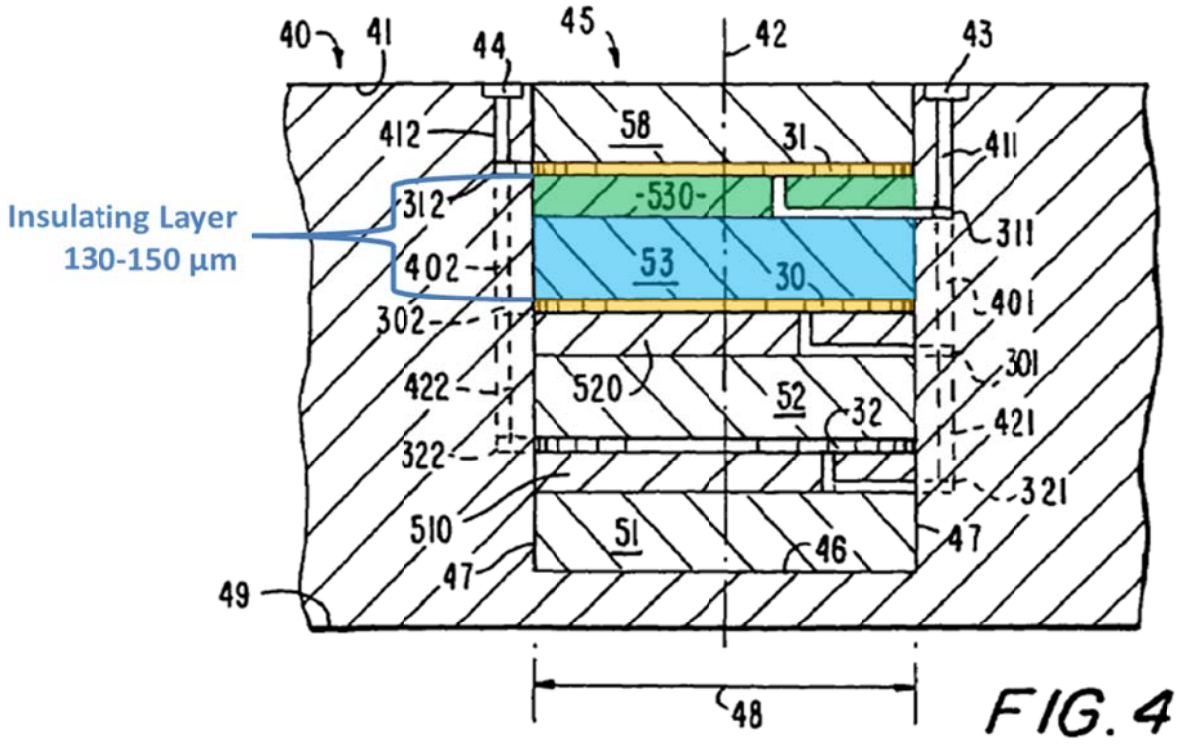


FIG. 4

(*Id.*, FIG. 4 (annotated); Ex. 1002, ¶116.)

Ahn explains that insulating layer 53 (blue) "is preferably formed having a thickness of about 100 µm," and insulating layer 530 (green) is preferably formed with a thickness "between about 30 µm and about 50 µm." (Ex. 1031, 5:52-59.) The insulator layers are sandwiched between conductive inductor layers 30 and 31 (yellow). (*Id.*, 5:52-66.) Thus, insulators 53 and 530 together form an insulator layer about 130 µm to 150 µm separating the conductors. (Ex. 1002, ¶117.)

Given the similarities between Lee and Ahn, a POSITA would have combined the teachings of Lee and Ahn because Lee discloses a multilayer winding inductor formed in a semiconductor substrate using oxide or dielectric

insulator layers and Ahn discloses stacked inductors formed in a semiconductor substrate using oxide or a dielectric insulator layers. (*Id.,* ¶118.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Ahn discloses the thickness of insulator layers in semiconductor inductors, an aspect on which Lee is silent. (*Id.*) *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007).

Moreover, the thickness of an insulating layer is a "result-effective variable" because it affects the overall thickness of the integrated circuit and also determines the amount of the insulation between conducting layers on both sides of the insulating layer. (Ex. 1002, ¶119.) That is, the thickness of the insulation affects the electrical performance of the integrated circuit. (*Id.*) Therefore, if "less than 5 cm" is an optimum number for the insulating layer thickness per claim 12, claim 12 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '960 patent provides no evidence that "less than 5 cm" thickness produces a new or unexpected result, and thus the claimed range cannot form the basis of patentability. (Ex. 1002, ¶119.) *In re Boesch*, 617 F.2d at 276; *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990). Therefore, a POSITA would

have been motivated to optimize the thickness of the insulating layer to achieve a balance between the required insulation and the overall thickness of the integrated circuit. (Ex. 1002, ¶119.)

C. Ground 3: Claim 13 is Obvious over Lee in View of Kyriazidou

1. Claim 13

a) The inductor of claim 1 wherein the inductor has an inductor quality factor greater than about 5.

Lee in combination with Kyriazidou discloses or suggests this limitation. (Ex. 1002, ¶¶120-123.) Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) While Lee does not expressly disclose that the inductor of figures 4A-4C has an "an inductor quality factor greater than about 5," Lee notes that a high value of the quality factor is desirable. (*Id.*, ¶¶[0008], [0009].) A POSITA would have understood that a quality factor of 5 is a relatively modest value, and would understand that by "maintain[ing] the Q value of the inductor," Lee's inductor would exceed a quality factor of 5. (Ex. 1002, ¶121; Ex. 1005, ¶[0035].)

Kyriazidou similarly discloses that "on-chip inductors are significant components of RF integrated circuits and are used in oscillators, impedance matching networks, emitter degeneration circuits, filters, and/or baluns." (Ex. 1019 at 1:26-29.) It discloses that "inductors having a high Q-factor dissipate less

power and thus improve the achievable gain. Further, high Q inductors allow an oscillating circuit to perform with minimal power injection from the driving transistor and hence minimize noise." (*Id.*, 1:39-44.) It further notes that "CMOS technology is widely used for cost effective fabrication of . . . RF integrated circuits" and that "on-chip inductors using CMOS technology are known to have a **modest quality factor** in the range of **5 to 10**." (*Id.*, 1:58-64 (emphasis added).) Furthermore, Kyriazidou discloses that "in one embodiment of an on-chip inductor using CMOS technology, the quality factor may be increased to as much as 150." (*Id.*, 4:29-31.) Therefore, Kyriazidou expressly discloses an "inductor quality factor greater than about 5," and supports the fact that a POSITA would understand Lee's teaching that the disclosed invention maintains the quality factor value as suggesting using a quality factor greater than 5. (Ex. 1002, ¶122.)

In view of Kyriazidou, a POSITA would have found it obvious to fabricate Lee's inductor such that it has a quality factor greater than 5, which would be known to be a "modest quality factor." (Ex. 1002, ¶123.) Indeed, a POSITA would have been motivated to do so because Lee discloses the use of on-chip inductors in RF integrated circuits and Kyriazidou discloses that on-chip inductors in such circuits typically have "a modest quality factor in the range of **5 to 10**" and that it is desirable to increase the quality factor even more given the benefits of a higher inductor quality factor. (*Id.*; Ex. 1019 at 1:60-64.) *See Unwired Planet,*

LLC v. Google Inc., 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). A POSITA would not only have been motivated to fabricate Lee's inductor such that it has a quality factor of at least 5 but also known how to do so. (Ex. 1002, ¶123.)

D. Ground 4: Claim 24 is Obvious over Lee in View of Partovi

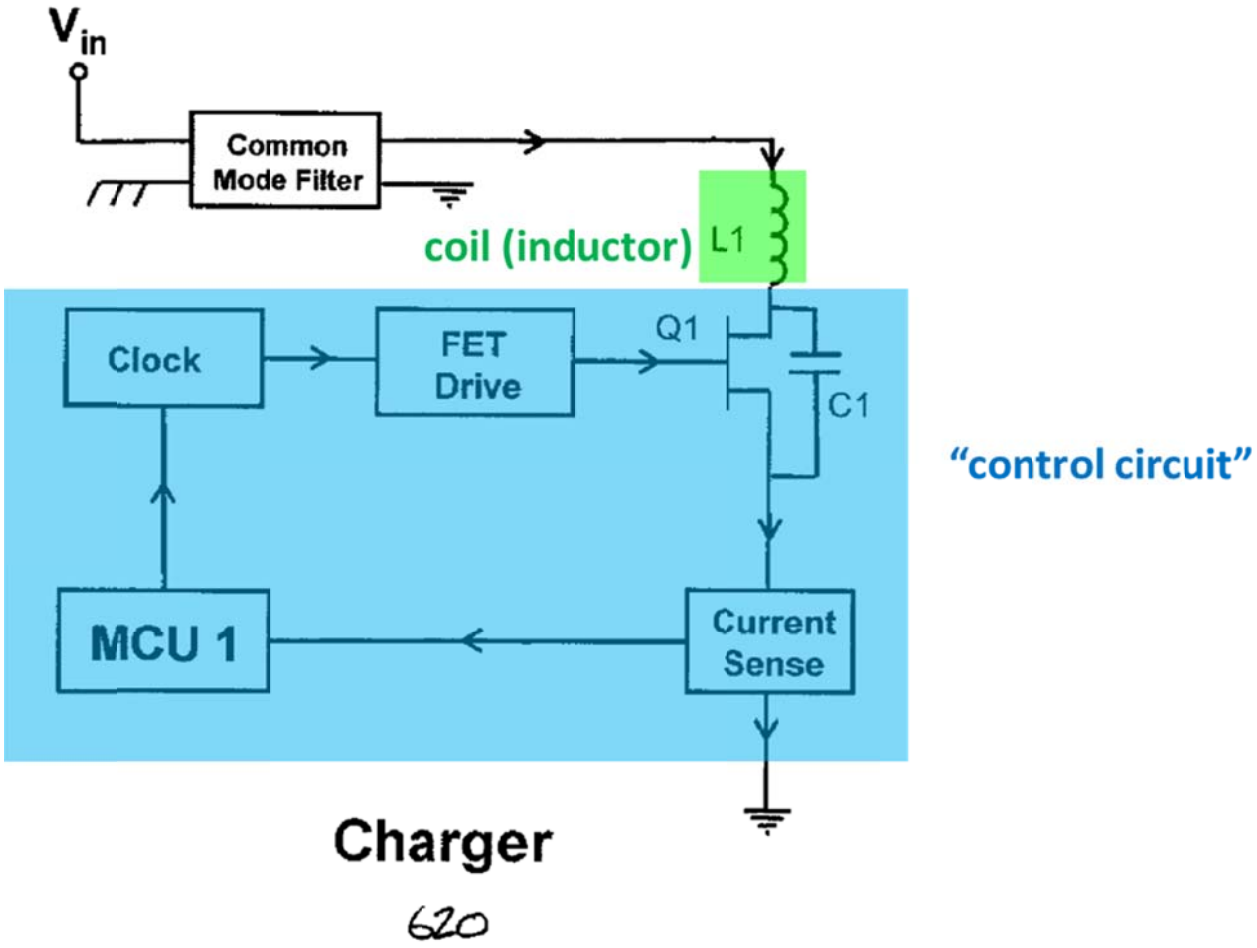
1. Claim 24

a) The inductor of claim 1 wherein a control circuit is electrically connectable to the inductor.

Lee in combination with Partovi discloses or suggests this feature. (Ex. 1002, ¶¶124-127.) Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) Lee further discloses that the inductor of figures 4A-4C is connected to "external or internal circuits" that provide a current passing through the inductor. (*Id.,* ¶ [0034].) But Lee does not disclose what those "external or internal circuits" are or how to utilize the inductor in RF circuits. (Ex. 1002, ¶125.) However, it would have been obvious to use Lee's inductor in an RF circuit, an example of which is disclosed by Partovi and where a control circuit is electrically connectable with the inductor. (*Id.*)

Partovi discloses "a system and method for inductive charging of portable devices." (Ex. 1009 at ¶[0003].) The general principles of Partovi's inductive

charging system are disclosed with reference to figure 2, which discloses power being transferred from a primary coil in a charger to a secondary coil in a receiver (e.g., in a mobile device). (*Id.*, ¶¶[0116]-[0117], FIG. 2; Ex. 1002, ¶126.) Figure 28 of Partovi discloses one implementation of the concepts disclosed in figure 2. (Ex. 1002, ¶126; Ex. 1009 at ¶[0260]-[0261].) In particular, figure 28 discloses "a digital control scheme," where "[t]he primary (charger or power supply) 620 is controlled by a Micro Control Unit (MCU1)." (Ex. 1009 at ¶[0261].) Partovi discloses that MCU1 receives signals from a Current Sensor that is connected in series with the primary coil L1 ("inductor") and then controls the power output by the primary coil L1 by controlling the switching frequency of FET Q1. (*Id.*, ¶¶[0261]-[0265].) In particular, Partovi's figure 28 circuit operates at a frequency of "1-2 MHz" (*id.* at ¶[0265]), which a POSITA would have understood is in the RF band. (Ex. 1002, ¶126; Ex. 1010 at 860 ("The present practicable limits of radio frequency are roughly 10 kHz (kilohertz) to 100 000 MHz (megahertz)"; *see also* Ex. 1009 at FIG. 10 (RFID reader in the charger circuit).) Accordingly, Partovi discloses or suggests "a control circuit is electrically connectable to the inductor." (Ex. 1002, ¶126.)



(Ex. 1009 at FIG. 28 (excerpted and annotated); Ex. 1002, ¶126.)

In view of the above, a POSITA would have combined the teachings of Lee and Partovi because Lee discloses an on-chip inductor used in RF circuits and Partovi discloses the use of RF circuits for inductive power transfer. (Ex. 1002, ¶127.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Partovi discloses specific examples of the use of inductors in RF circuit, an aspect on which Lee is silent. (*Id.*) Furthermore, a POSITA would have understood that using an **on-chip**

inductor in Lee in a circuit like in Partovi would have allowed reducing the size of Partovi's circuit because inductors created on-chip (as opposed to on a PCB like in Partovi) occupy less space. (*Id.*) Indeed, on-chip inductors have other advantages, such as "there are no assembly costs, as the inductors are formed directly on the circuit substrate, and tight tolerance can be achieved." (Ex. 1025 at ¶[0002].) As such, a POSITA would have been motivated to combine the teachings of Lee and Partovi such that Lee's inductor is used in a circuit like in Partovi. (Ex. 1002, ¶127.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). A POSITA would have reasonably expected success in combining the teachings and would have known how to make the necessary changes to the teachings drawn from Lee and Partovi in order to make a functioning circuit. (Ex. 1002, ¶127.)

E. Ground 5: Claims 1-8, 10, 15-22, and 25-30 are Obvious over Lee in View of Alldred

1. Claim 1

As discussed above with respect to claim element 1(f), Lee discloses that the current through its inductor changes (e.g., because the current is an alternating current) and that such an understanding is consistent with Lee's disclosure of the use of on-chip inductors in RF circuits. (*Supra* Section IX.A.1(f).) As discussed

below, Lee in combination with Alldred discloses the use of an on-chip inductor in an RF circuit where an alternating current propagates through the inductor. (Ex. 1002, ¶¶128-129.)

Lee discloses that "[c]onventionally, the on-chip inductor is . . . employed in integrated circuits designed for radio frequency (RF) band." (Ex. 1005, ¶[0005].) Lee further discloses that the **on-chip** inductor of figures 4A-4C is connected to "external or internal circuits" that provide a current to the inductor. (*Id.,* ¶ [0034].) But Lee does not disclose what those "external or internal circuits" are. (Ex. 1002, ¶130.)

Alldred, however, discloses an example of an RF integrated circuit that uses on-chip inductors. Specifically, Alldred discloses "60-GHz radio receiver with on-chip . . . inductors . . . ." (Ex. 1020, Title.) Figure 1 (reproduced below) is a block diagram of the RF integrated circuit receiving a 60 GHz RF signal and that includes, among other things, a low noise amplifier (LNA) and a mixer. (*Id.,* 51 (FIG. 1); Ex. 1002, ¶131.)

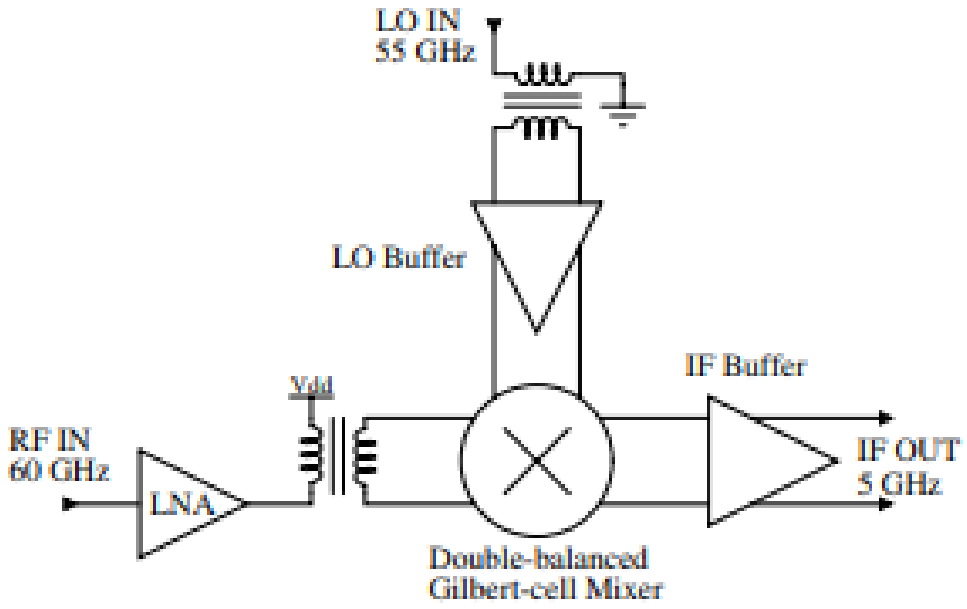


Figure 1. Receiver block diagram.

(Ex. 1020, 51 (FIG. 1).)

The LNA circuit is described in figure 2 and the mixer is described in figure 3. (*Id.,* 51, 52, FIGS. 2-3.) In particular, the LNA receives a 60 GHz and therefore, includes an inductor (see below) whose operating frequency is 60 GHz. (*See id.* at FIG. 2 (reproduced below); *id*. at 51 ("The inductors between the transistors in each stage absorb parasitic capacitance for increased gain over a broad bandwidth which extends beyond 60 GHz."); Ex. 1002, ¶132.)

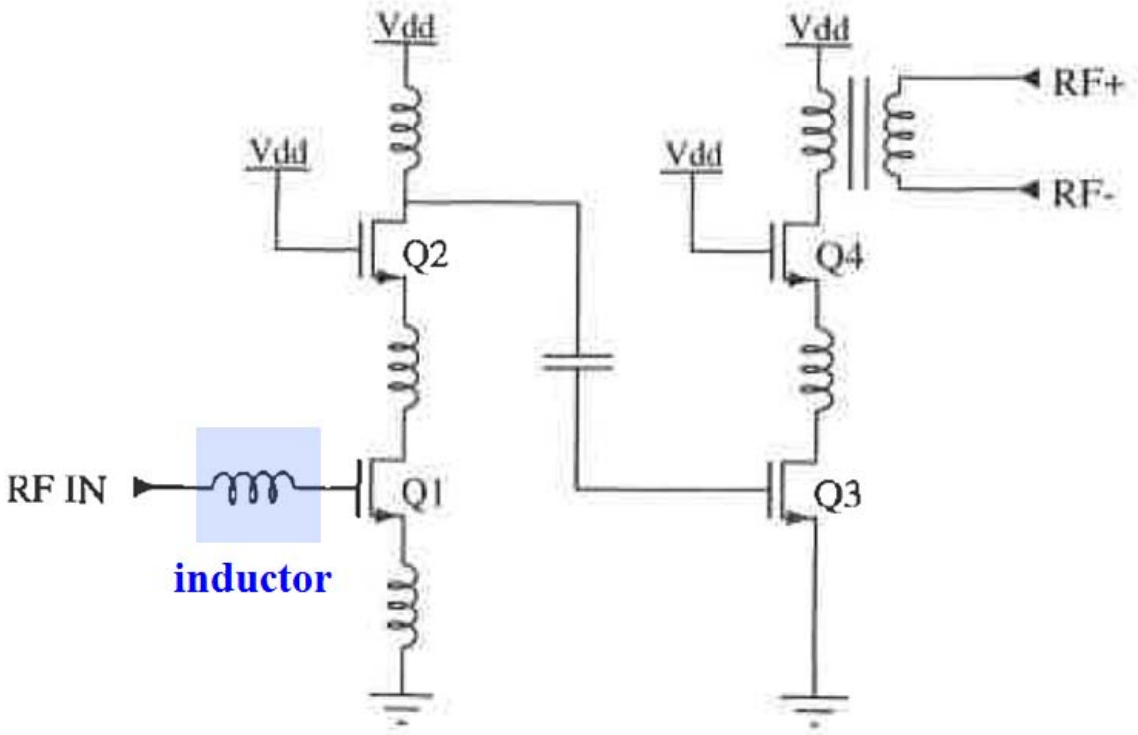


Figure 2. Two-stage cascode LNA schematic.

(Ex. 1020, FIG. 2 (annotated); Ex. 1002, ¶132.)

A POSITA would have combined the teachings of Lee and Alldred because Lee discloses that on-chip inductors are used in RF circuits and Alldred discloses one example of an RF circuit that uses on-chip inductors. (Ex. 1002, ¶133.) A POSITA would have recognized that it would have been advantageous to combine the teachings of these references because Lee discloses how to make on-chip inductors, an aspect on which Alldred is silent. (*Id.*) That is, the teachings of the two references complement each other. (*Id.*) Indeed, the combination of Lee with Alldred as discussed above in this section would have been a mere "combination of

familiar elements according to known methods [to] yield predictable results," as such a combination would have combined teachings regarding Lee's on-chip inductors with Alldred's teachings regarding an RF circuit that uses such inductors. KSR, 550 U.S. at 416. Moreover, because these two references complement each other, a POSITA would have recognized that these references would have been beneficially combined in the above manner. (Ex. 1002, ¶133.) *KSR*, 550 U.S. at 418 (explaining that for an obviousness analysis "a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ), 421 ("A person of ordinary skill is also a person of ordinary creativity").

As discussed above, in the Lee-Alldred combination, the inductor would receive a 60 GHz signal and therefore, an AC current would propagate through the inductor. (Ex. 1002, ¶134.) Such an AC current (which changes in magnitude) would result in the change of magnetic flux generated within the inductor, and therefore, the Lee-Alldred combination discloses or suggests claim elements 1(e) and 1(f). (*Id.*; *supra* Sections IX.A.1(e), (f).)

Lee in combination with Alldred discloses or suggests the remaining limitations of claim 1 for the reasons discussed above for claim 1 with the only modification to the analysis for claim 1 being that discussed above. (*Supra* Section IX.A.1; Ex. 1002, ¶135.)

2. Claim 2

Lee in combination with Alldred discloses or suggests the features of claim 2 for the reasons discussed above in Section IX.A.2. But claim 2 is disclosed or suggested for the additional reason that in the Lee-Alldred combination, an RF current (i.e., an alternating current) would propagate through Lee's inductor (*supra* Section IX.E.1) and because an AC current changes in magnitude over time, an EMF will necessarily be generated in the inductor. (Ex. 1002, ¶136; Ex. 1001, 1:54-64, 14:17-27.)

3. Claim 3

Lee in combination with Alldred discloses or suggests the features of claim 3 for the reasons discussed above in Section IX.A.3. But claim 3 is disclosed or suggested for the additional reason that in the Lee-Alldred combination, an RF current (i.e., an alternating current) would propagate through Lee's inductor (*supra* Section IX.E.1) and because an AC current changes in magnitude over time, and the magnetic flux within the inductor will change proportionally to the change in current through the inductor. (Ex. 1002, ¶137; Ex. 1001, 1:54-64, 14:17-27.)

4. Claims 5-7

The Lee-Alldred combination discloses or suggests the features of this claim because at a 60 GHz frequency, the skin depth for Lee's inductor (formed of copper with a resistivity of 1.678 10^{-8} ohm-metres and relative permeability of 1)

will be 0.2662 μm, and therefore, the thickness (i.e., 0.53 μm) of the looped conductive layers 311 (including the "first conductor layer" and the "second conductor layer") is almost two times the skin depth. (Ex. 1002, ¶138 (citing https://chemandy.com/calculators/skin-effect-calculator.htm); *supra* Section IX.E.1.)

5. Claim 15

The Lee-Alldred combination discloses or suggests the features of claim 15 because the frequency in the combination is 60 GHz. (Ex. 1002, ¶139; *supra* Section IX.E.1.)

6. Claim 21

Lee in combination with Alldred discloses or suggests the features of claim 21 because the inductor is connected with two stage of a low noise amplifier operating at 60 GHz. (Ex. 1002, ¶140; *supra* Section IX.E.1.) Each of the two stages is an "electrical circuit." (Ex. 1002, ¶140.)

7. Claim 22

The Lee-Alldred combination discloses or suggests the features of claim 22 because, in the Lee-Alldred combination, the "electrical circuit" includes two amplification stages, which a person of ordinary skill in the art would have understood is "an amplifying circuit," as recited in claim 22. (*Supra* Section IX.E.6; Ex. 1002, ¶141.)

8. Claim 29

Lee in combination with Alldred discloses or suggests the features of claim 29 for reasons similar to those discussed in Section IX.A.23 (analysis for claim 29 in Section IX.A.) (Ex. 1002, ¶142.) The combination further discloses claim elements 29[c] and 29[d] because it discloses that an AC current (which changes in magnitude) propagates through Lee's inductor. (*Supra* Section IX.A.23(c), (d); supra Section IX.E.1.) The propagation of such an AC current would result in the generation of magnetic flux and an "inductance" in the inductor. (*Supra* Section IX.A.23(c), (d).)

9. Claims 4, 8, 10, 16-20, 25-28, and 30

Lee in combination with Alldred discloses or suggests the limitations of these claims for reasons similar to those discussed in Section IX.A for these claims. (Ex. 1002, ¶143.) The same analysis presented above for these claims in Ground 1 is also applicable for the Lee-Alldred combination discussed above in Sections IX.E.1 (claim 1) and IX.E.8 (claim 29). (Ex. 1002, ¶143.) The combination of Lee with Alldred does not affect the analysis for these claims in Section IX.A. (*Id.*)

F. Ground 6: Claim 12 is Obvious over Lee in View of Alldred and Ahn

As discussed above in Section IX.E.1, Lee view of Alldred discloses or suggests all of the limitations of claim 1. But to the extent that the Lee-Aldred

combination does not explicitly disclose claim 12, a POSITA would have combined the teachings of Lee and Alldred with Ahn for the same reasons that a POSITA would have combined the teachings of Lee with Ahn that renders claim 12 obvious (*supra* Section IX.B). Therefore, the Lee-Alldred-Ahn combination renders claim 12 obvious for reasons similar to those discussed above in Section IX.B. (Ex. 1002, ¶144.) The addition of Alldred does not affect the Lee-Ahn combination in Section IX.B because Alldred was simply used to show an example of the use of an inductor in an RF circuit. (*Id.*)

G. Ground 7: Claim 13 is Obvious over Lee in View of Alldred and Kyriazidou

As discussed above in Section IX.E.1, Lee view of Alldred discloses or suggests all of the limitations of claim 1. But to the extent that the Lee-Aldred combination does not explicitly disclose claim 13, a POSITA would have combined the teachings of Lee and Alldred with Kyriazidou for the same reasons that a POSITA would have combined the teachings of Lee with Ahn that renders claim 13 obvious (supra Section IX.C). Therefore, the Lee-Alldred-Kyriazidou combination renders claim 13 obvious for reasons similar to those discussed above in Section IX.C. (Ex. 1002, ¶145.) The addition of Alldred does not affect the Lee-Kyriazidou combination in Section IX.C because Alldred was simply used to show an example of the use of an inductor in an RF circuit. (*Id.*)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-8, 10, 12, 13, 15-22, and 24-30 of the ’960 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,680,960 contains, as measured by the word-processing system used to prepare this paper, 13687 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
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Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,680,960 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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