UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

NUCURRENT, INC.,
Patent Owner

Patent No. 8,680,960

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,680,960

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 8,680,960
Ex. 1002	Declaration of Dr. Steven Leeb
Ex. 1003	Curriculum Vitae of Dr. Steven Leeb
Ex. 1004	Prosecution History of U.S. Patent No. 8,680,960
Ex. 1005	RESERVED
Ex. 1006	Semat and Katz, *Physics*, Chapters 29-32 (1958)
Ex. 1007	RESERVED
Ex. 1008	RESERVED
Ex. 1009	U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi")
Ex. 1010,	IEEE Standard Dictionary (1996)
Ex. 1011	U.S. Patent Application Publication No. 2007/0089773 A1 to Koester ("Koester")
Ex. 1012	U.S. Patent Application Publication No. 2012/0280765A1
Ex. 1013	U.S. Patent No. 6,432,497
Ex. 1014	RESERVED
Ex. 1015	Reinhold et al., *Efficient Antenna Design of Inductive Coupled RFID-Systems with High Power Demand* (2007)
Ex. 1016	U.S. Patent No. 4,549,042
Ex. 1017	U.S. Patent No. 5,812,344
Ex. 1018	Wheeler, *Formulas for the Skin Effect* (1942)
Ex. 1019	RESERVED

Ex. 1020	RESERVED
Ex. 1021	RESERVED
Ex. 1022	U.S. Patent No. 9,912,173 ("Tseng")
Ex. 1023	U.. Patent No. 7,248,138 ("Chiang")
Ex. 1024	U.S. Patent No. 5,084,958 ("Yerman")
Ex. 1025	U.S. Patent Application Publication No. 2007/0126544 A1 ("Wotherspoon")
Ex. 1026	RESERVED
Ex. 1027	RESERVED
Ex. 1028	U.S. Patent No. 9,820,374
Ex. 1029	U.S. Patent No. 7,601,919 ("Phan")
Ex. 1030	U.S. Patent No. 5,108,825
Ex. 1031	RESERVED
Ex. 1032	U.S. Patent No. 5,745,331
Ex. 1033	RESERVED
Ex. 1034	U.S. Patent No. 6,608,363

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-8, 10, 12-13, 15-22, and 24-30 ("the challenged claims") of U.S. Patent No. 8,680,960 ("the '960 patent") (Ex. 1001), which, according to PTO records, is assigned to NuCurrent, Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claim should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Related Matters: The '960 patent is at issue in *NuCurrent, Inc. v. Samsung Electronics Co. Ltd.* and *Samsung Electronics America, Inc.*, Case No. 1:19-cv-00798 (S.D.N.Y.). The '960 patent shares the same specification as U.S. Patent No. 8,698,591 ("the '591 patent"); U.S. Patent No. 8,710,948 ("the '948 patent"); and U.S. Patent No. 9,300,046 ("the '046 patent"). Petitioner is concurrently filing petitions challenging these patents. Moreover, Patent Owner has asserted U.S. Patent No. 9,941,729 ("the '729 patent") in the above litigation.

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel is (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), and (3) Howard Herr (*pro hac vice*

admission to be requested). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-NuCurrent-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '960 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-8, 10, 12-13, 15-22, and 24-30 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-4, 10, 15-17, 19, 21, 22, and 24-27 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") (Ex. 1009); and

Ground 2: Claims 5-7 and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 9,912,173 ("Tseng") (Ex. 1022); and

Ground 3: Claims 1-4, 10, 15-22, 24-27, 29, and 30 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 7,248,138 ("Chiang") (Ex. 1023); and

Ground 4: Claims 8, 12, 27, and 28 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 7,601,919 ("Phan") (Ex. 1029).

Ground 5: Claims 8, 12, 27, and 28 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and Phan.

Ground 6: Claims 5-7 and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and Tseng.

The '960 patent issued from U.S. patent application no. 13/797,387 (the '387 application"), filed March 12, 2013. (Ex. 1001, Cover.) The '960 claims priority to a series of related applications, including Provisional Application No. 61/158,688, filed March 9, 2009. For purposes of this proceeding only, Petitioner assumes the earliest effective filing date of the '960 patent is March 9, 2009.

Partovi was filed May 7, 2008. (Ex. 1009, Cover). Tseng is a continuation of U.S. Application No. 11/901,158, filed September 14, 2007. (Ex. 1022 at Cover). Phan was filed October 21, 2005. (Ex. 1029 at Cover). Therefore, Partovi, Tseng, and Phan are prior art under pre-AIA 35 U.S.C. § 102(e). Chiang issued on July 24, 2007. (Ex. 1023 at Cover). Therefore, Chiang is prior art under

pre-AIA 35 U.S.C. § 102(b). None of these references were considered by the Patent Office during prosecution of the '960 patent. (*See, e.g.*, Ex. 1001, Cover ("References Cited"); Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '960 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering, or a similar discipline and at least two years additional relevant experience with power electronics, including design or manufacturing of inductors. (Ex. 1002, ¶¶15-16.)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '960 PATENT AND THE PRIOR ART

A. The '960 Patent

The '960 patent, titled "Multi-layer-multi-turn structure for high efficiency inductors," is directed to "an inductor having a plurality of conductor layers separated by insulator layers," "for incorporation within electric circuits." (Ex. 1001, Abstract, 1:36-39, 4:22-23; *see also id.*, 4:24:25 (disclosing the inductor described is "most notably" for "electrical circuits that operate within and above

[1] Petitioner submits the declaration of Dr. Steven Leeb (Ex. 1002), an expert in the field of the '960 patent. (Ex. 1002, ¶¶1-16; Ex. 1003.)

the radio frequency range of at least 3 kHz"); Ex. 1002, ¶¶31-36.) The '960 patent discloses that one of its objectives is "reducing resistance loss . . . of the inductor structure" with a "multi-layer wire configuration." (Ex. 1001, 4:15-21.)

With reference to figure 1, the '960 patent discloses "a high-level diagram of an inductor 100 for use in an electronic or electrical circuit . . . compris[ing] a coil 102 and a multi-layer wire 104, that "may have a plurality of turns 122 . . . around a central axis point 124." (*Id.*, 15:8-11, 16:31-36.)

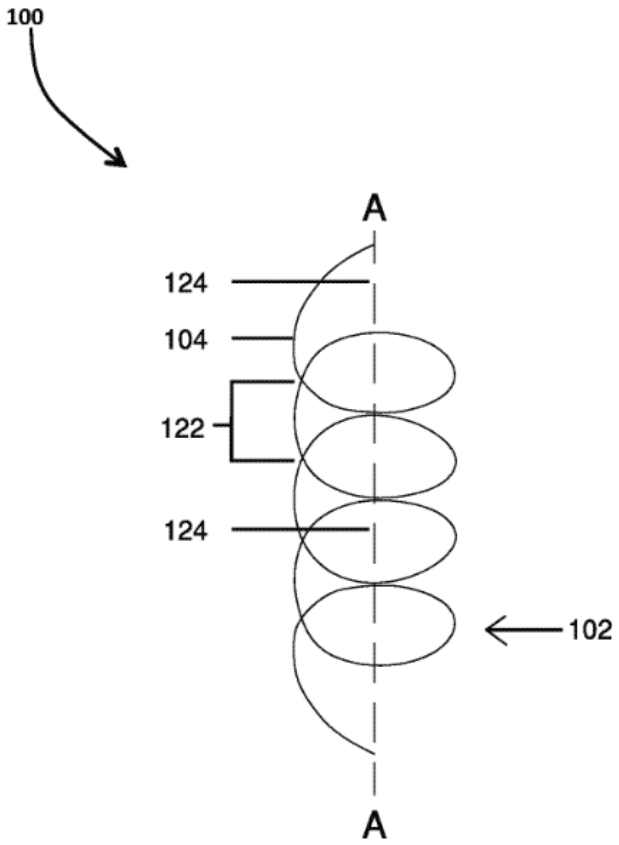
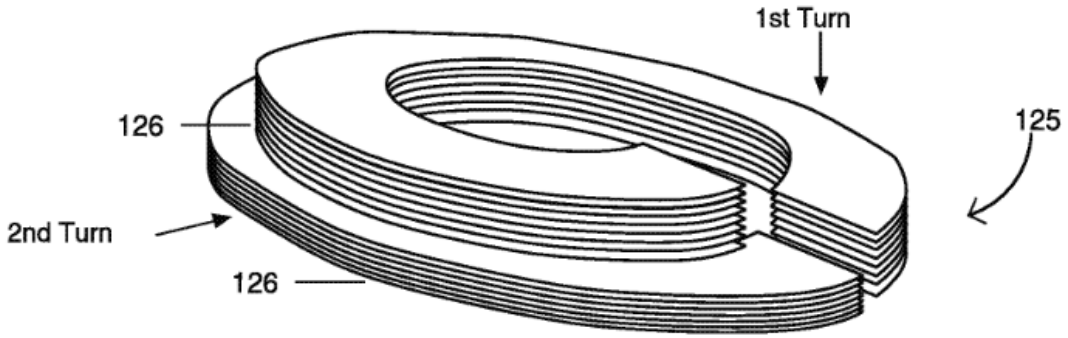


FIG. 1

(*Id.*, FIG. 1.)

The ’960 patent further discloses various embodiments including “a double turn circular spiral-solenoidal coil” in figure 3B “where each turn has N layers,” and “where ‘N’ is a number equal to or greater than one.” (*Id.*, FIG. 3B, 12:34-36, 16:40-47.)



F I G. 3B

(*Id.*, FIG. 3B.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415

F.3d at 1313; *see also id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002, ¶37.)

[2] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '960 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

IX. DETAILED EXPLANATION OF GROUNDS

As discussed below, claims 1-8, 10, 12-13, 15-22, and 24-30 are unpatentable in view of the prior art. (Ex. 1002, ¶¶45-157.)

A. Ground 1: Partovi Renders Obvious Claims 1-4, 10, 15-17, 19, 21, 22, 24-27

1. Claim 1

Preamble: An inductor comprising:

Partovi discloses this limitation. (Ex. 1002, ¶46.) For example, Partovi discloses an inductor, e.g., a coil (L_p) 116 used in an inductive power transfer system 110 as shown in figure 2 (reproduced below). (Ex. 1009, ¶[0118]; *see also id.*, Abstract; Ex. 1002, ¶¶38-44, 46.)

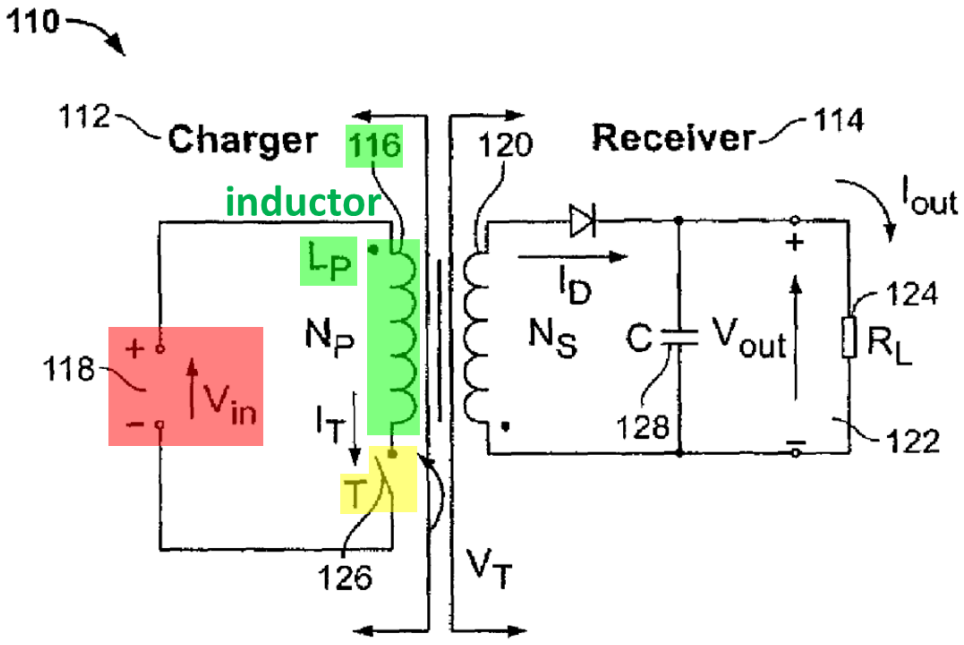


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶46.) Inductive power transfer system 110 includes a charger 112 having a primary coil (L_p) 116 (the claimed "inductor"), a power source (V_{in}) 118, and a switch (T) 126. (Ex. 1009, ¶¶[0117], [0018].) In operation, by switching switch 126 at a certain frequency, an alternating current flows through coil 116, which in turn generates an alternating magnetic field. (*Id.*, ¶¶[0117]-[0118]; *see also id.*, ¶¶ [0013], [0091], [0119].) Accordingly, Partovi discloses an inductor. (*See* citations and analyses below for the remaining elements of this claim; Ex. 1002, ¶46.)

a) a first conductor layer;

Partovi discloses or suggests this limitation. (Ex. 1002, ¶47.) For example, as discussed above in Section IX.A.1 (preamble), Partovi discloses a primary coil 116 ("inductor") with reference to a figure 2. (*See supra* Section IX.A.1 (preamble); Ex. 1009, ¶[0117] ("primary coil Lp 116").) Partovi further discloses, with reference to figure 18, an implementation of such a coil for "creat[ing] higher [magnetic] flux densities and more efficient power transfer." (Ex. 1009, ¶[0224]; *see also id.*at ¶[0212].)

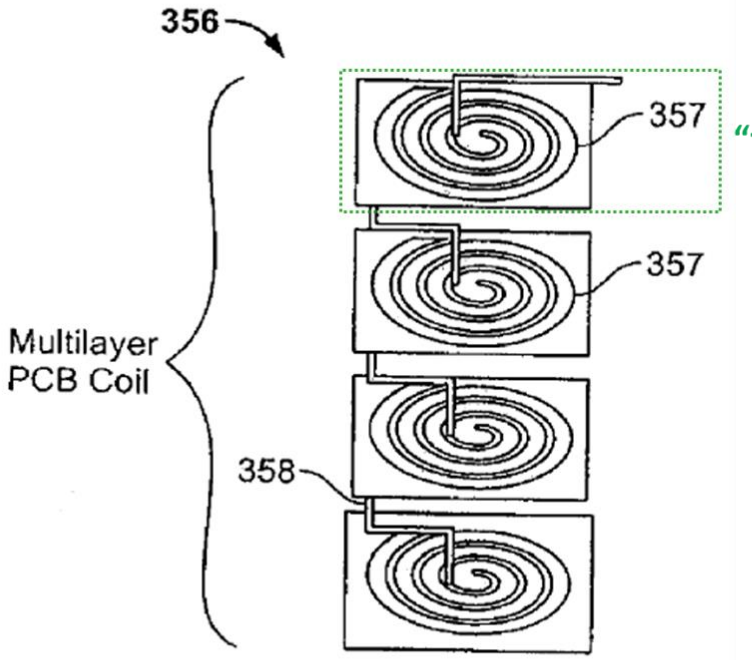


FIG.18

(*Id.*, FIG. 18 (annotated); Ex. 1002, ¶47.)

Partovi discloses that "to achieve higher flux densities, a coil is constructed with two or more layers, for example by using two or more layers of printed circuit board." (Ex. 1009, ¶[0212].) Figure 18 describes an example of such a multi-layer coil 356. (*Id.*, ¶¶[0212], [0224].) For example, multi-layer coil 356 includes four layers 357, where the top most layer 357 constitutes a "first conductor layer," as recited in claim element 1[a]. (Ex. 1002, ¶48.) In particular, Partovi explains that "coil 356 is created in separate PCB layers 357, which are then connected 358, and manufactured together via common techniques used in PCB fabrication, for example by use of a via or contacts." (Ex. 1009, ¶[0224], FIG. 18; *see also id.*,

¶¶[0213]-[0226]; Ex. 1002, ¶48.) A POSITA would have understood that a "PCB layer" is a conductive layer because the different PCB layers are connected through a "via or contacts" (Ex. 1009, ¶[0224]) and a via or contact is used to connect two conductive layers. (Ex. 1002, ¶48.) This is further confirmed by Partovi, which discloses that the coils of the inductor "can be made of copper material." (Ex. 1009, ¶[0225]; *see also id.*, ¶[0248].) When read as a whole, it would have been apparent to a POSITA that the multi-layer coil structure of figure 18 is applicable to the primary coil Lp 116 from figure 2. (Ex. 1002, ¶48.) That is, a POSITA would not have understood the disclosure of figure 18 as being an unrelated embodiment to figure 2, and instead would have understood that the disclosure of figure 18 may apply to all circuit implementations disclosed by Partovi. (*Id.*)

To the extent that the Patent Owner argues or the Board finds that the inductive power transfer system 110 of figure 2 (and other circuit implementations similarly disclosed in Partovi) and the multi-layer coil 356 of figure 18 constitute unrelated embodiments, it would have been obvious for a POSITA to combine the teachings of figure 2 and figure 18 such that the primary coil 116 in figure 2 is implemented as a multi-layer structure like in figure 18. (Ex. 1002, ¶49.)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary

skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007).

Partovi discloses that implementing a coil with multiple layers "allow[s] compact fabrication of high flux density coils." (Ex. 1009, ¶[0212].) By stacking the coils in multiple layers, "overall width of the coil is not increased" and "[t]his technique can be particularly useful for cases where small x-y coil dimensions are desired, and can be used to create higher flux densities and more efficient power transfer." (*Id.* ¶[0224].) As such, a POSITA would have recognized the above discussed benefits of using multi-layer coils and would have been motivated to use such multi-layer coils when implementing primary coil Lp 116 in figure 2 of Partovi because using such a multi-layered coil would have furthered Partovi's objectives of having devices with a "compact" design. (*Id.*, ¶¶[0010] (disclosing that "a common problem with such inductive units is that the windings are bulky, which restricts their use in lightweight portable devices"), [0212] (disclosing "multiple layer boards can be used to allow compact fabrication"), [0224] (disclosing a need for a coil design "where small x-y coil dimensions are desired"); Ex. 1002, ¶50.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]").

Furthermore, a POSITA would not have been deterred from utilizing a multi-layer coil inductor in any of Partovi's circuits (including the circuit of figure 2). (Ex. 1002, ¶51.) For example, Partovi discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212].) Partovi does not limit the primary coil used in any of its circuits (including figure 2) to a certain size or shape. Indeed, Partovi explains that the primary coil "can be formed in any number of different shapes" and "can also be **distributed in layers** of coils, spirals, and other various shapes." (Ex. 1009, ¶[225] (emphasis added).)

Moreover, a POSITA would have had the knowledge and skills to implement the primary coil 116 in figure 2 of Partovi as a multi-layer coil (like in figure 18 of Partovi). (*Id.*, ¶52.) Accordingly, Partovi discloses or suggests implementing primary coil 116 as a multi-layer coil (like in figure 18) and therefore, discloses an "inductor" that comprises "a first conductor layer." (*Id*. 1002, ¶53.)

b) a second conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive;

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶54-55.) For example, as explained above with respect to claim element 1(a), a POSITA would

have been motivated to implement Partovi's coil 116 as a multi-layer coil as shown in figure 18. (*See supra* Section IX.A.1(a); Ex. 1002, ¶54.) Such a multi-layer coil includes a second PCB layer 357 ("second conductor layer"). (Ex. 1009, FIG. 18, ¶¶[0212]-[0226]; *supra* Section IX.A.1(a) (explaining that each PCB layer is a conductive layer); Ex. 1002, ¶54.)

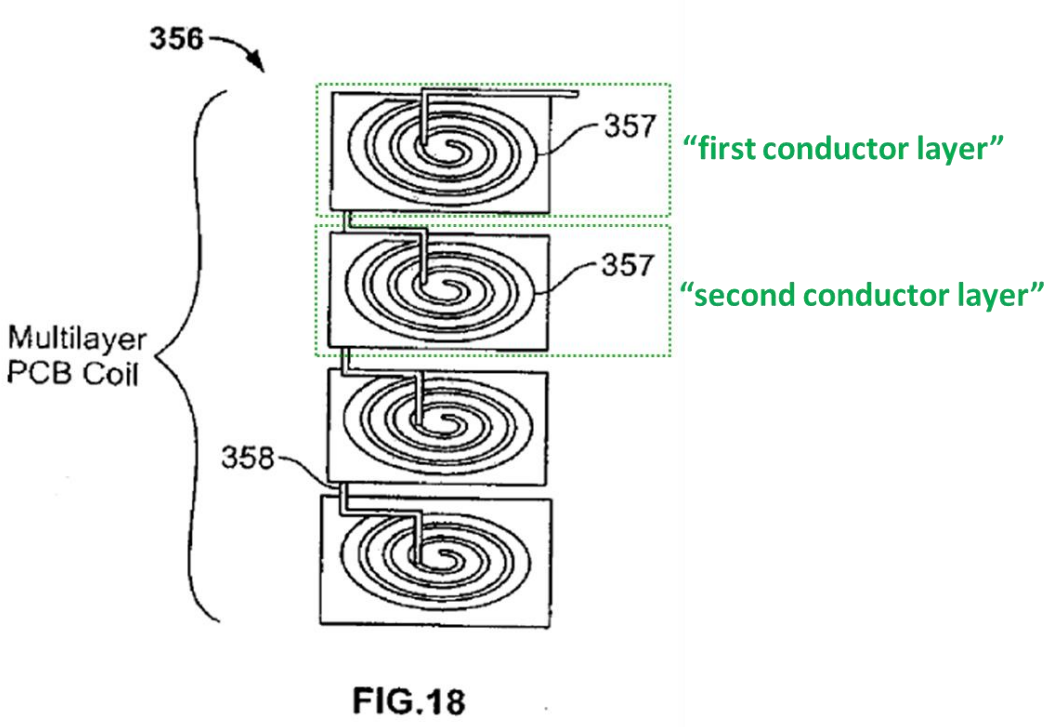


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶54.) Like the "first conductor layer" disclosed in Partovi, the disclosed "second conductor layer" can be "made of copper material." (Ex. 1009, ¶[0225]; *see also id.*, ¶[0248].) Accordingly, Partovi discloses "the first conductor layer and the second conductor layer being electrically conductive." (Ex. 1002, ¶54.)

Furthermore, Partovi discloses that the multi-layer PCB coil 356 "is created in **separate** PCB layers 357." (Ex. 1009, ¶[0224] (emphasis added), FIG. 18.) Accordingly, consistent with figure 18, Partovi discloses "a second conductor layer spaced apart from the first conductor layer." (Ex. 1002, ¶55.)

c) an insulator layer positioned in the space between the first conductor layer and the second conductor layer;

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶56-59.) Partovi discloses that the multi-layer PCB coil 356 (including the claimed "first conductor layer" and "second conductor layer") "is created in **separate** PCB layers 357," which are connected by via or contacts using "common techniques used in PCB fabrication." (Ex. 1009, ¶[0224] (emphasis added).) Because the PCB layers are "separate" and there is a connector between two PCB layers, a POSITA would have understood that there is an insulator between them as otherwise the two layers would be deemed the same layer and no connector would be needed. (Ex. 1002, ¶¶57-58.) The use of a via or contact between the PCB layers also clearly indicates the presence of an insulating layer between the traces. (*Id.*)

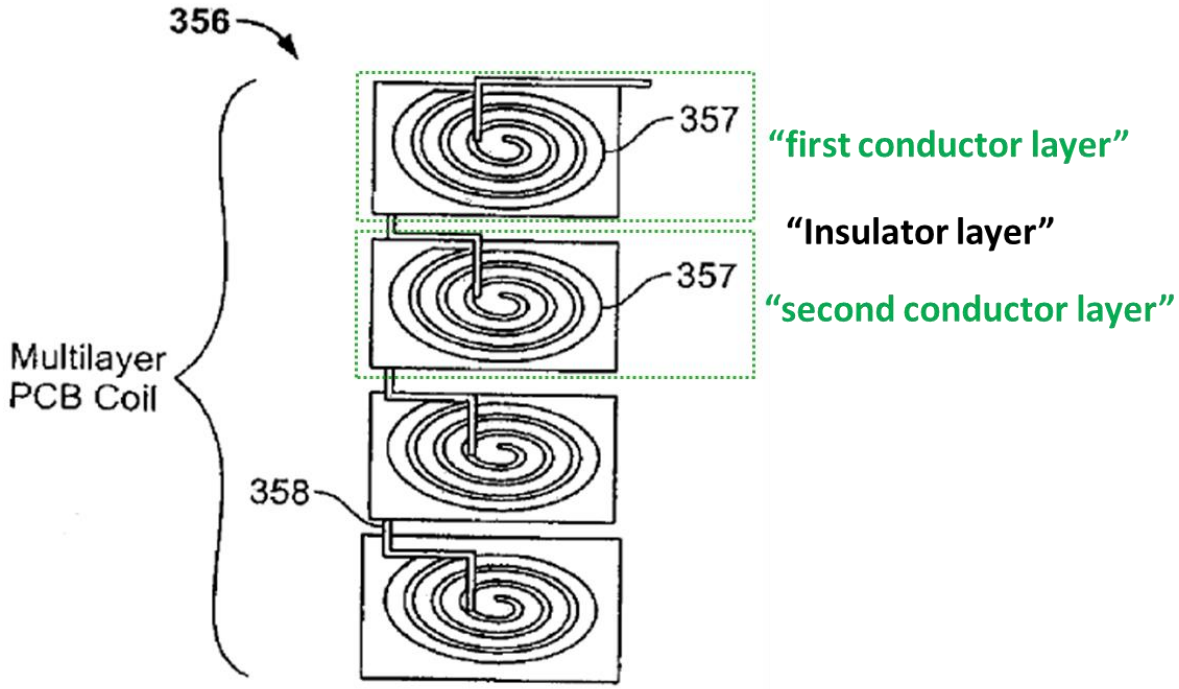


FIG.18

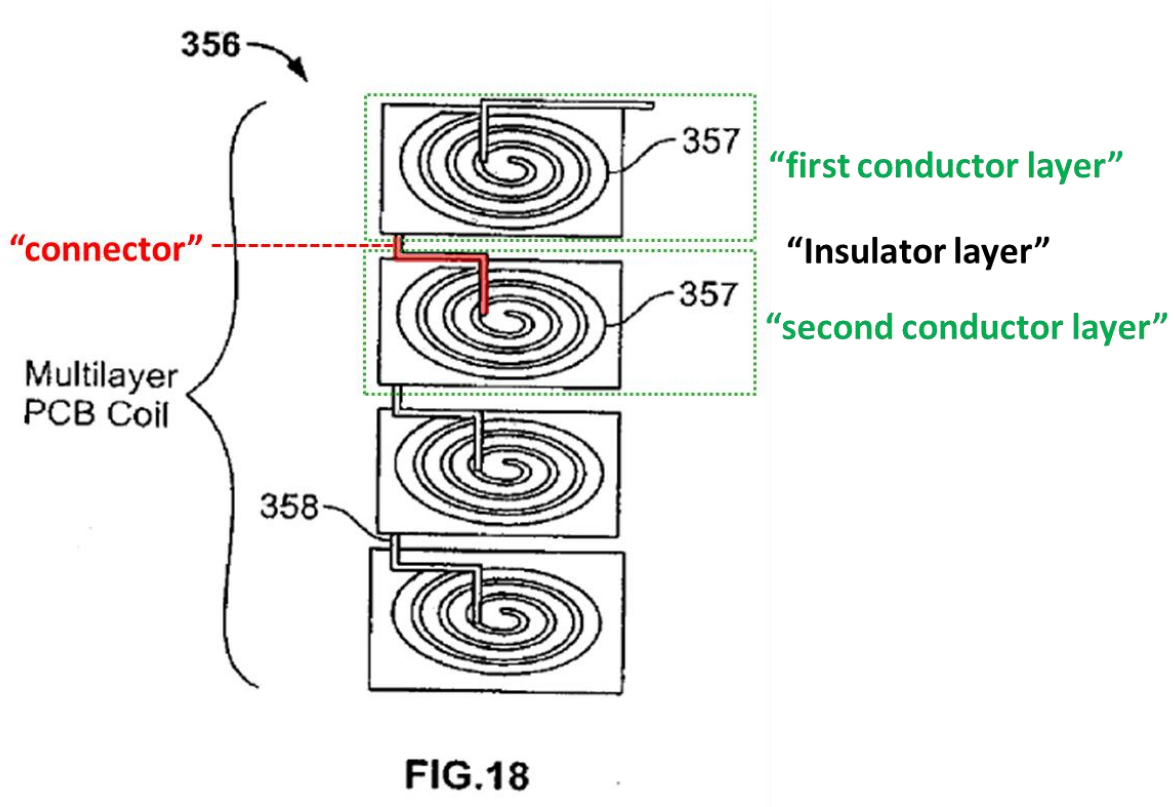
(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶56.)

Thus, Partovi discloses "an insulator layer" that is positioned in the space between all four layers 357, including the space between the top two layers ("first conductor layer" and "second conductor layer"). (Ex. 1002, ¶59.)

d) at least one connector electrically connecting the first conductor layer and the second conductor layer; and

Partovi discloses or suggests this limitation. (Ex. 1002, ¶60.) For example, Partovi discloses "a multi-layer PCB coil 356 is created in separate PCB layers 357" (including "the first conductor layer and the second conductor layer") which

are then "connected [by a via or contact] 358," as shown in figure 18 below. (Ex. 1009, ¶[0224], FIG. 18.)



(*Id.*, FIG. 18 (annotated); Ex. 1002, ¶60.)

e) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor; and

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶61-63.) As discussed above in Section IX.A.1(preamble), Partovi discloses that an AC current flows through the primary coil 116 resulting in the generation of an AC magnetic field. (*See supra* Section IX.A.1(preamble); Ex. 1009, ¶¶[0117], [0118], *see also id.*, ¶¶[0013], [0119].) For example, Partovi discloses that an "AC voltage" is

generated "across the primary coil Lp 116" and as a result, an "AC magnetic field" is generated. (Ex. 1009, ¶¶[0117].) The application of a voltage across the primary coil Lp 116 would therefore result in an AC current propagating through the primary coil Lp 116 the value of which would be proportional to the ratio of the applied voltage and the impedance of the primary coil Lp 116. (Ex. 1002, ¶61.) This AC current is shown as I_T in figure 2. (*Id.*)

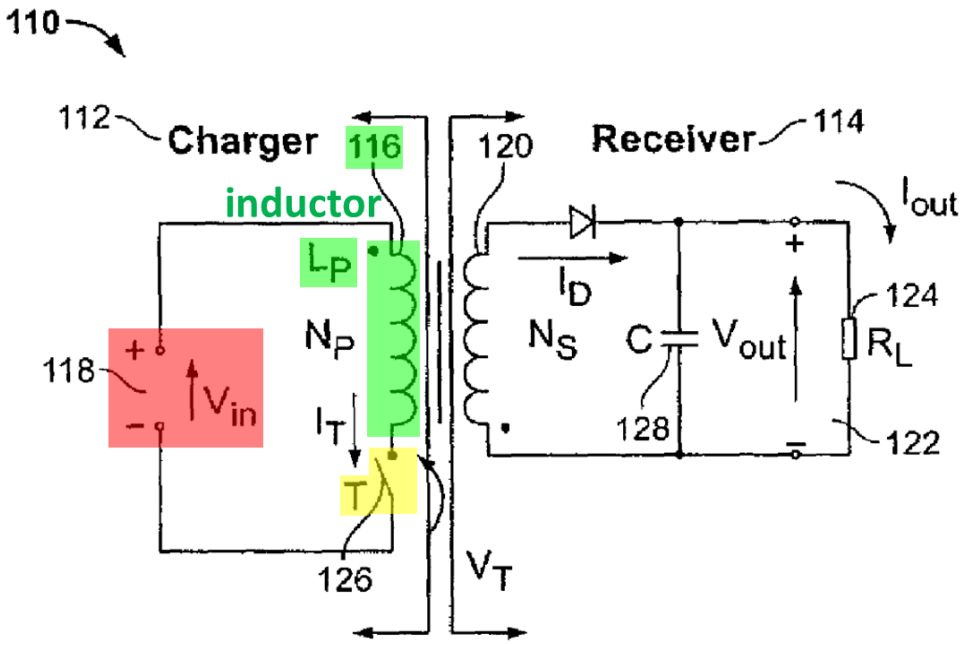


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶61.)

Because the primary coil Lp 116 includes the "first conductor layer" (*supra* Section IX.A.1(a)), the same current I_T also passes through the "first conductor layer." (*Id.*) Moreover, generation of a magnetic field is associated with

generation of a magnetic flux. (Ex. 1002, ¶62; Ex. 1006, 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil."), 554-555; Ex. 1009, ¶[0212], FIG. 18.) Therefore, Partovi system discloses that "when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor." (Ex. 1002, ¶62.)

Indeed, claim element 1[e] merely claims an inherent property of an inductor like primary coil 116. (Ex. 1006, 557-559, 560-65, 560-565, 604; Ex. 1002, ¶63.) The '960 patent admits as much. (Ex. 1001, 1:54-56.)

f) wherein when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated.

To begin, as admitted by the '960 patent, the claimed limitation is an inherent property of an inductor. (Ex. 1002, ¶64.) For example, the '960 patent admits that. (Ex. 1001, 1:54-64, 14:17-27; Ex. 1002, ¶64.) Therefore, when there is a change in the inductor current's frequency, magnitude, or waveform shape, an inductance is necessarily generated. (Ex. 1002, ¶64.) Accordingly, Partovi necessarily discloses this feature because Partovi discloses primary coil 116, which is an inductor. (*Id.*; *see also* Ex. 1009, ¶[0247] ("inductance of the coil").)

Furthermore, Partovi discloses this limitation for the following additional reasons. (Ex. 1002, ¶65.)

(1) **Partovi discloses "a change in . . . a magnitude . . . of the propagated electrical current"**

As discussed in Section IX.A.1(preamble), Partovi discloses with reference to figure 2 (shown below) that by switching switch 126 at a certain frequency, an alternating current is generated and provided through the inductor coil. (Ex. 1009, ¶¶[0117]-[0118]; *see also id.*, ¶¶[0013], [0119].)

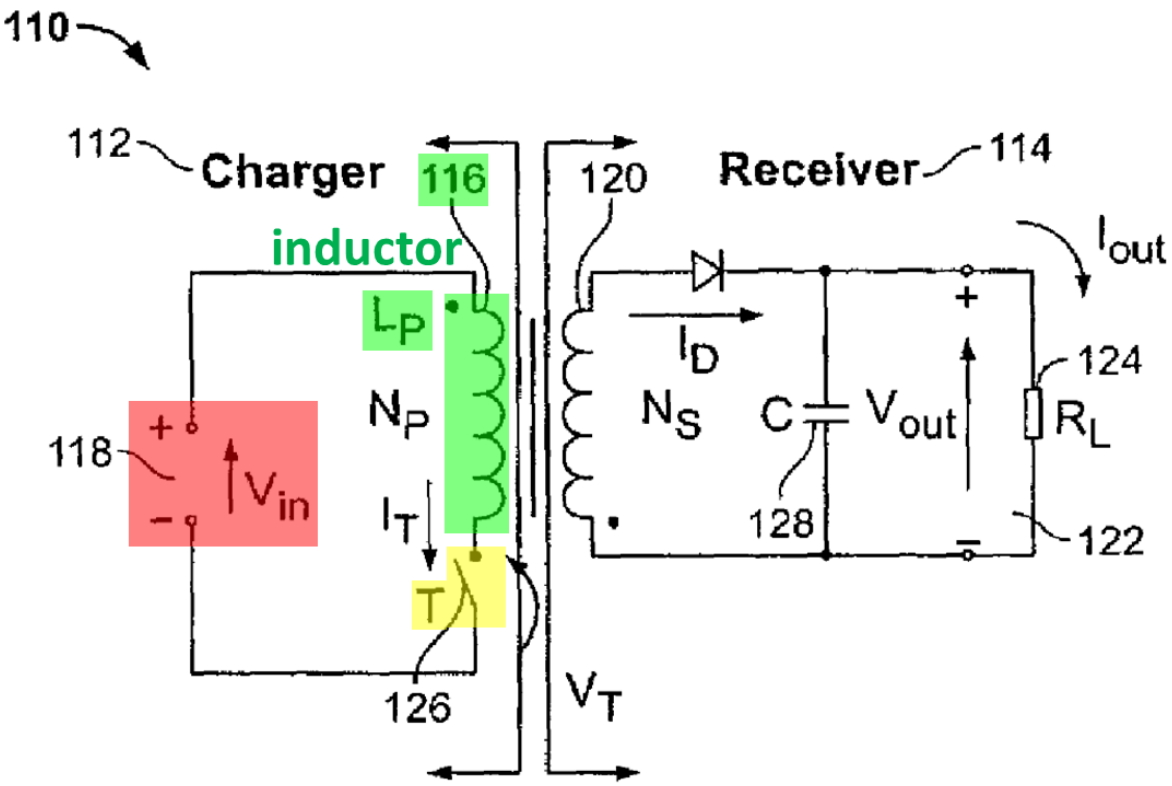


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶66.) A POSITA would have understood that an alternating current is a current whose magnitude changes with time. (Ex. 1002, ¶66; Ex. 1010, at 25.)

Accordingly, Partovi discloses "when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated," because the magnitude of the current propagating through the primary coil changes, which will necessarily generate an inductance. (Ex. 1002, ¶67; *see* Ex. 1001, 1:54-64.)

(2) Partovi discloses "a change in at least one of a <u>frequency</u> . . . or a <u>waveform shape</u> of the propagated electrical current"

Partovi also discloses that "the **duty cycle** of the charger switching circuit or its **frequency can be changed**" to adjust the system's output voltage to accommodate different charging or powering requirements of devices receiving power from the primary coil 126. (Ex. 1009, ¶¶[0119] (emphasis added).) That is, Partovi discloses changing the duty cycle or switching frequency of switch 126, which would in turn change the frequency and waveform shape of the current through the primary coil 126. (Ex. 1002, ¶68; *see also* Ex. 1009, ¶¶[0130], [0237], [0246], [258]-[259], [263].)

Accordingly, Partovi discloses "when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated," because the frequency or waveform shape of the current propagating through the primary coil changes, which will necessarily generate an inductance. (Ex. 1002, ¶69; *see* Ex. 1001, 1:54-64.)

2. Claim 2

a) The inductor of claim 1 wherein an electromotive force is generated when at least one of the frequency, the magnitude, or the waveform shape of the propagated electrical current is changed.

Partovi discloses or suggests this limitation. The claimed feature is merely an inherent property of an inductor, as admitted in the '960 patent, where a change in the current flowing through the inductor results in the generation of an EMF (electromotive force) across the inductor that opposes this change in current. (Ex. 1002, ¶70; Ex. 1001, 1:54-64, 14:17-27.) Therefore, because Partovi's primary coil 116 is an inductor, an electromotive force will necessarily be generated when there is change in "at least one of the frequency, the magnitude, or the waveform shape" of an electrical current flowing through the primary coil 116 (and therefore, through the "first conductor layer"). (Ex. 1002, ¶70.)

Furthermore, as discussed above in Section IX.A.1(f), Partovi discloses changing the magnitude, waveform shape, and frequency of the current through the primary coil 116 to generate an inductance. (*See supra* Section IX.A.1(f).) Given that inductance is simply a measure of EMF generated in response to a change in current per unit time, "electromotive force" is necessarily generated in the primary coil 116 when the above current passes through it. (Ex. 1002, ¶71; *see also* Ex. 1006, 601; Ex. 1010, at 517.) Indeed, as admitted in the '960 patent, generation of an electromotive force is an inherent property of an inductor when a change in at

least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs. (Ex. 1001, 1:54-64; Ex. 1002, ¶71.)

3. Claim 3

a) The inductor of claim 2 wherein a magnitude of the magnetic flux is proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶72.) As admitted by the '960 patent, the claimed limitation is an inherent property of an inductor. (Ex. 1001, 1:54-64 (emphases added); Ex. 1002, ¶72.) Thus, because Partovi discloses changing a frequency, magnitude, or the waveform shape of the current propagating through the primary coil (*supra* Section IX.A.1(f)), Partovi necessarily discloses "a magnitude of the magnetic flux is proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current." (*See supra* Section IX.A.1(f); Ex. 1002, ¶72; Ex. 1006, 592-593, 601.)

4. Claim 4

a) The inductor of claim 1 wherein, an electrical resistance of at least one of the first conductor layer is reducable when a cross-sectional area of a conducting skin depth within at least the first conductor layer is increased.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶73-77.) A POSITA would have understood that the claimed "conducting skin depth," as admitted by the '960 patent, is an inherent material property, which defines a depth below a conductor's surface where most of the current flows. (Ex. 1002, ¶73; *see also id.*, ¶¶26-29.) As explained below, a POSITA would have understood that as the conducting skin depth of a conductor (e.g., the top most layer 357 in figure 18 of Partovi, i.e., "first conductor layer") increases, cross-sectional area of the conducting skin depth of a conductor also increases, leading to a reduction of electrical resistance of the conductor. (Ex. 1002, ¶73.) As such, Partovi discloses "an electrical resistance of at least one of the first conductor layer is reducable when a cross-sectional area of a conducting skin depth within at least the first conductor layer is increased." (*Id.*)

When a high frequency current flows through a conductor, the current flow does not enter the core interior of the conductor as the current is substantially confined to a cross-sectional area that is defined by the skin depth at a given frequency near the surface of the conductor, thereby reducing the effective conductivity (or increasing the effective resistance) of the conductor. (Ex. 1002, ¶74; Ex. 1012 at ¶[0172]; Ex. 1015 at 16; Ex. 1017 at 1:11-21.)

Conversely, as the frequency reduces, the skin depth increases, and so does the cross-sectional area available for current flow, thereby increasing the effective

conductivity (or reducing the effective resistance) of the conductor. (Ex. 1002, ¶75.)

The skin depth effect occurs in conductive mediums, such as layers 357 of Partovi's the multi-layer inductor (which includes the "first conductor layer"), which can be made of copper. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1016 at 1:11-18; Ex. 1017 at 7:5-10, 8:12-28; Ex. 1002, ¶76.) Accordingly, a POSITA would have understood that when the frequency increases, the electrical resistance of layers 357 of Partovi's multi-layer inductor (including the "first conductor layer") increases as the cross-sectional area of a conducting skin depth of the inductor decrease. (Ex. 1002, ¶76.) Similarly, a POSITA would have also understood that when the frequency decreases, the electrical resistance of layers 357 decreases as the cross-sectional area of a conducting skin depth of the inductor increases. (*Id.*) Accordingly, Partovi discloses claim 4. (*Id.*, ¶¶76-77 (explaining that Partovi discloses reducing the frequency).)

5. Claim 10

a) The inductor of claim 1 wherein a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶78.) As discussed above in Section IX.A.4(a), a skin depth for a conductor is determined based on the frequency of the current propagating through the conductor, and intrinsic

properties of the conductor, including conductivity and permeability. (*See supra* Section IX.A.4(a).) At least because Partovi discloses that layers 357 (including "the first conductor layer" and "the second conductor layer") "can be made of copper material," Partovi discloses that these layers are made of the same material and thus the layers necessarily share the same conductivity and permeability. (Ex. 1009, ¶[0225]; *see also id.*, ¶[0248]; Ex. 1002, ¶78.) Furthermore, because layers 357 belong to the same primary coil 116, they are subject to the same current and frequency thereof. (Ex. 1002, ¶78.) Accordingly, each of layers 357 of Partovi's inductor has about the same skin depth because they have the same current, frequency, conductivity, and permeability. (*Id.*) Thus, Partovi discloses or suggests "a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer." (*Id.*)

6. Claim 15

a) The inductor of claim 1 wherein the frequency is at least 3 kHz.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶79.) For example, Partovi discloses that its inductive power transfer system operates at 1.3 MHz. (Ex. 1009, ¶[0177].) Indeed, a POSITA would have been motivated to ensure the operating frequency is above 1 MHz because it improves efficiency. (Ex. 1009, ¶[0248] ("Switching of these coils at high frequency (~1 MHz depending on the coil geometry and size) can transfer power across an air or material gap and an

efficient power supply with a very small transformer can be developed."); *see also id.*, ¶[166] ("By increasing the frequency to several or tens of MHz, one can obtain a working distance of several inches or feet depending on the application for the technology."), ¶[265], ¶[290]; Ex. 1002, ¶79.) A POSITA would have understood that the 1.3 MHZ frequency corresponds to the frequency of the transistor T in figure 2 of Partovi. (Ex. 1002, ¶79; Ex. 1009, ¶¶[0117] ("switch T 126 . . . is switched at an appropriate frequency"), ¶¶[0263]-[0265] (explaining the changing of the frequency of the FET drive that drives switch Q1, which corresponds to switch 126 in figure 2 of Partovi).) The frequency at which the switching transistor 126 switches corresponds to the frequency of the current that propagates through primary coil 116. (*See supra* Section IX.A.1(f).)

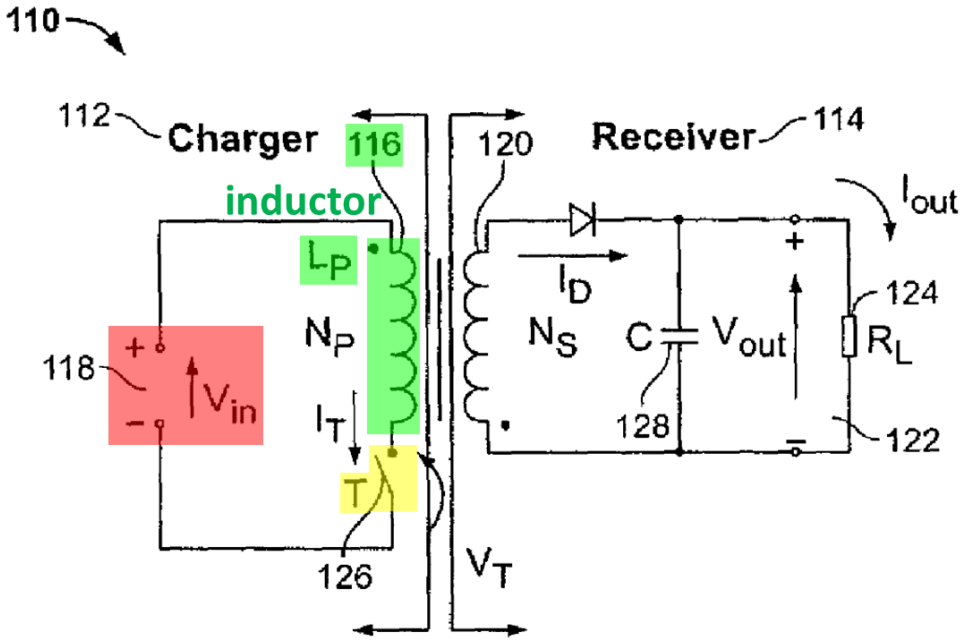


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶79.)

7. Claim 16

a) The inductor of claim 1 wherein at least one of the first and second conductor layers is formed from a thermally conductive material.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶80.) Partovi discloses that layers 357 (including "the first conductor layer" and "the second conductor layer") "can be made of copper material, which is thermally conductive, as a POSITA would have recognized. (*Id.*; Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1011 at ¶[0039] (describing copper as "thermally conductive material"); Ex. 1013 at 4:37-39 (disclosing copper as "having a high thermal conductivity").)

8. Claim 17

a) The inductor of claim 1 wherein the connector is selected from the group consisting of a via, a solder, a tab, a wire, a pin, a rivet, a filled mesh structure, a conductive polymer, a conductive composite, a conductive adhesive, a liquid metal, a foamed metal, and combinations thereof.

Partovi discloses this limitation. (Ex. 1002, ¶81.) For example, Partovi discloses that layers 357 of the multi-layer inductor are "connected . . . for example by use of a **via** or contacts." (Ex. 1009, ¶[0224] (emphasis added).)

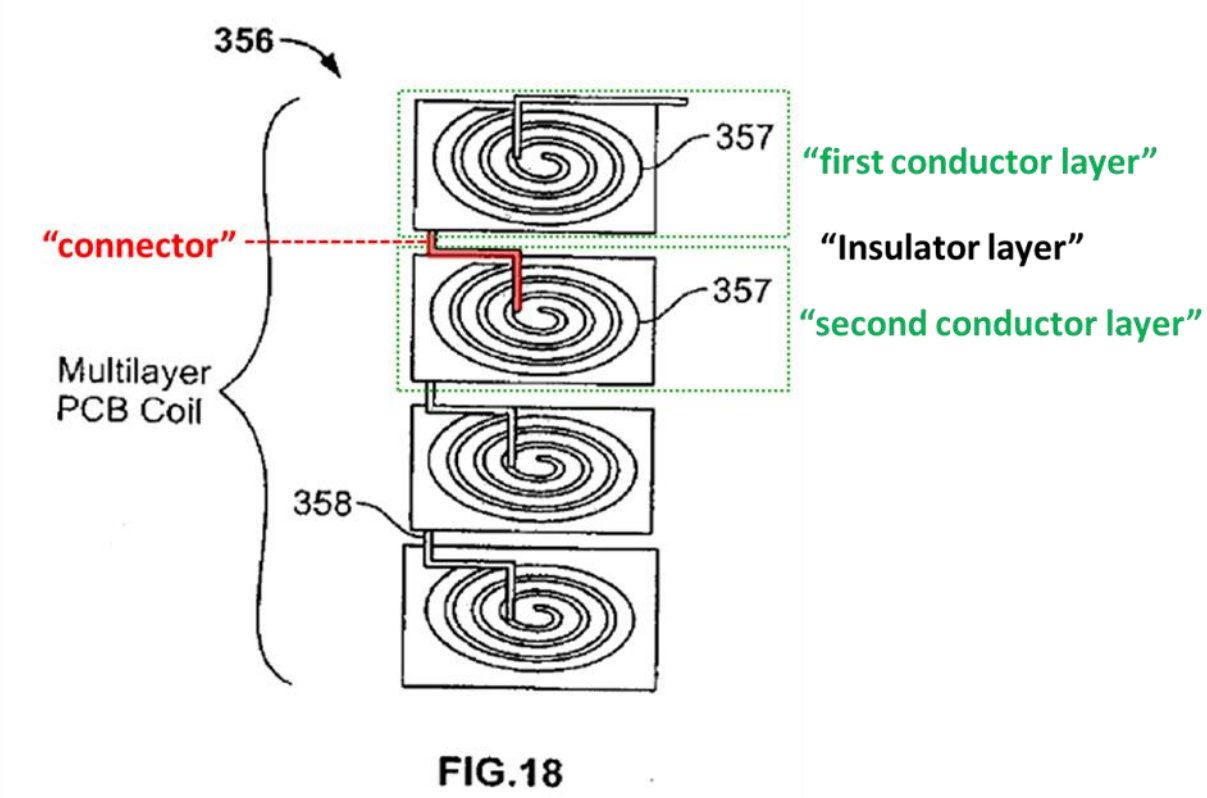


FIG.18

(*Id.*, FIG. 18 (annotated); Ex. 1002, ¶81.)

9. Claim 19

a) The inductor of claim 1 wherein the first conductor layer

and the second conductor layer form a structure in which the first and second conductor layers are positioned in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other.

Partovi discloses or suggests this limitation. (Ex. 1002 ¶¶82-83.) For example, Partovi discloses with reference to figure 18 that an inductor of high flux density is formed by stacking multiple coils in layers 357 (including "the first and second conductor layers") that are separate and spaced apart from each other. (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18.) Thus, a POSITA would have understood that layers 357 are positioned "in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other" because the conductors are in separate planes.

10. Claim 21

a) The inductor of claim 1 wherein the inductor is electrically connectable with an electrical circuit operating at about 100 kHz or greater.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶84-87.) As discussed above, the figure 2 circuit of Partovi includes a primary coil 116, which is an inductor. (*Supra* Section IX.A.1(preamble).) By switching switch 126 at a certain frequency, an alternating current flows through coil 116, which in turn generates an alternating magnetic field. (*Id.*; Ex. 1009, ¶¶[0117]-[0118]; *see also id.*, ¶¶[0013], [0091], [0119]; Ex. 1002, ¶84.)

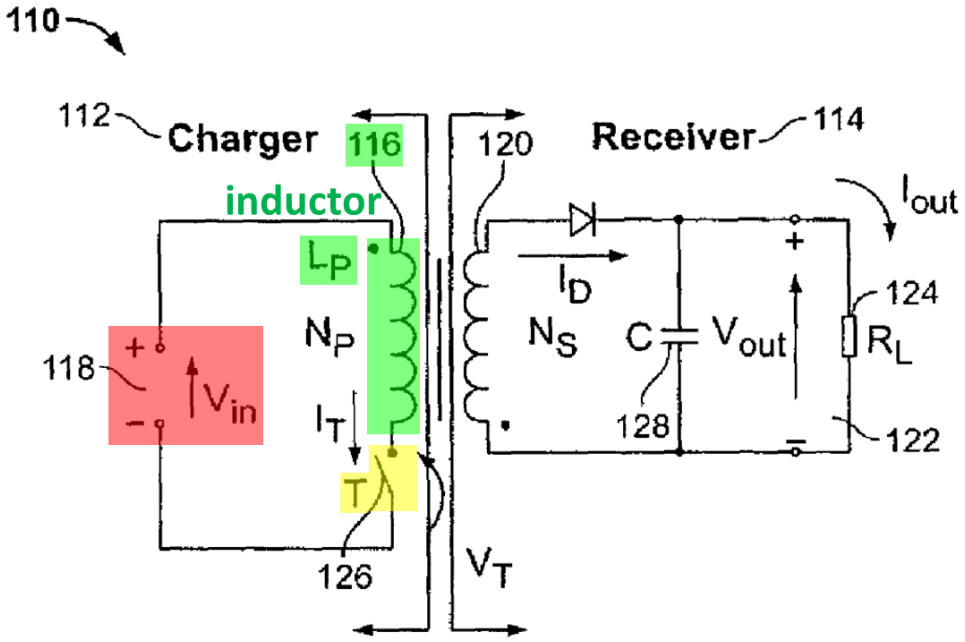


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶84.)

While Partovi discloses that switch 126 "can be a MOSFET or other switching mechanism" and that the duty cycle or frequency of the switch can be changed (Ex. 1009, ¶¶[0117], [0119]), figure 2 of Partovi does not explicitly disclose the circuitry that controls the switch 126 and changes its duty cycle or frequency. (Ex. 1002, ¶85.) But that is understandable because figure 2 of Partovi simply "shows the main components of a typical inductive power transfer system 110" and "[t]he circuit illustrated is used to illustrate the principle of inductive power transfer and is not meant to be limiting to an embodiment." (Ex. 1009, ¶[0117].) The description in Partovi following the discussion of figure 2 includes

various implementations of inductive power transfer systems that build on the principle of inductive power transfer illustrated with reference to figure 2 and disclose circuitry for controlling the switch. (*See, e.g.*, Ex. 1009, ¶¶[0177] (disclosing with reference to figure 10 that the switch is a field effect transistor (FET) driven by a driver circuit that is controlled by a micro control unit such that the "circuit in FIG. 2 . . . [is] tuned to operate a 1.3 MHz"), [0261] (disclosing with reference to figure 28 "a more sophisticated charger or power supply" that includes several components of the charger in figure 10 and allows the charger and the receiver to communicate wirelessly.)

In particular, figure 28 discloses one implementation of the inductive power transfer circuit of figure 2 where there is an inductive power transfer between the primary coil in the charger and the secondary coil in the receiver. (Ex. 1002, ¶86; Ex. 1009, ¶¶[0260], [0261].)

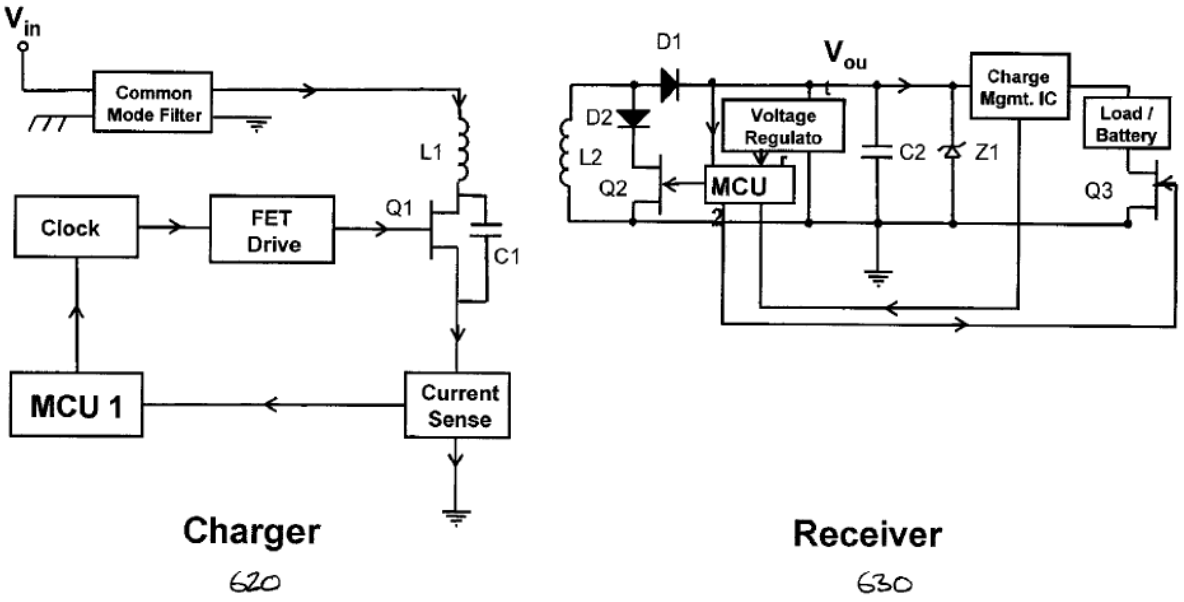
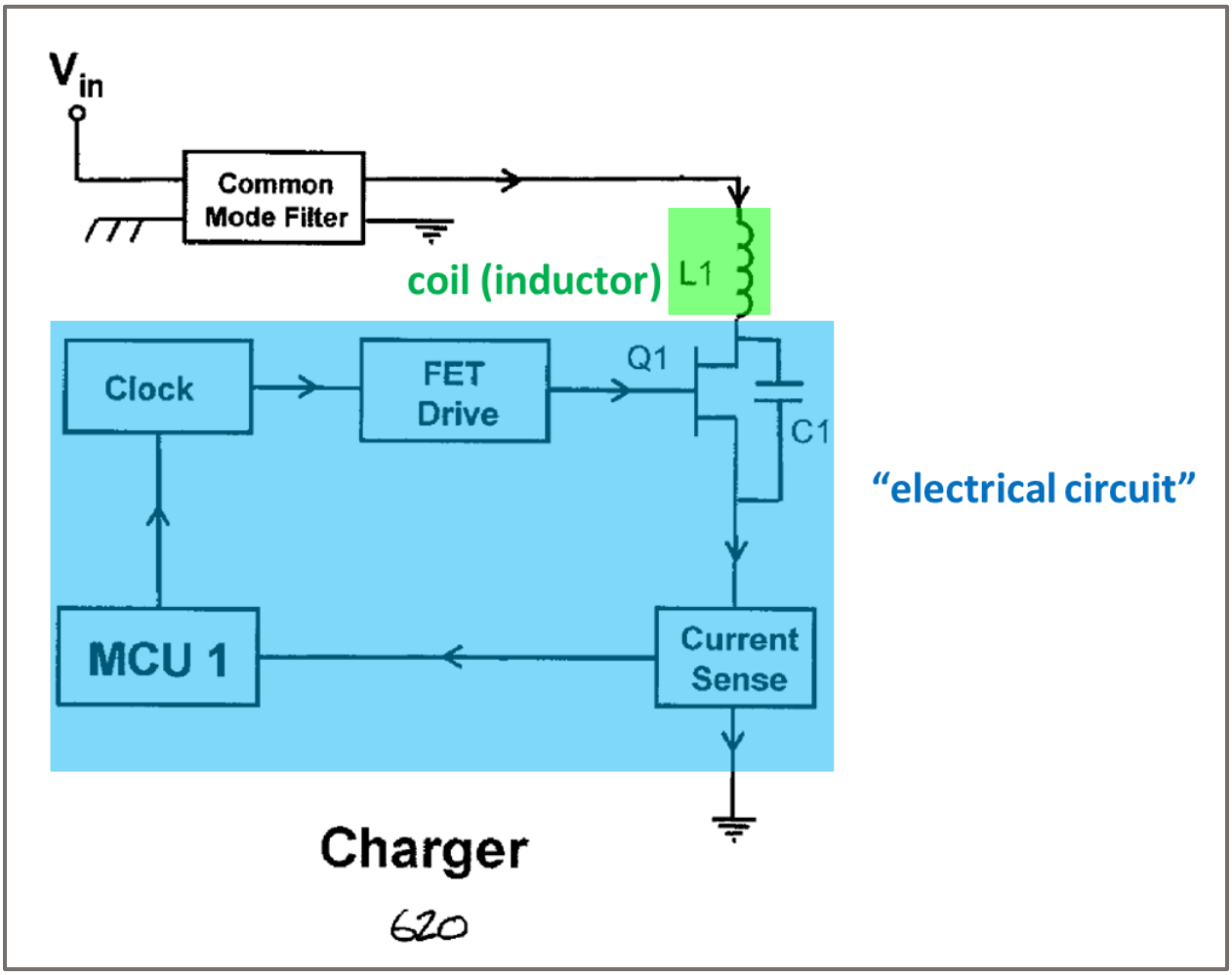


Figure 28

(Ex. 1009, FIG. 28.) A POSITA would have understood that coil L1 and FET Q1 correspond to the primary coil Lp 116 and switch 126, respectively, in figure 2 of Partovi. (Ex. 1002, ¶86; *see e.g.*, Ex. 1009, ¶[0117] (disclosing that switch 126 in figure 2 "can be a MOSFET or other switching mechanism").)

As shown below, the coil L1 ("inductor") is electrically connectable with an electrical circuit comprising FET Q1, capacitor C1, current sense circuit, MCU 1 (micro control unit), clock, and FET Drive circuit operating at 1.2-1.4 MHz ("electrical circuit operating at about 100 kHz or greater") where MCU1 controls the frequency of FET Q1 by controlling the clock to FET drive. (Ex. 1009, FIG 28, ¶¶[0263]-[0265].) This is consistent with Partovi's earlier disclosure that the "circuit in FIG. 2 . . . [is] tuned to operate a 1.3 MHz." (*Id.*, ¶[0177].)

Furthermore, Partovi discloses that MCU1 receives signals from a Current Sensor that is connected "in series with the coil" ("inductor"). (*Id.*; *see also id.*, ¶¶[0261]-[0270] (disclosing with reference to figure 28 a circuit for controlling output power of the charger).)



(Ex. 1009, FIG. 28 (annotated); Ex. 1002, ¶87.) Accordingly, Partovi discloses or suggests "the inductor is electrically connectable with an electrical circuit operating at about 100 kHz or greater." (Ex. 1002, ¶87.)

11. Claim 22

a) The inductor of claim 21 wherein the electrical circuit is selected from the group consisting of a mixer circuit, an impedance matching circuit, an upconverting mixer circuit, a downconverting mixer circuit, a modulator, a demodulator, a synthesizing circuit, a PLL synthesizing circuit, an amplifying circuit, an electrical driver circuit, an electrical detecting circuit, an RF log detector, an RF RMS detector, an electrical transceiver, a power controller, and combinations thereof.

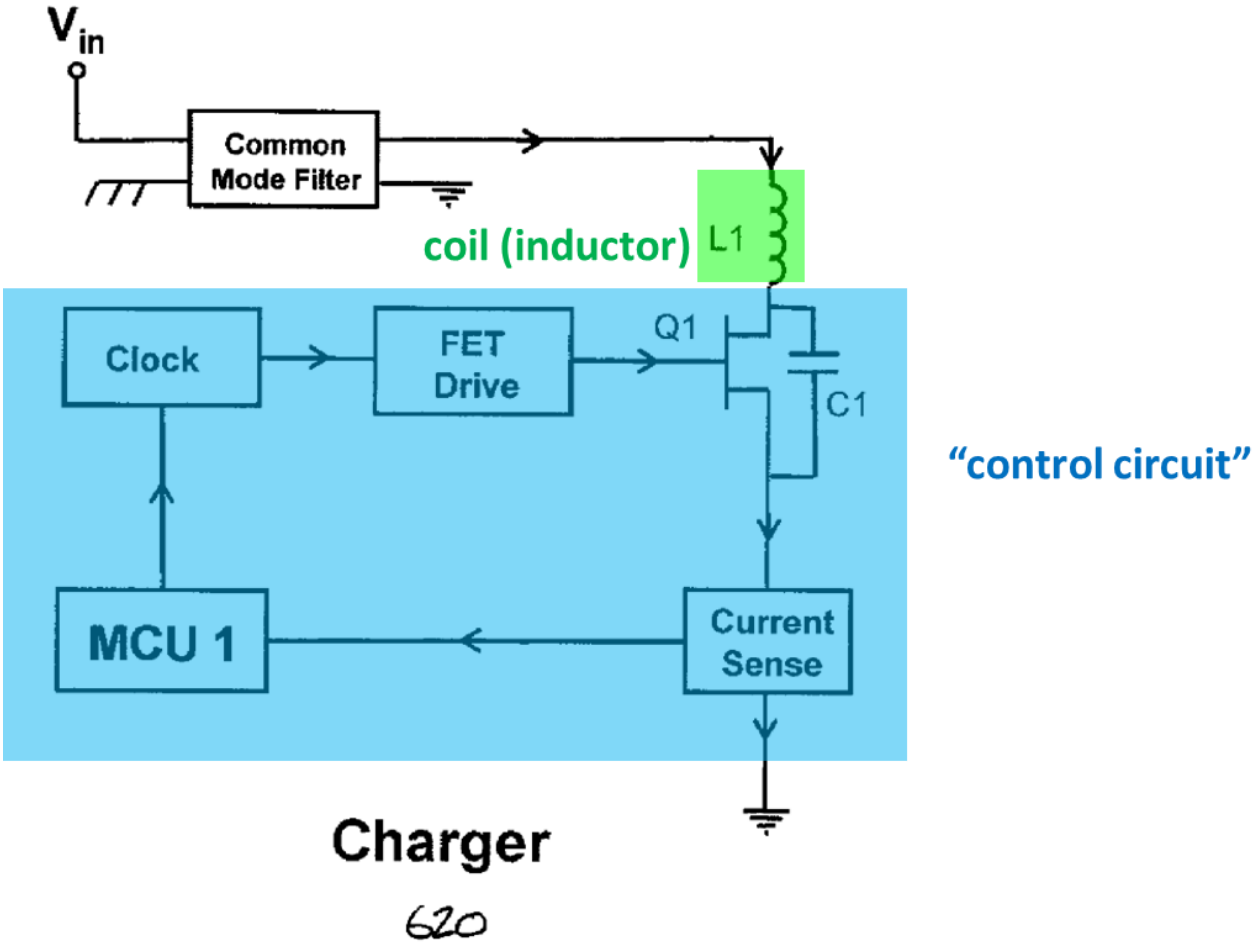
Partovi discloses or suggests this limitation. (Ex. 1002, ¶88.) For example, as discussed above for claim 21, the electrical circuit includes a FET drive ("electrical driver circuit") driving FET switch Q1, a current sense circuit ("electrical detecting circuit"), and a controller being a combination of MCU 1 and clock ("power controller"). (*See supra* Section IX.A.11; Ex. 1009, ¶¶[0261]-[0265].)

12. Claim 24

a) The inductor of claim 1 wherein a control circuit is electrically connectable to the inductor.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶89.) As discussed above, figure 28 discloses a particular implementation of the circuit of figure 2 of Partovi. (*Supra* Section IX.A.11 (analysis for claim 21).) Figure 28 discloses "a digital control scheme," where "[t]he primary (charger or power supply) 620 is controlled by a Micro Control Unit (MCU1)." (Ex. 1009, ¶[0261].) MCU1

receives signals from a Current Sensor that is connected "in series with the coil" ("inductor"). (*Id.*; *see also id.*, ¶¶[0261]-[0270] (disclosing with reference to figure 28 a circuit for controlling output power of the charger).) Accordingly, Partovi discloses or suggests "a control circuit is electrically connectable to the inductor." (Ex. 1002, ¶89.)



(Ex. 1009, FIG. 28 (excerpted and annotated); Ex. 1002, ¶89.)

13. Claim 25

a) The inductor of claim 1 wherein at least the first and

second conductor layers has at least a partial revolution.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶90.) For example, as shown in figure 18, Partovi discloses that each of the top two layers 357 ("the first and second conductors layers") of the multi-layer inductor has at least a partial revolution because they have at least three full turns. (Ex. 1009, FIG. 18; *see also id.*, ¶[0104], ¶¶[0212]-[0224].)

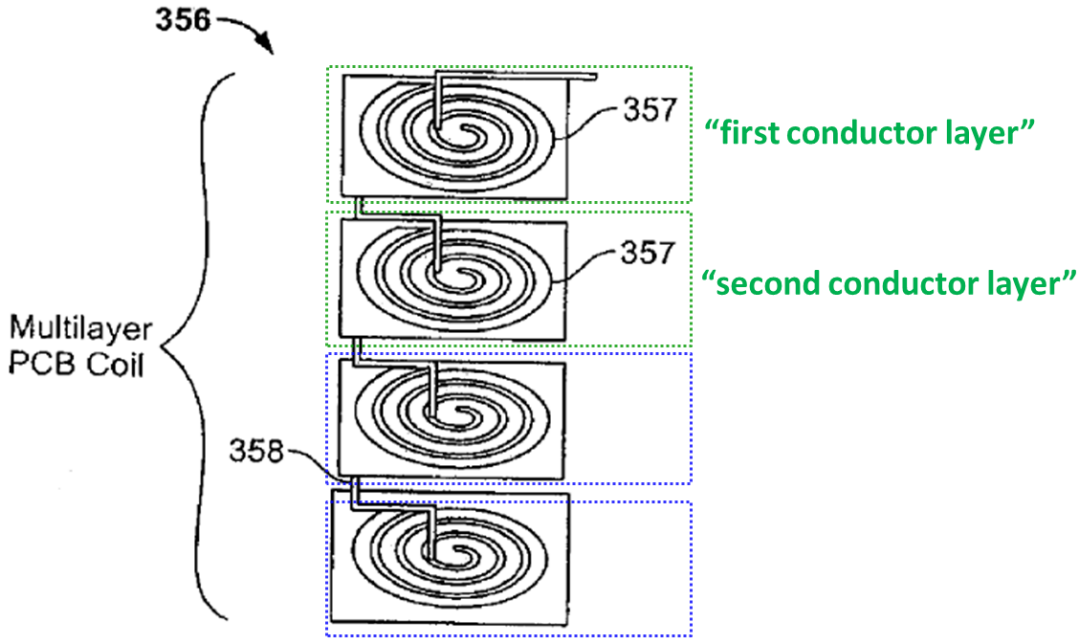


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶90.)

14. Claim 26

a) The inductor of claim 1 wherein the first conductor layer or the second conductor layer comprises a material selected from the group consisting of copper . . . .

Partovi discloses or suggests this limitation. (Ex. 1002, ¶91.) For example, Partovi discloses that layers 357 (including "first conductor layer" and "second conductor layer") "can be made of copper material" formed on PCB layers. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248].)

15. Claim 27

a) The inductor of claim 1 wherein at least one insulator layer is formed from an electrically insulative material.

Partovi discloses or suggests this limitation. (Ex. 1002, ¶92.) As discussed above, Partovi discloses an insulating layer between the PCB layers 357 that electrically insulates two PCB layers 357 from each other. (*Supra* Section IX.A.1(c).) Therefore, Partovi discloses that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex. 1002, ¶92; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

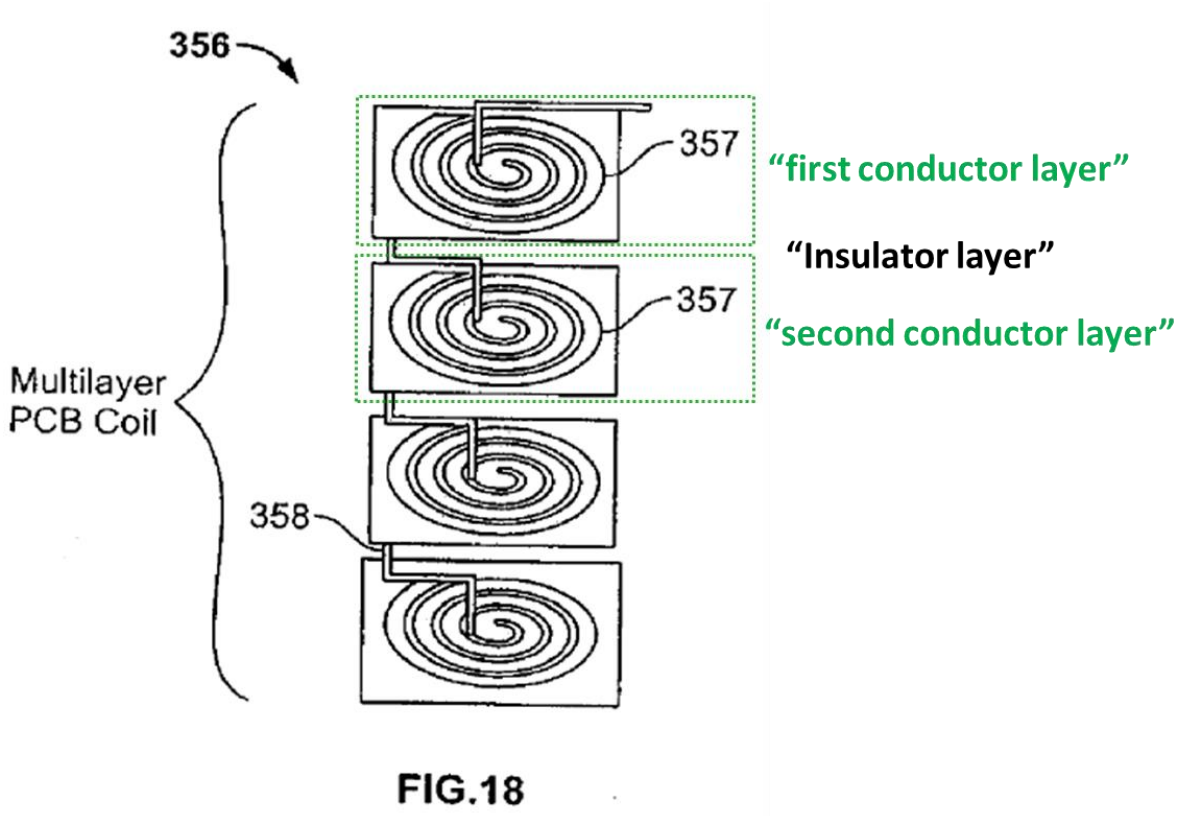


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶92.)

B. Ground 2: Partovi in View of Tseng Renders Obvious Claims 5-7 and 13

1. Claim 5

a) The inductor of claim 1 wherein a thickness of at least the first conductor layer is about equal to or greater than a thickness of a skin depth of the first conductor layer at a given frequency.

Partovi in view of Tseng discloses this limitation. (Ex. 1002, ¶¶93-98.) Partovi does not explicitly disclose that a thickness of the PCB layer 357 is "about equal to or greater than a thickness of a skin depth of the" PCB layer 357 at a given frequency. (*Id.*, ¶94.) But Tseng discloses such a feature and it would have been

obvious to implement PCB layer 357 in Partovi such that its thickness is at least two times the skin depth at a given frequency ("about equal to or greater than a thickness of a skin depth"). (*Id.*)

Similar to Partovi, Tseng generally discloses inductive power transfer system using coil inductors. (Ex. 1022 at Abstract (disclosing "a method and system for transferring power wirelessly to electronic devices," which "utilize magnetic coupling between two coils at close proximity to transfer sufficient power to charge an electronic device").) Indeed, just like Partovi, Tseng utilizes coil inductors formed on PCBs (*id.*, 5:37-40 (using "multiple layers of coils for generation of magnetic fields") and aims to improve efficiency of power transfer (*id.*, 10:48-51 (disclosing adjusting "the switching frequency in order to maximize the efficiency of power transfer"), 11:8-14 (disclosing "the efficiency of power transfer degrades due to various losses . . . include the conductor loss in coils"); Ex. 1002, ¶95.)

Tseng further discloses that, to reduce power loss in coils due to skin depth effect, "the metal thickness should be more than twice of the skin depth." (Ex. 1022 at 12:3-5; *see also id.*, 12:6-8, 11:66-12:14.) As such, when implementing the multi-layer PCB coil 356 in Partovi for primary coil 116, a POSITA would have found it obvious to ensure that the thickness of each of the PCB layers 357 is at least twice the skin depth at the system's operating frequency in order to

minimize conductor loss in these layers. (Ex. 1002, ¶¶96; *see also* Ex. 1024 at 1:34-38 (disclosing that "it has become commonplace to use a planar conductive film having a thickness on the order of **twice the skin depth** at the intended operating frequency as the magnetic components conductors.") (emphasis added).) *See Unwired Planet*, 841 F.3d at 1003.

A POSITA would have been able to make the necessary changes to the thickness of the PCB layers 357 making up the primary coil 116 based on the operating frequency. (Ex. 1002, ¶97.) For example, Partovi discloses that different sizes of copper, such as from 1 to 6 oz. (corresponding to thicknesses of from 1.4 to 8.2 mil), can be used to optimize the inductive circuit for a particular application. (Ex. 1009, ¶[0167], ¶[0212].) A POSITA would have understood that implementing the claimed feature would have involved no more than applying a known technique to a known device to yield a predictable result (e.g., designing and implementing a conductor based on the skin depth at a certain operating frequency). (Ex. 1002, ¶98.) *See KSR*, 550 U.S. at 416.

2. Claim 6

a) The inductor of claim 1 wherein a thickness of the first conductor layer ranges from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency.

Partovi in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶99.) For example, the Partovi-Tseng combination discloses or suggests

implementing PCB layers 357 in Partovi such that the thickness of the layers 357 (including "first conductor layer") is about twice of the skin depth at a given frequency. (*See supra* Section IX.B.1 (analysis for claim 5).)

3. Claim 7

a) The inductor of claim 1 wherein a thickness of the second conductor layer ranges from about 1.25 times to about 4 times a thickness of a skin depth of the second conductor layer at a given frequency.

Partovi in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶100.) For example, the Partovi-Tseng combination discloses or suggests implementing PCB layers 357 in Partovi such that the thickness of the layers 357 (including "second conductor layer") is about twice of the skin depth at a given frequency. (*See supra* Sections IX.B.1 (analysis for claim 5), IX.A.1(b) (one of PCB layers 357 is a "second conductor layer.")

4. Claim 13

a) The inductor of claim 1 wherein the inductor has an inductor quality factor greater than about 5.

Partovi in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶¶101-105.) As discussed above, Partovi discloses a primary coil 116, which is an "inductor." (*Supra* Section IX.A.1(a).) But Partovi does not disclose the inductor quality factor for primary coil 116. (Ex. 1002, ¶101.) However, as discussed

below, it would have been obvious to configure primary coil 116 such that it has an inductor quality factor greater than 5. (*Id.*)

As discussed above with respect to claim 5, a POSITA would have been motivated to combine teachings of Partovi and Tseng to reduce power loss in the primary coil 116 by ensuring that the thickness of the PCB layers forming the coil is at least twice the skin depth at the system's operating frequency. (*See supra* Section IX.B.1(a) (claim 5).) Tseng further discloses a high Q value of about 100 by optimizing the spacing between the conductive traces of an inductor. (Ex. 1022 at FIG. 24, 8:1-18; Ex. 1002, ¶102.)

Based on the combined teachings of Partovi and Tseng, a POSITA would have had reasons to consider the teachings of Tseng when contemplating the features disclosed by Partovi. (Ex. 1002, ¶103.) And, based on those disclosures, such a skilled person in the art would have found it obvious to optimize Partovi's inductor to improve its Q factor, i.e., improving efficiency or reducing power loss, in view of Tseng. (*Id.*) *See KSR*, 550 U.S. at 416.

For example, when implementing Partovi's inductor, a POSITA would have been motivated to find ways to improve the efficiency of the inductor and Tseng discloses at least a way to do so by optimizing the spaces between conductive traces of an inductor. (Ex. 1002, ¶104.) Indeed, by increasing the width of the traces (i.e., narrowing the spaces among them), Tseng shows that the inductor's

"coupling efficiency" is improved and the Q value improves from 50 to 100. (*Id.*; Ex. 1022 at FIG. 24, 8:1-18.) Furthermore, a POSITA would not have been deterred from optimizing Partovi's inductor in view of Tseng's teachings. (Ex. 1002, ¶104.) For example, Partovi discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and **coupling efficiency** for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212] (emphasis added); Ex. 1002, ¶104.)

Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil and/or circuits and to combine the same. (Ex. 1002, ¶105.) In fact, the '960 patent admits that multi-layer inductors "can be relatively easily achieved by existing manufacturing techniques (for example multi-layer printed wiring board, FIG. 21), and can therefore be integrated with other circuit components such as ICs, resistors, capacitors, surface mount components, etc." (Ex. 1001, 31:37-42; Ex. 1002, ¶105.)

C. Ground 3: Partovi in View of Chiang Renders Obvious Claims 1-4, 10, 15-22, 24-27, 29, and 30

1. Claim 1

As discussed above in Section IX.A.1, Partovi discloses or suggests all of the limitations of claim 1. With respect to claim element 1(c), Partovi discloses "an insulator layer" that is positioned in the space between all four layers 357,

including the space between the top two layers ("first conductor layer" and "second conductor layer"). (*Supra* Section IX.A.1(c).) To the extent that PO contends or the Board finds that the presence of such an "insulator layer" between the PCB layers 357 is not explicit or implied in Partovi, a POSITA would have been motivated to combine the teachings of Partovi with Chiang to provide an "insulator layer" between each of the PCB layers 357 to ensure they are electrically insulated from each other and therefore, capable of functioning in an expected manner. (Ex. 1002, ¶¶106-107.)

Like Partovi, Chiang discloses techniques for forming inductors using a multi-layer printed circuit board (PCB). (Ex. 1023 at 1:7-10, 4:67-5:9.) "An embodiment of an inductor according to the present invention formed on a six layer PCB and having two winding turns is shown in the exploded perspective view of FIG. 3 . . . ." (*Id.*, 6:19-23, FIG. 3.) Each of the six PCB layers (303) is separated from the other by an insulating layer 301. (*Id.*, 6:23-7:4, FIG. 3.) The PCB layers are connected with each other using "plated through holes" that are formed using "micro-**vias**." (*Id.* (emphasis added).) Therefore, as shown below, Chiang discloses "a first insulator layer" (e.g., insulating layer 301d) positioned in the space between a first conductor layer (303d) and a second conductor layer (303c).

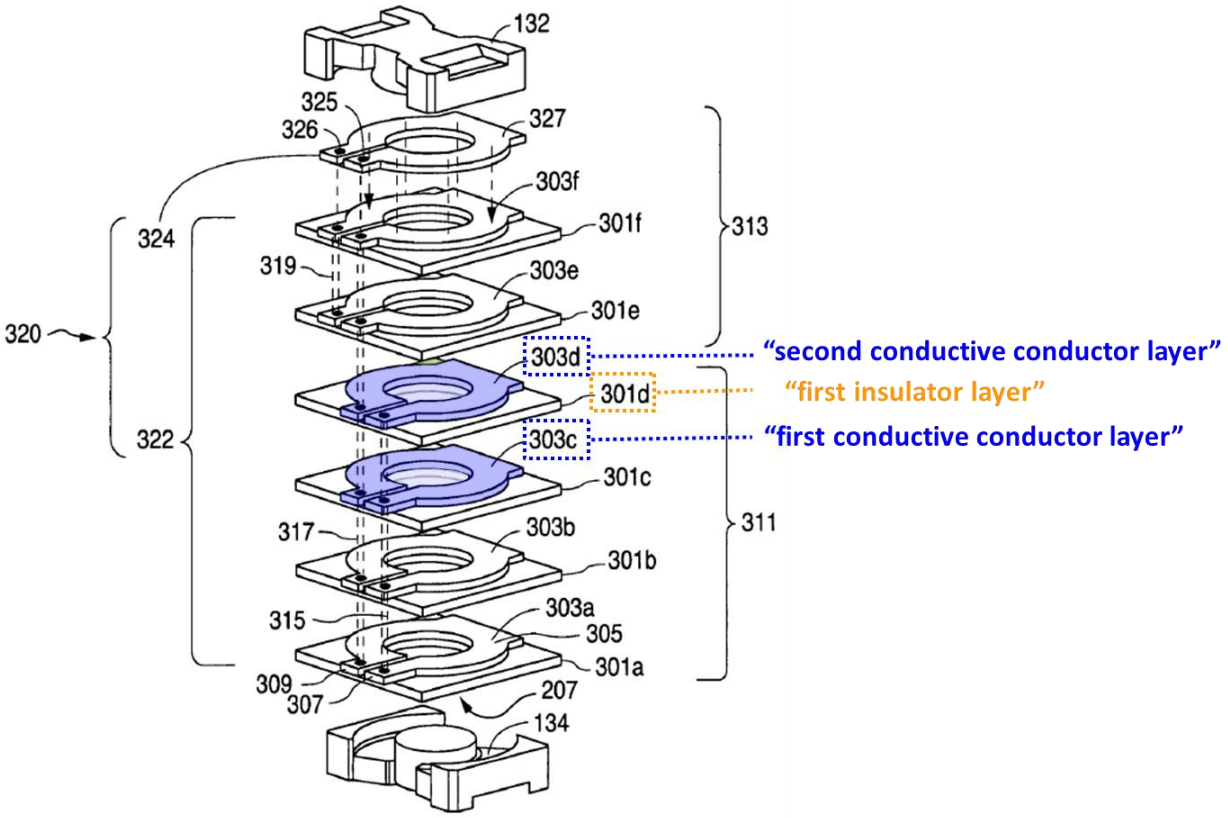


FIG. 3

(*Id.*, FIG. 3 (annotated); Ex. 1002, ¶108.)

Based on the combined teachings of Partovi and Chiang, a POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶109.) A POSITA seeking to implement Partovi would have looked to Chiang because both disclose PCB-based inductors. (*Id.*) Having looked to Chiang, a POSITA would have recognized that a typical multi-layer PCB includes conductor layers separated from each other by an insulating layer and would have therefore, combined the teachings of Partovi and

Chiang to include insulating layers between each of the PCB layers 357 in figure 18 of Partovi. (*Id.*) A POSITA would have been motivated to do so because such a configuration was typical for PCBs and required in order to ensure that adjacent PCB layers are not shorted. (*Id.*) If an insulating layer did not exist between two PCB layers then those two layers would be just one layer and not "separate[]" as disclosed by Partovi. (Ex. 1009, ¶[0224]; Ex. 1002, ¶109.) Indeed, using an insulating between two PCB layers 357 in figure 18 of Partovi would have been nothing more than the combination of familiar elements according to known techniques yielding the predictable result of a functional PCB-based inductor. (Ex. 1002, ¶109.) *KSR*, 550 U.S. at 416-21.

Partovi in combination with Chiang discloses or suggests the remaining limitations of claim 1 for the reasons discussed above for claim 1 with the only modification to the analysis for claim 1 being that discussed above. (*Supra* Section IX.A.1; Ex. 1002, ¶110.)

2. Claims 2-4, 10, 15-17, 19, 21, 22, and 24-27

Partovi in combination with Chiang discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.A.2-15; Ex. 1002, ¶111.) The same analysis presented above for these claims in Ground 1 is also applicable for the Partovi-Chiang combination discussed above in Section

IX.C.1. (Ex. 1002, ¶111.) The combination of Chiang with Partovi does not affect the analysis for these claims in Section IX.A.

3. Claim 27

Partovi in combination with Chiang discloses or suggests this limitation because as discussed above in Section IX.C.1, an insulating layer is included between each PCB layer 357 in the Partovi-Chiang combination. (Ex. 1002, ¶112.) An insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (*Id.*; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

4. Claim 29

Preamble An inductor comprising:

Partovi discloses this limitation, for at least the same reasons as presented above for preamble of claim 1. (*Supra* Section IX.A.1(preamble); Ex. 1002, ¶113; *see also infra* Sections IX.C.4(a)-(d) for the remaining elements of this claim.)

> **a)** a first inductor subassembly comprising: i) a first conductive conductor layer; ii) a second conductive conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive; ii) [sic] a first insulator layer positioned in the space between the first conductor layer and the second conductor layers, and iii) a first connector electrically connecting the first conductor layer and the second conductor layer in parallel;

Partovi in view of Chiang discloses or suggests this limitation. (Ex. 1002, ¶¶114-122.) Partovi discloses or suggest implementing the primary coil 116 ("inductor") in figure 2 using a multi-layer PCB coil (e.g., coil 356 in figure 18 of Partovi). (*Supra* Section IX.A.1(a).) Therefore, for reasons similar to those discussed above in Sections IX.A.1(a)-(d), Partovi discloses the claimed "first conductive conductor layer," "a second conductive conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive," "a first insulator layer positioned in the space between the first conductor layer and the second conductor layers," and a "first connector electrically connecting the first conductor layer and the second conductor layer . . . ." (*Supra* Sections IX.A.1(a)-(d); Ex. 1002, ¶114.) Accordingly, Partovi discloses a "first inductor subassembly" that includes the above components.

But Partovi does not explicitly disclose that the first connector electrically connects the PCB layers 357 ("first conductor layer" and "second conductor layer") *in parallel*, as required by claim 29. Nonetheless, a POSITA would have found it obvious to implement such a feature in view of Chiang and the knowledge of such a person. (Ex. 1002, ¶115.)

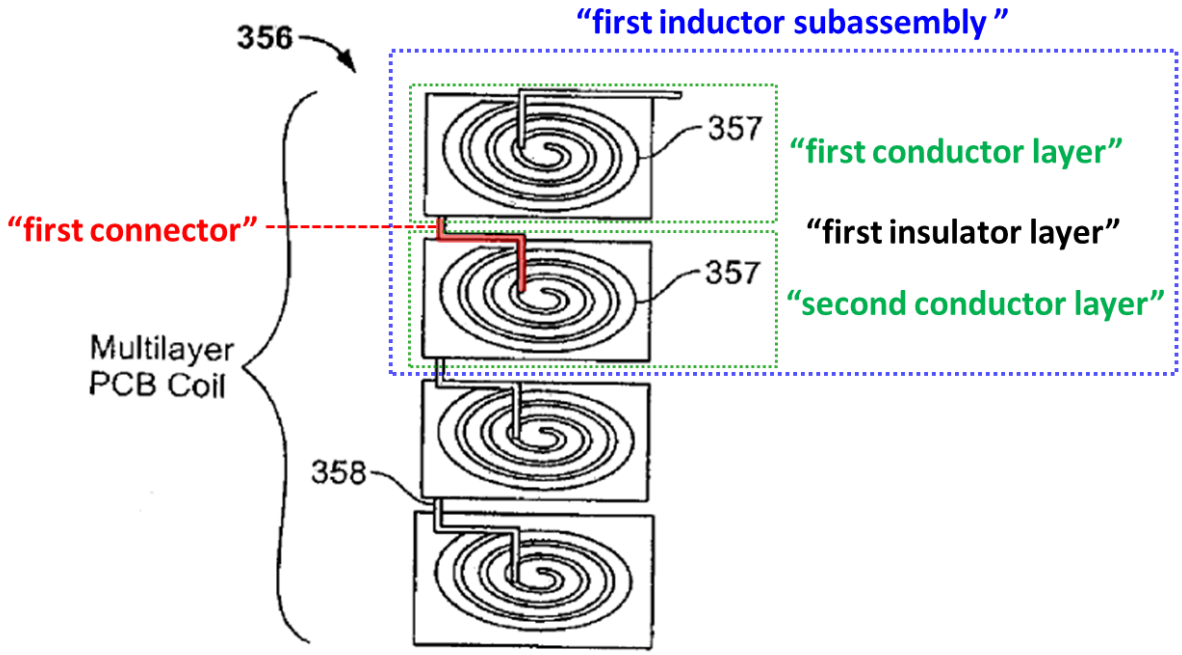


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶115.)

Like Partovi, Chiang discloses a multi-layer PCB inductor. (*See, e.g.*, Ex. 1023 at Title, Abstract, 1:7-10, 4:20-22, 4:62-5:4, 6:19-23, FIGs. 3-5.) For example, Chiang discloses with reference to figure 3 (below) a winding 320 that includes a multi-layer PCB 322, which includes a first turn 311 and a second turn 313, collectively formed by six conducting layers 303a-303f and six insulating layers 301a-303f. (*Id.*at 6:23-30.) The two ends (307 and 309) on conducting layer 303 are "interconnected through the insulating layers . . . by one or more plated through holes formed therein." (*Id.*, 6:37-40; *see also id.*, 6:30-37.) Chiang

additionally discloses that by adding conducting layer 324 to the multi-layer PCB 322 the winding 320 can accept an increased current flow. (*Id.*, 7:12-14.)

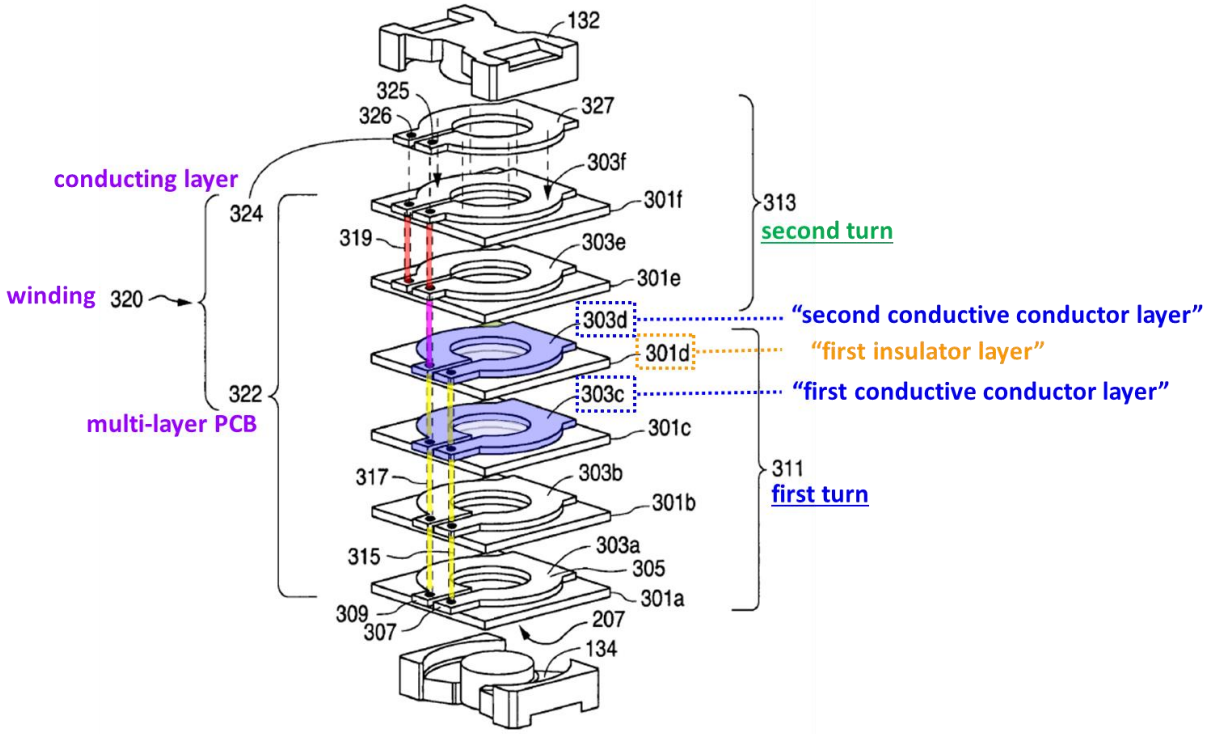


FIG. 3

(Ex. 1023 at FIG. 3 (annotated); Ex. 1002, ¶116.)

Accordingly, similar to Partovi, Chiang also discloses "a first conductive conductor layer" (conducting layer 303c), "a second conductive conductor layer" (conducting layer 303d) that is spaced apart from the first conductor layer, where "the first conductor layer and the second conductor layer being electrically conductive." (Ex. 1002, ¶117; Ex. 1023 at 1:43-46 (disclosing that "[i]n a multi-layer PCB, a PCB winding is formed from a plurality of patterned conductive

traces, typically of copper"), FIG. 4 (indicating the conducting layers 303 are made of copper), 6:51-7:4.) Chiang likewise discloses that "a first insulator layer" (insulating layer 301d) is positioned in the space between the first conductor layer and the second conductor layers. (*See e.g.*, Ex. 1023 at 6:51-7:4; Ex. 1002, ¶117.)

Furthermore, Chiang discloses that each of the conducting layers may be "**connected in parallel to decrease the impedance** of a particular turn of the winding." (Ex. 1023 at 1:62-64 (emphasis added).) For example, Chiang discloses that conducting layer 303c ("first conductive conductor layer") and conducting layer 303d ("second conductive conductor layer") are electrically connected in parallel by plated through holes 315 and 317 ("a first connector"). (*Id.*, 7:5-14; *see also id.*, 6:51-7:4.) Conducting layers 303c and 303d are also connected in parallel with conducting layers 303a and 303b, thereby forming a first turn 311 ("first subassembly") as shown in figure 5 below. (*Id.*, FIG. 5, 7:5-14; Ex. 1002, ¶118.)

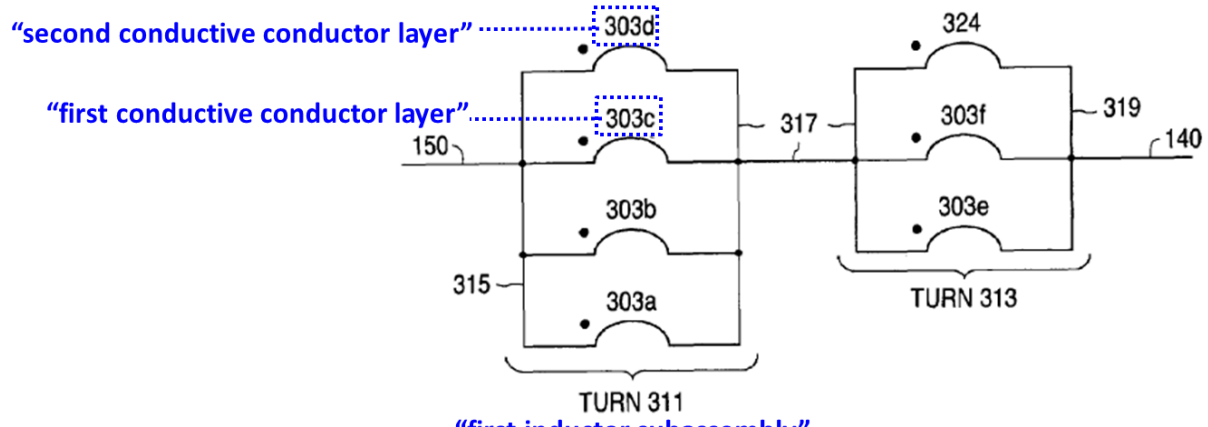


FIG. 5

(Ex. 1023 at FIG. 5 (annotated); Ex. 1002, ¶118.)

Based on the combined teachings of Partovi and Chiang, a POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶119.) A POSITA seeking to implement Partovi would have looked to Chiang because both disclose PCB-based inductors. (*Id*.) And, based on those disclosures, such a skilled person in the art would have found it obvious to modify the multi-layer coil 356 in figure 18 of Partovi such that the connector connects the PCB layers 357 (including the "first conductive conductor layer" and the "second conductive conductor layer") **in parallel**. (*Id.*) As discussed below, a POSITA would have been motivated to do so because it would have decreased the resistance of the coil, an objective of Partovi's. (*Id.*)

Partovi discloses that while multiple layers of PCB coils can be stacked for "compact fabrication" of high flux density coils (Ex. 1009, ¶[0212], FIG. 18), such a configuration has some drawbacks. (Ex. 1002, ¶120.) Notably, Partovi discloses that "[w]hile larger values [of inductance] can be obtained by increasing the number of turns or stacking a number of coils vertically and connecting them in series, this larger induction **comes at the price of increased resistance and therefore loss in the inductor**." (Ex. 1009, ¶[0255] (emphasis added).) Partovi notes that "for the power efficiency to be maximized and to minimize losses in the coil, the coils should be manufactured to have as low a resistance as possible."

(*Id.*, ¶[0167.) As such, a POSITA would have been motivated to utilize a parallel connection between the PCB layers 357 ("first conductor layer" and "second conductor layer") in Partovi because doing so would have improved the performance of the circuit by, e.g., **reducing resistance** and loss of the inductor. (Ex. 1002, ¶120; Ex. 1023 at 1:62-64; *see also* Ex. 1025 at ¶¶[0030] (explaining that forming an inductor using two conducting layers connected in parallel halves the resistance of the inductor by doubling the cross-sectional area of the inductor), [0036] (explaining that such an inductor may be formed by PCB laminations).) *See Unwired Planet*, 841 F.3d at 1003.

Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil and/or circuits and to combine the same. (*Id.*) In fact, the '960 patent admits that multi-layer inductors "can be relatively easily achieved by existing manufacturing techniques (for example multi-layer printed wiring board, FIG. 21), and can therefore be integrated with other circuit components such as ICs, resistors, capacitors, surface mount components, etc." (Ex. 1001, 31:37-42; Ex. 1002, ¶121.) Therefore, a POSITA would have understood and appreciated that the proposed Partovi-Chiang combination involved a combination of known prior art elements and technologies (e.g., the multi-layer inductor disclosed by Chiang that reduces resistance and the multi-layer inductor disclosed by Partovi that would benefit from a reduced resistance) according to known methods (e.g.,

connecting two conductive layers in an inductor using at least two connectors or vias as discussed by Chiang) to yield the predictable result of a circuit with an improved efficiency for having a reduced series resistance. (Ex. 1002, ¶120.) *See KSR*, 550 U.S. at 416.

Accordingly, the Partovi-Chiang combination discloses or suggests claim element 29[a]. (Ex. 1002, ¶121.)

> **b)** a second inductor subassembly comprising: i) a third conductor layer; ii) a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive; iii) a second insulator layer positioned in the space between the third conductor layer and the fourth conductor layers; and iv) a second connector electrically connects the third conductor layer and the fourth conductor layer in parallel or series, wherein the first inductor subassembly is electrically connected in series or parallel to the second inductor subassembly; and

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶123-132.) For example, as shown in figure 18 below, Partovi discloses that the multi-layer PCB coil 356 includes two additional layers 357 ("third conductor layer" and "fourth conductor layer") below the disclosed "first conductor layer" and the "second conductor layer." (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18; Ex. 1002, ¶123.)

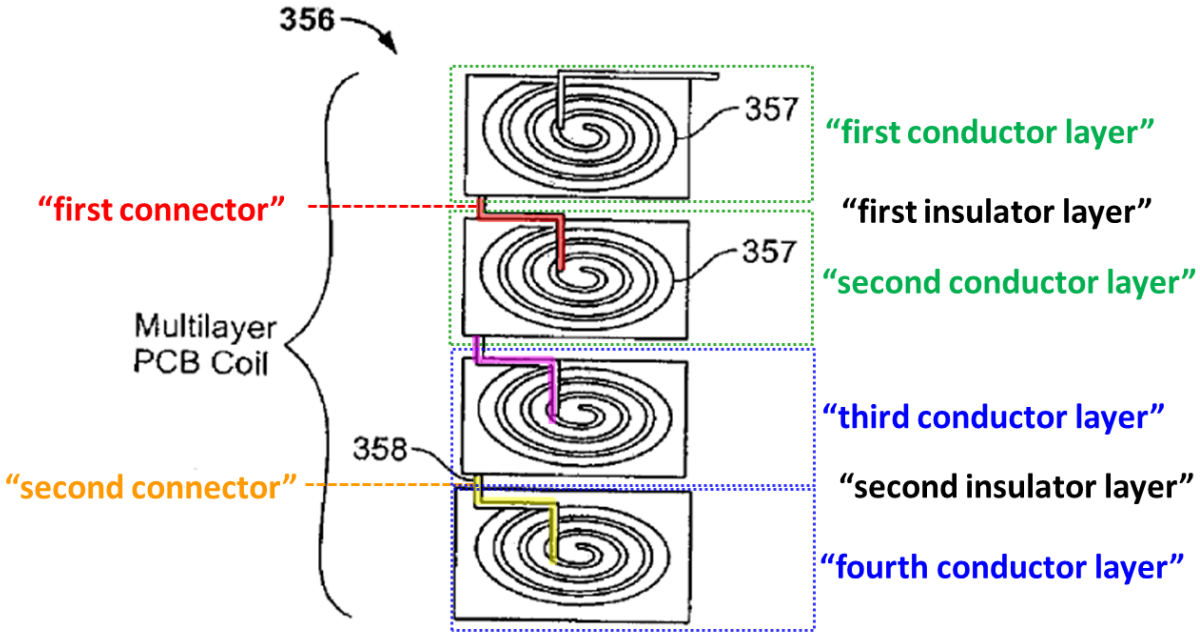


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶123.) Moreover, for reasons similar to those discussed above with respect to claim 1(b), Partovi discloses the claimed "a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive." (*Supra* Sections IX.A.1(b).) Partovi further discloses "a second insulator layer positioned in the space between the third conductor layer and the fourth conductor layers" for the same reasons that Partovi discloses a "first insulator layer" in the space between the first and second conductor layers. (*Supra* Section IX.A.1(c).)

Additionally, Partovi in view of Chiang discloses "a second connector electrically connects the third conductor layer and the fourth conductor layer in parallel or series." (Ex. 1002, ¶124.) As shown above, the bottom two PCB layers

in Partovi's PCB coil 356 ("third conductor layer" and "fourth conductor four") are electrically connected by a connector 358. (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18; Ex. 1002, ¶124.)

Partovi, however, does not explicitly disclose that the connector 358 connects the third and fourth conductor layers *in parallel or series*. (Ex. 1002, ¶125.) Chiang, however, discloses a third and a fourth conductor layer that are connected *in parallel*. (*Id.*) For example, as shown in figure 3 below, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023 at FIG. 3, 7:5-14; *see also id.*, FIG. 5.)

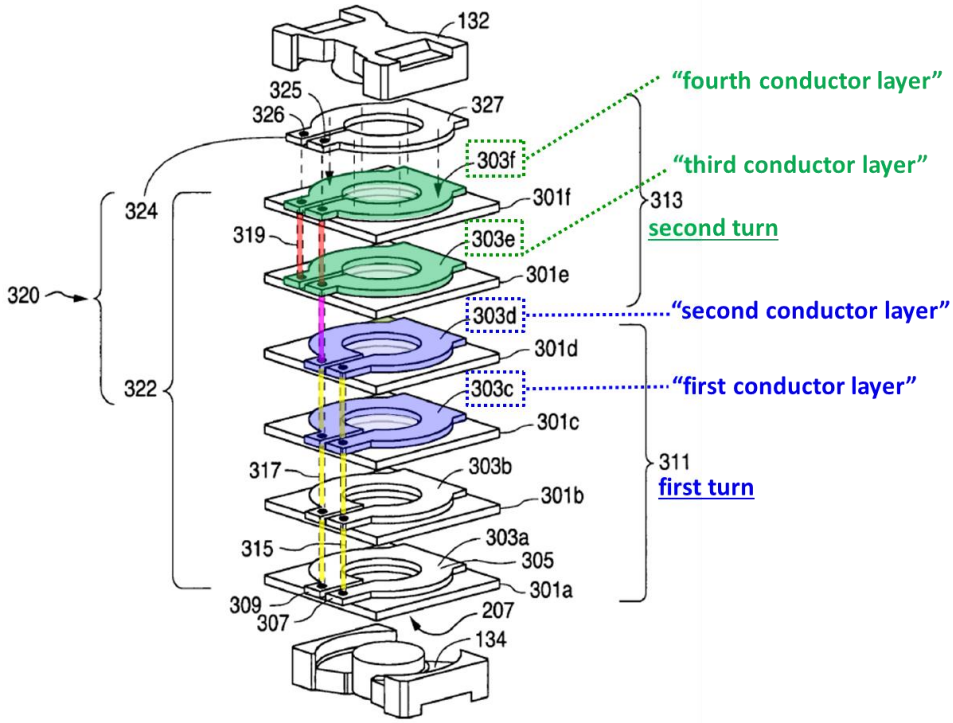


FIG. 3

(Ex. 1023 at FIG. 3 (annotated); Ex. 1002, ¶125.) Therefore, Chiang discloses "a third conductor layer and a fourth conductor layer electrically connected in *parallel* or series" (emphasis added). (Ex. 1002, ¶125.)

As discussed above in Section IX.C.4(a) (claim element 29(a)), a POSITA would have been motivated to connect two PCB layers 357 (e.g., "first conductor layer" and "second conductor layer") in parallel to reduce series resistance of the inductor in view of the disclosure of Chiang, e.g., figure 3, reproduced above. (*See above* Section IX.C.4(a).) For similar reasons, a POSITA would have found it obvious to connect the bottom two PCB layers 357 (corresponding to "third

conductor layer" and "fourth conductor layer") in figure 18 of Partovi in parallel. (*Id.*; Ex. 1002, ¶126.)

Accordingly, the Partovi-Chiang combination discloses or suggests "a second connector electrically connects the third conductor layer and the fourth conductor layer *in parallel* or series." (*Id.* (emphases added).) The Partovi-Chiang combination thus far may be illustrated as follows:

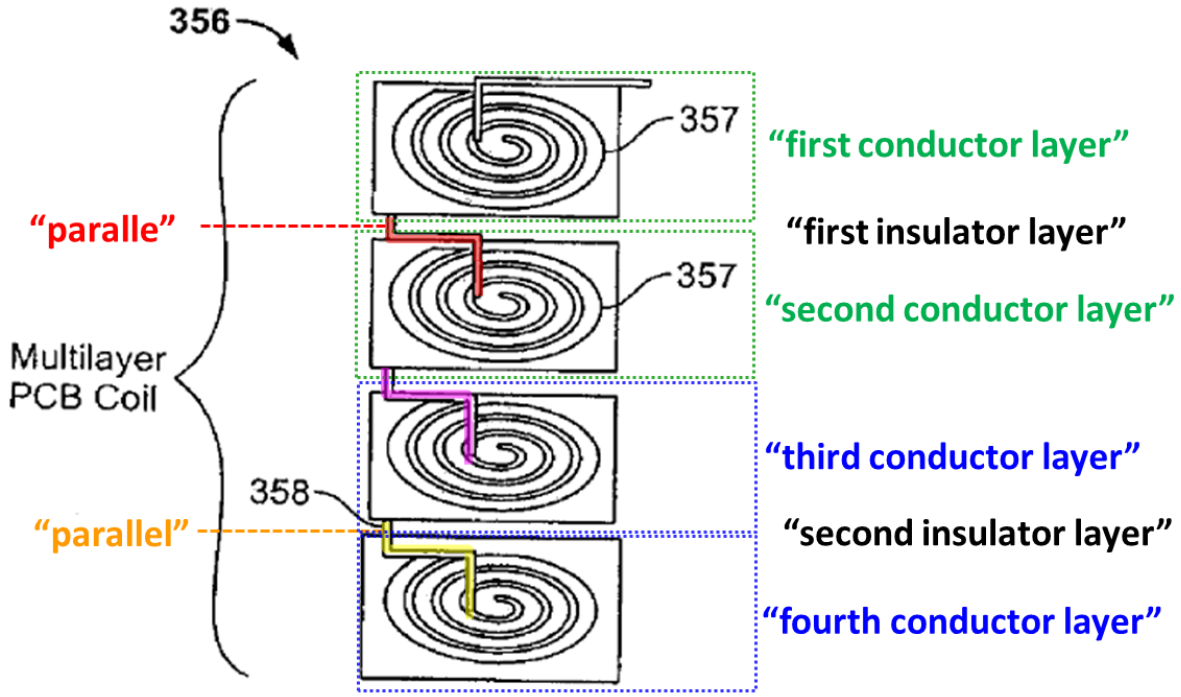


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶127.) As seen in the demonstrative above, the first and second conductor layers are connected in parallel, and the third and fourth conductors are connected in parallel. (Ex. 1002, ¶127.)

While, as seen in the above demonstrative, the first and second conductor layers are connected with the third and fourth conductor layers through a connector (highlighted in pink), Partovi does not explicitly disclose whether the connector (pink) is a series or parallel connection. (Ex. 1002, ¶128.) Nevertheless, as explained below, a POSITA would have found it obvious to implement the connector (pink) as a series connection to increase the inductance of the inductor coil ("the first inductor subassembly is electrically connected in series or parallel to the second inductor subassembly"). (*Id.*)

Partovi discloses that the inductance of a coil increases with the number of turns. (Ex. 1009, ¶¶[0250]-[0254] (showing that inductance L is proportional to number of turns N).) Partovi also discloses that "a larger induction" may be created by "stacking a number of coils vertically and **connecting them in series**." (*Id.*, ¶[0255].) But Partovi recognizes that a balanced approach is needed. For example, Partovi explains that if coils are connected in series, the inductance increases because the number of turns increases, but such a series connection also results in an increase in the resistance. (Ex. 1009, ¶[0255].) In view of the above, a POSITA would have for example, above discussed above, connected the top two layers 357 ("first and second conductors") in parallel to form a first turn ("first inductor subassembly"); and connected the bottom two layers 357 ("the third and fourth conductors") also in parallel to form a second turns ("second inductor

subassembly") to reduce the series resistance of each of the turns. (*Id.*) Additionally, to increase inductance of the inductor, such a person would have connected the two turns in series, to form a winding inductor of multiple turns, each turn having multiple layers. (*Id.*)

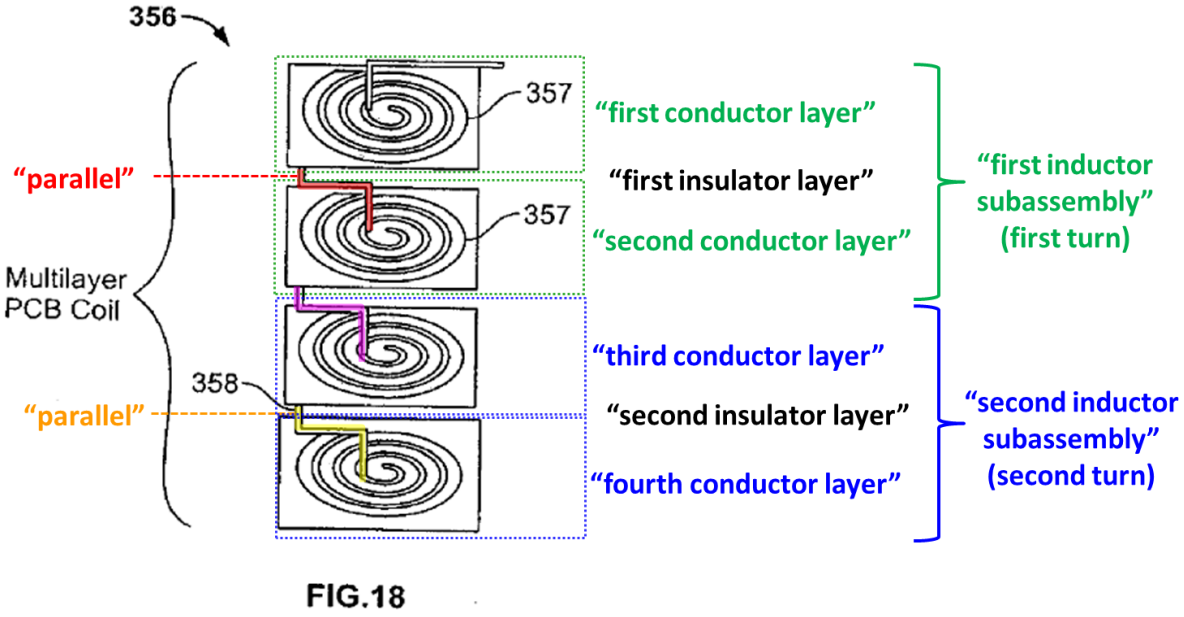


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶129.)

Such an approach is consistent with Chiang's disclosure where two turns are created by stacking conductor layers in parallel. (Ex. 1002, ¶130.) For example, as shown in figure 3 above, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023 at FIG. 3, 7:5-14; *see also id.*, FIG. 5.) The two turns are connected in series because only a single through hole connects the two turns when

two through holes connect the layers that are connected in parallel. (*See id.*, FIG. 3 below.)

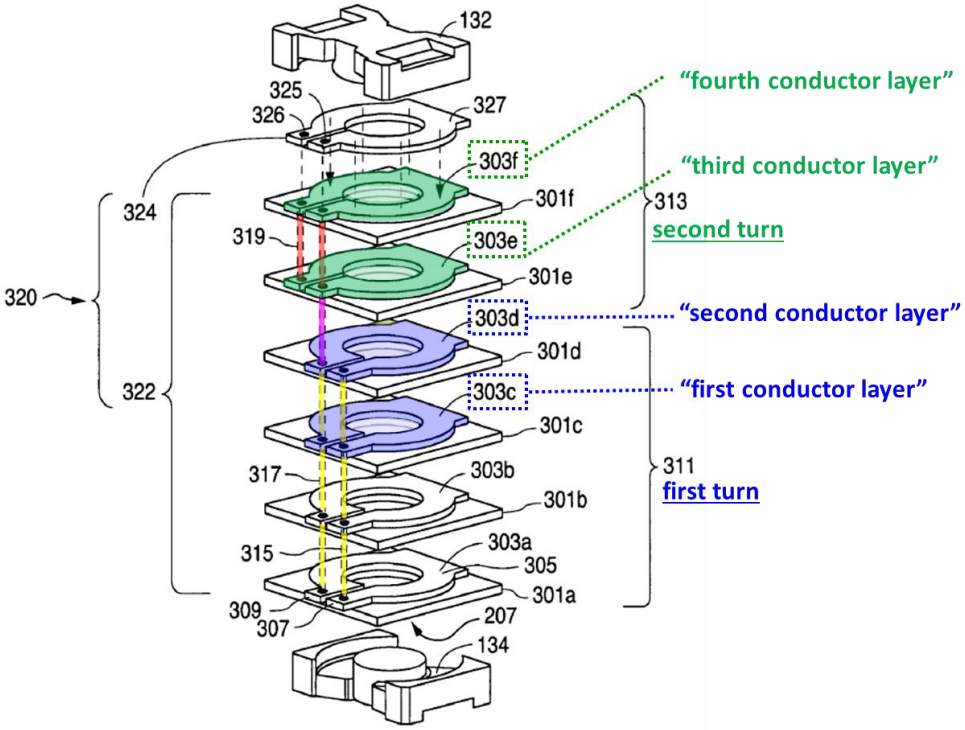


FIG. 3

(Ex. 1023 at FIG. 3 (annotated)); Ex. 1002, ¶130.)

As such, based on the teachings of Partovi and Chiang, a POSITA would have been motivated to take such a balanced approach, i.e., to include additional turn(s) in an inductor winding to **increase inductance**, while having the added turns be constructed with layers connected in parallel to **reduce series resistance**. (Ex. 1002, ¶131.) And, based on those disclosures, such a skilled person would have found it obvious to connect the top two PCB layers 357 in parallel, connect

the bottom two PCB layers 357 in parallel, and implement a series connection between them. (*Id.*) *See KSR*, 550 U.S. at 416.

Accordingly, the Partovi-Chiang combination discloses or suggests the Partovi-Chiang combination recited in claim element 29[b]. (Ex. 1002, ¶132.)

c) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor; and

The Partovi-Chiang combination discloses or suggests this limitation for at least the same reasons as presented above for limitation 1(e). (*Supra* Section IX.A.1(e); Ex. 1002, ¶133.) The modification of Partovi based on Chiang to include a parallel connection between the first and second conductor layers does not affect Partovi's disclosure of this limitation as discussed above with respect to claim element 1(e). (Ex. 1002, ¶133.)

d) wherein when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs, an inductance is generated.

The Partovi-Chiang combination discloses or suggests this limitation for at least the same reasons as presented above for limitation 1(f). (*Supra* Section IX.A.1(f); Ex. 1002, ¶134.) The modification of Partovi based on Chiang to include a parallel connection between the first and second conductor layers does not affect Partovi's disclosure of this limitation as discussed above with respect to claim element 1(f). (Ex. 1002, ¶134.)

5. Claim 30

a) The inductor of claim 29 wherein the first inductor subassembly and the second inductor subassembly are oriented such that the first and second inductor subassemblies are positioned about parallel, about perpendicular, or at an angular relationship with respect to each other.

Partovi in view of Chiang discloses or suggests this limitation. (Ex. 1002, ¶135.) As discussed above with respect to claim 29, in the Partovi-Chiang combination, the PCB layers 357 in Partovi form the "first inductor subassembly" and the "second inductor subassembly." (*Supra* Section IX.C.4.)

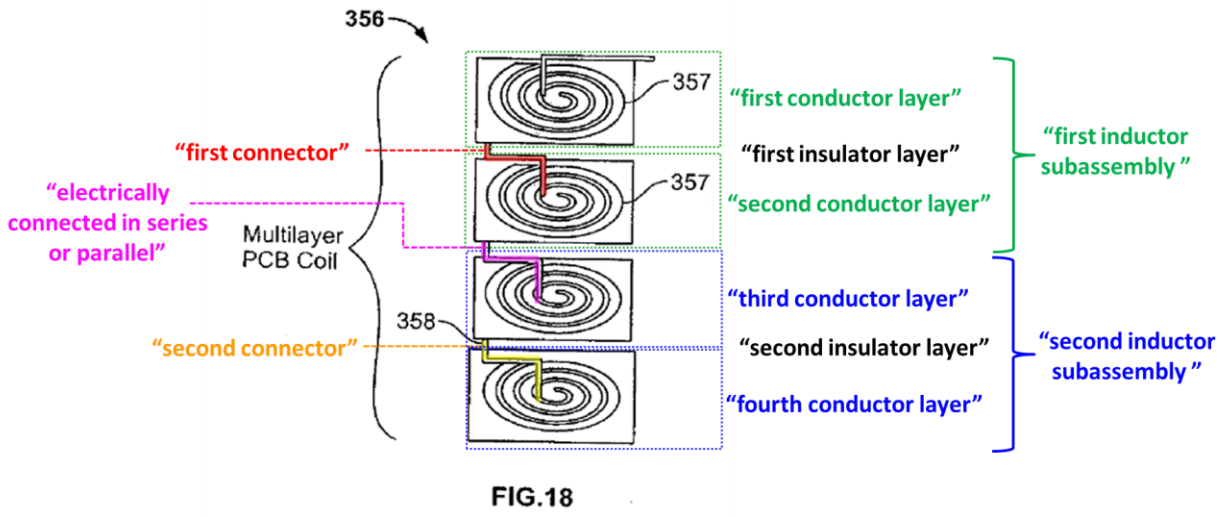


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶135.)

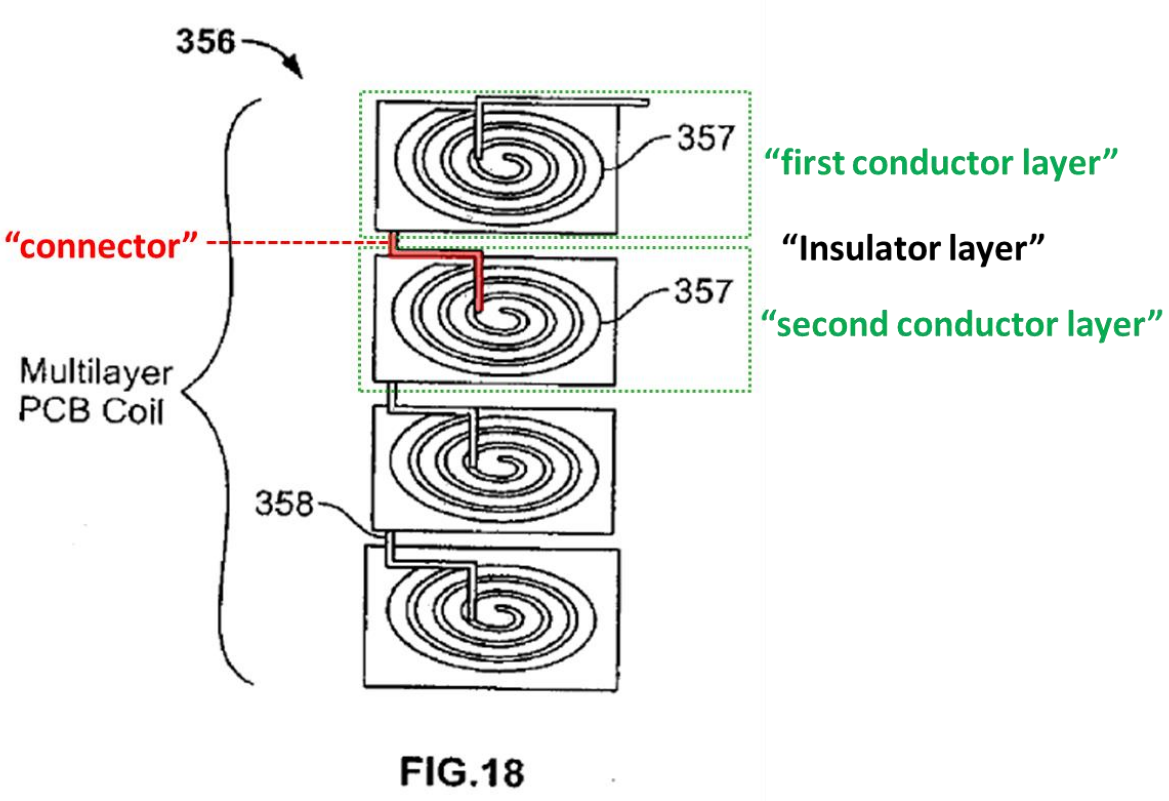
Because each of the PCB layers 357 are separate and spaced apart from each other, (Ex. 1009, ¶¶[0212]-[0224], FIG. 18), the two subassemblies are necessarily "positioned about parallel, about perpendicular, or at an angular relationship with

respect to each other," as they are in different planes. (Ex. 1002, ¶136; *id.*, ¶¶82-83.)

6. Claim 18

a) The inductor of claim 1 wherein at least one connector electrically connects the first conductor layer and the second conductor layer in parallel.

Partovi in view of Chiang discloses or suggests this limitation. (Ex. 1002, ¶137.) As discussed above, Partovi discloses a connector that electrically connects the "first" and "second" conductor layers. (*Supra* Section IX.A.1(d).)



(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶137.)

Partovi does not explicitly disclose that the "connector" electrically connects the top two PCB layers 357 "in parallel," as required by claim 18. But for the same reasons as discussed above with respect to claim element 29[a], a POSITA would have found it obvious to configure the "connector" such that the top two PCB layers are connected in parallel. (*Supra* Sections IX.C.4(a)-(b); Ex. 1002, ¶138.)

7. Claim 20

a) The inductor of claim 1 comprising a third conductor layer and a fourth conductor layer electrically connected in parallel or series and wherein the first and second conductive layers are connected electrically in series or parallel with the third and fourth conductor layers.

The Partovi-Chiang combination discloses or suggests this limitation for reasons similar to as discussed above in Section IX.C.4(b) (claim element 29(b)). (*Supra* Section IX.C.4(b); Ex. 1002, ¶139.)

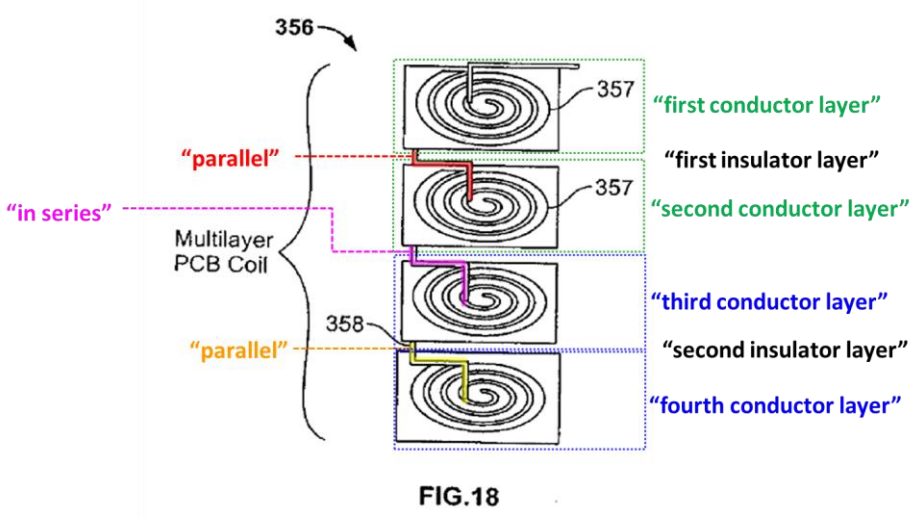


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶139.) For example, as shown in figure 18 above, the Partovi-Chiang combination discloses claim 20. (Ex. 1002, ¶139.)

D. Ground 4: Partovi in View of Phan Renders Obvious Claims 8, 12, 27, and 28

1. Claim 8

a) The inductor of claim 1 wherein a first conductor layer thickness is about the same as a second conductor layer thickness.

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶140-145.) As discussed above, the top two PCB layers 357 in figure 18 of Partovi correspond to the claimed "first conductor layer" and "second conductor layer." (*Supra* Section IX.A.1(a), (b).) (Ex. 1002, ¶141.)

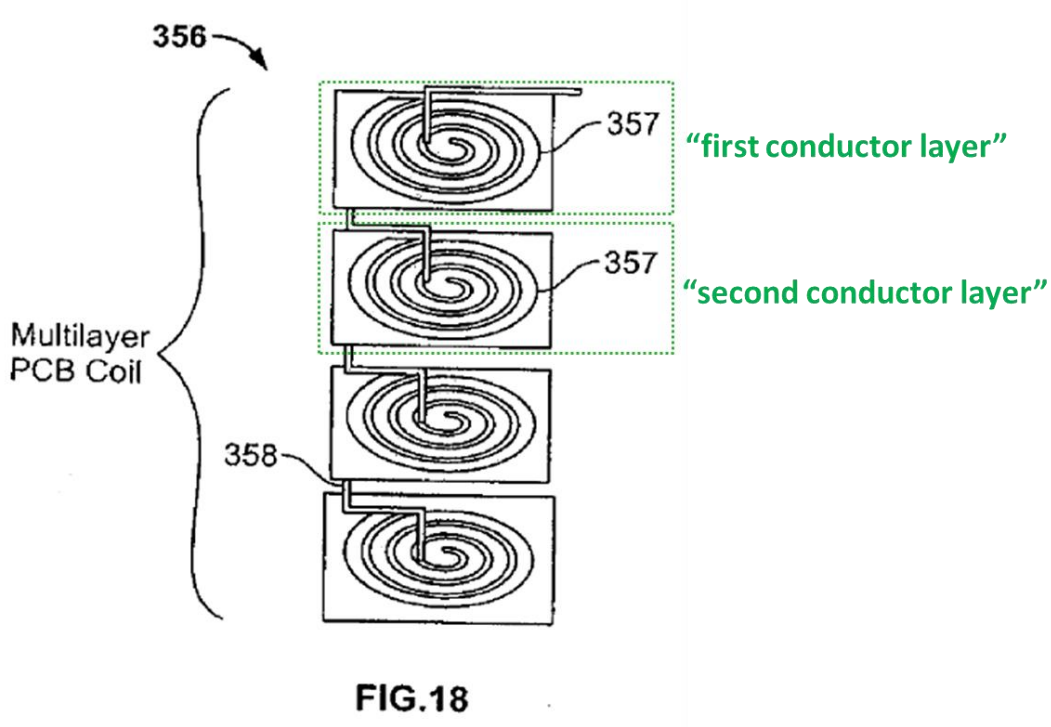


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶141.)

While Partovi does not explicitly disclose that a thickness of the PCB layers 357 is about the same, a POSITA would have found it obvious to use about the same thickness for each of the PCB layers 357 in view of Phan ("wherein a first conductor layer thickness is about the same as a second conductor layer thickness"). (Ex. 1002, ¶142.)

For example, using two PCB layers 357 ("first conductor layer" and "second conductor layer") of the same thickness would have been obvious because there are only two choices: either using layers of the same thickness or using layers of different thickness. (*Id.*, ¶143.) Thus, choosing two PCB layers 357 of the same thickness would have been one of two choices available to a POSITA. (*Id.*) Accordingly, using layers of the same thickness would have been obvious because it would have been one of a "finite number of identified, predictable solutions." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (holding that a claimed step was obvious when it was one of three available choices). Indeed, there is nothing special about setting the thickness of two layers to be the same and this is evident from claims 8 and 9 of the '960 patent. (Ex. 1002, ¶143.) Specifically, while claim 8 recites that the first and second conductor layers have "about the same" thickness, claim 9 recites that the thickness of the two layers is "different." (*Id.*; Ex. 1001, claims 8, 9.)

Phan discloses a multilayer PCB stackup in figure 3 that includes six conducting layers, 302, 304, 306, 308, 310, and 312. (Ex. 1029 at 5:43-46, FIG. 3 (reproduced below).) Each of the conductor layers has the same thickness as shown below in figure 3. (Ex. 1029 at 5:46-48 ("each conductor layer can be made of half ounce of copper and be 0.0007 inches in thickness"); *see also id.*, Abstract, 3:55-61, 3:66-4:4, 5:43-46.)

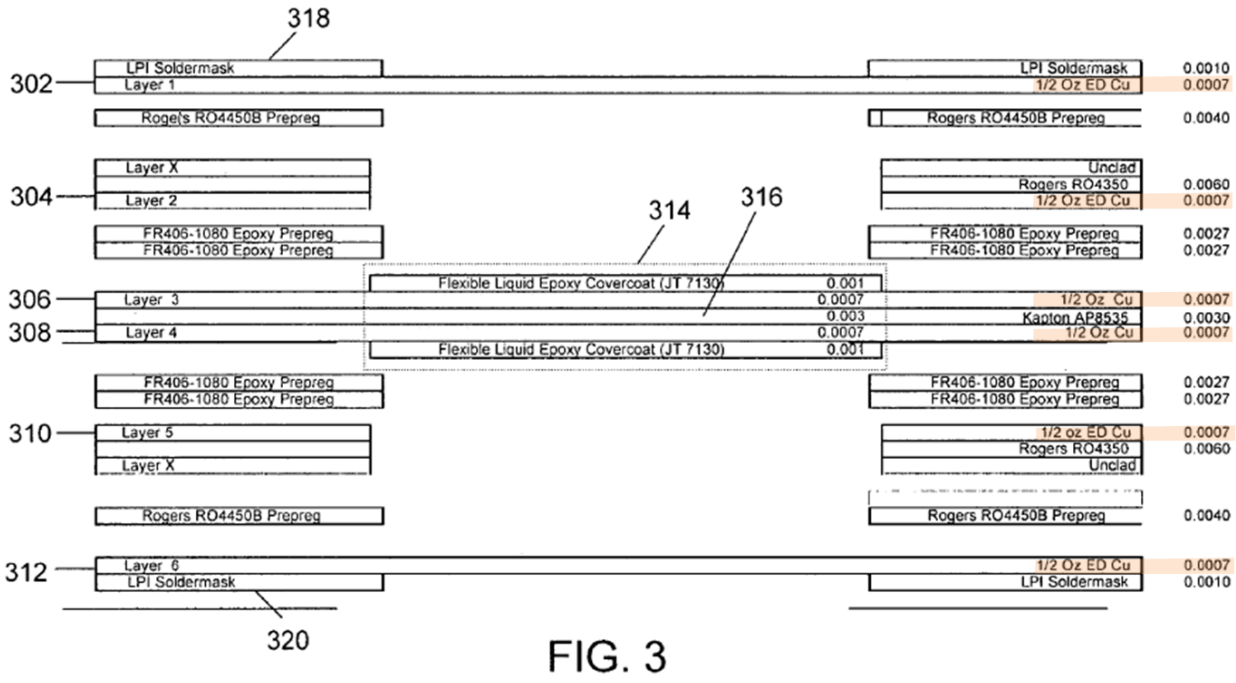


FIG. 3

(Ex. 1029 at FIG. 3 (annotated); Ex. 1002, ¶144.) Phan further explains that "[i]n one embodiment of the invention, the number of layers in [the PCBs] is six," however, in other embodiments "the number of layers . . . can be four . . . or any other number." (Ex. 1029 at 4:28:36.)

A POSITA would have had the skills and knowledge to implement the PCB layers 357 in Partovi such that they were each about the same thickness. (Ex. 1002, ¶145.) Implementing Partovi's PCB layers 357 in such a manner based on the teachings of Phan would have been obvious because, as discussed above, choosing the same thickness for the different PCB layers 357 would have been one of two choices available to a POSITA and a POSITA would have selected the same thickness to suit a POSITA's design objective. (*Id.*) In fact, implementing Partovi's PCB layers 357 to have the same or about the same thickness would have been merely the application of a known technique (e.g., using conductor layers having the same thickness) to a known device (Partovi's PCB-based inductor) according to known methods (e.g., modifying the thickness of conducting layers) to yield the predictable result of an inductor having conducting layers of the same thickness. (Ex. 1002, ¶¶145.) *See KSR*, 550 U.S. at 416-21. The above modification is consistent with Partovi because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212]; *see also id.*at ¶[0479] ("The diameter, thickness, or width of the wire or PCB trace can be optimized to provide optimum resistance."); Ex. 1002, ¶145.)

2. Claim 12

a) The inductor of claim 1 wherein a thickness of the insulating layer is less than about 5 cm.

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶146-150.) While Partovi does not explicitly disclose a thickness of the insulating layer between PCB layers 357, a POSITA would have found it obvious to use insulating layers each having a thickness that is less than 5 cm based on common sense and in view of Phan. (*Id.*, ¶146.)

To begin, given Partovi's objectives of providing devices that are "lightweight," "portable," and have a "compact" design, a POSITA would have been motivated to minimize the thickness of the insulating layers between the PCB layers 357 to ensure that the overall thickness of the PCB is as thin as possible. (Ex. 1009, ¶¶[0010] (disclosing that "a common problem with such inductive units is that the windings are bulky, which restricts their use in lightweight portable devices"), [0212] (disclosing "multiple layer boards can be used to allow compact fabrication"), [0224] (disclosing a need for a coil design "where small x-y coil dimensions are desired")); Ex. 1002, ¶147.) Partovi envisions such an optimization because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212]; *see also id.*, ¶[0479] ("The

diameter, thickness, or width of the wire or PCB trace can be optimized to provide optimum resistance."); Ex. 1002, ¶147.)

Moreover, PCBs where the insulating layer thickness was less than 5 cm were well-known. As discussed above, Phan like Partovi discloses a multi-layer PCB. (*Supra* Section IX.D.1.) Phan discloses using insulating layers of thickness on the order of thousandths of an inch (1/1000 of an inch is 0.00254 cm) to separate PCB conductive layers ("wherein a thickness of the insulating layer is less than about 5 cm"). (Ex. 1029 at 5:40-49, FIG. 3.) For example, Phan discloses "an insulating layer 316 of Kapton" having a thickness of 0.003 inches (which is equal to 0.00762 cm) positioned between conducting layers 306 and 308. (*Id.*; Ex. 1002, ¶148.)

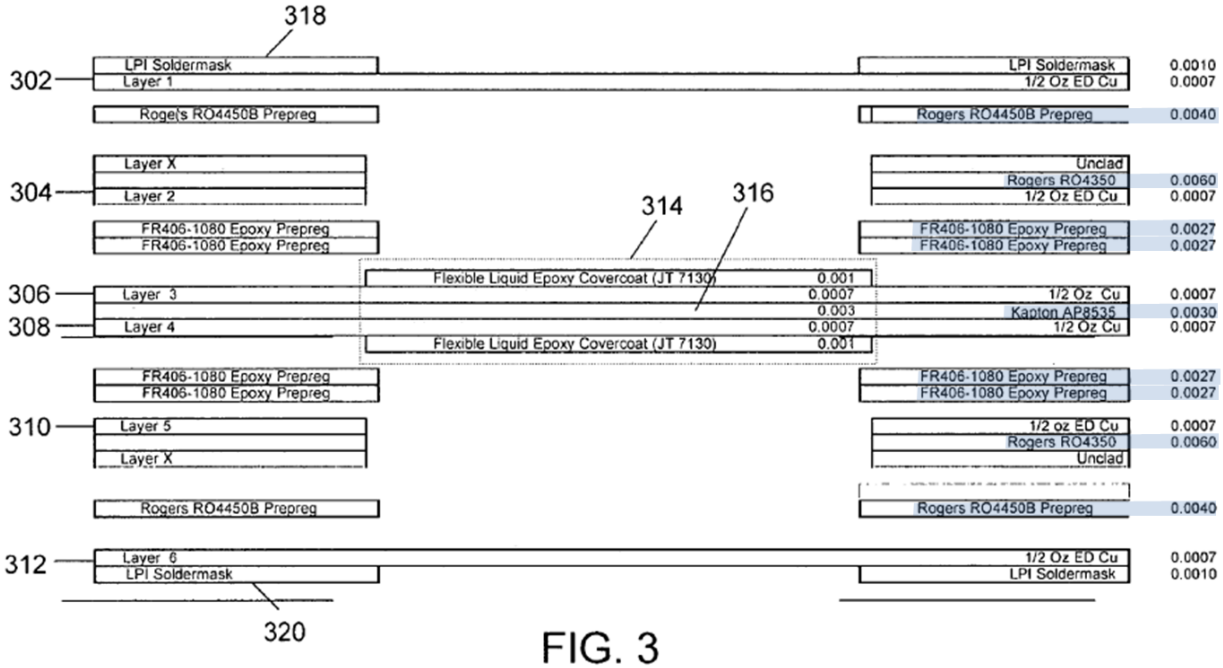


FIG. 3

(Ex. 1029 at FIG. 3 (annotated); Ex. 1002, ¶148.)

A POSITA had the skills and knowledge to design and manufacture the insulating layers in figure 18 of Partovi to be less than 5 cm given the teachings of Phan and such person's knowledge. (Ex. 1002, ¶149.) Therefore, a POSITA would have understood and appreciated that the proposed combination involved combining known prior art elements, and known technologies according to known methods and common sense (e.g., modifying the thickness of insulating layers in Partovi's inductor to be less than 5 cm) to yield the predictable result of an inductor having insulating layers each having a thickness of less than 5 cm. (Ex. 1002, ¶149.) *See KSR*, 550 U.S. at 416-21.

Moreover, the thickness of an insulating layer is a "result-effective variable" because it affects the overall thickness of the PCB and also determines the amount of the insulation between conducting layers on both sides of the insulating layer. (Ex. 1002, ¶150.) Therefore, if "less than 5 cm" is an optimum number for the insulating layer thickness per claim 12, claim 12 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '960 patent provides no evidence that "less than 5 cm" thickness produces a new or

unexpected result, and thus the claimed range cannot form the basis of patentability. (Ex. 1002, ¶150.) *In re Boesch*, 617 F.2d at 276; *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

3. Claim 27

Partovi in view of Phan discloses or suggests this limitation for reasons similar to that discussed below for claim 28. (Ex. 1002, ¶151; *see infra* Section IX.D.4.) In particular, as discussed below with respect to claim 28, a POSITA would have found it obvious to use an electrically insulative material like Kapton for the insulator layer.

4. Claim 28

a) The inductor of claim 1 wherein the insulator layer comprises an electrically insulative material selected from the group consisting of air, polystyrene, silicon dioxide, a biocompatible ceramic, a conductive dielectric material, a non-conductive dielectric material, a piezoelectric material, a pyroelectric material, a ferrite material, and combinations thereof.

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶152-155.) As explained above, Partovi discloses an insulating layer positioned in the space between PCB layers 357. (*Supra* Section IX.A.1(c).) Therefore, Partovi discloses that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex.

1002, ¶152; Ex. 1028 at 1:6-23.) Furthermore, an insulating layer is also a "non-conductive dielectric material." (*Id.*)

To the extent it is argued that Partovi does not disclose such a "non-conductive dielectric material," it would been obvious to combine the teachings of Partovi with Phan such that the insulating material in Partovi's PCB is a "non-conductive dielectric material." (Ex. 1002, ¶153.)

As discussed above, Phan like Partovi discloses a multi-layer PCB. (*Supra* Section IX.D.1; *see also* Ex. 1002, ¶30.) Phan discloses "an insulating layer 316 of Kapton" positioned between conducting layers 306 and 308. (Ex. 1029 at 5:40-49, FIG. 3.)

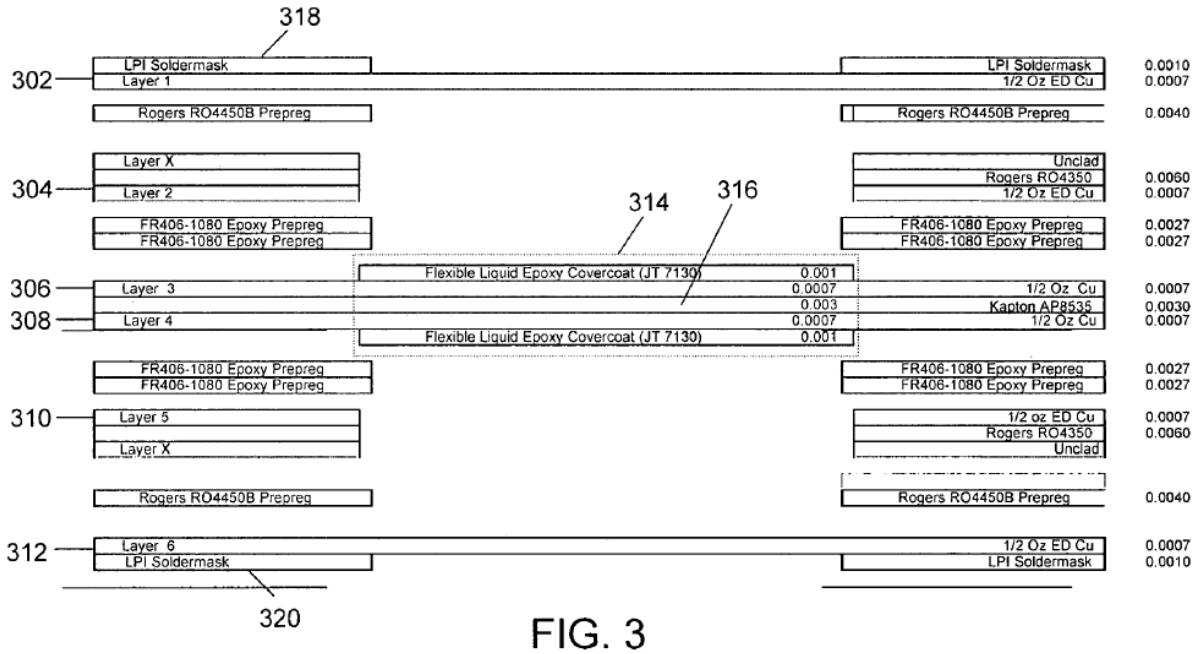


FIG. 3

(*Id.*, FIG. 3.) Kapton is an "electrically insulative material." (Ex. 1032 at 9:3-4, 9:25-27.) Moreover, Kapton is a "non-conductive dielectric material" because it is is electrically insulating, as discussed above, and it was well-known that Kapton is a "dielectric material." (Ex. 1002, ¶154; Ex. 1030 at 2:60-61 ("dielectric layers such as Kapton ® polyimide"); Ex. 1032 at 9:3-4, 9:25-27.)

A POSITA would have found it obvious to use Kapton as the insulating material between Partovi's PCB layers 357. (Ex. 1002, ¶155.) In particular, a POSITA would have known that Kapton is a well-known insulating layer that is **flexible**. (*Id.*; Ex. 1029 at 3:48-55, 5:50-52.) Indeed, the use of Kapton in flexible PCBs is acknowledged by Partovi itself. (Ex. 1009, ¶[0355] ("flexible PCB material such as Kapton").) Given that there were several advantages to a flexible PCB (Ex. 1009, ¶¶[0137], [0151]), a POSITA would have found it obvious to use Kapton as the insulating material in the Partovi PCB. (Ex. 1002, ¶155.) *See Unwired Planet*, 841 F.3d at 1003. Therefore, the Partovi-Phan combination discloses or suggests claim 28 because in the combination, the insulating layer is an "electrically insulative material" such as Kapton, which is a "non-conductive dielectric material."

E. Ground 5: Partovi in View of Chiang and Phan Renders Obvious Claims 8, 12, 27, and 28

As discussed above in Section IX.C.1, Partovi in view of Chiang discloses or suggests all of the limitations of claim 1. But to the extent that the Partovi-

Chiang combination does not explicitly disclose the limitations of claims 8, 12, 27, and 28, a POSITA would have combined the teachings of Partovi and Chiang with Phan for the same reasons that a POSITA would have combined the teachings of Partovi with Phan that renders these claims obvious (*supra* Section IX.D). Therefore, the Partovi-Chiang-Phan combination renders these claims obvious for reasons similar to those discussed above in Section IX.D. (Ex. 1002, ¶156.) Indeed, Chiang's teachings are consistent with Phan's because both disclose multi-layer PCBs in which conducting layers are separated by insulator layers. (Ex. 1023 at 6:23-7:4, FIG. 3; Ex. 1029 at 5:40-49, FIG. 3; Ex. 1002, ¶156.)

F. Ground 6: Partovi in View of Chiang and Tseng Renders Obvious Claims 5-7 and 13

As discussed above in Section IX.C.1, Partovi in view of Chiang discloses or suggests all of the limitations of claim 1. But the Partovi-Chiang combination does not explicitly disclose the limitations of claims 5, 6, 7, and 13. Tseng, however, discloses such limitations. (*Supra* Section IX.B.) Therefore, a POSITA would have combined the teachings of Partovi and Chiang with Tseng for the same reasons that a POSITA would have combined the teachings of Partovi with Tseng that renders these claims obvious (*supra* Section IX.B). Therefore, the Partovi-Chiang-Tseng combination renders these claims obvious for reasons similar to those discussed above in Section IX.B. (Ex. 1002, ¶157.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-8, 10, 12-13, 15-22, and 24-30 of the ’960 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,680,960 contains, as measured by the word-processing system used to prepare this paper, 13,444 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,680,960 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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