UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

NUCURRENT, INC.,
Patent Owner

Patent No. 9,300,046

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,300,046

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-3, 5-8, 10, 12, 13, 15-21, and 23-29 ("the challenged claims") of U.S. Patent No. 9,300,046 ("the '046 patent") (Ex. 1001), which, according to PTO records, is assigned to NuCurrent, INC. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claim should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

Related Matters: The '046 patent is at issue in *NuCurrent, Inc. v. Samsung Electronics Co. Ltd.* and *Samsung Electronics America, Inc.*, Case No. 1:19-cv-00798 (S.D.N.Y.). The '046 patent shares the same specification as U.S. Patent No. 8,698,591 ("the '591 patent"); U.S. Patent No. 8,710,948 ("the '948 patent"); and U.S. Patent No. 8,680,960 ("the '960 patent"). Petitioner is concurrently filing petitions challenging these patents. Moreover, Patent Owner has asserted U.S. Patent No. 9,941,729 ("the '729 patent") in the above litigation.

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel is (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan

R. Bansal (Limited Recognition No. L0667), and (3) Howard Herr (*pro hac vice* admission to be requested). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-NuCurrent-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '046 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-3, 5-8, 10, 12, 13, 15-21, 23-29 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-3, 10, 15-21, 23-26, 28, and 29 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") (Ex. 1009) and U.S. Patent No. 7,248,138 ("Chiang") (Ex. 1023);

Ground 2: Claims 6, 7, and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and U.S. Patent No. 9,912,173 ("Tseng") (Ex. 1022); and

Ground 3: Claims 8, 12, 26, and 27 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and U.S. Patent No. 7,601,919 ("Phan") (Ex. 1029).

Ground 4: Claim 5 is unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and Hu et al., "AC Resistance to Planar Power Inductors and the Quasidistributed Gap Technique," *IEEE Transactions on Power Electronics*, Vol. 16, No. 4, July 2001 ("Hu") (Ex. 1033).

The '046 patent issued from U.S. patent application no. 13/797,459 (the '459 application"), filed March 12, 2013. (Ex. 1001, Cover.) The '046 claims priority to a series of related applications, including Provisional Application No. 61/158,688, filed March 9, 2009. For purposes of this proceeding only however, Petitioner assumes the earliest effective filing date of the '046 patent is March 9, 2009.

Partovi was filed May 7, 2008. (Ex. 1009, Cover). Tseng is a continuation of U.S. Application No. 11/901,158, filed September 14, 2007. (Ex. 1022, Cover). Phan was filed October 21, 2005. (Ex. 1029, Cover). Therefore, Partovi, Tseng,

and Phan are prior art under pre-AIA 35 U.S.C. § 102(e). Chiang issued on July 24, 2007. (Ex. 1023, Cover).

Hu is an IEEE publication that was publicly available to persons interested and skilled in the art in 2001, and at a minimum before March 9, 2009. The Board has routinely held that IEEE publications like Hu are printed publications. *Power Integrations, Inc., v. Semiconductor Components Industries, LLC*, IPR2018-00377, Paper No. 10 at 10 (July 17, 2018) (quoting *Ericsson, Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 at 11 (May 18, 2015)). Indeed, in *Ericsson*, the Board "accept[ed] the publication information on the IEEE copyright line on page 1 of [the IEEE reference] as evidence of its date of publication and public accessibility." *Ericsson*, IPR2014-00527, Paper 41, 10-11; *see also Coriant (USA) Inc. v. Oyster Optics, LLC*, IPR2018-00258, Paper 13 at 11 (June 6, 2018); *Microsoft Corp. v. Bradium Techs. LLC*, IPR2016-00449, Paper 9 at 13 (PTAB July 27, 2016) (noting generally that "IEEE publications, such as the one in which Reddy appeared, are distributed widely and intended to be accessible to the public").

Hu bears the marking "IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 16, NO. 4, JULY 2001" at the top of pages 558, 560, 562, 564, and 566, the title page similarly indicates "JULY 2001 VOLUME 16 NUMBER 4," the copyright page bears the marking "© 2001 by The Institute of

Electrical and Electronics Engineers, Inc.," and the footer on page 558 bears the marking "©2001 IEEE." (Ex. 1033 at Title page (page 1), copyright page (page 2), 558, 560, 562, 564, 566; *see also* Ex. 1038 at 1 ("Date of Publication: Jul 2001" and "Published in: IEEE Transactions on Power Electronics (Volume: 16 , Issue: 4 , Jul 2001)" and "Publisher: IEEE").) With such markings, Hu is similar to the *Microsoft* case referenced above. *Microsoft*, IPR2017-00890, Paper 49 at 19 (Sept. 6, 2018). Moreover, several IEEE publications that were published before the alleged invention date of the '046 patent, and that do not have any co-authors in common with Hu, cite to Hu, demonstrating that Hu was publicly accessible before March 9, 2009. (Ex. 1039 at title page (page 1) ("MAY 2003"), copyright page (page 2) ("Copyright © 2003 by The Institute of Electrical and Electronics Engineers, Inc."), 896 ("MAY 2003" and "© 2003 IEEE"), 906 (citation [17] is to Hu and includes a date of "July 2001"); Ex. 1040 at title page (page 1) ("MARCH 2004"), copyright page (page 3) ("Copyright © 2004 by The Institute of Electrical and Electronics Engineers, Inc."), 531 ("MARCH 2004" and "© 2004 IEEE"), 541 (citation [15] is to Hu and includes a date of "July 2001"); Ex. 1041 at title page (page 1) ("AUGUST 2007), copyright page (page 2) ("Copyright © 2004 by The Institute of Electrical and Electronics Engineers, Inc."), first page of Contents (page 3) ("AUGUST 2007"), 3387 ("AUGUST 2007" and "© 2007 IEEE"), 3394 (citation [2] is to Hu and includes a date of "Jul. 2001").)

Therefore, Chiang and Hu are prior art under pre-AIA 35 U.S.C. § 102(b). None of these references were considered by the Patent Office during prosecution of the '046 patent. (*See, e.g.*, Ex. 1001, Cover ("References Cited"); Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '046 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering, or a similar discipline and at least two years additional relevant experience with power electronics, including design or manufacturing of inductors. (Ex. 1002, ¶¶15-16.)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '046 PATENT AND THE PRIOR ART

A. The '046 Patent

The '046 patent, titled "Multi-layer-multi-turn structure for high efficiency inductors," is directed to "an inductor having a plurality of conductor layers separated by insulator layers," "for incorporation within electric circuits." (Ex. 1001, Abstract, 1:37-40, 4:23-25; *see also id.* at 4:25-26 (disclosing the inductor described is "most notably" for "electrical circuits that operate within and above

[1] Petitioner submits the declaration of Dr. Steven Leeb (Ex. 1002), an expert in the field of the '046 patent. (Ex. 1002, ¶¶1-16; Ex. 1003.)

the radio frequency range of at least 3 kHz"); Ex. 1002, ¶¶31-36.) The '046 patent discloses that one of its objectives is "reducing resistance loss . . . of the inductor structure" with a "multi-layer wire configuration." (*Id.* at 4:16-22.)

With reference to figure 1, the '046 patent discloses "a high-level diagram of an inductor 100 for use in an electronic or electrical circuit . . . compris[ing] a coil 102 and a multi-layer wire 104," that "may have a plurality of turns 122 . . . around a central axis point 124." (*Id.* at 15:8-11, 16:31-36.)

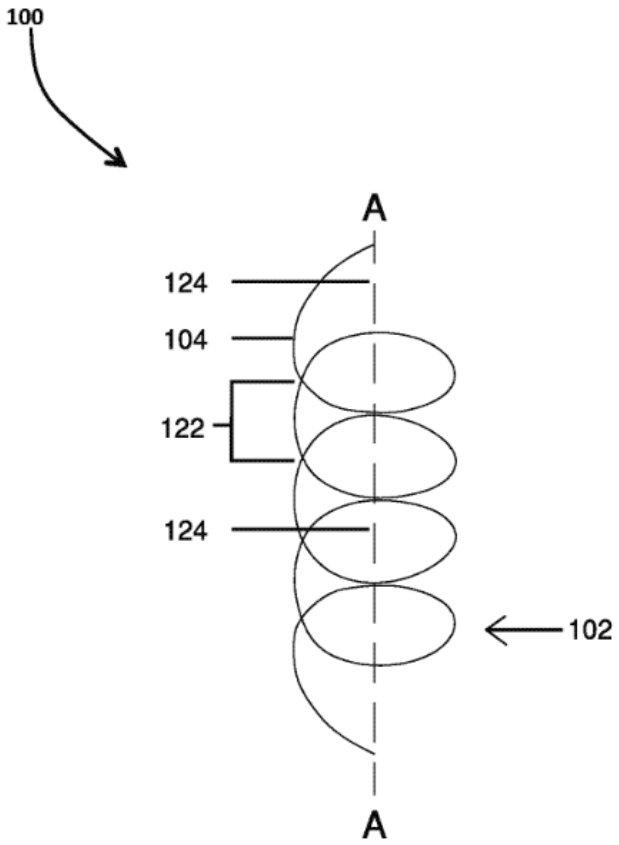
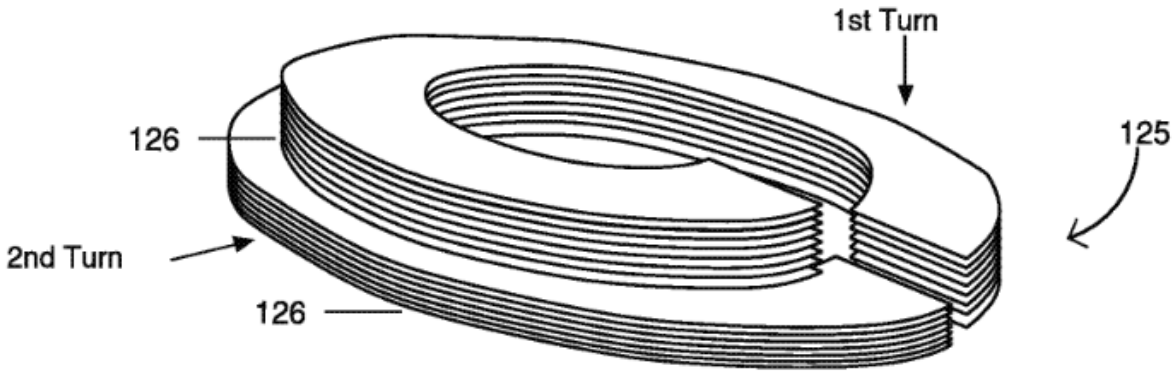


FIG. 1

(*Id.* at FIG. 1.)

The ’046 patent further discloses various embodiments including “a double turn circular spiral-solenoidal coil” in figure 3B “where each turn has N layers,” and “where ‘N’ is a number equal to or greater than one.” (*Id.* at FIG. 3B, 12:34-36, 16:39-46.)



F I G. 3B

(*Id.* at FIG. 3B.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language

of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002, ¶37.)

[2] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '046 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

IX. DETAILED EXPLANATION OF GROUNDS

As discussed below, claims 1-3, 5-8, 10, 12, 13, 15-21, 23-29 are unpatentable in view of the prior art. (Ex. 1002, ¶¶45-154; *see also id.* at ¶¶17-43.)

A. Ground 1: Partovi and Chiang Render Obvious Claims 1-3, 10, 15-21, 23-26, 28, and 29

1. Claim 1

Preamble: A method of manufacturing an inductor structure, the method comprising the following steps:

Partovi in combination with Chiang discloses or suggests this limitation. (Ex. 1002, ¶¶46-47.) For example, Partovi discloses an inductor, e.g., a coil (L_p) 116 used in an inductive power transfer system 110 as shown in figure 2 (reproduced below). (Ex. 1009, ¶[0118] (disclosing a circuit that "can receive energy fed to it from a power source, store the energy alternately in the inductor and the timing capacitor . . . , and subsequently produce an output as a continuous alternating current (AC) wave"); *see also id.* at Abstract; Ex. 1002, ¶¶38-43.)

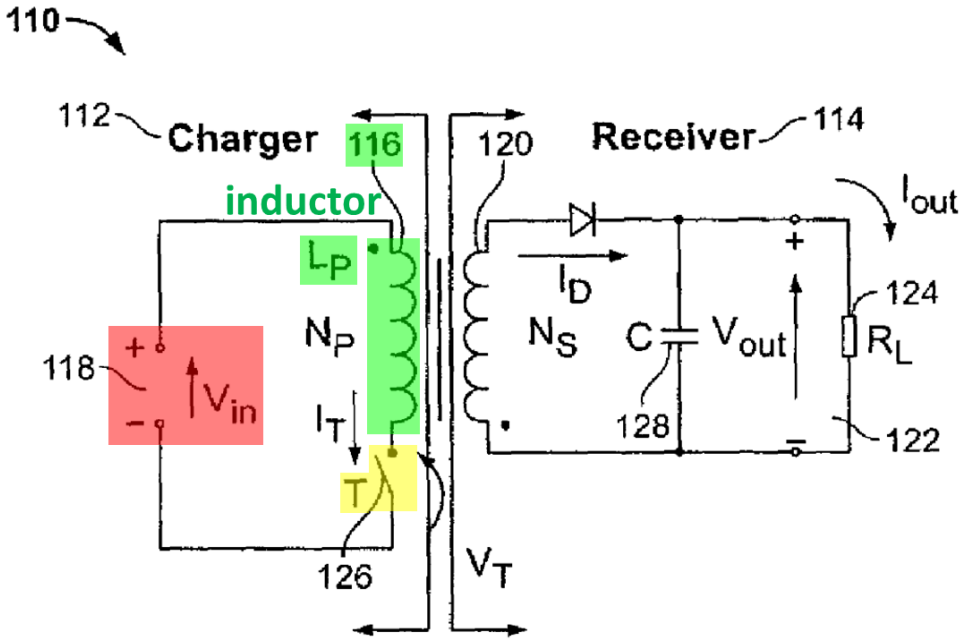


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶46.) Inductive power transfer system 110 includes a charger 112 having a primary coil (L_p) 116 (the claimed "inductor"), a power source (V_{in}) 118, and a switch (T) 126. (Ex. 1009, ¶¶[0117], [0018].) In operation, by switching switch 126 at a certain frequency, an alternating current flows through coil 116, which in turn generates an alternating magnetic field. (*Id.* at ¶¶[0117]-[0118]; *see also id*. at ¶¶[0013], [0091], [0119].) "This [magnetic] field then generates a voltage in the coil 120 in the receiver 11 . . . to provide power 122 to a load RI 124." (*Id.* at ¶[0117]; Ex. 1002, ¶46.)

As discussed below, Partovi in combination with Chiang discloses how to construct the primary coil Lp 116 ("manufacturing an inductor structure"). (*See infra* Sections IX.A.1(a)-(d); Ex. 1002, ¶¶48-81.)

a) providing a first conductor layer and a second conductor layer, the first conductor layer and the second conductor layer being electrically conductive;

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶48-81.) For clarity, this limitation is discussed below in two parts. (*Id.*)

First, Partovi discloses a "first conductor layer." (*Id.*) For example, as discussed above in Section IX.A.1 (preamble), Partovi discloses a primary coil 116 ("inductor") with reference to a figure 2. (*See supra* Section IX.A.1 (preamble); Ex. 1009, ¶[0117] ("primary coil Lp 116").) Partovi further discloses, with reference to figure 18, an implementation of such a coil for "creat[ing] higher [magnetic] flux densities and more efficient power transfer." (Ex. 1009, ¶[0224]; *see also id.* at ¶[0212].)

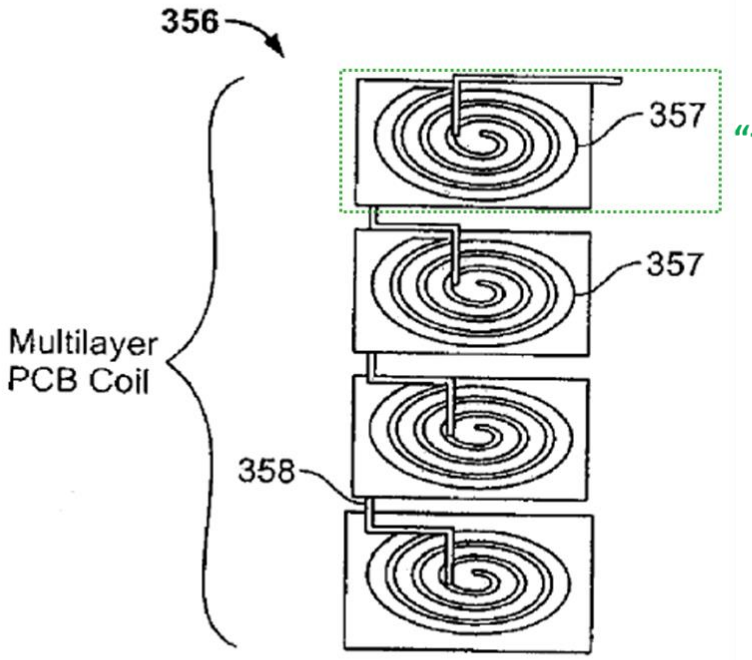


FIG.18

(*Id.* at FIG. 18 (annotated); Ex. 1002, ¶49.)

Partovi discloses that "to achieve higher flux densities, a coil is constructed with two or more layers, for example by using two or more layers of printed circuit board." (Ex. 1009, ¶[0212].) Figure 18 describes an example of such a multi-layer coil 356. (*Id.* at ¶¶[0212], [0224].) For example, multi-layer coil 356 includes four layers 357, where the top most layer 357 constitutes a "first conductor layer," as recited in claim element 1[a]. (Ex. 1002, ¶50.) In particular, Partovi explains that "coil 356 is created in separate PCB layers 357, which are then connected 358, and manufactured together via common techniques used in PCB fabrication, for example by use of a via or contacts." (Ex. 1009, ¶[0224], FIG. 18; *see also id.* at

¶¶[0213]-[0226]; Ex. 1002, ¶50.) A POSITA would have understood that a "PCB layer" is a conductive layer because the different PCB layers are connected through a "via or contacts" (Ex. 1009, ¶[0224]) and a via or contact is used to connect two conductive layers. (Ex. 1002, ¶50.) This is further confirmed by Partovi, which discloses that the coils of the inductor "can be made of copper material." (Ex. 1009, ¶[0225]; *see also id.* at ¶[0248].) When read as a whole, it would have been apparent to a POSITA that the multi-layer coil structure of figure 18 is applicable to the primary coil Lp 116 from figure 2. (Ex. 1002, ¶50.) That is, a POSITA would not have understood the disclosure of figure 18 as being an unrelated embodiment to figure 2, and instead would have understood that the disclosure of figure 18 may apply to all circuit implementations disclosed by Partovi. (*Id.*)

To the extent that the Patent Owner argues or the Board finds that the inductive power transfer system 110 of figure 2 (and other circuit implementations similarly disclosed in Partovi) and the multi-layer coil 356 of figure 18 constitute unrelated embodiments, it would have been obvious for a POSITA to combine the teachings of figure 2 and figure 18 such that the primary coil 116 in figure 2 is implemented as a multi-layer structure like in figure 18. (Ex. 1002, ¶51.)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary

skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007).

Partovi discloses that implementing a coil with multiple layers "allow[s] compact fabrication of high flux density coils." (Ex. 1009, ¶[0212].) By stacking the coils in multiple layers, "overall width of the coil is not increased" and "[t]his technique can be particularly useful for cases where small x-y coil dimensions are desired, and can be used to create higher flux densities and more efficient power transfer." (*Id.* ¶[0224].) As such, a POSITA would have recognized the above discussed benefits of using multi-layer coils and would have been motivated to use such multi-layer coils when implementing primary coil Lp 116 in figure 2 of Partovi because using such a multi-layered coil would have furthered Partovi's objectives of having devices with a "compact" design. (*Id.* at ¶¶[0010] (disclosing that "a common problem with such inductive units is that the windings are bulky, which restricts their use in lightweight portable devices"), [0212] (disclosing "multiple layer boards can be used to allow compact fabrication"), [0224] (disclosing a need for a coil design "where small x-y coil dimensions are desired"); Ex. 1002, ¶52.) *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]").

Furthermore, a POSITA would not have been deterred from utilizing a multi-layer coil inductor in any of Partovi's circuits (including the circuit of figure 2). (Ex. 1002, ¶53.) For example, Partovi discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212].) Partovi does not limit the primary coil used in any of its circuits (including figure 2) to a certain size or shape. Indeed, Partovi explains that the primary coil "can be formed in any number of different shapes" and "can also be **distributed in layers** of coils, spirals, and other various shapes." (Ex. 1009, ¶[225] (emphasis added).)

Moreover, a POSITA would have had the knowledge and skills to implement the primary coil 116 in figure 2 of Partovi as a multi-layer coil (like in figure 18 of Partovi). (*Id.*) This is confirmed by the '046 patent, which admits that systems using multi-layer inductors "can be relatively easily achieved by existing manufacturing techniques (for example multi-layer printed wiring board, FIG. 21), and can therefore be integrated with other circuit components such as ICs, resistors, capacitors, surface mount components, etc." (Ex. 1001, 31:37-42; Ex. 1002, ¶54.) Accordingly, Partovi discloses "a first conductor layer." (*Id.*.)

Second, Partovi discloses "a second conductor layer, the first conductor layer and the second conductor layer being electrically conductive." (*Id.* at ¶¶55-

56.) For example, as explained above, a POSITA would have been motivated to implement Partovi's coil 116 as a multi-layer coil as shown in figure 18. (*See supra* Section IX.A.1(a); Ex. 1002, ¶¶55-56.) Such a multi-layer coil includes a second PCB layer 357 ("second conductor layer"). (Ex. 1009, FIG. 18, ¶¶[0212]-[0226]; Ex. 1002, ¶¶55-56.)

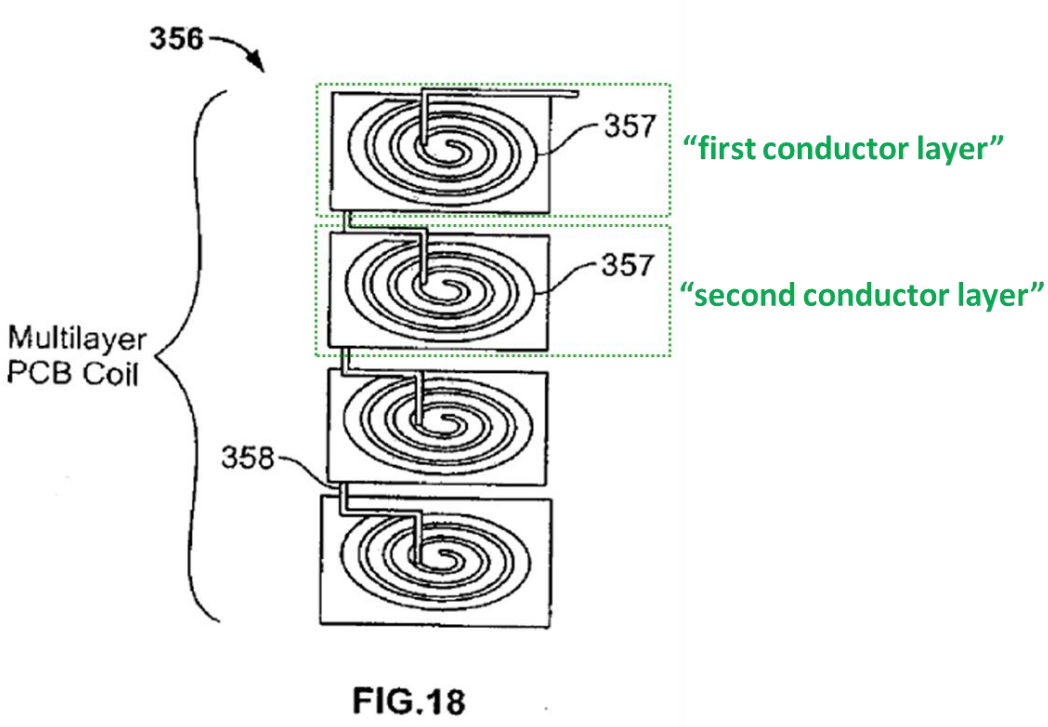


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶55.)

Like the "first conductor layer" disclosed in Partovi, the disclosed "second conductor layer" can be "made of copper material." (Ex. 1009, ¶[0225]; *see also id.* at ¶[0248].) Accordingly, Partovi discloses "the first conductor layer and the second conductor layer being electrically conductive." (Ex. 1002, ¶56.)

b) positioning an insulator layer between the first conductor layer and the second conductor layer; and

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶57-61.) Partovi discloses that the multi-layer PCB coil 356 (including the claimed "first conductor layer" and "second conductor layer") "is created in **separate** PCB layers 357", which are connected by via or contacts using "common techniques used in PCB fabrication." (Ex. 1009, ¶[0224] (emphasis added).) Because the PCB layers are "separate" and there is a connector between two PCB layers, a POSITA would have understood that there is an insulator between them as otherwise the two layers would be deemed the same layer and no connector would be needed. (Ex. 1002, ¶57.) The use of a via or contact between the PCB layers also clearly indicates the presence of an insulating layer between the traces. (*Id.*)

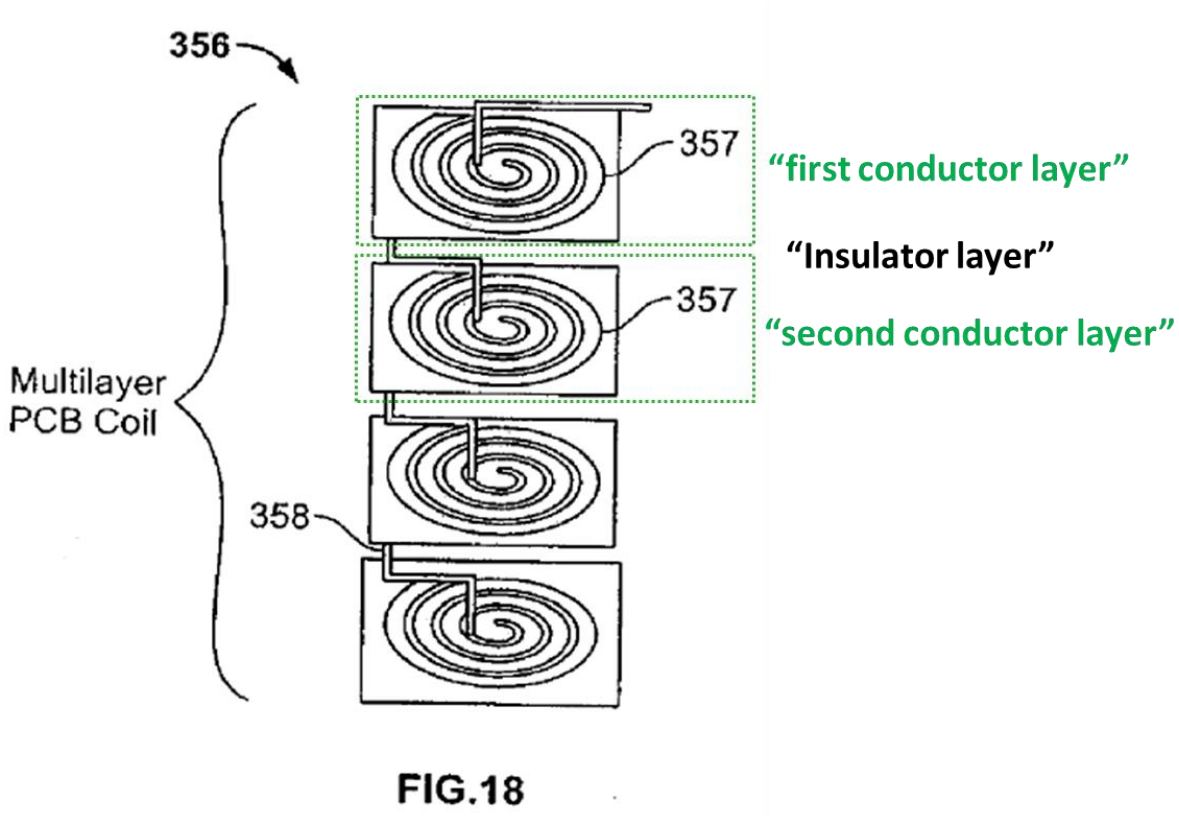


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶57.)

Thus, Partovi discloses "an insulator layer" that is positioned in the space between all four layers 357, including the space between the top two layers ("first conductor layer" and "second conductor layer"). (Ex. 1002, ¶58.) Accordingly, Partovi discloses "positioning an insulator layer between the first conductor layer and the second conductor layer." (*Id.*)

To the extent that PO contends or the Board finds that the presence of such an "insulator layer" between the PCB layers 357 is not explicit or implied in Partovi, a POSITA would have been motivated to combine the teachings of Partovi with Chiang to provide an "insulator layer" between each of the PCB layers 357 to

ensure they are electrically insulated from each other and therefore, capable of functioning in an expected manner. (Ex. 1002, ¶59.)

Like Partovi, Chiang discloses techniques for forming inductors using a multi-layer printed circuit board (PCB). (Ex. 1023 at 1:7-10, 4:67-5:9.) "An embodiment of an inductor according to the present invention formed on a six layer PCB and having two winding turns is shown in the exploded perspective view of FIG. 3 . . . ." (*Id.* at 6:19-23, FIG. 3.) Each of the six PCB layers (303) is separated from the other by an insulating layer 301. (*Id.* at 6:23-7:4, FIG. 3.) The PCB layers are connected with each other using "plated through holes" that are formed using "micro-**vias**." (*Id.* (emphasis added).) Therefore, as shown below, Chiang discloses "a first insulator layer" (e.g., insulating layer 301d) positioned in the space between a first conductor layer (303d) and a second conductor layer (303c).

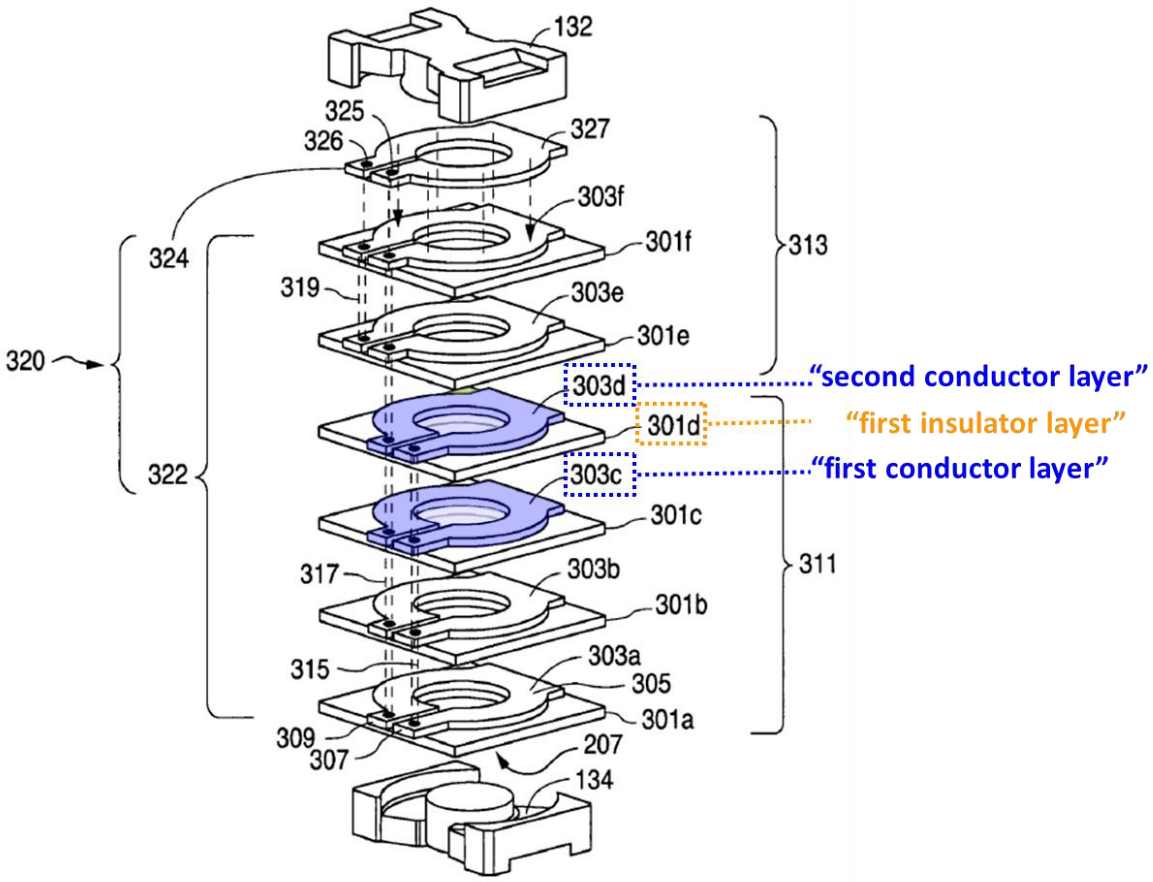


FIG. 3

(*Id.* at FIG. 3 (annotated); Ex. 1002, ¶60.)

Based on the combined teachings of Partovi and Chiang, a POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶61.) A POSITA seeking to implement Partovi would have looked to Chiang because both disclose PCB-based inductors. (*Id.*) Having looked to Chiang, a POSITA would have recognized that a typical multi-layer PCB includes conductor layers separated from each other by an

insulating layer and would have therefore, combined the teachings of Partovi and Chiang to include insulating layers between each of the PCB layers 357 in figure 18 of Partovi. (*Id.*) A POSITA would have been motivated to do so because such a configuration was typical for PCBs and required in order to ensure that adjacent PCB layers are not shorted. (*Id.*) If an insulating layer did not exist between two PCB layers then those two layers would be just one layer and not "separate[]" as disclosed by Partovi. (Ex. 1009, ¶[0224]; Ex. 1002, ¶61.) Indeed, using an insulating between two PCB layers 357 in figure 18 of Partovi would have been nothing more than the combination of familiar elements according to known techniques yielding the predictable result of a functional PCB-based inductor. (Ex. 1002, ¶61.) *KSR*, 550 U.S. at 416-21.

c) connecting the first conductor layer and the second conductor layer in an electrically parallel connection with at least two connectors, each connector having an electrical impedance;

Partovi in view of Chiang discloses or suggests this limitation. (Ex. 1002, ¶¶62-70.) To begin, Partovi discloses "a multi-layer PCB coil 356 is created in separate PCB layers 357" (including "the first conductor layer and the second conductor layer") which are then "connected [by a via or contact] 358," as shown in figure 18 below. (Ex. 1009, ¶[0224], FIG. 18.) Therefore, Partovi discloses "connecting the first conductor layer and the second conductor layer."

Furthermore, as seen below, the two layers are electrically connected by a connector.

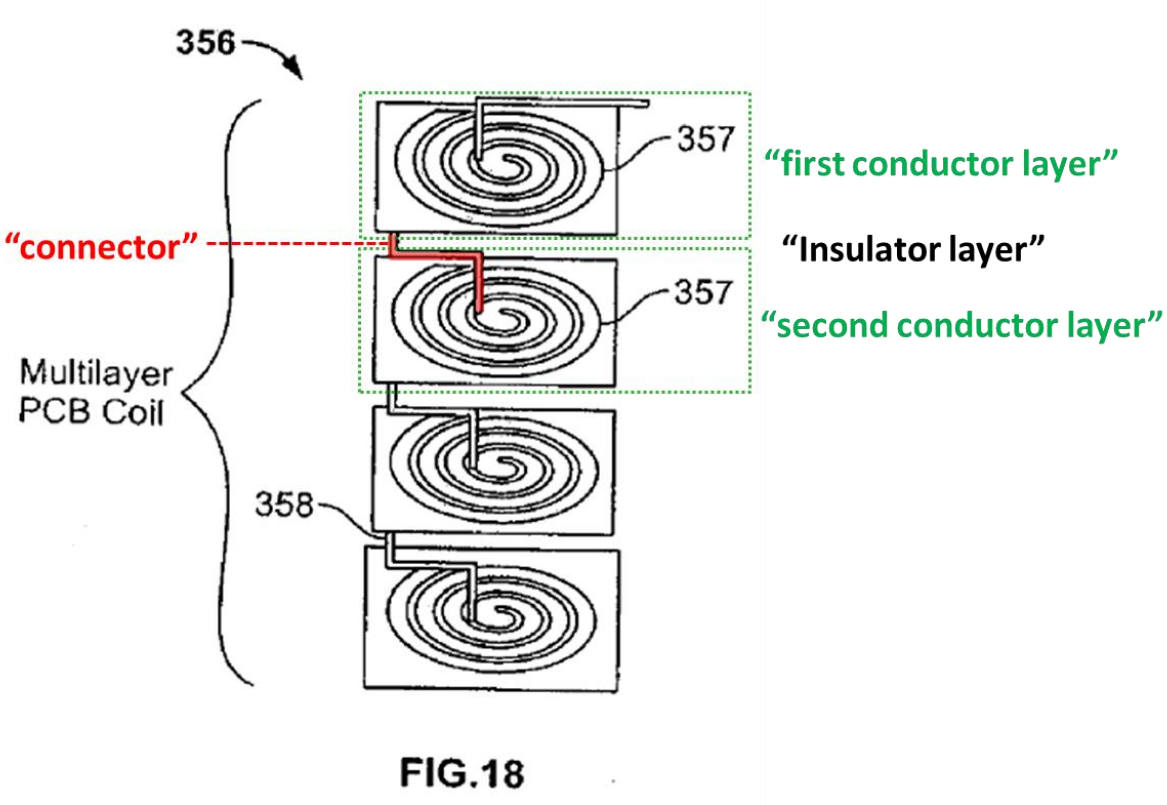


FIG.18

(*Id.* at FIG. 18 (annotated); Ex. 1002, ¶62.)

But Partovi does not explicitly disclose connecting the top two PCB layers 357 ("the first conductor layer and the second conductor layer") in an electrically *parallel* connection *with at least two connectors, each connector having an electrical impedance*, as required by claim 1. Nonetheless, a POSITA would have found it obvious to implement such a feature in view of Chiang and the knowledge of such a person. (Ex. 1002, ¶63.)

Like Partovi, Chiang discloses a multi-layer PCB inductor. (*See, e.g.*, Ex. 1023 at Title, Abstract, 1:7-10, 4:20-22, 4:62-5:4, 6:19-23, FIGs. 3-5.) For example, Chiang discloses with reference to figure 3 (below) a winding 320 that includes a multi-layer PCB 322, which includes a first turn 311 and a second turn 313, collectively formed by six conducting layers 303a-303f and six insulating layers 301a-303f. (*Id.* at 6:23-30.) The two ends (307 and 309) on conducting layer 303 are "interconnected through the insulating layers . . . by one or more plated through holes formed therein." (*Id.* at 6:37-40; *see also id.* at 6:30-37.)

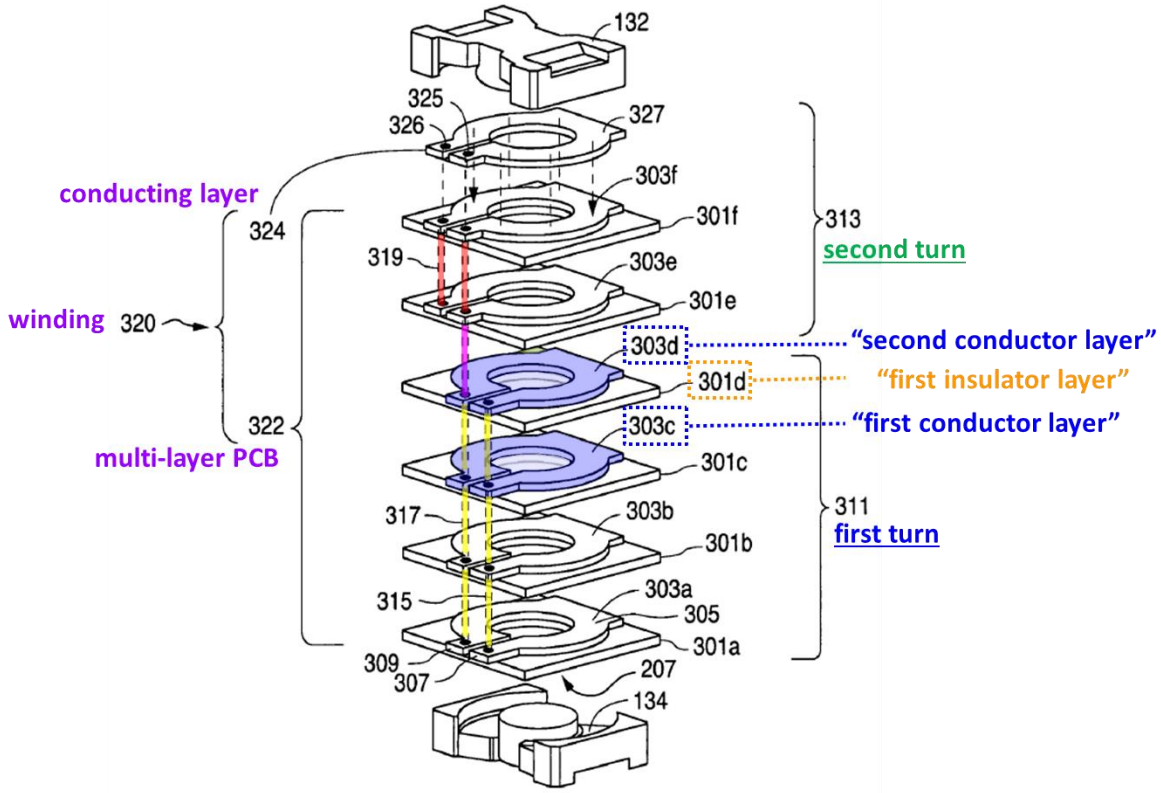


FIG. 3

(*Id.* at FIG. 3 (annotated); Ex. 1002, ¶64.)

Furthermore, Chiang discloses that each of the conducting layers may be "**connected in parallel to decrease the impedance** of a particular turn of the winding." (Ex. 1023 at 1:62-64 (emphasis added).) For example, Chiang discloses that conducting layer 303c ("first conductor layer") and conducting layer 303d ("second conductor layer") are electrically connected in parallel by plated through holes 315 and 317 ("at least two connectors"). (Ex. 1023 at 7:5-14; *see also id.* at 6:51-7:4.) Each of plated through holes 315 and 317 has an "electrical impedance"

because Chiang discloses that they have a certain "conductivity." (*Id.* at 6:45-50; Ex. 1002, ¶65.)

Therefore, Chiang discloses "connecting the first conductor layer and the second conductor layer in an electrically parallel connection with at least two connectors, each connector having an electrical impedance." (Ex. 1002, ¶66.)

Based on the combined teachings of Partovi and Chiang, a POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶67.) A POSITA seeking to implement Partovi would have looked to Chiang because both disclose PCB-based inductors. (*Id*.) And, based on those disclosures, such a skilled person in the art would have found it obvious to modify the multi-layer coil 356 in figure 18 of Partovi such that at least two connectors connect the PCB layers 357 (including the "first conductor layer" and the "second conductor layer") **"in an electrically parallel connection with at least two connectors, each connector having an electrical impedance**." (*Id.*) For example, in such a combination, the connector connecting the top two PCB layers 357 in figure 18 of Partovi could have been implemented using at least two connectors (like plated through holes 315 and 317 in Chiang) connecting the two PCB layers in parallel. (*Id.*) As discussed below, a POSITA would have been motivated to do so because it would have decreased the resistance of the coil, which is an objective of Partovi. (*Id.*)

Partovi discloses that while multiple layers of PCB coils can be stacked for "compact fabrication" of high flux density coils (Ex. 1009, ¶[0212], FIG. 18), such a configuration has some drawbacks. (Ex. 1002, ¶68.) Notably, Partovi discloses that "[w]hile larger values [of inductance] can be obtained by increasing the number of turns or stacking a number of coils vertically and connecting them in series, this larger induction **comes at the price of increased resistance and therefore loss in the inductor**." (Ex. 1009, ¶[0255] (emphasis added).) Partovi notes that "for the power efficiency to be maximized and to minimize losses in the coil, the coils should be manufactured to have as low a resistance as possible." (*Id.* at ¶[0167.) As such, a POSITA would have been motivated to utilize a parallel connection between the PCB layers 357 in Partovi because doing so would have improved the performance of the circuit by, e.g., **reducing resistance** and loss of the inductor. (Ex. 1002, ¶68; Ex. 1023 at 1:62-64; *see also* Ex. 1025 at ¶¶[0030], [0036].) *See Unwired Planet*, 841 F.3d at 1003.

Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil and/or circuits and to combine the same. (Ex. 1002, ¶69.) Therefore, a POSITA would have understood and appreciated that the proposed Partovi-Chiang combination involved a combination of known prior art elements and technologies (e.g., the multi-layer inductor disclosed by Chiang that reduces resistance and the multi-layer inductor disclosed by Partovi that would benefit

from a reduced resistance) according to known methods (e.g., connecting two conductive layers in an inductor using at least two connectors or vias as discussed by Chiang) to yield the predictable result of a circuit with an improved efficiency for having a reduced series resistance. (Ex. 1002, ¶69.) *See KSR*, 550 U.S. at 416.

Accordingly, the Partovi-Chiang combination discloses or suggests claim element 1[c]. (Ex. 1002, ¶70.)

d) wherein, when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶71-77.) For clarity, this limitation is discussed below in two parts.

First, Partovi discloses "when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor." (*Id.*) As discussed above in Section IX.A.1(preamble), Partovi discloses that an AC current flows through the primary coil 116 resulting in the generation of an AC magnetic field. (*See supra* Section IX.A.1(preamble); Ex. 1009, ¶¶[0117], [0118], *see also id*. at ¶¶[0013], [0119].) For example, Partovi discloses that an "AC voltage" is generated "across the primary coil Lp 116" and as a result, an "AC magnetic field" is generated. (Ex. 1009, ¶¶[0117].) The application of a voltage across the primary coil Lp 116 would therefore result in an AC current propagating

through the primary coil Lp 116 the value of which would be proportional to the ratio of the applied voltage and the impedance of the primary coil Lp 116. (Ex. 1002, ¶72.) This AC current is shown as I_T in figure 2. (*Id.*)

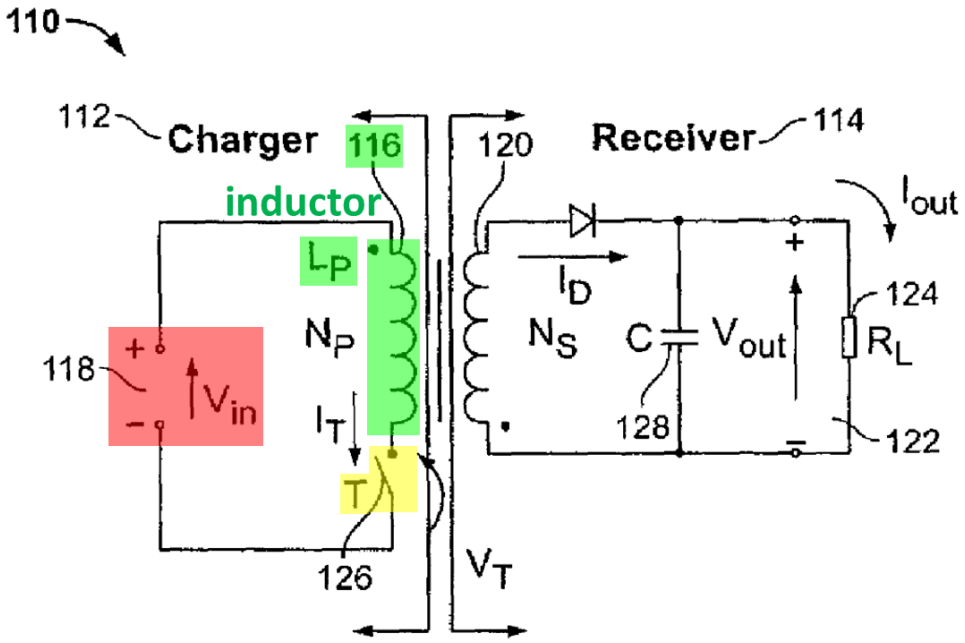


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶72.)

Because the primary coil Lp 116 includes the "first conductor layer" (*supra* Section IX.A.1(a)), the same current I_T also passes through the "first conductor layer." (Ex. 1002, ¶73.) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect Partovi's disclosure that an AC current propagates through the "first conductor layer." (*Id.*) Moreover, generation of a magnetic field is associated with generation of a magnetic flux. (Ex. 1002, ¶73

(flux density B = constant*H (i.e., magnetic field*permeability), and B*Area=flux); Ex. 1006 at 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil."), 554-555; Ex. 1009, ¶[0212] (disclosing that a coil constructed with two or more layers can achieve a higher magnetic flux density than a single layer coil), FIG. 18.) Therefore, Partovi system discloses that "when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor." (Ex. 1002, ¶73.)

Indeed, claim element 1[d] merely claims an inherent property of an inductor like primary coil 116. (Ex. 1006 at 557-559, 560-565, 604; Ex. 1002, ¶74.) The '046 patent admits as much. (Ex. 1001, 1:55-57 ("In an inductor, electric current travels through the metallic coil generating a magnetic flux that is proportional to the amount of electric current.")

Second, the Partovi-Chiang combination discloses "a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current." (Ex. 1002, ¶75.)

To begin, as admitted by the '046 patent, the claimed limitation is an inherent property of an inductor. (Ex. 1002, ¶76.) For example, the '046 patent

admits that. (Ex. 1001, 1:55-65, 14:17-27; Ex. 1002, ¶76) Therefore, when there is a change in the inductor current's frequency, magnitude, or waveform shape, an inductance and a magnetic flux are necessarily generated. (Ex. 1002, ¶76.) Accordingly, the Partovi-Chiang combination necessarily discloses this feature because the combination discloses using an inductor. (*Id.*; *see also* Ex. 1009, ¶[0247] ("inductance of the coil").)

Furthermore, the Partovi-Chiang combination discloses this limitation for the following additional reasons. (Ex. 1002, ¶¶77-81.)

(1) **The Partovi-Chiang combination discloses "a change occurs in . . . a <u>magnitude</u> . . . of the propagated electrical current"**

As discussed in Section IX.A.1(preamble), Partovi discloses with reference to figure 2 (shown below) that by switching switch 126 at a certain frequency, an alternating current is generated and provided through the inductor coil. (Ex. 1009, ¶¶[0117]-[0118]; *see also id*. at ¶¶[0013], [0119].)

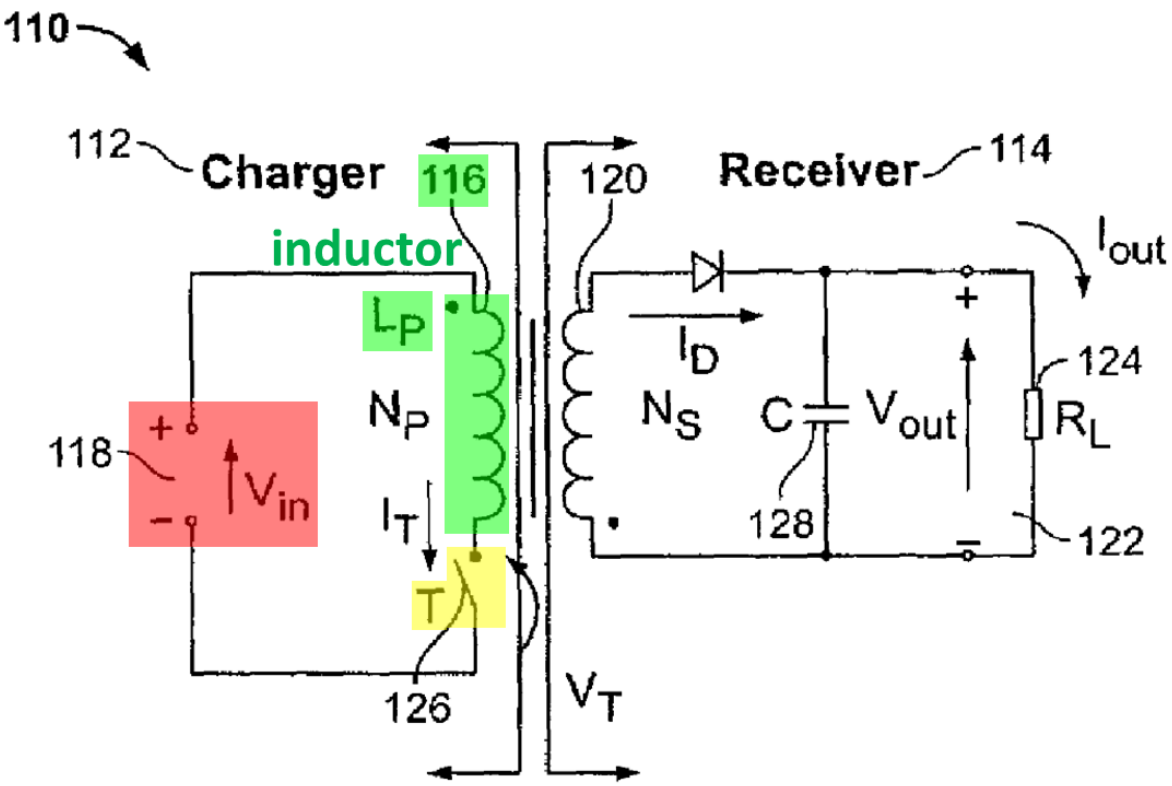


FIG. 2

(*Id.* at FIG. 2 (annotated); Ex. 1002, ¶78.) A POSITA would have understood that an alternating current is a current whose magnitude changes with time. (Ex. 1002, ¶78; Ex. 1010 at 25.) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect such disclosure. (Ex. 1002, ¶78.)

Accordingly, the Partovi-Chiang combination discloses "a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current," because the magnitude of the current propagating through the primary coil changes, which

will necessarily generate a change in magnetic flux. (Ex. 1002, ¶79; *see* Ex. 1001, 1:55-65.)

(2) The Partovi-Chiang combination discloses "a change occurs in at least one of a <u>frequency</u> . . . or a <u>waveform shape</u> of the propagated electrical current"

Partovi also discloses that "the **duty cycle** of the charger switching circuit or its **frequency can be changed**" to adjust the system's output voltage to accommodate different charging or powering requirements of devices receiving power from the primary coil 126. (Ex. 1009, ¶¶[0119] (emphasis added).) That is, Partovi discloses changing the duty cycle or switching frequency of switch 126, which would in turn change the frequency and waveform shape of the current through the primary coil 126. (Ex. 1002, ¶80; *see also* Ex. 1009, ¶¶[0130], [0237], [0246], [263].) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect such disclosure. (Ex. 1002, ¶80.)

Accordingly, the Partovi-Chiang combination discloses "a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current," because the frequency or waveform shape of the current propagating through the primary coil changes, which will necessarily generate a change in magnetic flux. (Ex. 1002, ¶81; *see* Ex. 1001, 1:55-65.)

2. Claim 2

a) The method of claim 1 further generating an electromotive force when at least one of the frequency, the magnitude, or the waveform shape is changed.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶82-83.) The claimed feature is merely an inherent property of an inductor, as admitted in the '046 patent, where a change in the current flowing through the inductor results in the generation of an EMF (electromotive force) across the inductor that opposes this change in current. (Ex. 1002, ¶82; Ex. 1001, 1:55-65, 14:17-27.) Therefore, because the Partovi-Chiang combination discloses an inductor (i.e., the primary coil 116), an electromotive force will necessarily be generated when there is change in "at least one of the frequency, the magnitude, or the waveform shape" of an electrical current flowing through the inductor (and therefore, through the "first conductor layer"). (Ex. 1002, ¶82.)

Furthermore, as discussed above in Section IX.A.1(d), the Partovi-Chiang combination discloses changing the magnitude, waveform shape, and frequency of the current through the primary coil 116 to generate an inductance and a magnetic flux. (*See supra* Section IX.A.1(d).) Given that inductance is simply a measure of EMF generated in response to a change in current per unit time, "electromotive force" is necessarily generated in the primary coil 116 when the above current passes through it. (Ex. 1002, ¶83; *see also* Ex. 1006 at 601; Ex. 1010 at 517.)

Indeed, as admitted in the '046 patent, generation of an electromotive force is an inherent property of an inductor when a change in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current occurs. (Ex. 1001, 1:55-65; Ex. 1002, ¶83.)

3. Claim 3

a) The method of claim 1 further providing a magnitude of the magnetic flux proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶84.) As admitted by the '046 patent, the claimed limitation is an inherent property of an inductor. (Ex. 1001, 1:55-61 (emphases added); Ex. 1002, ¶84.) Thus, because the Partovi-Chiang combination discloses changing a frequency, magnitude, or the waveform shape of the current propagating through the primary coil (*supra* Section IX.A.1(d)), the combination necessarily discloses "a magnitude of the magnetic flux proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current." (*See supra* Section IX.A.1(d); Ex. 1002, ¶84; Ex. 1006 at 592-593, 601 ("When current is sent through a coil, a magnetic field is established through it, and any changes in the current generate changes in the magnetic flux through the coil.").)

4. Claim 10

a) The method of claim 1 further providing a thickness of a first skin depth of the first conductor layer about the same as a thickness of a second skin depth of the second conductor layer.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶85-86.) As admitted by the '046 patent, "skin depth" defines a depth below a conductor's surface where most of the current flows. (*Id.*) Skin depth for a conductor is determined based on the frequency of the current propagating through the conductor, and intrinsic properties of the conductor, including conductivity and permeability. (Ex. 1002, ¶¶85-86.) At least because Partovi discloses that layers 357 (including "the first conductor layer" and "the second conductor layer") "can be made of copper material," Partovi discloses that these layers are made of the same material and thus the layers necessarily share the same conductivity and permeability. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1002, ¶¶85-86.) Furthermore, because layers 357 belong to the same primary coil 116, they are subject to the same current and frequency thereof. (Ex. 1002, ¶¶85-86.) Accordingly, each of layers 357 of Partovi's inductor has about the same skin depth because they have the same current, frequency, conductivity, and permeability. (*Id.*) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect such disclosure. (*Id.*)

5. Claim 15

a) The method of claim 1 further forming at least one of the first and second conductor layers from a thermally conductive material.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶87.) Partovi discloses that layers 357 (including "the first conductor layer" and "the second conductor layer") "can be made of copper material," which is thermally conductive. (*Id.*; Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1011 at ¶[0039] (describing copper as "thermally conductive material"); Ex. 1013 at 4:37-39 (disclosing copper has "having a high thermal conductivity").) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect such disclosure.

6. Claim 16

a) The method of claim 1 further providing the connector comprising at least one of a via, a solder, a tab, a wire, a pin, a rivet, a filled mesh structure, a conductive polymer, a conductive composite, a conductive adhesive, a liquid metal, or a foamed metal.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶88.) For example, as discussed above in Section IX.A.1(c), the combination discloses connecting the "first conductor layer" and the "second conductor layer" with least two connectors. (*See supra* Section IX.A.1(c).) Furthermore, the combination discloses using vias and/or solder as the connectors.

(Ex. 1023 at 6:45-50; Ex. 1009, ¶[0224] (disclosing "separate PCB layers 357 . . . are then connected . . . for example by use of a via or contacts").) Accordingly, the Partovi-Chiang combination discloses claim 16. (Ex. 1002, ¶88.)

7. Claim 17

a) The method of claim 1 further providing at least two connectors electrically connecting the first conductor layer and the second conductor layer in parallel.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶89-90.) As discussed above with respect to claim element 1[c], in the Partovi-Chiang combination, connector 358 connecting the top two PCB layers 357 ("the first conductor layer and the second conductor layer") in figure 18 of Partovi could have been implemented using at least two connectors (like plated through holes 315 and 317 in Chiang) to connect the two PCB layers in parallel. (*Supra* Section IX.A.1(c).) Therefore, the Partovi-Chiang combination discloses or suggests "providing at least two connectors electrically connecting the first conductor layer and the second conductor layer in parallel." (Ex. 1002, ¶89.)

To the extent claim 17 is interpreted such that the "at least two connectors" recited in claim 17 are different from the "at least two connectors" in claim 1, the Partovi-Chiang combination discloses or suggest such a feature. Specifically, each of the plated through holes 315 and 317 in Chiang "is preferably formed using **a large number of plated micro-vias** to increase conductivity of the conductor

formed between the conductive traces on adjacent layers of PCB 322." (Ex. 1023 at 6:45-50.) Therefore, each plated hole has at least two micro-vias. Accordingly, there are a total of at least four micro-vias between the two plated through holes 315 and 317. (Ex. 1002, ¶90.) As such, two of those four micro-vias would correspond to the "at least two connectors" in claim 1 and the other two would correspond to the "at least two connectors" in claim 17. (*Id.*)

8. Claim 18

a) The method of claim 1 further forming a structure in which the first and second conductor layers are positioned in about a parallel orientation, a perpendicular, or at an angular relationship therebetween.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶91-92.) For example, Partovi discloses with reference to figure 18 that an inductor of high flux density is formed by stacking multiple coils in layers 357 (including "the first and second conductor layers") that are separate and spaced apart from each other. (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18.) The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect such disclosure. Thus, a POSITA would have understood that PCB layers 357 are positioned "in about a parallel orientation, about perpendicular, or at an angular relationship with respect to each other." (Ex. 1002, ¶¶91-92.)

9. Claim 19

a) The method of claim 1 further providing a third conductor layer and a fourth conductor layer electrically connected in parallel wherein the first and second conductor layers are connected electrically in parallel and are further connected electrically in series with the third and fourth conductor layer.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶93-101.) As shown below, the bottom two PCB layers in Partovi's PCB coil 356 constitute a "third conductor layer" and a "fourth conductor layer," and they are electrically connected by a connector 358. (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18; Ex. 1002, ¶93.)

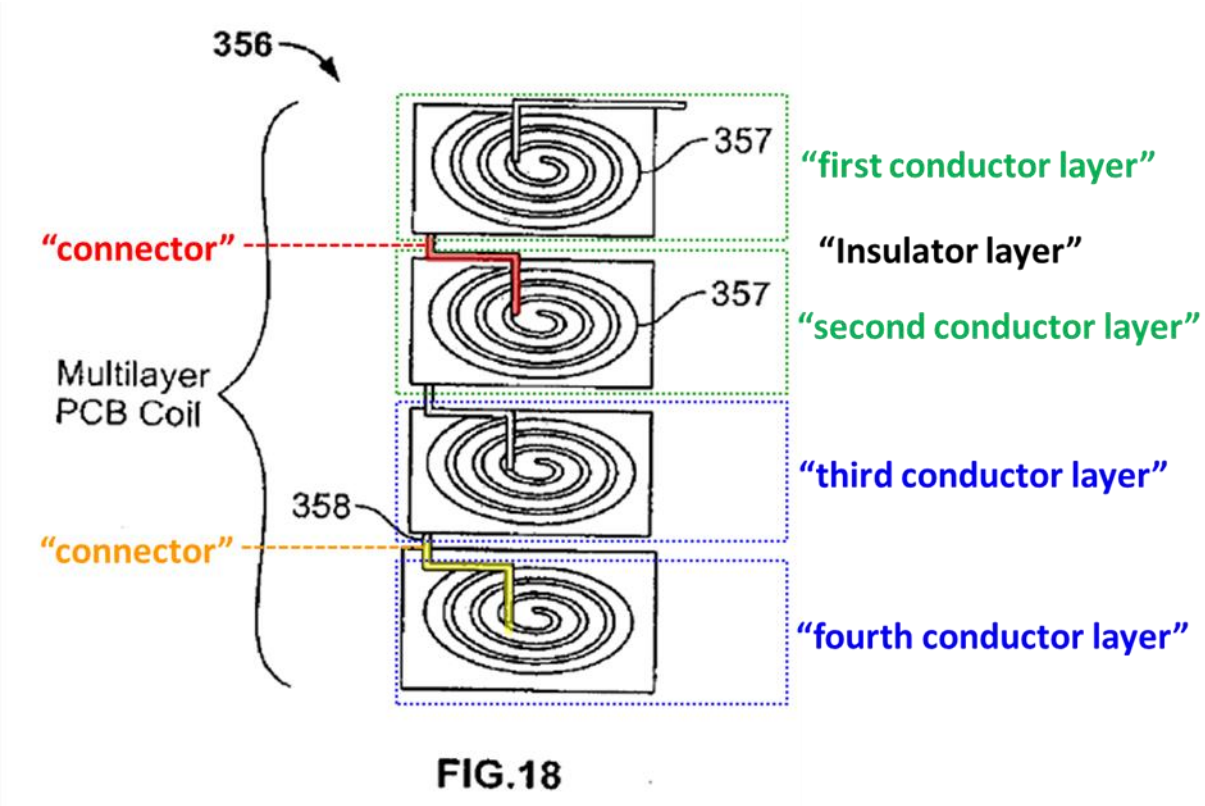


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶93.)

Partovi, however, does not explicitly disclose that the connector 358 connects the third and fourth conductor layers *in parallel*. (Ex. 1002, ¶94.) Chiang, however, discloses a third and a fourth conductor layer that are connected in parallel. (*Id.*) For example, as shown in figure 3 above, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023 at FIG. 3, 7:5-14; *see also id.* at FIG. 5.)

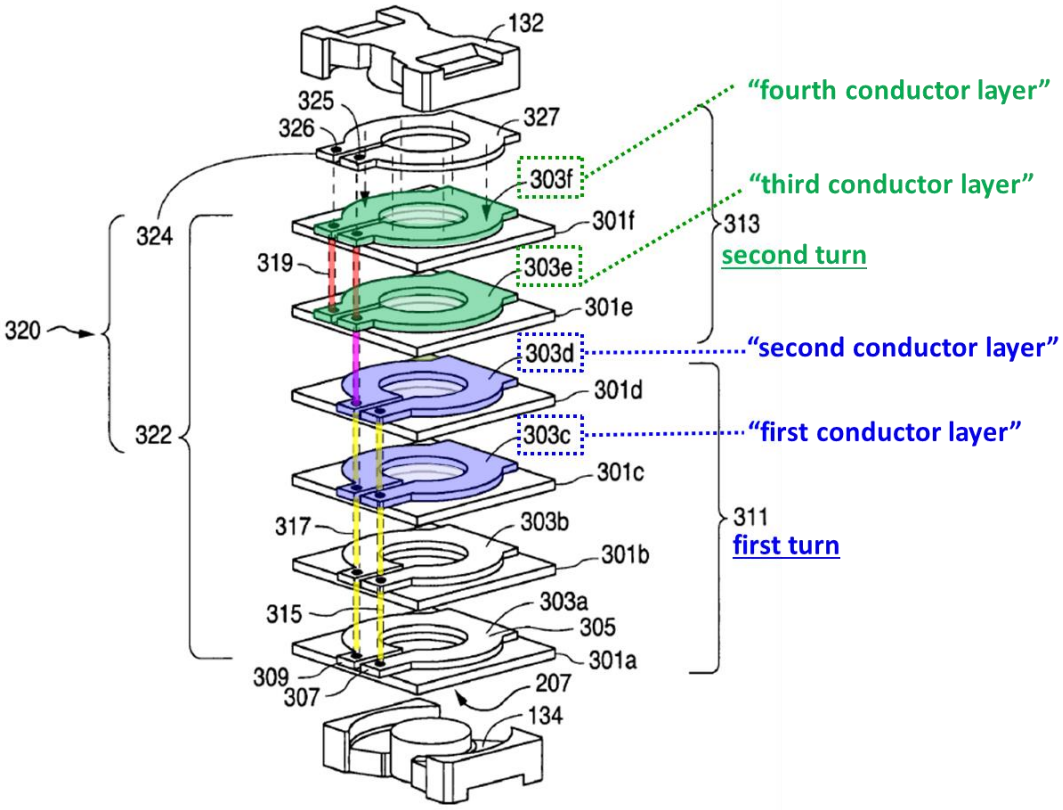


FIG. 3

(Ex. 1023 at FIG. 3 (annotated); Ex. 1002, ¶94.) Therefore, Chiang discloses "providing a third conductor layer and a fourth conductor layer electrically connected in parallel wherein the first and second conductor layers are connected electrically in parallel."

As discussed above in Section IX.A.1(c), a POSITA would have found it obvious to connect two PCB layers 357 ("the first conductor layer and the second conductor layer") in parallel to reduce series resistance of the inductor in view of the disclosure of Chiang, e.g., figure 3, reproduced above. (*See supra* Section

IX.A.1(c).) For similar reasons, a POSITA would have found it obvious to connect the bottom two PCB layers 357 (corresponding to the "third conductor layer" and the "fourth conductor layer") in figure 18 of Partovi in parallel. (*Id.*; Ex. 1002, ¶95.)

Accordingly, the Partovi-Chiang combination discloses or suggests "further providing a third conductor layer and a fourth conductor layer electrically connected in parallel wherein the first and second conductor layers are connected electrically in parallel." The Partovi-Chiang combination thus far may be illustrated as follows:

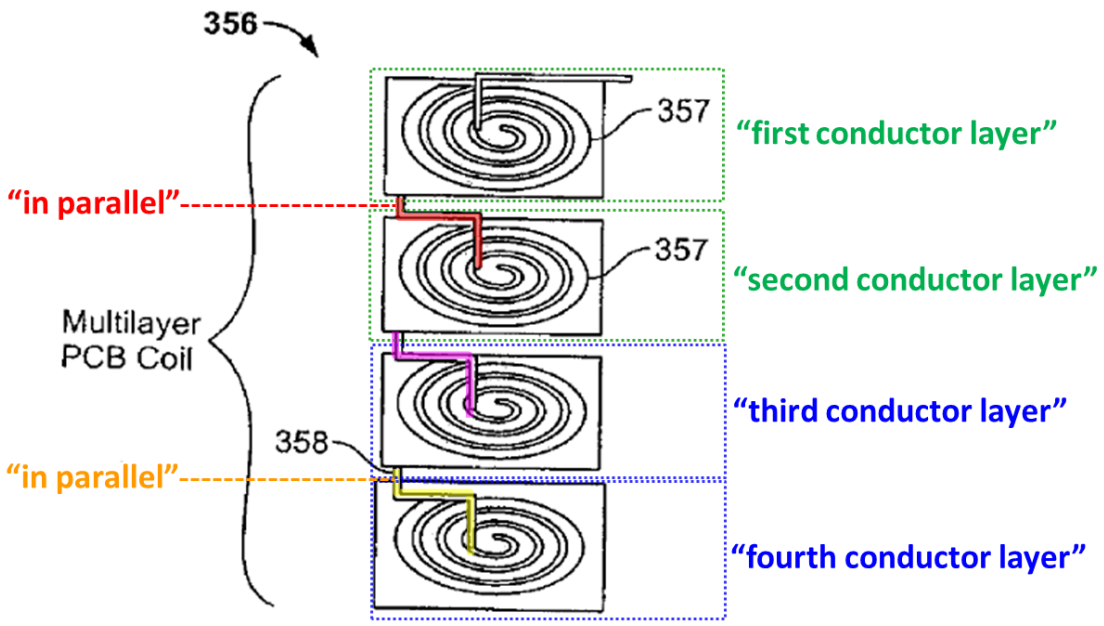


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶96.) As seen in the demonstrative above, the first and second conductor layers are connected in parallel, and the third and fourth

conductor layers are connected in parallel. As also seen in the above demonstrative, the first and second conductor layers are connected with the third and fourth conductor layers through a connector (highlighted in pink). Partovi does not explicitly disclose that the connector (pink) implements a series connection. (Ex. 1002, ¶96.)

However, a POSITA would have found it obvious to implement the connector (pink) as a series connection. (Ex. 1002, ¶97.) As explained below, a POSITA would have done so in order to increase the inductance of the inductor coil. (*Id.*)

Partovi discloses that the inductance of a coil increases with the number of turns. (Ex. 1009, ¶¶[0250]-[0254] (showing that inductance L is proportional to number of turns N).) Partovi further discloses that "a larger induction" may be created by "stacking a number of coils vertically and **connecting them in series**." (*Id*. at ¶[0255].) But Partovi recognizes that a balanced approach is needed between the number of turns and the number of layers that are connected in parallel. For example, Partovi explains that if coils are connected in series, the inductance increases because the number of turns increases, but such a series connection also results in an increase in the resistance. (Ex. 1009, ¶[0255].) In view of the above, a POSITA would have for example, connected the top two layers 357 ("first and second conductor layers") in parallel to form a first turn; and

connected the bottom two layers 357 ("the third and fourth conductor layer") also in parallel to form a second turns to reduce the series resistance of each of the turns. (Ex. 1002, ¶98.) Additionally, to increase inductance of the inductor, such a person would have connected the two turns in series, to form a winding inductor of multiple turns, each turn having multiple layers. (*Id.*)

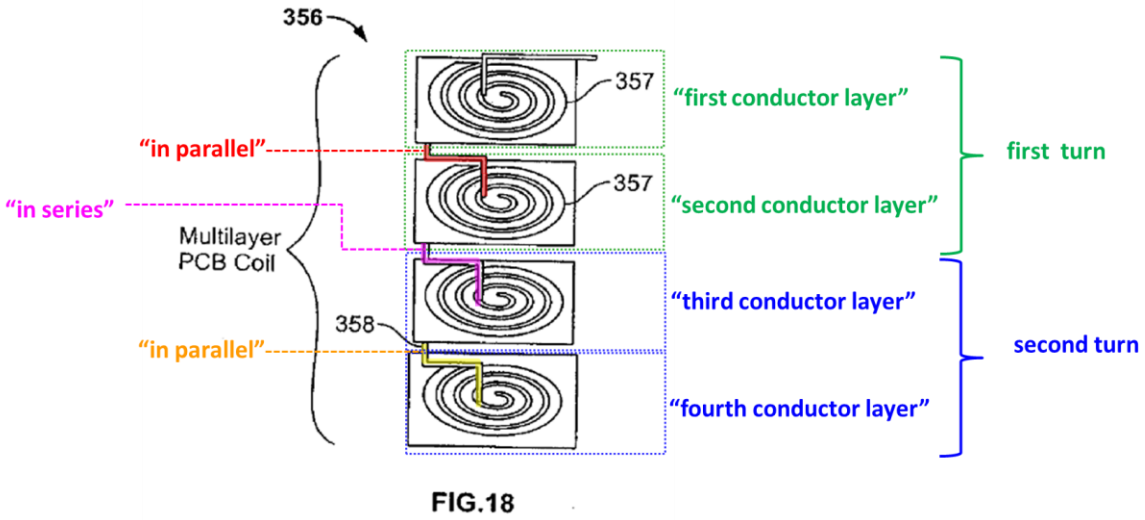


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶98.)

Such an approach is consistent with Chiang's disclosure where two turns are created by stacking conducting layers in parallel. (Ex. 1002, ¶99.) For example, as shown in figure 3 above, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023 at FIG. 3, 7:5-14; *see also id.* at FIG. 5.) The two turns are connected in series because only a single through hole connects the two turns when

two through holes connect the layers that are connected in parallel. (*See id.* at FIG. 3 below.)

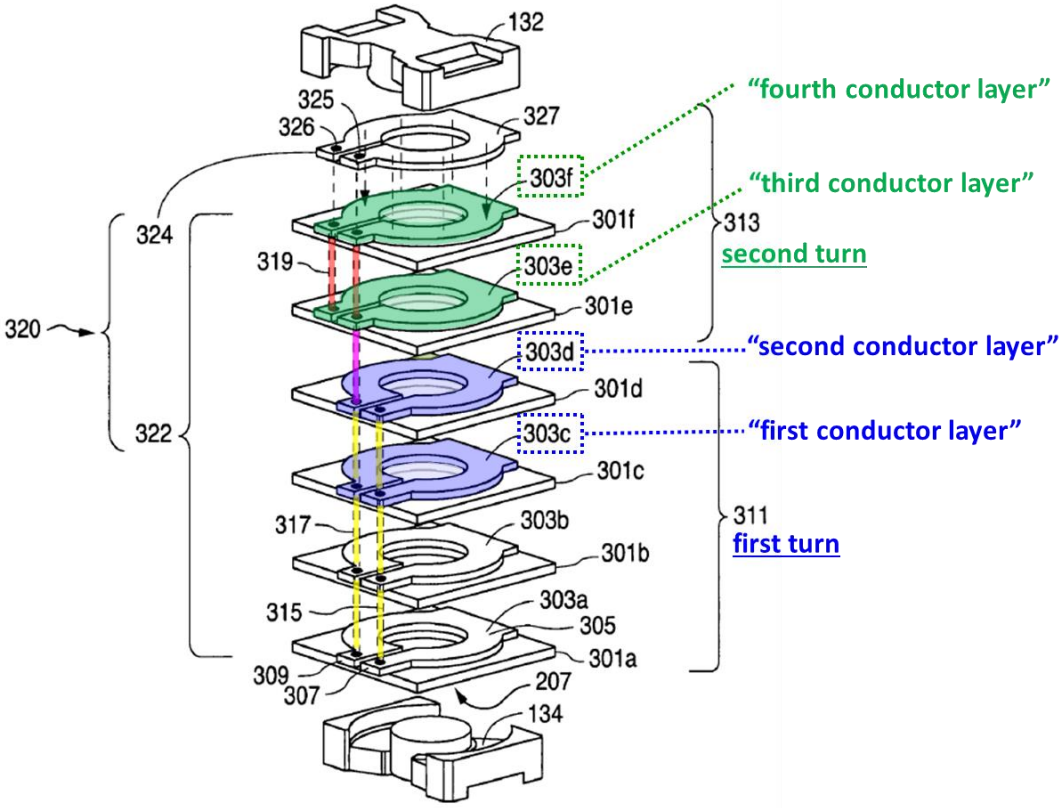


FIG. 3

(Ex. 1023 at FIG. 3 (annotated); Ex. 1002, ¶99.)

As such, based on the teachings of Partovi and Chiang, a POSITA would have been motivated to take a balanced approach, i.e., to include additional turn(s) in an inductor winding to **increase inductance**, while having the added turns be constructed with layers connected in parallel to **reduce series resistance**. (Ex. 1002, ¶100.) And, based on those disclosures, such a skilled person would have

found it obvious to connect the top two PCB layers 357 in parallel, connect the bottom two PCB layers 357 in parallel, and implement a series connection between them. (*Id.*) *See KSR*, 550 U.S. at 416.

Accordingly, the Partovi-Chiang combination discloses or suggests claim 19. (Ex. 1002, ¶101.)

10. Claim 20

a) The method of claim 1 further connecting the inductor electrically within an electrical circuit operating at about 100 kHz or greater.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶102-105.) As discussed above, the figure 2 circuit of Partovi includes a primary coil 116, which is an inductor. (*Supra* Section IX.A.1(preamble).) By switching switch 126 at a certain frequency, an alternating current flows through coil 116, which in turn generates an alternating magnetic field. (*Id.*; Ex. 1009, ¶¶[0117]-[0118]; *see also id*. at ¶¶[0013], [0091], [0119].)

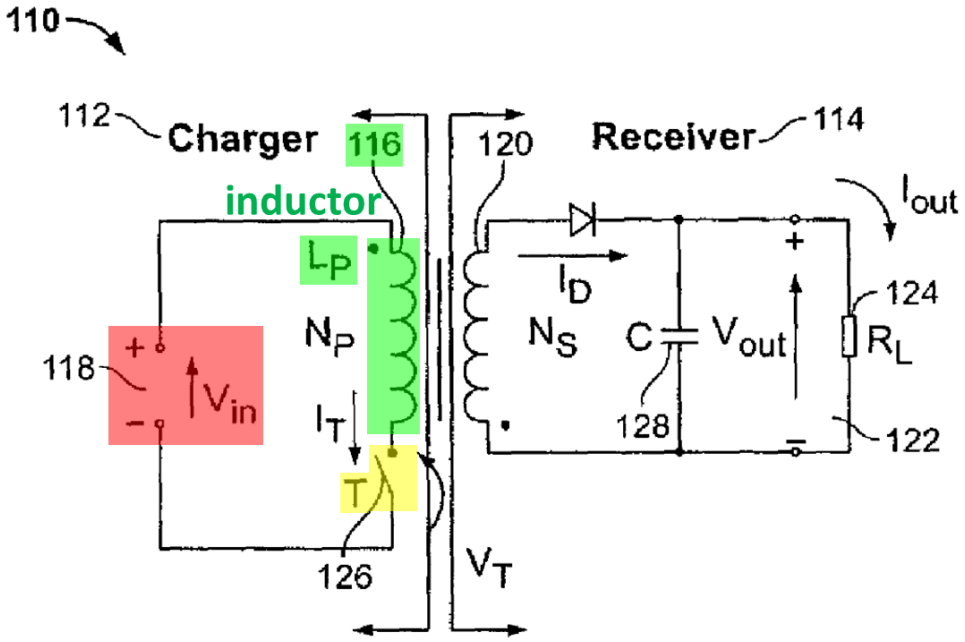


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶102.)

While Partovi discloses that switch 126 "can be a MOSFET or other switching mechanism" and that the duty cycle or frequency of the switch can be changed (Ex. 1009, ¶¶[0117], [0119]), figure 2 of Partovi does not explicitly disclose the circuitry that controls the switch 126 and changes its duty cycle or frequency. (Ex. 1002, ¶103.) But that is understandable because figure 2 of Partovi simply "shows the main components of a typical inductive power transfer system 110" and "[t]he circuit illustrated is used to illustrate the principle of inductive power transfer and is not meant to be limiting to an embodiment." (Ex. 1009, ¶[0117].) The description in Partovi following the discussion of figure 2

includes various implementations of inductive power transfer systems that build on the principle of inductive power transfer illustrated with reference to figure 2 and disclose circuitry for controlling the switch. (*See, e.g., id.* at ¶¶[0177] (disclosing with reference to figure 10 that the switch is a field effect transistor (FET) driven by a driver circuit that is controlled by a micro control unit such that the "circuit in FIG. 2 . . . [is] tuned to operate a 1.3 MHz"), [0261] (disclosing with reference to figure 28 "a more sophisticated charger or power supply" that includes several components of the charger in figure 10 and allows the charger and the receiver to communicate wirelessly.)

In particular, figure 28 discloses one implementation of the inductive power transfer circuit of figure 2 where there is an inductive power transfer between the primary coil in the charger and the secondary coil in the receiver. (Ex. 1002, ¶104; Ex. 1009, ¶¶[0260], [0261].)

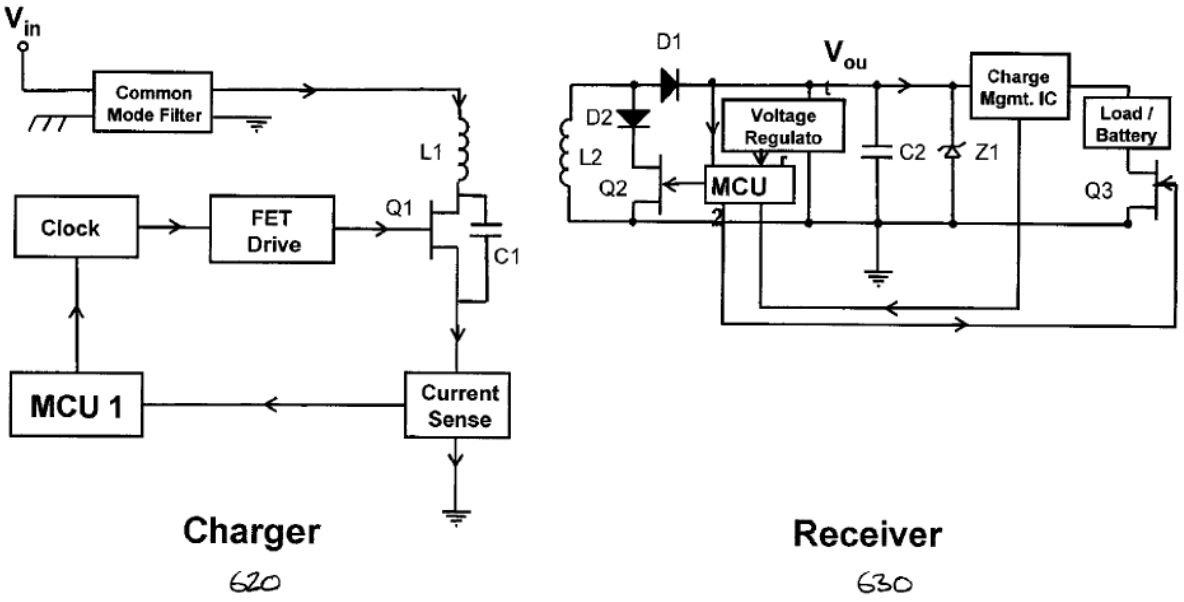
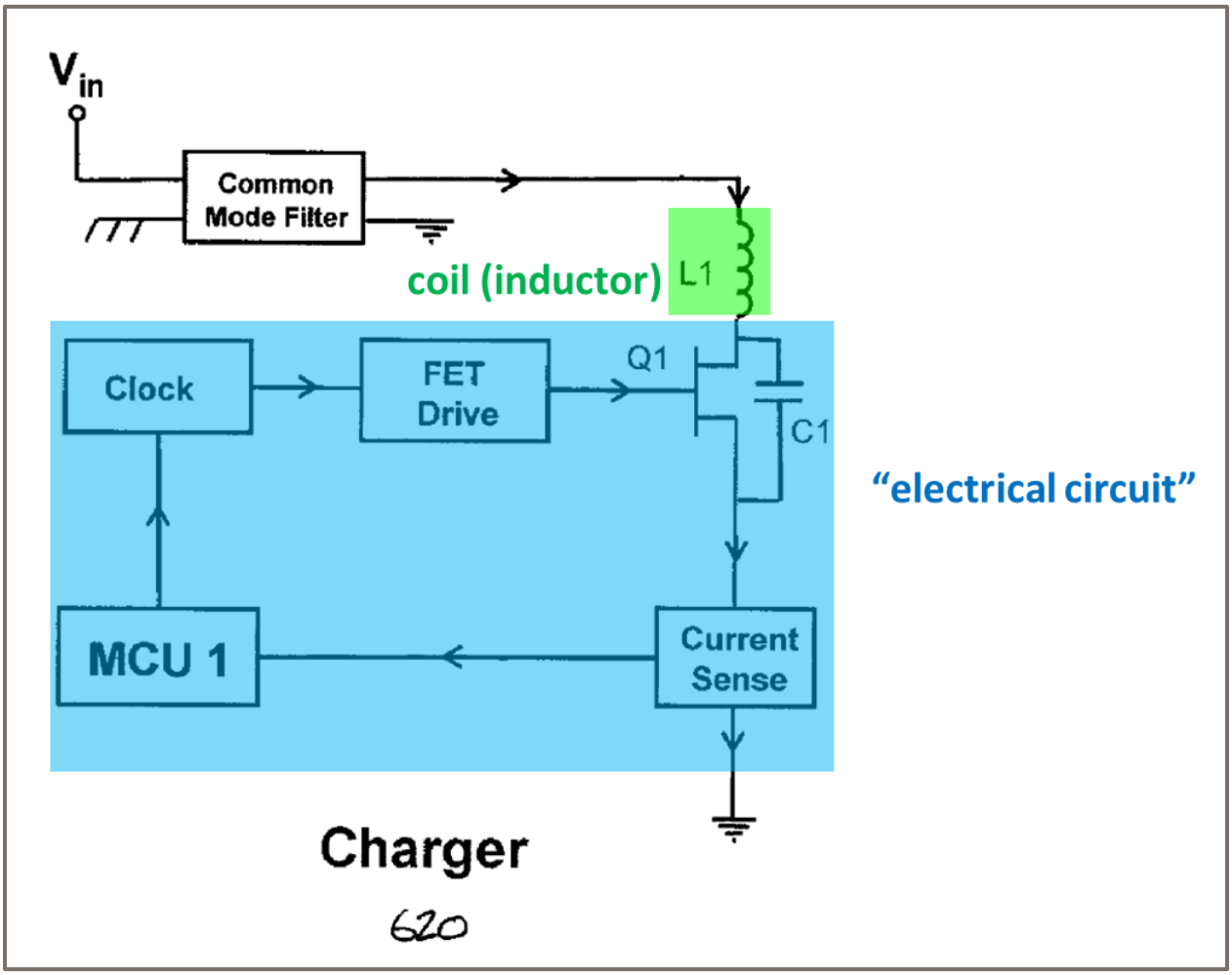


Figure 28

(Ex. 1009, FIG. 28.) A POSITA would have understood that coil L1 and FET Q1 correspond to the primary coil Lp 116 and switch 126, respectively, in figure 2 of Partovi. (Ex. 1002, ¶104; *see e.g., id.* at ¶[0117] (disclosing that switch 126 in figure 2 "can be a MOSFET or other switching mechanism").)

As shown below, the coil L1 ("inductor") is electrically connectable with an electrical circuit comprising FET Q1, capacitor C1, current sense circuit, MCU 1 (micro control unit), clock, and FET Drive circuit operating at 1.2-1.4 MHz ("electrical circuit operating at about 100 kHz or greater") where MCU1 controls the frequency of FET Q1 by controlling the clock to FET drive. (Ex. 1009, FIG. 28, ¶¶[0263]-[0265].) This is consistent with Partovi's earlier disclosure that the "circuit in FIG. 2 . . . [is] tuned to operate a 1.3 MHz." (*Id.* at ¶[0177].)

Furthermore, Partovi discloses that MCU1 receives signals from a Current Sensor that is connected "in series with the coil" ("inductor"). (*Id.*; *see also id.* at ¶¶[0261]-[0270] (disclosing with reference to figure 28 a circuit for controlling output power of the charger).)



(Ex. 1009, FIG. 28 (annotated); Ex. 1002, ¶105.) Accordingly, the Partovi-Chiang combination discloses or suggests that "the inductor is electrically connectable with an electrical circuit operating at about 100 kHz or greater." (Ex. 1002, ¶105.)

The modification of Partovi in view of Chiang discussed above in Section IX.A.1(c) does not affect Partovi's disclosure of this limitation.

11. Claim 21

a) The method of claim 20 further selecting the electrical circuit from the group consisting of a mixer circuit, an impedance matching circuit, an upconverting mixer circuit, a downconverting mixer circuit, a modulator, a demodulator, a synthesizing circuit, a PLL synthesizing circuit, an amplifying circuit, an electrical driver circuit, an electrical detecting circuit, an RF log detector, an RF RMS detector, an electrical transceiver, a power controller, and combinations thereof.

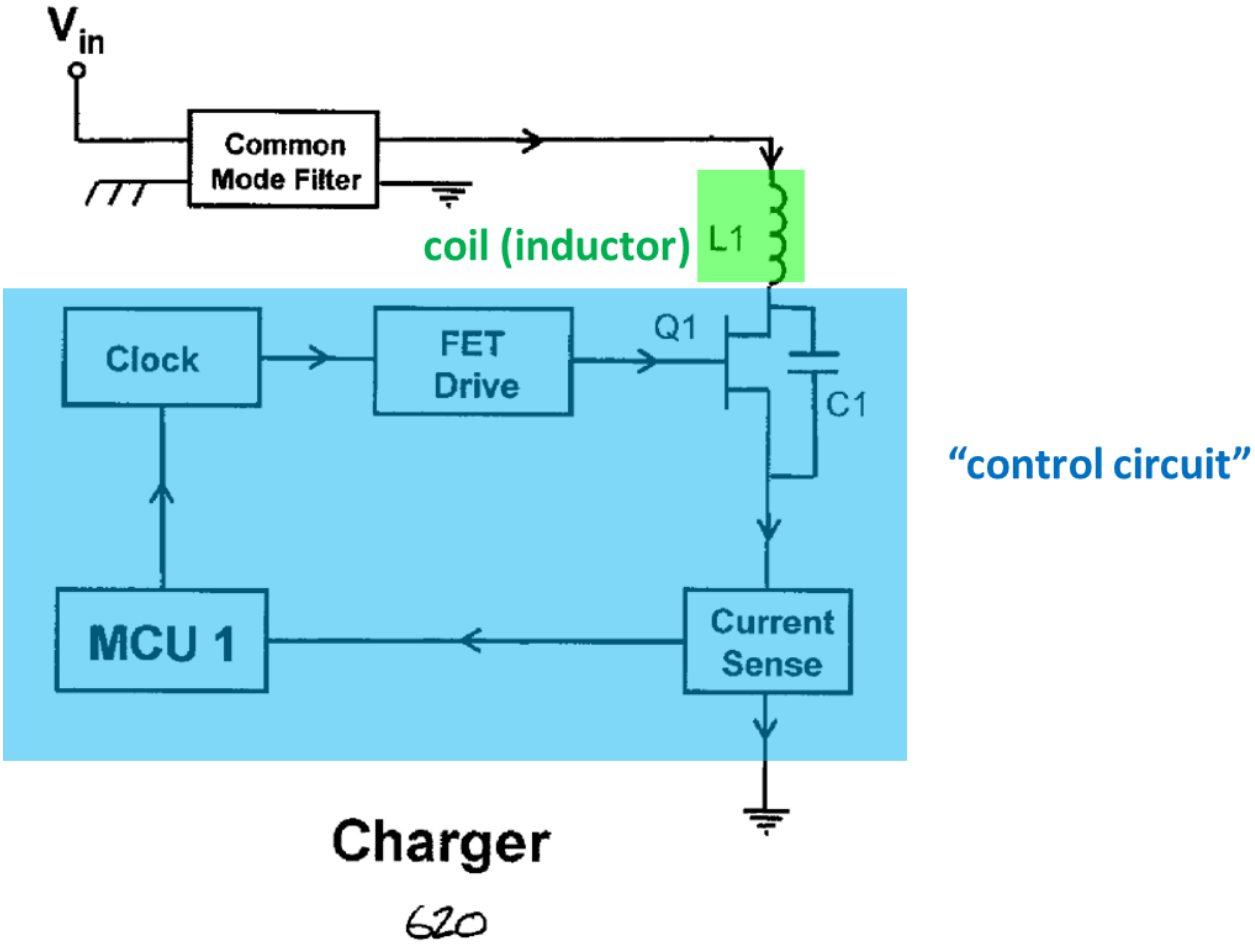
The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶106.) For example, as discussed above for claim 20, the electrical circuit includes a FET drive ("electrical driver circuit") driving FET switch Q1, a current sense circuit ("electrical detecting circuit"), and a controller being a combination of MCU 1 and clock ("power controller"). (*See supra* Section IX.A.10; Ex. 1009, ¶¶[0261]-[0265].)

12. Claim 23

a) The method of claim 1 further connecting a control circuit electrically with the inductor.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶107.) As discussed above, figure 28 discloses a particular implementation of the circuit of figure 2 of Partovi. (*Supra* Section IX.A.11 (analysis for claim

21).) Figure 28 discloses "a digital control scheme," where "[t]he primary (charger or power supply) 620 is controlled by a Micro Control Unit (MCU1)." (Ex. 1009, ¶[0261].) MCU1 receives signals from a Current Sensor that is connected "in series with the coil" ("inductor"). (*Id.*; *see also id.* at ¶¶[0261]-[0270] (disclosing with reference to figure 28 a circuit for controlling output power of the charger).)



(Ex. 1009, FIG. 28 (excerpted and annotated); Ex. 1002, ¶108.)

13. Claim 24

a) The method of claim 1 further providing at least the first

and second conductor layers with at least a partial revolution.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶108.) For example, as shown in figure 18, Partovi discloses that each of the top two layers 357 ("the first and second conductors layers") of the multi-layer inductor has at least a partial revolution because they have at least three full turns. (Ex. 1009, FIG. 18; *see also id.* at ¶[0104], ¶¶[0212]-[0224].)

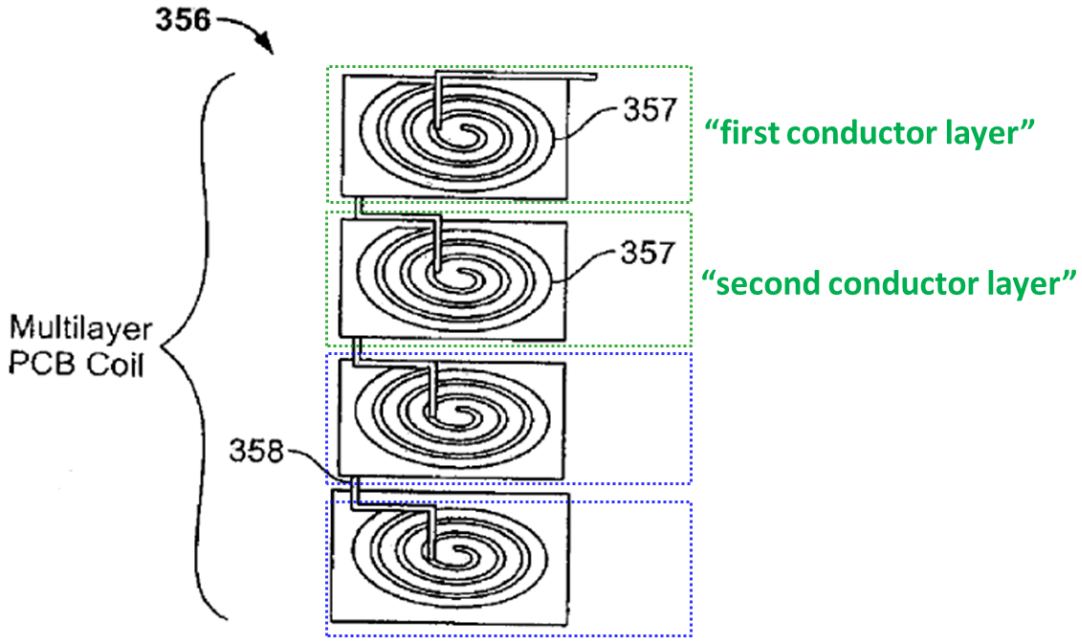


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶108.)

14. Claim 25

a) The method of claim 1 further providing the first conductor layer or the second conductor layer having a material selected from the group consisting of copper . . . .

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶109.) For example, Partovi discloses that layers 357 (including "first conductor layer" and "second conductor layer") "can be made of copper material" formed on PCB layers. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248].)

15. Claim 26

a) The method of claim 1 further forming at least one insulator layer from an electrically insulative material.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶110.) As discussed above, the Partovi-Chiang combination discloses or suggests an insulating layer between the PCB layers 357 that electrically insulates two PCB layers 357 from each other. (*Supra* Section IX.A.1(c).) Therefore, the combination discloses that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex. 1002, ¶110; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

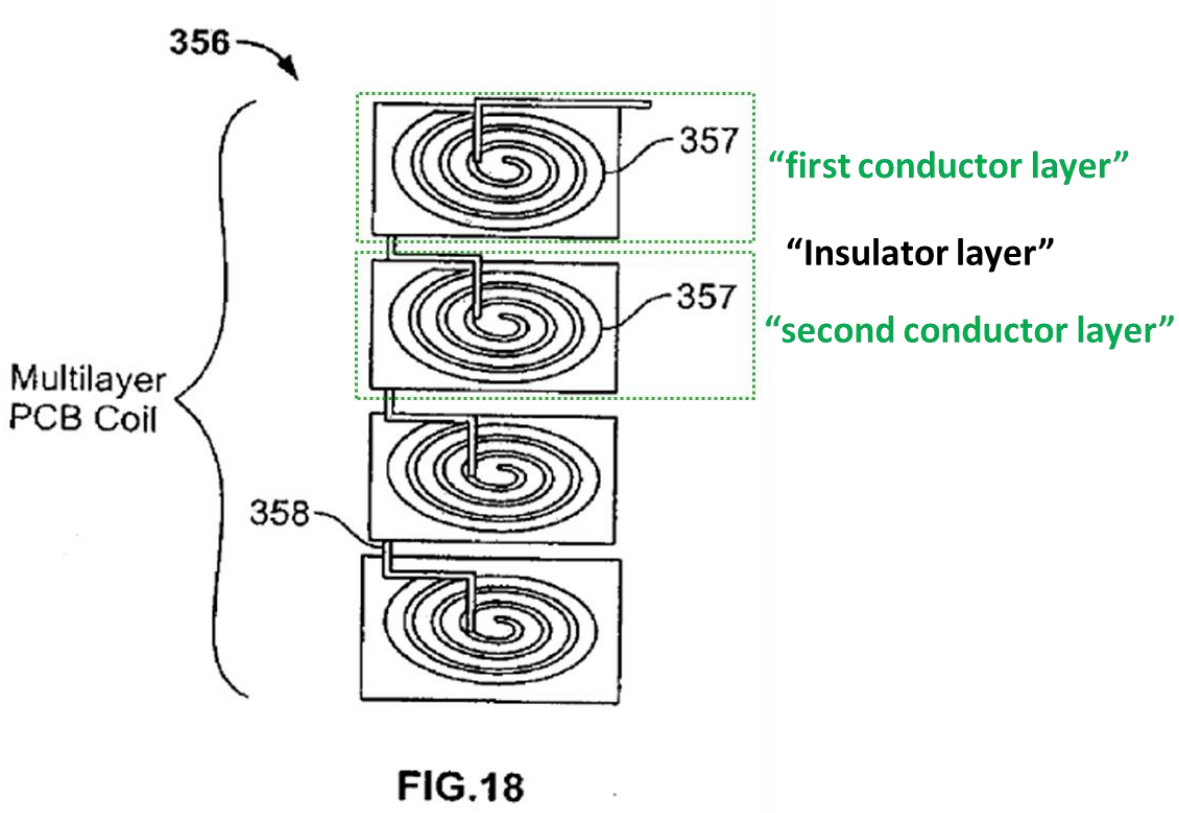


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶110.)

16. Claim 28

Preamble: A method of manufacturing an inductor structure, the method comprising the following steps:

Partovi in combination with Chiang discloses or suggests this limitation for reasons similar to those discussed above with respect to claim element 1[preamble]. (Ex. 1002, ¶111.) In particular, Partovi discloses a primary coil Lp 116 ("inductor") and as discussed below, the Partovi-Chiang combination discloses how to construct such a coil. (*See infra* Sections IX.A.16(a)-(d); Ex. 1002, ¶¶112-120.)

a) providing a first inductor subassembly comprising the

following steps:

(1) providing a first conductive conductor layer and a second conductive conductor layer spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive; positioning a first insulator layer in a space between the first conductor layer and the second conductor layers;

The Partovi-Chiang combination discloses or suggests this limitation for reasons similar to those discussed above with respect to claim elements 1(a) and (b). (*Supra* Section IX.A.1.(a)-(b); Ex. 1002 at ¶112.) In particular, the Partovi-Chiang combination discloses, as shown in figure 18 below, providing a first conductive conductor layer (top most layer 357) and a second conductive conductor layer (second layer 357) spaced apart from the first conductor layer, the first conductor layer and the second conductor layer being electrically conductive; and positioning a first insulator layer in a space between the first conductor layer and the second conductor layers. (*Id.*; *see supra* Sections IX.A.1(a)-(b).) The first and second conductor layers are "spaced apart" because a first insulator is positioned between them (*supra* Section IX.A.1(b)) and PCB layers 357 are "separate." (Ex. 1009, ¶[0224].)

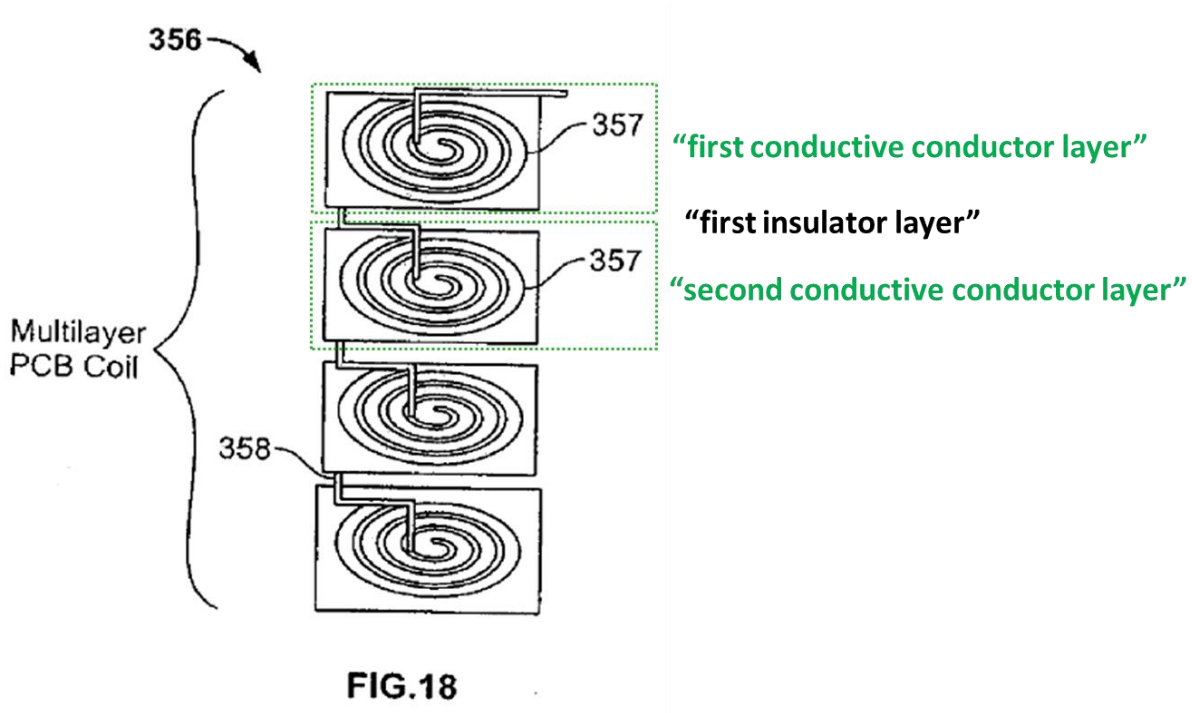


FIG.18

(*Id.* at FIG. 18 (annotated); Ex. 1002, ¶112.)

(2) connecting the first conductor layer and the second conductor layer electrically in parallel with a first connector, the first connector having a first connector electrical impedance;

The Partovi-Chiang combination discloses or suggests this limitation for reasons similar to those discussed above with respect to claim element 1(c). (*Supra* Section IX.A.1(c); Ex. 1002, ¶113.) In particular, the combination discloses, as shown in figure 18 below, connecting the first conductor layer and the second conductor layer electrically in parallel with a first connector, the first connector having a first connector electrical impedance. (*Id.*; *see supra* Section IX.A.1(c).)

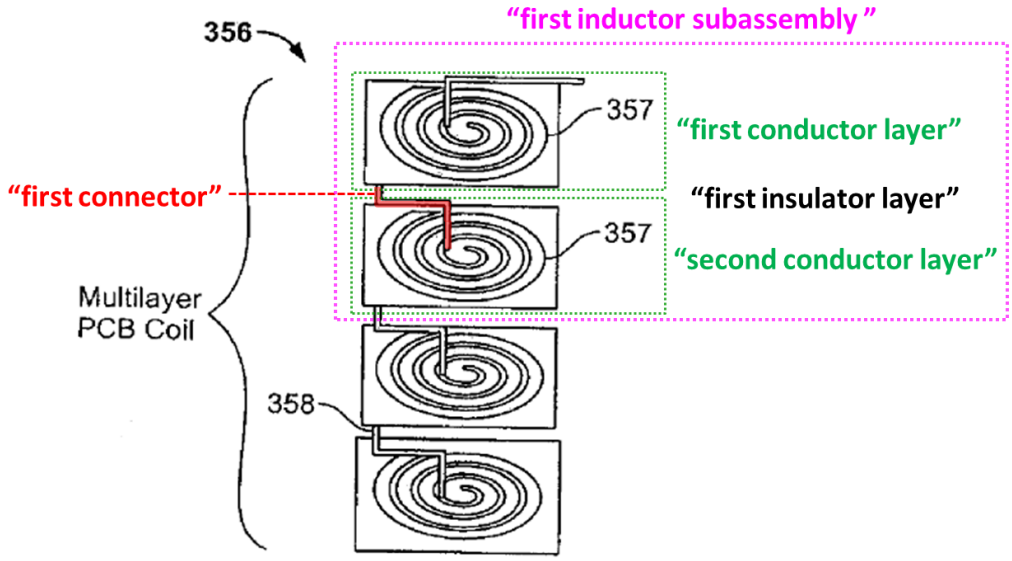


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶113.)

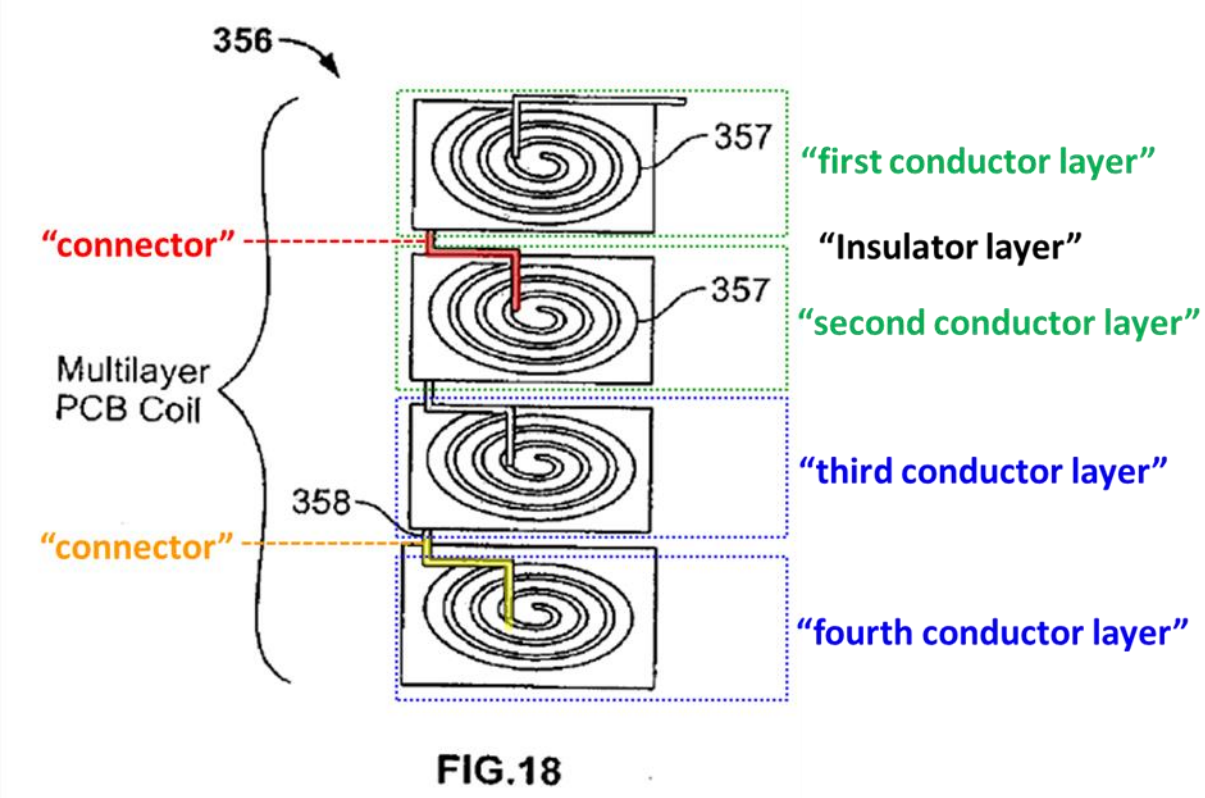
As discussed above in claim 19, the top two layers 357 ("the first conductor layer and the second conductor layer"), being connected in parallel, form a first turn ("first inductor subassembly") of the inductor. (*See supra* Section IX.A.9(a); Ex. 1002, ¶114.)

b) providing a second inductor subassembly comprising the following steps:

(1) providing a third conductor layer and a fourth conductor layer spaced apart from the third conductor layer, the third conductor layer and the fourth conductor layer being electrically conductive;

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶115.) For example, as shown in the figure 18 below, the multi-layer PCB coil 356 includes two additional layers 357 ("third conductor layer" and "fourth

conductor layer") below the disclosed "first conductor layer" and the "second conductor layer." (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18; Ex. 1002, ¶115; *see also supra* Section IX.A.9.) The layers 357 are spaced apart from each other. (Ex. 1009, ¶[0224] (disclosing that the multi-layer PCB coil 356 "is created in **separate** PCB layers 357") (emphasis added), FIG. 18).) And they are electrically conductive. (Ex. 1009, ¶[0225] (disclosing that the layers "can be made of copper material"); *see also id.* at ¶[0248]; Ex. 1002, ¶115.)



(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶115.)

(2) positioning a second insulator layer in a space between the third conductor layer and the fourth conductor layers;

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶116.) Partovi discloses that the multi-layer PCB coil 356 (including the claimed "third conductor layer" and "fourth conductor layer") "is created in **separate** PCB layers 357", which are connected by via or contacts using "common techniques used in PCB fabrication." (Ex. 1009, ¶[0224] (emphasis added).) Thus, the Partovi-Chiang combination discloses or suggests "positioning a second insulator layer in a space between the third conductor layer and the fourth conductor layers" for reasons similar to those discussed above with respect to claim element 1(b). (Ex. 1002, ¶116; *supra* Section IX.A.1(b).)

> (3) connecting the third conductor layer and the fourth conductor layer electrically in parallel with a second connector, the second connector having a second connector electrical impedance; and

The Partovi-Chiang combination discloses or suggests this limitation for reasons similar to those discussed above with respect to claim 19. (Ex. 1002, ¶117.) In particular, the Partovi-Chiang combination discloses, as shown in figure 18 below, connecting the third conductor layer and the fourth conductor layer electrically in parallel with a second connector. (*Id.*; *see supra* Section IX.A.9 (claim 19).) Furthermore, Partovi disclose that "the second connector having a second connector electrical impedance" for similar reasons discuss above in claim element 1(c).

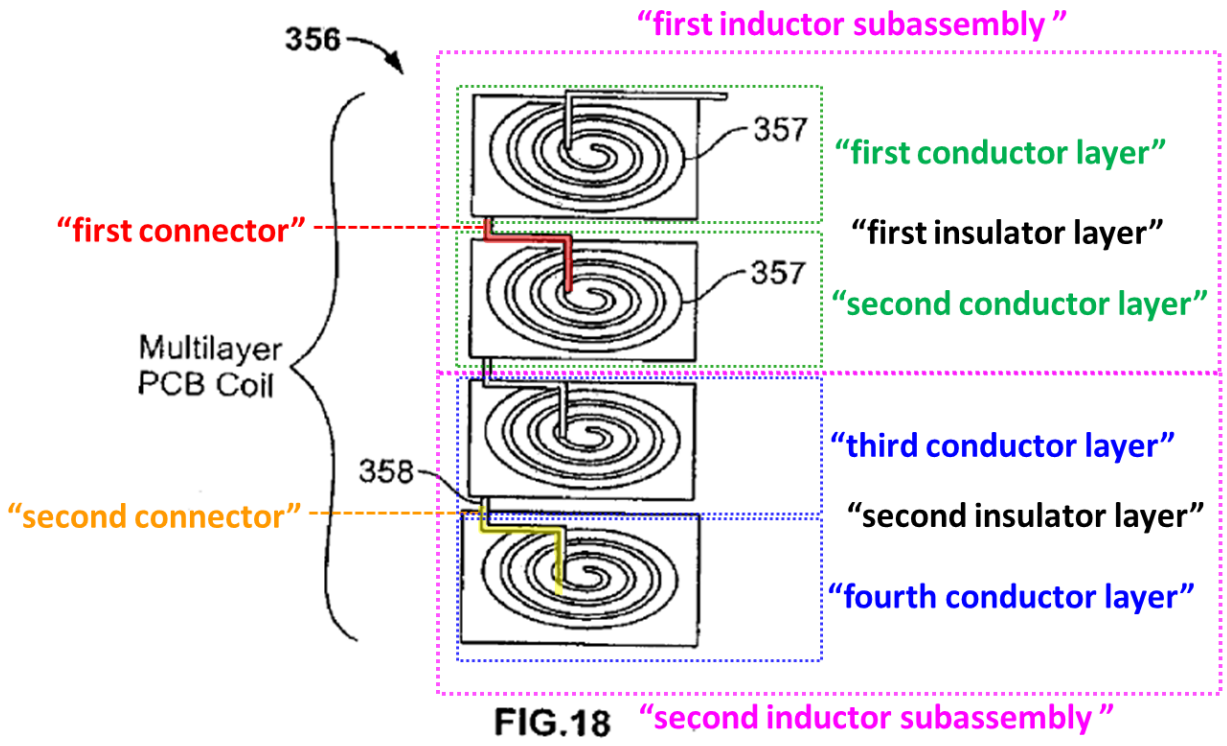


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶117.)

Moreover, as discussed above in claim 19, the bottom two layers 357 ("third conductor layer and the fourth conductor layer"), being connected in parallel, form a second turn ("second inductor subassembly") of the inductor. (*See supra* Section IX.A.9(a); Ex. 1002, ¶118.)

c) connecting the first inductor subassembly electrically in series to the second inductor subassembly;

The Partovi-Chiang combination discloses this limitation for reasons similar to those discussed above with respect to claim 19. (Ex. 1002, ¶119.) (*See supra* Section IX.A.9(a); Ex. 1002, ¶119.) Specifically, as shown below, the connector (pink) connects the two subassemblies in series. (*See supra* Section IX.A.9(a).)

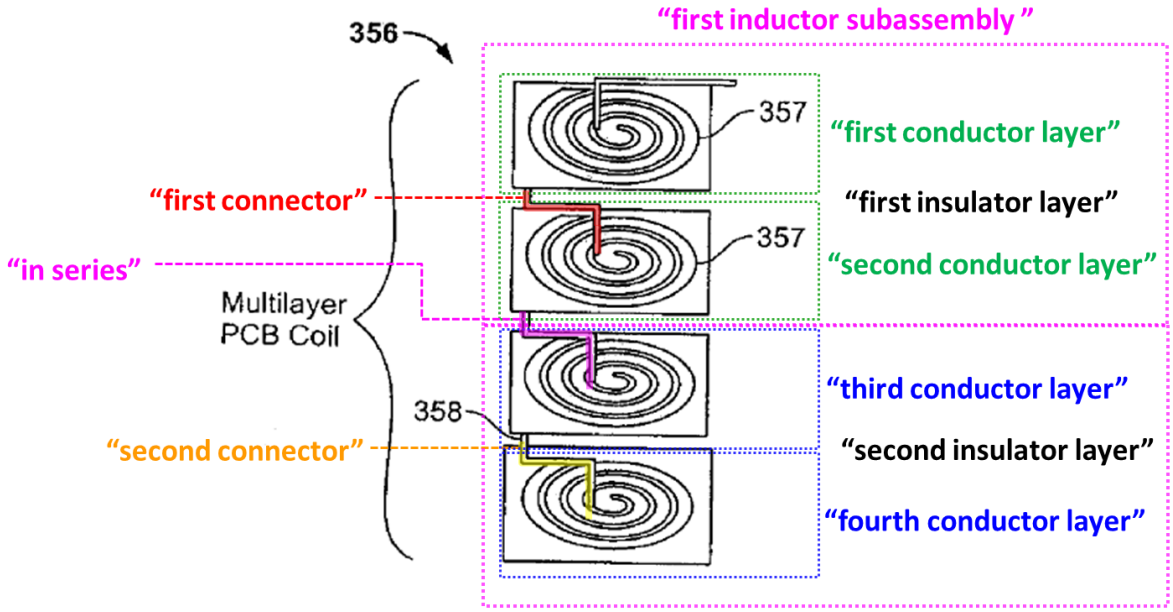


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶119.)

d) wherein when an electrical current is propagated within at least the first conductor layer, a magnetic flux is generated within the inductor when a change occurs in at least one of a frequency, a magnitude, or a waveform shape of the propagated electrical current.

The Partovi-Chiang combination discloses this limitation for reasons similar to those discussed above with respect to claim element 1(d). (*See supra* Section IX.A.1(d); Ex. 1002, ¶120.)

17. Claim 29

a) The method of claim 28 further orienting the first conductor subassembly and the second inductor subassembly such that the first and second inductor subassemblies are positioned about parallel, about perpendicular, or at an angular relationship therebetween.

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶121.) As discussed above with respect to claim 28, in the Partovi-Chiang combination, the PCB layers 357 in Partovi form the "first inductor subassembly" and the "second inductor subassembly." (*Supra* Section IX.A.16.)

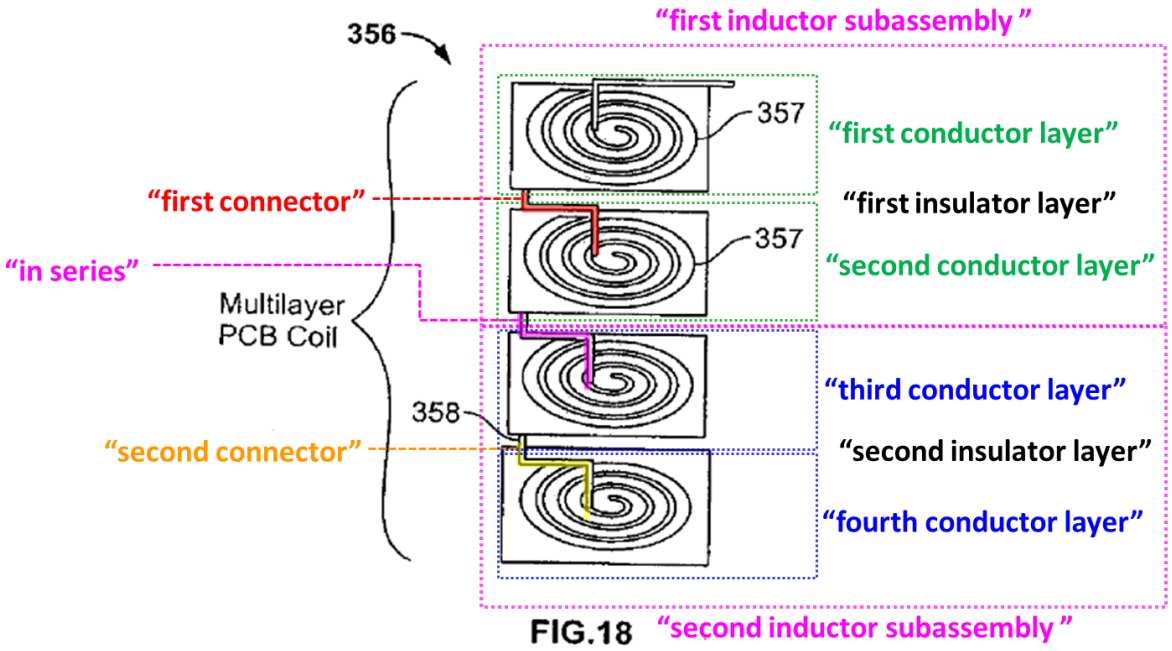


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶121.)

Because each of the PCB layers 357 are separate and spaced apart from each other, (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18), the two subassemblies are necessarily "positioned about parallel, about perpendicular, or at an angular relationship with respect to each other." (Ex. 1002, ¶122.)

B. Ground 2: Partovi in View of Chiang and Tseng Renders Obvious Claims 6, 7, and 13

1. Claim 6

a) The method of claim 1 further providing a thickness of the first conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency.

The Partovi-Chiang combination in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶¶124-128.) The Partovi-Chiang combination does not explicitly disclose that providing a thickness of the PCB layer 357 ("first conductor") ranging from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency. But Tseng discloses such a feature and it would have been obvious to implement PCB layer 357 in Partovi such that its thickness is at least two times the skin depth at a given frequency ("providing a thickness of the first conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor layer at a given frequency"). (*Id.* at ¶124.)

Similar to the Partovi-Chiang combination, Tseng generally discloses inductive power transfer system using coil inductors. (Ex. 1022 at Abstract (disclosing "a method and system for transferring power wirelessly to electronic devices," which "utilize magnetic coupling between two coils at close proximity to transfer sufficient power to charge an electronic device").) Indeed, just like the

Partovi-Chiang combination, Tseng utilizes coil inductors formed on PCBs (*id.* at 5:37-40 (using "multiple layers of coils for generation of magnetic fields") and aims to improve efficiency of power transfer (*id.* at 10:48-51 (disclosing adjusting "the switching frequency in order to maximize the efficiency of power transfer"), 11:8-14 (disclosing "the efficiency of power transfer degrades due to various losses . . . include the conductor loss in coils"); Ex. 1002, ¶125.)

Tseng further discloses that, to reduce power loss in coils due to skin depth effect, "the metal thickness should be **more than twice of the skin depth**." (Ex. 1022 at 12:3-5 (emphasis added); *see also id.* at 12:6-8 (disclosing that "substrates with a thicker metal layer can be used, or additional metal can be plated to increase the thickness"), 11:66-12:14.) As such, when implementing the multi-layer PCB coil 356 in the Partovi-Chiang combination for primary coil 116, a POSITA would have found it obvious to ensure that the thickness of each of the PCB layers 357 is at least twice the skin depth at the system's operating frequency in order to minimize conductor loss in these layers. (Ex. 1002, ¶126; *see also* Ex. 1024 at 1:34-38 (disclosing that "it has become commonplace to use a planar conductive film having a thickness on the order of **twice the skin depth** at the intended operating frequency as the magnetic components conductors.") (emphasis added).) *See Unwired Planet*, 841 F.3d at 1003.

A POSITA would have been able to make the necessary changes to the thickness of the PCB layers 357 making up the primary coil 116 based on the operating frequency. (Ex. 1002, ¶127.) For example, Partovi discloses that different sizes of copper, such as from 1 to 6 oz. (corresponding to thicknesses of from 1.4 to 8.2 mil), can be used to optimize the inductive circuit for a particular application. (Ex. 1009, ¶[0167] (disclosing that "Most common PCBs use 1-2 oz copper PCBs" and "the coil PCB used for the wireless charger can be made from PCBs clad with between 2 and 4, or even 6 oz copper"); *see also id.* at ¶[0212].)

A POSITA would have understood that implementing the claimed feature would have involved no more than applying a known technique to a known device to yield a predictable result (e.g., designing and implementing a conductor based on the skin depth at a certain operating frequency). (Ex. 1002, ¶128.) *See KSR*, 550 U.S. at 416.

2. Claim 7

a) The method of claim 1 further providing a thickness of the second conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the second conductor layer at a given frequency.

The Partovi-Chiang combination in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶129.) For example, the Partovi-Chiang-Tseng system discloses or suggests implementing PCB layers 357 in Partovi such that the thickness of the layers 357 (including "second conductor layer") is about twice of

the skin depth at a given frequency for similar reasons as discussed above in claim 6. (*See supra* Sections IX.B.1 (analysis for claim 6), IX.A.1(b) (one of PCB layers 357 is a "second conductor layer.").)

3. Claim 13

a) The method of claim 1 further providing an inductor quality factor greater than about 5.

The Partovi-Chiang combination in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶130.) As discussed above, Partovi discloses a primary coil 116, which is an "inductor." (*Supra* Section IX.A.1(a).) But Partovi does not disclose the inductor quality factor for primary coil 116. (Ex. 1002, ¶130.) However, as discussed below, it would have been obvious to configure primary coil 116 such that it has an inductor quality factor greater than 5.

As discussed above with respect to claim 6, a POSITA would have been motivated to combine teachings of the Partovi-Chiang combination and Tseng to reduce power loss in the primary coil 116 by ensuring that the thickness of the PCB layers forming the coil is at least twice the skin depth at the system's operating frequency. (*See supra* Section IX.B.1(a) (claim 6).) Tseng further discloses a high Q value of about 100 by optimizing the spacing between the conductive traces of an inductor. (Ex. 1022 at FIG. 24, 8:1-18; Ex. 1002, ¶131.)

Based on the combined teachings of Partovi, Chiang, and Tseng, a POSITA would have had reasons to consider the teachings of Tseng when contemplating the

features disclosed by the Partovi-Chiang combination. (*Id.* at ¶132 (citing Ex. 1034).) And, based on those disclosures, such a skilled person in the art would have found it obvious to optimize the Partovi-Chiang inductor to improve its Q factor, i.e., improving efficiency or reducing power loss, in view of Tseng. (*Id.*) *See KSR*, 550 U.S. at 416.

For example, when implementing the Partovi-Chiang inductor, a POSITA would have been motivated to find ways to improve the efficiency of the inductor and Tseng discloses at least a way to do so by optimizing the spaces between conductive traces of an inductor. (Ex. 1002, ¶133.) Indeed, by increasing the width of the traces (i.e., narrowing the spaces among them), Tseng shows that the inductor's "coupling efficiency" is improved and the Q value improves from 50 to 100. (*Id.*; Ex. 1022 at FIG. 24, 8:1-18.) Furthermore, a POSITA would not have been deterred from optimizing Partovi's inductor in view of Tseng's teachings. (Ex. 1002, ¶133.) For example, Partovi discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and **coupling efficiency** for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212] (emphasis added); Ex. 1002, ¶133.)

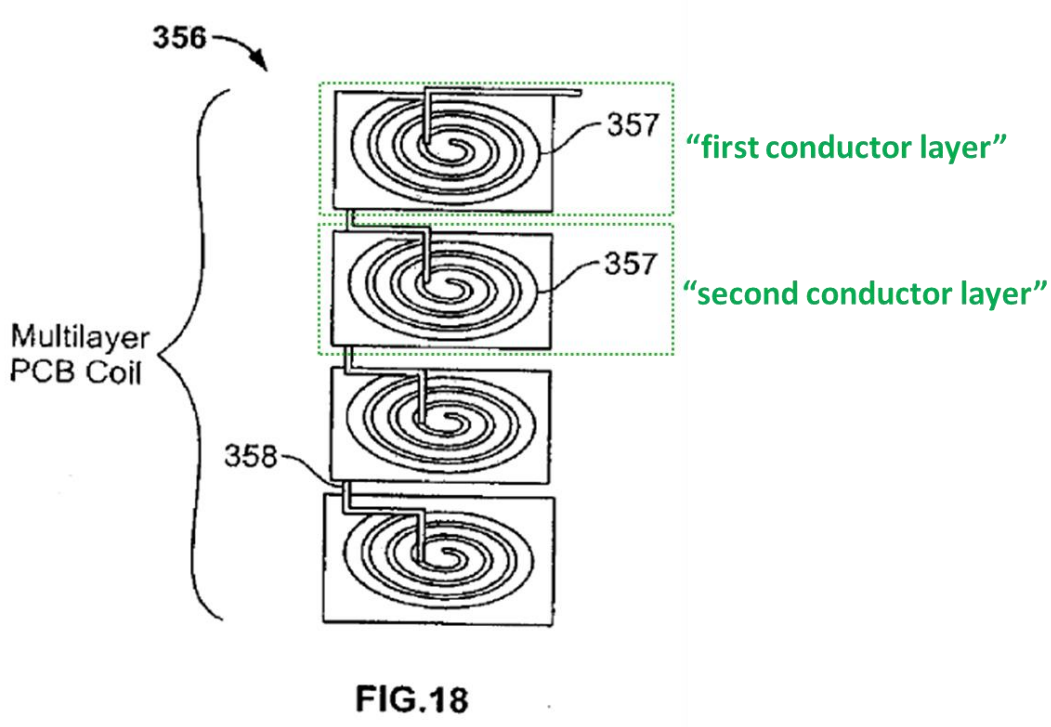
Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil and/or circuits and to combine the same. (Ex. 1002, ¶134.)

C. Ground 3: Partovi in View of Chiang and Phan Renders Obvious Claims 8, 12, 26, and 27

1. Claim 8

a) The method of claim 1 further providing a first conductor layer thickness about the same as a second conductor layer thickness.

Partovi in view of Chiang and Phan discloses or suggests this limitation. (Ex. 1002, ¶¶136-140.) As discussed above, the top two PCB layers 357 in figure 18 of Partovi correspond to the claimed "first conductor layer" and "second conductor layer." (*Supra* Section IX.A.1(a).)



(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶136.)

While Partovi does not explicitly disclose that a thickness of the PCB layers 357 is about the same, a POSITA would have found it obvious to use about the

same thickness for each of the PCB layers 357 in view of Phan ("wherein a first conductor layer thickness is about the same as a second conductor layer thickness"). (Ex. 1002, ¶137.)

For example, using two PCB layers 357 ("first conductor layer" and "second conductor layer") of the same thickness would have been obvious because there are only two choices: either using layers of the same thickness or using layers of different thickness. (*Id.*, ¶138.) Thus, choosing two PCB layers 357 of the same thickness would have been one of two choices available to a POSITA. (*Id.*) Accordingly, using layers of the same thickness would have been obvious because it would have been one of a "finite number of identified, predictable solutions." *Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1331 (Fed. Cir. 2009) (holding that a claimed step was obvious when it was one of three available choices). Indeed, there is nothing special about setting the thickness of two layers to be the same and this is evident from claims 8 and 9 of the '046 patent. (Ex. 1002, ¶138.) Specifically, while claim 8 recites that the first and second conductor layers have "about the same" thickness, claim 9 recites that the thickness of the two layers is "different." (*Id.*; Ex. 1001, claims 8, 9.)

Phan discloses a multilayer PCB stackup in figure 3 that includes six conducting layers, 302, 304, 306, 308, 310, and 312. (Ex. 1029 at 5:43-46, FIG. 3 (reproduced below).) Each of the conductor layers has the same thickness as

shown below in figure 3. (*Id.* at 5:46-48 ("each conductor layer can be made of half ounce of copper and be 0.0007 inches in thickness"); *see also id.* at Abstract, 3:55-61, 3:66-4:4, 5:43-46.)

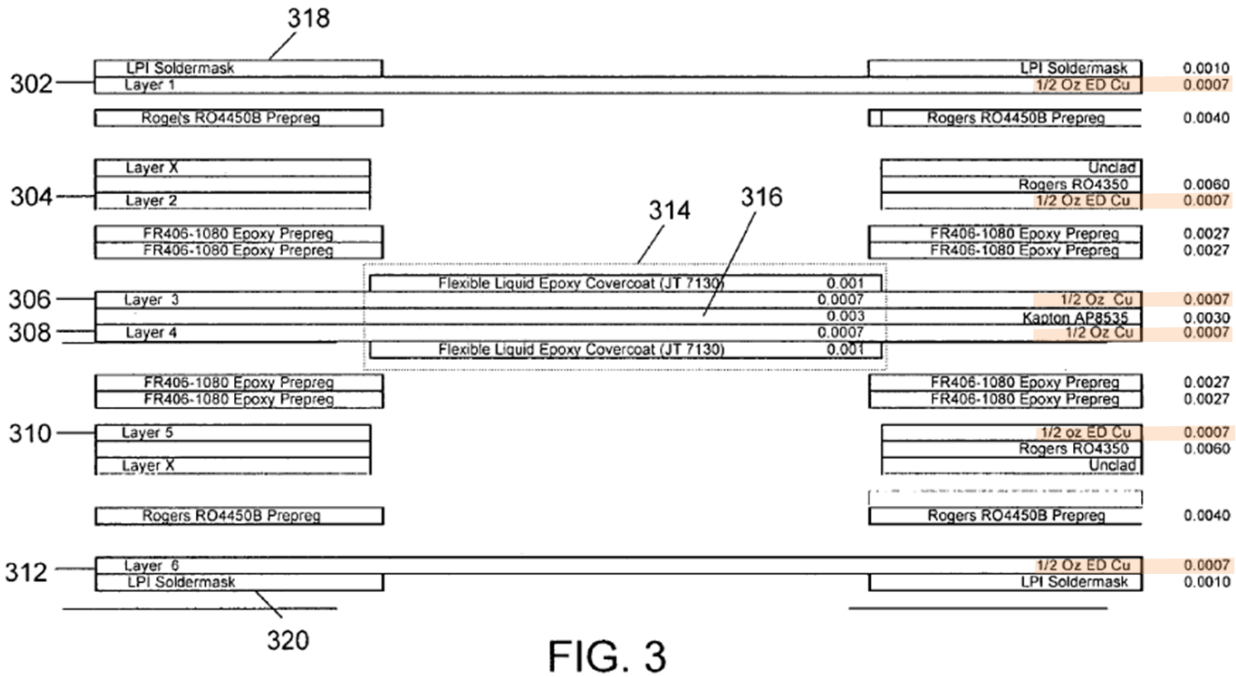


FIG. 3

(Ex. 1029 at FIG. 3 (annotated); Ex. 1002, ¶139.) Phan further explains that "[i]n one embodiment of the invention, the number of layers in [the PCBs] is six," however, in other embodiments "the number of layers . . . can be four . . . or any other number." (Ex. 1029 at 4:28:36.)

A POSITA would have the skills and knowledge to implement the PCB layers 357 in Partovi such that they were each about the same thickness. (Ex. 1002, ¶140.) Implementing Partovi's PCB layers 357 in such a manner based on the teachings of Phan would have been obvious because, as discussed above,

choosing the same thickness for the different PCB layers 357 would have been one of two choices available to a POSITA and a POSITA would have selected the same thickness to suit a POSITA's design objective. (*Id.*) In fact, implementing Partovi's PCB layers 357 to have the same or about the same thickness would have been merely the application of a known technique (e.g., using conductor layers having the same thickness) to a known device (Partovi's PCB-based inductor) according to known methods (e.g., modifying the thickness of conducting layers) to yield the predictable result of an inductor having conducting layers of the same thickness. (Ex. 1002, ¶140.) *See KSR*, 550 U.S. at 416-21. The above modification is consistent with Partovi because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212]; *see also id.*at ¶[0479]; Ex. 1002, ¶140.)

2. Claim 12

a) The method of claim 1 further providing a thickness of the insulating layer less than about 5 cm.

Partovi in view of Chiang and Phan discloses or suggests this limitation. (Ex. 1002, ¶¶141-145.) While Partovi and Chiang do not explicitly disclose a thickness of the insulating layer between PCB layers 357, a POSITA would have

found it obvious to use insulating layers each having a thickness that is less than 5 cm based on common sense and in view of Phan. (*Id.* at ¶141.)

To begin, given Partovi's objectives of providing devices that are "lightweight," "portable," and have a "compact" design, a POSITA would have been motivated to minimize the thickness of the insulating layers between the PCB layers 357 to ensure that the overall thickness of the PCB is as thin as possible. (Ex. 1009, ¶¶[0010] (disclosing that "a common problem with such inductive units is that the windings are bulky, which restricts their use in lightweight portable devices"), [0212] (disclosing "multiple layer boards can be used to allow compact fabrication"), [0224] (disclosing a need for a coil design "where small x-y coil dimensions are desired")); Ex. 1002, ¶142.) Partovi envisions such an optimization because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[212]; *see also id.* at ¶[0479]; Ex. 1002, ¶142.)

Moreover, PCBs where the insulating layer thickness was less than 5 cm were well-known. As discussed above, Phan like the Partovi-Chiang combination discloses a multi-layer PCB. (*Supra* Section IX.C.1.) Phan discloses using insulating layers of thickness on the order of thousandths of an inch (1/1000 of an

inch is 0.00254 cm) to separate PCB conductive layers ("wherein a thickness of the insulating layer is less than about 5 cm"). (Ex. 1029 at 5:40-49, FIG. 3.) For example, Phan discloses "an insulating layer 316 of Kapton" having a thickness of 0.003 inches (which is equal to 0.00762 cm) positioned between conducting layers 306 and 308. (*Id.*; Ex. 1002, ¶143.)

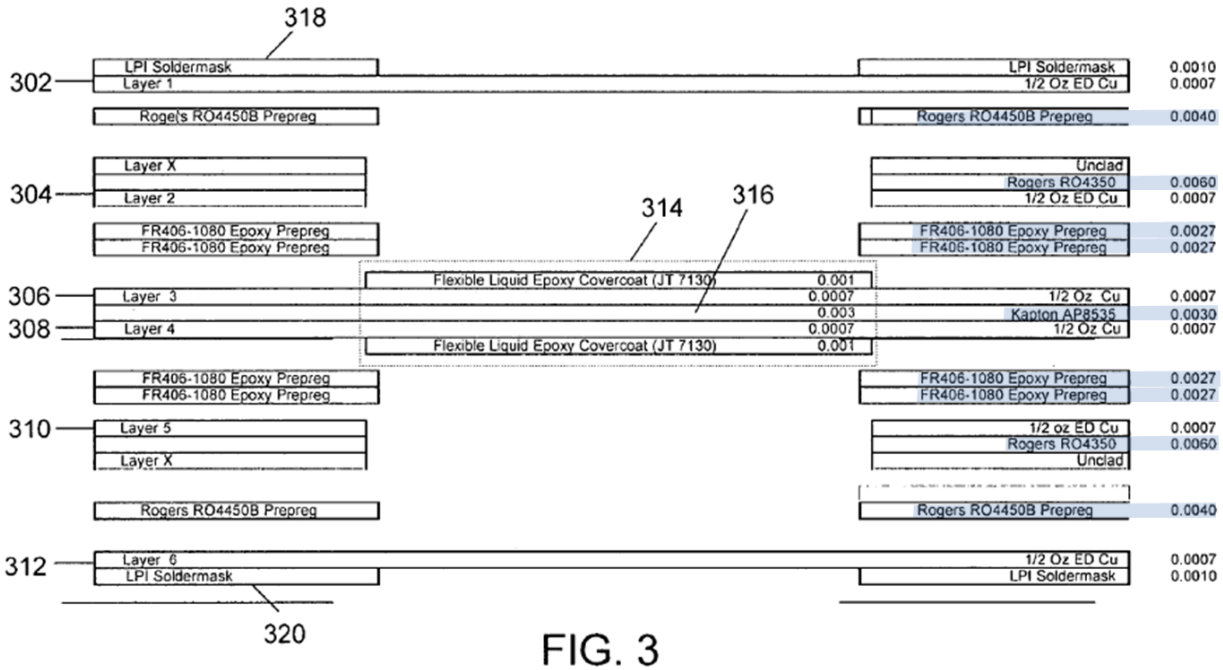


FIG. 3

(Ex. 1029 at FIG. 3 (annotated); Ex. 1002, ¶143.)

A POSITA had the skills and knowledge to design and manufacture the insulating layers in figure 18 of Partovi to be less than 5 cm given the teachings of Phan and such person's knowledge. (Ex. 1002, ¶144.) Therefore, a POSITA would have understood and appreciated that the proposed combination involved combining known prior art elements, and known technologies according to known

methods and common sense (e.g., modifying the thickness of insulating layers in Partovi's inductor to be less than 5 cm) to yield the predictable result of an inductor having insulating layers each having a thickness of less than 5 cm. . (Ex. 1002, ¶144.) *See KSR*, 550 U.S. at 416-21.

Moreover, the thickness of an insulating layer is a "result-effective variable" because it affects the overall thickness of the PCB and also determines the amount of the insulation between conducting layers on both sides of the insulating layer. (Ex. 1002, ¶145.) Therefore, if "less than 5 cm" is an optimum number for the insulating layer thickness per claim 12, claim 12 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '046 patent provides no evidence that "less than 5 cm" thickness produces a new or unexpected result, and thus the claimed range cannot form the basis of patentability. (Ex. 1002, ¶145.) *In re Boesch*, 617 F.2d at 276; *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

3. Claim 26

a) The method of claim 1 further forming at least one insulator layer from an electrically insulative material.

Partovi in view of Chiang and Phan discloses or suggests this limitation for reasons similar to that discussed below for claim 27. (Ex. 1002, ¶146; *see infra* Section IX.C.4.) In particular, as discussed below with respect to claim 27, a POSITA would have found it obvious to use an electrically insulative material like Kapton for the insulator layer.

4. Claim 27

a) The method of claim 1 further providing the insulator layer having an electrically insulative material selected from the group consisting of air, polystyrene, silicon dioxide, a biocompatible ceramic, a conductive dielectric material, a non-conductive dielectric material, a piezoelectric material, a pyroelectric material, a ferrite material, and combinations thereof.

Partovi in view of Chiang and Phan discloses or suggests this limitation. (Ex. 1002, ¶¶147-150.) As explained above, the Partovi-Chiang combination discloses or suggests an insulating layer positioned in the space between PCB layers 357. (*Supra* Section IX.A.1(c).) Therefore, the Partovi-Chiang combination discloses or suggests that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex. 1002, ¶147; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

To the extent it is argued that the Partovi-Chiang combination does not disclose such a "non-conductive dielectric material," it would have been obvious to combine the teachings of the Partovi-Chiang combination with Phan such that the insulating material in the combined Partovi-Chiang PCB is a "non-conductive dielectric material." (Ex. 1002, ¶148.)

As discussed above, Phan like the Partovi-Chiang combination discloses a multi-layer PCB. (*Supra* Section IX.C.1.) Phan discloses "an insulating layer 316 of Kapton" positioned between conducting layers 306 and 308. (Ex. 1029 at 5:40-49, FIG. 3.)

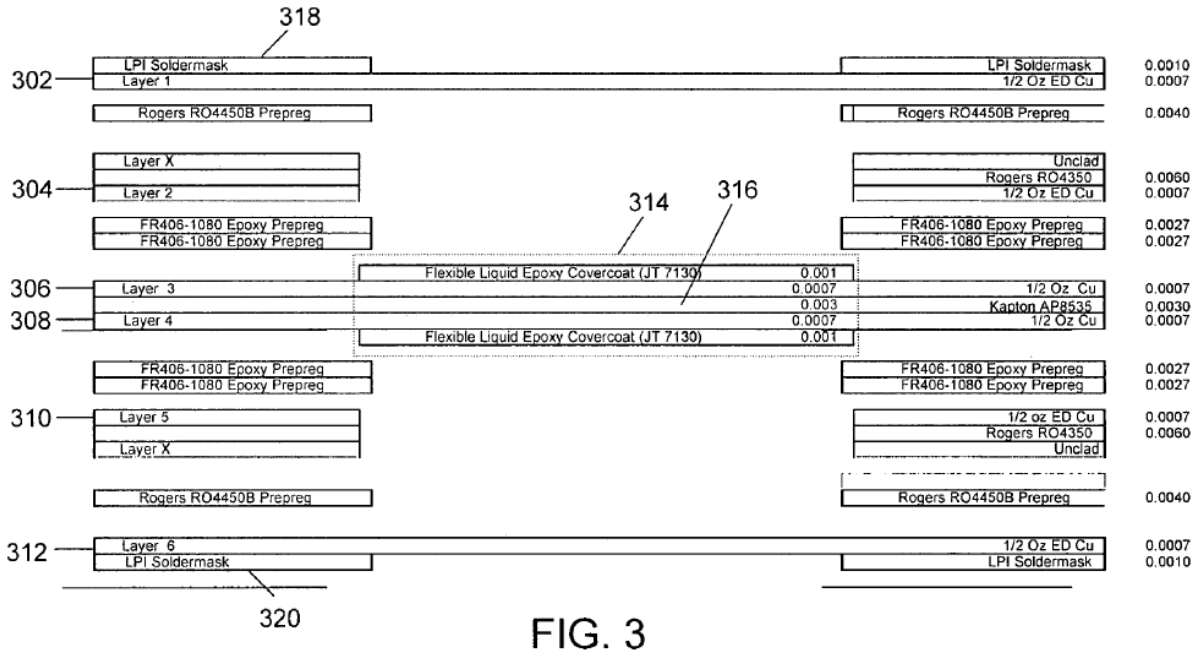


FIG. 3

(*Id.* at FIG. 3.) Kapton is an "electrically insulative material." (Ex. 1032 at 9:3-4, 9:25-27.) Moreover, Kapton is a "non-conductive dielectric material" because it is

is electrically insulating, as discussed above, and it was well-known that Kapton is a "dielectric material." (Ex. 1002, ¶149; Ex. 1030 at 2:60-61 ("dielectric layers such as Kapton ® polyimide"); Ex. 1032 at 9:3-4, 9:25-27.)

A POSITA would have found it obvious to use Kapton as the insulating material between Partovi's PCB layers 357. (Ex. 1002, ¶150.) In particular, a POSITA would have known that Kapton is a well-known insulating layer that is **flexible**. (*Id.*; Ex. 1029 at 3:48-55, 5:50-52.) Indeed, the use of Kapton in flexible PCBs is acknowledged by Partovi itself. (Ex. 1009, ¶[0355] ("flexible PCB material such as Kapton").) Given that there were several advantages to a flexible PCB (Ex. 1009, ¶¶[0137], [0151]), a POSITA would have found it obvious to use Kapton as the insulating material in the Partovi-Chiang PCB. (Ex. 1002, ¶150.) *See Unwired Planet*, 841 F.3d at 1003. Therefore, the Partovi-Chiang-Phan combination discloses or suggests claim 27 because in the combination, the insulating layer is an "electrically insulative material" such as Kapton, which is a "non-conductive dielectric material."

D. Ground 4: Claim 5 is obvious over Partovi in view of Chiang and Hu

The Partovi-Chiang combination in view of Hu discloses or suggests this limitation. (Ex. 1002, ¶¶151-154.) To the extent that the Partovi-Chiang combination does not inherently or explicitly discloses "providing a thickness of the first conductor layer about equal to a thickness of a skin depth of the first

conductor layer at a given frequency," Hu discloses such a feature and it would have been obvious to implement the conductive layers of coil 356 (including "first conductor layer") in Partovi such that its thickness is about one to two times the skin depth at a given operating frequency. (*Id.* at ¶151.)

Similar to Partovi, Hu discloses a PCB integrated inductor and concerns reducing resistance when operating in the RF range. (Ex. 1033 at 558 (Abstract disclosing "[l]ow-ac-resistance planar or foil-wound inductors"), 564 (disclosing an inductor designed for operating at a RF frequency, e.g., at 1 MHz).) Thus, a POSITA would have at least contemplated Hu's disclosure when designing the PCB-based inductor as disclosed in Partovi. (Ex. 1002, ¶152.) Hu further discloses that "the choice of conductor thickness" in the disclosed inductor is "already well understood." (Ex. 1033 at 559.) In particular, Hu discloses

> since current will mainly flow in the top skin depth, a thickness of **one to two skin depths** is sufficient to achieve near-minimum ac resistance.

(*Id.*)

As such, when implementing each of conductive layers of coil 356, in Partovi's inductor, a POSITA would have found it obvious to ensure that the thickness of each of the conductive traces is at least **one to two skin depths** at the

inductor's operating frequency in order to minimize conductor loss in these layers. (Ex. 1002, ¶153.) *See Unwired Planet*, 841 F.3d at 1003.

A POSITA would have understood that implementing the claimed feature would have involved no more than applying a known technique to a known device to yield a predictable result (e.g., designing and implementing a conductor based on the skin depth at a certain operating frequency or altering the operating frequency to ensure that the skin depth is one or two times the conductor thickness). (Ex. 1002, ¶154.) *See KSR*, 550 U.S. at 416.

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-3, 6-8, 10, 12, 13, 15-21, and 23-29 of the '046 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 22, 2019 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,300,046 contains, as measured by the word-processing system used to prepare this paper, 13,834 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,300,046 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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