UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

NUCURRENT, INC.
Patent Owner

Patent No. 8,698,591

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,698,591

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review of claims 1-4, 6-8, 10, 12, 13, 15-21, 24-28, 35, and 37-39 ("the challenged claims") of U.S. Patent No. 8,698,591 ("the '591 patent") (Ex. 1001), which, according to PTO records, is assigned to NuCurrent, Inc. ("Patent Owner" or "PO"). For the reasons set forth below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.

Related Matters: The '591 patent is at issue in *NuCurrent, Inc. v. Samsung Electronics Co., Ltd.*, 1:19-cv-00798-DLC (S.D.N.Y.). The '591 patent shares the same specification as U.S. Patent No. 8,680,960 ("the '960 patent"); U.S. Patent No. 8,710,948 ("the '948 patent"); and U.S. Patent No. 9,300,046 ("the '046 patent"). Petitioner is concurrently filing petitions challenging these patents. Moreover, Patent Owner has also asserted U.S. Patent No. 9,941,729 ("the '729 patent") in the above litigation.

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan

R. Bansal (Limited Recognition No. L0667), (3) Howard Herr (*pro hac vice* admission to be requested), and (4) David Valente (Reg. No. 76,287). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-NuCurrent-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the ’591 patent is available for review and Petitioner is not barred or estopped from requesting IPR on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review Is Requested

Petitioner respectfully requests review of claims 1-4, 6-8, 10, 12, 13, 15-21, 24-28, 35, and 37-39 (“challenged claims”) of the ’591 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 1-4, 10, 15-17, 19, 21, 24-27, 37, and 38 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over U.S. Patent Application Publication No. 2009/0096413 A1 to Partovi ("Partovi") (Ex. 1009).

Ground 2: Claims 6, 7, and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 9,912,173 ("Tseng") (Ex. 1022).

Ground 3: Claims 8, 12, 27, and 28 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 7,601,919 ("Phan") (Ex. 1029).

Ground 4: Claims 1-4, 10, 15-21, 24-27, 35, and 37-39 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi and U.S. Patent No. 7,248,138 ("Chiang") (Ex. 1023).

Ground 5: Claims 6, 7, and 13 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and Tseng.

Ground 6: Claims 8, 12, 27, and 28 are unpatentable under pre-AIA 35 U.S.C. § 103(a) as being obvious over Partovi, Chiang, and Phan.

The '591 patent issued from U.S. patent application no. 13/797,581 (the '581 application"), filed March 12, 2013. (Ex. 1001, Cover.) The '581 application claims priority to a series of related applications, including Provisional Application No. 61/158,688, filed March 9, 2009. For purposes of this proceeding only,

Petitioner assumes the earliest effective filing date of the '591 patent is March 9, 2009.

Partovi was filed May 7, 2008. (Ex. 1009, Cover). Tseng is a continuation of U.S. Application No. 11/901,158, filed September 14, 2007. (Ex. 1022, Cover). Phan was filed October 21, 2005. (Ex. 1029, Cover). Therefore, Partovi, Tseng, and Phan are prior art under pre-AIA 35 U.S.C. § 102(e). Chiang issued on July 24, 2007. (Ex. 1023, Cover). Therefore, Chiang is prior art under pre-AIA 35 U.S.C. § 102(b). None of these references were considered by the Patent Office during prosecution of the '591 patent. (*See, e.g.*, Ex. 1001, Cover ("References Cited"); Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art as of the claimed priority date of the '591 patent ("POSITA") would have had at least a Bachelor's degree in electrical engineering, or a similar discipline and at least two years additional relevant experience with power electronics, including design or manufacturing of inductors. (Ex. 1002, ¶15.)[1] More education can supplement practical experience and vice versa. (*Id.*)

[1] Petitioner submits the declaration of Dr. Steven Leeb (Ex. 1002), an expert in the field of the '591 patent. (Ex. 1002, ¶¶3-10; Ex. 1003.)

VII. THE '591 PATENT

The '591 patent, titled "Method for Operation of Multi-Layer-Multi-Turn High Efficiency Tunable Inductors," is directed to "an inductor having a plurality of conductor layers separated by layers of insulator," "for incorporation within electric circuits." (Ex. 1001, Title, Abstract, 1:37-40, 4:23-24; *see also id.* at 4:25-26 (disclosing the inductor described is "[m]ost notably" for "electrical circuits that operate within and above the radio frequency range of at least 3 kHz"); Ex. 1002, ¶¶31-36; *see also* Ex.1002, ¶¶17-30 (citing Exs. 1006, 1009, 1012, 1015-18.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-51,359 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA, at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Here, given the close correlation and substantial identity between the prior

art references and the challenged claims, Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims.[2] (Ex. 1002, ¶37.)

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Partovi Renders Obvious Claims 1-4, 10, 15-17, 19, 21, 24-27, 37, and 38

1. Claim 1

a) "A method of operating an electrical circuit, the method comprising the following steps:"

Partovi discloses this limitation. (Ex. 1002, ¶¶46-47.) Partovi discloses a "charger." (Ex. 1009, FIG. 29[3] (reproduced below), ¶[0272]-[0273].) The "charger" is an electrical circuit. (Ex. 1002, ¶46; see also *id*. at ¶¶38-44.)

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[2] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '591 patent in this petition, including invalidity under 35 U.S.C. § 112.

[3] The configuration of figure 29 is an "enhancement" of the charger or power supply disclosed in figure 28. (*See* Ex. 1009, ¶¶[0260]-[0261], [0270]-[0273]; Ex. 1002, ¶46, n2.) Accordingly, the description of figure 29 does not repeat the details associated with figure 28. (Ex. 1002, ¶46, n2.)

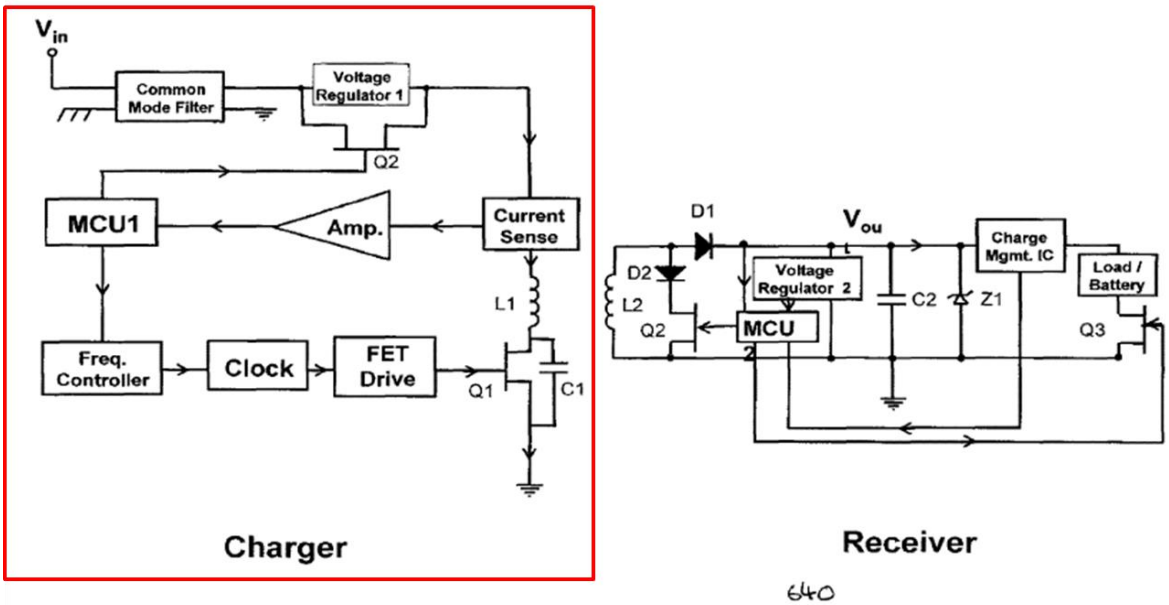


Figure 29

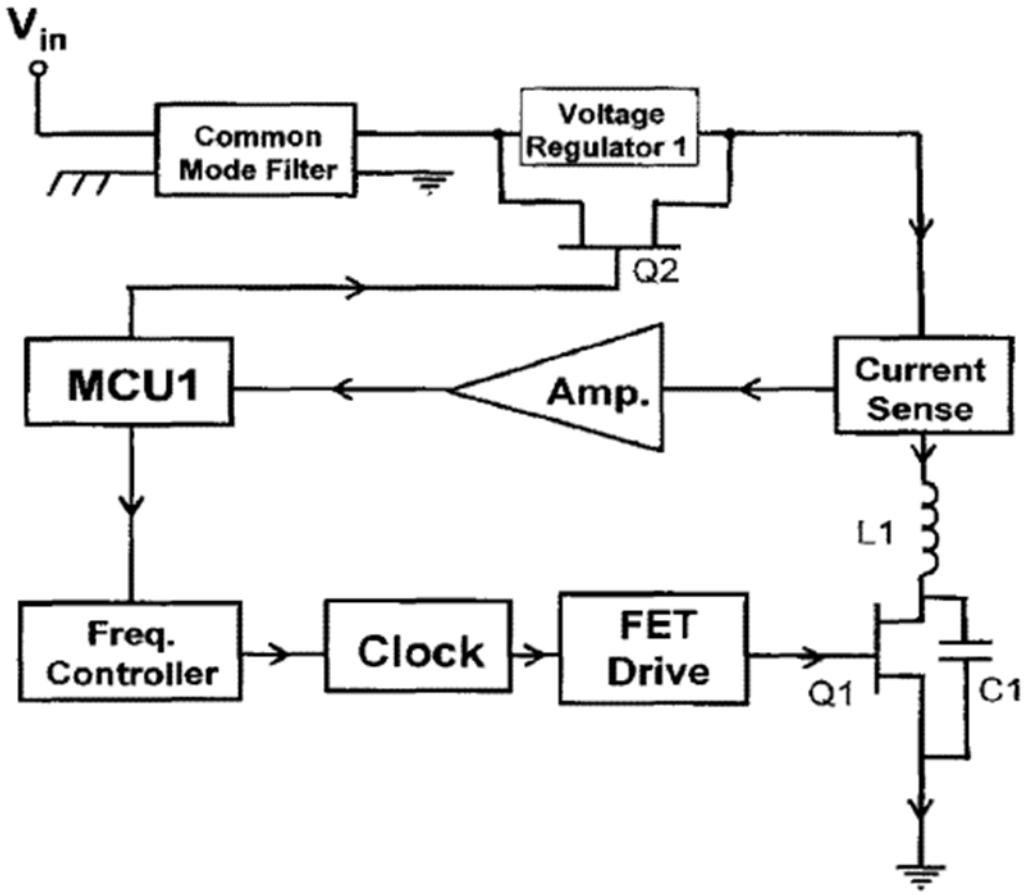
(Ex. 1009, FIG. 29 (annotated); Ex. 1002, ¶46.)

Partovi further explains a method of operation for the "charger" in figure 29. Partovi describes regulating the voltage provided to the inductor coil L1 based on the power needs of the receiver. (Ex. 1009, ¶¶[0272]-[0273]; Ex. 1002, ¶47; *see also infra* Sections IX.A.1(b)-(j).)

b) **"a) providing a first electrical circuit electrically connectable to a power source, the first electrical circuit comprising at least an inductor, comprising:"**

Partovi discloses this limitation. (Ex. 1002, ¶¶48-51.) For example, the charger in figure 29 contains an electrical circuit that includes an inductor L1 ("a first electrical circuit . . . the first electrical circuit comprising at least an

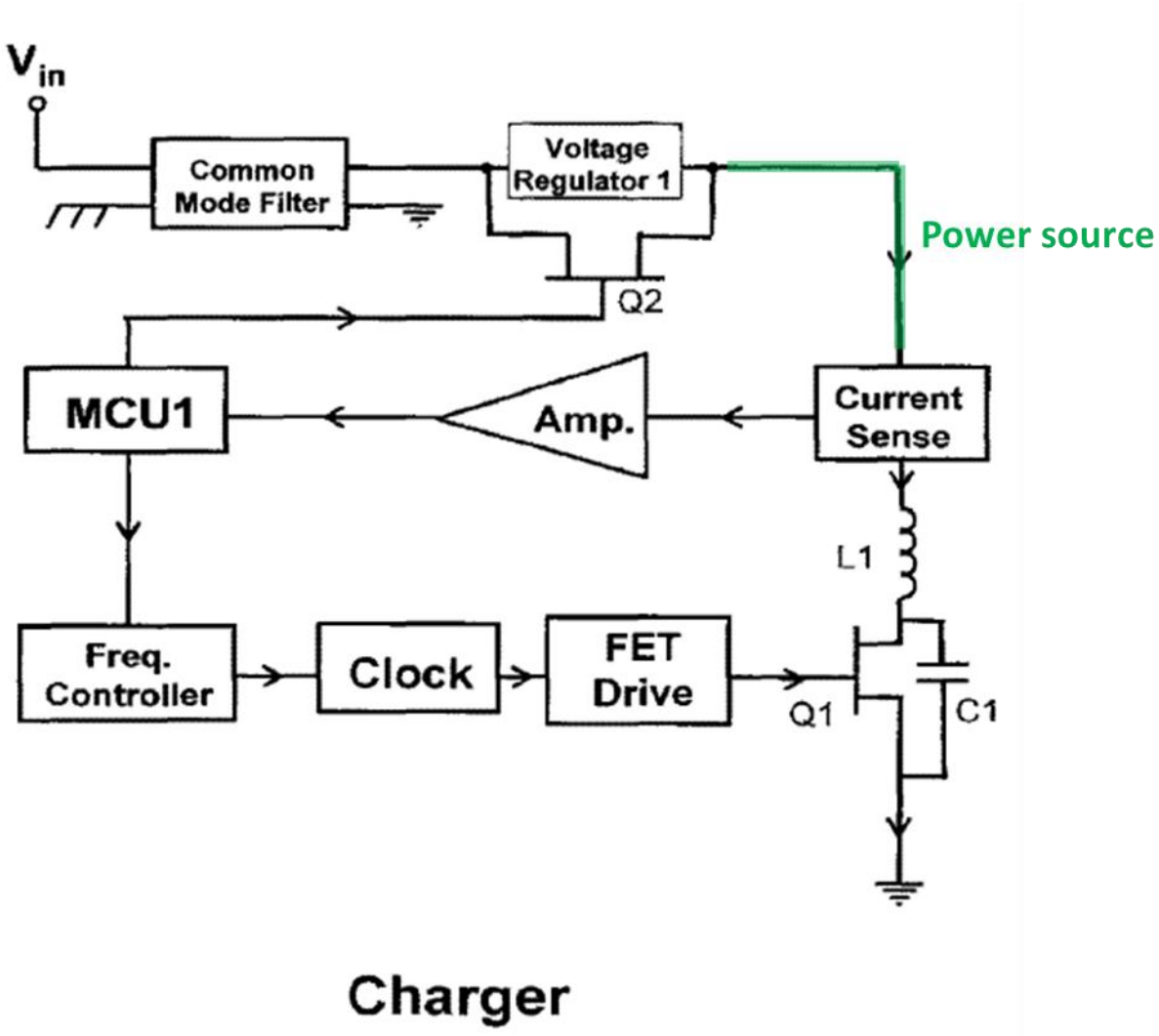
inductor"), a current sense circuit, and a FET Q1. (Ex. 1009, FIG. 29, ¶¶[0272]-[0273].[4])



(Ex. 1009, FIG. 29 (excerpt).)

[4] The current sensor is connected "in series with the" inductor coil L1. (Ex. 1009, ¶[0261].) Such disclosure corresponds to both figures 28 and 29. (Ex. 1002, ¶48, n.3; Ex. 1009, ¶¶[0270], [0271].)

Partovi also discloses that the first electrical circuit is "electrically connectable to a power source." (Ex. 1002, ¶49.) As seen below, Partovi discloses an electrical bus/wire that connects voltage regulator 1 and switch Q2 to the electrical circuit. (*Id.*) As explained below, the electrical bus/wire is a "power source" that provides a voltage output. (*Id.*)



(Ex. 1009, FIG. 29 (excerpt, annotated); Ex. 1002, ¶49.)

During normal operation, voltage regulator 1 is shut down, and Q2 is closed and V_{in} (e.g., 5 V) passes through. (*Id.*, ¶[0272]-[0273].) But, if the receiver requires less power, voltage regulator 1 is switched on to reduce the voltage (e.g., from 5 V to 3 V). (*Id.*, ¶[0272]) Therefore, the electrical bus/wire is a "power source" because it provides a voltage to the electrical circuit (including inductor L1). (Ex. 1002, ¶50.)

Furthermore, figure 29 (see above) makes clear that the electrical bus is electrically connected to the electrical circuit because the voltage on the bus is provided to inductor L1. (Ex. 1009, FIG. 29, ¶¶[0272]-[0273]; Ex. 1002, ¶51.) Therefore, Partovi discloses "a first electrical circuit electrically connectable to a power source." (Ex. 1002, ¶51.)

c) **"a.i) a first conductor; a.ii) second conductor spaced apart from the first conductor, the first conductor and the second conductor being electrically conductive;"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶52-61.)

As discussed above, Partovi does not expressly disclose inductor L1's configuration. (*See supra* Section IX.A.1(b).) In figure 18 Partovi discloses an implementation of a coil for "creat[ing] higher [magnetic] flux densities and more efficient power transfer." (Ex. 1009, ¶[0224]; *see also id.*at ¶[0212].)

Partovi discloses that "to achieve higher flux densities, a coil is constructed with two or more layers, for example by using two or more layers of printed circuit

board." (Ex. 1009, ¶[0212].) Figure 18 describes an example of such a multi-layer coil 356. (*Id.*, ¶¶[0212], [0224].) For example, multi-layer coil 356 includes four PCB layers 357, where the top two layers 357 constitute a "first conductor" and a "second conductor" as recited in claim element 1[c]. (Ex. 1002, ¶¶53-54; Ex. 1009, ¶[0224], FIG. 18; *see also id*. at ¶¶[0213]-[0226].)

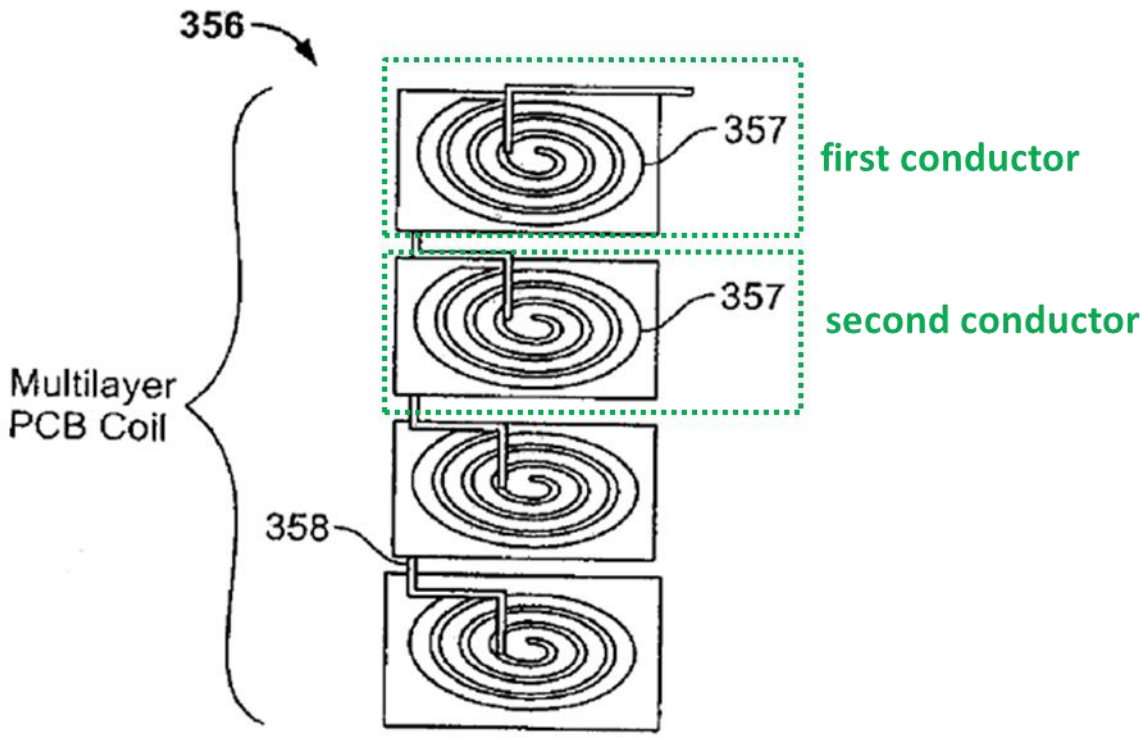


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶54.)

A POSITA would have understood that a "PCB layer" is a conductive layer because the different PCB layers are connected through a "via or contacts" (Ex. 1009, ¶[0224]) and a via or contact is used to connect two conductive layers. (Ex.

1002, ¶55.) This is further confirmed by Partovi, which discloses that the coils of the inductor "can be made of copper material." (Ex. 1009, ¶[0225]; *see also id.* at ¶[0248].) Moreover, Partovi's first and second conductors are spaced apart from each other because the PCB layers 357 are "separate" and connected through a via or contact. (*Id.*, ¶[0224], FIG. 18; Ex. 1002, ¶54.)

A POSITA would have understood that the multi-layer coil structure of figure 18 is applicable to the inductor coil L1 of figure 29. (Ex. 1002, ¶56.) To the extent that the Patent Owner argues or the Board finds otherwise, it would have been obvious for a POSITA to combine the teachings of the figure 29 implementation and figure 18. (Ex. 1002, ¶57.)

In general, obviousness entails an inquiry that is "expansive and flexible" and takes into account "the inferences and creative steps that a person of ordinary skill in the art would employ" when presented with the teachings of the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 415-18 (2007). Under this flexible approach, it important to identify "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements" in the way claimed. *Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356-57 (Fed. Cir. 2007). But that reason may be found "explicitly or implicitly in market forces; design incentives; the interrelated teachings of multiple patents; any need or problem known in the field of endeavor at the time of invention and

addressed by the patent; and the background knowledge, creativity, and common sense of the person of ordinary skill." *ZUP, LLC v. Nash Mfg., Inc.*, 896 F.3d 1365, 1371 (Fed. Cir. 2018) (internal quotations and citations omitted); *see also KSR*, 550 U.S. at 419-20. Moreover, "'if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.'" *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016) (quoting *KSR*, 550 U.S. at 417).

A POSITA would have recognized the benefits of using multi-layer coils and would have been motivated to use such multi-layer coils when implementing inductor coil L1. (Ex. 1009, ¶¶[0010], [0212], [0224]; Ex. 1002, ¶58.) *See Unwired Planet*, 841 F.3d at 1003-04 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"); *KSR*, 550 U.S. at 424.

Furthermore, a POSITA would not have been deterred from utilizing a multi-layer coil inductor in any of Partovi's circuits (including the circuit of figure 29). (Ex. 1002, ¶59.) Moreover, a POSITA would have had the knowledge and skills to implement the inductor coil L1 in figure 29 of Partovi as a multi-layer coil (like in figure 18 of Partovi). (Ex. 1002, ¶60.)

Accordingly, Partovi discloses or suggests implementing inductor coil L1 in figure 29 as a multi-layer coil (like in figure 18) and therefore, discloses an "inductor" that comprises "a first conductor" and a "second conductor spaced apart from the first conductor." (Ex. 1002, ¶61.)

Partovi explains that "[f]or example, the coils [of figure 18] can be made of **copper** material that is sputtered, deposited, or formed onto a printed circuit board (PCB)." (Ex. 1009, ¶[0225].) It was commonly known, and a POSITA would have understood, that copper is an electrically conductive material. (Ex. 1002, ¶62.) As such, Partovi discloses "the first conductor and the second conductor being electrically conductive." (*Id*.)

d) **"a.iii) an insulator positioned in the space between the first conductor and the second conductor; and"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶63.) Partovi discloses that the multi-layer PCB coil 356 (including the claimed "first conductor" and "second conductor") "is created in **separate** PCB layers 357", which are connected by via or contacts using "common techniques used in PCB fabrication." (Ex. 1009, ¶[0224] (emphasis added).) Because the PCB layers are "separate" and there is a connector between two PCB layers, a POSITA would have understood that there is an insulator between them as otherwise the two layers would be deemed the same layer and no connector would be needed. (Ex. 1002, ¶63.)

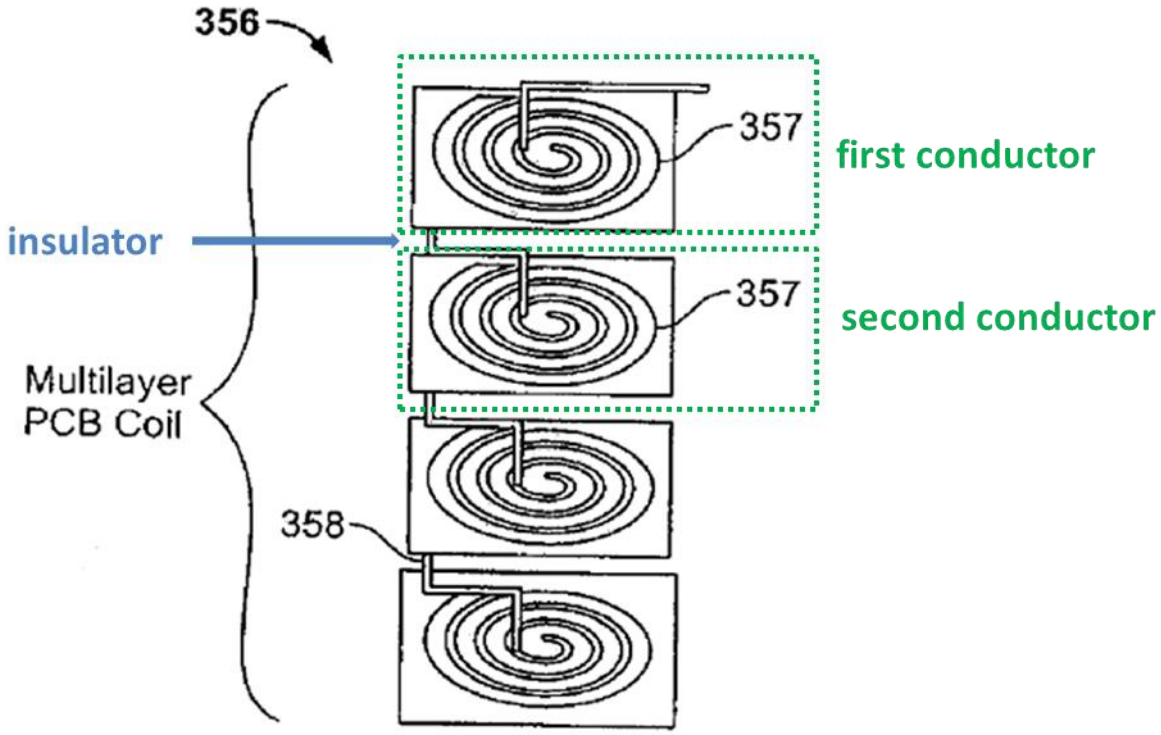


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶63.)

e) **"a.iv) at least one connector electrically connecting the first conductor and the second conductor;"**

Partovi discloses that "multi-layer PCB coil 356 is created in separate PCB layers 357, which are then **connected 358**, and manufactured together via common techniques used in PCB fabrication, **for example by use of a via** or contacts" ("at least one connector electrically connecting the first and second conductor"). (Ex. 1009, ¶[0224] (emphasis added).) A POSITA would have understood that a "via" or "contact" provides an electrical connection between two conducting layers and that Partovi discloses "at least one connector electrically connecting the first

conductor and the second conductor." (Ex. 1002, ¶64; *see supra* Section IX.A.1(c).)

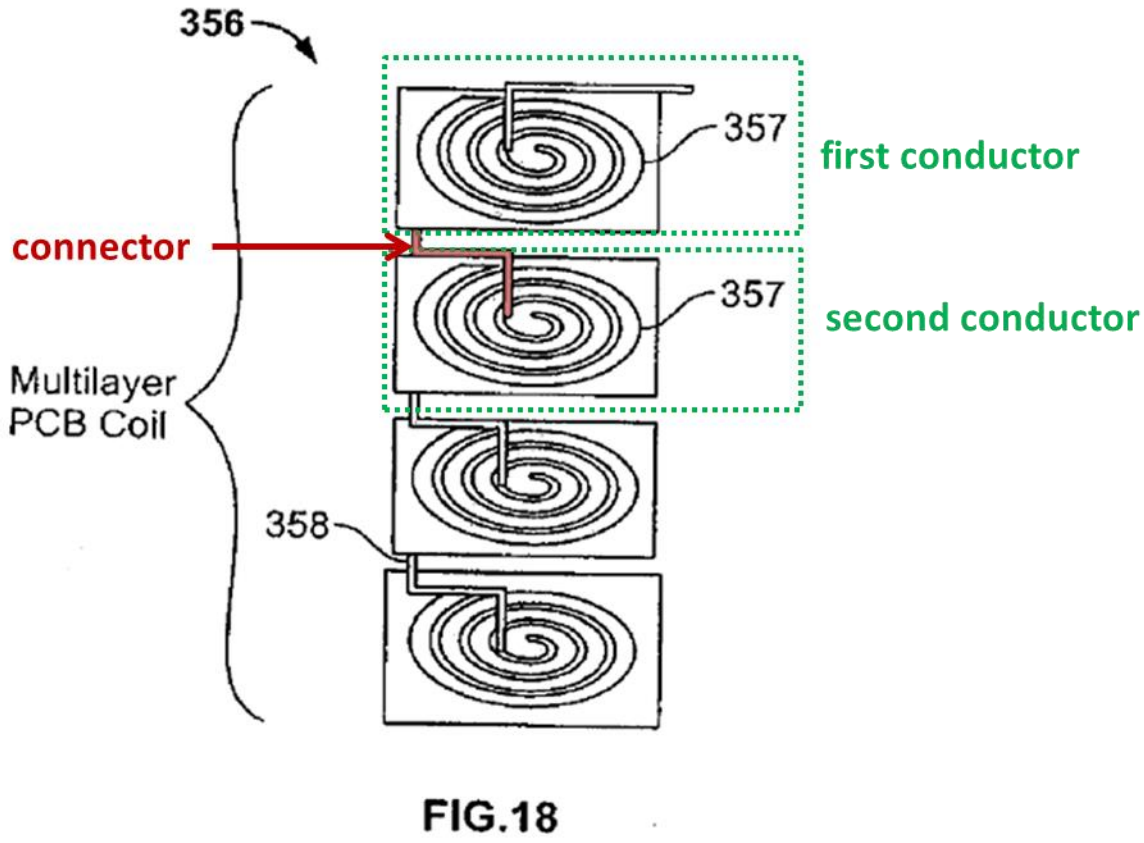


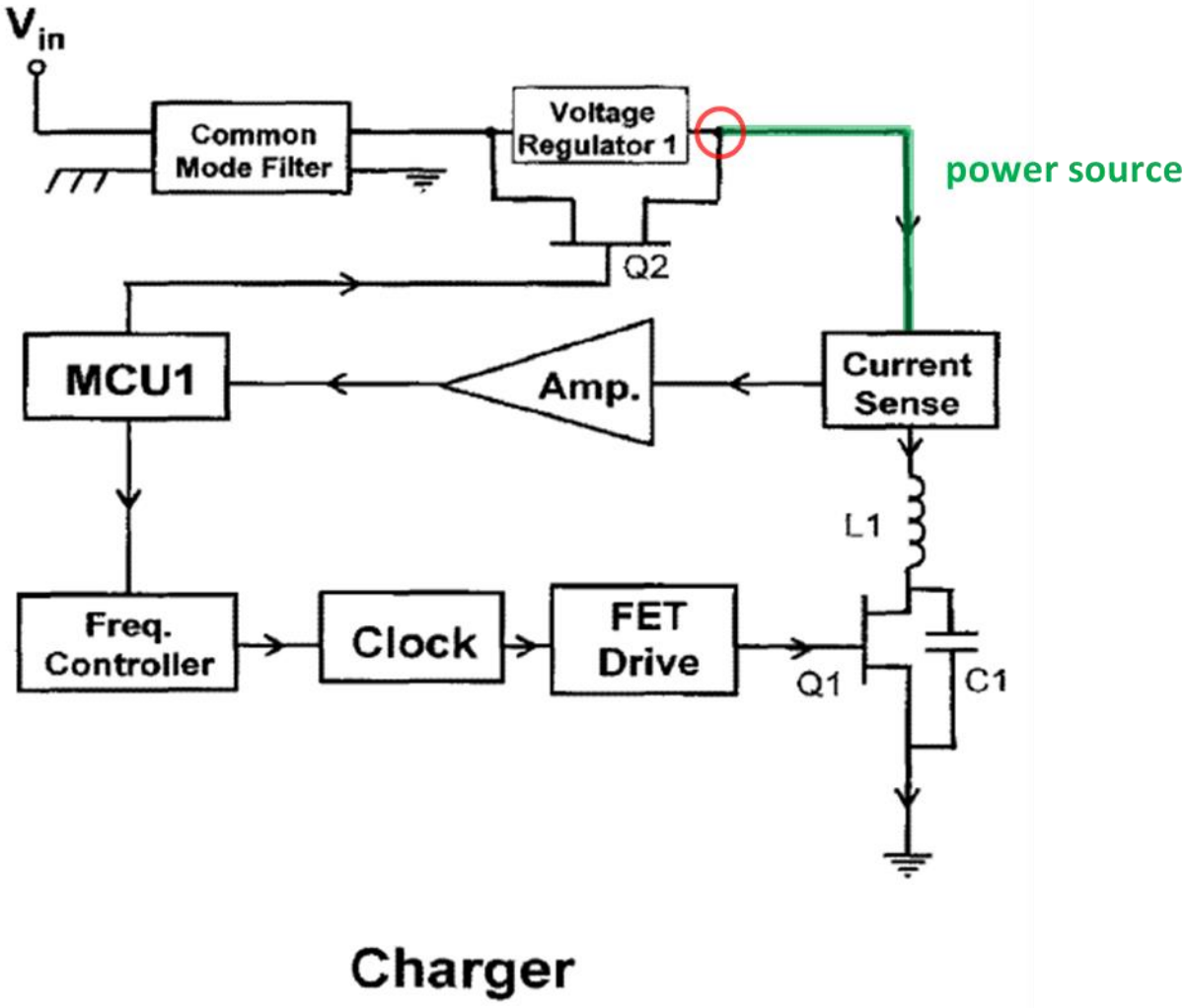
FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶64.)

f) **"b) adjusting an input power level of the power source;"**

Partovi discloses this limitation. (Ex. 1002, ¶65.) For example, as described above for claim element 1[b], Partovi discloses adjusting an input voltage of the electrical bus ("power source"). (*See supra* Section IX.A.1(b)) In particular, Partovi discloses that the input voltage to inductor coil L1 is adjusted based on the power needs of the receiver. (*Id.*; Ex. 1009, ¶¶[0272]-[0273].) Hence, the output

voltage of the combination of voltage regulator 1 and Q2 that is the input to the electrical bus ("power source") is adjusted. Annotated figure 29, reproduced below, highlights the power source in green and the input to the power source in red. (Ex. 1009, FIG. 29; Ex. 1002, ¶65.)



(Ex. 1009, FIG. 29 (excerpt, annotated); Ex. 1002, ¶65.)

Thus, Partovi discloses adjusting the input voltage to the electrical bus (annotated in green above). (Ex. 1002, ¶66.) Accordingly, Partovi discloses or suggests "adjusting an input power level of the power source." (*Id.*)

g) **"c) adjusting an electrical circuit operating frequency to at least about 3 kHz;"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶67-68.) As discussed above, the "charger" of figure 29 includes an "electrical circuit" that includes an inductor L1, FET Q1, and a current sense circuit. (*Supra* Section IX.A.1(b).) Partovi discloses that the above electrical circuit operates "in the 1-2 MHz" range and that the micro control unit (MCU1) changes this frequency to adjust the output power of the primary coil L1. (Ex. 1009, ¶¶[0263]-[0265].) In particular, this frequency corresponds to the frequency at which FET Q1 is switched. (*Id.*; Ex. 1002, ¶67.) Accordingly, Partovi discloses or suggests "adjusting an electrical circuit operating frequency to *at least* about 3 kHz." (Ex. 1002, ¶67.)

Partovi describes controlling the operating frequency primarily in reference to the implementations in figures 26 through 28 (Ex. 1009, ¶¶[0246]-[0270].) However, "the basic concepts for the control . . . are applicable to other geometries and topologies, and can be implemented in a similar manner." (Ex. 1009, ¶[0269].) Thus, a POSITA would have understood that the above disclosures related to figures 26 through 28 also apply to figure 29. (Ex. 1002, ¶68.)

h) **"d) propagating an electrical current within at least the first conductor;"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶69-72.) For example, Partovi discloses that an "input voltage is directly available for the Coil L1." (Ex. 1009, ¶[0272].) Partovi further discloses that the FET Q1 is switched at a certain frequency (e.g., 1-2 MHz). (*Id.*, ¶[0265]; *supra* Section IX.A.1(g).) Accordingly, a POSITA would have understood that an AC current propagates through inductor coil L1. (Ex. 1002, ¶69.)

Inductive power transfer system 110 of figure 2 includes a charger 112 having a primary coil (L_p) 116, a power source (V_{in}) 118, and a switch (T) 126. (Ex. 1009, ¶¶[0117], [0018].) In operation, by switching switch 126 at a certain frequency, an alternating current flows through coil 116, which in turn generates an alternating magnetic field. (*Id.*, ¶¶[0117]-[0118]; *see also id*. at ¶¶ [0013], [0091], [0119]; Ex. 1002, ¶70.)

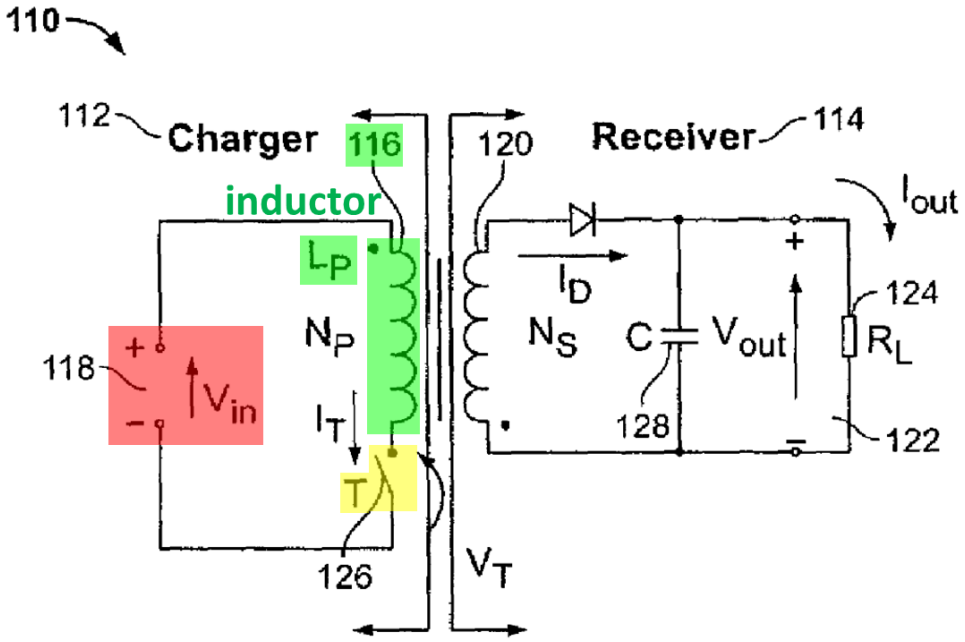


FIG. 2

(Ex. 1009, FIG. 2 (annotated); Ex. 1002, ¶70.)

It would have been apparent to a POSITA that switching of FET Q1 in figures 28 and 29 would also result in an AC current propagating through inductor coil L1. (Ex 1002 at ¶71.) Because inductor L1 in figure 29 includes the first and second conductors (*see supra* Section IX.A.1(c)), when an AC current propagates through inductor L1, it is necessarily propagated within the first conductor. (Ex. 1002, ¶72.)

i) **"e) changing at least one of a frequency, a magnitude, or a waveform shape of the electrical current such that a magnetic flux is generated within the inductor; and"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶73-78.) As discussed above, Partovi discloses that an alternating current propagates through the inductor coil L1. (*Supra* Sections IX.A.1(g), (h).) A POSITA would have known that an alternating current is a current whose magnitude changes with time. (Ex. 1002, ¶73; Ex. 1010 at 25.)

Partovi further discloses changing a frequency of this AC current because Partovi discloses adjusting the switching frequency of the switch Q2. (*Supra* Section IX.A.1(g).) A change in frequency at which the FET Q1 switches also switches a frequency of the current propagating through the inductor. (*See, e.g.*, Ex. 1009, ¶¶[0093], [0117].) Indeed, Partovi states that a "[h]igher drive frequency [of the FET] corresponds to a lower output power" from inductor coil L1. (Ex. 1009, ¶[0263]; *see also id.* at ¶¶[0122]-[0126], [0247], [0248], [0290].)

Therefore, Partovi discloses or suggests "changing at least one of a frequency, magnitude, or waveform shape of the electrical current." (Ex. 1002, ¶¶74-75.)

A POSITA would have understood that such changes would have necessarily changed the magnetic flux generated within the inductor coil L1. (Ex. 1002, ¶¶76-77.) Indeed, it is an inherent property of an inductor that when a current passes through it, a magnetic flux is generated, which changes when the propagating current changes. (*Id.*)

j) **"f) selecting an adjustable inductor quality factor."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶79-80.) A POSITA would have known that the inductor quality factor is a function of frequency, inductance, and resistance. (*Id.*, ¶79.) For example, it was well known that an inductor's quality factor is given by the formula $Q=2\pi fL/R$, where f is the operating frequency, L is the inductance and R is the resistance of the inductor. (*Id*; Ex. 1034 at 2:2-5.) The '591 patent confirms this. (Ex. 1001, 20:26-34; Ex. 1002, ¶79.) As discussed above, Partovi discloses that an AC current propagates through the inductor coil L1 because of the switching of FET Q1. (*See supra* Section IX.A.1(i).) Partovi further discloses adjusting the switching frequency of FET Q1, which changes a frequency of the current propagating through the inductor L1. (*See supra* Section IX.A.1(i); Ex. 1002, ¶79.)

Therefore, Partovi discloses changing the frequency of the current propagating through inductor L1 and discloses selecting the quality factor of inductor L1 ("selecting an adjustable inductor quality factor"). (Ex. 1002, ¶80.) The quality factor is "adjustable" because it can be changed by changing the frequency, inductance, or resistance. (*Id.*)

2. Claim 2

a) **"The method of claim 1 including generating an electromotive force when at least one of the frequency, the magnitude, or the waveform shape of the electrical current is changed."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶81-82.) The claimed feature is merely an inherent property of an inductor, as admitted in the '591 patent, where a change in the current flowing through the inductor results in the generation of an EMF (electromotive force) across the inductor that opposes this change in current. (Ex. 1002, ¶81; Ex. 1001, 1:55-64, 14:17-27.) Therefore, because Partovi's coil L1 is an inductor, an electromotive force will necessarily be generated when there is change in "at least one of the frequency, the magnitude, or the waveform shape" of an electrical current flowing through it (and therefore, through the "first conductor layer"). (Ex. 1002, ¶81.)

Furthermore, as discussed above in Section IX.A.1(i), Partovi discloses changing at least one of the magnitude, waveform shape, and frequency of the current propagating through the inductor coil L1 to change the magnetic flux within the inductor. (*See supra* Section IX.A.1(i).) Thus, an "electromotive force" is necessarily generated in the inductor coil L1 when such a change occurs in the current through inductor L1. (Ex. 1006 at 601; Ex. 1010 at 517; Ex. 1002, ¶82.)

3. Claim 3

a) **"The method of claim 2 including providing a magnitude of the magnetic flux proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶83.) As described above for claim 2, the '591 patent admits this is a known inherent property of an inductor. (Ex. 1001, 1:55-59.) Because Partovi discloses changing at least the frequency and magnitude of the electric current propagating through inductor L1 (*supra* Section IX.A.1(i)), Partovi necessarily discloses "providing a magnitude of the magnetic flux proportional to the amount of change of at least one of the frequency, the magnitude, or the waveform shape of the electrical current." (*See supra* Section IX.A.2; Ex. 1002, ¶83.)

4. Claim 4

a) **"The method of claim 1 including providing an electrical resistance of at least one of the first conductor or the second conductor is reducible when a cross-sectional area of a conducting skin depth within at least the first conductor or the second conductor is increased."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶¶84-86.) A POSITA would have understood that the claimed "conducting skin depth," as admitted by the '591 patent, is an inherent material property, which defines a depth below a conductor's surface where most of the current flows. (Ex. 1002, ¶84.) As explained below, a POSITA would have understood that as the conducting skin depth of a conductor (e.g., either of the top two layers 357 in figure 18 of Partovi, i.e., "the first conductor or the second conductor") increases, cross-sectional area of the conducting skin depth of a conductor also increases, leading to a reduction

of electrical resistance of the conductor. (*Id.*) As such, Partovi discloses "providing an electrical resistance of at least one of the first conductor or the second conductor is reducible when a cross-sectional area of a conducting skin depth within at least the first conductor or the second conductor is increased." (*Id.*)

A POSITA would have understood that the skin depth decreases as the frequency increases. (Ex. 1002, ¶84.) Conversely, as the frequency decreases, the skin depth increases, and so does the cross-sectional area available for current flow, thereby increasing the effective conductivity (or reducing the effective resistance) of the conductor. (*Id.*, ¶85.) The skin depth effect occurs in conductive mediums, such as layers 357 of Partovi's multi-layer inductor (which includes the "first conductor" and "second conductor"), which can be made of copper. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1016 at 1:11-18; Ex. 1017 at 7:5-11, 8:12-28; Ex. 1002, ¶86.) Accordingly, a POSITA would have understood that when the frequency increases, the electrical resistance of layers 357 of Partovi's multi-layer inductor (including the "first conductor layer") increases as the cross-sectional area of a conducting skin depth of the inductor decreases. (Ex. 1002, ¶86.) Similarly, a POSITA would have also understood that when the frequency decreases, the electrical resistance of layers 357 decreases as the cross-sectional area of a conducting skin depth of the inductor increases. (*Id.*)

5. Claim 10

a) **"The method of claim 1 including providing a thickness of a first skin depth of the first conductor about the same as a thickness of a second skin depth of the second conductor."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶87.) As discussed above in Section IX.A.4, a skin depth for a conductor is determined based on the frequency of the current propagating through the conductor, and intrinsic properties of the conductor, including conductivity and permeability. (*See supra* Section IX.A.4.) At least because Partovi discloses that the coils, and hence the layers 357, (including "the first conductor" and "the second conductor") "can be made of copper material," Partovi discloses that these layers are made of the same material and thus the layers necessarily share the same conductivity and permeability. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248]; Ex. 1002, ¶87.) Furthermore, because layers 357 belong to the same inductor coil L1, they are subject to the same current and frequency thereof. (Ex. 1002, ¶87.) Accordingly, each of layers 357 of Partovi's inductor has about the same skin depth because each has the same current, frequency, conductivity, and permeability. (*Id.*) Thus, Partovi discloses or suggests "a thickness of a first skin depth of the first conductor layer is about the same as a thickness of a second skin depth of the second conductor layer." (*Id.*)

6. Claim 15

a) **"The method of claim 1 including operating the**

inductor at an inductor operating frequency of at least 3 kHz."

Partovi discloses or suggests this limitation. (Ex. 1002, ¶88.) For example, Partovi discloses operating inductor L1 in figure 29 at 1-2 MHz ("operating the inductor at an inductor operating frequency of at least 3 kHz"). (Ex. 1009, ¶[0265].) The frequency at which the FET Q1 switches corresponds to the frequency of the AC voltage generated across inductor coil L1. (*See, e.g.*, Ex. 1009, ¶¶[0093], [0117].) Indeed, Partovi states that a "[h]igher drive frequency [of the FET] corresponds to a lower output power" from inductor coil L1. (Ex. 1009, ¶[0263]; *see also id.* at ¶¶[0122]-[0126], [0247], [0248].) Therefore, the switching frequency of FET Q1 is also the operating frequency of the inductor coil L1. (Ex. 1002, ¶88.) Because the operating frequency of FET Q1 is 1-2 MHz (*supra* Section IX.A.1(g)), the operating frequency of inductor coil L1 is also 1-2 MHz. (*Id*.; *see also* Ex. 1009, ¶[0290] ("Switching L1 at high frequency (100 kHz to several MHz) through a Field Effect Transistor (FET) such as Q1 . . . .").)

7. Claim 16

a) **"The method of claim 1 including providing at least one of the first and second conductors formed of a thermally conductive material."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶89.) Partovi discloses that layers 357 (including "the first conductor" and "the second conductor") "can be made of copper material, which is thermally conductive, as a

POSITA would have recognized. (*Id.*; Ex. 1009, ¶[0225]; *see also id.* at ¶[0248]; Ex. 1011 at ¶[0039] (describing copper as "thermally conductive material"); Ex. 1013 at 4:37-39 (disclosing copper as "having a high thermal conductivity").)

8. Claim 17

a) **"The method of claim 1 including providing the connector comprising at least one of a via, a solder, a tab, a wire, a pin, a rivet, a filled mesh structure, a conductive polymer, a conductive composite, a conductive adhesive, a liquid metal, or a foamed metal."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶90.) For example, Partovi discloses that layers 357 of the multi-layer inductor are "connected . . . for example by use of a **via** or contacts." (Ex. 1009, ¶[0224] (emphasis added).)

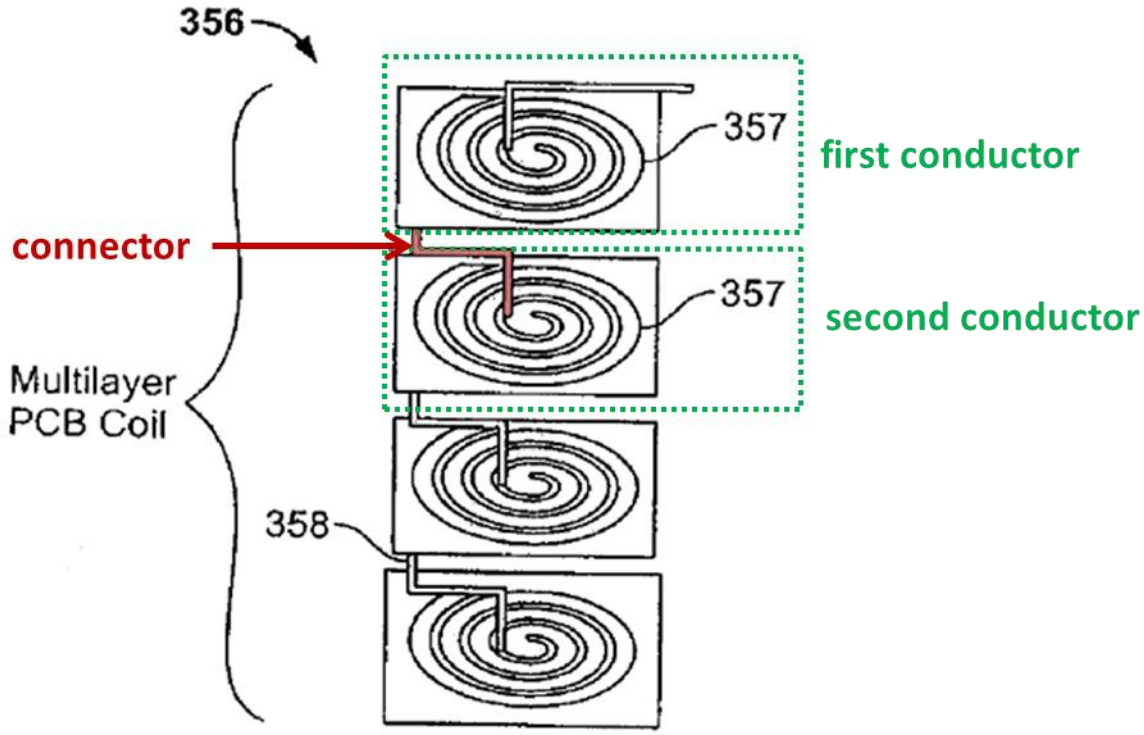


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶90.)

9. Claim 19

a) **"The method of claim 1 including providing the first conductor and the second conductor forming a structure in which the first and second conductors are positioned in about a parallel orientation, a perpendicular, or at an angular relationship with respect to each other."**

Partovi discloses or suggests this limitation. (Ex. 1002 ¶¶91-92.) As an initial matter, the two conductors necessarily satisfy this claim feature as the two conductors having "an angular relationship with respect to each other" encompasses all possible orientations of the two conductors, and a POSITA would

have understood that such an angular relationship would have always existed for the two conductors. (*Id.*, ¶91.)

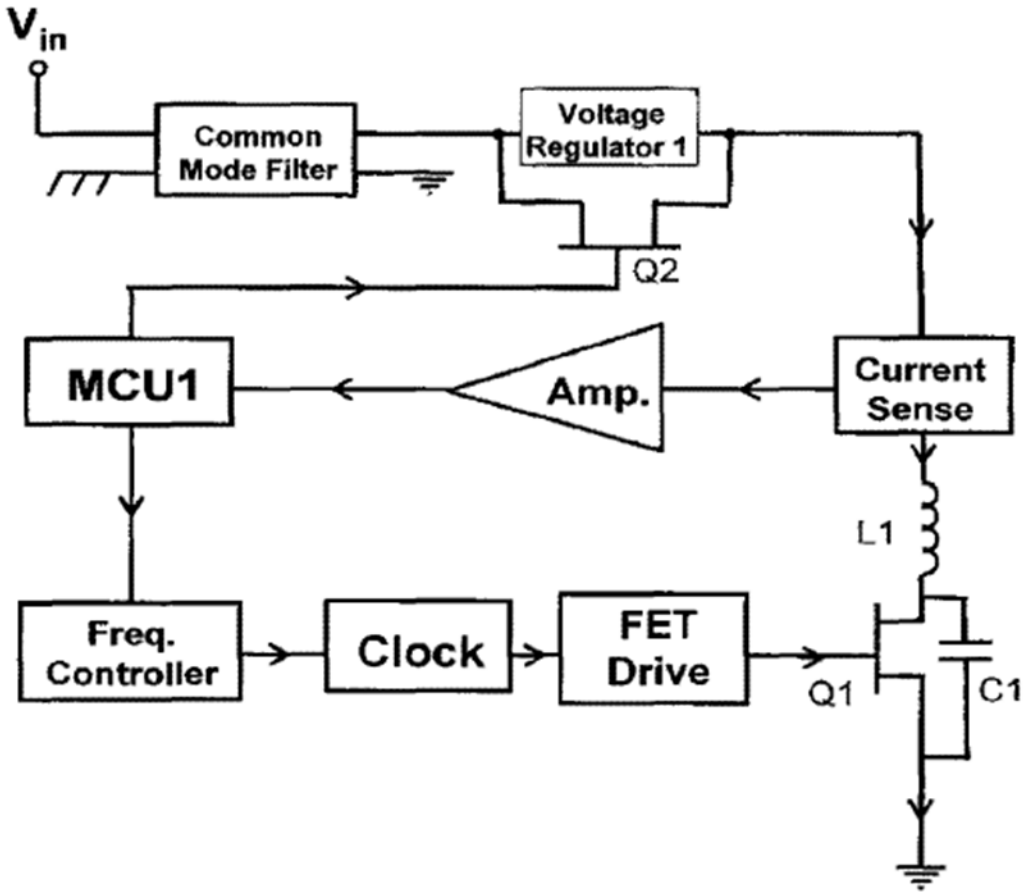
In addition, Partovi discloses with reference to figure 18 coils that are separate and spaced apart from each other in separate planes. (Ex. 1009, ¶¶[0212]-[0224], FIG. 18; *supra* Section IX.A.1(c); Ex. 1002, ¶92.)

10. Claim 21

a) **"The method of claim 1 including providing the inductor electrically connectable with a second electrical circuit operating at about 3 kHz or greater."**

Partovi discloses or suggests this limitation. (Ex. 1002 ¶¶93-94.) As an initial matter, a POSITA would have understood that essentially any electrical circuit is "connectable" to an inductor, regardless of the nature of the electrical circuit or any particular frequency at which it may operate and claim 21 does not impose any constraint on the inductor coil L1 and the second electrical circuit that may be connected to it. (*Id.*, 93.)

Alternatively, Partovi discloses a "second electrical circuit" that is connected to the inductor coil L1. For example, Partovi discloses "FET drive" in figure 29, which drives FET Q1, and is electrically connected to inductor L1 through FET Q1. (Ex. 1009, FIG. 29, ¶¶[0263]-[0264].) The operating frequency of "FET drive" is 1-2 MHz because the FET Q1 is driven to a frequency of 1-2 MHz. (*Id.*, ¶[0265]; Ex. 1002, ¶94.)



Charger

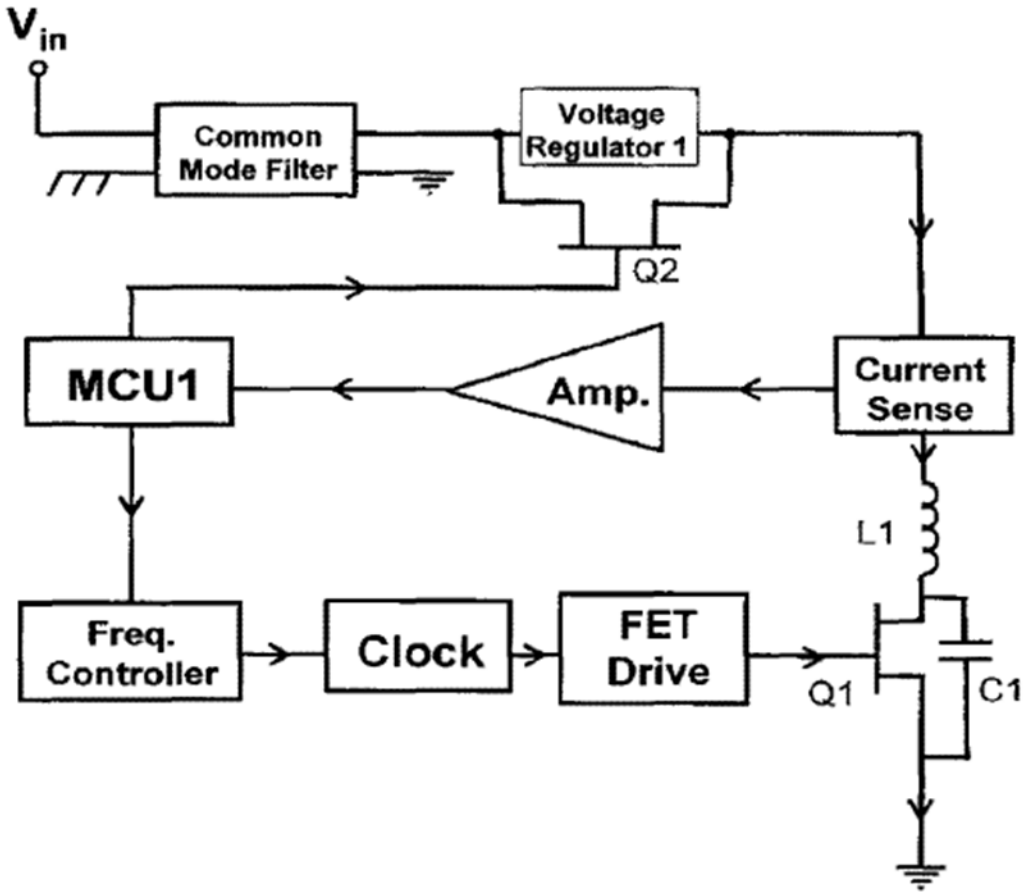
(Ex. 1009, FIG. 29 (excerpt).)

11. Claim 24

a) **"The method of claim 1 including providing a control circuit electrically connectable to the inductor or other component comprising the first electrical circuit."**

Partovi discloses or suggests this limitation. (Ex. 1002 ¶95.) For example, Partovi discloses a micro control unit (MCU1) that controls, via the frequency controller, clock, and FET drive, the frequency at which FET Q1 switches. (Ex.

1029, FIG. 29, ¶¶[0263]-[0265].) Because FET Q1 is a component included in the "first electrical circuit" (*see supra* Section IX.A.1(b)), Partovi discloses a "control circuit" electrically connectable to "other component comprising the first electrical circuit." (Ex. 1002, ¶95.)



Charger

(Ex. 1009, FIG. 29 (excerpt).)

12. Claim 25

a) **"The method of claim 1 including providing at least the first and second conductor layers having at least a partial revolution.[5]"**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶96.) For example, as shown in annotated figure 18 below, Partovi discloses that each of the top two conductor layers 357 ("the first and second conductor layers") of the multi-layer inductor has at least a partial revolution because they each have at least three full turns, where a full turn corresponds to a full revolution. (*Id.*; Ex. 1009, FIG. 18; *see also id.* at ¶[0104], ¶¶[0212]-[0224].)

[5] There is no antecedent basis for "the first and second conductor **layers**" (emphasis added). Petitioner assumes that "the first and second conductor layers" refer to the "first and second conductors" in claim 1.

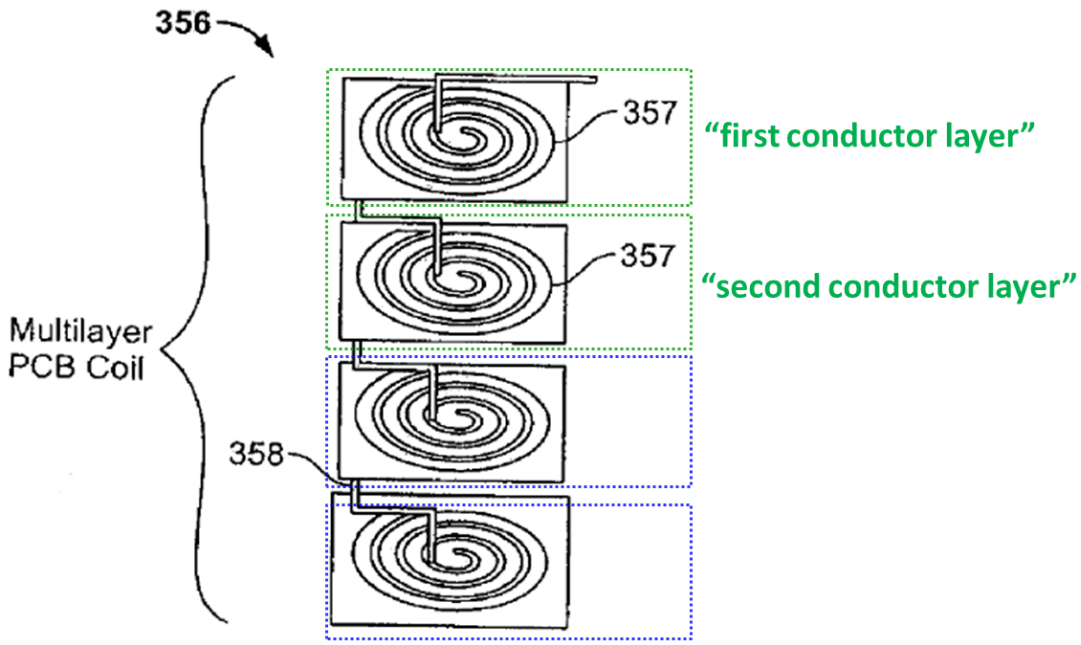


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶96.)

13. Claim 26

a) **"The method of claim 1 including selecting the first conductor or the second conductor having a material selected from the group of materials consisting of copper . . . ."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶97.) For example, Partovi discloses that layers 357 (including "first conductor" and "second conductor") "can be made of copper material" formed on PCB layers. (Ex. 1009, ¶[0225]; *see also id.*at ¶[0248].)

14. Claim 27

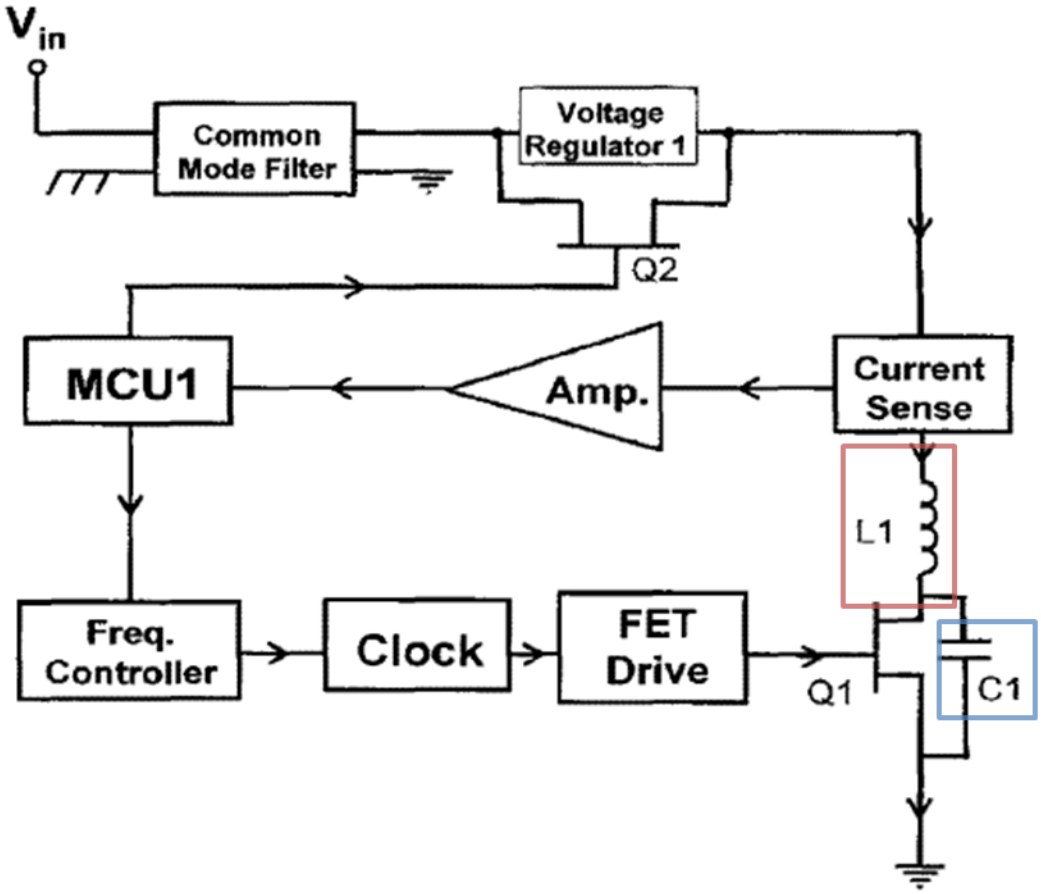
a) **"The method of claim 1 including providing at least one insulator layer of an electrically insulative material."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶98.) As discussed above, Partovi discloses an insulating layer between the PCB layers 357 that electrically insulates two PCB layers 357 from each other. (*Supra* Section IX.A.1(d).) Therefore, Partovi discloses that the insulating layer is an "electrically insulative material." (Ex. 1002, ¶98; Ex. 1028 at 1:6-23.)

15. Claim 37

a) **"The method of claim 1 including electrically connecting a resistor or a capacitor to the first electrical circuit."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶99.) As discussed above, inductor L1, current sense circuit, and FET Q1 in figure 29 constitute a "first electrical circuit." (*Supra* Section IX.A.1(b).) As seen in figure 29, a capacitor C1 is connected to the inductor and therefore, to the first electrical circuit (Ex. 1009, FIG. 29, ¶[0249]; Ex. 1002, ¶99.)



Charger

(Ex. 1009, FIG. 29 (excerpt, annotated); Ex. 1002, ¶99.)

16. Claim 38

a) **"The method of claim 1 including adjusting an electrical circuit operating frequency of the first electrical circuit to at least about 3 kHz."**

Partovi discloses or suggests this limitation. (Ex. 1002, ¶100.) For example, Partovi discloses adjusting the frequency of FET Q1 between 1-2 MHz. (*Supra* Section IX.A.1(g).) In one example, the frequency is adjusted to 1.2-1.4 MHz.

(Ex. 1009, ¶[0265].) Adjusting the frequency of the FET Q1 is "adjusting an electrical circuit operating frequency of the first electrical circuit." (Ex. 1002, ¶100.)

B. Ground 2: Partovi in View of Tseng Renders Obvious Claims 6, 7, and 13

1. Claim 6

a) **"The method of claim 1 including providing a thickness of the first conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the first conductor at a given operating frequency."**

Partovi in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶¶101-106.) Partovi does not explicitly disclose providing a thickness of the PCB layer 357 ("first conductor") ranging from about 1.25 times to about 4 times a thickness of a skin depth of the layer at a given frequency. But Tseng discloses such a feature, and it would have been obvious to implement PCB layer 357 in Partovi such that its thickness is at least two times the skin depth at a given operating frequency. (*Id.*, 102.)

Similar to Partovi, Tseng generally discloses inductive power transfer system using coil inductors. (Ex. 1022, Abstract.) Indeed, just like Partovi, Tseng utilizes coil inductors formed on PCBs (*id.* at 5:37-40 (using "multiple layers of coils for generation of magnetic fields") and aims to improve efficiency of power transfer (*id.* at 10:48-51 (disclosing adjusting "the switching frequency in order to maximize the efficiency of power transfer"), 11:8-14 (disclosing "the efficiency of

power transfer degrades due to various losses . . . . These losses include the conductor loss in coils . . . .").) (Ex. 1002, ¶103.)

Tseng further discloses that, to reduce power loss in coils due to skin depth effect, "the metal thickness should be **more than twice of the skin depth**." (Ex. 1022, 12:3-5 (emphasis added); *see also id.* at 12:6-8 (disclosing that "substrates with a thicker metal layer can be used, or additional metal can be plated to increase the thickness"), 11:66-12:14.) As such, when implementing inductor coil L1 using the multi-layer PCB coil 356 in Partovi, a POSITA would have found it obvious to ensure that the thickness of each of the PCB layers 357 is at least twice the skin depth at the system's operating frequency in order to minimize conductor loss in these layers. (Ex. 1002, ¶104; *see also* Ex. 1024 at 1:34-38 (disclosing that "it has become commonplace to use a planar conductive film having a thickness on the order of **twice the skin depth** at the intended operating frequency as the magnetic component's conductors.") (emphasis added).) *See Unwired Planet*, 841 F.3d at 1003-04 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]").

A POSITA would have been able to make the necessary changes to the thickness of the PCB layers 357 making up the inductor coil L1 based on the operating frequency. (Ex. 1002, ¶105.) For example, Partovi discloses that

different sizes of copper, such as from 1 to 6 oz. (corresponding to thicknesses of from 1.4 to 8.2 mil), can be used to optimize the inductive circuit for a particular application. (Ex. 1009, ¶[0167] (disclosing that "[m]ost common PCBs use 1-2 oz copper PCBs" and "the coil PCB used for the wireless charger can be made from PCBs clad with between 2 and 4, or even 6 oz copper"); *see also id.* at ¶[0212] (disclosing that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application."); Ex. 1002, ¶105.)

A POSITA would have understood that implementing the claimed feature of claim 6 would have involved no more than applying a known technique to a known device to yield a predictable result (e.g., designing and implementing a conductor based on the skin depth at a certain operating frequency). (Ex. 1002, ¶106.) *See KSR*, 550 U.S. at 416.

2. Claim 7

a) **"The method of claim 1 including providing a thickness of the second conductor ranging from about 1.25 times to about 4 times a thickness of a skin depth of the second conductor at a given operating frequency."**

Partovi in view of Tseng discloses or suggests this limitation. (Ex. 1002, ¶107.) For example, the Partovi-Tseng system discloses or suggests implementing

PCB layers 357 in Partovi such that the thickness of the layers 357 (including the "second conductor") is about twice the skin depth at a given frequency. (*See supra* Sections IX.A.1(c) (one of PCB layers 357 is a "second conductor"), IX.B.1 (analysis for claim 6).)

3. Claim 13

a) **"The method of claim 1 including providing the inductor having an inductor quality factor greater than about 5."**

The Partovi-Tseng combination discloses or suggests this limitation. (Ex. 1002, ¶108.) Partovi discloses an "inductor" (inductor coil L1). (*Supra* Section IX.A.1(b).) But Partovi does not disclose the inductor quality factor for the coil. (Ex. 1002, ¶108.) However, as discussed below, it would have been obvious to configure the inductor coil L1 such that it has an inductor quality factor greater than 5. (*Id.*)

As discussed above with respect to claim 6, a POSITA would have been motivated in view of the teachings of Partovi and Tseng to reduce power loss in Partovi's inductor coil L1 by ensuring that the thickness of the PCB layers forming the coil is at least twice the skin depth at the system's operating frequency. (*See supra* Section IX.B.1.) Tseng further discloses a high Q value of about 100 by optimizing the spacing between the conductive traces of an inductor. (Ex. 1022, FIG. 24, 8:1-18; Ex. 1002, ¶109.)

Based on the combined teachings of Partovi and Tseng, a POSITA would have had reasons to consider the teachings of Tseng when contemplating the features disclosed by Partovi. (Ex. 1002, ¶110.) And, based on those disclosures, such a skilled person in the art would have found it obvious to optimize Partovi's inductor to improve its Q factor to be greater than 5 to improve efficiency or reduce power loss in the inductor in view of Tseng. (Ex. 1034 at 2:5-6; Ex. 1002, ¶110.) *See KSR*, 550 U.S. at 416.

For example, when implementing Partovi's inductor, a POSITA would have been motivated to find ways to improve the efficiency of the inductor and Tseng discloses at least a way to do so by optimizing the spaces between conductive traces of an inductor. (Ex. 1002, ¶111.) Indeed, by increasing the width of the traces (i.e., narrowing the spaces among them), Tseng shows that the inductor's "coupling efficiency" is improved and the Q value improves from 50 to 100. (*Id.*; Ex. 1022, FIG. 24, 8:1-18.) Furthermore, a POSITA would not have been deterred from optimizing Partovi's inductor in view of Tseng's teachings. (Ex. 1002, ¶111.) For example, Partovi discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and **coupling efficiency** for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[0212] (emphasis added); Ex. 1002, ¶111.)

Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil and/or circuits and to combine them. (Ex. 1002, ¶112.) In fact, the '591 patent admits that multi-layer inductors "can be relatively easily achieved by existing manufacturing techniques (for example multi-layer printed wiring board, FIG. 21), and can therefore be integrated with other circuit components such as ICs, resistors, capacitors, surface mount components, etc." (Ex. 1001, 31:37-42; Ex. 1002, ¶112.)

C. Ground 3: Partovi in View of Phan Renders Obvious Claims 8, 12, 27, and 28

1. Claim 8

a) **"The method of claim 1 including providing a first conductor thickness about the same as a second conductor thickness."**

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶114-117.) As discussed above, the top two PCB layers 357 in figure 18 of Partovi correspond to the claimed "first conductor layer" and "second conductor layer." (*Supra* Section IX.A.1(c).)

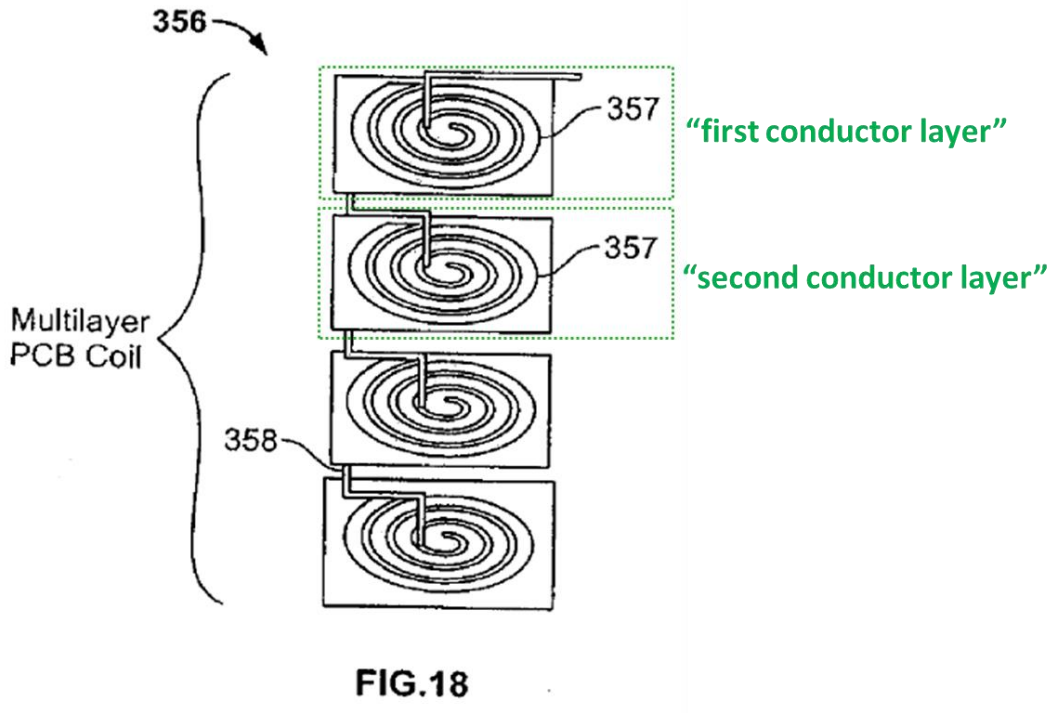


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶114.)

While Partovi does not explicitly disclose that the thickness of the PCB layers 357 is about the same, a POSITA would have found it obvious in view of Phan to use about the same thickness for each of the PCB layers 357 ("wherein a first conductor layer thickness is about the same as a second conductor layer thickness"). (Ex. 1002, ¶115.)

For example, using two PCB layers 357 ("first conductor layer" and "second conductor layer") of the same thickness would have been obvious because there are only two choices: either using layers of the same thickness or using layers of different thickness. (*Id.*.) Thus, choosing two PCB layers 357 of the same thickness would have been one of two choices available to a POSITA. (*Id.*.)

Accordingly, using layers of the same thickness would have been obvious because it would have been one of a "finite number of identified, predictable solutions." *Perfect Web Techs., Inc. v. InfoUSA, Inc*., 587 F.3d 1324, 1331 (Fed. Cir. 2009) (internal citation omitted) (holding that a claimed step was obvious when it was one of three available choices). Indeed, there is nothing special about setting the thickness of two layers to be the same and this is evident from claims 8 and 9 of the '591 patent. (Ex. 1002, ¶115.) Specifically, while claim 8 recites that the first and second conductor layers have "about the same" thickness, claim 9 recites that the thickness of the two layers is "different." (*Id.*; Ex. 1001, claims 8, 9.)

Phan discloses a multilayer PCB stackup in figure 3 that includes six conducting layers, 302, 304, 306, 308, 310, and 312. (Ex. 1029, 5:43-46, FIG. 3 (reproduced below).) Each of the conductor layers has the same thickness as shown below in figure 3. (Ex. 1029, 5:46-48 ("each conductor layer can be made of half ounce of copper and be 0.0007 inches in thickness"); *see also id.* at Abstract, 3:55-61, 3:66-4:4, 5:43-46.)

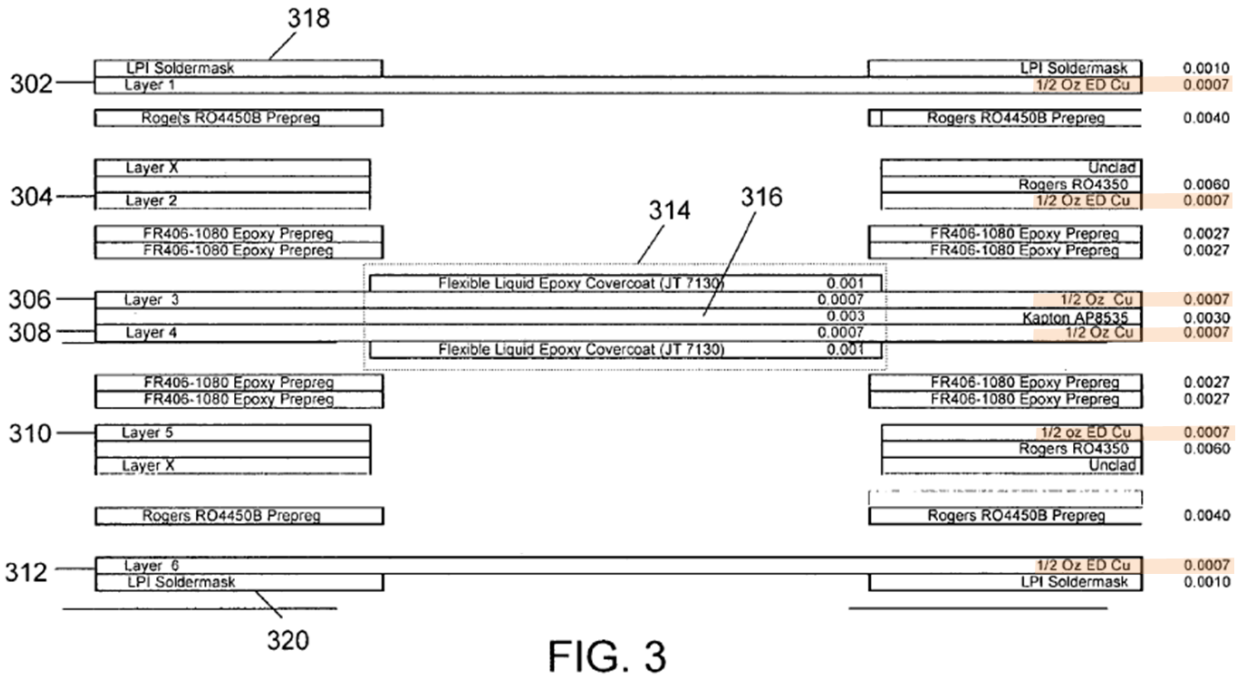


FIG. 3

(Ex. 1029, FIG. 3 (annotated); Ex. 1002, ¶116.) Phan further explains that "[i]n one embodiment of the invention, the number of layers in [the PCBs] is six," however, in other embodiments "the number of layers . . . can be four . . . or any other number." (Ex. 1029, 4:28:36; Ex. 1002, ¶116.)

A POSITA would have had the skills and knowledge to implement the PCB layers 357 in Partovi such that they are each about the same thickness. (Ex. 1002, ¶117.) Implementing Partovi's PCB layers 357 in such a manner based on the teachings of Phan would have been obvious to a POSITA because, as discussed above in this section, choosing the same thickness for the different PCB layers 357 would have been one of two choices available to a POSITA and such a person would have selected the same thickness to suit a POSITA's design objective. (*Id.*)

In fact, implementing Partovi's PCB layers 357 to have the same or about the same thickness would have been merely the application of a known technique (e.g., using conductor layers having the same thickness) to a known device (Partovi's PCB-based inductor) according to known methods (e.g., modifying the thickness of conducting layers) to yield the predictable result of an inductor having conducting layers of the same thickness. (Ex. 1002, ¶117.) *See KSR*, 550 U.S. at 416-21. The above modification is consistent with Partovi's disclosure because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[0212]; *see also id.*at ¶[0479] ("The diameter, thickness, or width of the wire or PCB trace can be optimized to provide optimum resistance."); Ex. 1002, ¶117.)

2. Claim 12

a) **"The method of claim 1 including providing a thickness of the insulator less than about 5 cm."**

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶118-122.) While Partovi does not explicitly disclose a thickness of the insulating layer between PCB layers 357 in its inductor, a POSITA would have found it obvious to use insulating layers each having a thickness that is less than 5 cm based on common sense and in view of Phan. (*Id.*, ¶118.)

To begin, given Partovi's objectives of providing devices that are "lightweight," "portable," and have a "compact" design, a POSITA would have been motivated to minimize the thickness of the insulating layers in its PCB inductor to ensure that the overall thickness of the inductor is as thin as possible. (Ex. 1009, ¶¶[0010] (disclosing that "a common problem with such inductive units is that the windings are bulky, which restricts their use in lightweight portable devices"), [0212] (disclosing "[m]ultiple layer boards can be used to allow compact fabrication"), [0224] (disclosing a need for a coil design "where small x-y coil dimensions are desired"); Ex. 1002, ¶119.) Partovi envisions such an optimization because it discloses that coil dimensions, such as thickness, width, and number of turns, can be altered, such that "the resistance, inductance, flux density, and coupling efficiency for the coils can be adjusted so as to be optimized for a particular application." (Ex. 1009, ¶[0212]; *see also id.* at ¶[0479] ("The diameter, thickness, or width of the wire or PCB trace can be optimized to provide optimum resistance."); Ex. 1002, ¶119.)

Moreover, PCB devices having an insulating layer thickness less than 5 cm were well-known. As discussed above, Phan, like Partovi, discloses a multi-layer PCB. (*Supra* Section IX.C.1.) Furthermore, Phan discloses using insulating layers having thicknesses on the order of thousandths of an inch (1/1000 of an inch is 0.00254 cm) to separate PCB conductive layers ("wherein a thickness of the

insulating layer is less than about 5 cm"). (Ex. 1029, 5:40-59, FIG. 3; Ex. 1002, ¶120.) For example, Phan discloses "an insulating layer 316 of Kapton" having a thickness of 0.003 inches (which is equal to 0.00762 cm) positioned between conducting layers 306 and 308. (Ex. 1029, 5:40-59, FIG. 3; Ex. 1002, ¶120.)

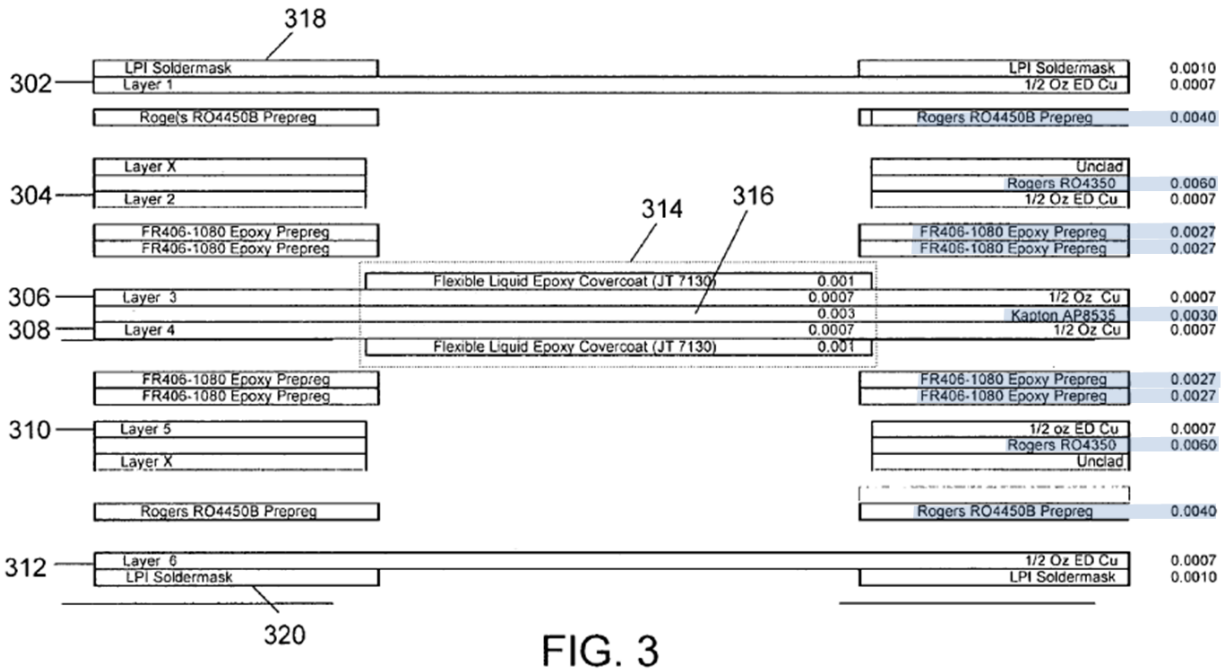


FIG. 3

(Ex. 1029, FIG. 3 (annotated); Ex. 1002, ¶120.)

A POSITA would have the skills and knowledge to design and manufacture the insulating layers in figure 18 of Partovi to be less than 5 cm, similar to as disclosed in Phan. (Ex. 1002, ¶121.) Therefore, a POSITA would have understood and appreciated that the proposed combination involved combining known prior art elements and known technologies according to known methods and common sense (e.g., modifying the thickness of insulating layers in Partovi's

inductor to be less than 5 cm) to yield the predictable result of an inductor having insulating layers each having a thickness of less than 5 cm. (Ex. 1002, ¶121.) *See KSR*, 550 U.S. at 416-21.

Moreover, the thickness of an insulating layer is a "result-effective variable" because it affects the overall thickness of the PCB and also determines the amount of the insulation between the conducting layers on both sides of the insulating layer. (Ex. 1002, ¶122.) A POSITA would have understood that the thickness of the insulation affects the electrical performance of the printed circuit board. (*Id.*) Therefore, if "less than 5 cm" is an optimum number for the insulating layer thickness per claim 12, claim 12 is obvious because "discovery of an optimum value of a result effective variable in a known process is ordinarily within the skill of the art." *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980); *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955); *see also In re Applied Materials, Inc.*, 692 F.3d 1289, 1295 (Fed. Cir. 2012). This is especially true given that the '591 patent provides no evidence that "less than 5 cm" thickness produces a new or unexpected result, and thus the claimed range cannot form the basis of patentability. (Ex. 1002, ¶122.) *In re Boesch*, 617 F.2d at 276; *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

3. Claim 27

a) **"The method of claim 1 including providing at least**

one insulator layer of an electrically insulative material."

Partovi in view of Phan discloses or suggests this limitation for reasons similar to those discussed below for claim 28. (Ex. 1002, ¶123; *see infra* Section IX.C.4.) In particular, as discussed below with respect to claim 28, a POSITA would have found it obvious to use an electrically insulative material like Kapton for the insulator layer.

4. Claim 28

a) **"The method of claim 1 including selecting the insulator layer having an electrically insulative material selected from the group of materials consisting of air, polystyrene, silicon dioxide, a biocompatible ceramic, a conductive dielectric material, a non-conductive dielectric material, a piezoelectric material, a pyroelectric material, a ferrite material, and combinations thereof."**

Partovi in view of Phan discloses or suggests this limitation. (Ex. 1002, ¶¶124-127.) As explained above, Partovi discloses an insulating layer positioned in the space between PCB layers 357. (*Supra* Section IX.A.1(d).) Therefore, Partovi discloses that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex. 1002, ¶124; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

While Partovi does not explicitly disclose what material is used for the insulating layer between PCB layers 357, it would have been obvious for a POSITA to use a non-conducting dielectric material. (Ex. 1002, ¶125.) Such non-conducting dielectric materials are commonly used in PCBs to provide the insulating layer between conducting layers. (*Id*.) For example, as discussed below, Phan discloses a non-conducting dielectric material that is used as an insulating layer between conductive layers in a PCB and a POSITA would have been motivated to combine the teachings of Partovi with Phan such that the insulating material in Partovi's PCB is a "non-conductive dielectric material." (*Id*.)

As discussed above, Phan like Partovi discloses a multi-layer PCB. (*Supra* Section IX.C.1.) Phan discloses "an insulating layer 316 of Kapton" positioned between conducting layers 306 and 308. (Ex. 1029, 5:40-50, FIG. 3.)

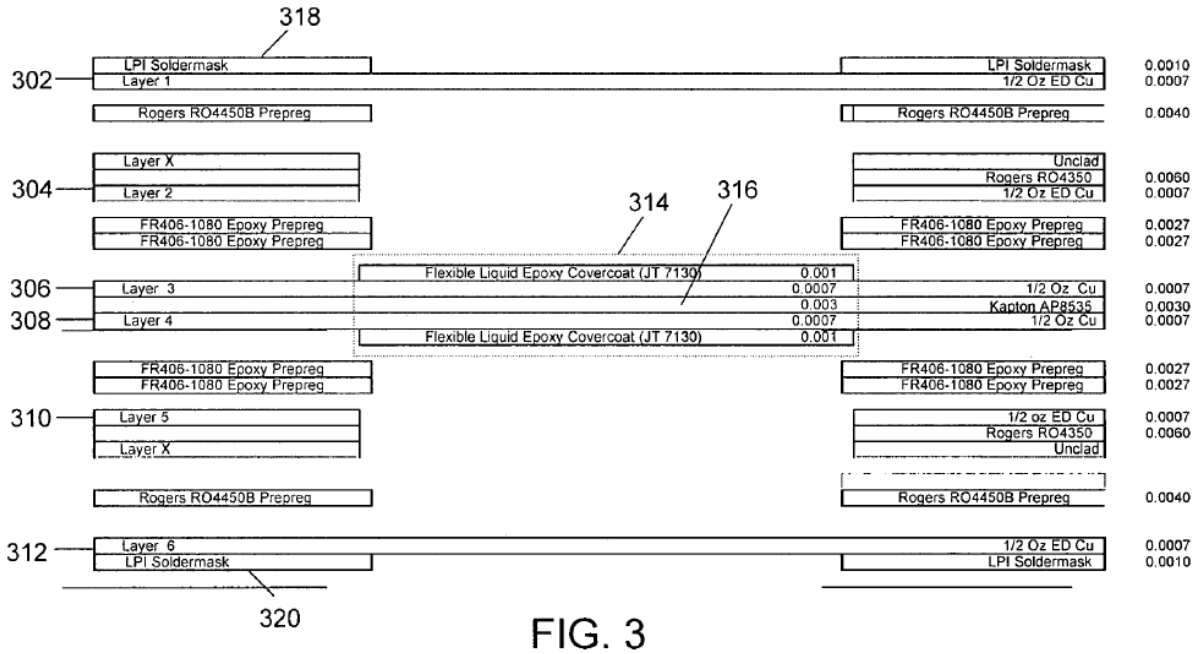


FIG. 3

(*Id.*, FIG. 3.)

Kapton is an "electrically insulative material." (Ex. 1032 at 9:3-4, 9:25-27; Ex. 1002, ¶126.) Kapton is also a "dielectric material." (Ex. 1030 at 2:60-61 ("dielectric layers such as Kapton ® polyimide"); Ex. 1032 at 9:3-4, 9:25-27.) Therefore, Kapton is a "non-conductive dielectric material." (Ex. 1002, ¶126.)

A POSITA would have found it obvious to use Kapton as the insulating material between Partovi's PCB layers 357. (Ex. 1002, ¶127.) In particular, a POSITA would have known that Kapton is a well-known insulating layer that is **flexible**. (*Id.*; Ex. 1029, 3:49-54.) Indeed, the use of Kapton in flexible PCBs is acknowledged by Partovi itself. (Ex. 1009, ¶[0355] ("flexible PCB material such as Kapton").) Given that there were several advantages to a flexible PCB (Ex.

1009, ¶¶[0137], [0151]), a POSITA would have found it obvious to use Kapton as the insulating material in the Partovi PCB. (Ex. 1002, ¶127.) *See Unwired Planet*, 841 F.3d at 1003-04 (affirming a finding of obviousness because a POSITA "could have seen the advantages of applying the teachings of a [secondary reference] to improve [the primary reference]"). Therefore, the Partovi-Phan combination discloses or suggests claim 28 because in the combination, the insulating layer is an "electrically insulative material" such as Kapton, which is a "non-conductive dielectric material." (Ex. 1002, ¶127.)

D. Ground 4: Partovi in View of Chiang Renders Obvious Claims 1-4, 10, 15-21, 24-27, 35, and 37-39

1. Claim 1

As discussed above in Section IX.A.1, Partovi discloses or suggests all of the limitations of claim 1. With respect to claim element 1[d], Partovi discloses "an insulator layer" that is positioned in the space between all four layers 357, including the space between the top two layers ("first conductor" and "second conductor"). (*Supra* Section IX.A.1(d).) To the extent that PO contends or the Board finds that the presence of such an "insulator layer" between the PCB layers 357 is not explicit or implied in Partovi, a POSITA would have been motivated to combine the teachings of Partovi with Chiang to provide an "insulator layer" between each of the PCB layers 357 to ensure they are electrically insulated from

each other and therefore, capable of functioning in an expected manner. (Ex. 1002, ¶129.)

Like Partovi, Chiang discloses techniques for forming inductors using a multi-layer printed circuit board (PCB). (Ex. 1023, 1:7-10, 4:67-5:9.) "An embodiment of an inductor according to the present invention formed on a six layer PCB and having two winding turns is shown in the exploded perspective view of FIG. 3 . . . ." (*Id.*, 6:19-23, FIG. 3.) Each of the six PCB layers (303) is separated from the other by an insulating layer 301. (*Id.*, 6:23-7:4, FIG. 3.) The PCB layers are connected with each other using "plated through holes" that are formed using "micro-**vias**." (*Id.*, 6:38-50 (emphasis added); *see also id.* at 6:23-7:4.) Therefore, as shown below, Chiang discloses "an insulator layer" (e.g., insulating layer 301d) positioned in the space between a first conductor layer (303d) and a second conductor layer (303c). (Ex. 1002, ¶130.)

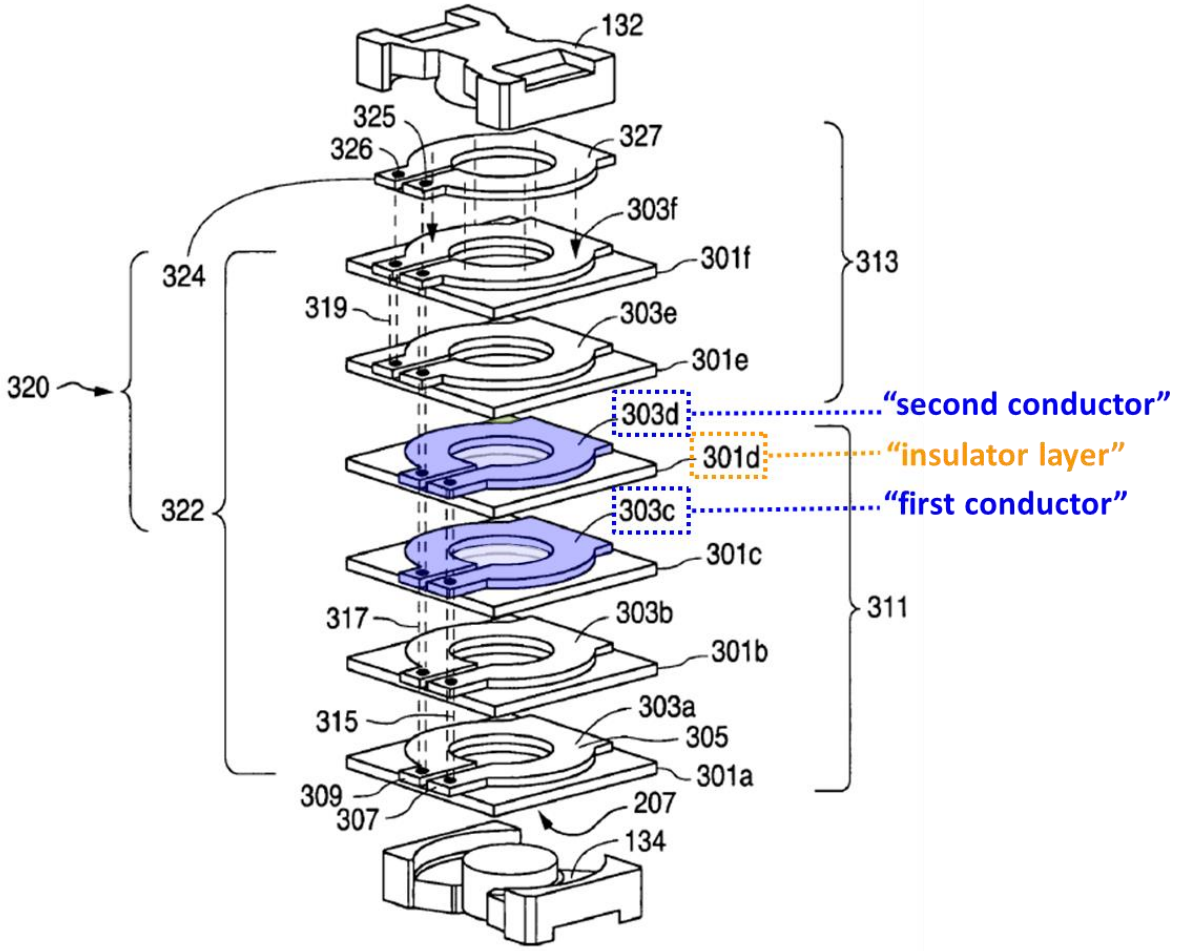


FIG. 3

(Ex. 1023, FIG. 3 (annotated); Ex. 1002, ¶130.)

A POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶131.) A POSITA seeking to implement Partovi's inductor would have looked to Chiang because both disclose PCB-based inductors. (*Id.*) Having looked to Chiang, a POSITA would have recognized that a typical multi-layer PCB includes conductor

layers separated from each other by an insulating layer and would have therefore combined the teachings of Partovi and Chiang to include insulating layers between each of the PCB layers 357 in figure 18 of Partovi. (*Id.*; Ex. 1028 at 1:8-20.) A POSITA would have been motivated to do so because such a configuration was typical for PCBs and required in order to ensure that adjacent PCB layers are not shorted. (Ex. 1002, ¶131.) If an insulating layer did not exist between two PCB layers then those two layers would be just one layer and not "separate" as disclosed by Partovi. (Ex. 1009, ¶[0224]; Ex. 1002, ¶131.) Indeed, using an insulating layer between two PCB layers 357 in figure 18 of Partovi would have been nothing more than the combination of familiar elements according to known techniques yielding the predictable result of a functional PCB-based inductor. (Ex. 1002, ¶131.) *KSR*, 550 U.S. at 416-21.

Partovi in combination with Chiang discloses or suggests the remaining limitations of claim 1 for the reasons discussed above for claim 1 with the only modification to the analysis for claim 1 being that discussed immediately above. (*Supra* Section IX.A.1; Ex. 1002, ¶132.)

2. Claim 18

a) **"The method of claim 1 including connecting electrically at least the one connector to the first conductor and the second conductor in parallel or series."**

Partovi in view of Chiang discloses or suggests this limitation. (Ex. 1002, ¶¶133-140.) Partovi discloses or suggest implementing the inductor coil L1 ("inductor") in figure 29 using a multi-layer PCB coil (e.g., coil 356 in figure 18 of Partovi). (*Supra* Section IX.A.1(c).) Therefore, for reasons similar to those discussed above in Sections IX.A.1(a)-(e),the top two layers 357 of Partovi's inductor discloses the claimed "first conductor," "second conductor," "insulator positioned in the space between the first conductor and the second conductor," and "at least one connector electrically connecting the first conductor and the second conductor," as shown in figure 18 below. (*Supra* Sections IX.A.1(a)-(e); Ex. 1009, FIG. 18; Ex. 1002, ¶133.)

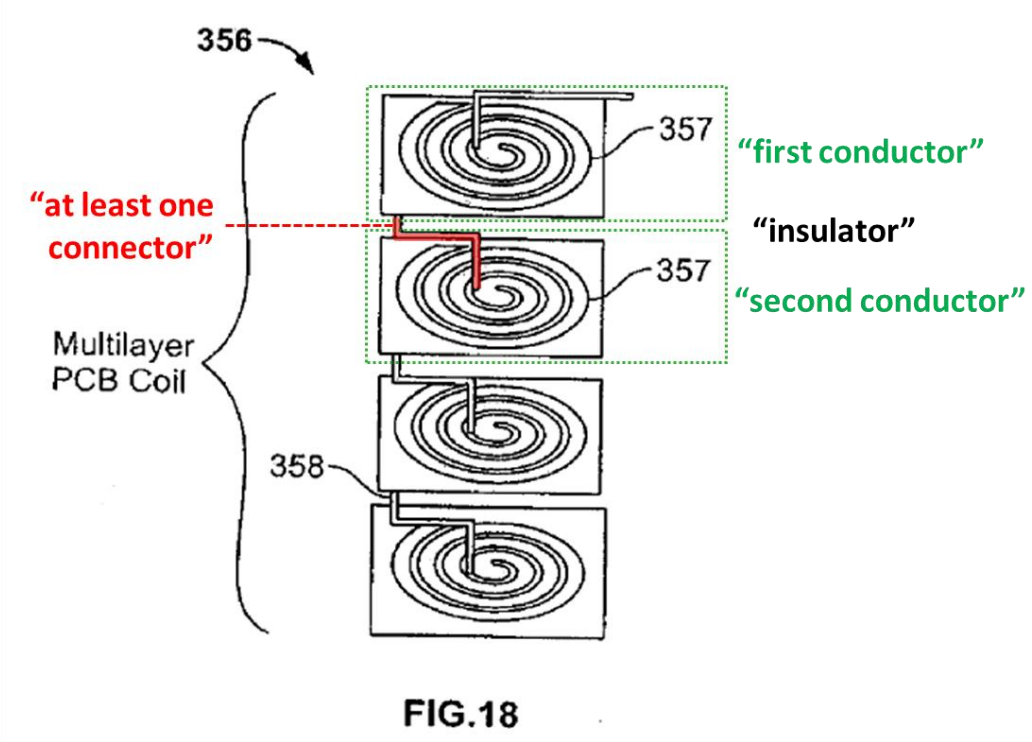


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶133.)

But Partovi does not explicitly disclose whether the disclosed "at least one connector" connects electrically to the first conductor and the second conductor **in parallel or series**. (Ex. 1002, ¶134.) Nonetheless, a POSITA would have found it obvious to implement such a feature in view of Chiang and the knowledge of such a person. (*Id.*.)

Like Partovi, Chiang discloses a multi-layer PCB inductor. (*See, e.g.*, Ex. 1023, Title, Abstract, 1:7-10, 4:20-22, 4:62-5:4, 6:19-23, FIGs. 3-5.) For example, Chiang discloses with reference to figure 3 (below) a winding 320 that includes a multi-layer PCB 322, which includes a first turn 311 and a second turn 313, collectively formed by six conducting layers 303a-303f and six insulating layers 301a-303f. (*Id.*at 6:23-30.) The two ends (307 and 309) on conducting layer 303 are "interconnected through the insulating layers . . . by one or more plated through holes formed therein." (*Id.*, 6:37-40; *see also id.* at 6:30-37; Ex. 1002, ¶135.)

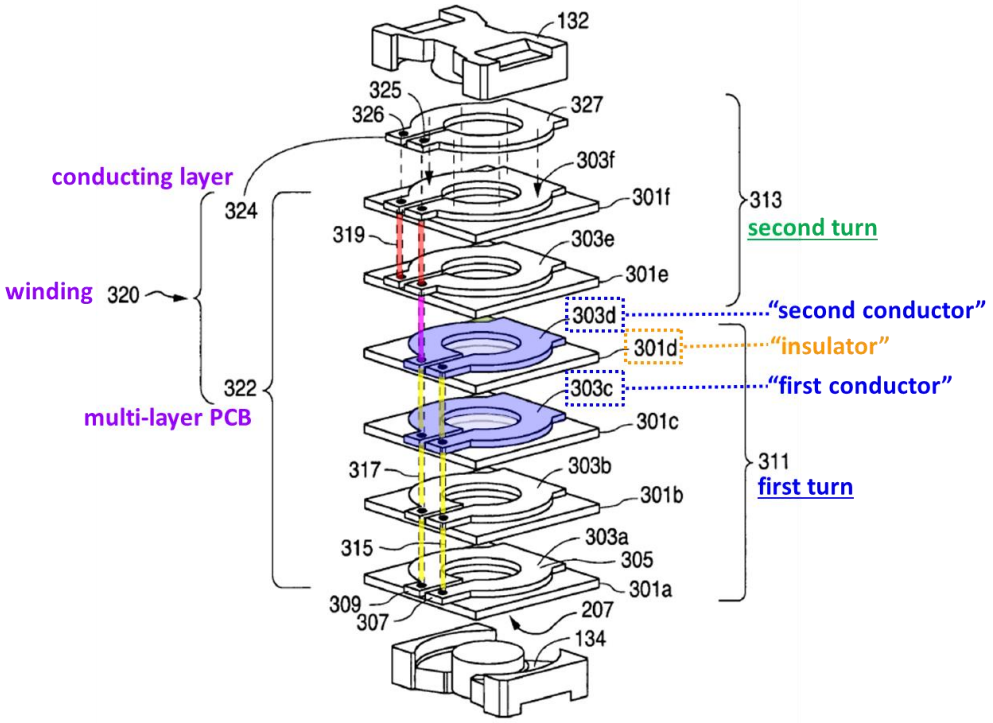


FIG. 3

(Ex. 1023, FIG. 3 (annotated); Ex. 1002, ¶135.)

Accordingly, similar to Partovi, Chiang also discloses "a first conductor" (conducting layer 303c), "a second conductor" (conducting layer 303d) that is spaced apart from the first conductor layer. (Ex. 1002, ¶136; Ex. 1023, 1:43-46 (disclosing that "[i]n a multi-layer PCB, a PCB winding is formed from a plurality of patterned conductive traces, typically of copper"), FIG. 4 (indicating the conducting layers 303 are made of copper), 6:51-7:4.) Chiang likewise discloses that "an insulator layer" (insulating layer 301d) is positioned in the space between

the first conductor and the second conductor. (*See e.g.*, Ex. 1023, 6:51-7:4; Ex. 1002, ¶136.)

Furthermore, Chiang discloses that conducting layers may be "**connected in parallel to decrease the impedance** of a particular turn of the winding." (Ex. 1023, 1:62-64 (emphasis added).) For example, Chiang discloses that conducting layer 303c ("first conductor") and conducting layer 303d ("second conductor") are electrically connected in parallel by plated through holes 315 and 317 ("at least the one connector"). (Ex. 1023, 7:5-14; *see also id.* at 6:51-7:4.) Conducting layers 303c and 303d are also connected in parallel with conducting layers 303a and 303b, thereby forming a first turn 311 as shown in figure 5 below. (*Id.*, FIG. 5, 7:5-14; Ex. 1002, ¶137.)

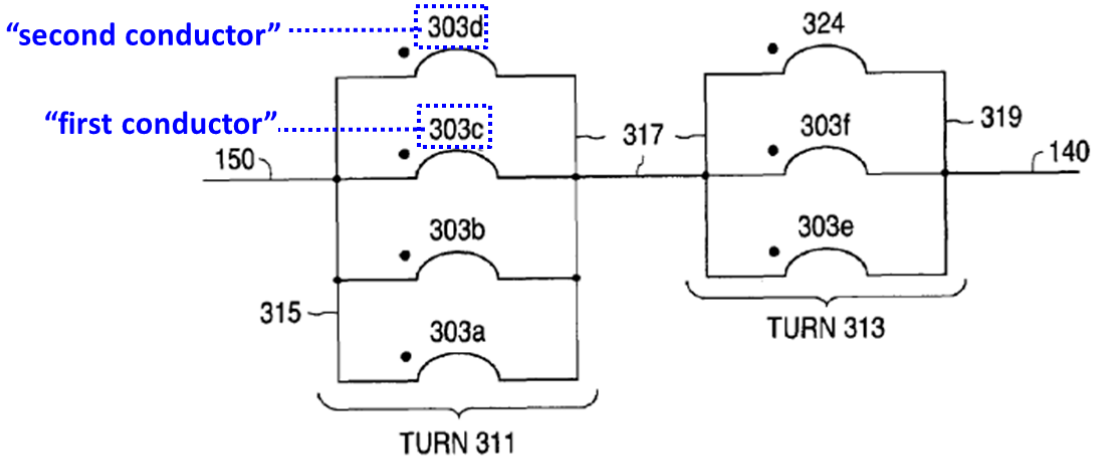


FIG. 5

(Ex. 1023, FIG. 5 (annotated); Ex. 1002, ¶137.)

Based on the combined teachings of Partovi and Chiang, a POSITA would have had reasons to consider the teachings of Chiang when contemplating the features disclosed by Partovi. (Ex. 1002, ¶138.) A POSITA seeking to implement Partovi would have looked to Chiang because both disclose PCB-based inductors. (*Id*.) And, based on those disclosures, such a skilled person would have found it obvious to modify the multi-layer coil 356 in figure 18 of Partovi such that the PCB layers 357 (including the "first conductor" and the "second conductor") are electrically connected **in parallel** using two connectors ("at least the one connector"), like plated through holes 315 and 317 in Chiang. (*Id.*) As discussed below, a POSITA would have been motivated to do so because it would have decreased the resistance of the coil. (*Id.*)

Partovi discloses that while multiple layers of PCB coils can be stacked for "compact fabrication" of high flux density coils (Ex. 1009, ¶[0212], FIG. 18), such a configuration has some drawbacks. (Ex. 1002, ¶139.) Notably, Partovi discloses that "[w]hile larger values [of inductance] can be obtained by increasing the number of turns or stacking a number of coils vertically and connecting them in series, this larger induction **comes at the price of increased resistance and therefore loss in the inductor**." (Ex. 1009, ¶[0255] (emphasis added).) Partovi notes that "for the power efficiency to be maximized and to minimize losses in the coil, the coils should be manufactured to have as low a resistance as possible."

(*Id.*, ¶[0167].) As such, a POSITA would have been motivated to utilize a parallel connection between the PCB layers 357 in Partovi because doing so would have improved the performance of the circuit by, e.g., **reducing resistance** and loss of the inductor. (Ex. 1002, ¶139; Ex. 1023, 1:62-64; *see also* Ex. 1025 at ¶¶[0030] (explaining that forming an inductor using two conducting layers connected in parallel halves the resistance of the inductor by doubling the cross-sectional area of the inductor), [0036] (explaining that such an inductor may be formed by PCB laminations).) *See Unwired Planet*, 841 F.3d at 1003-04.

Additionally, a POSITA would have the knowledge and skill to modify the disclosed coil of Partovi in view of Chiang. (Ex. 1002, ¶140.) In fact, the '591 patent admits that multi-layer inductors "can be relatively easily achieved by existing manufacturing techniques (for example multi-layer printed wiring board, FIG. 21), and can therefore be integrated with other circuit components such as ICs, resistors, capacitors, surface mount components, etc." (Ex. 1001, 31:37-42; Ex. 1002, ¶140.) Therefore, a POSITA would have understood and appreciated that the proposed Partovi-Chiang combination involved a combination of known prior art elements and technologies (e.g., the multi-layer inductor disclosed by Chiang having conductor layers connected parallel and a multi-layer inductor like in Partovi) according to known methods (e.g., connecting two conductors in parallel using connectors) to yield the predictable result of a circuit with an

improved efficiency and a reduced resistance. (Ex. 1002, ¶140.) *See KSR*, 550 U.S. at 416. Accordingly, the Partovi-Chiang combination discloses or suggests claim 18.

3. Claim 20

a) **"The method of claim 1 including providing a third conductor and a fourth conductor electrically connected in parallel or series, wherein the first and second conductors are connected electrically in parallel or series and are further electrically connectable in series or parallel with the third and fourth conductors."**

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶¶141-149.) As shown below, the bottom two PCB layers in Partovi's PCB coil 356 constitute a "third conductor" and a "fourth conductor," and they are electrically connected by a connector 358. (Ex. 1009, ¶¶ [0212]-[0224], FIG. 18; Ex. 1002, ¶141; ; *see also supra* Section IX.A.1(c).)

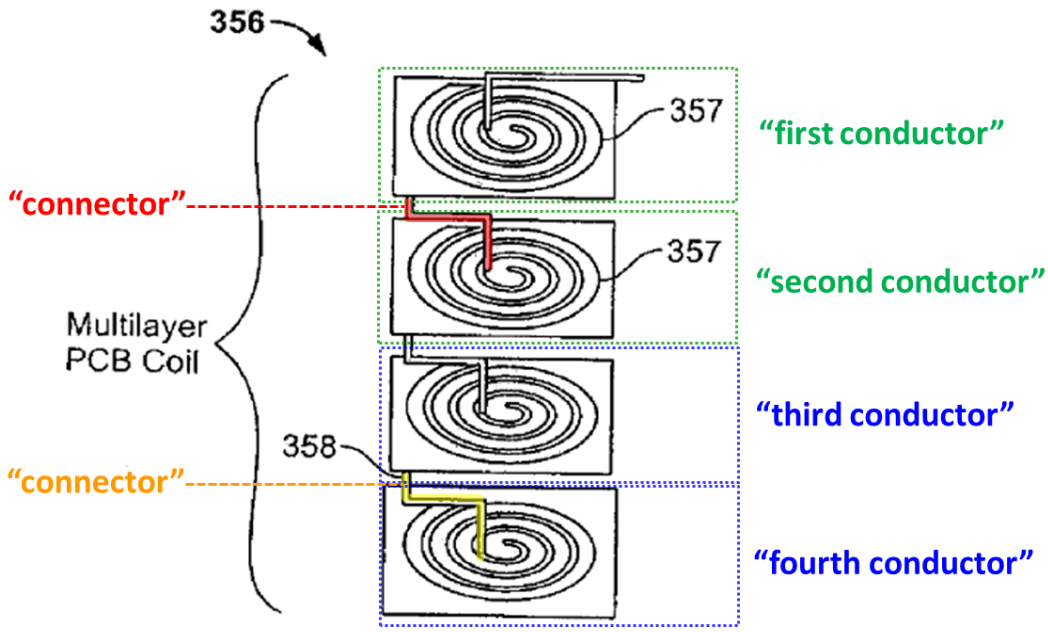


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶141.)

Partovi, however, does not explicitly disclose that the connector 358 connects the third and fourth conductor layers **in parallel or series**. (Ex. 1002, ¶142.) Chiang, however, discloses a third and a fourth conductor layer that are connected in parallel. (*Id.*) For example, as shown in figure 3 above, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023, FIG. 3, 7:5-14; *see also id.* at FIG. 5.)

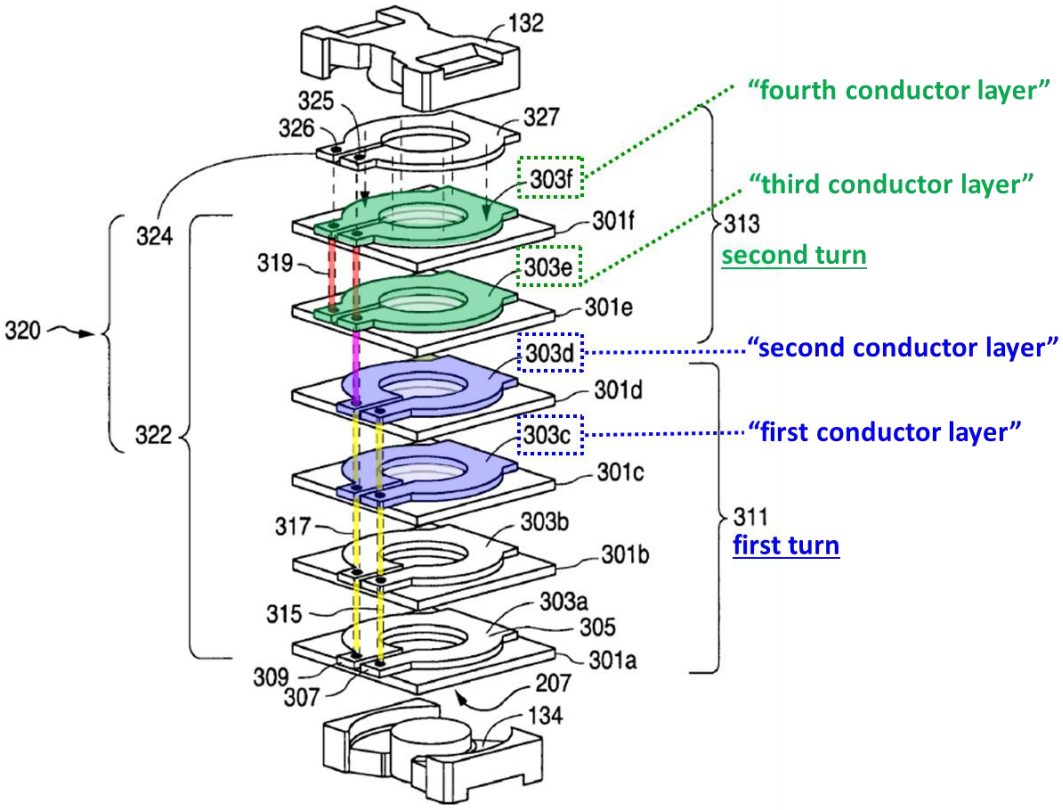


FIG. 3

(Ex. 1023, FIG. 3 (annotated); Ex. 1002, ¶142.) Therefore, Chiang discloses "providing a third conductor and a fourth conductor electrically connected in parallel or series." (Ex. 1002, ¶142.)

As discussed above in Section IX.D.2 (claim 18), a POSITA would have found it obvious to connect two PCB layers 357 ("first conductor" and "second conductor") in parallel to reduce series resistance of the inductor in view of the disclosure of Chiang, e.g., figure 3, reproduced above. (*See supra* Section IX.D.2.) For similar reasons, a POSITA would have found it obvious to connect the bottom

two PCB layers 357 (corresponding to "third conductor" and "fourth conductor") in figure 18 of Partovi in parallel. (*Id.*; Ex. 1002, ¶143.)

Accordingly, the Partovi-Chiang combination discloses or suggests "providing a third conductor and a fourth conductor electrically connected in **parallel** or series, wherein the first and second conductors are connected electrically in **parallel** or series." (*Id.* (emphases added).) The Partovi-Chiang combination thus far may be illustrated as follows:

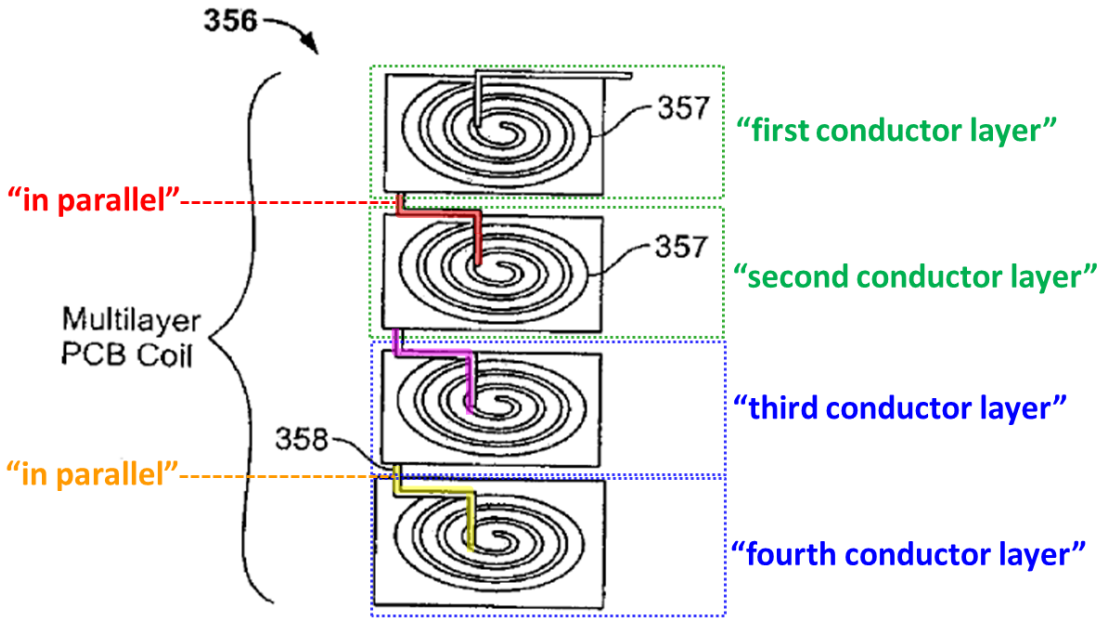


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶144.) As seen in the demonstrative above, the first and second conductors are connected in parallel, and the third and fourth conductors are connected in parallel.

While, as seen in the above demonstrative, the first and second conductors are connected with the third and fourth conductors through a connector (highlighted in pink), Partovi does not explicitly disclose whether the connector (pink) is a series or parallel connection. (Ex. 1002, ¶145.) Nevertheless, as explained below, a POSITA would have found it obvious to implement the connector (pink) as a series connection to increase the inductance of the inductor coil. (*Id*.)

Partovi discloses that the inductance of a coil increases with the number of turns. (Ex. 1009, ¶¶[0250]-[0254] (showing that inductance L is proportional to number of turns N).) Partovi also discloses that "a larger induction" may be created by "stacking a number of coils vertically and **connecting them in series**." (*Id.*, ¶[0255].) But Partovi recognizes that a balanced approach is needed. For example, Partovi explains that if coils are connected in series, the inductance increases because the number of turns increases, but such a series connection also results in an increase in the resistance. (Ex. 1009, ¶[0255].) In view of the above, a POSITA would have for example, connected the top two layers 357 ("first and second conductors") in parallel to form a first turn; and connected the bottom two layers 357 ("the third and fourth conductors") also in parallel to form a second turn, where the parallel connection would have reduced the resistance of each of the turns. (*Id.*; Ex. 1002, ¶146.) Additionally, to increase inductance of the

inductor, such a person would have connected the two turns in series, to form an inductor of multiple turns, each turn having multiple layers. (Ex. 1002, ¶146.)

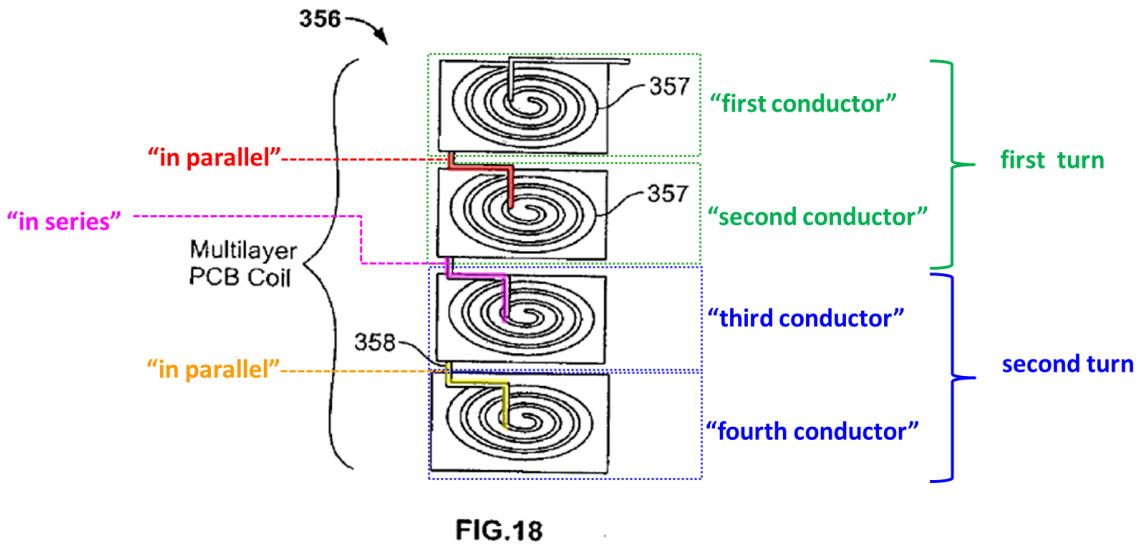


FIG.18

(Ex. 1009, FIG. 18; Ex. 1002, ¶146.)

Such an approach is consistent with Chiang's disclosure where two turns are created by connecting stacked conductor layers in parallel. (Ex. 1002, ¶147.) For example, as shown in figure 3 below, Chiang discloses an inductor winding, including two turns, where the first turn includes conducting layers 303a-303d connected in parallel, and the second turn includes conducting layers 303e-303f also connected in parallel. (Ex. 1023, FIG. 3, 7:5-14; *see also id.* at FIG. 5.) The two turns are connected in series because only a single through hole (via) that is highlighted in pink between layers 303d and 303e connects the two turns when two

through holes connect the layers that are connected in parallel (highlighted in red and yellow). (*See id.* at FIG. 3 below.)

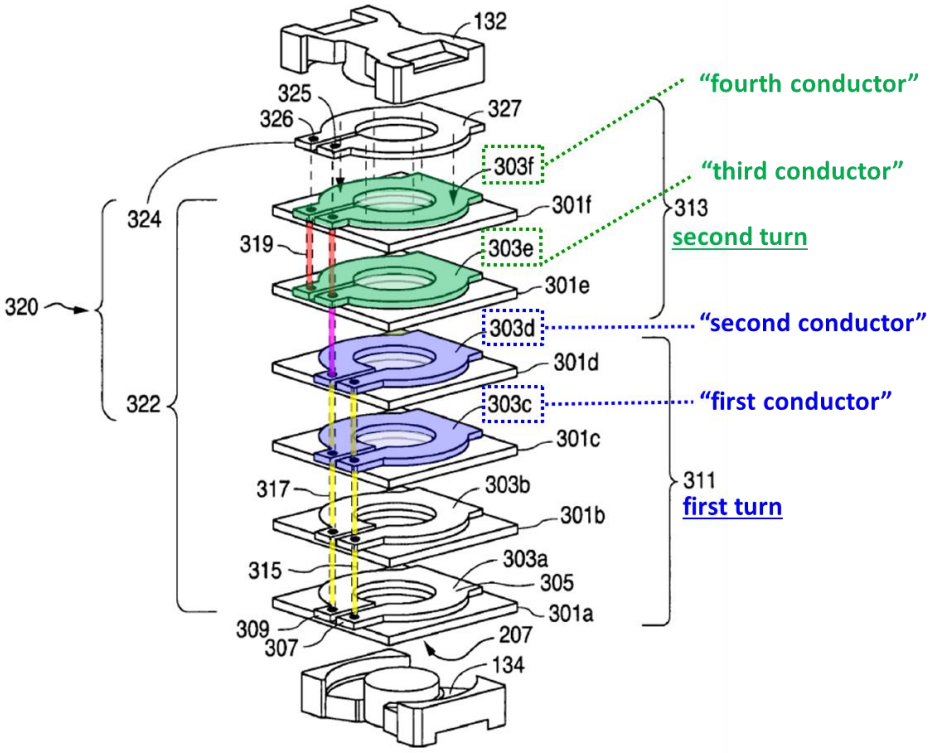


FIG. 3

(Ex. 1023, FIG. 3 (annotated); Ex. 1002, ¶147.)

As such, based on the teachings of Partovi and Chiang, a POSITA would have been motivated to take a balanced approach, i.e., to include additional turn(s) in an inductor winding to **increase inductance**, while having the added turns be constructed with layers connected in parallel to **reduce series resistance**. (Ex. 1002, ¶148.) And, based on those disclosures, such a skilled person would have found it obvious to connect the top two PCB layers 357 in parallel, connect the

bottom two PCB layers 357 in parallel, and implement a series connection between them. (*Id.*) *See KSR*, 550 U.S. at 416.

Accordingly, the Partovi-Chiang combination discloses or suggests claim 20. (Ex. 1002, ¶149.)

4. Claim 27

a) **"The method of claim 1 including providing at least one insulator layer of an electrically insulative material."**

Partovi in combination with Chiang discloses or suggests this limitation because as discussed above in Section IX.D.1, an insulating layer is included between each PCB layer 357 in the Partovi-Chiang combination. (*Supra* Section IX.D.1; Ex. 1002, ¶151.) Therefore, Partovi discloses that the insulating layer is an "electrically insulative material" because in the context of PCBs, a POSITA would have understood that an insulating layer provided between conductive layers is electrically insulating. (Ex. 1002, ¶151; Ex. 1028 at 1:6-23 ("Insulating layers electrically isolate conductive layers from one another.").)

5. Claims 2-4, 10, 15-17, 19, 21, 24-26, 37, and 38

Partovi in combination with Chiang discloses or suggests the limitations of these claims for reasons similar to those discussed in Sections IX.A.2-IX.A.13 and IX.A.15-IX.A.16. (*Supra* Sections IX.A.2-13, IX.A.15-16; Ex. 1002, ¶151.) The same analysis presented above for these claims in Ground 1 is also applicable for the Partovi-Chiang combination discussed above in Section IX.D.1. (Ex. 1002,

¶151.) The combination of Chiang with Partovi does not affect the analysis for these claims in Section IX.A. (*Id.*)

6. Claim 35

a) **"A method of operating an electrical circuit, the method comprising the following steps:"**

Partovi discloses this limitation for reasons similar to those discussed in Section IX.A.1(a) (claim 1 preamble). (*Supra* Section IX.A.1(a); Ex. 1002, ¶152.)

b) **"a) providing an electrical circuit electrically connectable to a power source, the electrical circuit comprising at least an inductor, comprising:"**

Partovi discloses this limitation for reasons similar to those discussed in Section IX.A.1(b). (*Supra* Section IX.A.1(b); Ex. 1002, ¶153.) For example, the charger in figure 29 of Partovi contains an electrical circuit (inductor L1, FET Q1, and current sense). First, the electrical circuit is electrically connectable to a bus ("power source") that provides the input voltage to the electrical circuit. (*Supra* Section IX.A.1(b); Ex. 1002, ¶153.) Second, the electrical circuit is electrically connectable to voltage regulator 1 and Q2, the combination of which also constitute a "power source" because they output a voltage to the electrical circuit. (Ex. 1009, ¶¶[0272]-[0273], FIG. 29; Ex. 1002, ¶153.)

c) **"a.i) a first inductor subassembly comprising a first conductor; a.ii) a second conductor spaced apart from the first conductor, the first conductor and the second conductor being electrically conductive; a.iii) a first insulator positioned in the space between the first**

conductor and the second conductor; a.iv) a first connector electrically connecting the first conductor and the second conductor in parallel or series;"

Partovi in combination with Chiang discloses or suggests this limitation. (Ex. 1002, ¶¶154-155.) As discussed above in Sections IX.D.1-3 (claims 1, 18 and 20), the Partovi-Chiang combination discloses forming a "first inductor subassembly, as shown in figure 18 below. (*Supra* Sections IX.D.1-3.)

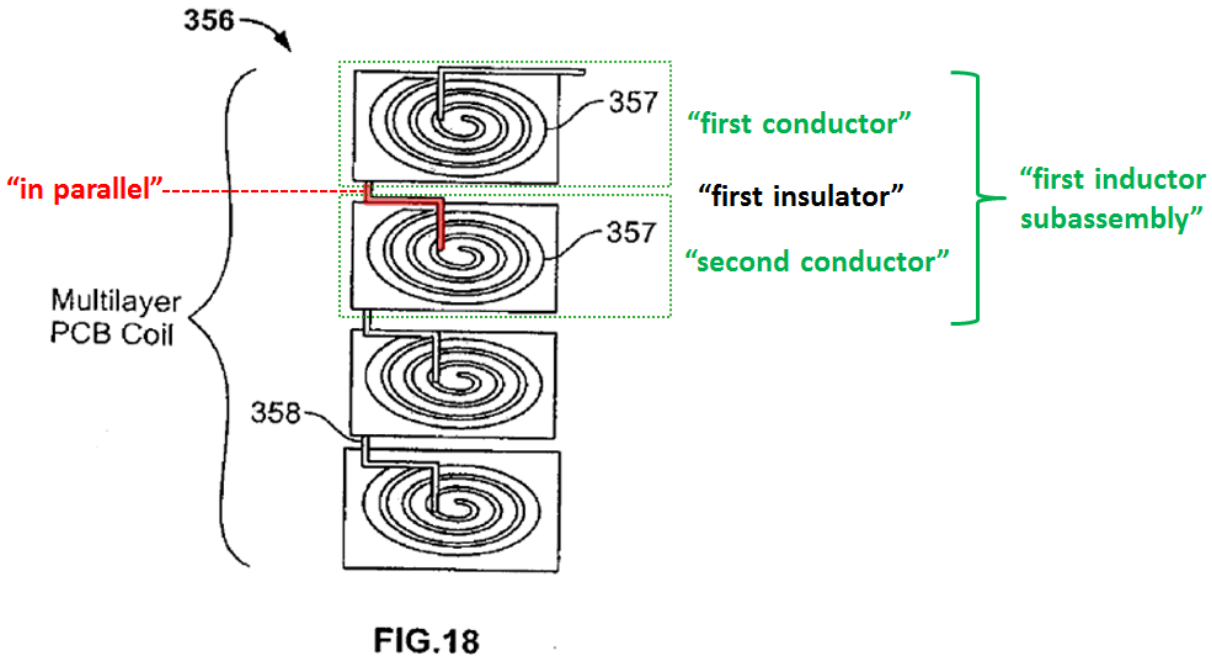


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶154.) The "first inductor subassembly includes the top two layers 357, which may be made of copper, that are spaced apart from each other ("a first conductor" and "a second conductor spaced apart from the first conductor, the first conductor and the second conductor being "electrically conductive"). (Ex. 1002, ¶154; *supra* Section IX.A.1(c).)

The "first inductor subassembly" also includes an insulating layer positioned in the space between the top two layers 357 ("a first insulator positioned in the space between the first conductor and the second conductor"). (*See supra* Sections IX.A.1(c)-(d), IX.D.1; Ex. 1002, ¶155.) Moreover, the first subassembly includes two connectors that electrically connect the top two layers 357 in parallel ("a first connector electrically connecting the first conductor and the second conductor in parallel or series"). (*Supra* Section IX.D.2; Ex. 1002, ¶155.)

d) **"a.v) a second inductor subassembly comprising a third conductor and a fourth conductor spaced apart from the third conductor, the third conductor and the fourth conductor being electrically conductive;**

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶156.) As discussed above in Sections IX.D.1-3 (claims 1, 18 and 20), the Partovi-Chiang combination discloses forming a "second inductor subassembly", as shown in figure 18 below. (*Supra* Sections IX.D.1-3.)

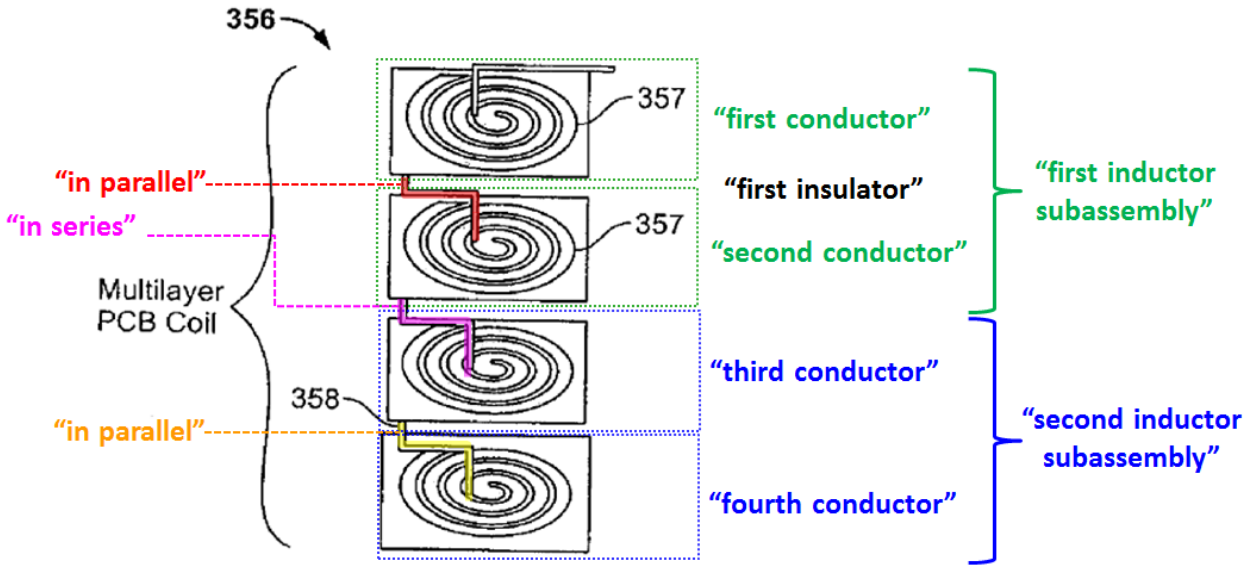


FIG.18

(Ex. 1009, FIG. 18 (annotated); Ex. 1002, ¶156.) The "second conductor subassembly" includes the bottom two layers 357, which may be made of copper, that are spaced apart from each other ("a third conductor" and "a fourth conductor spaced apart from the third conductor, the third conductor and the fourth conductor being electrically conductive). (Ex. 1002, ¶156; Ex. 1009, ¶¶[0224]-[0225] (disclosing that the PCB layers 357 are formed from copper, are "separate," and connected with each other through vias and contacts).)

e) **"a.vi) a second insulator layer positioned in the space between the third conductor and the fourth conductor layers conductors; and"**

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶157.) As discussed in Section IX.D.1 (claim 1), the Partovi-Chiang combination discloses providing an "insulator layer" between each of the PCB

layers 357 to ensure they are electrically insulated from each other and therefore, capable of functioning in an expected manner. (*See supra* Section IX.D.1 (claim 1).) Accordingly, the Partovi-Chiang combination discloses a "second insulator layer" positioned in the space between the bottom two layers 357 ("third conductor and the fourth conductor layers"). (Ex. 1002, ¶157.)

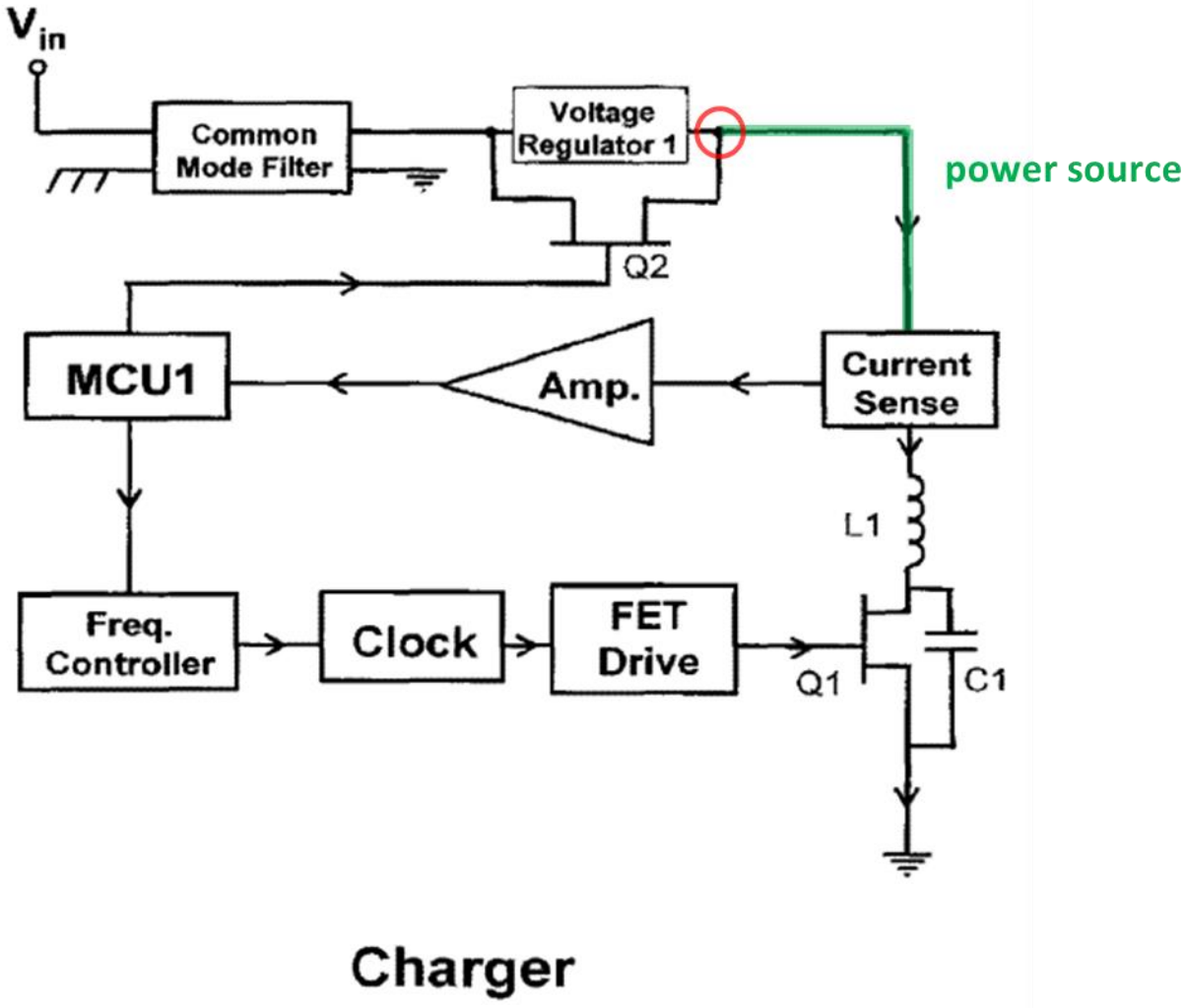
f) **"a.vii) a second connector electrically connecting the third conductor and the fourth conductor in parallel or series, wherein the first inductor subassembly is electrically connectable in series or parallel to the second inductor subassembly;"**

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002, ¶¶158-159.) As discussed in Section IX.D.3 (claim 20), the Partovi-Chiang combination discloses using two connectors ("a second connector") to electrically connect the bottom two layers ("the third conductor and the fourth conductor") in parallel. (Section IX.D.3 (claim 20); Ex. 1002, ¶158.)

Moreover, as discussed in the same section, the Partovi-Chiang combination discloses the "first inductor subassembly" is electrically connected in series to the "second inductor subassembly." (Section IX.D.3 (claim 20); Ex. 1002, ¶159.) Accordingly, the Partovi-Chiang combination discloses these limitations. (Ex. 1002, ¶159.)

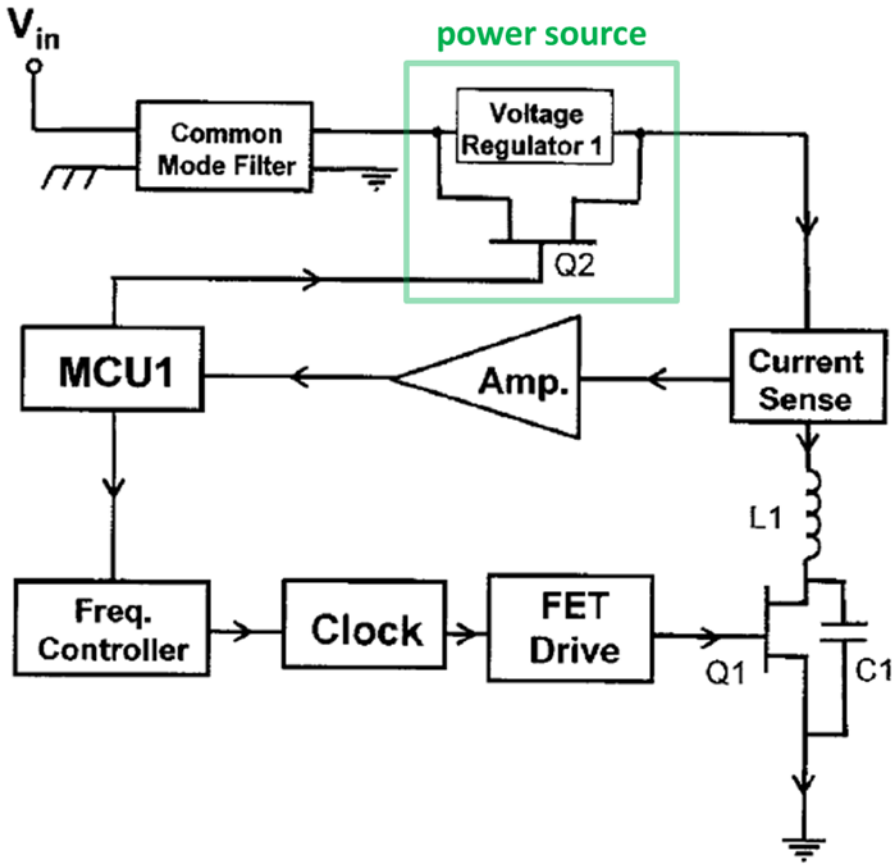
g) **"b) adjusting a power level of the power source;"**

The Partovi-Chiang combination discloses this limitation in two ways. (Ex. 1002, ¶¶160-162.) **First**, Partovi discloses adjusting an input power level ("a power level") of the power source (e.g., the wire/bus connecting Q2 with the current sense circuit) as described above for claim element 1[f]. (*See supra* Section IX.A.1(f).)



(Ex. 1009, FIG. 29 (excerpt, annotated); Ex. 1002, ¶160.)

Second, Partovi also discloses that the combination of voltage regulator 1 or Q2 also constitutes a "power source" because they output a voltage to the first electrical circuit. (Ex. 1009, ¶¶[0272]-[0273], FIG. 29.) For example, one of voltage regulator 1 or Q2 is switched on to change the input voltage of the inductor coil L1. (*Id.*) Because the combination of these two circuit elements provides a voltage (and therefore, current) to the inductor coil L1, the combination of voltage regulator 1 and Q2 is a "power source." (Ex. 1002, ¶161.)



Charger

(Ex. 1029, FIG. 29 (excerpt, annotated); Ex. 1002, ¶162.)

Partovi discloses adjusting the voltage level ("adjusting a power level of the power source") output by the combination of voltage regulator 1 and Q2 ("power source") based on the power needs of the receiver. (Ex. 1009, ¶¶[0272]-[0273].) Accordingly, the Partovi-Chiang combination discloses this limitation. (Ex. 1002, ¶162.)

h) **"c) adjusting an electrical circuit operating frequency to at least about 3 kHz; d) propagating an electrical current within at least the first conductor; e) changing at least one of a frequency, a magnitude, or a waveform shape of the electrical current such that a magnetic flux is generated; and f) selecting an adjustable inductor quality factor."**

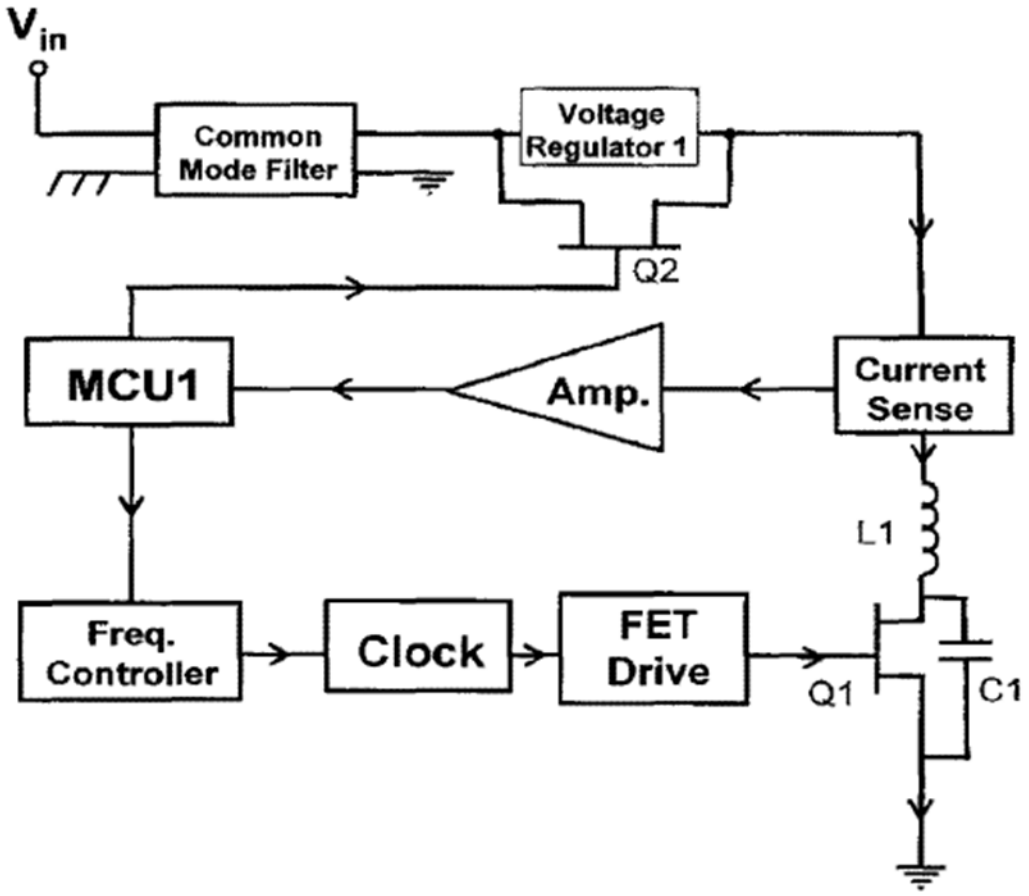
The Partovi-Chiang combination discloses or suggests these limitations for reasons similar to those discussed in Sections IX.A.1(g)-(j). (*See supra* Sections IX.A.1(g)-(j); Ex. 1002, ¶163.)

7. Claim 39

a) **"The method of claim 35 including providing a control circuit electrically connectable to the inductor and/or another electrical component comprising the electrical circuit."**

The Partovi-Chiang combination discloses or suggests this limitation. (Ex. 1002 ¶164.) For example, Partovi discloses a micro control unit (MCU1) that controls, via the frequency controller, clock, and FET drive, the frequency at which FET Q1 switches. (Ex. 1029, FIG. 29, ¶¶[0263]-[0265].) Because FET Q1 is a

component included in the "electrical circuit" (*see supra* Section IX.D.6(b)), Partovi discloses a "control circuit" electrically connectable to "another electrical component comprising the circuit." (Ex. 1002, ¶164.)



(Ex. 1009, FIG. 29 (excerpt).)

E. Ground 5: Partovi in View of Chiang and Tseng Renders Obvious Claims 6, 7, and 13

As discussed above in Section IX.D.1, Partovi in view of Chiang discloses or suggests all of the limitations of claim 1. But the Partovi-Chiang combination does not explicitly disclose the limitations of claims 6, 7, and 13. Tseng, however, discloses such limitations. (*Supra* Section IX.B.) Therefore, a POSITA would have combined the teachings of Partovi and Chiang with Tseng for the same reasons that a POSITA would have combined the teachings of Partovi with Tseng that renders these claims obvious (*supra* Section IX.B). (Ex. 1002, ¶¶165-166.)Therefore, the Partovi-Chiang-Tseng combination renders these claims obvious for reasons similar to those discussed above in Section IX.B. (*Id*.)

F. Ground 6: Partovi in View of Chiang and Phan Renders Obvious Claims 8, 12, 27, and 28

As discussed above in Section IX.D.1, Partovi in view of Chiang discloses or suggests all of the limitations of claim 1. But to the extent that the Partovi-Chiang combination does not explicitly disclose the limitations of claims 8, 12, 27, and 28, a POSITA would have combined the teachings of Partovi and Chiang with Phan for the same reasons that a POSITA would have combined the teachings of Partovi with Phan (*supra* Section IX.C). (Ex. 1002, ¶¶167-168.) Therefore, the Partovi-Chiang-Phan combination renders these claims obvious for reasons similar to those discussed above in Section IX.C. (*Id*.) Indeed, Chiang's teachings are

consistent with Phan's because both disclose multi-layer PCBs in which conducting layers are separated by insulator layers. (Ex. 1023, 6:23-7:4, FIG. 3; Ex. 1029, 5:40-50, FIG. 3; Ex. 1002, ¶168.)

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1-4, 6-8, 10, 12, 13, 15-21, 24-28, 35, and 37-39 of the '591 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,698,591 contains, as measured by the word-processing system used to prepare this paper, 13,293 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: March 22, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 22, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,698,591 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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Washington, D.C. 20001

A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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