UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.
Petitioner

v.

VENKAT KONDA
Patent Owner

Patent No. 8,269,523

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,269,523

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I. INTRODUCTION

Flex Logix Technologies, Inc. ("Petitioner") requests *inter partes* review ("IPR") of claims 1, 15-18, 20-22, 32, and 47 ("the challenged claims") of U.S. Patent No. 8,269,523 ("the '523 patent") (Ex. 1001), which, according to PTO records, is assigned to Venkat Konda ("Patent Owner" or "PO"). For the reasons below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc. as the real party-in-interest.

B. Related Matters

1. Litigations and PTAB Proceedings

PO has asserted the '523 patent against Petitioner in *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581 (N.D. Cal.). PO has also asserted U.S. Patent Nos. 8,898,611 ("the '611 patent"), 9,529,958 ("the '958 patent"), 10,050,904 ("the '904 patent"), 10,003,553 ("the '553 patent") in the foregoing district court litigation. The '553 patent is the subject of pending instituted post-grant review (PGR) proceedings PGR2019-00037 and PGR2019-00042, and another PGR petition (in PGR2019-00040) regarding the '553 patent was previously

denied.

2. Related Applications

The '523 patent issued from U.S. Application No. 12/601,275 ("the '275 application"), which is a national stage entry of International Application PCT/US2008/064605, and claims priority to U.S. Provisional Application No. 60/940,394 filed May 25, 2007.[1] Pending U.S. Application No. 16/202,067 claims priority to the '275 application, according to the PTO PAIR database.

3. Concurrently-filed petitions

Petitioner is concurrently filing two additional petitions for IPR of certain claims of the '523 patent.

C. Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,

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[1] Petitioner does not concede that the national stage was properly entered or that the '523 patent properly issued, and reserves the right to assert such issues in other forums. (*See, e.g.*, Ex. 1004, 1-2, 148-159.)

email: PH-FlexLogix-Konda-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(a)

Petitioner certifies that the '523 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1, 15-18, 20-22, 32, and 47 ("challenged claims") of the '523 patent, and cancellation of these claims as unpatentable.

B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 1, 16, 20-22, and 32 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as being anticipated by Published PCT Application No. WO 2008/109756 ("*Konda '756 PCT*") (Ex. 1009).

Ground 2: Claims 15 and 17 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Konda '756 PCT*.

Ground 3: Claims 18 and 47 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Konda '756 PCT* in view of U.S. Patent No. 6,940,308 to Wong ("*Wong*") (Ex. 1008).

As discussed below, *Konda '756 PCT* and *Wong* qualify as prior art and are properly relied upon for showing unpatentability of the '523 patent.

1. Earliest Effective Filing Date of '523 Patent

The '523 patent issued from U.S. Application No. 12/601,275 ("the '275 application"), which claims priority to U.S. Provisional Application No. 60/940,394 ("the '394 provisional") filed May 25, 2007 and is a national stage entry of International Application PCT/US2008/064605 ("the '605 PCT"), which was filed May 22, 2008 (Ex. 1007 is the as-filed body of the application) and published as International Publication No. WO2008/147928 (Ex. 1005). However, the '523 patent is not entitled to claim priority to May 25, 2007 or to May 22, 2008, because as explained below, the claims of the '523 patent are not fully supported, and also are not enabled, by the '394 provisional or the '605 PCT (collectively, "the priority applications"). (Ex. 1002, ¶¶40-67.) Therefore, the earliest effective filing date for the '523 patent is November 22, 2009, which is the date of filing of the U.S. national

stage application (i.e., the '275 application, *see* Ex. 1004, 158). (Ex. 1004, 150-158).

In order for a claim in a U.S. application to be entitled to the benefit of the filing date of an earlier filed U.S. or PCT application, the following two requirements (among others) must be met. First, the subject matter of the claim must be disclosed in the earlier-filed application in accordance with the written description requirement of Section 112. *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) (subject matter disclosed for first time in a continuation application does not receive benefit of the parent's filing date); *see also In re Gosteli*, 872 F.2d 1008, 1010–11 (Fed. Cir. 1989). Second, the claim must also meet the enablement requirement of Section 112. *In re Hafner*, 410 F.2d 1403, 1406, (CCPA 1969) ("[T]o be entitled to the benefits provided by [35 U.S.C. § 120], the invention disclosed in the "previously filed" application must be described therein in such a manner as to satisfy all the requirements of the first paragraph of [35 U.S.C. §] 112, including that which requires the description to be sufficient to enable one skilled in the art to use the [invention]."). Here, neither of the foregoing two requirements are met. (Ex. 1002, ¶¶40-67.)

a) Lack of written description support in priority applications

To comply with the written description requirement, the specification or earlier-filed application "must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed Cir. 2005); *see also Lockwood*, 107 F.3d at 1572; *Allergan, Inc. v. Sandoz Inc.*, 796 F.3d 1293, 1308-09 (Fed. Cir. 2015). "The test requires an objective inquiry in to the four corners of the specification from the perspective" of a person of ordinary skill in the art ("POSITA"). *Ariad*, 598 F.3d at 1351. Whether the added subject matter is an obvious variant of the disclosed subject matter is irrelevant. *Lockwood*, 107 F.3d at 1572.

As explained below, A POSITA reviewing the priority applications would not have understood that the named inventor of the '523 patent was in possession of the subject matter recited in claim 1 of the '523 patent. (Ex. 1002, ¶44.) Therefore, the subject matter of claim 1 is not disclosed in the priority applications in accordance with the written description requirement.

Original claim 1 filed with the '275 application recites an integrated circuit device that includes a plurality of sub-integrated circuit blocks and a routing network, where:

> Said routing network comprising of a plurality of stages y , starting from the lowest stage to the highest stage; and

(Ex. 1004, 217.)

In addition to a plurality of stages, original claim 1 also includes, for each sub-integrated circuit block, a plurality of inlet links, a plurality of outlet links, a plurality of forward connecting links (each connecting a switch in a lower stage to a switch in the immediate succeeding higher stage), and a plurality of backward connecting links (each connecting a switch in a higher stage to a switch in the immediate preceding lower stage). (*Id*.) Original claim 1 further specifies that, in each of the forward and backward connecting links for each sub-integrated circuit block, there is a plurality of straight links and a plurality of cross links. (*Id*., 217-218.)

During prosecution, applicant amended claim 1 to read (in part) as follows:

> Said routing network comprising of a plurality of stages y , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y , where $y \geq 1$; and

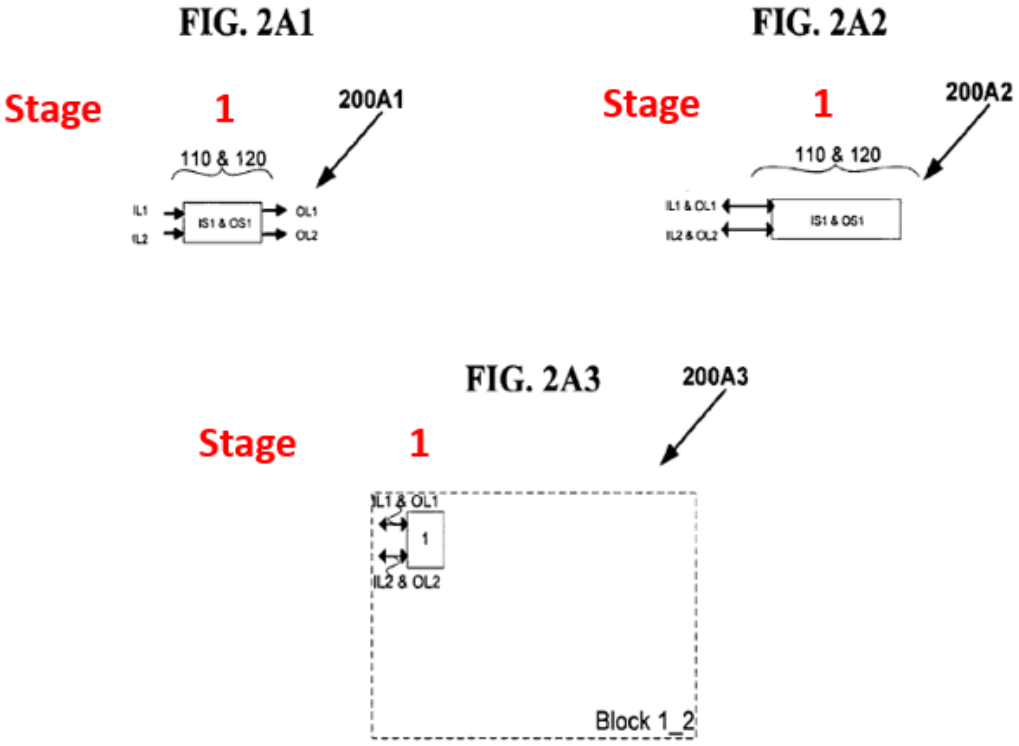
(Ex. 1004, 39.)

Specifically, claim 1 was broadened with respect to the number of stages. Instead of simply requiring a "plurality of stages y," the amendment changed the scope of claim 1 to encompass a routing network where each sub-integrated circuit block only has one stage. That is because the phrase "$y \geq 1$" covers the case where y equals 1 in addition to the case where y is greater than 1. (Ex. 1002, ¶48.) A POSITA reading the amended limitation would have understood claim 1 to cover a routing network that includes sub-integrated circuit blocks that all include only a *single stage*. (*Id.*) This is because if $y = 1$ (one of the possibilities that are covered by the limitation "$y \geq 1$"), then the lowest stage is 1 and the highest stage of y is also 1 (i.e., there must be only one stage for this to hold true). (*Id.*)

A POSITA would not have understood, based on the disclosures of the priority applications of the '523 patent, that the named inventor possessed an invention that includes an integrated circuit device that includes a "routing network comprising a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where $y \geq 1$," and where such a network also includes the remaining limitations of claim 1, including sub-integrated circuit blocks with the recited pluralities of forward connecting links, backward connecting links, straight links, and cross links. (Ex. 1002, ¶49.) As discussed below, neither of the priority applications discloses any routing network with only one stage in each

sub-integrated circuit block that has forward and backward connecting links of any sort, let alone pluralities of such links that further include pluralities of straight links and cross links. (*Id.*)

Each of the priority applications characterizes figures 2A1-2A3 below as a network with one stage. (Ex. 1007, 7:10-21; Ex. 1026, 4:4-15.)



(Ex. 1007, FIGs. 2A1-2A3 (annotated); *see also* Ex. 1026, FIGs. 2A1-2A3; Ex. 1002, ¶50.)

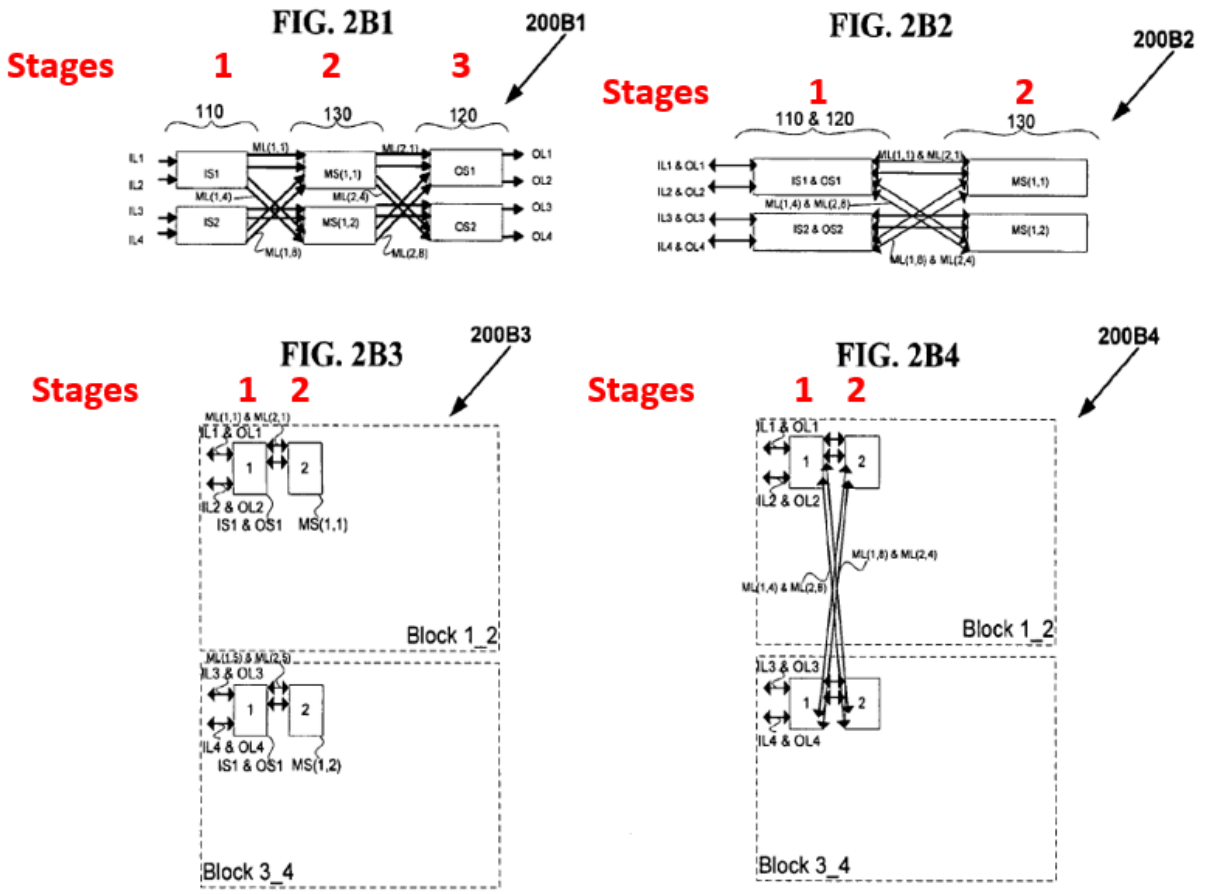
Both of the priority applications note that FIG. 2A3 shows the layout of the network "**illustrating all the connection links**." (Ex. 1007, 7:19-21 (emphasis

added); Ex. 1026, 4:13-15 (emphasis added).) The only links shown in figure 2A3 are the inlet links (IL1 and IL2) and the outlet links (OL1 and OL2), and a POSITA would have recognized that are **no forward connecting links** and **no backward connecting links** that connect switches in higher and lower stages to each other. The inlet and outlet links shown in figures 2A1-2A3 are different from "forward connecting links" and "backward connecting links" as recited in claim 1, which are required to connect from switches in one stage to switches in an immediately succeeding/preceding stage, respectively. This difference would have been clear to a POSITA based on claim 1 of the '523 patent, which recites "inlet links" and "outlet links" (Ex. 1001, 35:25-27) separately from "forward connecting links" and "backward connecting links" (*id.*, 35:43-49). (Ex. 1002, ¶51.)

A POSITA would have understood that there cannot be "a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage" if there is only one stage in the network. (*Id.*, ¶52.) If there is only one stage, there is no "immediate succeeding higher stage." Similarly, if there is only one stage, there cannot be "a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage" because there is no "immediate preceding lower stage." (*Id.*)

In contrast, figure 2B1 of the priority applications includes three stages. After folding, the network is reduced to two stages as is shown in figures 2B2-2B4, which, in the context of claim 1 means that y = 2.[2]

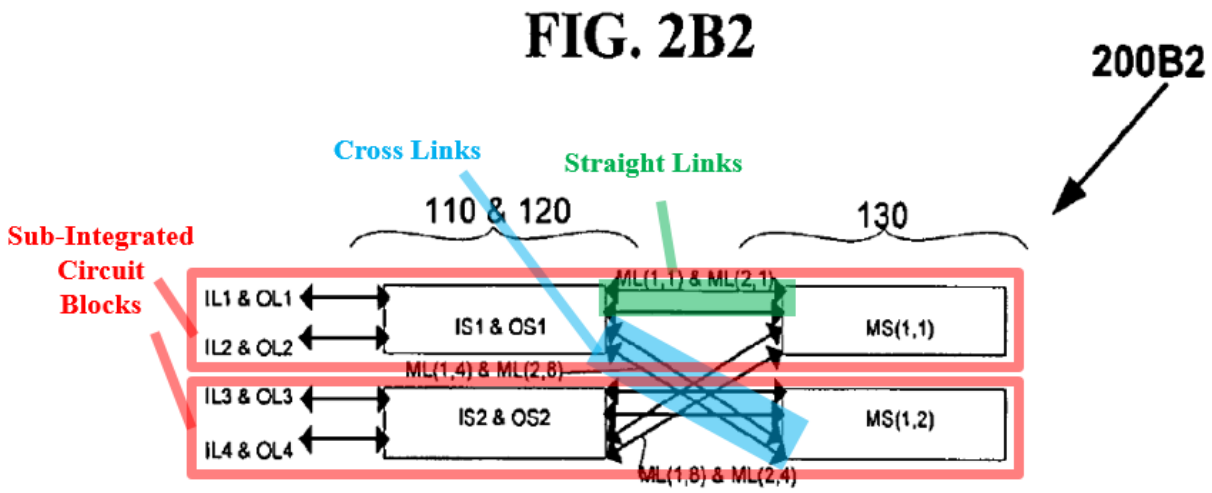
[2] The priority applications each incorrectly state that figures 2B1-2B2, 2C11-2C12, and 2D1-2D2 have a "connection topology of one stage." (Ex. 1005, 7:22-23, 7:26-8:1, 8:9-10, 8:13-15, 8:26-27, 9:3-5; Ex. 1026, 4:16-17, 4:20-23, 5:1-2, 5:5-7, 5:18-19, 5:23-25.) As is apparent from these figures, each of those networks includes more than one stage, where a stage corresponds to a column of switches in each of the sub-integrated circuit blocks. For example, figure 2C11 shows a network with five stages and figure 2C12 shows a network with three stages. (Ex. 1002, ¶53 fn.3.)



(Ex. 1007, FIGs. 2B1-2B4 (annotated); Ex. 1026, FIGs. 2B1-2B4 (annotated); Ex. 1002, ¶53.)

The two-stage network shown in figure 2B2 above includes a plurality of forward connecting links (links going from left to right between the switches in stage 1 and those in stage 2) and a plurality of backward connecting links (links going from right to left between switches in stage 2 and those in stage 1), where the forward and backward connecting links include straight links (links within the same sub-

integrated circuit block) and cross links (links between different sub-integrated circuit blocks). (Ex. 1026, 12:7-15.)



(Ex. 1007, FIG. 2B2 (annotated); Ex. 1026, FIG. 2B2 (annotated); Ex. 1002, ¶54.)

As shown above, each of the "sub-integrated circuit blocks" corresponds to a row of switches. (Ex. 1007, 20:26-28 ("Each block implements all the switches in one row of network 100B of FIG. 1B, one of the key aspects of the current invention."), 24:8-9, 43:10-12, 46:17-19, 48:1-5, 50:20-22, 51:3-7; Ex. 1026, 16:28-30, 38:13-15, 42:26-27, 45:24-25; Ex. 1002, ¶55.)

A POSITA would not have understood that the priority applications show that the named inventor had possession of an invention in which a network includes a "plurality of stages y, in each said sub-integrated circuit block, starting from the

lowest stage of 1 to the highest stage of y, where y ≥ 1" in conjunction with the limitations requiring forward and backward connecting links between switches in different stages because the priority applications do not disclose any sub-integrated circuit blocks that only have one stage and still have such forward and backward connecting links. (Ex. 1002, ¶56.)

Indeed, in PGR2019-00037, which concerns U.S. Patent 10,003,553 ("the '553 patent") (Ex. 1006) that is also assigned to PO, Petitioner raised a similar argument that the '553 patent does not have written description support for a single stage network (Ex. 1046 (Petition in PGR2019-00037), 60-66) and that such a single stage network would not support "straight links connected from a switch in a stage in a subnetwork to a switch in another stage of the same subnetwork" as claimed in the '553 patent (*id.*, 66 fn. 5.). The '553 patent incorporates by reference the '523 patent, the '605 PCT, and the '394 provisional by reference. (Ex. 1006, 2:20-32.) In response to the Institution Decision (Ex. 1047) in the '553 PGR proceeding, PO did not even attempt to show support for the single stage network with such straight links in any of the '523 patent, the '605 PCT, or the '394 provisional, and instead submitted a motion to amend that narrows the claims of the '553 patent to recite "a plurality of stages" instead of "y stages, where y ≥ 1." (Ex. 1048 (Motion to Amend in PGR2019-00037), 6 (4 of 55), 32 (30 of 55).) PO's motion to amend in the '553

PGR proceeding tacitly concedes the lack of support in the '523 patent (incorporated by reference in the '553 patent) and its alleged priority applications for a single stage network that includes the links recited in claim 1 of the '523 patent.

Petitioner anticipates that PO may contend that claim 1 only requires that each sub-integrated circuit block "comprises" y stages, and therefore if the specification discloses sub-integrated circuit blocks with more than one stage, then it discloses sub-integrated circuit blocks that "comprise" one stage and thereby discloses the lower end of the claimed range. Such a reading of the claim language would be illogical and improper. (Ex. 1002, ¶57.) If claim 1 were understood to mean that each sub-integrated circuit block simply *includes* at least one stage, then the recitation of "lowest stage of 1 to the highest stage of y, where $y \geq 1$" would be superfluous, as the claim element is being read as simply meaning "each sub-integrated circuit block includes y stages, where $y = 1$." Indeed, such a broad reading of this claim element would not provide any further restriction on the language "each sub-integrated circuit block comprising a stage." (*Id.*)

To the extent PO contends that claim 1 still requires "a plurality of stages" and therefore is limited to sub-integrated circuit blocks that include at least two stages, such an argument would directly conflict with the very amendment PO made during prosecution of the '275 application. (Ex. 1002, ¶58.) As originally filed,

claim 1 required "a plurality of stages y" where a POSITA would have understood that for there to be a "plurality of stages," y would necessarily be 2 or larger. However, PO amended claim 1 to specifically encompass "y=1" when he amended the claim to recite "$y \geq 1$." PO could have amended the claim to recite "$y > 1$," but specifically chose not to do so.

The understanding that PO intentionally broadened claim 1 to read on a network having only one stage is further supported by other amendments made during prosecution. (Ex. 1002, ¶59.) For example, pending claim 8 (which eventually issued as claim 7 of the '523 patent) was amended during prosecution to recite "$y \geq (\log_2 N)$, where $N>1$," (Ex. 1004, 42), which a POSITA would have understood simply requires $y \geq 1$. (Ex. 1002, ¶59.) A similar amendment was made to each of pending claims 12, 25, 29, 40, and 44 (Ex. 1004, 42-49), which eventually issued as claims 11, 24, 28, 39, and 43 of the '523 patent, respectively. Therefore, PO was consistent in amending the claims to encompass embodiments where y=1 and there is only a single stage in each sub-integrated circuit block in the network.

No claims were filed with the '394 provisional, and the claims filed with the '605 PCT recite the same limitations as those recited in the original claims of the '275 application. (Ex. 1002, ¶60.) As such, a POSITA would have understood that the claims of the '605 PCT require a plurality of stages in the routing network. (Ex.

1007, 57:10-11 ("Said routing network comprising a plurality of stages y, starting from the lowest stage to the highest stage;"); Ex. 1002, ¶60.) A POSITA would have understood that the broadening amendments made during prosecution of the '275 application are not supported by either of the priority applications, including the claims included in the '605 PCT. (Ex. 1002, ¶60.)

The foregoing lack of written description support in the priority applications applies to the remaining challenged claims as well because they ultimately depend from claim 1. (*Id.*, ¶61.)

b) Lack of enablement in priority applications

To meet the enablement requirement of 35 U.S.C. § 112, the specification must teach a POSITA how to make and use the full scope of the claimed invention without "undue experimentation." *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (internal citation omitted). Factors to be considered in determining whether undue experimentation is required include the amount of direction or guidance presented, the presence or absence of working examples, the state of the prior art, and the quantity of experimentation necessary. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). However, analysis of all the "*Wands*" factors is not required; "they are illustrative, not mandatory. What is relevant depends on the facts" of the particular case. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1213

(Fed. Cir. 1991); *Wyeth v. Abbott Labs.*, No. 08-1021 (JAP), 2012 WL 175023, at *12 (D.N.J. Jan. 19, 2012) (holding that there was undue experimentation when "a substantial amount of experimentation would be required" to practice the invention), *aff'd sub nom. Wyeth & Cordis Corp. v. Abbott Labs.*, 720 F.3d 1380, 1386 (Fed. Cir. 2013) ("Here, the specification similarly discloses only a starting point for further iterative research.").

Here, PO "has not enabled preparation of [the claimed invention] sufficient to support its all-encompassing claims." (Ex. 1002, ¶¶62-67.) *Amgen, Inc.*, 927 F.2d at 1213. The priority applications ('394 provisional and '605 PCT) do not teach a POSITA how to make and use at least a "routing network comprising a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y" where y=1 (i.e., a single stage), which is implicitly part of the claimed "$y \geq 1$," and where such a network also includes the remaining limitations of claim 1, including sub-integrated circuit blocks with the recited pluralities of forward connecting links, backward connecting links, straight links, and cross links as claimed in claim 1. (Ex. 1002, ¶63.)

As discussed above (*supra* Section V.B.1(a)), neither of the priority applications discloses any routing network with only one stage that has forward and backward connecting links of any sort, let alone pluralities of such links that further

include pluralities of straight links and cross links. (Ex. 1002, ¶64.) To the extent there is any guidance provided in the disclosure of the priority applications to make and/or use the claimed invention, it is all directed to *multi-stage* networks. (*Id.*) The priority applications are devoid of any guidance or working examples of a single stage network that includes the above-discussed forward/backward/straight/cross links, as covered by claim 1. (*Id.*)

Moreover, a network with all sub-integrated circuit blocks having a single stage, as included in the claimed range of "$y \geq 1$," would have been incompatible with other parts of the claim such as "lower stage," "immediate succeeding higher stage," "higher stage," and "immediate preceding lower stage." (Ex. 1001, 35:43-49; Ex. 1002, ¶65.) As such, these are plainly and unambiguously incompatible features (i.e., incompatible with a single stage) and no amount of experimentation would have led a POSITA to make and/or use the claimed single-stage routing network with the remaining limitations regarding forward/backward/straight/cross links as claimed in claim 1. (Ex. 1002, ¶65.) *Auto. Techs. Int'l, Inc. v. BMW of N. Am., Inc.*, 501 F.3d 1274, 1281, 1284 (Fed. Cir. 2007).

Furthermore, the materials incorporated by reference in the disclosures of the priority applications do not cure this deficiency. (Ex. 1002, ¶66.) None of those materials provide any explanation of the claimed single-stage routing network with

the remaining limitations regarding forward/backward/straight/cross links as claimed in claim 1. (*Id.*) Additionally, the priority applications would not have provided any direction or guidance to a POSITA regarding the relevance of the incorporated material in relation to how to make and/or use the claimed invention. (*Id.*)

The foregoing lack of enablement in the priority applications applies to the remaining challenged claims as well because they ultimately depend from claim 1. (*Id.*, ¶67.)

2. *Konda '756 PCT*

Konda '756 PCT (Ex. 1009) was published September 12, 2008 and therefore qualifies as prior art under pre-AIA § 102(b) against the '523 patent, which, as discussed above, has an earliest effective filing date of November 22, 2009. (*Supra* Section V.B.1; *see also* Ex. 1002, ¶¶68-71 (overview of *Konda '756 PCT*).) *Konda '756 PCT* incorporates by reference, among other applications, the '394 provisional, which is the **same provisional application to which the '523 patent claims**

priority. (Ex. 1009, 2:14-17.)[3] The '394 provisional became publically available as of the date of *Konda '756 PCT* publication, i.e., September 12, 2008. *See* 37 C.F.R. § 1.14(a)(1)(vi); *Flex Logix Technologies Inc. v. Konda Technologies Inc.*, PGR2019-00042, Paper 14 at 26-27 (PTAB Sept. 19, 2019); *Ex Parte Xiaoming Bao & Stephen M. Allen*, Appeal No. 2016-006293, 2017 WL 1397726, at *4 (PTAB Mar. 28, 2017). Moreover, because the '394 provisional is incorporated by reference in *Konda '756 PCT*, the contents of the '394 provisional were effectively contained in *Konda '756 PCT* itself when it was published. *See MPEP* at § 2163.07(b)[4]

Konda '756 PCT was not considered by the Patent Office during prosecution.

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[3] Exhibits 1010-1023, 1026, 1029-1030, and 1039 are, *inter alia*, various documents purportedly incorporated by reference into the '523 patent, *Konda '756 PCT*, and/or the '394 provisional.

[4] For convenience, this Petition includes citations directly to the '394 provisional (Ex. 1026), in addition to citations to *Konda '756 PCT* (Ex. 1009), but as discussed above, such citations to the '394 provisional are effectively also to *Konda '756 PCT* itself.

(Ex. 1004, Cover ("References Cited" section); *see generally* Ex. 1004.)

3. *Wong*

Wong issued on September 6, 2005 and therefore qualifies as prior art under § 102(b). (*See* Ex. 1002, ¶¶72-76 (overview of *Wong*).) *Wong* was considered by the Patent Office during prosecution. (*See, e.g.*, Ex. 1004, 92-117 (claim rejections based in part on *Wong*).) However, Petitioner presents *Wong* in a new light never considered by the Office—as a secondary reference in an obviousness combination with *Konda '756 PCT*. (*Infra* Section IX.C.) Here, Petitioner presents testimony from R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '523 patent (Ex. 1002, ¶¶1-19; Ex. 1003), who confirms that the relevant teachings of *Konda '756 PCT* and *Wong* disclose or suggest what is claimed by challenged claims 18 and 47 of the '523 patent. (*See* Ex. 1002, ¶¶163-178; *see also infra* Section IX.C.)

Wong is only relied upon in this Petition as a secondary reference for certain dependent claims (*infra* Section IX.C), whereas the Examiner allowed the '275 patent to issue as the '523 patent based on considerations relating to claim 1. (Ex. 1004, 28 (Examiner's statement of reasons for allowance, discussing amended claim 1), 39 (amendment of claim 1 following Examiner interview), 57 (interview summary indicating that "[a]greement was reached for the proposed amendment of claim 1…").) As such, any consideration of *Wong* by the Patent Office during

prosecution of the '523 patent should not preclude the Board from considering and instituting the grounds in this Petition.

VI. LEVEL OF ORDINARY SKILL IN THE ART

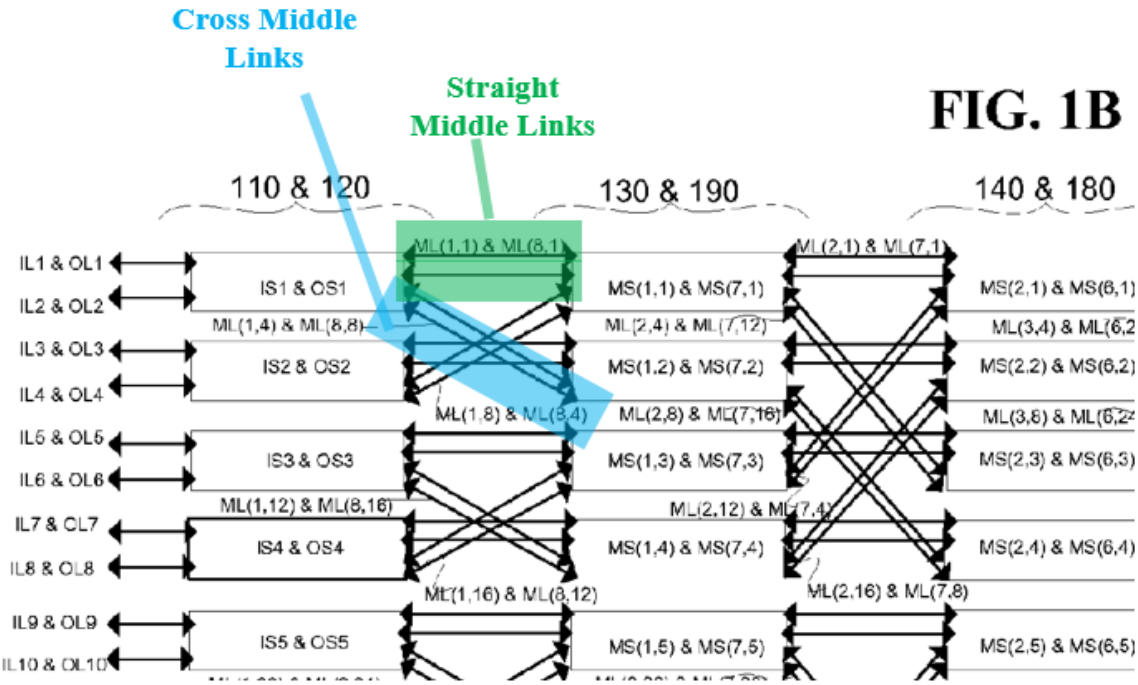
A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '523 patent would have had a master's degree in electrical engineering or a similar field, and at least two to three years of experience with integrated circuits and networks. (Ex. 1002, ¶¶18-19.) More education can supplement practical experience and vice versa. (*Id*.)

VII. OVERVIEW OF THE '523 PATENT

The '523 patent is entitled "VLSI Layouts of Fully Connected Generalized Networks." (Ex. 1001, Title.) The '523 patent acknowledges that multi-stage hierarchical networks were known and used in many applications, including field-programmable gate arrays (FPGAs). (*Id.*, 2:25-27, 2:62-67; Ex. 1002, ¶¶31-38.) The '523 patent contends that prior art network layouts were "inefficient and complicated" (Ex. 1001, 2:28-30, 3:1-6) and alleges to disclose layouts of networks that use horizontal and vertical cross links between switches in succeeding stages. (*Id.*, 3:21-29.)

In addition to inlet and outlet links on the periphery of the network, the '523 patent discloses middle links that provide connections between the switches in the

different stages of the network. "The middle links which connect switches in the same row in two successive middle stages are called hereinafter **straight middle links**; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter **cross middle links**." (Ex. 1001, 9:45-49 (emphasis added).) Examples of straight and cross middle links are highlighted in figure 1B below.



(*Id.*, FIG. 1B (excerpt, annotated); Ex. 1002, ¶38.)

As explained below (*infra* Section IX), the above features were all known in the prior art. (*See* Ex. 1002, ¶¶78-179; *see also id.*, ¶¶20-30 (describing the state of the art).)

VIII. CLAIM CONSTRUCTION

In an IPR, claims are construed in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.200(b). In particular, claim terms are generally given their "ordinary and customary meaning," that is, "the meaning that the term would have to a POSITA in question at the time of the invention, i.e., as the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems*, Inc., IPR2015-00633, Paper 11 at 16 (August 14, 2015). Petitioner submits that for purposes of this proceeding, no term requires construction.[5] (Ex. 1002, ¶39.)

[5] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '523 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: *Konda '756 PCT* Anticipates Claims 1, 16, 20-22, and 32

1. Claim 1

a) "An integrated circuit device comprising"

To the extent the preamble is limiting, *Konda '756 PCT*, by way of its incorporation of the '394 provisional, discloses an integrated circuit device. (Ex. 1002, ¶¶79-80.) For instance, *Konda '756 PCT* discloses a "semiconductor chip" such as an FPGA (Ex. 1026, 8:21-9:2; 9:8-10), and a POSITA would have understood that disclosure of a "semiconductor chip" discloses an "integrated circuit device." (Ex. 1002, ¶80; *see also infra* Sections IX.A.1(b)-(k) regarding the remaining elements of this claim.)

b) "**a plurality of sub-integrated circuit blocks and a routing network**"

Konda '756 PCT discloses this limitation, as explained below. (Ex. 1002, ¶¶81-88.)

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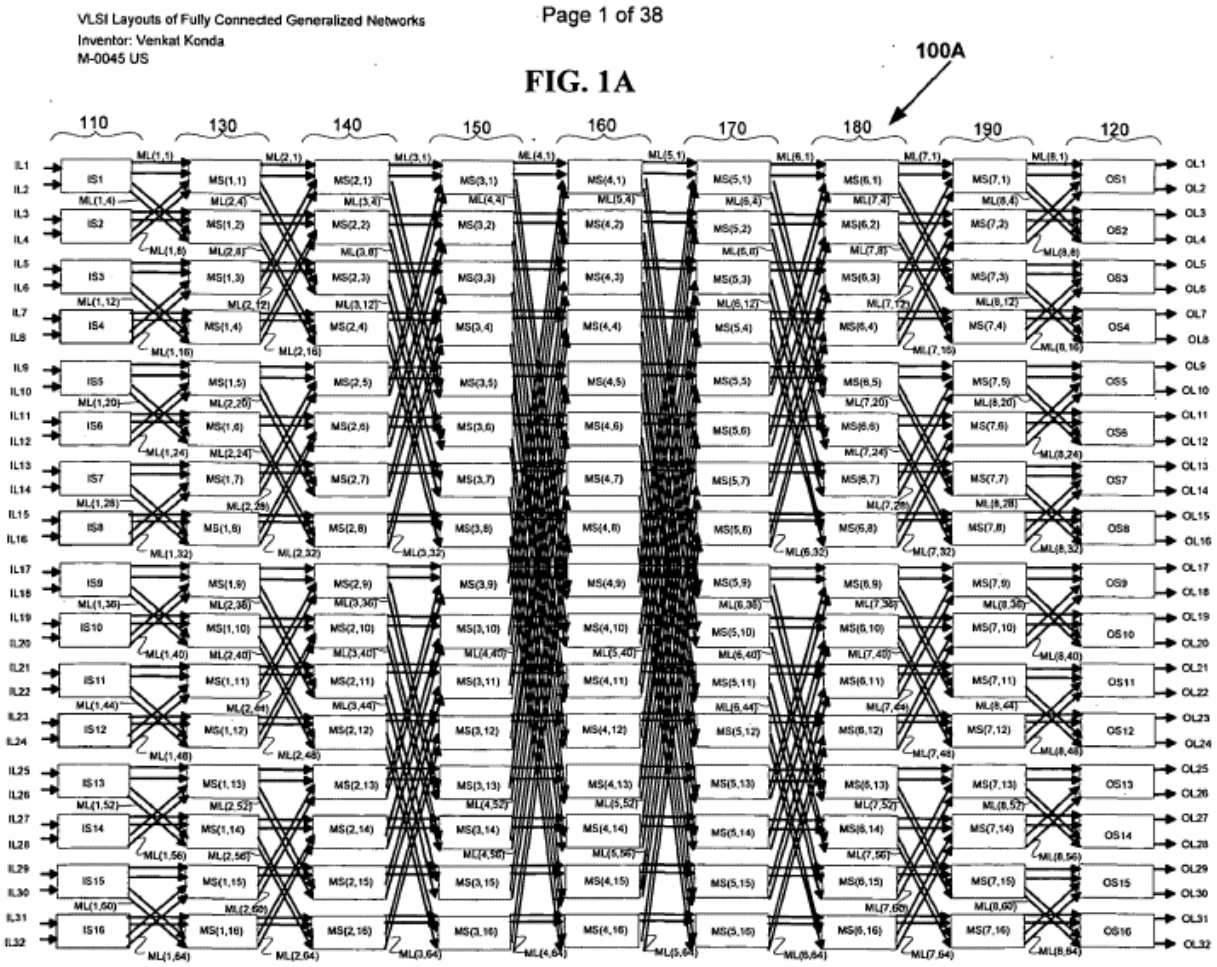
that are not presented here given the similarities between the references and the patent.

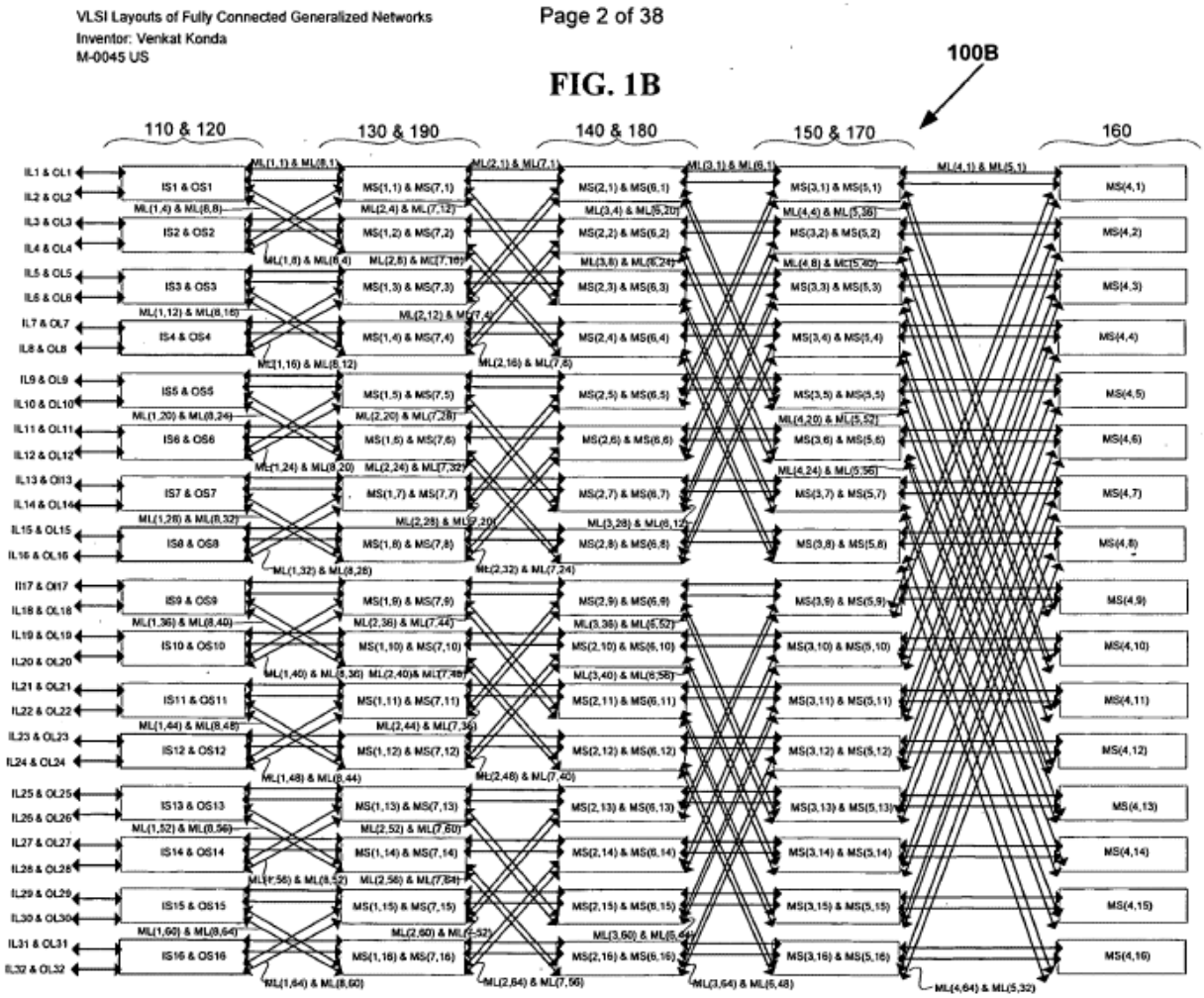
(1) a routing network

Konda '756 PCT discloses a routing network. (Ex. 1002, ¶¶82-85.) For instance, the '394 provisional, as incorporated by reference in *Konda '756 PCT*, discloses "[t]he present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast, and multicast connections." (Ex. 1026, 8:12-13.) Figure 1A of the '394 provisional illustrates an "exemplary generalized multi-link multi-stage network … with nine stages of one hundred forty four switches for satisfying communication requests, such as setting up . . . a connection between configuration logic blocks." (*Id.*, 10:25-11:2.)


VLSI Layouts of Fully Connected Generalized Networks
Inventor: Venkat Konda
M-0045 US
Page 1 of 38
100A
FIG. 1A
110
130
140
150
160
170
180
190
120

(*Id.*, FIG. 1A.)

The '394 provisional discloses that connections are set up "between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190." (*Id.*, 11:1-3.) The '394 provisional further discloses that figure 1B, replicated below, is a folded version of the network shown in figure 1A. (*Id.*, 2:12-13, 15:3-4; Ex. 1002, ¶84.)

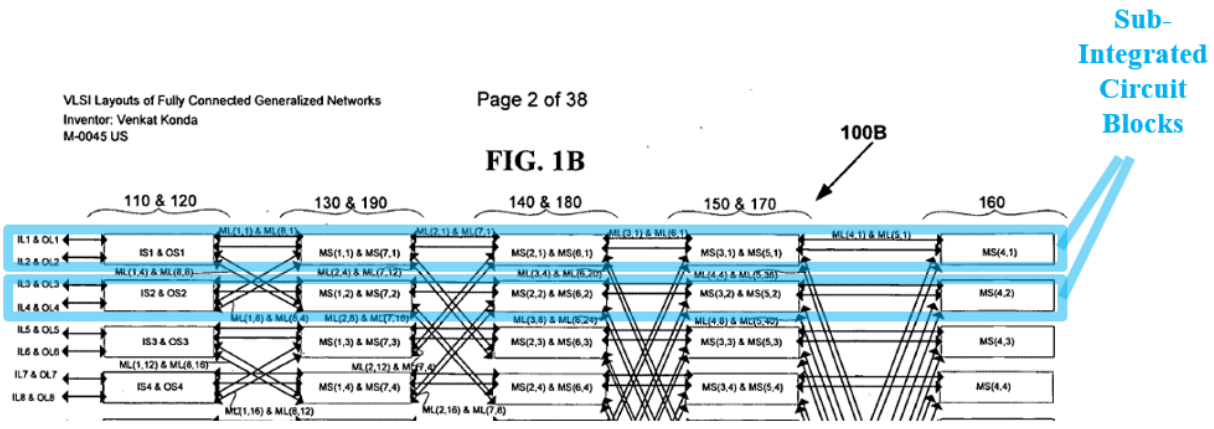


(Ex. 1026, FIG. 1B.)

Therefore, much of the description regarding the network of figure 1A in the '394 provisional is also applicable to figure 1B of the '394 provisional. (*Id.*, 15:4-5; Ex. 1002, ¶85.) The network shown in figure 1B of the '394 provisional, which can be included on a FPGA integrated circuit, is "a routing network" as it allows connections to be "routed" between inputs and outputs. (Ex. 1026, 11:1-3; Ex. 1002, ¶85.)

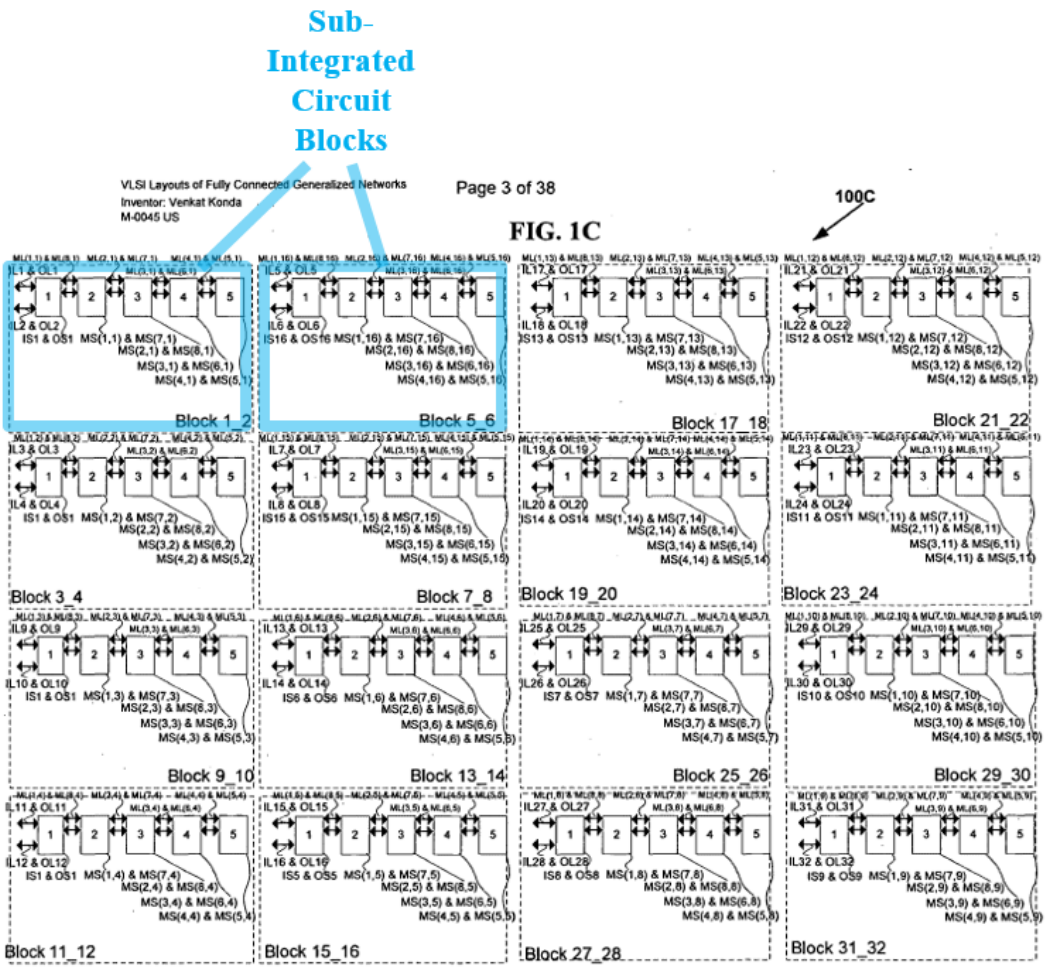
(2) a plurality of sub-integrated circuit blocks

Konda '756 PCT discloses a plurality of sub-integrated circuit blocks. (Ex. 1002, ¶¶86-88.) The '394 provisional, as incorporated by reference in *Konda '756 PCT*, discloses that the network shown in figure 1B includes a plurality of sub-integrated circuit blocks. (*Id.*, ¶86.) Annotated figure 1B below shows that each row of switches in the network is included in a different sub-integrated circuit block.



(Ex. 1026, FIG. 1B (excerpt, annotated); Ex. 1002, ¶86.)

According to the '394 provisional, the layout shown in figure 1C below includes 16 blocks, where "[e]ach block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention." (Ex. 1026, 16:25-30.)



(*Id.*, FIG. 1C (annotated); Ex. 1002, ¶87.)

Therefore, each of the "blocks" shown in figure 1C of the '394 provisional above corresponds to a row of switches in the network illustrated in figure 1B. (Ex.

1026, 16:25-30.) Each row of switches corresponds to a portion of the overall block of switches within the integrated circuit in which the network is included, and therefore a POSITA would have understood that each row of switches corresponds to a different "sub-integrated circuit block." (Ex. 1002, ¶88.) Because figure 1B includes 16 rows of switches, it includes 16 sub-integrated circuit blocks, each of which is illustrated as a "block" in figure 1C. (*Id.*; Ex. 1026, FIGs. 1B, 1C.)

c) "Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶89-91.) For example, the '394 provisional, as incorporated by reference in *Konda '756 PCT*, discloses that "[e]ven through it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit depending on the application in different embodiments." (Ex. 1026, 17:15-17.)[6] A POSITA would have understood that such CLBs or other

[6] Confusingly, the '523 patent refers to "Configurable Logic Blocks (CLB) or any arbitrary digital circuit" as "sub-integrated circuit blocks" in their own right. (Ex. 1001 at 13:38-42.) Viewing the configurable logic blocks or arbitrary digital circuit

arbitrary digital circuits have inputs ("plurality of inlet links") that receive outputs from the switches in the network and outputs ("plurality of outlet links") that provide inputs to the switches in the network. (Ex. 1002, ¶89.) Such an understanding is supported by the disclosure that the network of figure 1A (and hence the networks of figures 1B and 1C) includes switches for "setting up a … connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages … ." (Ex. 1026, 10:25-11:3; Ex. 1002, ¶89.)

Figure 1K1 of the '394 provisional shows "detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connecting links going in and coming out … ." (Ex. 1026, 3:19-20.) Figure 1K1 is annotated below to show the inclusion of a configurable logic block (CLB) in block 1_2, which is one of the blocks included in the network of figures 1B and 1C. (*Id.*) The outputs of the CLB (shown as IL1 and IL2) constitute a "plurality of outlet links," and the inputs

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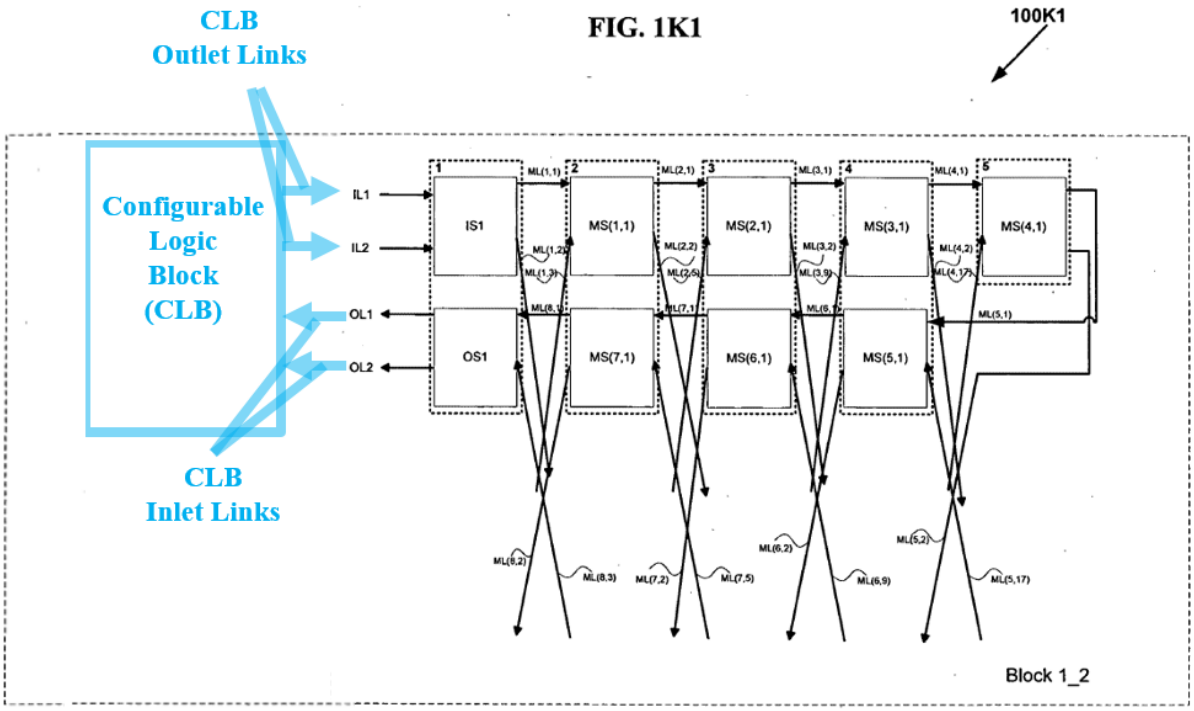
alone as a sub-integrated circuit block does not make sense in the context of claim 1, which requires the sub-integrated circuit blocks to include numerous links that are only disclosed in the '523 patent as being part of the network of switches. (Ex. 1002, ¶89 fn.4.)

of the CLB (shown at OL1 and OL2) constitute a "plurality of inlet links" as those terms are used in the context of claim 1 of the '523 patent. (Ex. 1002, ¶90.)

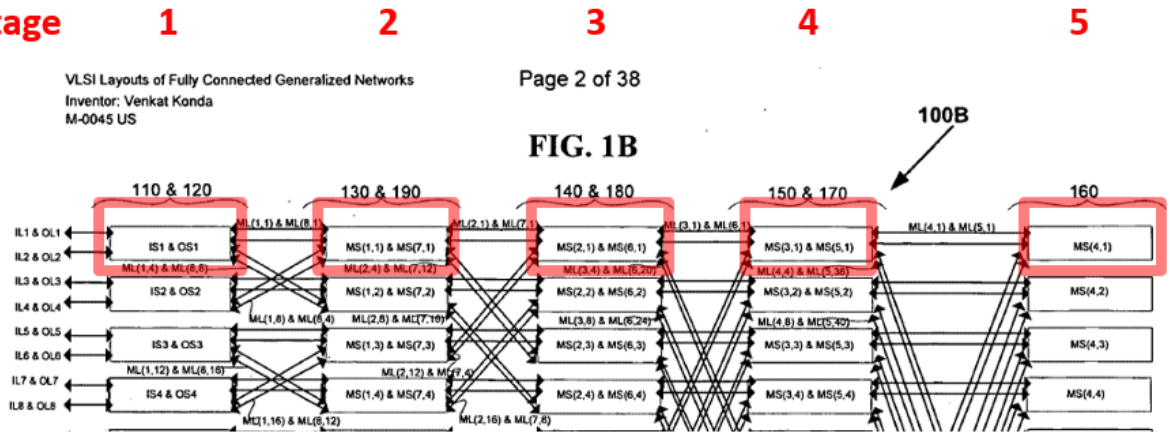


(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶90.)

As discussed below with respect to claim element 1(f), *Konda '756 PCT* further discloses that the plurality of inlet links and the plurality of outlet links, discussed here and shown in annotated figure 1K1 above, are directly connected to the inlet links and outlet links of the switches in the lowest stage (stage 1) of the routing network. (*Infra* Section IX.A.1(f); Ex. 1002, ¶91.)

d) "Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y ≥ 1; and"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶92.) For example, as shown in an annotated excerpt of figure 1B of the '394 provisional below, the routing network includes five stages that are highlighted in the top-most sub-integrated circuit block. (*Id.*; Ex. 1026, 2:12-14.) Therefore, *Konda '756 PCT*, which incorporates the '394 provisional by reference, discloses the "routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y ≥ 1," as it discloses a network with a number of stages (y) equal to five, and 5 ≥ 1. (Ex. 1002, ¶92.)



(Ex. 1026, FIG. 1B (excerpt, annotated); Ex. 1002, ¶92.)

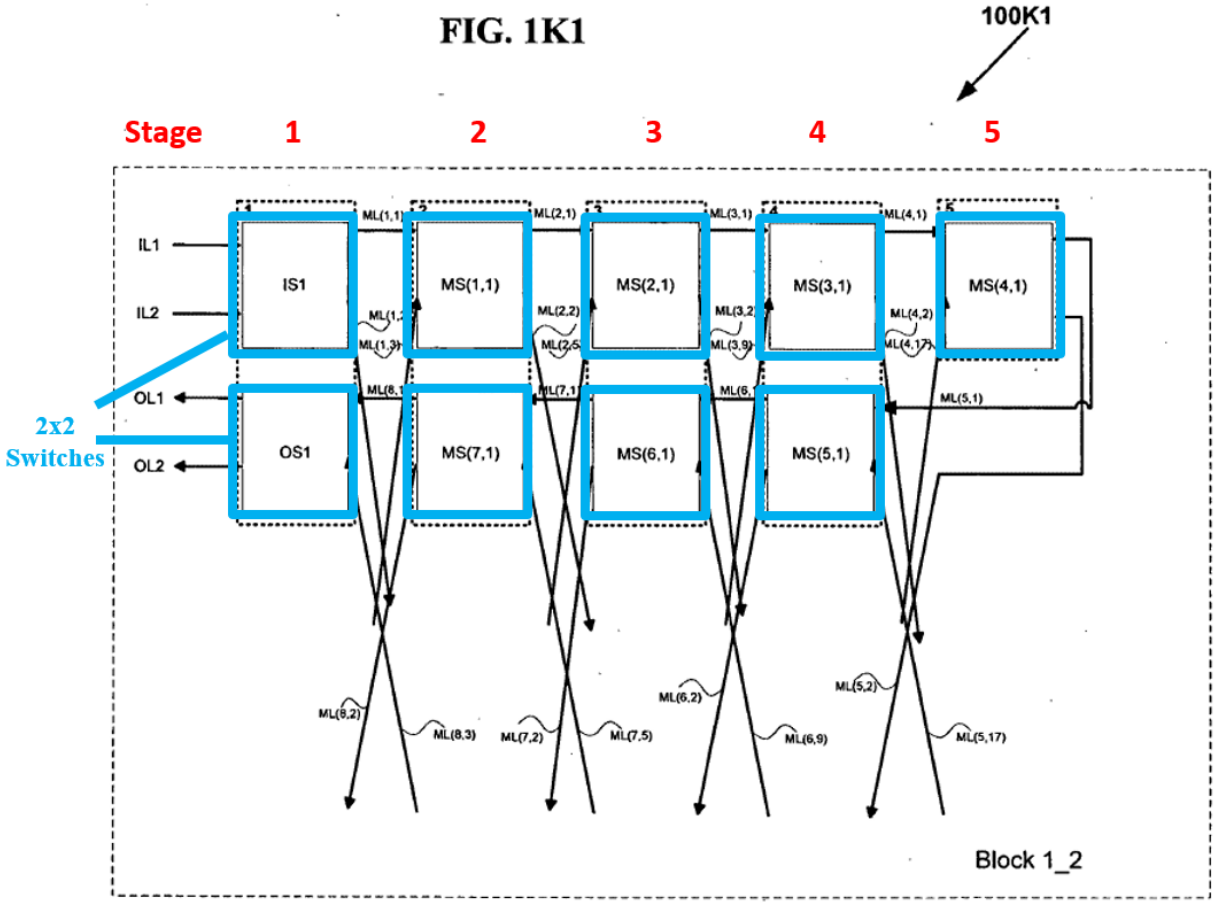
e) "**Said routing network comprising a plurality of switches of size dxd, where d≥2, in each said stage and each said switch of size dxd having d inlet links and d outlet links; and**"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶93-98.) According to limitation 1(e), each stage of the network includes a plurality of switches, each of which has at least two inlet links (d inputs) and the same number of outlet links (d outputs). Notably, a "switch of size dxd" in the context of "each said switch of size dxd having d inlet links and d outlet links" would have informed a POSITA about the input/output configuration of the switch, and not the actual area (i.e., physical size) of the switch. (*Id.*, ¶93.)

A POSITA would have understood that a dxd switch is a symmetrical switch, in that it has the same number of inputs and outputs. (*Id.*, ¶94 (citing Ex. 1006).) The '394 provisional discloses an embodiment in which the network of figure 1B is constructed using a plurality of 2x2 switches in each of the stages. (Ex. 1002, ¶¶94-96; Ex. 1026, 29:2-5, 29:8-22 (stating that the switches corresponding to the input stage, the output stage, and the middle stages that are combined together are 2x2 switches).)

As shown in annotated figure 1K1 below, each stage in each sub-integrated circuit block includes at least one 2x2 switch. (Ex. 1002, ¶97.) Because the network

includes a plurality of sub-integrated circuit blocks (e.g., one corresponding to each row shown in figure 1B, as discussed above in Section IX.A.1(b)(2)), each stage of the network includes a plurality of 2x2 switches. (Ex. 1002, ¶97.) For example, because there are 16 sub-integrated circuit blocks in the network of figure 1B, each of stages 1-4 in the routing network has 32 2x2 switches (two switches per sub-integrated circuit block in each of stages 1-4) and stage 5 has 16 2x2 switches (one switch per sub-integrated circuit block in stage 5, as shown in annotated figure 1K1 below). (Ex. 1026, FIG. 1K1; Ex. 1002, ¶97.) Therefore, *Konda '756 PCT* discloses limitation 1(e). (Ex. 1002, ¶97.)



(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶97.)

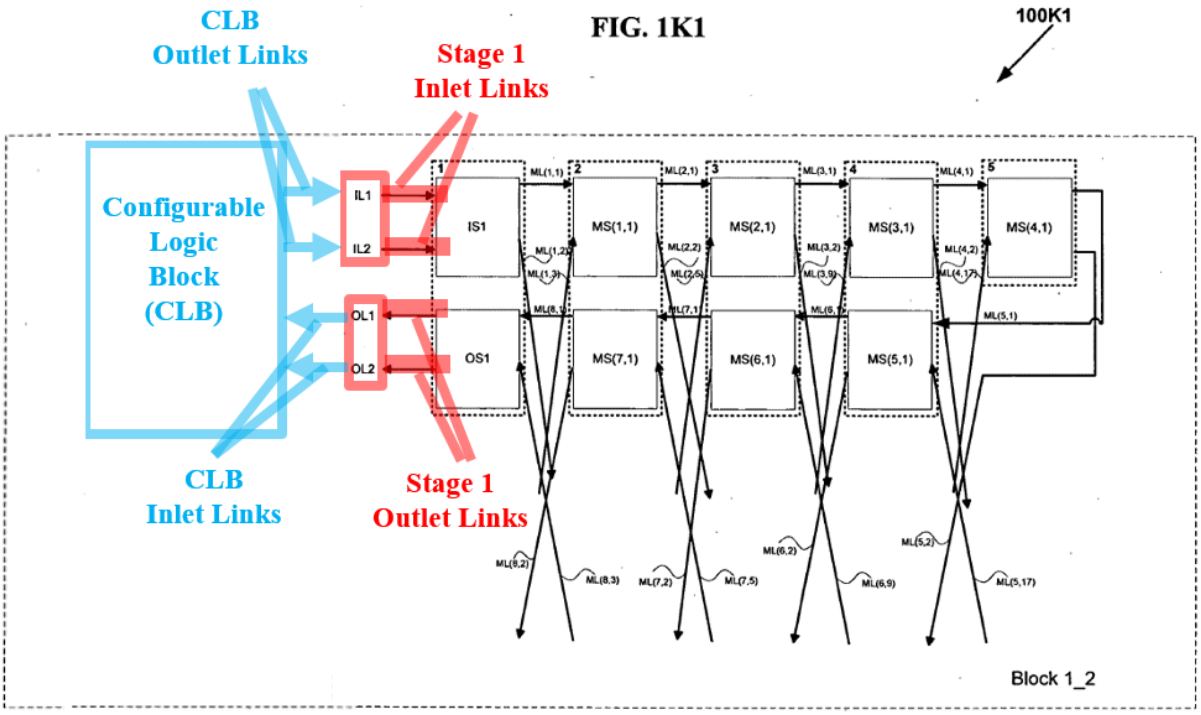
Notably, a POSITA would have understood that limitation 1(e) does not require a plurality of dxd switches **in each stage in each sub-integrated circuit block**, but instead simply requires a plurality of dxd switches **in each stage of the routing network**. (Ex. 1002, ¶98.) Original claim 1 of the '275 application included, in addition to the feature that issued as limitation 1(e), an additional limitation that required "[s]aid each sub-integrated circuit block comprising a plurality of said switches corresponding to each stage." (Ex. 1004, 217, 325.) But

that additional feature, which required a plurality of dxd switches in each stage in **each sub-integrated circuit block**, was deleted by PO during prosecution. (*Id.*, 67.)

> **f)** "**Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and**"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶99-103.) For instance, as discussed above with respect to claim limitation 1(c), the '394 provisional, as incorporated by reference in *Konda '756 PCT*, discloses that each sub-integrated circuit block includes a plurality of inlet links and a plurality of outlet links that correspond to the inputs and outputs of the Configurable Logic Blocks, respectively. (*See supra* Section IX.A.1(c); Ex. 1026, 17:15-17; Ex. 1002, ¶99.)

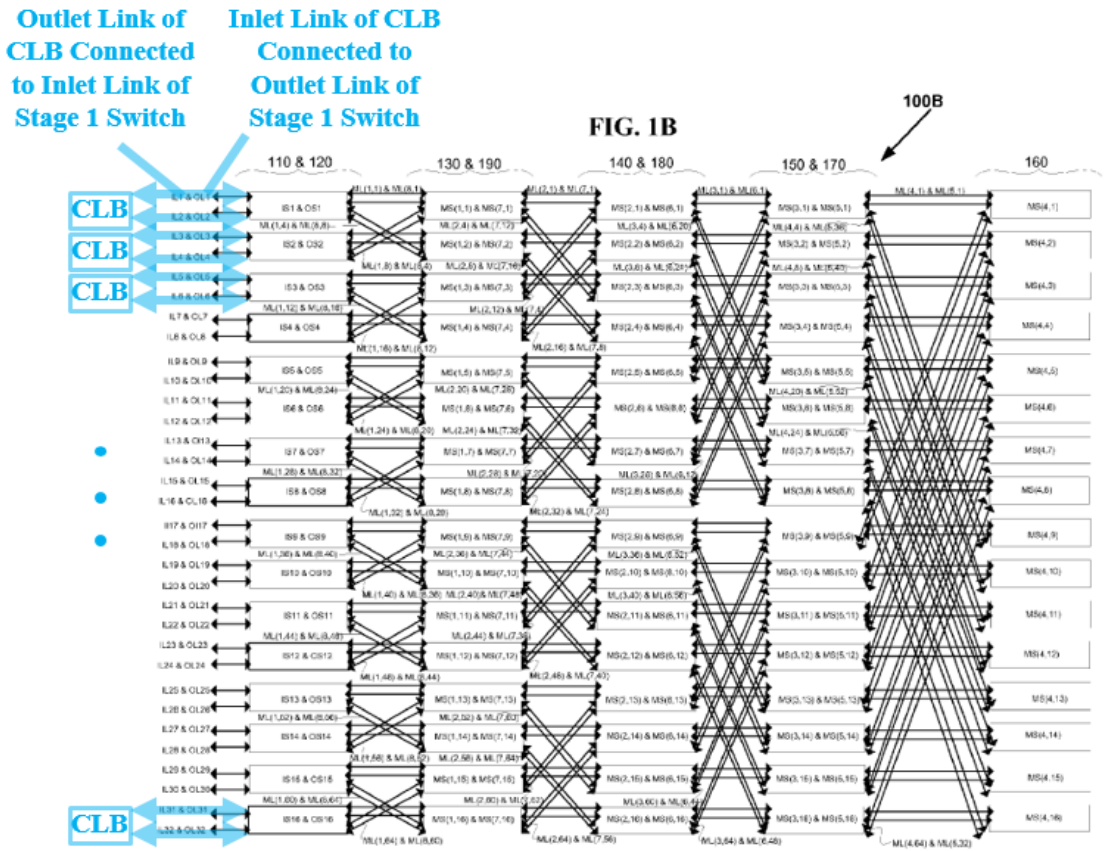
As shown in annotated figure 1K1 of the '394 provisional below, the outputs of the CLB ("plurality of outlet links of said each sub-integrated circuit block") are directly connected to the inputs of the first stage ("said inlet links of said switches of its corresponding said lowest stage of 1"). (Ex. 1002, ¶100.) Similarly, the inputs of the CLB ("plurality of inlet links of said each sub-integrated circuit block") are directly connected to the outputs of the first stage ("said outlet links of said switches of its corresponding said lowest stage of 1"). (*Id.*)



(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶100.)

Figure 1B of the '394 provisional is annotated below to show the Configurable Logic Blocks included in the integrated circuit device that have inlet links and outlet links that are directly connected to the outlet links and inlet links, respectively, of the switches in stage 1 (input switches IS1-IS16 and output switches OS1-OS16). (Ex. 1002, ¶101.) A POSITA would have recognized that each double-ended arrow in figure 1B below represents two links—one going in one direction, and the other going in the other direction. (*Id.*, ¶¶102-103.) For example, the inlet links IL1 and IL2 of switch IS1 are connected to the outlet links of the top-most CLB. (*Id.*, ¶101.) Similarly, the outlet links OL1 and Ol2 of switch OS1 are directly connected to the

inlet links of the top-most CLB. (Ex. 1026, 15:3-11, 29:1-14, FIG. 1B; Ex. 1002, ¶101.)

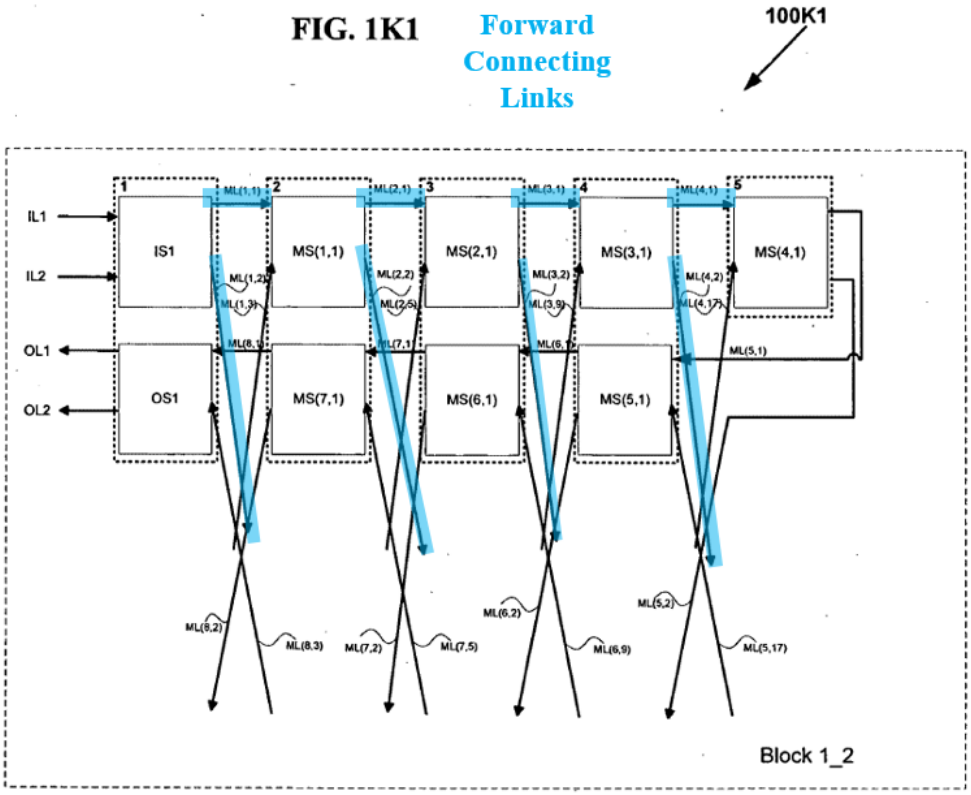


(Ex. 1026, FIG. 1B (annotated); Ex. 1002, ¶101.)

g) "Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage; and"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶104-109.) With respect to the forward connecting links, figure 1K1 of the '394 provisional, which

depicts one of the sub-integrated circuit blocks (block 1_2) included in the network of figures 1B and 1C (Ex. 1026, 29:1-8, 30:1-5), illustrates a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage. (Ex. 1002, ¶104.)



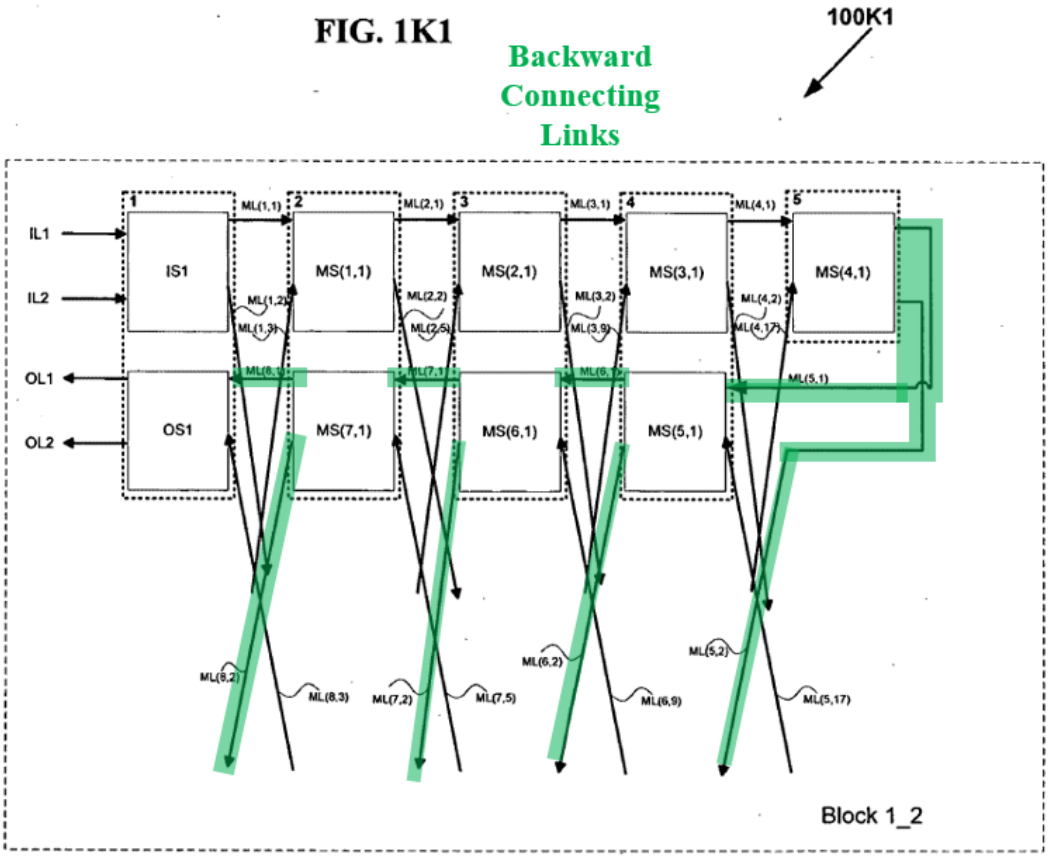
(Ex. 1026, FIG. 1K1 (annotated to show forward connecting links (blue) of the sub-integrated circuit block corresponding to the top row of FIG. 1B); Ex. 1002, ¶104.)

As shown in annotated figure 1K1 above, each of the forward connecting links connects from a switch in a lower stage to a switch in a higher stage. (Ex. 1002,

¶105.) For example, forward connecting link ML(1,1) connects switch IS1 in stage 1 to switch MS(1,1) in stage 2. Similarly, forward connecting link ML(1,2) connects the switch IS1 in stage 1 to the switch MS(1,2) in stage 2 of the sub-integrated circuit block corresponding to the second row of the network shown in figure 1B. (Ex. 1026, FIG. 1B.) Indeed, the description of what the '523 patent considers "forward connecting links" matches the description of the right-going middle links depicted in figures 1B and 1K1. (Ex. 1026, 15:3-9; Ex. 1001, 12:6-16; Ex. 1002, ¶105.)

While the annotated version of figure 1K1 above only highlights the forward connecting links for the switches in the top-most row in figure 1B, figure 1B shows that each of the rows included in the routing network includes a plurality of forward connecting links. (Ex. 1026, FIGs. 1B, 1K1; Ex. 1002, ¶106.)

Konda '756 PCT also discloses the backward connecting links recited in limitation 1(g). (Ex. 1002, ¶107.) For example, figure 1K1 of the '394 provisional illustrates a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage. (*Id.*)



(Ex. 1026, FIG. 1K1 (annotated to show backward connecting links (green) of the sub-integrated circuit block corresponding to the top row of FIG. 1B); Ex. 1002, ¶107.)

As shown in annotated figure 1K1 above, each of the backward connecting links connects from a switch in a higher stage to a switch in an immediately preceding lower stage. (Ex. 1002, ¶108.) For example, backward connecting link ML(8,1) connects switch MS(7,1) in stage 2 to switch OS1 in stage 1. Similarly, backward connecting link ML(8,2) connects the switch MS(7,1) in stage 2 to the

switch OS2 in stage 1 of the sub-integrated circuit block corresponding to the second row of the network shown in figure 1B. (Ex. 1026, FIG. 1B.) Indeed, the description of what the '523 patent considers "backward connecting links" matches the description of the left-going middle links depicted in figures 1B and 1K1. (*Id.*, 15:3-11; Ex. 1001, 12:6-16; Ex. 1002, ¶108.)

While the annotated version of figure 1K1 above only highlights the backward connecting links for the switches in the top-most row in figure 1B, figure 1B shows that each of the rows illustrated includes a plurality of backward connecting links. (Ex. 1026, FIGs. 1B, 1K1; Ex. 1002, ¶109.)

h) "**Said each sub-integrated circuit block comprising a plurality [of] straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage,**"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶110-122.) As discussed above with respect to limitation 1(g), *Konda '756 PCT* discloses that each

sub-integrated circuit block includes a plurality of forward connecting links and a plurality of backward connecting links. (*Supra* Section IX.A.1(g).) As demonstrated below, the *Konda '756 PCT* further discloses that each sub-integrated circuit block includes a plurality of straight links in each of the forward and backward connecting links as well as a plurality of cross links in each of the forward and backward connecting links. (Ex. 1002, ¶110.)

The '523 patent does not use the terms "straight link" and "cross link" outside of the claims, but the specification of the '523 patent states:

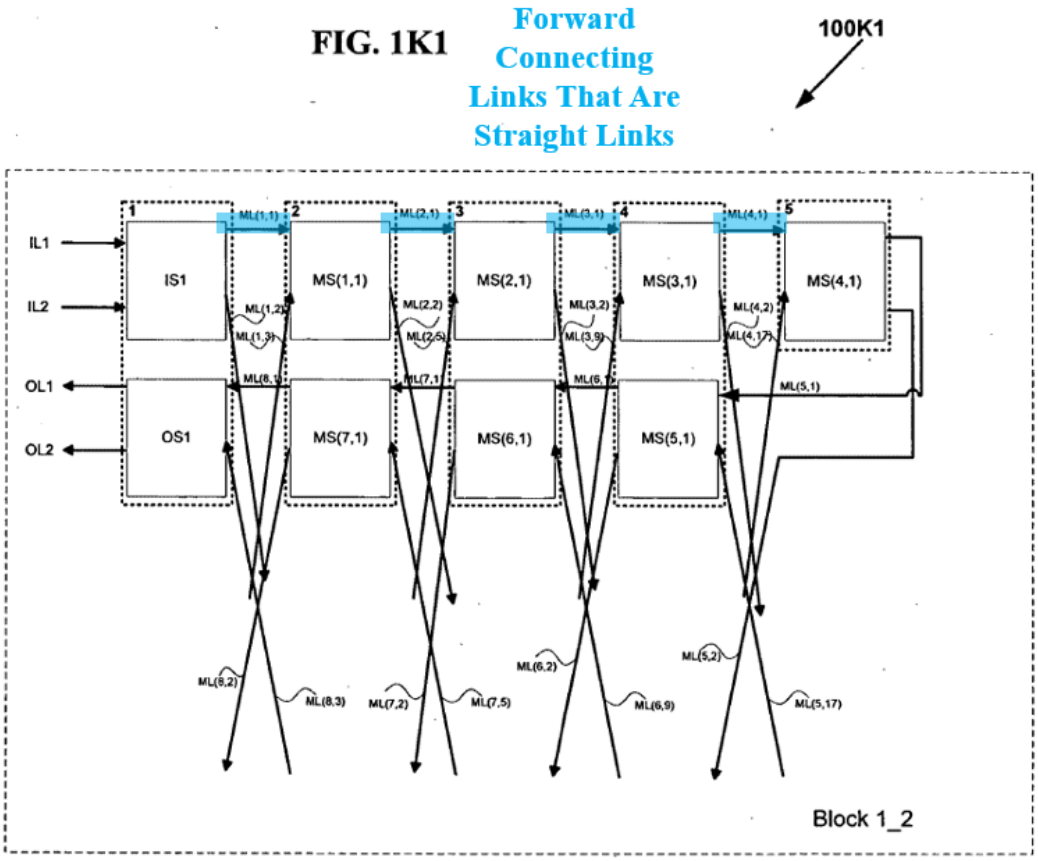
> The middle links which connect switches in the same row in two successive middle stages are called hereinafter **straight middle links**; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter **cross middle links**. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are **straight middle links**; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch (MS1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are **cross middle links**.

(Ex. 1001, 9:45-57 (emphasis added); Ex. 1002, ¶111.)

The '394 provisional contains the very same language. (Ex. 1026, 12:7-15; Ex. 1002, ¶112.) The understanding that "straight links" are links between switches in the same sub-integrated circuit block (e.g., same row in figure 1B) and that "cross links" are links between switches in different sub-integrated circuit blocks (e.g., different rows in figure 1B) is also consistent with limitation 1(j) discussed below. (*Infra* Section IX.A.1(j); Ex. 1002, ¶112.)

(1) "a plurality [of] straight links in said forward connecting links"

As discussed above with respect to claim limitation 1(g), *Konda '756 PCT* discloses that each sub-integrated circuit block includes a plurality of forward connecting links. (*Supra* Section IX.A.1(g); Ex. 1002, ¶113.) The subset of forward connecting links that are also "straight links" is highlighted in annotated figure 1K1 below. (Ex. 1026, FIG. 1K1, 12:10-12; Ex. 1002, ¶114.)

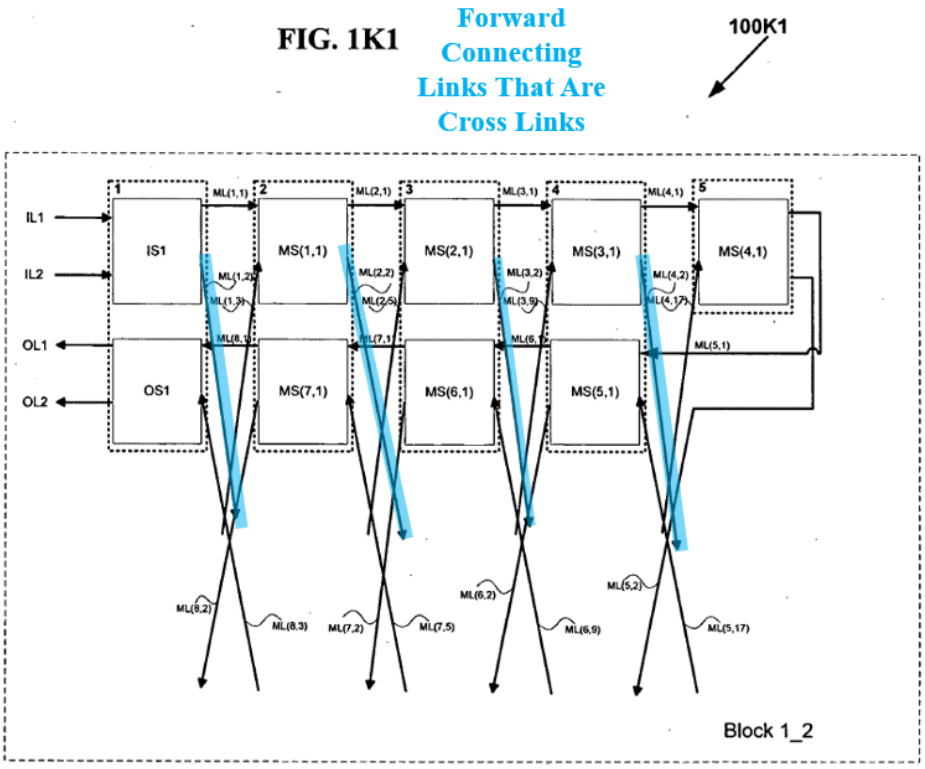


(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶114.)

As shown in annotated figure 1K1 above, middle links ML(1,1), ML(2,1), ML(3,1), and ML(4,1) are forward connecting links between switches in the same sub-integrated circuit block, and a POSITA would have recognized those links are "straight links" in the context of the '523 patent. (Ex. 1002, ¶115.)

(2) "a plurality [of] cross links in said forward connecting links"

The subset of forward connecting links that are also "cross links" is highlighted in annotated figure 1K1 below. (Ex. 1026, FIG. 1K1, 12:10-15; Ex. 1002, ¶116.)



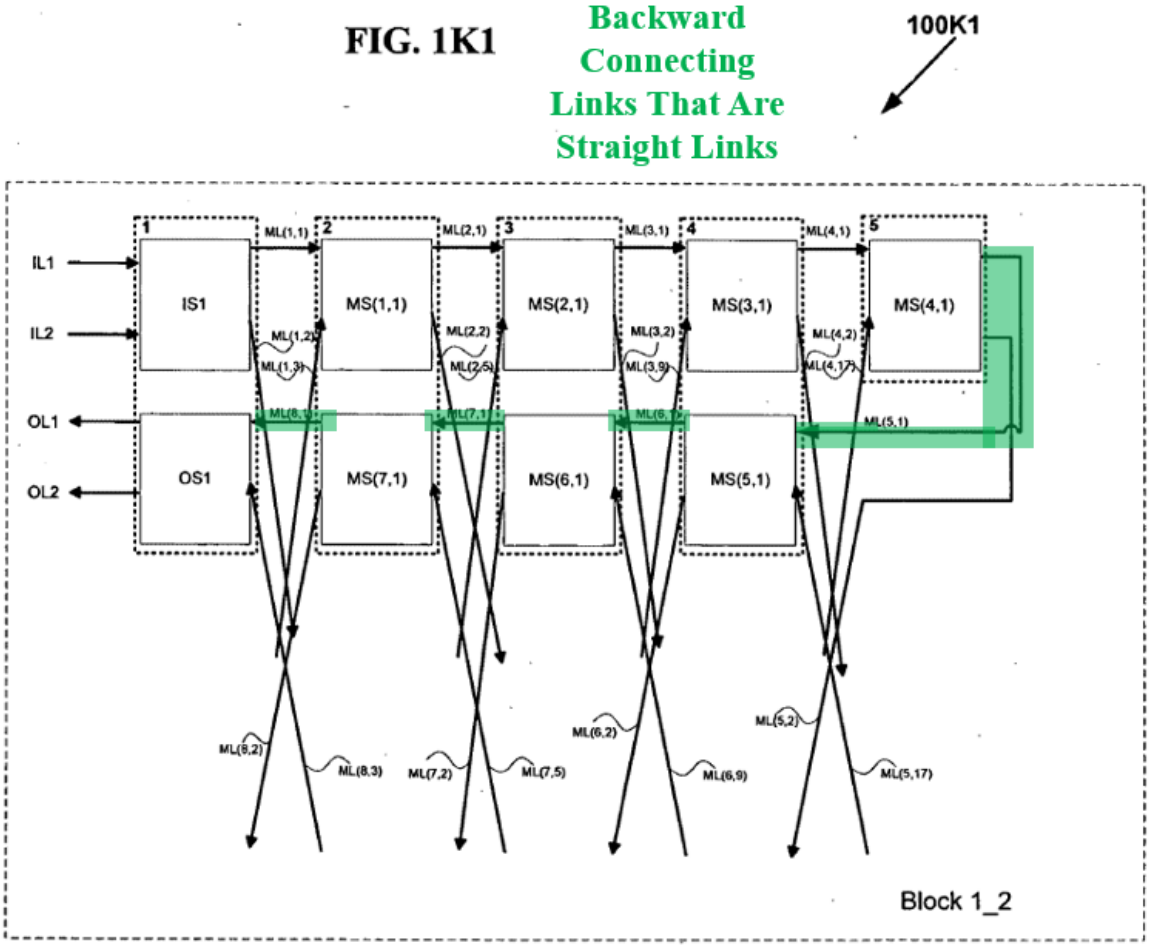
(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶116.)

As shown in annotated figure 1K1 above, middle links ML(1,2), ML(2,2), ML(3,2), and ML(4,2) are forward connecting links between switches in different

sub-integrated circuit blocks, and a POSITA would have recognized those links are "cross links" in the context of the '523 patent. (Ex. 1002, ¶117.)

(3) "a plurality of straight links in said backward connecting links"

As discussed above with respect to limitation 1(g), *Konda '756 PCT* discloses that each sub-integrated circuit block includes a plurality of backward connecting links. (*Supra* Section IX.A.1(g); Ex. 1002, ¶118.) The subset of backward connecting links that are also "straight links" is highlighted in annotated figure 1K1 below. (Ex. 1026, FIG. 1K1, 12:10-15; Ex. 1002, ¶119.)

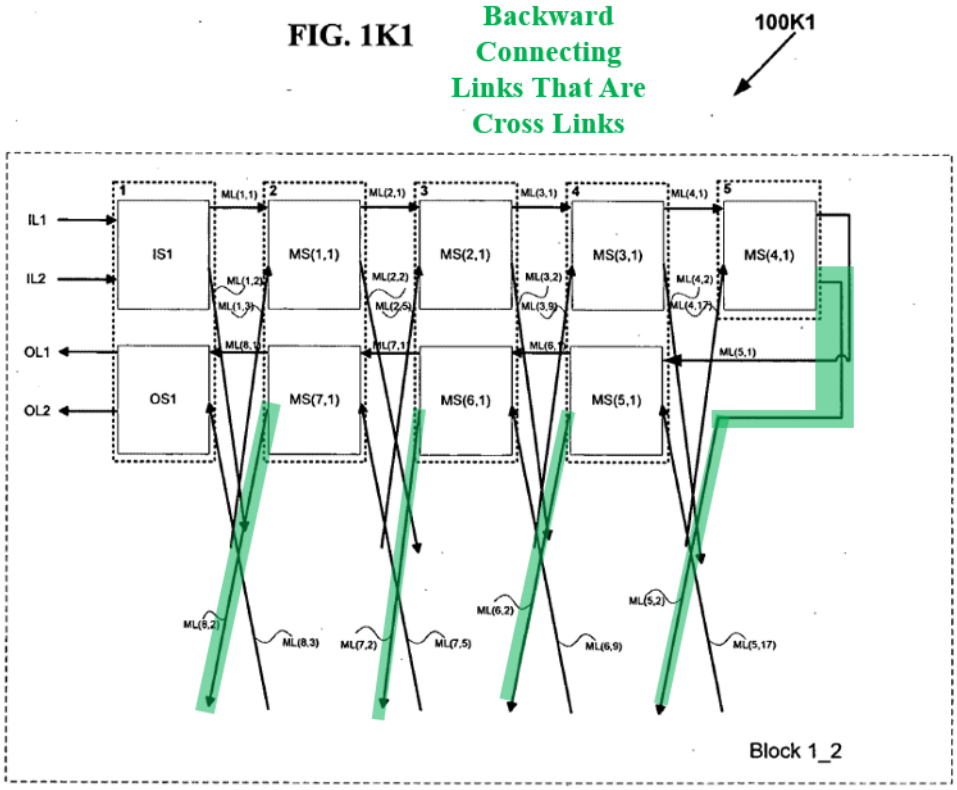


(Ex. 1026 FIG. 1K1 (annotated); Ex. 1002, ¶119.)

As shown in annotated figure 1K1 above, middle links ML(5,1), ML(6,1), ML(7,1), and ML(8,1) are backward connecting links between switches in the same sub-integrated circuit block, and a POSITA would have recognized those links are "straight links" in the context of the '523 patent. (Ex. 1002, ¶120.)

(4) "a plurality of cross links in said backward connecting links"

The subset of backward connecting links that are also "cross links" is shown in annotated figure 1K1 below. (Ex. 1026, FIG. 1K1, 12:10-15; Ex. 1002, ¶121.)

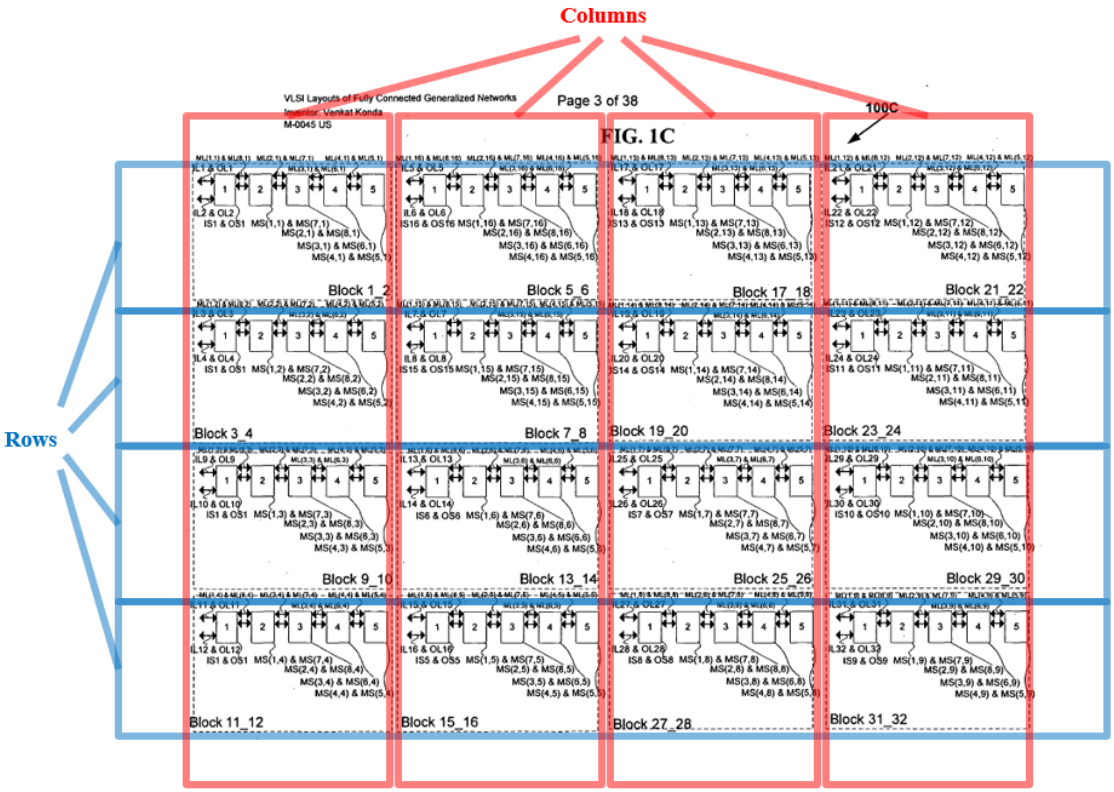


(Ex. 1026, FIG. 1K1 (annotated); Ex. 1002, ¶121.)

As shown in annotated figure 1K1 above, middle links ML(5,2), ML(6,2), ML(7,2), and ML(8,2) are backward connecting links between switches in different sub-integrated circuit blocks, and a POSITA would have recognized those links are "cross links" in the context of the '523 patent. (Ex. 1002, ¶122.)

i) "said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns; and"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶123-124.) For example, figure 1C of the '394 provisional, which is a layout of the network shown in figure 1B, shows the "plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns." (Ex. 1026, 2:17-19, FIG. 1C; Ex. 1002, ¶123.)



(Ex. 1026, FIG. 1C (annotated); Ex. 1002, ¶123.)

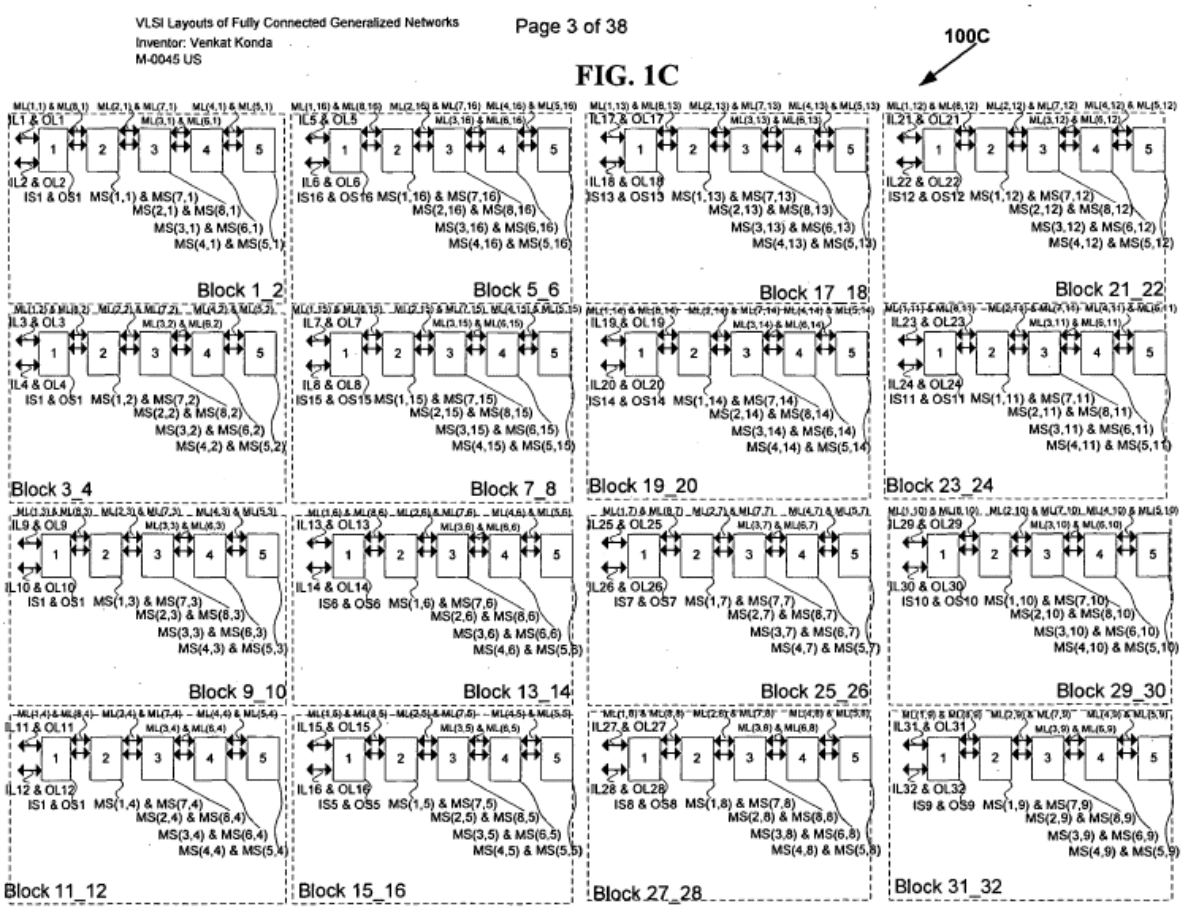
As discussed above with respect to limitation 1(b)(2), each row of switches in the network of figure 1B corresponds to one of the sub-integrated circuit blocks (e.g., one of {block 1_2, block 3_4, … block 31_32}) shown in figure 1C. (Ex. 1026, 20:5-6; *supra* Section IX.A.1(b)(2); Ex. 1002, ¶124.) Similarly, each of figures 1D, 1E, 1F, and 1G shows the blocks of the network of figure 1B arranged in rows and columns. (Ex. 1026, 19:25-20:4, FIGs. 1D-1G; Ex. 1002, ¶124.)

j) "**said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,**"

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶125-130.) As discussed above with respect to limitations 1(h)(1) and 1(h)(3), all of the straight links in the network connect switches within the same sub-integrated circuit block ("said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same integrated circuit block"). (Ex. 1026, FIG. 1K1, 12:10-12; *supra* Sections IX.A.1(h)(1), (3); Ex. 1002, ¶125.)

As shown in figure 1C (below), all of the straight links for the network of figure 1B are between switches within each sub-integrated circuit block. (Ex. 1026, 17:8-14; Ex. 1002, ¶126.)[7]

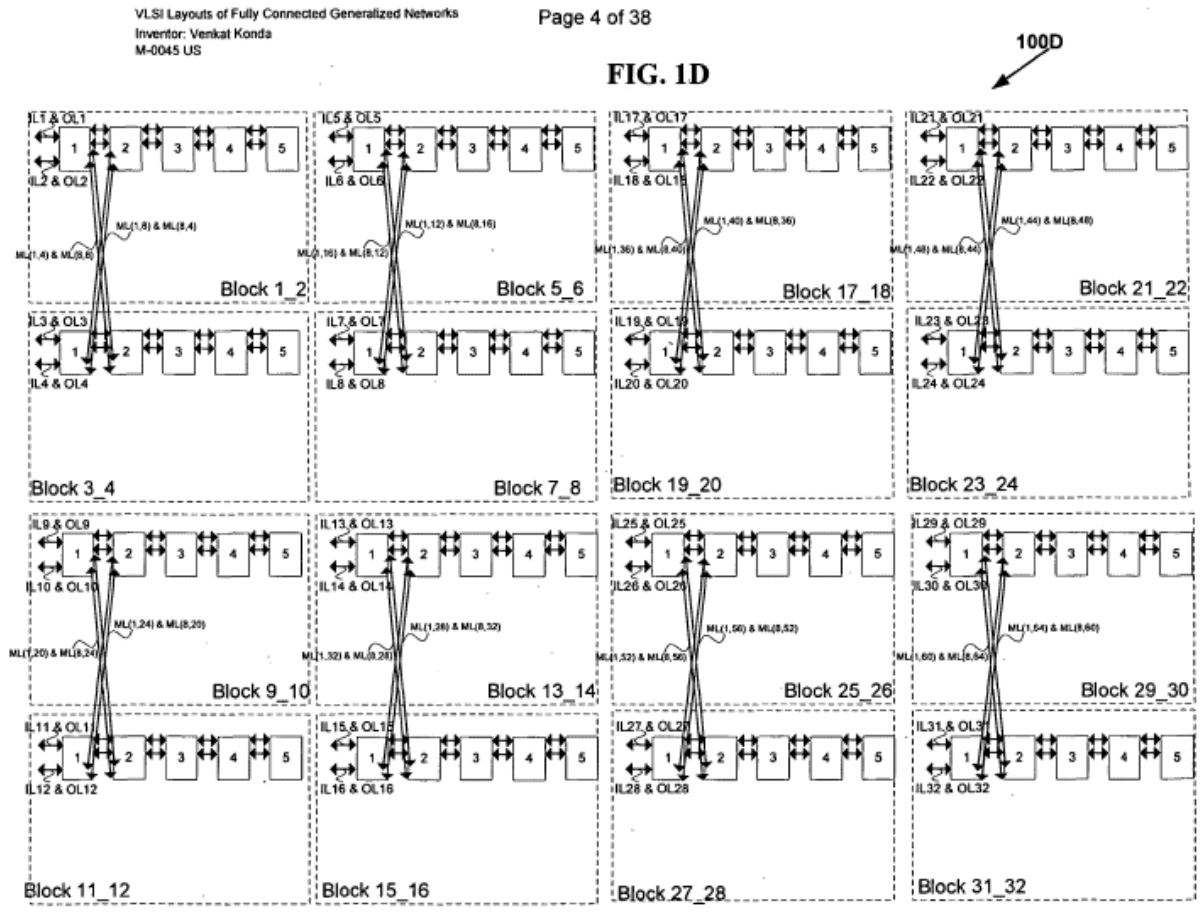
[7] A POSITA would have understood that some of the links shown in figures 1B and 1C of the '394 provisional application are not included in the embodiment shown in figure 1K1, as there is only one link between each set of two switches in figure 1K1 as opposed to two links as shown in figures 1B and 1C. Petitioner's analysis does not rely on those links in figures 1B and 1C that are not present in figure 1K1. (Ex. 1002, ¶126 fn.7.)



(*Id.*, FIG. 1C.)

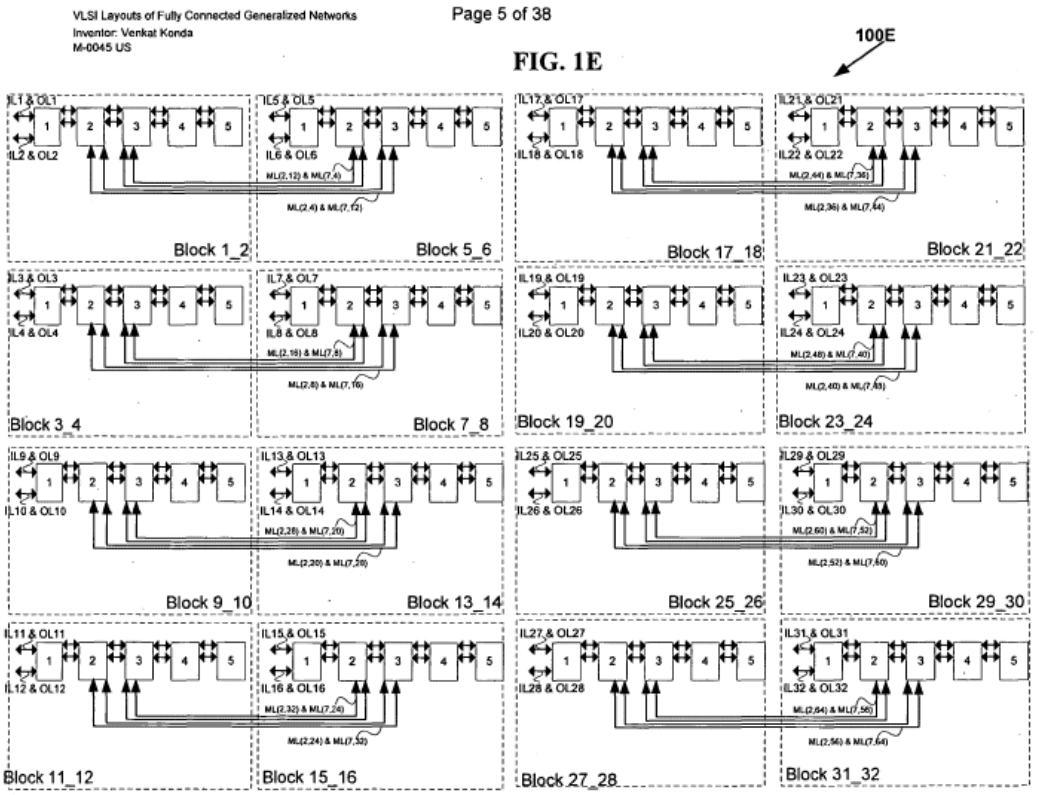
The '394 provisional also discloses that all of the cross links can be implemented as horizontal or vertical tracks between the different sub-integrated circuit blocks of the network, where the sub-integrated circuit blocks are arranged in the two-dimensional grid ("said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right"). (Ex. 1002, ¶127.) For example, figure 1D shows the inter-block

links ("cross links") between stages 1 and 2 are vertical links between switches that are placed vertically above or below each other. (Ex. 1026, 18:11-16, FIG. 1D.)



(*Id.*, FIG. 1D.)

Similarly, figure 1E shows the inter-block links ("cross links") between stages 2 and 3 are horizontal links between switches that are placed horizontally to the left and the right of each other.[8] (*Id.*, 18:11-16, FIG. 1E; Ex. 1002, ¶128.)



(Ex. 1026, FIG. 1E.)

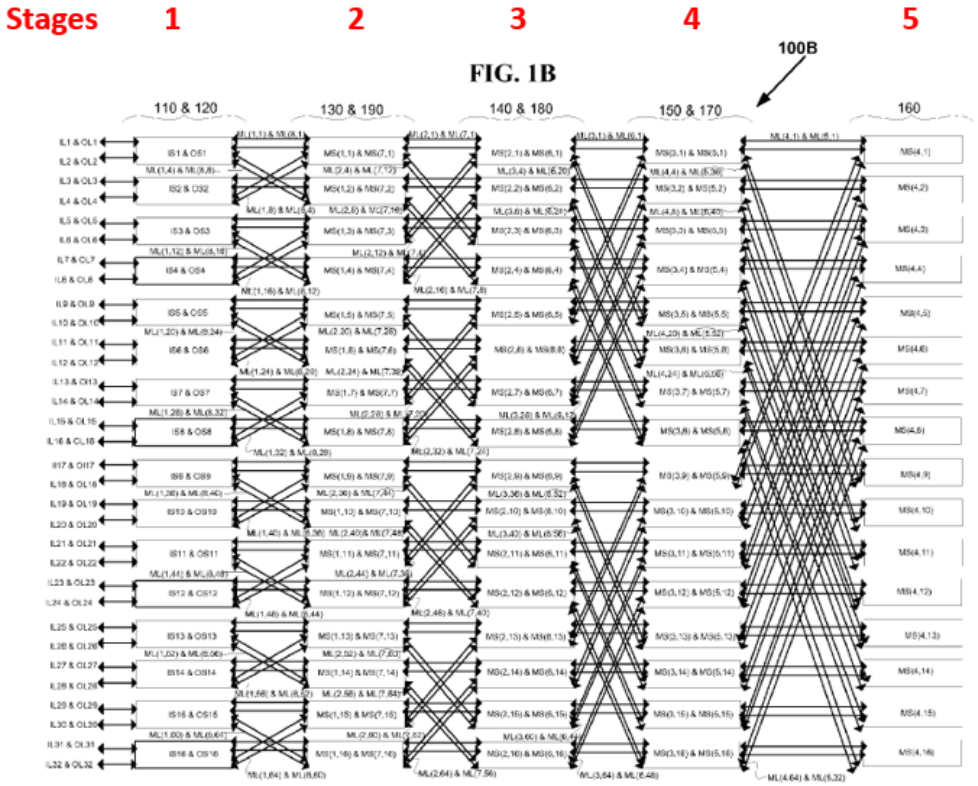
[8] The '394 provisional application incorrectly states that the example inter-stage cross links listed (e.g., ML(2,3), etc.) are between block 1_2 and block 3_4. (Ex. 1026, 18:12-13; Ex. 1002, ¶128 fn.8.) As depicted in figure 1E, the links are actually between block 1_2 and block 5_6. (Ex. 1026, FIG. 1E; Ex. 1002, ¶128 fn.8.)

The '394 provisional includes similar disclosure regarding figures 1F (*id.*, 19:3-8, FIG. 1F) having vertical tracks between stages 3 and 4, and figure 1G (*id.*, 19:14-19, FIG. 1G) having horizontal tracks between stages 4 and 5. (Ex. 1002, ¶129.) According to the '394 provisional, the complete layout for the network 100B of figure 1B can be constructed by combining the links shown in figures 1C-1G, where there is a pattern of alternating vertical and horizontal tracks and all the inter-block links are either horizontal or vertical tracks. (Ex. 1026, 19:25-20:10.)

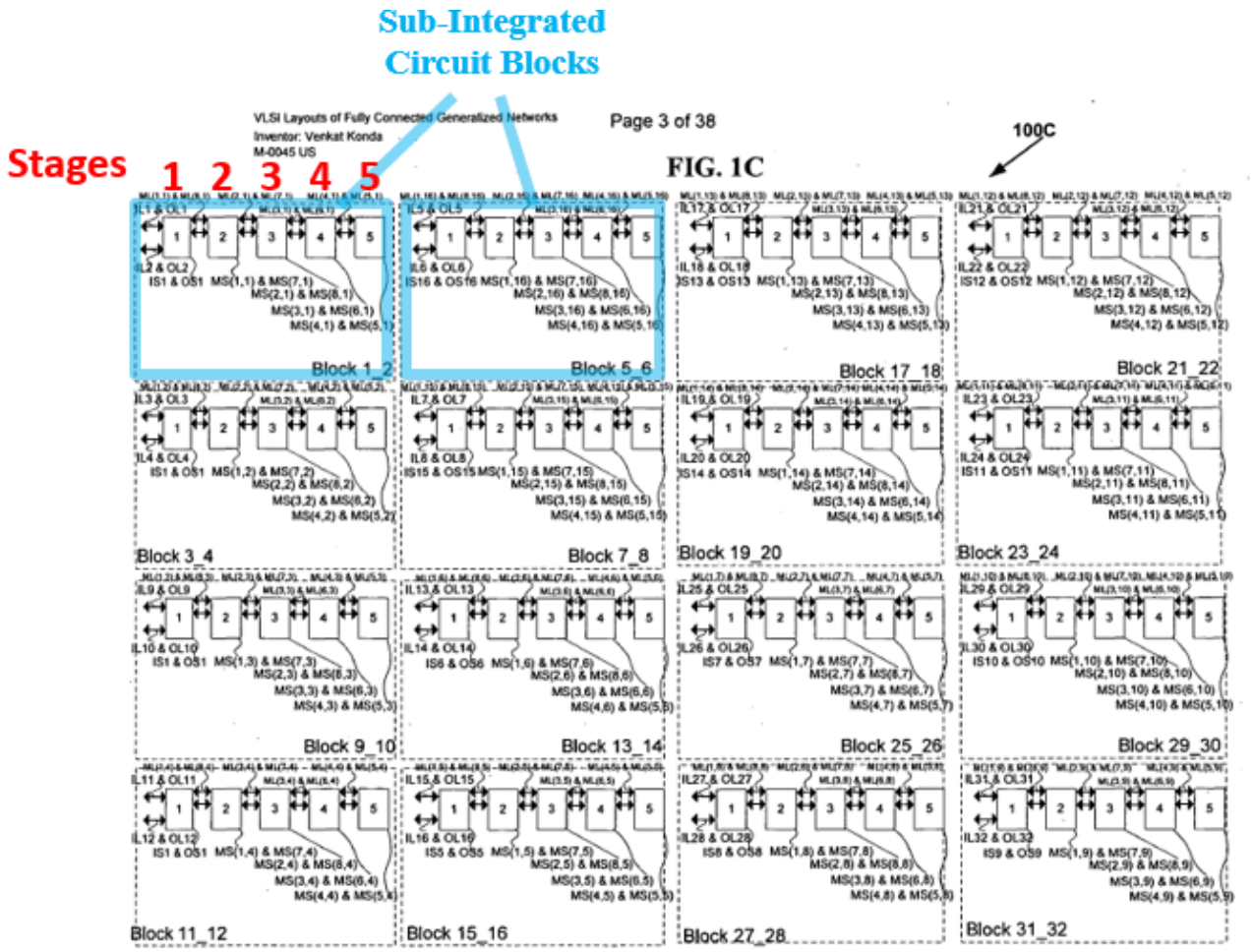
As discussed above, the inter-block links correspond to "cross links," as they connect switches in different blocks. (Ex. 1002, ¶130.) Therefore *Konda '756 PCT* discloses that in the network of figure 1B of the '394 provisional, "said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right" as recited in claim 1. (*Id.*)

k) "each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid."

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶131-136.) For example, figures 1B and 1C of the '394 provisional show that each of the rows in the network ("sub-integrated circuit blocks") has five stages ("same number of stages"). (*Id.*, ¶131.)



(Ex. 1026, FIG. 1B (annotated); Ex. 1002, ¶131.)

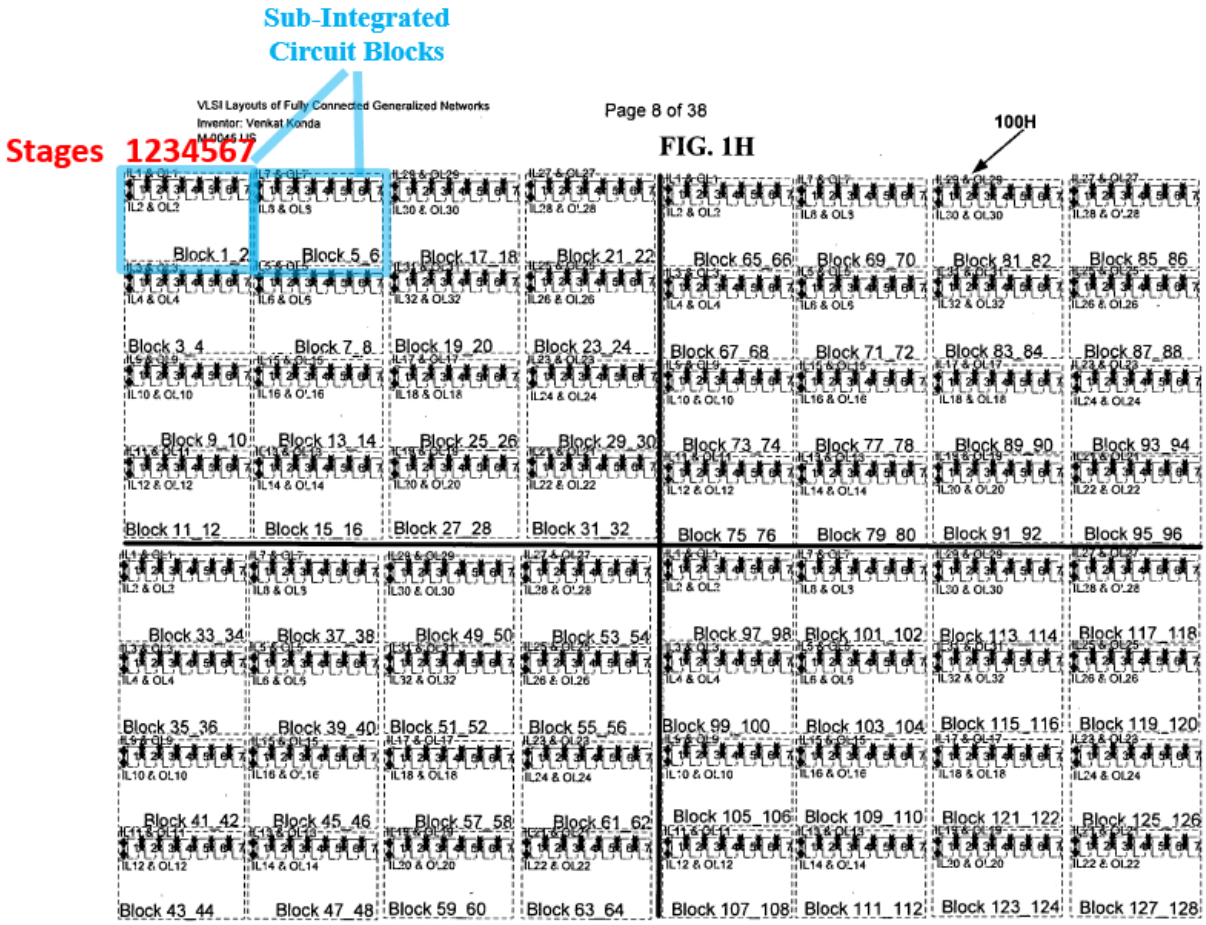


(Ex. 1026, FIG. 1C (annotated); Ex. 1002, ¶131.)

The '394 provisional also discloses that, for each stage in the network of figure 1B, each sub-integrated circuit block has the same number of switches ("each said plurality of sub-integrated circuit blocks comprising same number of … said switches in each said stage"). (Ex. 1002, ¶132.) For example, the '394 provisional discloses "FIG. 1K1 illustrates a high-level implementation of Block 1_2 **(Each of the other blocks have similar implementation)** of layout 100C of FIG. 1C … ."

(Ex. 1026, 30:1-2 (emphasis added).) Therefore, the '394 provisional discloses that each sub-integrated circuit block has the same configuration in the network, and accordingly has the same number of switches in each stage as every other sub-integrated circuit block. (Ex. 1002, ¶132.)

As further disclosed by the '394 provisional, each sub-integrated circuit block has the same configuration (e.g., same number of stages and same number of switches in each stage) regardless of the size of the network. (*Id.*, ¶133.) For example, the '394 provisional states that the pattern of alternating vertical and horizontal tracks for the inter-block links "continues recursively for larger networks of N > 32." (Ex. 1026, 20:2-3.) Similarly, "[i]n accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network … ." (*Id.*, 20:13-15.) Such an extension is shown in figure 1H, where the total number of blocks is 64 in comparison to the 16 blocks in figures 1B and 1C. (*Id.*, 20:19-23; Ex. 1002, ¶133.)



(Ex. 1026, FIG. 1H (annotated); Ex. 1002, ¶133.)

The '394 provisional explains that each block in figure 1H has two more switches (switches 6 and 7) in addition to the switches 1-5 from figure 1C, where the connections between switches 1-5 for figure 1H are the same as that shown in figures 1D-1G. (Ex. 1026, 20:20-28; Ex. 1002, ¶134.) The '394 provisional further discloses that the inter-block links between the switches 6 and 7 in super-quadrants of figure 1H are also vertical and horizontal tracks. (Ex. 1026, 21:7-16; Ex. 1002, ¶135.)

Therefore, the '394 provisional discloses that the network can be expanded by adding additional stages and switches to each of the sub-integrated circuit blocks, where the layout of the blocks continues in a two-dimensional grid and horizontal and vertical links between the blocks are used to provide the inter-block connections. (Ex. 1002, ¶136.) Accordingly, *Konda '756 PCT* discloses that each sub-integrated circuit block in the network has the same number of stages and same number of switches in each stage "regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid." (*Id.*)

2. Claim 16

a) "The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell."

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶137-144.) *Konda '756 PCT* includes figures 4A1-4A4, which correspond to figures 5A1-5A4 of the '523 patent. (*Id.*, ¶137.)

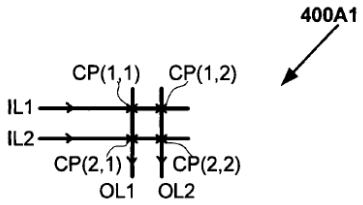


FIG. 4A1
(Prior Art)

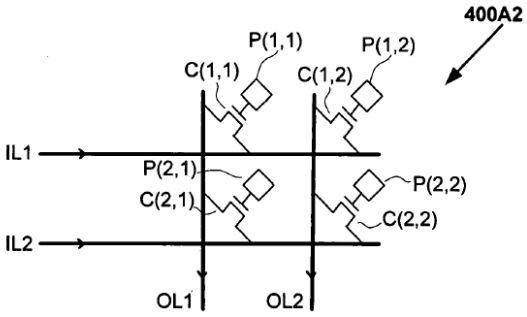


FIG. 4A2
(Prior Art)

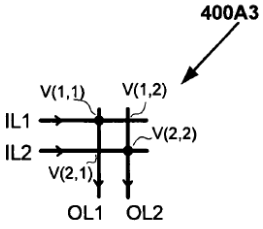


FIG. 4A3
(Prior Art)

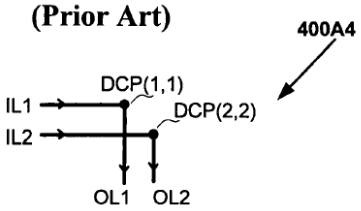


FIG. 4A4

(Ex. 1009, FIGs. 4A1-4A4.)

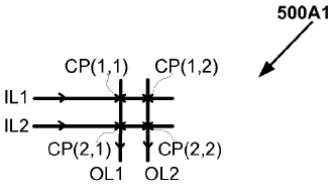


FIG. 5A1
(Prior Art)

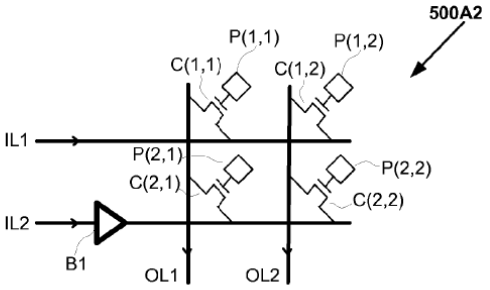


FIG. 5A2
(Prior Art)

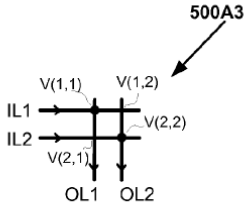


FIG. 5A3
(Prior Art)

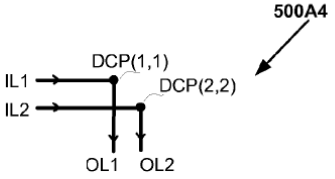


FIG. 5A4

(Ex. 1001, FIGs. 5A1-5A4.)

Aside from the inclusion of a buffer B1 in figure 5A2 of the '523 patent, the figures are otherwise identical aside from the numbering of the illustrated elements. (Ex. 1009, FIGs. 4A1-4A4; Ex. 1001, FIGs. 5A1-5A4; Ex. 1002, ¶138.) Similarly, the text describing figures 4A1-4A4 in *Konda '756 PCT* is virtually identical to that describing figures 5A1-5A4 in the '523 patent. (Ex. 1009, 69:1-72:10; Ex. 1001, 32:60-35:11; Ex. 1002, ¶138.) As discussed below, figures 4A1-4A4 of *Konda '756 PCT*, just like figures 5A1-5A4 of the '523 patent, relate to the disclosure of implementations of cross point switches in one time programmable and reprogrammable embodiments of networks, including the network in figure 1B of the '394 provisional. (Ex. 1002, ¶138.) Therefore, the disclosure in *Konda '756 PCT* of the implementation of the switches in networks as cross points and their use in integrated circuit devices is consistent with that of the '523 patent. (*Id.*)

For example, as disclosed in *Konda '756 PCT*:

> All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 4A1 illustrates the diagram of 400A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(I, I)[sic], CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 4A1. For example the diagram of 400A1 may [be] the implementation of middle switch MS(I, I) [sic] of the diagram I00A [sic] of FIG. IA [sic] … .

(Ex. 1009, 69:2-9; Ex. 1002, ¶139.)

A POSITA would have understood that *Konda '756 PCT*, which incorporates the '394 provisional by reference, discloses that the switches in the networks disclosed, including those of the '394 provisional, can be implemented as cross points such as those shown in figure 4A1. (Ex. 1002, ¶140.)

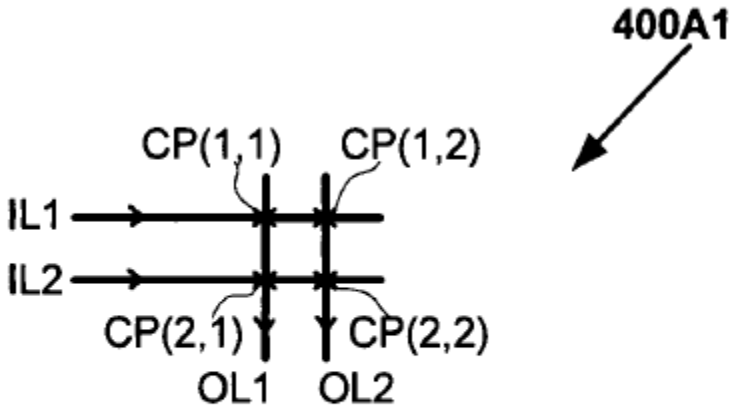


FIG. 4A1
(Prior Art)

(Ex. 1009, FIG. 4A1.)

Moreover, *Konda '756 PCT* also discloses that "[a]ll the embodiments disclosed in the current invention are useful in programmable integrated circuit applications" and that "FIG. 4A2 illustrates the detailed diagram 400A2 for the implementation of the diagram 400A1 in programmable integrated circuit embodiments." (Ex. 1009, 69:14-17; Ex. 1002, ¶141.) As further disclosed by *Konda '756 PCT*, transistors (e.g., C(1,1), C(1,2), C(2,1), and C(2,2) shown in FIG. 4A2 below) are used to implement the cross points between inlet links and outlet links, where the transistors are controlled by corresponding programmable cells (e.g., P(1,1), P(1,2), P(2,1), and P(2,2)). (Ex. 1009, 69:17-70:3; Ex. 1002, ¶142.)

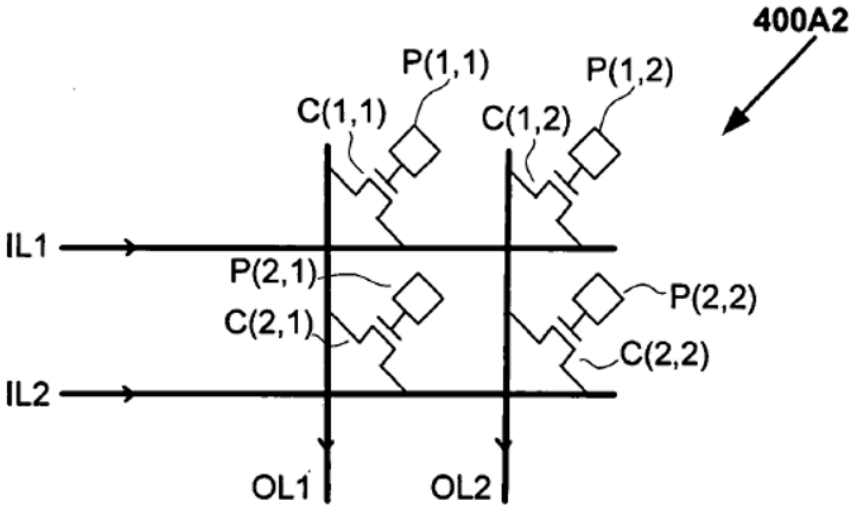


FIG. 4A2
(Prior Art)

(Ex. 1009, FIG. 4A2.)

Konda '756 PCT further discloses that the programmable cells P(1,1), P(1,2), P(2,1), and P(2,2) that configure the switches by controlling the transistors C(1,1), C(1,2), C(2,1), and C(2,2) can be SRAM or Flash cells. (Ex. 1009, 70:3-6; Ex. 1002, ¶143.) Cross points that are configurable by the transistors that are "on" or "off" based on the SRAM and Flash cells are cross points that are "active and reprogrammable cross points." (Ex. 1002, ¶144.) Therefore, *Konda '756 PCT* discloses that the switches shown in the figure 1B embodiment of the '394 provisional can be implemented using cross points with SRAM or Flash memory cells controlling the switches ("said switches comprising active and reprogrammable

cross points and said each cross point is programmable by an SRAM cell or a Flash Cell"). (*Id.*)

3. Claim 20

a) "The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits."

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶145.) As discussed above with respect to limitations 1(b)(2) and 1(c), the '394 provisional discloses an integrated circuit device that includes a "plurality of sub-integrated circuit blocks." (*Supra* Sections IX.A.1(b)(2), IX.A.1(c).) The '394 provisional discloses that "[e]ven through it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be **Configurable Logic Blocks (CLB) or any arbitrary digital circuit** depending on the application in different embodiments." (Ex. 1026, 17:15-17 (emphasis added).) The disclosure of "Configurable Logic Blocks (CLB) or any arbitrary digital circuit" discloses "arbitrary hardware logic" as recited in claim 20. (Ex. 1002, ¶145.) Therefore, *Konda '756 PCT* discloses "said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits." (*Id.*)

4. Claim 21

a) "The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or structured ASIC device."

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶146-151.) As discussed above with respect to claim 16, *Konda '756 PCT* includes figures 4A1-4A4 and the corresponding descriptive text, which is virtually the same disclosure as figures 5A1-5A4 and the accompanying text in the '523 patent. (*Supra* Section IX.A.2.) As such, the disclosure in *Konda '756 PCT* of the implementation of the switches in networks as cross points and their use in integrated circuit devices such as ASICs is consistent with that of the '523 patent. (Ex. 1002, ¶146.)

For example, *Konda '756 PCT*, which incorporates the '394 provisional, discloses that the switches in the disclosed networks, including those of the '394 provisional, can be implemented as cross points such as those shown in figure 4A1. (*Id.*, ¶147.) As disclosed in *Konda '756 PCT*:

> All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 4A1 illustrates the diagram of 400A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(I, I)[sic], CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 4A1. For example the diagram of 400A1 may [be] the implementation of middle switch MS(I, I) [sic] of the diagram I00A [sic] of FIG. IA [sic] … .

(Ex. 1009, 69:2-9.)

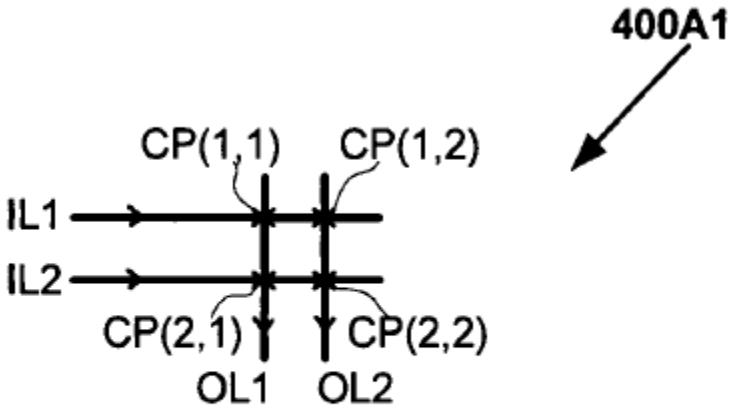


FIG. 4A1
(Prior Art)

(Ex. 1009, FIG. 4A1.)

Konda '756 PCT also discloses:

> All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 4A3 illustrates the detailed diagram 400A3 for the implementation of the diagram 400A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments.

(*Id.*, 70:11-16; Ex. 1002, ¶148.)

Figure 4A3 of *Konda '756 PCT* shows the implementation of the 2x2 switches of figure 4A1 in one-time programmable integrated circuit embodiments.

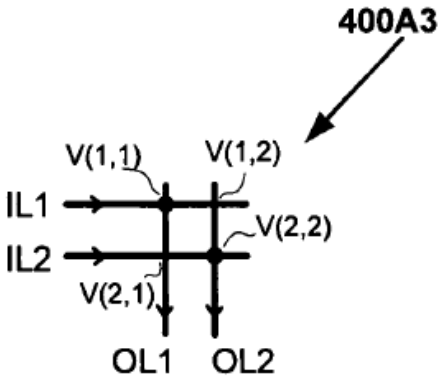


FIG. 4A3
(Prior Art)

(Ex. 1009, FIG. 4A3.)

Konda '756 PCT further discloses that "the programmable integrated circuit embodiments may implement, field programmable logic arrays (FPGA) devices, or programmable Logic devices (PLD), or **Application Specific Integrated Circuits (ASIC)** embedded with programmable logic circuits or 3D-FPGAs." (*Id.*, 70:6-9 (emphasis added); Ex. 1002, ¶150.)

Konda '756 PCT discloses that the switches in the network of figure 1B of the '394 provisional can be implemented as one-time programmable cross points in Application Specific Integrated Circuit (ASIC) embodiments. (Ex. 1002, ¶151.) Therefore, *Konda '756 PCT* discloses the features of claim 21. (*Id.*)

5. Claim 22

a) "The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a[n] Application Specific Integrated Circuit (ASIC) device."

Konda '756 PCT discloses this limitation. (Ex. 1002, ¶¶152-153.) As discussed above with respect to claim 16, *Konda '756 PCT* includes figures 4A1-4A4 and the corresponding descriptive text, which is virtually the same disclosure as figures 5A1-5A4 and the accompanying text in the '523 patent. (*Supra* Section IX.A.2.) As such, the disclosure in *Konda '756 PCT* of the implementation of the switches in networks as cross points and their use in integrated circuit devices such

as ASICs is consistent with that of the '523 patent. (Ex. 1002, ¶152.) For example, *Konda '756 PCT* discloses that all of the disclosed embodiments can be used in ASICs that include cross point switches where vias are used to connect inlet and outlet links of the switches. (Ex. 1009, 70:6-16.)

Konda '756 PCT, which incorporates the '394 provisional, discloses that the switches in the networks disclosed, including those of the '394 provisional, can be implemented as "passive cross points or just connection of two links or not and said integrated circuit device is a[n] Application Specific Integrated Circuit (ASIC) device" as recited in claim 22. (Ex. 1002, ¶153.) For example, in addition to the cross points discussed above with respect to claim 21, figure 4A3 shows that the presence or absence of a via at the intersection of an inlet link and an outlet link corresponds to "just connection of two links or not." (*Id.*)

6. Claim 32

a) "The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

Said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks."

Konda '756 PCT discloses this limitation, for at least the same reasons presented above regarding limitation 1(j). (*Supra* Section IX.A.1(j); Ex. 1002, ¶154.)

B. Ground 2: *Konda '756 PCT* Renders Obvious Claims 15 and 17

1. Claim 15

a) "The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers."

Konda '756 PCT discloses or suggests this limitation. (Ex. 1002, ¶¶155-160.) As discussed above with respect to claim 16, *Konda '756 PCT* includes figures 4A1-4A4 and the corresponding descriptive text, which is virtually the same disclosure as figures 5A1-5A4 and the accompanying text in the '523 patent. (*Supra* Section IX.A.2.) As such, the disclosure in *Konda '756 PCT* of the implementation of the switches in networks as cross points and their use in ASIC devices is consistent with that of the '523 patent. (Ex. 1002, ¶155.) For example, *Konda '756 PCT* discloses

that all of the disclosed embodiments can be used in ASICs that include cross point switches where vias are used to connect inlet and outlet links of the switches. (Ex. 1009, 70:6-16.)

While *Konda '756 PCT* does not explicitly disclose that the inlet links and outlet links, which include the horizontal and vertical cross links, are routed using two or more metal layers, this feature would have been obvious. (Ex. 1002, ¶¶156-160.) A POSITA would have known that metal layers are typically used to provide electrical connections on an integrated circuit. (*Id.*, ¶156 (citing Ex. 1008, 13:49-54).)[9] Moreover, *Konda '756 PCT* describes using "vias" to connect inlet links and outlet links (Ex. 1009, 70:14-16), and a POSITA would have known that vias are commonly used to interconnect two different metal layers in an integrated circuit device. (Ex. 1002, ¶157 (citing Ex. 1041, 1:8-9, 5:17-19; Ex. 1042, 1:60-61).)[10]

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[9] Petitioner is citing *Wong* (Ex. 1008) only to demonstrate knowledge of a POSITA, and does not rely on *Wong* in this unpatentability ground.

[10] Petitioner is citing *Ireland* (Ex. 1041) and *Cai* (Ex. 1042) only to demonstrate knowledge of a POSITA, and does not rely on *Ireland* or *Cai* in this unpatentability ground.

As discussed above with respect to claim 21, figure 4A3 of *Konda '756 PCT* shows an implementation of 2x2 switches that can be used in some embodiments corresponding to figure 1B of the '394 provisional. (*Supra* Section IX.A.4; Ex. 1002, ¶158.) For switches in stages 2-5 of figures 1B and 1K1 of the '394 provisional, some of the inlet links and outlet links correspond to cross links included in the network. (*Supra* Sections IX.A.1(e),(g),(h); Ex. 1002, ¶158.) As discussed above with respect to claim element 1(j), those cross links are implemented as horizontal or vertical links. (*Supra* Section IX.A.1(j); Ex. 1002, ¶158.)

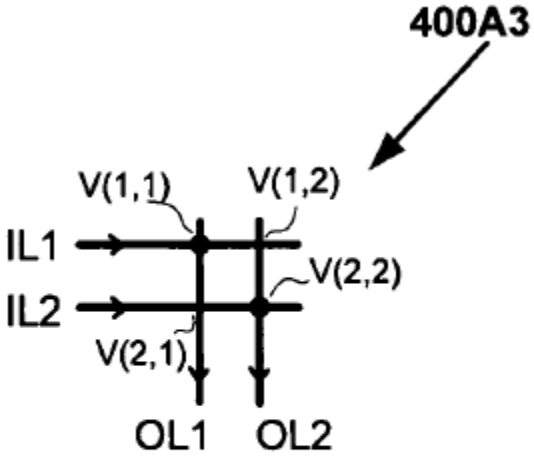


FIG. 4A3
(Prior Art)

(Ex. 1009, FIG. 4A3.)

Konda '756 PCT discloses that via V(1,1) provides a connection between inlet link IL1 and outlet link OL1 of the 2x2 switch, whereas via V(2,2) provides a

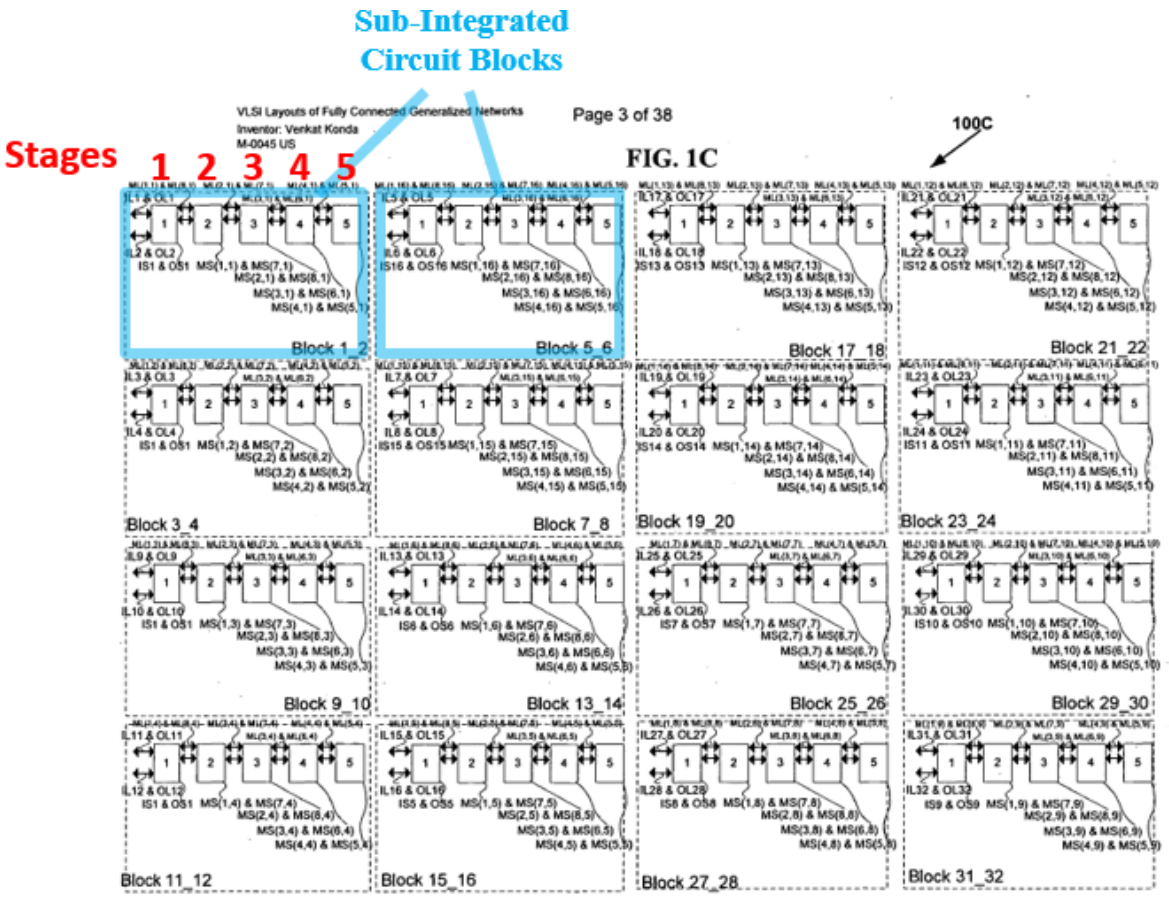
connection between inlet link IL2 and outlet link OL2 of the 2x2 switch. (Ex. 1009, 70:22-71:1; Ex. 1002, ¶159.) It would have been obvious to implement the inlet links IL1 and IL2 in a different metal layer than the outlet links OL1 and OL2. (Ex. 1002, ¶159.) This would have been a mere combination of known components and technologies, according to known methods, to produce predictable results. (*Id.*, ¶¶159-160.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Indeed, if the same metal layer were used for IL1, IL2, OL1, and OL2, the inlet links would connect to the outlet links at every point of intersection, which would not allow selective connections to be made. (Ex. 1002, ¶159.) Conversely, a POSITA would also have understood that if IL1 and IL2 are in one metal layer and OL1 and OL2 are in another metal layer, then the inlet links can advantageously cross over/under the outlet links without forming a connection. (*Id.*) When a connection is desired, a via is used to connect the two links, which is consistent with the disclosure of *Konda '756 PCT* and the '523 patent. (*Id.*)

Therefore, *Konda '756 PCT* discloses that the inlet links and outlet links shown in figure 4A3 above include cross links implemented as vertical and horizontal links in the routing network, and it would have been obvious to configure the integrated circuit device of *Konda '756 PCT* to implement the inlet links in one metal layer and the outlet links in a different metal layer. (*Id.*, ¶160.)

2. Claim 17

a) "The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks are of equal die size."

Konda '756 PCT discloses or suggests this limitation. (Ex. 1002, ¶¶161-162.) As discussed above with respect to limitation 1(k), the '394 provisional, which is incorporated by reference in *Konda '756 PCT*, discloses "FIG. 1K1 illustrates a high-level implementation of Block 1_2 **(Each of the other blocks have similar implementation)** of layout 100C of FIG. 1C … ." (Ex. 1026, 30:1-2 (emphasis added); *supra* Section IX.A.1(k); Ex. 1002, ¶161.)



(Ex. 1026, FIG. 1C (annotated); Ex. 1002, ¶161.)

Therefore, the '394 provisional discloses that each sub-integrated circuit block has the same configuration (same number of stages and same number of switches in each stage) in the network. (*Supra* Section IX.A.1(k); Ex. 1002, ¶162.) While the '394 provisional does not explicitly disclose that the "sub-integrated circuit blocks are of equal die size," it would have been obvious to configure the integrated circuit device of *Konda '756 PCT* to use the same layout for each of the sub-integrated circuit blocks on the integrated circuit device. (Ex. 1002, ¶162.) The

use of equal (as opposed to unequal) die size would have been recognized as being a mere choice among a finite number of known alternatives, each having predictable outcomes. (*Id.*) *KSR*, 550 U.S. at 421. Reusing the layout for each of the blocks would have been recognized as more efficient from a design standpoint and would have ensured uniformity in placing the blocks in the two-dimensional grid and uniformity in block operation (delays, drive strength, etc.). (Ex. 1002, ¶162.) Because a POSITA would have been motivated to use the same layout for the sub-integrated circuit blocks, the area on the integrated circuit occupied by each of the sub-integrated circuit blocks ("die size") would have been the same in such a configuration. (*Id.*) Therefore, *Konda '756 PCT* discloses or suggests that all of the sub-integrated circuit blocks have "equal die size."

C. Ground 3: *Konda '756 PCT* In View of *Wong* Renders Obvious Claims 18 and 47

1. Claim 18

a) "The integrated circuit device of claim 15, where said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device."

Konda '756 PCT in view of *Wong* discloses or suggests this limitation. (Ex. 1002, ¶¶163-171.) As discussed above, *Konda '756 PCT* discloses or suggests an

integrated circuit as recited in claim 15. (*Supra* Section IX.B.1.) Moreover, as discussed above with respect to limitation 1(a), *Konda '756 PCT* discloses that the integrated circuit is an FPGA. (Ex. 1026, 8:21-9:2, 9:8-10; *supra* Section IX.A.1(a).) *Konda '756 PCT* does not explicitly disclose "where said sub-integrated circuit blocks are Lookup Tables (hereinafter 'LUTs')."[11] However, *Wong* discloses the inclusion of lookup tables with the routing network, and it would have been obvious to include such lookup tables in the integrated circuit that includes the network of figure 1B of the '394 provisional as incorporated by reference in *Konda '756 PCT*. (Ex. 1002, ¶164.)

Wong, like *Konda '756 PCT*, is in the field of interconnection networks used in, for example, FPGA devices. (Ex. 1008, Title, 1:14-17; Ex. 1009, 13:23-14:5; Ex. 1026, 8:21-9:7; Ex. 1002, ¶165.) Indeed, *Wong*, like *Konda '756 PCT*, discloses

[11] Claim 18 conflicts with claim 1 by stating that the "sub-integrated circuit blocks **are** Lookup Tables." For the present analysis, Petitioner assumes that claim 18 requires that a lookup table is included in each of the sub-integrated circuit blocks recited in claim 1 like the configurable logic blocks or arbitrary digital circuits interconnected by the routing network. (Ex. 1001, 13:38-42; Ex. 1002, ¶164 fn.9.)

Benes networks that include a plurality of stages of switches for use in FPGAs. (Ex. 1008, 1:59-2:6; Ex. 1026, 15:1-2, 2:7-16.) Therefore, a POSITA implementing an integrated circuit device that includes a routing network as disclosed in of *Konda '756 PCT* would have had reason to look to *Wong*. (Ex. 1002, ¶165.)

Wong discloses a network with the same general topology as figure 1B of the '394 provisional application. (*Id.*, ¶166.) For example, similar to figure 1B of the '394 provisional application, figure 13A of *Wong* shows a routing network made up of switches in stages, where the network is used to provide connections between logic cells. (Ex. 1008, FIG. 13A.)

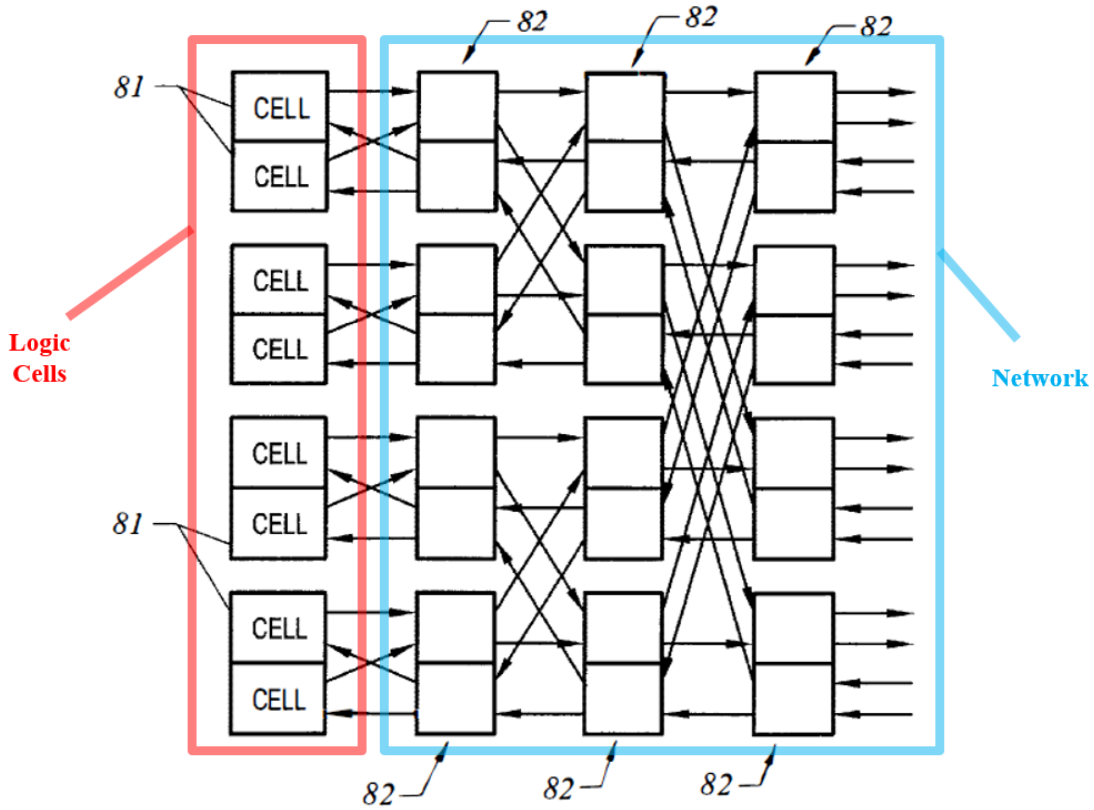
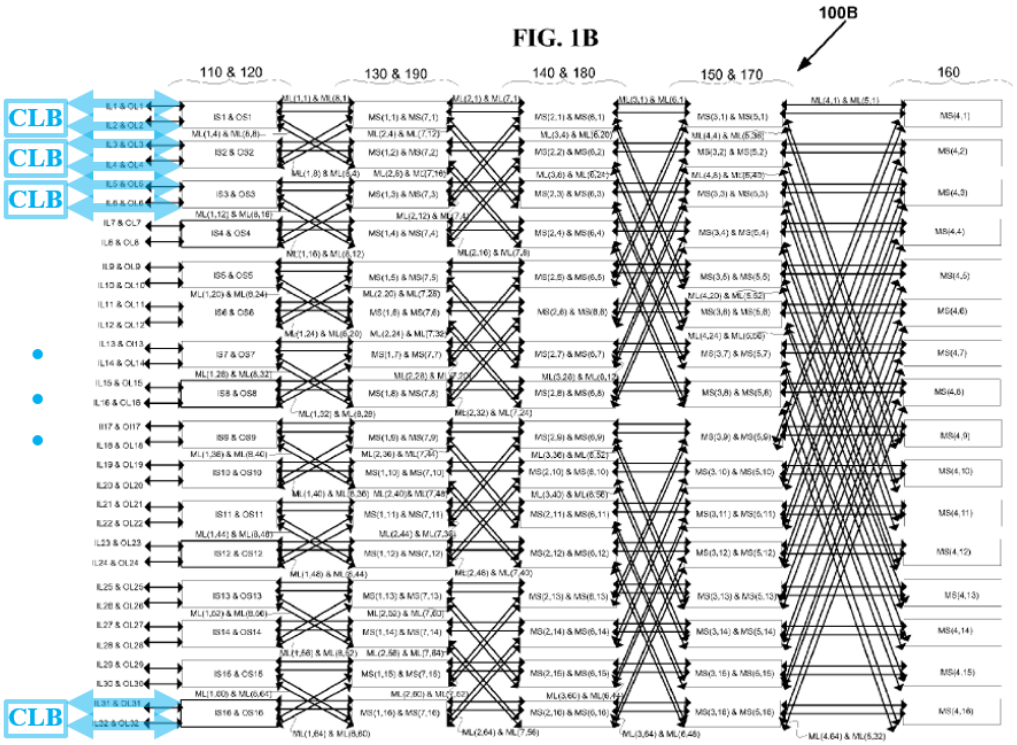


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶166.)

As discussed above with respect to limitations 1(c) and 1(f), *Konda '756 PCT*, which incorporates the '394 provisional by reference, similarly discloses a routing network that connects to "configurable logic blocks" shown as CLBs in annotated figure 1B below. (Ex. 1026, FIG. 1B; *supra* Sections IX.A.1(c), (f); Ex. 1002, ¶167.) The '394 provisional discloses that "[e]ven through it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be **Configurable Logic Blocks (CLB) or any arbitrary digital circuit** depending on

the application in different embodiments." (Ex. 1026, 17:15-17 (emphasis added).) While *Konda '756 PCT* does not explicitly disclose the "Configurable Logic Blocks (CLB) or any arbitrary digital circuit" can include a lookup table, it would have been obvious in light of *Wong* to implement this feature in the integrated circuit device of *Konda '756 PCT*. (Ex. 1002, ¶167.)



(Ex. 1026, FIG. 1B (annotated); Ex. 1002, ¶167.)

Wong discloses that the logic cells that connect to the routing network in FPGA embodiments can be lookup tables. (Ex. 1008, 8:51-51, 9:9-11; Ex. 1002, ¶168.) A POSITA would have known that a lookup table provides a flexible circuit that can be configured to provide a variety of logic functions. (Ex. 1002, ¶168.) A

POSITA would have understood that lookup tables are especially advantageous in FPGAs where a user may wish to not only configure the routing of the network, but also may want to configure the logic that is interconnected by the network. (*Id.* (citing Ex. 1026, 10:25-11:3, 17:15-17).) A POSITA would have been motivated to use lookup tables in conjunction with the network of figure 1B of the '394 provisional. (Ex. 1002, ¶169.) The '394 provisional does not disclose specifics regarding what constitutes a "configurable logic block," so a POSITA would have had cause to look to *Wong*, which discloses the use of lookup tables in the same manner as the configurable logic blocks in the '394 provisional. (*Id.*)

The use of lookup tables with the network disclosed in the '394 provisional would have been straightforward to implement because *Wong* discloses how such lookup tables can be used in conjunction with such a network. (Ex. 1008, 8:51-51, 9:9-11, FIG. 9; Ex. 1002, ¶170.) A POSITA would have thus had reason and the capability to modify *Konda '756 PCT* based on *Wong* as discussed immediately above. (Ex. 1002, ¶171.) This modification would have been a predictable combination of known components, according to known methods, to produce predictable results. (*Id.*) *KSR*, 550 U.S. at 416.

2. Claim 47

a) "The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers."

Konda '756 PCT in view of *Wong* discloses or suggests this limitation. (Ex. 1002, ¶¶172-178.) As discussed above, *Konda '756 PCT* discloses an integrated circuit as recited in claim 1, which includes a plurality of forward connecting links and a plurality of backward connecting links. (*Supra* Section IX.A.1.) *Konda '756 PCT* does not explicitly disclose "said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers," but it would have been obvious in view of *Wong* to include such buffers in the forward and backward connecting links of the integrated circuit that includes the network of figure 1B of the '394 provisional as incorporated by reference in *Konda '756 PCT*. (Ex. 1002, ¶172.)

As discussed above with respect to claim 18, a POSITA implementing the integrated circuit device that includes a routing network of *Konda '756 PCT* would

have had reason to look to *Wong*. (*Supra* Section IX.C.1.) As also discussed above, *Wong* discloses a network with the same topology as figure 1B of the '394 provisional. (*Id.*) For example, similar to figure 1B of the '394 provisional, figure 13A of *Wong* shows a routing network made up of switches in stages, where the network is used to provide connections between logic cells. (Ex. 1008, FIG. 13A; Ex. 1002, ¶173.)

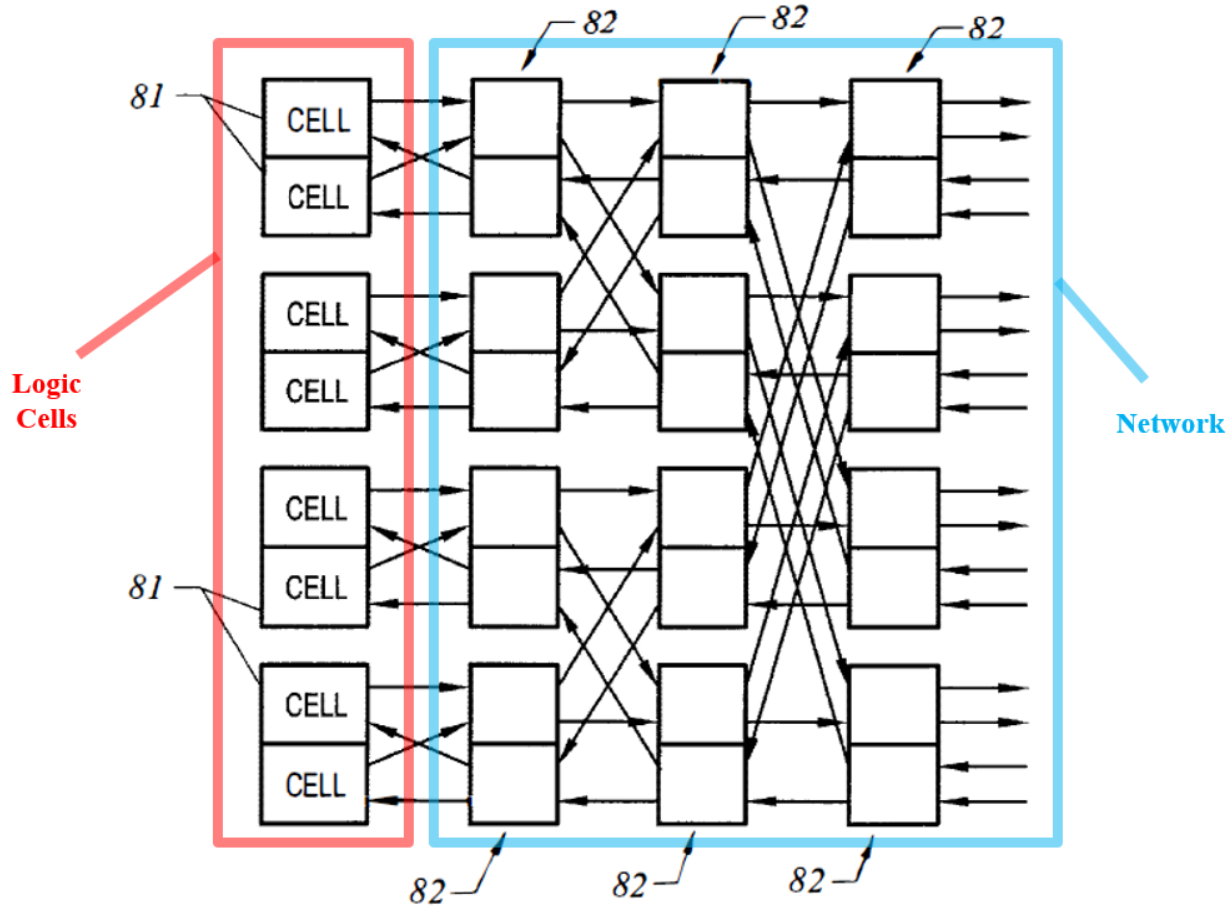


FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶173.)

The network in figure 13A of *Wong* includes forward connecting links (links with arrows going to the right) and backward connecting links (links with arrows going to the left). (Ex. 1008, FIG. 13; Ex. 1002, ¶174.) *Wong* further discloses:

> Buffers can be inserted without affecting the logic of the design. In fact, most commercial place-and-route tools will insert buffers on signals with long routing lines in order to improve their overall delay; this is done transparently for the user. The present invention allows buffer insertion to be made simply because the signal delays through the interconnect network are known.

(Ex. 1008, 10:60-67.)

Wong also discloses that buffers can be inserted to lengthen shorter delay paths until the delay paths match. (*Id.*, 11:1-6.) A POSITA would have understood that the buffers disclosed by *Wong* include "non-inverting" buffers. (Ex. 1002, ¶175.) *Wong* discloses that "[b]uffers can be inserted without affecting the logic of the design," thereby indicating that no further circuitry is required to maintain the logic of a circuit to which the buffers are added. (*Id.*; Ex. 1008, 10:60-61; *see also id.*, FIGs. 11A, 11B.) If inverting buffers were used, further inversion would be required in order to restore the non-inverted state of the signal being inverted. (Ex. 1002, ¶175.) In any event, the use of a non-inverting buffer was well known long

before the alleged *invention* date of the '523 patent, e.g., for adjusting or compensating timing in a circuit. (*Id*. (citing Ex. 1045, 2:9-11.)) Therefore, the use of "non-inverting" buffers would have been entirely predictable. (Ex. 1002, ¶175.)

Both inverting and non-inverting buffers were commonly used in circuit designs in order to alter the delay of a signal or the drive strength for a signal. (*Id.*, ¶176.) A POSITA would have been motivated to include buffers in the forward and backward connecting links in the network of figure 1B of the '394 provisional. (*Id.*) Such a person would have understood that by including buffers, timing and drive strength issues can be rectified such that signals properly propagate through the network. (*Id.* (citing Ex. 1008, 10:60-67, 11:1-6).)

The inclusion of buffers in the forward and backward connecting links of the network disclosed in the '394 provisional would have been straightforward to implement because a POSITA would have been very familiar with the use of such buffers. (Ex. 1002, ¶177 (citing Ex. 1008, 10:60-67, 11:1-6).) Moreover, a POSITA would also have understood that such buffers can be either inverting or non-inverting, where an example of an inverting buffer is an inverter, whereas a non-inverting buffer can be realized with two serially-connected inverters. (Ex. 1002, ¶177.)

A POSITA would have thus had reason and the capability to modify *Konda '756 PCT* based on *Wong* as discussed immediately above. (*Id.*, ¶178.) Therefore, a POSITA would have been motivated to make, and would have been capable of making, the above-noted modification of the *Konda '756 PCT* circuit based on *Wong*. (*Id.*) This modification would have been a predictable combination of known components, according to known methods, to produce predictable results. (*Id.*) *KSR*, 550 U.S. at 416.

X. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1, 15-18, 20-22, 32, and 47 of the '523 patent, and a finding that the claims are unpatentable based on the above grounds.

Respectfully submitted,

Dated: December 16, 2019 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,269,523 contains, as measured by the word processing system used to prepare this paper, 13,834 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: December 16, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on December 16, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,269,523 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

Konda Technologies, Inc
6278 Grand Oak Way
San Jose, CA 95135

A courtesy copy was also sent via electronic mail to the Patent Owner at the following address:

venkat@kondatech.com

Respectfully submitted,

Dated: December 16, 2019

By: /Naveen Modi/
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Counsel for Petitioner