Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMIC, AMERICAS,

Petitioner

v.

INNOVATIVE FOUNDRY TECHNOLOGIES, LLC,

Patent Owner

CASE NO.: IPR2020-00837
PATENT NO. 6,608,126

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,608,126

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Exhibit No.	Description
Exhibit 1001	U.S. Patent No. 6,806,126 to Scott Luning, *et al*., filed on September 6, 2002, and issued on October 19, 2004 ("'126 patent").
Exhibit 1002	Prosecution history of the '126 patent.
Exhibit 1003	U.S. Patent No. 6,258,680 to Fulford, Jr. *et al*. ("AMD 680").
Exhibit 1004	U.S. Patent No. 6,235,598 to Jan *et al*. ("Intel 598").
Exhibit 1005	Declaration of R. Jacob Baker, Ph.D.
Exhibit 1006	U.S. Patent No. 6,344,405 to Saha ("Phillips 405").
Exhibit 1007	Claim chart – Ground 1: Claims 1-19 of the '126 patent would have been obvious under 35 U.S.C. §103(a) over AMD 680 (Ex. 1003) in view of Intel 598 (Ex. 1004) and the knowledge of one of ordinary skill in the art.
Exhibit 1008	Claim chart – Ground 2: Claims 1-2, 4-8, 12, 14, 16-17 and 19 of the '126 patent are anticipated by AMD 680 (Ex. 1003) under 35 U.S.C. §102(b).
Exhibit 1009	B.E. Deal & A. S. Grove, *General Relationship for the Thermal Oxidation of* Silicon, Abstract, Journal of Applied Physics; vol. 36, no. 12 (Dec. 1965).
Exhibit 1010	*Curriculum Vitae* of R. Jacob Baker, Ph.D.
Exhibit 1011	U.S. Patent No. 6,498,067 ("TSMC 067") to Perng *et al*.
Exhibit 1012	U.S. Patent No. 6,596,576 ("AMI 576") to Fu *et al*.
Exhibit 1013	U.S. Patent No. 6,225,176 ("AMD 176") to Yu
Exhibit 1014	U.S. Patent No. 6,383,882 ("Samsung 882") to Lee *et al*.
Exhibit 1015	U.S. Patent No. 6,291,354 to Hsiao *et al.* ("UMC 354").
Exhibit 1016	U.S. Patent No. 6,274,906 to Kim *et al*. ("Samsung 906").
Exhibit 1017	Complaint for Patent Infringement, filed on December 20, 2019, by Innovative Foundry Technologies, LLC, Case No. 6:19-cv-00719-ADA (W.D. Texas).

Exhibit No.	Description
Exhibit 1018	Complaint for Declaratory Judgment, filed on April 2, 2020 in *SMIC, Americas et al. v. Innovative Foundry Technologies, LLC*, No. 3:20-cv-02256-JCS (N.D. Cal.).

I. INTRODUCTION

SMIC, Americas ("SMIC" or "Petitioner") respectfully requests *Inter Partes* Review ("IPR") of claims 1-19 ("Challenged Claims") of U.S. Patent No. 6,806,126 to Luning *et al.*, ("'126 patent") (Ex. 1001) under 35 U.S.C. § 102(b) as anticipated and under 35 U.S.C. §103(a) as obvious in view of the prior art. SMIC is reasonably likely to prevail on the grounds of unpatentability submitted herein with respect to at least one Challenged Claim. The claims of the '126 patent recite nothing more than well-known techniques of (i) using spacers to form graded junctions for the purpose of reducing short-channel effects in semiconductor devices, and (ii) recessing the spacers to increase the amount of exposed silicon surface area for forming silicide on the gate sidewalls of the semiconductor devices for the purpose of reducing gate resistance. The prior art presented in this Petition—U.S. Patent Nos. 6,258,680 ("AMD 680") and 6,235,598 ("Intel 598")—discloses the very same techniques and was not considered during original prosecution. SMIC therefore respectfully requests that the Board institute IPR and cancel claims 1-19 of the '126 patent.

II. MANDATORY NOTICES (37 C.F.R. § 42.8)

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

In accordance with 37 C.F.R. § 42.8(b)(1), Petitioner SMIC is a real party-in-interest. Semiconductor Manufacturing International Corporation, at P.O. Box 2681, Cricket Square, Hutchins Drive, George Town, Grand Cayman KY1-111,

Cayman Islands, ("SMIC Cayman") is a named defendant in the related, co-pending litigation, discussed below, and is a holding company without any operations and does not manufacture, use, sell, offer to sell, or import into the United States any products accused of infringement in the related litigation. Petitioner does not believe that SMIC Cayman qualifies as a real party-in-interest. However, Petitioner identifies SMIC Cayman under 37 CFR § 42.8(b)(1) and confirms that SMIC Cayman is willing to be treated as a real party-in-interest in both this IPR and the related district court litigation, but only because it is a named defendant in that litigation. Petitioner also identifies the following entities as real parties-in-interest: Semiconductor Manufacturing International (Shanghai) Corporation ("SMIC Shanghai"); Semiconductor Manufacturing International (Beijing) Corporation ("SMIC Beijing"); Semiconductor Manufacturing International (Tianjin) Corporation ("SMIC Tianjin"); Semiconductor Manufacturing International (BVI) Corporation ("SMIC BVI"); Semiconductor Manufacturing North China (Beijing) Corporation ("SMNC"); Semiconductor Manufacturing South China Corporation ("SMSC"); Semiconductor Manufacturing International (Shenzhen) Corporation; Broadcom Incorporated and Broadcom Corporation (because they are named defendants in the related litigation and customers of Petitioner); and Cypress Semiconductor Corporation (because it is a named defendant in the related litigation and customer of Petitioner).

B. Related Judicial and Administrative Matters (37 C.F.R. § 42.8(b)(2))

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner states that the '126 patent is currently the subject of the following lawsuit: *Innovative Foundry Technologies, LLC v. SMIC, et al*., No. 6:19-cv-00719-ADA (W.D. Texas), filed December 20, 2019.[1] Petitioner is also filing concurrently herewith a Petition for *Inter Partes* Review of U.S. Patent No. 6,933,620 (the "'620 patent"), which is a continuation of the '126 patent. In addition, Petitioner SMIC and SMIC Shanghai, SMIC Beijing, SMIC Tianjin, SMIC BVI, SMNC, and SMSC filed a complaint for a declaratory judgment of non-infringement for the '126 and '620 patents (among others) on April 2, 2020 in *SMIC, Americas et al. v. Innovative Foundry Technologies, LLC*, No. 3:20-cv-02256-JCS (N.D. Cal.).[2]

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)) and Service Information (37 C.F.R. § 42.8(b)(4))

In accordance with 37 C.F.R. § 42.8(b)(3), Petitioner provides the following designation of counsel. Concurrently filed is a Power of Attorney pursuant to 37 C.F.R. § 42.10(b). In accordance with 37 C.F.R. § 42.8(b)(4), Petitioner identifies the following service information:

[1] A copy of the Complaint is attached as Exhibit 1017.

[2] A copy of the Complaint is attached as Exhibit 1018.

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SMIC consents to electronic service.

III. GROUNDS FOR STANDING (37 C.F.R. § 42.104(a))

Pursuant to 37 C.F.R. § 42.104(a), SMIC certifies that the ’126 patent is available for IPR and that SMIC is not barred or estopped from requesting IPR challenging claims 1-19 of the ’126 patent on the grounds identified in this Petition.

IV. PAYMENT OF FEES (37 C.F.R. § 42.15(a) and § 42.103)

The required fees are submitted herewith in accordance with 37 C.F.R. §§ 42.103(a) and 42.15(a). If any additional fees are due during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 033975 (058559.0000002). Any overpayment or refund of fees may also be deposited into this Deposit Account.

V. BACKGROUND OF THE TECHNOLOGY

"Semiconductor device manufacturers are constantly improving device performance while lowering their cost of manufacture. One way manufacturers have reduced costs has been to shrink the sizes of the devices so that more devices can be made from a single semiconductor wafer." Ex. 1001 ('126 patent), 1:10-14. Reducing semiconductor device sizes generally results in improved performance and lower manufacturing costs. *Id.*, 1:25-28; Ex. 1005, ¶70.

However, there are adverse effects that come with shrinking device sizes. These adverse effects include effects referred to as "short channel" effects. Ex. 1001, 1:28-34; Ex. 1005, ¶71. Some examples of short-channel effects include (i) a decrease in source-drain breakdown voltage of the semiconductor device, and (ii) an increase in junction capacitance of the device. *Id.*, 1:16-21. Each of these effects can be harmful and degrade device performance, potentially resulting in instability of the device's threshold voltage. *See id.*; Ex. 1005, *id*.

One method of mitigating short-channel effects in semiconductor devices is to configure spacers along the sidewalls of the gate structures in these devices to form a graded junction between the drain and channel regions. *See* Ex. 1005, ¶72; Ex. 1003 (AMD 680), 3:48-4:7, 8:35-47 & Fig. 8. The spacers are used as masks for implanting or depositing different doping concentration profiles into different areas of the semiconductor substrate beneath the spacers in these devices. *Id*.

The different doping concentrations are spaced apart at different offsets from the gate structure to form a graded junction. *Id.* The different spaced offsets are delineated by the relative thicknesses of the spacers. *Id.* As a result, a graded junction is formed having higher doping concentration regions formed outside of lower concentration regions, relative to the channel region of the device. Ex. 1003, 4:65-5:1; Ex. 1005, *id.* A graded junction is used for the purpose of reducing short-channel effects in these devices. *Id.*, 4:55-60; Ex. 1005, *id*.

This technique of using spacers to form graded junctions in semiconductor devices was well-known and conventional in the field at the time of the ’126 patent. Ex. 1005, ¶73. For example, U.S. Patent No. 6,274,906 (“Samsung 906” – Ex. 1016) discloses a semiconductor manufacturing process using pairs of spacers formed along the sidewalls of the gate structure of a metal-oxide-semiconductor (“MOS”) transistor to form graded junctions in semiconductor devices in the same configuration as disclosed in the ’126 patent. *See* Ex. 1005, *id.*; Ex. 1016,

Abstract, 3:11-45 & Fig. 1:

FIG. 1

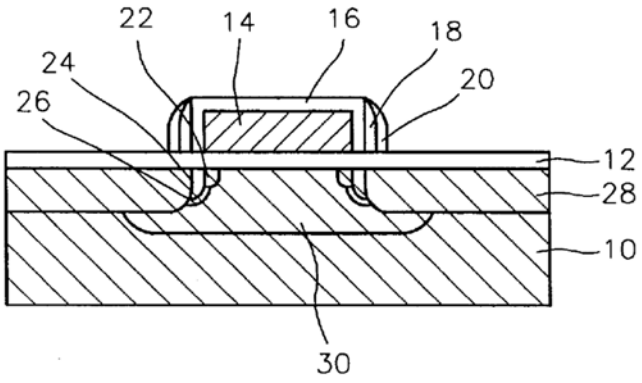


Fig. 1 above shows a first pair of spacers 18 formed around the gate electrode 14 in contact with the gate sidewalls and a second pair of spacers 20 in contact with the first pair of spacers 18. *See* Ex. 1005, ¶74; Ex. 1001, *id.* The spacers are used as masks for implanting different doping concentration profiles 22, 24 and 26 into different areas of the semiconductor substrate 10. *Id*. The doping concentrations 24 and 28 are aligned with spacers 18 and 20 respectively at different offsets from the gate structure to form a graded junction. *Id.* As a result, a graded junction is formed having higher doping concentration regions formed outside of lower concentrations regions relative to the channel region of the device. *Id.*

U.S. Patent No. 6,344,405 ("Phillips 405" – Ex. 1006) also discloses a method of manufacturing a semiconductor transistor device with a sequence of

oxide and/or nitride spacers disposed along the sidewalls of the device gate structure to form a graded junction with an optimized doping concentration profile. *See* Ex. 1005, ¶75; Ex. 1006, 1:8-18, 2:7-18, 53-58, 3:40-44, 8:30-37 & Fig. 9:

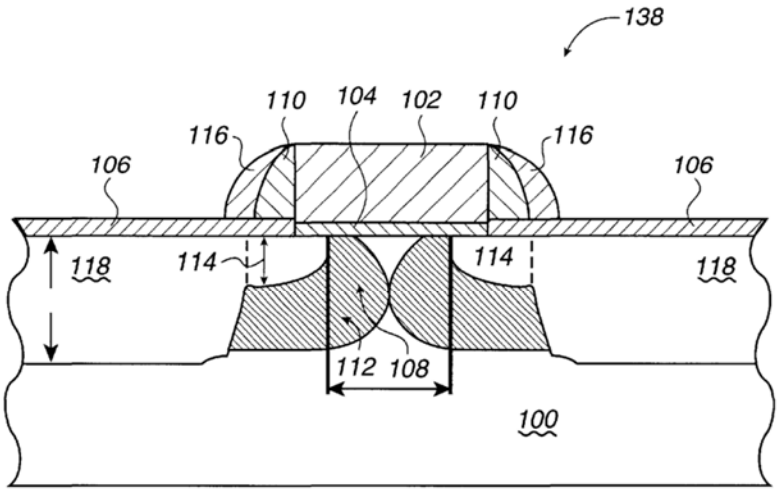


Fig. 9

This is done for the purpose of improving performance in devices with reduced device dimensions having shorter device gate lengths to minimize short-channel effects such as leakage currents, punch through, and excessive channel resistance. The transistor device shown in Fig. 9 above includes a sequence of pairs of offset spacers 110/116 formed along the sides of the gate structure 102. As stated in Phillips 405, the offset spacers may be formed using any number of techniques and are made of either oxide or silicon nitride. Ex. 1005, ¶76; Ex. 1006, 5:26-31, 6:57-67. The offset spacers 110/116 facilitate the formation of a graded junction comprising a shallow region having a higher doping concentration and a deep region having a lower doping concentration. *Id.*, 2:28-36, 5:36-39 &

8:54-63 (claim 1).

U.S. Patent No. 6,498,067 ("TSMC 067" – Ex. 1011) discloses a semiconductor manufacturing process for forming multi-layer nitride spacers on the sidewalls of a gate structure of a MOSFET[3] device to form graded junctions in the same configuration as disclosed in the '126 patent. *See* Ex. 1005, ¶77; Ex. 1011, Fig. 7:

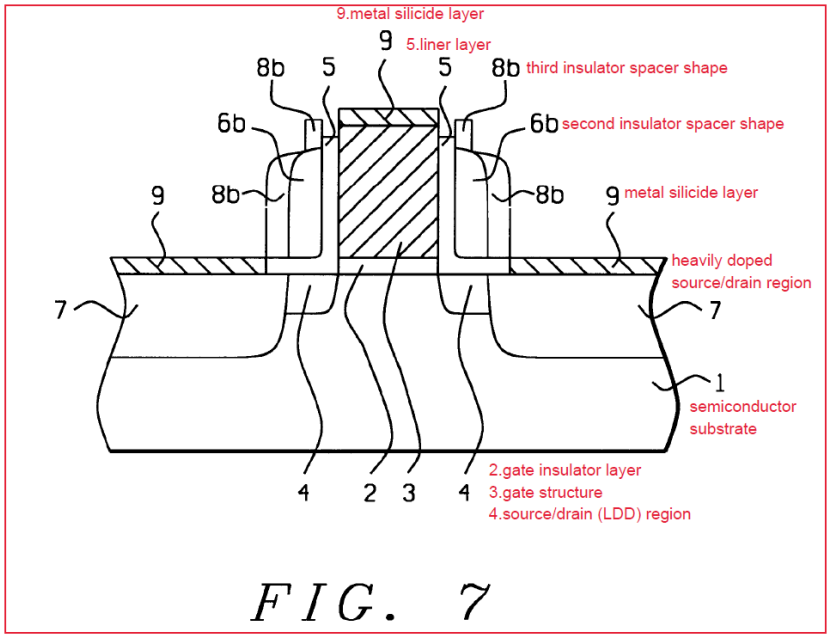


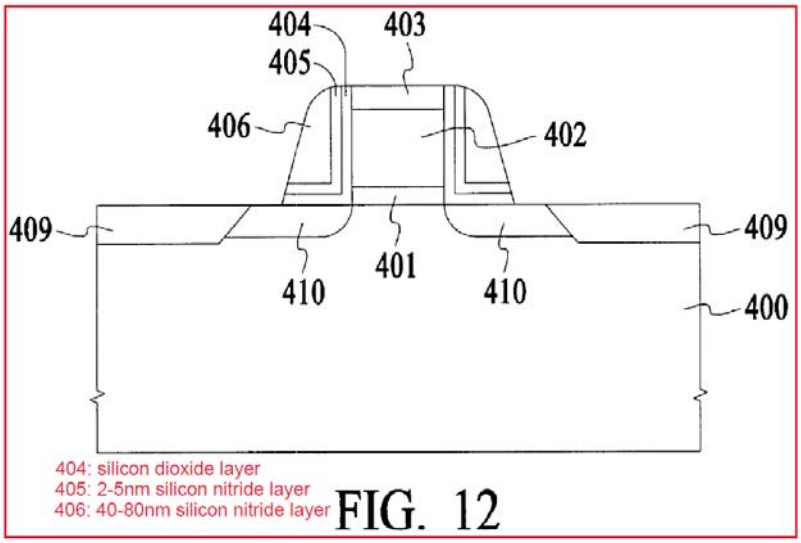
FIG. 7

Fig. 7 above shows a gate structure 3, oxide layers 5 formed on the gate sidewalls, a first pair of nitride spacers 6b in contact with the oxide layers, and a second pair of nitride spacers 8b in contact with the first pair of nitride spacers 6b. Ex. 1011, *id*. The spacers are used to form a graded junction comprised of lightly

[3] Metal-oxide-semiconductor field-effect transistor ("MOSFET")

doped source/drain (LDD) regions (4) adjacent to heavily doped source/drain regions (7). *See id.*, 3:43-50, 5:5-12 & Fig. 7; Ex. 1005, ¶78. The spacers also reduce the risk of gate leakage or short circuits that can occur during salicide formation. Ex. 1001, Abstract; Ex. 1005, *id*.

U.S. Patent No. 6,596,576 ("AMI 576" – Ex. 1012) also relates to a semiconductor manufacturing process for forming multi-layer nitride spacers on the sides of a MOSFET gate structure in a configuration very similar to the one disclosed in the '126 patent. *See* Ex. 1005, ¶79; Ex. 1012, Fig. 12:



As shown in Fig. 12 above, AMI 576 discloses a method of fabricating a semiconductor device with a gate structure 401-403, a pair of silicon dioxide liners 404 formed against the gate structure, a first pair of silicon nitride layers 405 in contact with the silicon dioxide liners 404, and a second pair of silicon nitride layers 406 in contact with the first silicon nitride layers 405. *See, e.g.*, Ex. 1012,

Abstract, 5:20-64 & Fig. 12; Ex. 1005, ¶80. In AMI 576, a barrier layer is formed over the oxide layer 404 before the silicon nitride spacers 405 and 406 are formed to reduce, or prevent altogether, diffusion of the hydrogen absorbed by the silicon nitride spacers into the gate oxide and channel during low temperature chemical vapor deposition of the silicon nitride. *Id.*

Further, U.S. Patent No. 6,225,176 ("AMD 176" – Ex. 1013) discloses a method of manufacturing a semiconductor device with multiple nitride spacers for reducing short-channel effects in the same manner as the '126 patent. *See* Ex. 1005, ¶81; Ex. 1013, Fig. 1:

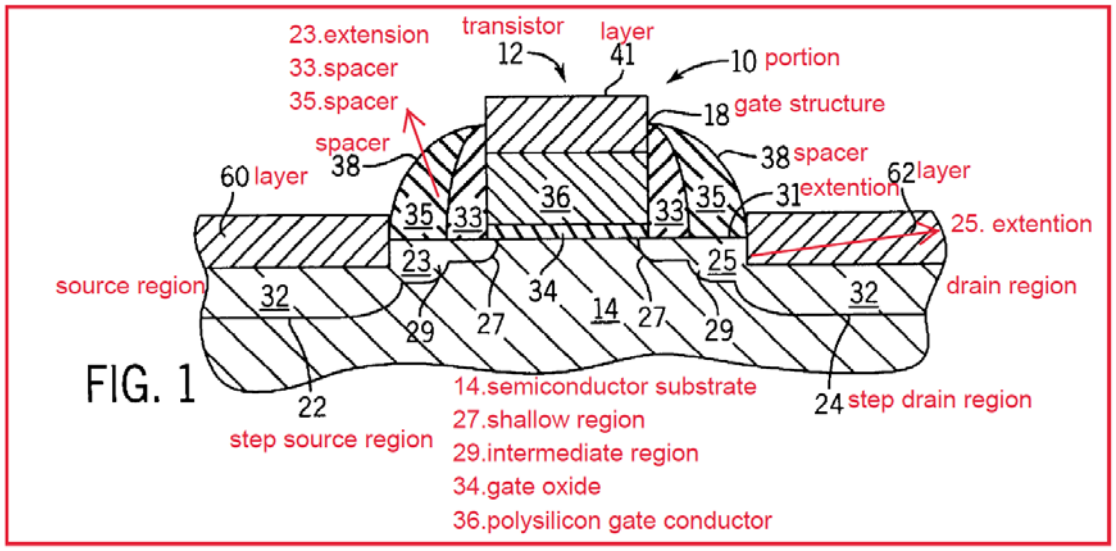


Fig. 1 above shows a semiconductor transistor device 12 having two pairs of nitride spacers 33/35 adjacent to a gate structure 36 and having source/drain doped regions (22, 23, 24, 25 and 27) of varying depths forming a graded junction. *See* Ex. 1001, 3:59-4:25 & Fig. 1; Ex. 1005, ¶82. The multiple nitride spacers are used

to form a graded junction for the purpose of reducing short-channel effects in the semiconductor transistor device. *Id*.

The adverse effects that come with shrinking semiconductor device sizes also include increased difficulty in forming silicide on the smaller gate structures in such devices which leads to increased gate resistance because gate resistance is dependent upon the amount of gate silicon surface area available for silicide formation. Ex. 1001, 1:28-34, 55-58; Ex. 1005, ¶83.

U.S. Patent No. 6,383,882 ("Samsung 882" – Ex. 1014) concerns a method of manufacturing a metal-oxide-semiconductor (MOS) semiconductor transistor device that includes nitride spacers that have been recessed to increase the exposed gate silicon surface area for silicide formation in the same manner as in the '126 patent. Ex. 1005, ¶84; Ex. 1014, Abstract & Fig. 11:

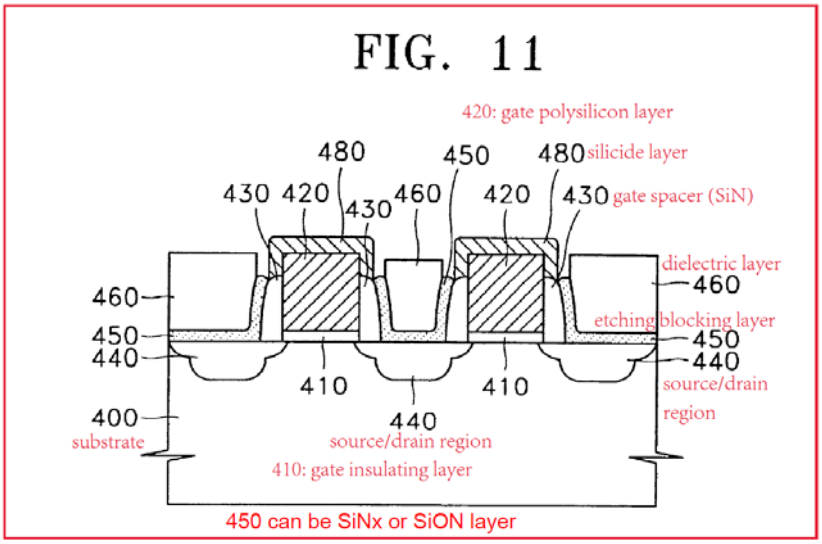


Fig. 11 above shows a MOS transistor device with two gate structures 420

having pairs of nitride spacers 430 that are recessed from the top surface of the gate structure to increase the silicon surface area for improved silicide formation 480. Ex. 1001, *id*.; Ex. 1005, ¶85.

U.S. Patent No. 6,291,354 ("UMC 354" – Ex. 1015) also concerns a method of manufacturing a semiconductor device with recessed nitride spacers to increase the exposed silicon surface area on the gate electrode for improved silicide formation. *See* Ex. 1005, ¶86; Ex. 1008, Figs. 4D & 4E:

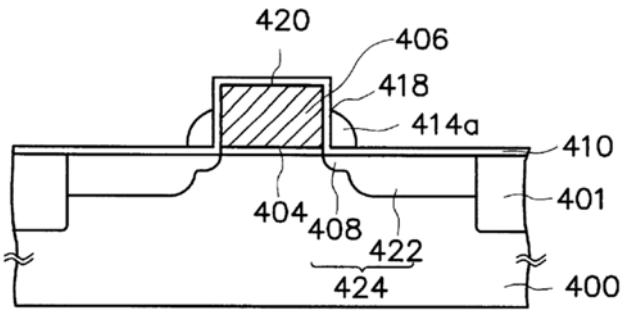


FIG. 4D

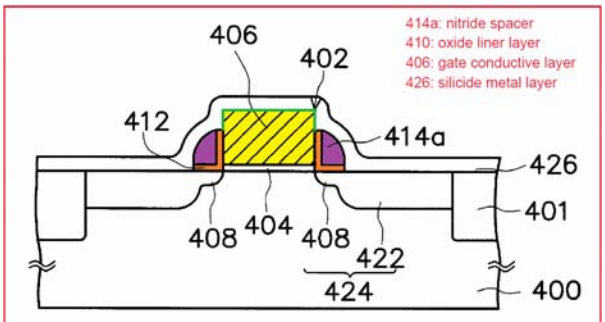


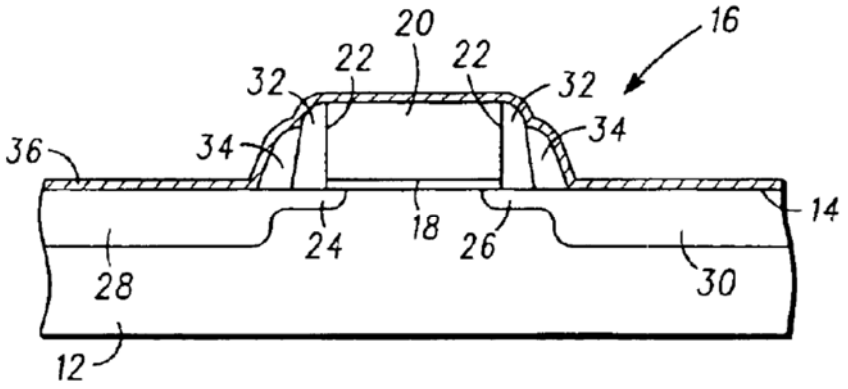
FIG. 4E

As shown in Figs. 4D and 4E above, a pair of nitride spacers 414a and oxide liner layers 410 are recessed from the top surface of the sidewalls of the gate structure 406, thereby exposing the upper portions of the sidewalls and increasing the gate silicon surface area for silicide formation 426. *See* Ex. 1008, *id*.; Ex. 1005, ¶87.

VI. THE '126 PATENT

The '126 patent relates to a known technique for reducing short-channel effects in semiconductor devices. Fig. 1 of the '126 patent below shows that a

prior art solution to these short-channel effects was to position pairs of spacers made of oxide and/or nitride adjacent to the gate structure of a semiconductor device. *See* Ex. 1005, ¶89; Ex. 1001, 1:33-48 & Fig. 1:



10
-Prior Art-
Fig. 1

As shown above, the semiconductor device 16 includes a gate 20, gate oxide 18, oxide spacers 32 adjacent to gate 20, nitride spacers 34 adjacent to oxide spacers 32, and graded source regions 24/28 and graded drain regions 26/30. Ex. 1001, *id*. A layer of refractory metal 36 is formed on gate structure 20, source region 28, and drain region 30. *Id.* Silicide forms on the exposed portions of the gate 20 and the source and drain regions 28/30 in contact with the metal layer 36. *See id.*, 1:55-60; Ex. 1005, ¶90.

Prior art solutions used graded junctions to soften the abruptness of the change in electric field between the drain and channel regions of semiconductor devices. *See, e.g.*, Ex. 1003, 3:6-7, 21-33, 5:1-9; Ex. 1005, ¶91. A graded junction introduces a more gradual change in the doping concentration profile in drain

regions 24/28 and source regions 26/30 that reduces the electric field near the drain side of the channel area. *Id*. A smoother doping profile produces a smoother voltage drop at the channel/drain junctions of the device, which reduces the electric field. *Id*. The graded junction arrangement acts to minimize the peak drain-to-channel electric field, and thus mitigates short-channel effects. *See* Ex. 1001, 1:21-24 & Fig. 1; Ex. 1005, *id*.

Referring back to Fig. 1 above, the spacers 32/34 are used as masks in forming the graded junction to isolate the different regions of the device so that different doping concentration profiles can be implanted or deposited beneath the spacers at different offsets a spaced distance apart from the gate sidewalls. *Id*., 1:41-48 & Fig. 1; Ex. 1005, ¶92.

The spaced distances of the offsets are delineated by the thickness of each of the pairs of spacers. Ex. 1001, *id.;* Ex. 1005, ¶93. This technique results in the structure shown in Fig. 1 of the ’126 patent, wherein the source/drain regions 24/26 aligned with oxide spacers 32 have a lower doping concentration profile than the source/drain regions 28/30 aligned with the nitride spacers 34. *Id*.

The other problem the ’126 patent purports to address is the one that arises with the reduced silicon surface area on gate structures in semiconductor devices that results from shrinking device sizes. *See id.*, 1:27-33; Ex. 1005, ¶94. The ’126 patent purports to focus specifically on lowering gate resistance in semiconductor

devices that have reduced gate widths. *See* Ex. 1001, 1:59-63; Ex. 1005, *id*. Any decrease in device gate width results in less surface area of exposed silicon, which makes it more difficult to form silicide on the gate structure. *Id*., 1:27-33, 1:55-58, Ex. 1005, *id*. Silicide formation is important because it facilitates conduction of charge carriers across the gate, which lowers gate resistance and improves device performance. *Id*.

According to the '126 patent, this problem is compounded in semiconductor devices that use spacers for creating graded junctions because the spacers obstruct silicide formation on the gate sidewalls, which further reduces the exposed gate silicon surface area available for silicide formation. In such cases, the silicide can only form on the top of the gate structure, increasing gate resistance in such devices. Ex. 1001, 1:53-58; Ex. 1005, ¶95.

The '126 patent concerns a method of manufacturing semiconductor devices that purports to solve this problem by recessing the spacers to reduce their obstruction of the gate sidewalls. This increases the area of exposed gate silicon available for silicide formation. Ex. 1005, ¶96; Ex. 1001, 2:62-65, 4:58-60, Fig. 7:

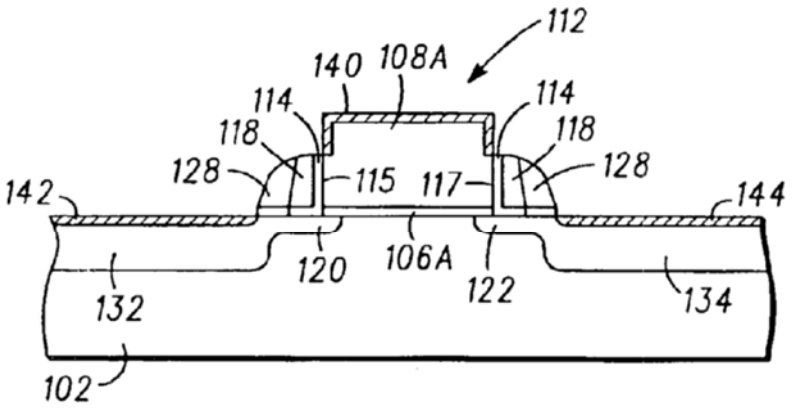


Fig. 7

The ’126 patent uses spacers made of the same material so they can be recessed together with a single over-etch step. Ex. 1005, ¶97; Ex. 1001, 4:65-5:2.

In Fig. 7, spacers 118/128 are disposed adjacent to gate 108A and are recessed to expose the silicon gate material on the upper portion of sidewalls 115 and 117. *Id.* Silicide can then be formed thereon to reduce the overall gate resistance. *Id.*, 2:33-38; Ex. 1005, ¶98.

VII. PROSECUTION HISTORY OF THE ’126 PATENT

The ’126 patent issued from U.S. Patent Application No. 10/236,200 (“the ’200 application”) filed on September 6, 2002. Ex. 1001. The earliest effective filing date for the ’126 patent is September 6, 2002, which Petitioner uses for this Petition only, while reserving the right to contest this claim to priority in the related litigation. The application as filed included originally-filed claims 1-25. A copy of the prosecution history of the ’126 patent is attached to this Petition as Exhibit 1002.

On February 5, 2003, the applicant filed an information disclosure statement and on February 2, 2004 the applicant filed a supplemental information disclosure statement. *See* Ex. 1002 ('126 Pat. Pros. History), Information Discl. Stmts. dated 2/5/03 & 2/2/04. None of the prior art presented in this Petition—U.S. Patent Nos. 6,258,680 ("AMD 680") and 6,235,598 ("Intel 598")—were cited in these information disclosure statements.

A restriction requirement under 35 U.S.C. § 121 issued on February 6, 2004 that restricted the claims into group 1 (claims 20-25) drawn to a semiconductor device and group 2 (claims 1-19) drawn to a process of making a semiconductor device. *See id.*, Rest. Req. dated 2/6/04. On February 17, 2004 the applicant filed a response to the restriction requirement electing group 2 (claims 1-19) and withdrawing Group 1 (claims 20-25) from consideration without prejudice.

A first Office Action on the merits issued on March 10, 2004 rejecting claims 1-19 under 35 U.S.C. § 103 over the "Background of the Invention" section of the application in view of U.S. Patent No. 6,194,279 to Chen et al. ("Chen"). *See id.*, Office Action dated 03/10/04. In the Office Action, the Examiner asserted that the Background of the Invention disclosed all the limitations of claim 1 except for the limitation concerning the third and fourth spacers exposing portions of the first and second sidewalls of the gate structure and disclosed all of the limitations of claim 12 except the first nitride spacer. For those limitations, the Office Action

cited to sections of Chen. *Id.*, 4-5. The Office Action also objected to the drawings as lacking a prior art designation for Fig. 1. *Id.*, at 2.

The applicant filed an Amendment on April 29, 2004 in which the claims were narrowed to their present scope in the issued patent and traversed the rejections in light of the amendments. The applicant also added a new claim set 26-31 directed to the embodiment wherein the pairs of nitride spacers were in direct contact with one another.

A Notice of Allowance issued on May 13, 2004 in which all pending claims 1-19 and 26-31were allowed. *See id.*, Notice of Allowance dated 5/13/04. In the Notice of Allowance, the Examiner stated his reasons for allowance as follows:

> None of the references of record teaches or suggests the claimed Semiconductor Component and Method of Manufacture having third and fourth spacers adjacent the first and second spacers, respectively, the third and fourth spacers comprising the first dielectric material; exposing portions of the first and second sides of the gate structure.

See id., 2.

Formal drawings were submitted August 3, 2004 and the ’126 patent issued on October 18, 2004.

A request for a certificate of correction was later submitted on September 6, 2005 to change the word “suicide” to “silicide” in issued dependent claim 11.

The prior art presented in this Petition—AMD 680 and Intel 598—were not cited or discussed during prosecution of the ’126 patent.

VIII. CLAIM CONSTRUCTION

The claim construction standard used for claims subject to IPR is the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) and its progeny, which is the same standard used to construe claims in civil actions in federal district court. 37 C.F.R. § 42.100(b). Petitioner contends that, unless otherwise specifically noted herein, the terms and phrases recited in the claims of the ’126 patent are accorded their ordinary and customary meaning that they would have to one of ordinary skill in the art at the time of the invention.

Petitioner’s interpretation of the claim terms in the ’126 patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below. Under the *Phillips* standard and for clarity, Petitioner provides the following proposed claim construction believed to be relevant to this Petition.[4]

A. “silicide” means “silicide, salicide and/or polysilicide”

Dependent claims 10 and 11 recite the claim term “silicide.” A person of ordinary skill in the art (“POSA”) would understand the term “silicide” in the context of the ’126 patent to refer to “silicide, salicide and/or polysilicide.”

[4] Petitioner does not concede that the challenged claims are valid under 35 U.S.C. § 112.

Silicides can be self-aligning or non-self-aligning. Ex. 1005, ¶107. If a silicide is self-aligning, it may be called "salicide." *Id*. "Salicide" is a compaction of the phrase "self-aligned silicide." *Id*. Self-aligned means that the electrical contacts can be formed on the semiconductor component without requiring a photolithography patterning process, as opposed to a non-aligned technology such as "polycide" (also referred to as "polysilicide"). *Id*. The term refers to microelectronics technology used to form electrical contacts between semiconductor components and their metal interconnections. The silicide process involves a reaction of a metal thin film with silicon material, forming a metal silicide contact through a series of annealing (i.e., heating at high temperatures) and/or etch processes. *See* Ex. 1001, 5:43-48, 57-59; Ex. 1005, *id*.

IX. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED

A. Claims for Which Review is Requested

SMIC requests IPR under 35 U.S.C. § 311 of claims 1-19 of the '126 patent and cancellation of those claims as unpatentable.

B. Statutory Grounds of Challenge

SMIC requests IPR of claims 1-19 of the '126 patent in view of the following references, each of which is prior art to the '126 patent under 35 U.S.C. § 102(b):

Ground	Proposed Rejections for the ’126 patent	Exhibit Number(s)
1	Claims 1-19 would have been obvious under 35 U.S.C. §103 over AMD 680 (Ex. 1003) in view of Intel 598 (Ex. 1004) and the knowledge of one of ordinary skill in the art.	**1003, 1004**
2	Claims 1-2, 4-8, 12, 14, 16-17 and 19 of the ’126 patent are anticipated by AMD 680 (Ex. 1003) under 35 U.S.C. §102(b).	**1003**

C. Level of Ordinary Skill in the Art

A POSA concerning the ’126 patent would have had an undergraduate degree in electrical engineering or related field with two to four years of experience in semiconductor process technology, or a master’s degree with one or more years of experience in the field, or equivalent combination of education and experience. Ex. 1005, ¶69.

D. Overview of the Challenge of the Patentability of Claims 1-19

As set forth above, using spacers to form graded junctions for the purpose of reducing short-channel effects in semiconductor devices was not new at the time of the ’126 patent; nor was recessing the spacers for the purpose of increasing the amount of exposed silicon surface area on the gate sidewalls to improve silicide formation for the purpose of reducing gate resistance.

Prior art that was not considered by the Examiner during prosecution discloses the very same claimed configuration of nitride spacers used for reducing short-channel effects and gate resistance in semiconductor devices.

X. GROUND 1: CLAIMS 1-19 ARE OBVIOUS OVER AMD 680 IN VIEW OF INTEL 598 AND THE KNOWLEDGE OF ONE OF ORDINARY SKILL IN THE ART

Obviousness is a question of law based upon several factual inquires; namely, the scope and content of the prior art, the differences between the prior art and the claimed invention, the level of ordinary skill in the art, and secondary considerations of nonobviousness. *Graham v. John Deere Co*., 383 U.S. 1, 17-18 (1966); *see also Al-Site Corp. v. VSI Int'l Inc*., 174 F.3d 1308 (Fed. Cir. 1999). To prove obviousness, a challenger must show "prior art references which alone or combined with other references would have rendered the invention obvious to one of ordinary skill in the art at the time of invention." *Al-Site Corp.*, 174 F.3d at 1323. The combined references must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991), *see also In re Royka*, 490 F.2d 981 (C.C.P.A. 1974).

The U.S. Supreme Court decision in *KSR International Co. v. Teleflex Inc., et al*., 127 S.Ct. 1727 at 1739 (2007) ("*KSR*") held that a claimed invention can be obvious even if there is no teaching, suggestion, or motivation for combining the prior art to produce that invention. *KSR* holds that patents that are based on combinations of elements or components already known in a technical field may be found to be obvious. In *KSR*, the Supreme Court emphasized the principle that "[t]he combination of familiar elements according to known methods is likely to be

obvious when it does no more than yield predictable results." *Id*., 1739. A key inquiry is whether the "improvement is more than the predictable use of prior art elements according to their established functions." *Id.*, 1740.

Using this legal framework established by the Supreme Court in both *Graham v. Deere* and *KSR*, Petitioner submits that the challenged claims 1-19 represent nothing more than a known prior art technique of using spacers to reduce short-channel effects in semiconductor devices.

A. The Scope And Content Of The Prior Art

1. AMD 680 (Ex. 1003)

U.S. Patent No. 6,258,680 ("AMD 680") qualifies as prior art to the '126 patent under 35 U.S.C. § 102(b). Ex. 1003. AMD 680 discloses a method of manufacturing a semiconductor device comprised of a sequence of interposed pairs of oxide and nitride spacers formed on either side of the sidewalls of the gate structure that were used to form a graded junction with a relatively smooth doping concentration profile. *See* Ex. 1003, at 4:56-5:9, 9:48-53; Ex. 1005, at ¶109. The purpose of smoothing the doping profile is to minimize the abruptness of the voltage change at the junction, thus reducing the electric field at the junction. *Id.*, 3:6-7, 21-33. This, in turn, reduces the short-channel effects in the device. *Id.*, 5:1-9, 25-28; 9:53-55. Dispersing abrupt voltage changes reduces the strength of the electric field and the associated harmful short-channel effects. *See id*., 3:23-23,

9:56-59; Ex. 1005, *id*.

In AMD 680, nitride spacers are used as a mask for an ion implantation doping process to produce devices with a graded junction profile. *See id.*, 9:20-33, 48-53. As depicted below in Fig. 12, the device includes a thermal oxide liner 128, nitride spacers 136/138 and 160/162 formed on either side of gate 114, and oxide spacers 148/150 interposed among the nitride spacers. Ex. 1005, ¶110; Ex. 1003, 5:42-45 & Fig. 12:

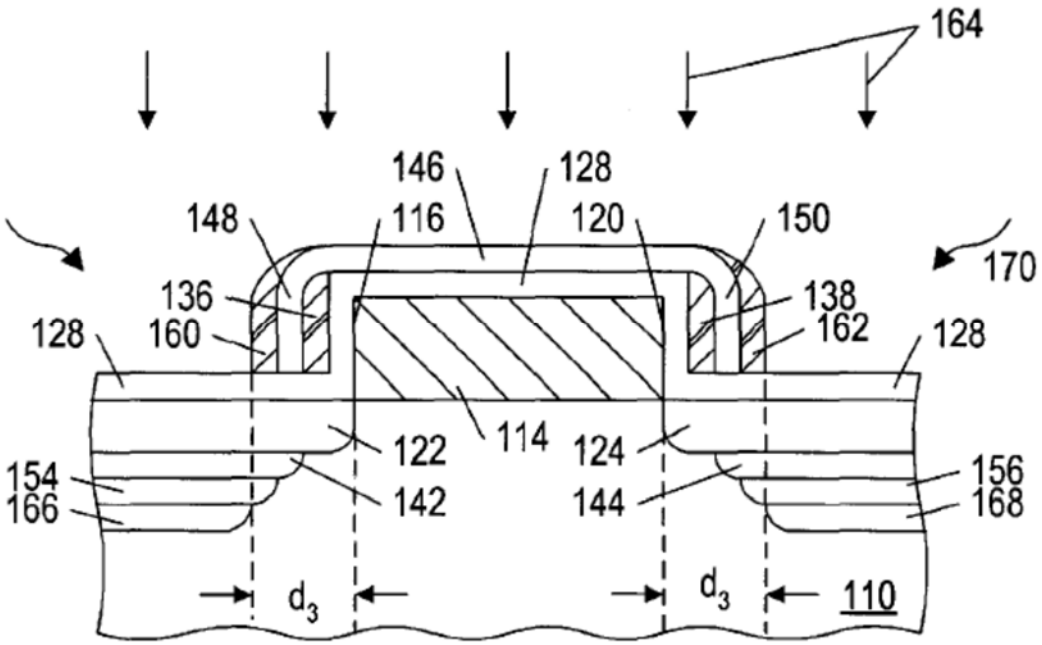


FIG. 12

Dielectrics of dissimilar etch characteristics are interposed among the nitride spacers which allows the pairs of spacers to be individually removed using a selective etch process. *Id.*, 5:57-65, 6:1-4, 8:19-22; Ex. 1005, at ¶111.

The source/drain regions are doped with n-type or p-type doping agents. *Id.*, 1:36-37; Ex. 1005, ¶112. Doping agents of different concentration profiles are

implanted into the source/drain regions of the semiconductor substrate 110 at different spaced distances offset from the gate sidewalls 116/120 in accordance with the relative thicknesses of the nitride spacers. *Id.*, at Abstract, 5:47-50; 6:4-9. As a result, a graded junction is formed having higher doping concentration regions formed outside of lighter doping concentration regions to form a graded junction for the purpose of reducing short-channel effects in the semiconductor component. *Id.*, Abstract, 4:65-6:1; Ex. 1005, *id*.

Fig. 12 depicted above shows the ion implanted doping concentration profiles 142/144 and 166/168 aligned with the nitride spacers 136/138 and 160/162, respectively.

2. Intel 598 (Ex. 1004)

U.S. Patent No. 6,235,598 ("Intel 598") qualifies as prior art to the '126 patent under 35 U.S.C. § 102(b). Ex. 1004. Intel 598 discloses a method of manufacturing semiconductor devices for improved polycide resistance on gate electrodes. *Id.*, 1:6-11. Like the '126 patent, the solution in Intel 598 concerns lowering the increased gate resistance in devices that comes with inadequate silicide formation on gate structures with smaller gate widths. *See* Ex. 1004, 1:44-52, 2:21-23; Ex. 1005, at ¶114. Inadequate formation of a gate silicide layer is attributed to the reduced reaction area for the conductive layer to form on which leads to increased gate resistance. *Id.*, 2:21-30. "This is detrimental to the

efficiency of the semiconductor device, as higher resistance decreases the speed of the semiconductor circuitry." *Id*., 1:52-54. The smaller gate structural dimensions lead to a reduction in the available nucleation sites on which the conductive layer can form. *See id.*, 2:21-30; Ex. 1005, *id*.

To solve this problem, Intel 598 discloses a method of manufacturing semiconductor devices with a gate structure like the ones taught in the '126 patent and AMD 680—namely, gate structures comprised of pairs of interposed oxide and nitride spacers formed on either side of the gate sidewalls. *See* Ex. 1005, ¶115; Ex. 1003, Fig. 6m & 6e:

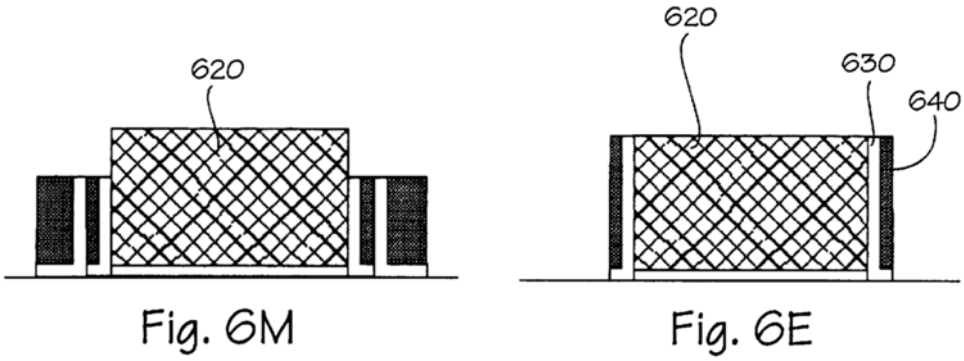


Fig. 6M Fig. 6E

The spacers 640 are positioned on either side of the gate structure 126 to prevent transfer of electric current between the gate 126 and surrounding structures in the semiconductor substrate 600. Ex. 1005, ¶116, Ex. 1003, 1:37-40 & Fig. 6a, 6e:

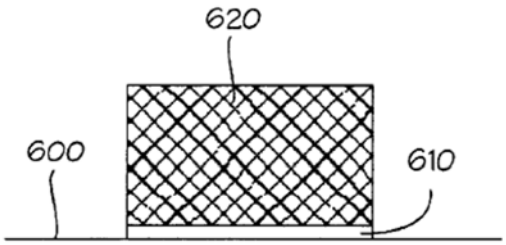


Fig. 6A

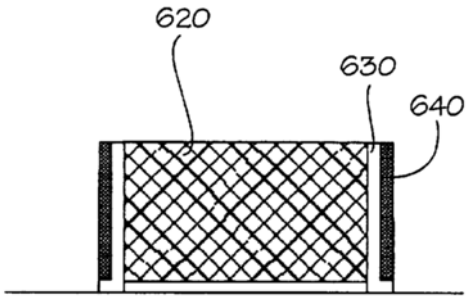


Fig. 6E

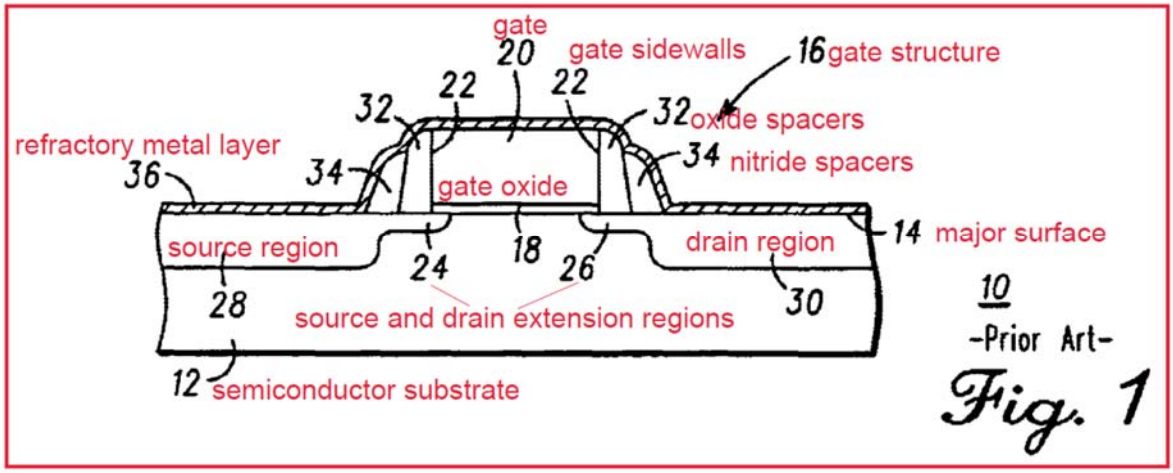
As shown, a thin first spacer layer 630 is deposited on gate layer 126 and substrate 600. The thin first spacer layer 630 can be an oxide layer (hereinafter "oxide layer 630"). *Id.* In one embodiment, Intel 598 discloses that the thickness of the oxide layer 630 is approximately 50-150 Angstroms (Å). *Id.*, 8:21-29. The oxide layer 630 is deposited using deposition techniques that were well known in the art at the time. Ex. 1004, *id.*; Ex. 1005, at ¶117.

Like in the '126 patent, Intel 598 discloses using an etch process to recess the spacers to expose the upper portions of the gate sidewalls which forms a larger reaction surface area for the silicide to form on. *Id.*, at 9:39-54 & Fig. 6m (above). In Intel 598, an anisotropic etching process is used to remove the nitride spacers, but not the oxide (*see id.*, 9:40-43), and an isotropic etching process is used to remove the oxide spacers, but not the nitride (*see, id.*, 8:45-49). Ex. 1005, at ¶118.

3. Knowledge Of One Of Ordinary Skill In The Art

The knowledge of a POSA is deemed to at least include any admitted prior art disclosed in a patent's "Background of the Invention" section. Thus, in terms

of the ’126 patent, the knowledge of a POSA includes the semiconductor device shown in Fig. 1 below. *See* Ex. 1005, at ¶119; Ex. 1001, 1:33-53 & Fig. 1:



In addition, the knowledge of a POSA would have also included known techniques for forming a dielectric material of a specified thickness. Indeed, the ’126 patent acknowledges that forming a dielectric material such as oxide with a thickness ranging from 10 to 100 Å could be carried out using techniques known to those skilled in the art at the time. *See* Ex. 1005, ¶120; Ex. 1001, 3:22-35.

Further, the knowledge of a POSA would have included techniques for thermally growing oxide layers on silicon in a dry oxygen ambient at temperatures ranging from 700ºC to 1300ºC, including between approximately 750ºC and 900ºC. *See* B.E. Deal & A. S. Grove, *General Relationship for the Thermal Oxidation of Silicon*, Abstract, Journal of Applied Physics; vol. 36, no. 12 (Dec. 1965) (Ex. 1009).

Thus, forming a dielectric layer with a thickness less than 100 Å would have been an obvious design choice that was within the knowledge of a POSA at the time. *See* Ex. 1004, 8:21-29; Ex. 1005, ¶121.

B. Potential Differences Between The Prior Art And The Challenged Claims

AMD 680 discloses a semiconductor component comprised of a gate structure that has an oxide layer 128 formed on the gate sidewalls, but AMD 680 does not explicitly specify any particular thickness for the oxide layer. *See* Ex. 1003, 8:13-17 & Fig. 6 (oxide layer 128). Claims 1, 2 and 13 of the '126 patent expressly recite an oxide layer having a thickness in a range of less than 100 Å.

Further, AMD 680 does not explicitly disclose recessing the spacers to expose more gate silicon surface area for silicide formation. Claims 4, 10 and 15 of the '126 patent expressly recite limitations relating to this feature.

As noted above, techniques for forming dielectric layers (e.g., oxide layers) of a specified thickness were well-known in the art. Therefore, specifying an oxide layer with a thickness in the range of less than 100 Å would have been an obvious design choice for a POSA. And regardless, Intel 598 discloses using a selective etch process for recessing oxide/nitride spacers to expose more gate silicon surface area for silicide formation in the same manner as in the '126 patent. *See*, *e.g.*, Ex. 1004, 9:39-55 & Fig. 6m & 6e:

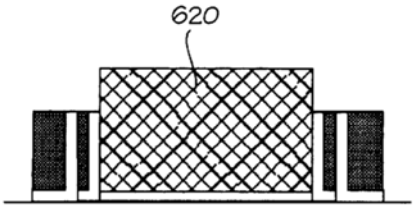


Fig. 6M

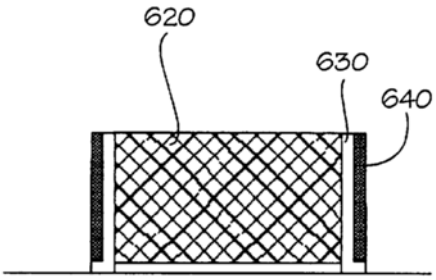


Fig. 6E

In addition, Intel 598 explicitly discloses forming the thin oxide layer 630 with a thickness in a range of less than 100 Å. *See* Ex. 1004, 8:21-29.

A POSA would have had both of the prior art techniques disclosed in AMD 680 and Intel 598 at his or her fingertips for use in designing gate structures for semiconductor devices with small gate widths. A POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with more exposed gate silicon surface area for silicide formation to improve gate resistance (Intel 598) and with spacers used for forming a graded junction to reduce short-channel effects (AMD 680). Ex. 1005, ¶¶122, 128.

Thus, the potential difference between AMD 680 and the challenged claims is expressly disclosed by Intel 598, and a POSA would have clearly been motivated to combine AMD 680 with Intel 598. Ex. 1005, *id*.

C. The Level Of Skill In The Art

Petitioner provides the level of ordinary skill in the art, in Section IX. C. above.

D. There Would Have Been A Motivation To Combine AMD 680 With Intel 598

The rationale to combine or modify prior art references is significantly stronger when the references seek to solve the same problem, come from the same field, and correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). It would have been obvious to a POSA to have combined the teachings of AMD 680 with those of Intel 598. Ex. 1005, *id*. AMD 680 and Intel 598 both concern the same field of semiconductor processing, solve similar problems resulting from shrinking gate widths in semiconductor devices, and their respective teachings correspond remarkably well. *Id*.

Both AMD 680 and Intel 598 concern forming silicide on gate structures. For example, Fig. 17 of AMD 680 depicts silicide layers 198, 200 and 202 formed on the top of gate structure 114. *See* Ex. 1005, ¶124; Ex. 1003, 11:56-63, Fig. 17:

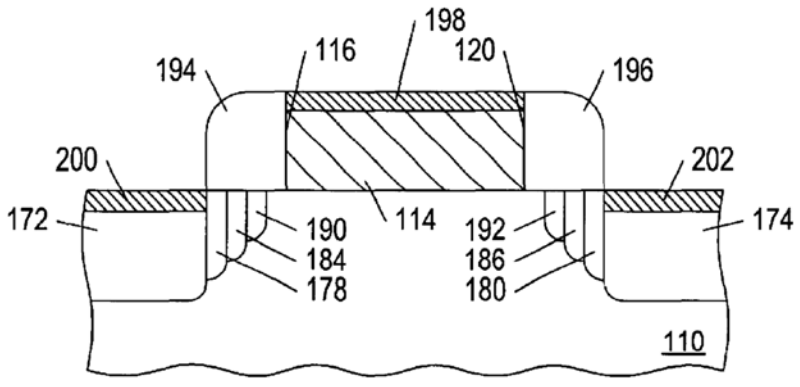


FIG. 17

Intel 598 discloses using an etch process for selectively recessing the thin oxide layer 630 and nitride spacers 640 to expose more gate silicon surface area on

the upper portions of the gate structure 126 for silicide to form on. Ex. 1005, ¶125; Ex. 1004, 9:39-63 & Fig. 6n:

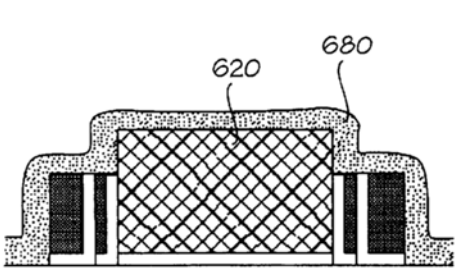


Fig. 6N

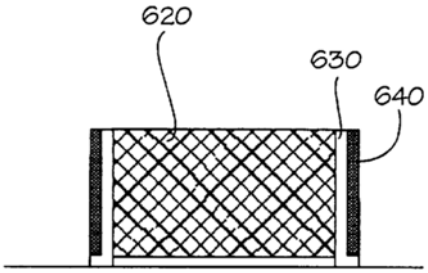


Fig. 6E

Nitride spacers 640 are recessed to expose more of the upper portions of the sidewalls of gate structure 620 for the reactant layer 680 to form on. This produces more silicide formation on the gate structure 620. *See* Ex. 1005, ¶126; Ex. 1004, 9:39-63 & Fig. 6m:

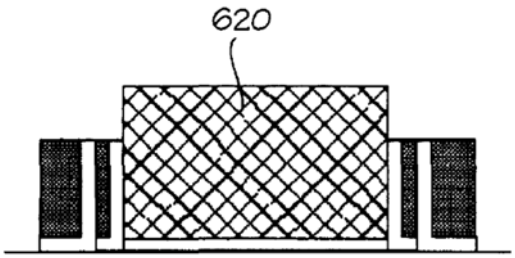


Fig. 6M

AMD 680 and Intel 598 are fully compatible, as there is nothing taught in AMD 680 that would exclude using Intel 598's method of recessing spacers for increased gate silicon surface area for silicide to form on. Ex, 1005, ¶127. The spacers disclosed in AMD 680 could be recessed in the same manner disclosed in Intel 598 at any point in the fabrication process without effecting the principle of

operation of the method. *Id*. Likewise, there is nothing disclosed in Intel 598 that would exclude using AMD 680's method of using oxide/nitride spacers for forming graded junctions in the source/drain regions of the device to reduce short-channel effects. *Id*. The spacers disclosed in Intel 598 could have also been used as masks for selective doping of different regions in the semiconductor device at various offsets from the gate structure to form a graded junction in the same manner as disclosed in AMD 680. *Id*.

Thus, a POSA would have had both of these prior art techniques readily available for use in designing gate structures for semiconductor devices having reduced device sizes with smaller gate widths. Ex. 1005, ¶128. A POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with more exposed gate silicon surface area for silicide formation to improve gate resistance (Intel 598) and with oxide/nitride spacers for forming a graded junction to reduce short-channel effects (AMD 680). *Id*.

As explained in more detail below, there is no difference between the scope and content of this combined prior art and the subject matter of the challenged claims. Thus, the combination of AMD 680 and Intel 598 render the challenged claims obvious. Ex. 1005, ¶129.

E. Independent Claim 1

The combined teachings of AMD 680 and Intel 598 disclose each and every

limitation recited in independent claim 1 of the ’126 patent. To begin with, AMD 680 discloses a “method for manufacturing a semiconductor component,” as recited in the preamble of independent claim 1. *See* Ex. 1003, 1:11-14 (“This invention relates to semiconductor processing and, more particularly, to a method of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects.”). Intel 598 also discloses a semiconductor component. Intel 598 also discloses a method for manufacturing a semiconductor component. *See* Ex. 1004, 1:6-9 (“The present invention relates to the field of semiconductor devices. More particularly, the present invention relates to a method and device for improved resistance on gate electrodes.”). *See* Ex. 1005, ¶130.[5]

AMD 680 discloses limitation 1(a): “providing a semiconductor material of a first conductivity type having a major surface.” For example, the semiconductor component disclosed in Fig 6 of AMD 680 included a semiconductor substrate 110 comprising n-type or p-type doped silicon material of a first conductivity type and

[5] Petitioner’s position in this Petition regarding the ordering of the steps in the challenged method claims of the ’126 Patent is based on Patent Owner’s apparent construction in the related district court litigation that the claimed methods need not be performed in the order listed.

having a major surface, at least at the intersection of substrate 110 and oxide layer 128. Ex. 1005, ¶131; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

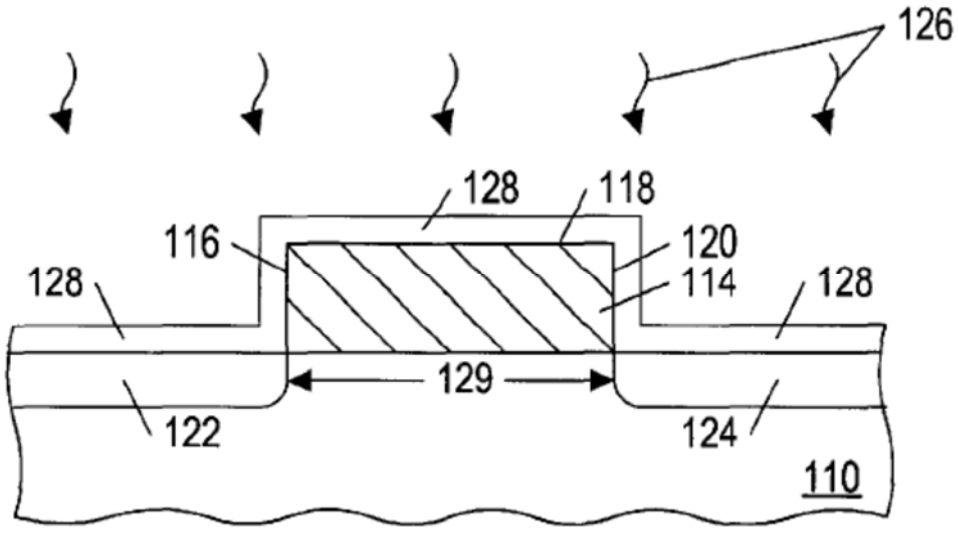
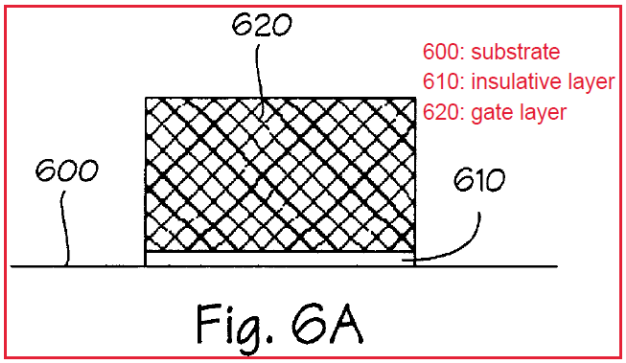


FIG. 6

AMD 680 discloses limitation 1(b): "forming a gate structure on the major surface, the gate structure having first and second sides and a top surface." For example, the semiconductor component disclosed in Fig 6 includes a gate structure 114 disposed on substrate 110, the gate structure 114 having a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1003 7:63-67 & Fig. 6; Ex. 1005, ¶132.

Intel 598 also discloses this limitation. For example, Fig. 6a below discloses a gate structure 126 on a substrate 600 with a top surface and sidewalls. *See* Ex. 1005, ¶133; Ex. 1004, 8:15-20 & Fig. 6a:



AMD 680 discloses limitation 1(c): "forming first and second spacers adjacent the first and second sides of the gate structure, respectively, the first and second spacers comprising a first dielectric material."[6] As shown in Fig. 7 below, AMD 680 discloses a semiconductor component with a first nitride spacer 136 formed adjacent to gate sidewall 116 and a second nitride spacer 138 formed adjacent to gate sidewall 120. The first and second nitride spacers comprise a first dielectric material. *See* Ex. 1005, ¶134; Ex. 1003, 8:23-35 & Fig. 7:

[6] Petitioner's position in this Petition with respect to the "adjacent" claim term is based on Patent Owner's apparent construction of that term in the related district court litigation.

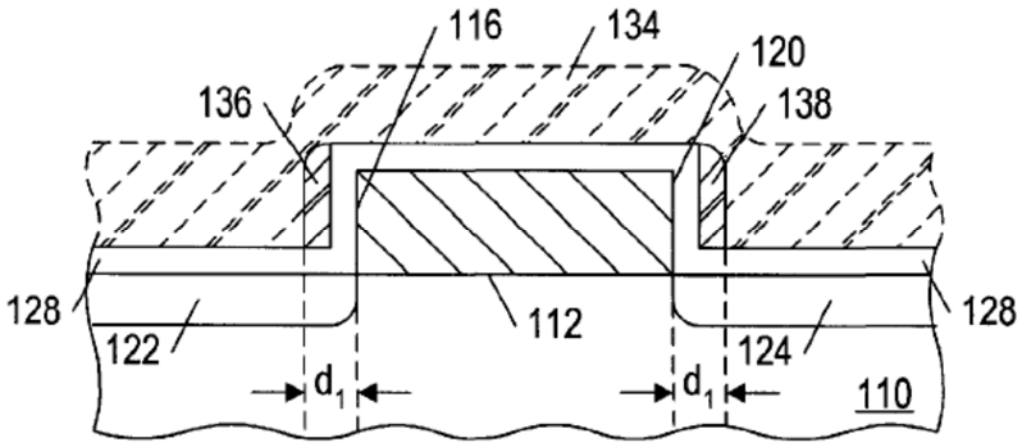


FIG. 7

Intel 598 also discloses this limitation. *See, e.g.*, Ex. 1005, ¶135; Ex. 1004, 8:30-32, 61-64 & Figs. 6c, 6g:

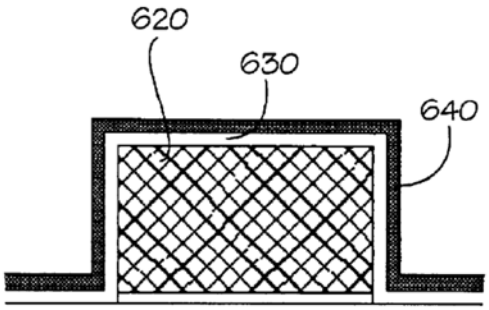


Fig. 6C

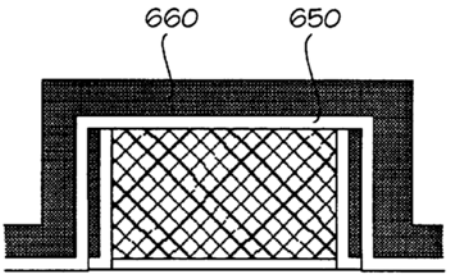


Fig. 6G

The figures above show a semiconductor component with first and second nitride spacers 640 formed adjacent to the sidewalls of gate structure 620. Ex. 1005, ¶136.

AMD 680 discloses 1(d): "forming source and drain extension regions in the semiconductor material, the source extension region aligned to the first spacer and the drain extension region aligned to the second spacer." *See* Ex. 1005, ¶137; Ex. 1003, 8:35-47 & Fig. 8:

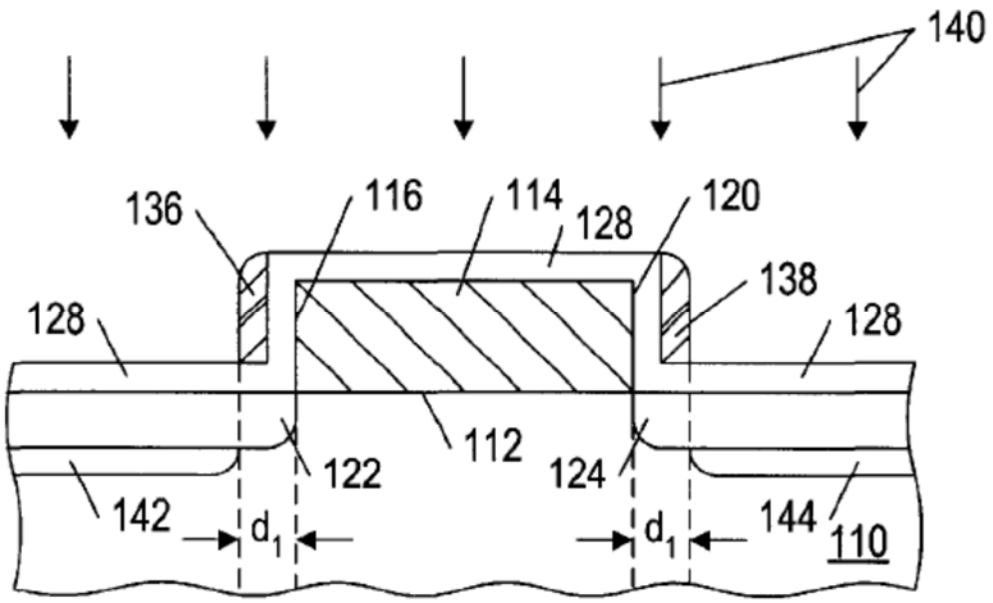


FIG. 8

Fig. 8 above shows a semiconductor component includes a source/drain extension region 142 aligned to the first nitride spacer 136 and a source/drain extension region 144 aligned to the second nitride spacer 138.

AMD 680 discloses 1(e): "forming third and fourth spacers adjacent the first and second spacers, respectively, the third and fourth spacers comprising the first dielectric material." For example, Fig. 11 below shows a third nitride spacer 160 (which is a dielectric material) that is formed on one side of the first nitride spacer 136 and a fourth nitride spacer 162 (dielectric material) that is formed on the other side of the second nitride spacer 138. The third and fourth spacers 160/162 comprise a first dielectric material. *See* Ex. 1005, ¶139; Ex. 1003, 9:4-14 & Fig. 11:

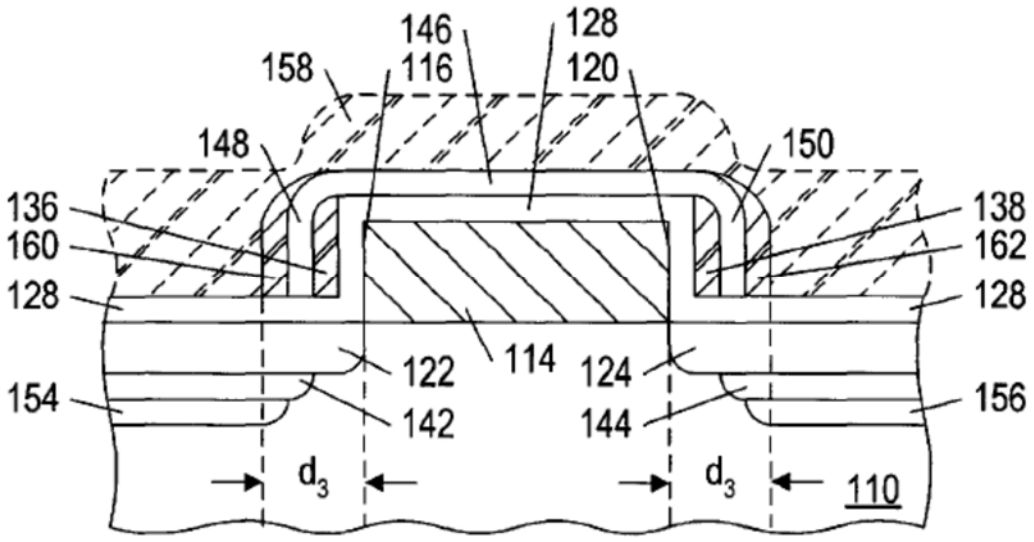


FIG. 11

Intel 598 also discloses this limitation. For example, the figures below show third and fourth nitride spacers 660 (one on each side) formed on either side of the first and second nitride spacers 640 (one each side). Each of these nitride spacers comprise a first dielectric material. *See* Ex. 1005, ¶140; Ex. 1004, 8:53-9:2 & Figs. 6f, 6h:

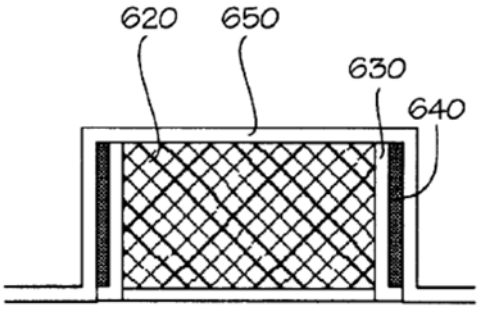


Fig. 6F

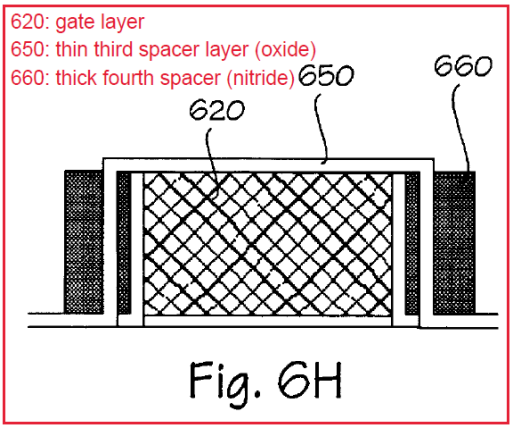


Fig. 6H

AMD 680 discloses 1(f): "exposing portions of the first and second sides of the gate structure." For example, Fig. 17 below shows a semiconductor component

wherein the first nitride spacer 136 and the second nitride spacer 138 and the oxide layer 128 have been removed by an overetching process to expose the first gate sidewall 116 and the second gate sidewall 120. *See* Ex. 1005, ¶142; Ex. 1003, 11:10-14, 56-57 & Fig. 17:

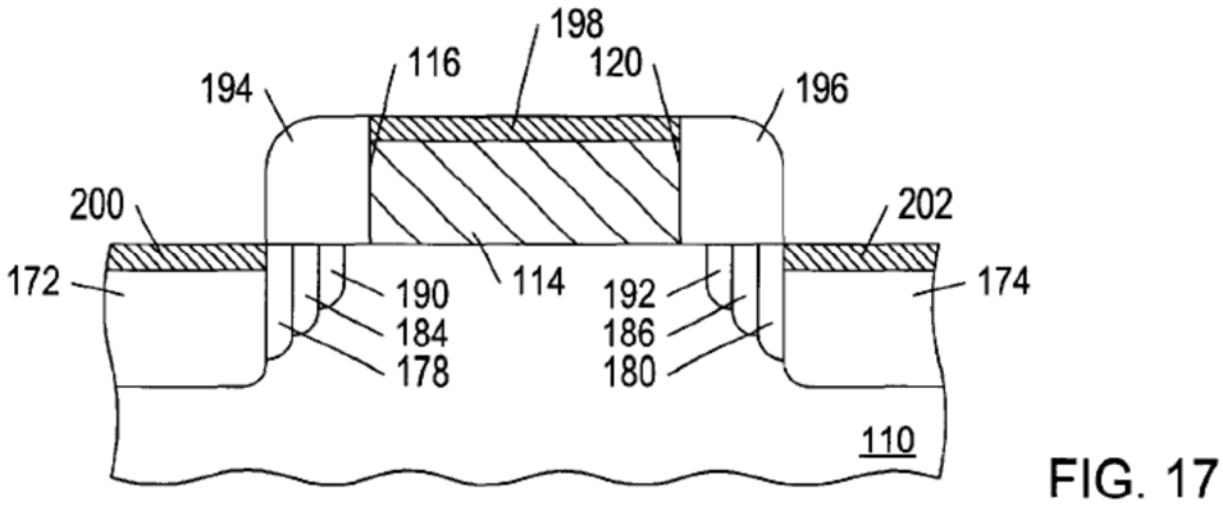
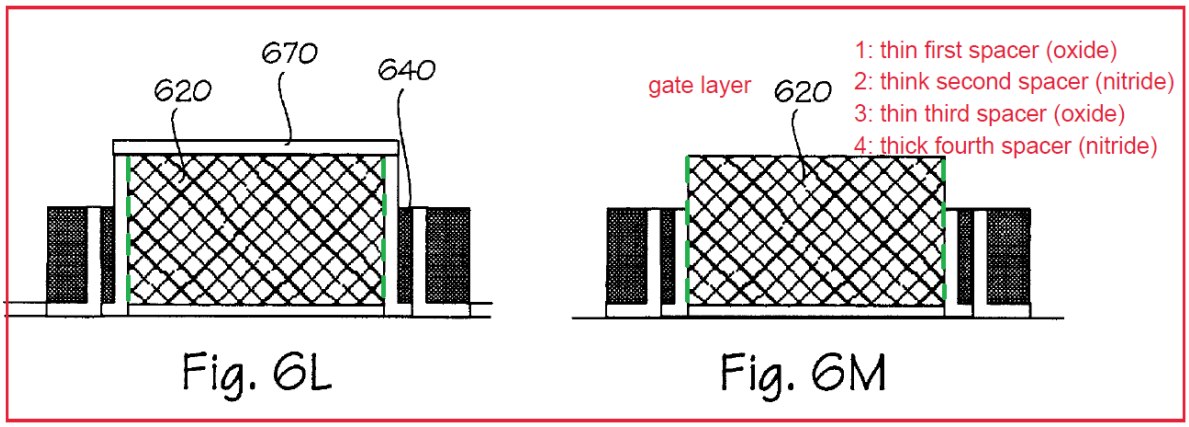


FIG. 17

Intel 598 also discloses this limitation. *See* Ex. 1005, ¶143; Ex. 1004, 9:40-55; 10:47-51 & Figs. 6l, 6m:



The thin first spacer layer 630 (not labeled) is recessed by an etching process

to expose the upper portions of the sidewalls of gate structure 620.

AMD 680 discloses 1(g): "forming source and drain regions in the semiconductor material, the source region aligned to the third spacer and the drain region aligned to the fourth spacer." For example, Fig. 12 below shows a semiconductor device with a source/drain region 166 aligned to the third nitride spacer 160 and a source/drain region 168 aligned to the fourth nitride spacer 162. Ex. 1005, ¶144; Ex. 1003, 9:20-34 & Fig. 12:

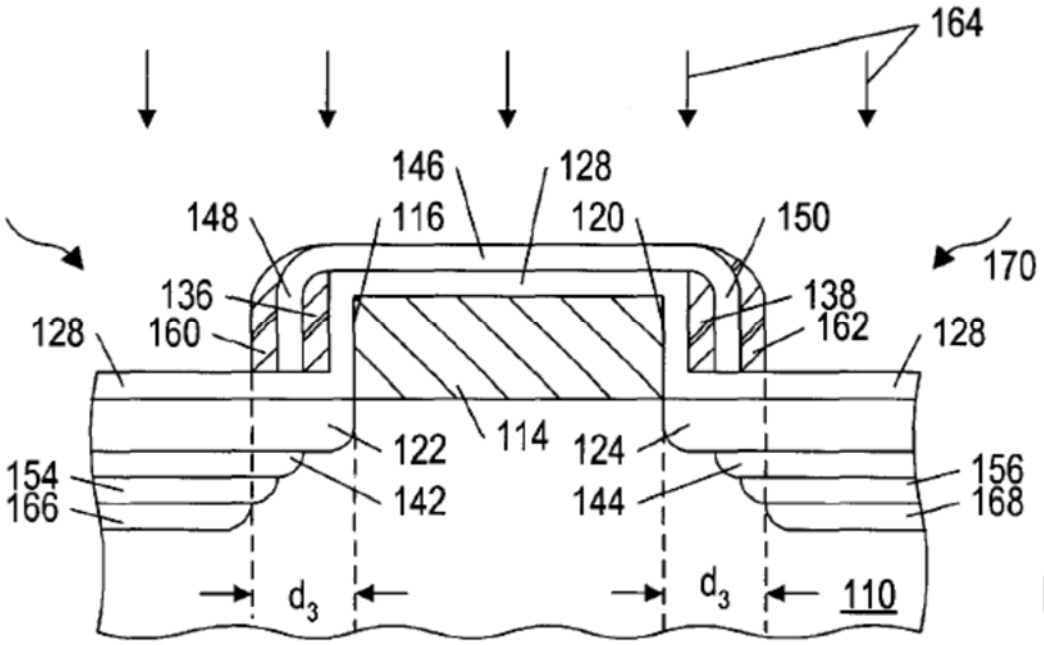


FIG. 12

Thus, the combined teachings of AMD 680 in view of Intel 598 disclose each and every limitation recited in independent claim 1 of the '126 patent. For at least the foregoing reasons, Petitioner respectfully requests the Board find claim 1 unpatentable.

F. Dependent Claims 2-11

The combined teachings of AMD 680 in view of Intel 598 disclose each and every limitation recited in dependent claims 2-11. AMD discloses the limitations of claim 2: "wherein forming the first and second spacers includes forming a layer of oxide on the gate structure, the layer of oxide between the first and second spacers and the gate structure." For example, Fig. 7 below shows a semiconductor component with an oxide layer 128 formed between the gate structure 114 and the first and second nitride spacers 136/138. *See* Ex. 1005, ¶147; Ex. 1003, Fig. 7:

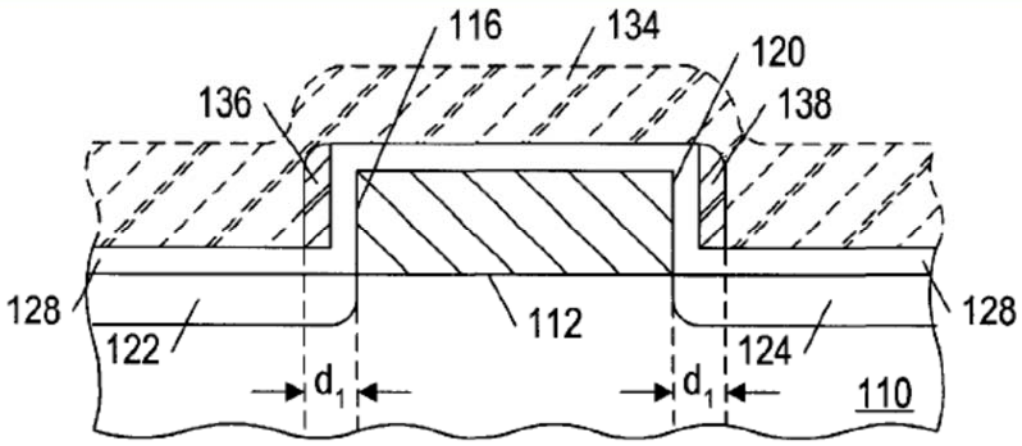


FIG. 7

Intel 598 also discloses this limitation. For example, Fig. 6e below shows a gate structure 620 with a thin oxide layer 630 formed between the gate structure 620 and the first and second nitride spacers 640 (one on each side). *See* Ex. 1005, ¶148; Ex. 1004, 8:45-49 & Fig. 6e:

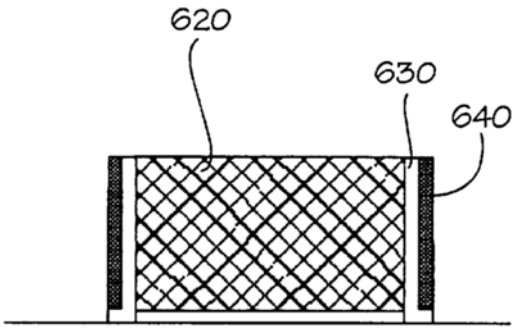


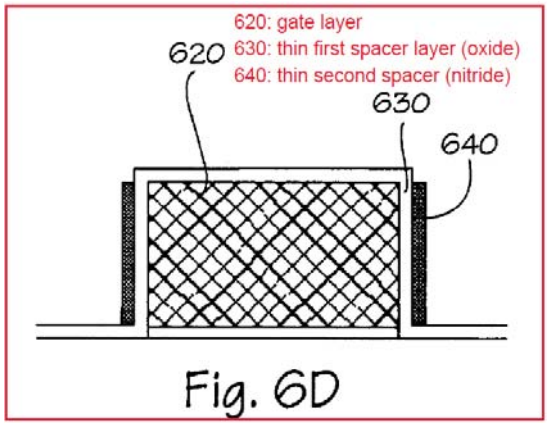
Fig. 6E

The combined teachings of AMD 680 and Intel 598 disclose the limitations of dependent claim 3: "wherein the layer of oxide has a thickness ranging from 10 Angstroms to 60 Angstroms." AMD 680 discloses an oxide layer 128 (*see* Fig. 7 above) on the semiconductor substrate 110, the top surface 118 of the gate conductor 114, and upon the gate sidewalls 116/120. Ex. 1005, ¶149; Ex. 1003, 8:11-19.

As noted above, although AMD 680 does not explicitly disclose an oxide layer of any particular thickness, it would have been an obvious design choice to do so. Ex. 1005, ¶150. AMD 680 discloses thermally growing an oxide layer or depositing a conformal oxide layer on a semiconductor material using a Chemical Vapor Deposition (CVD) process. *See* Ex. 1003, 1:27-30, 2:2-3. CVD is commonly used to deposit conformal films and protect substrate surfaces. CVD is very useful in the process of atomic layer deposition for depositing extremely thin layers of material, including oxide films. Ex. 1005, *id*.

The'126 patent specification makes clear that those skilled in the art would have been apprised of known techniques for forming oxides, including thermal oxidation and CVD. *See* Ex. 1001, 3:22-28. Thermally growing a thin layer of dielectric material such as oxide (or, alternatively, depositing it using a CVD process) with a thickness less than 100 Å was within the knowledge of one skilled in the art the time, and such person would have known thermal oxidation or CVD to be useful specifically for that purpose. *See* Ex. 1005, ¶151.

And, regardless, Intel 598 discloses this limitation. For example, Fig. 6d below shows a thin oxide layer 630 formed between the gate 620 and nitride spacers 640 having a thickness in the range of "50-150 Å, for example, 50 Å." *See* Ex. 1005, ¶15253; Ex. 1004, 8:21-27 & Fig. 6d:



It would have been obvious for a POSA to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer with Intel 598's specific disclosure of forming an oxide layer with a thickness in the

claimed range. These combined teachings render obvious the limitations recited in claim 3. *See* Ex. 1005, ¶153.

AMD 680 discloses the limitations of claim 4: "wherein forming the first and second spacers includes controllably growing a layer of oxide on the gate structure and on the semiconductor material." For example, AMD 680 discloses thermally growing an oxide layer 128 (*see* Fig. 7 above) on the semiconductor substrate 110, by oxidizing silicon in those areas. Ex. 1005, ¶154; Ex. 1003, 8:11-19.

Intel 598 also discloses this limitation. For example, Intel discloses depositing or growing a thin first oxide layer 630 using deposition techniques that were well known in the art at the time. Ex. 1005, ¶155; Ex. 1004, 8:21-29 & Fig. 6b:

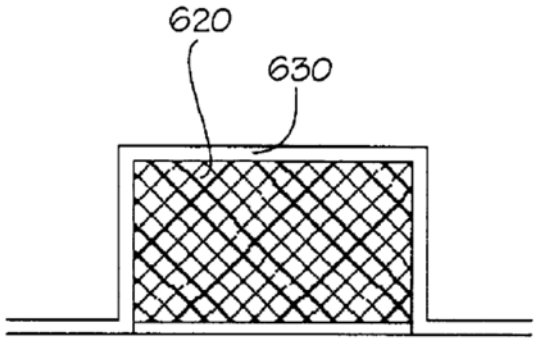


Fig. 6B

In addition, the '126 patent acknowledges that a layer of oxide as a gate dielectric material may be formed by techniques known to those skilled in the art at

the time, including thermal oxidation, chemical vapor deposition, and the like. Ex. 1005, ¶156; Ex. 1001, 3:22-28.

Both AMD 680 and Intel 598 disclose or render obvious the limitations of claim 5: "wherein controllably growing the layer of oxide includes growing the layer of oxide in a dry oxygen ambient at a temperature ranging between approximately 750 degrees Celsius and approximately 900 degrees Celsius." *See* Ex. 1005, ¶157; Ex. 1003, 8:11-19; Ex. 1004, 8:21-29. As stated in section X.A.3. above, forming oxide layers on silicon by growing them in a dry oxygen ambient at temperature ranges between 750ºC and 900ºC was well known at the time of the '126 patent and would have been an obvious design choice for a POSA. *See* Ex. 1001, 3:22-28: ("A layer of dielectric material 106 is formed on major surface 104. Dielectric layer 106 serves as a gate dielectric material and may be formed by techniques known to those skilled in the art including thermal oxidation, chemical vapor deposition, and the like.")

AMD 680 discloses the limitations of claim 6: "wherein forming the first and second spacers comprises forming the first and second spacers as nitride spacers by: forming a first layer of nitride over the gate structure and over the portions of the semiconductor material adjacent the gate structure; and anisotropically etching the layer of nitride to form the first and second spacers." Ex. 1005, ¶158; Ex. 1003, 8:23-34 & Fig. 7:

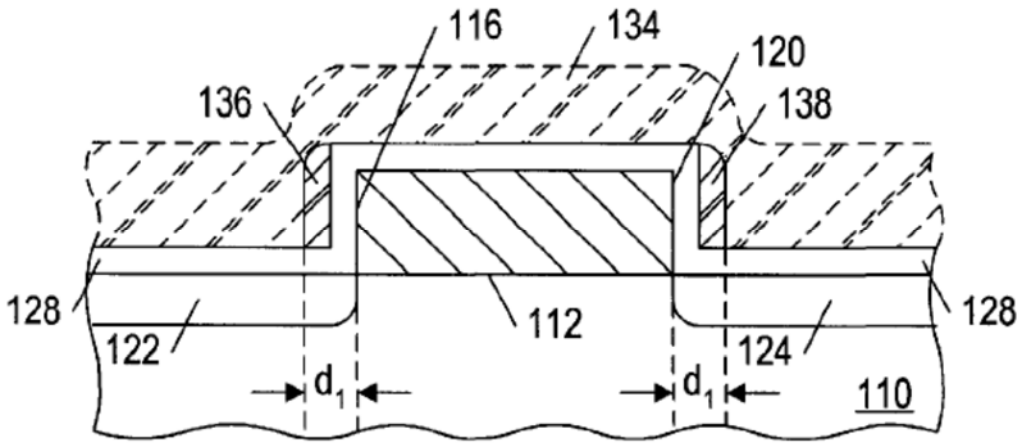


FIG. 7

Fig. 7 above shows a semiconductor component with a layer of nitride formed 134 formed over the gate structure 114 that is anisotropically etched to form the first and second nitride spacers 136/138.

Intel 598 also discloses this limitation. For example, in the figures below a thin second spacer 640 is formed over the gate structure and anisotropically etched to form the first and second nitride spacers 640. Ex. 1005, ¶159; Ex. 1004, 8:30-44 & Figs. 6c, 6d:

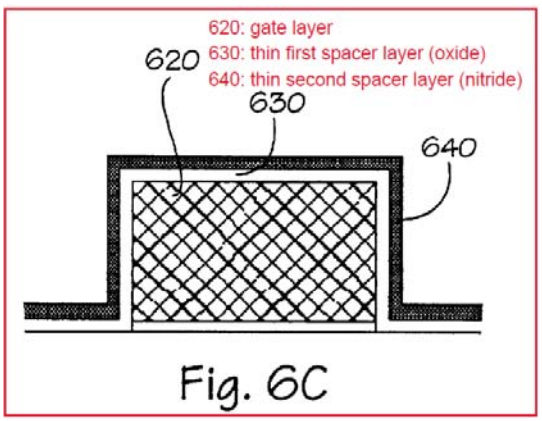


Fig. 6C

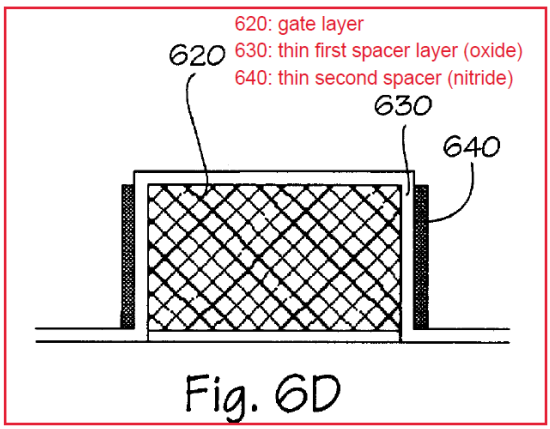


Fig. 6D

AMD 680 discloses the limitations of claim 7: "wherein forming the third and fourth spacers comprises forming the third and fourth spacers as nitride spacers by: forming a second layer of nitride over the gate structure, the first and second spacers, and over the portions of the semiconductor material adjacent the first and second nitride spacers; and anisotropically etching the second layer of nitride to form the third and fourth spacers." For example, Fig. 11 below shows a semiconductor component with a second layer of nitride 158 formed over the gate structure 114 and the first and second spacers 136/138 that is anisotropically etched to form the third and fourth nitride spacers 160/162. Ex. 1005, ¶¶160-61; Ex. 1003, 9:4-14 & Fig. 11:

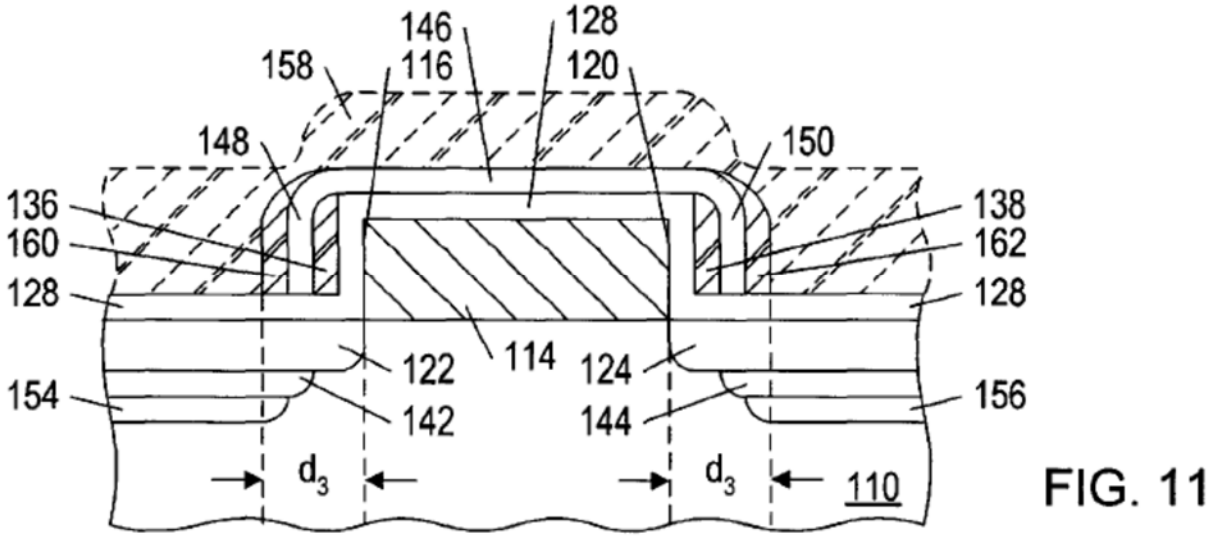


FIG. 11

Intel 598 also discloses this limitation. For example, the figures below show a thick nitride layer 660 formed over the gate structure 620 and the first and second nitride spacers 640 that is anisotropically etched to form the third and fourth nitride

spacers 660 (one on each side of the gate structure). Ex. 1005, ¶162; Ex. 1004, 8:61-64, 9:3-7 & Figs. 6g, 6h:

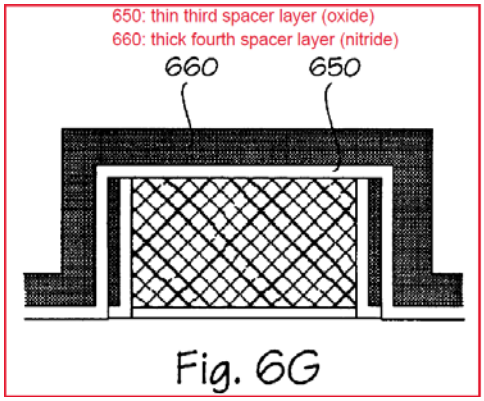


Fig. 6G

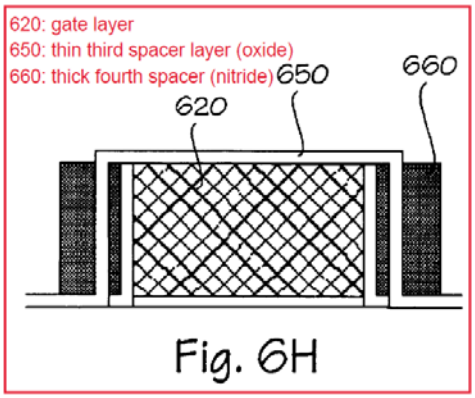


Fig. 6H

AMD 680 discloses the limitations of claim 8: "wherein exposing the portions of the first and second sidewalls of the gate structure includes overetching the first and second spacers." For example, Fig. 17 below shows a semiconductor component wherein the first and second nitride spacers 136/138 and the oxide layer 128 have been removed by an overetching process to expose the first gate sidewall 116 and the second gate sidewall 120. *See* Ex. 1005, ¶163; Ex. 1003, 11:10-14, 56-57 & Fig. 17:

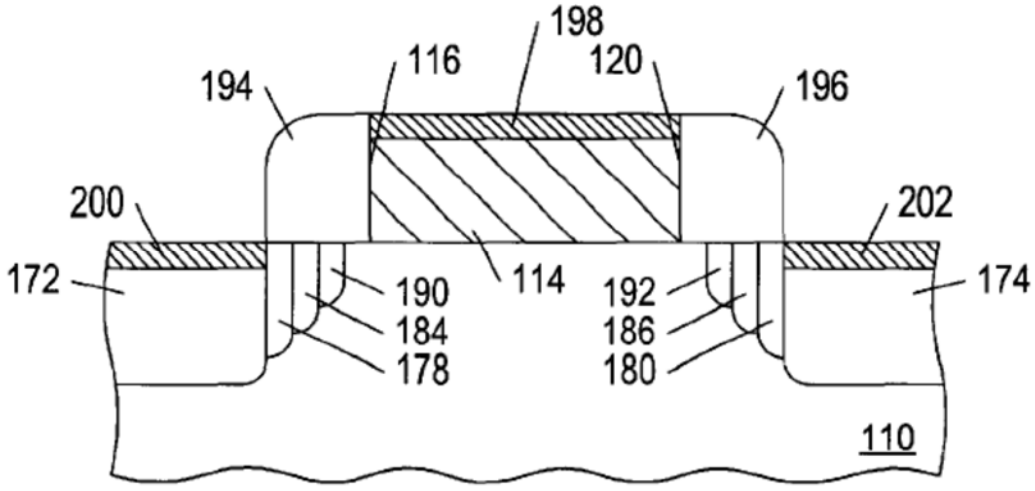


FIG. 17

Intel 598 also discloses this limitation. For example, Fig. 6m shows the thin first and second spacer layer 640 (one on each side) that are recessed by an etching process to form a gate structure with exposed upper portions of the sidewalls of gate 620. *See, e.g.*, Ex. 1005, ¶164; Ex. 1004, 9:40-55; 10:47-51 & Figs. 6l, 6m:

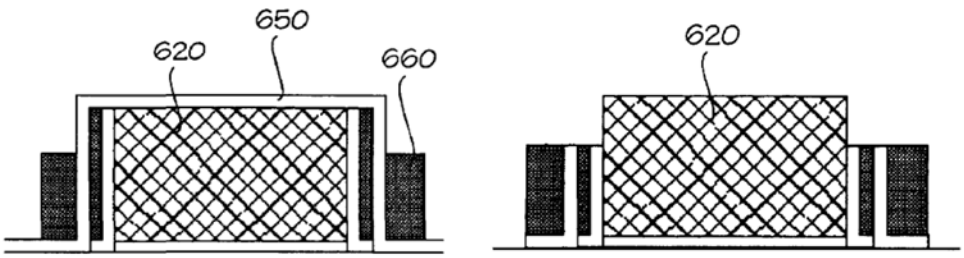


Fig. 6l Fig. 6M

The combined teachings of AMD 680 in view of Intel 598 disclose the limitations of dependent claim 9: "further including forming an electrically conductive material in the source region, the drain region, the top surface and portions of the first and second sides of the gate structure." While AMD 680 discloses forming an electrically conductive material on the source region, drain

region, and top of the gate region of a semiconductor device to form silicide thereon, it does not explicitly disclose forming silicide on the gate sidewalls. Ex. 1005, ¶165; Ex. 1003, 11:61-63 & Fig. 17:

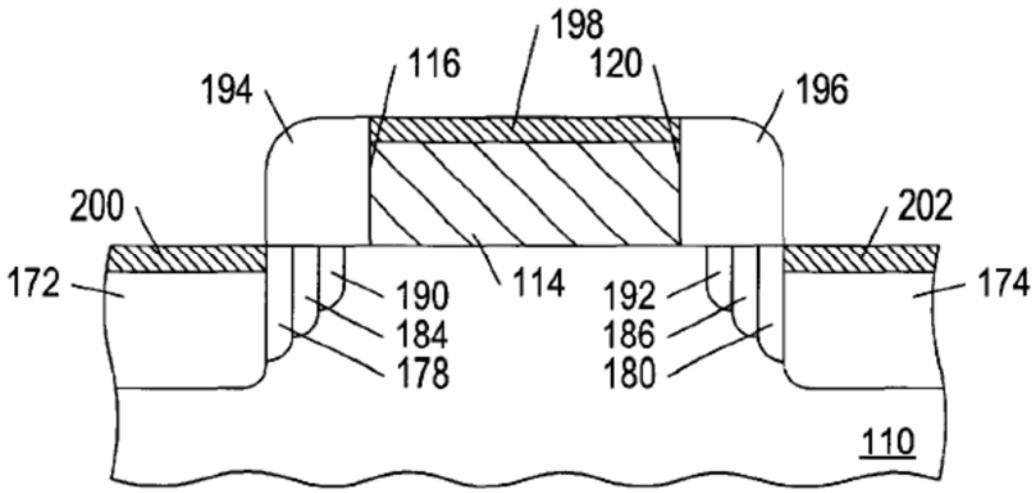


FIG. 17

Intel 598 discloses using an etch process for selectively recessing the oxide layer and nitride spacers to expose more gate silicon surface area for forming the electrically conductive layer that forms silicide on the upper portions of the gate structure. *See, e.g.*, Ex. 1005, ¶¶165-166; Ex. 1004, 9:45-55 & Fig. 6e, 6n:

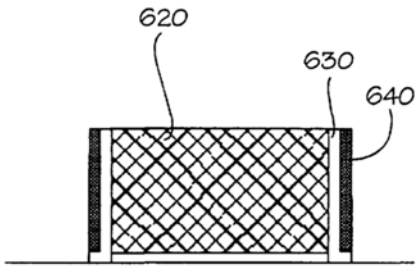


Fig. 6E

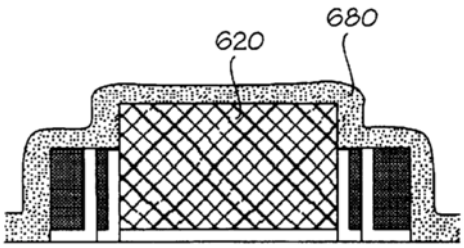


Fig. 6N

The figures above show the results of an etch process for recessing the thin oxide layer 630 and nitride spacers 640 and 660 (on each side) to expose more

silicon surface area of gate 126 for the reactant layer 680 to form on, which enables silicide formation on the upper portion of the gate sidewalls. Ex. 1005, ¶167.

As explained above, it would have been obvious for a POSA to combine the teachings of AMD 680 relating to using oxide and nitride spacers to form graded junctions in semiconductor devices with the teachings of Intel 598 relating to recessing oxide and nitride spacers for increasing the gate silicon surface area for facilitating silicide formation. Ex. 1005, ¶168. A POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with improved gate resistance (Intel 598) and reduced short-channel effects (AMD 680). *Id*. Thus, these combined teachings render obvious the limitations of claim 9.

Both AMD 680 and Intel 598 disclose the limitations of claim 10: "wherein forming the electrically conductive material includes forming silicide." As above, AMD 680 and Intel 598 disclose forming silicide on the on the source, drain, and top of the gate regions of a semiconductor device. Ex. 1005, ¶169; Ex. 1003, 11:61-63 & Fig. 17 (above); Ex. 1004, 9:45-55 & Fig. 6e, 6n (above).

The combined teachings of AMD 680 in view of Intel 598 disclose the limitations of dependent claim 11: "wherein the silicide is selected from the group of suicides comprising platinum silicide, nickel silicide, cobalt silicide, and

titanium silicide." While AMD 680 discloses forming silicide areas on the source, drain, and gate regions of a semiconductor device, AMD 680 does not explicitly identify which types of silicide could be used. Intel 598 discloses this limitation.

In particular, Intel 598 discloses titanium salicide ($TiSi_2$) selected from the claimed group. *See* Ex. 1004 1:33-34; Ex. 1005, ¶170. It would have been obvious for a POSA to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of silicide layers upon the gate structure with Intel 598's specific disclosure of titanium salicide selected from the claimed group. Ex. 1005, ¶171. As discussed above, a POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with improved gate resistance (Intel 598) and reduced short-channel effects (AMD 680). *Id*. Thus, these combined teachings render obvious the limitations of claim 11.

In accordance with the above, the combined teachings of AMD 680 in view of Intel 598 render obvious each and every limitation recited by dependent claims 2-11 of the '126 patent. For at least the foregoing reasons, Petitioner respectfully requests the Board find claims 2-11 unpatentable.

G. Independent Claim 12

The combined teachings of AMD 680 in view of Intel 598 disclose each of the limitations recited in independent claim 12 of the '126 patent. AMD 680 discloses a "method for manufacturing a semiconductor component" as recited in

the preamble of independent claim 12. *See* Ex. 1003, 1:11-14 ("This invention relates to semiconductor processing and, more particularly, to a method of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects."). Intel 598 also discloses a method for manufacturing a semiconductor component. *See* Ex. 1004, 1:6-9 ("The present invention relates to the field of semiconductor devices. More particularly, the present invention relates to a method and device for improved resistance on gate electrodes."); Ex. 1005, ¶¶173-74.[7]

AMD 680 discloses claim limitation 12(a): "providing a semiconductor material of a first conductivity type having a major surface." For example, Fig 6. below shows a semiconductor substrate 110 comprising n-type or p-type doped silicon material of a first conductivity type and having a major surface, at least at the intersection of substrate 110 and oxide layer 128. Ex. 1005, ¶¶175-76; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

[7] Petitioner's position in this Petition regarding the ordering of the steps in the challenged method claims of the '126 Patent is based on Patent Owner's apparent construction in the related district court litigation that the claimed methods need not be performed in the order listed.

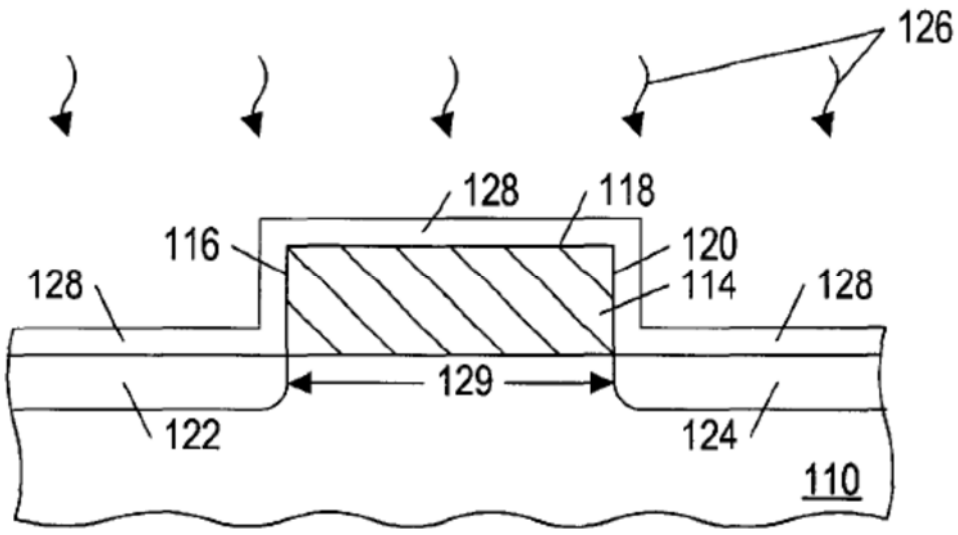


FIG. 6

Intel 598 also discloses this limitation. For example, Fig. 6a below shows a semiconductor component made of semiconductor materials having a first conductivity type and having a major surface 600. Ex. 1005, ¶¶177-78; Ex. 1004, 8:22-29 & Fig. 6a:

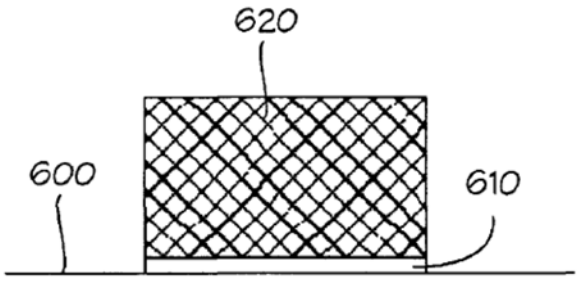


Fig. 6A

AMD 680 discloses 12(b): "forming a gate structure on the major surface, the gate structure having a first side and a second side." For example, the semiconductor component disclosed in Fig 6 above includes a gate structure 114

disposed on substrate 110, the gate structure 114 having a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1003 7:63-67 & Fig. 6 (above); Ex. 1005, ¶179.

Intel 598 also discloses this limitation. For example, Fig. 6a above discloses a gate structure 126 on a substrate 600 with a top surface and sidewalls. *See* Ex. 1005, ¶180; Ex. 1004, 8:15-20 & Fig. 6a (above).

AMD 680 discloses 12(c): "forming a first nitride spacer adjacent the first side of the gate structure and a second nitride spacer adjacent the second side of the gate structure." As shown in Fig. 7 below, AMD 680 discloses a semiconductor component with a first nitride spacer 136 formed adjacent to gate sidewall 116 and a second nitride spacer 138 formed adjacent to gate sidewall 120. *See* Ex. 1005, ¶181; Ex. 1003, 8:23-35 & Fig. 7:

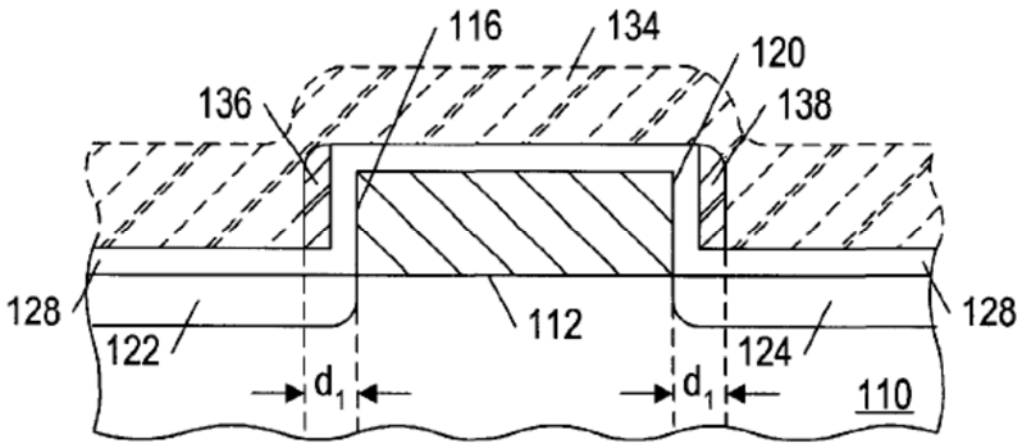


FIG. 7

Intel 598 also discloses this limitation. For example, the figures below show a semiconductor component with first and second nitride spacers 640 formed

adjacent to the sidewalls of gate structure 620. *See* Ex. 1005, ¶182; Ex. 1004, 8:30-32, 61-64 & Figs. 6c, 6g:

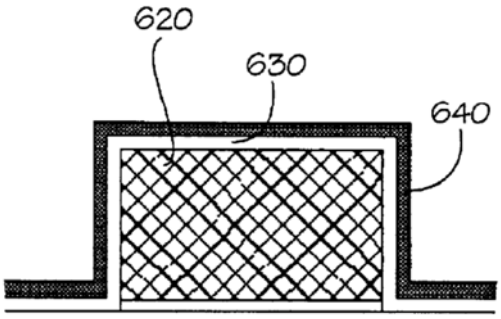


Fig. 6C

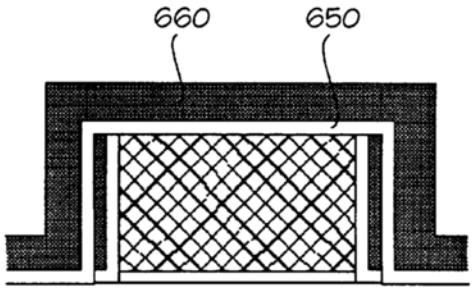


Fig. 6G

AMD 680 discloses limitation 12(d): "forming a first doped region in a portion of the semiconductor material adjacent the first nitride spacer and a second doped region in a portion of the semiconductor material adjacent the second nitride spacer." For example, Fig. 8 below shows a semiconductor component that includes a first doped region 142 aligned to the first nitride spacer 136 and a second doped region 144 aligned to the second nitride spacer 138. *See* Ex. 1005, ¶183; Ex. 1003, 8:35-47 & Fig. 8:

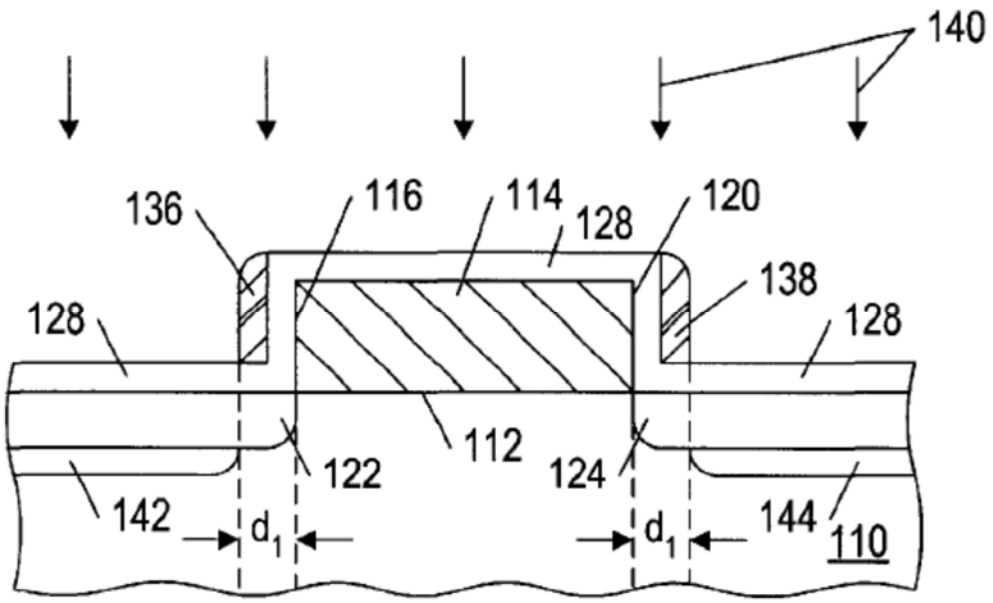


FIG. 8

AMD 680 discloses limitation 12(e): "forming a third nitride spacer adjacent the first nitride spacer." For example, Fig. 11 below shows a third nitride spacer 160 formed on one side of the first nitride spacer 136. *See* Ex. 1005, ¶¶184-85; Ex. 1003, 9:4-14 & Fig. 11:

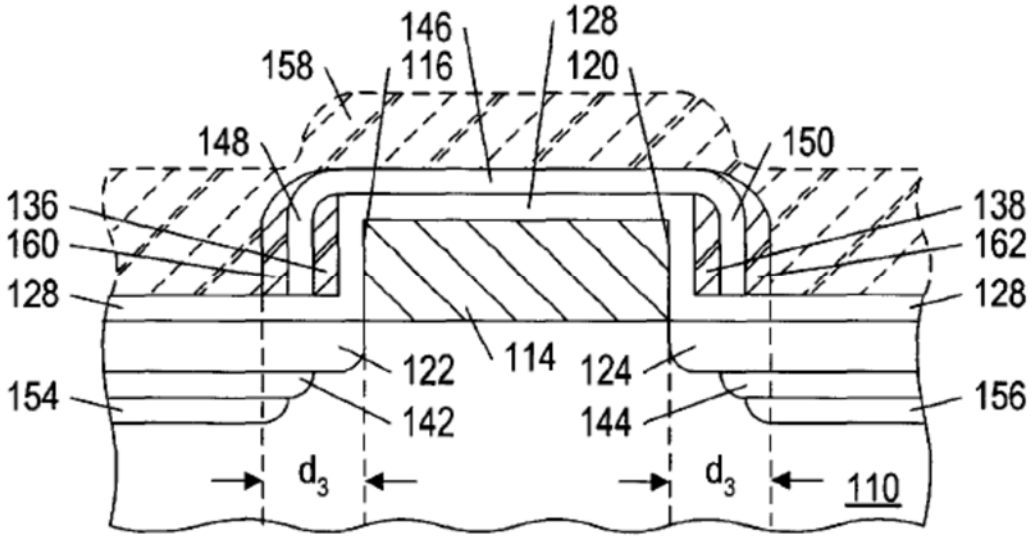


FIG. 11

Intel 598 also discloses this limitation. For example, the figures below show a third nitride spacer 660 formed on the side of the first nitride spacer 640. *See* Ex. 1005, ¶186. *See* Ex. 1004, Figs. 6h, 6l:

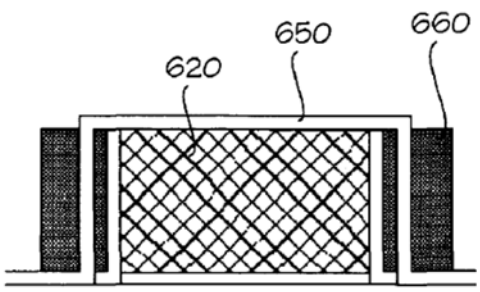


Fig. 6H

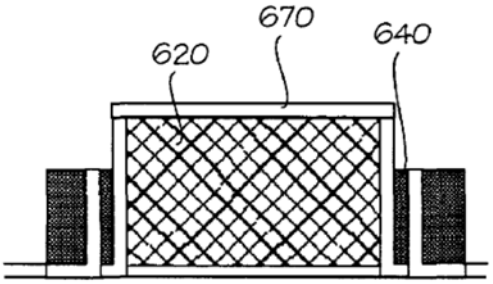


Fig. 6L

AMD 680 discloses limitation 12(f): "forming a third doped region in a portion of the semiconductor material adjacent the third nitride spacer." For example, Fig. 12 below shows a semiconductor device with a third doped region 166 aligned to the third nitride spacer 160. Ex. 1005, ¶187; Ex. 1003, 9:20-34 & Fig. 12:

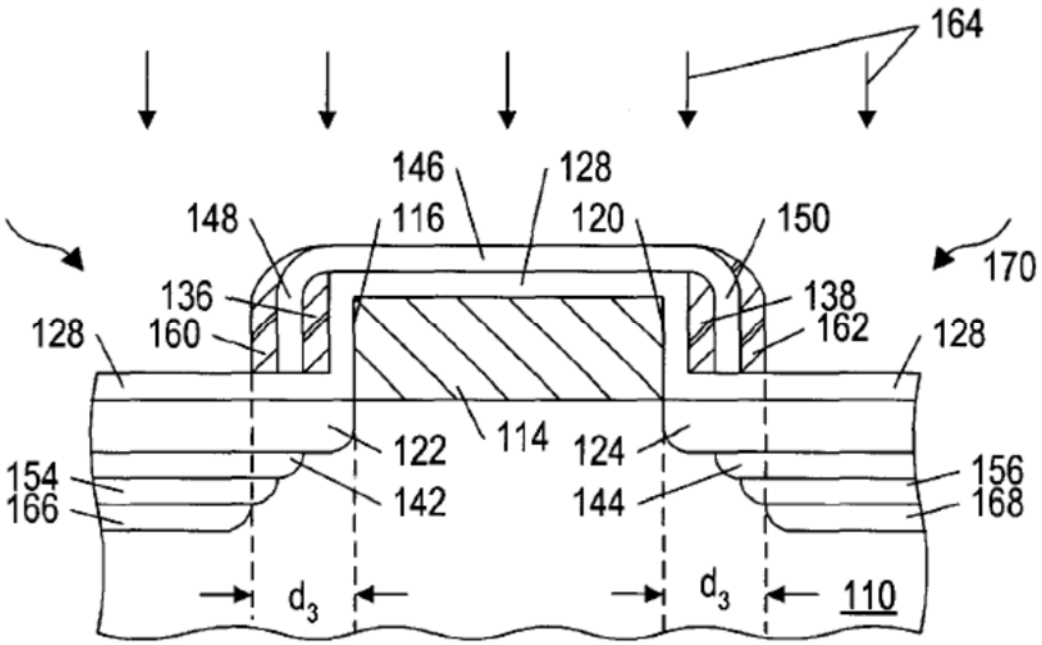


FIG. 12

AMD 680 discloses limitation 12(g): "forming a fourth doped region in a portion of the semiconductor material adjacent the second side of the gate structure." For example, Fig. 12 above shows a semiconductor device with a fourth doped region 168 formed the right of the second gate sidewall 120 of the gate structure 114. Ex. 1005, ¶188; Ex. 1003, 9:20-34 & Fig. 12.

Thus, the combined teachings of AMD 680 in view of Intel 598 render obvious each and every limitation recited in independent claim 12 of the '126 patent. For at least the reasons set forth above, Petitioner respectfully requests the Board find claim 12 unpatentable.

H. Dependent Claims 13-19

The combined teachings of AMD 680 in view of Intel 598 disclose each and every limitation recited in dependent claims 13-19. AMD 680 in view of Intel 598

discloses the limitations of dependent claim 13: "wherein forming the first nitride spacer includes forming a layer of oxide on the gate structure before forming the first nitride spacer, the layer of oxide having a thickness less than 100 Angstroms." For example, Fig. 7 of AMD 680 below shows a semiconductor component with an oxide layer 128 formed on the gate structure 114 before forming the first and second nitride spacers 136/138. *See* Ex. 1005, ¶¶190-91; Ex. 1003, 8:14-35 & Fig. 7:

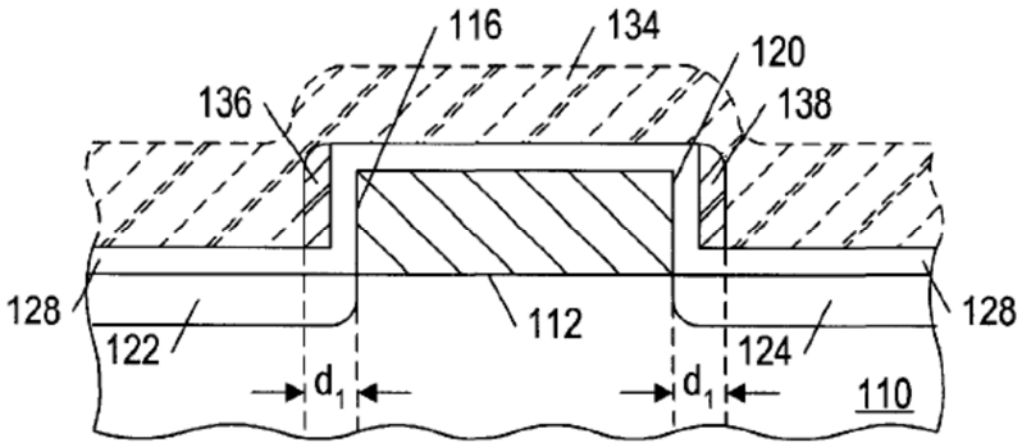


FIG. 7

As noted above, although AMD 680 does not explicitly disclose an oxide layer of any particular thickness, it would have been an obvious design choice for a POSA to do so. Ex. 1005, ¶192. And, regardless, Intel 598 discloses this limitation. For example, Fig. 6e below shows a gate structure 620 with a thin oxide layer 630 formed on the gate structure 620 before the formation of the first and second nitride spacers 640 (one on each side). *See* Ex. 1005, *id.*; Ex. 1004, 8:21-38 & Fig. 6c:

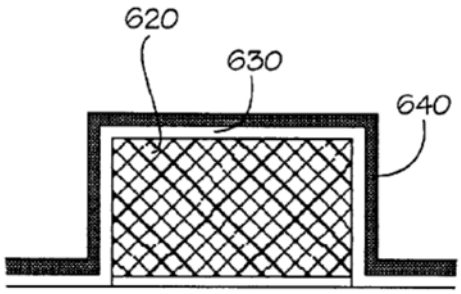


Fig. 6C

Further, Intel 598 discloses that the thin oxide layer 630 comprises a thickness in the range of "50-150 Å, for example, 50 Å." *See* Ex. 1005, ¶193; Ex. 1004, 8:21-27.

It would have been obvious for a POSA to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer with Intel 598's specific disclosure of forming an oxide layer with a thickness in the claimed range. Ex. 1005, ¶194. These combined teachings render obvious the limitations recited in claim 13.

Both AMD 680 and Intel 598 disclose and/or render obvious the limitations of claim 14(a): "wherein forming the first and second nitride spacers comprises: growing a layer of oxide on the gate structure in an oxygen ambient and at a temperature between 700 degrees Celsius and 950 degrees Celsius." *See* Ex. 1005 ¶195, Ex. 1003, 8:11-19; Ex. 1004, 8:21-29. As stated in section X. A. 3. above, forming oxide layers on silicon by growing them in a dry oxygen ambient at temperature ranges between 750ºC and 900ºC was well known at the time of the

’126 patent and would have been an obvious design choice for a POSA. *See id.;* Ex. 1005, ¶195; Ex. 1001, 3:22-28: (“A layer of dielectric material 106 is formed on major surface 104. Dielectric layer 106 serves as a gate dielectric material and may be formed by techniques known to those skilled in the art including thermal oxidation, chemical vapor deposition, and the like.”)

Both AMD 680 and Intel 598 disclose the limitations recited in 14(b) and 14(c): “depositing a layer of nitride on the layer of oxide on the gate structure and above the semiconductor material; and anisotropically etching the layer of nitride.” *See* Ex. 1005, ¶196; Ex. 1003, 8:23-35 & Fig. 7:

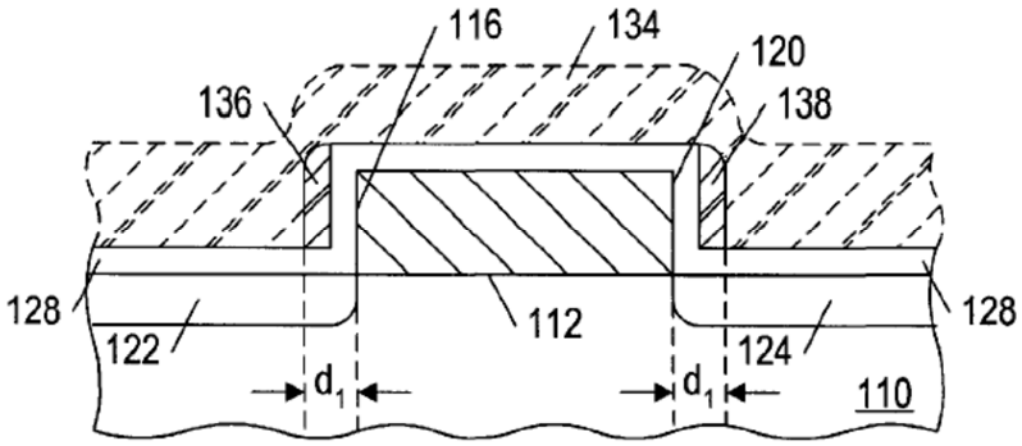


FIG. 7

Fig. 7 above shows a layer of nitride 134 deposited on the layer of oxide 128 on the gate structure 114 and above the semiconductor substrate 110 which is anisotropically etched to form the first nitride spacer 136 adjacent to the first gate sidewall 116 and the second nitride spacer 138 adjacent to the second gate sidewall

120. Intel 598 also discloses this limitation. *See* Ex. 1005, ¶¶197-198; Ex. 1004, 8:61-9:7, Figs. 6g, 6h:

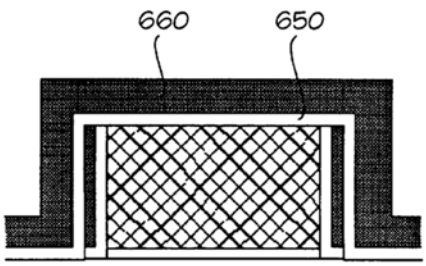


Fig. 6G

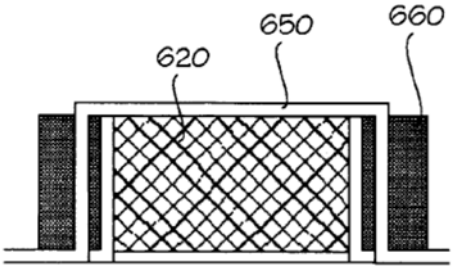


Fig. 6H

AMD 680 discloses the limitations of claim 15: "wherein forming the third nitride spacer includes exposing a portion of the first side of the gate structure." For example, Fig. 17 below shows a semiconductor component wherein the first nitride spacer 136 and the second nitride spacer 138 and the oxide layer 128 have been removed by an overetching process to expose the first gate sidewall 116 and the second gate sidewall 120. *See* Ex. 1005, ¶199; Ex. 1003, 11:10-14, 56-57 & Fig. 17:

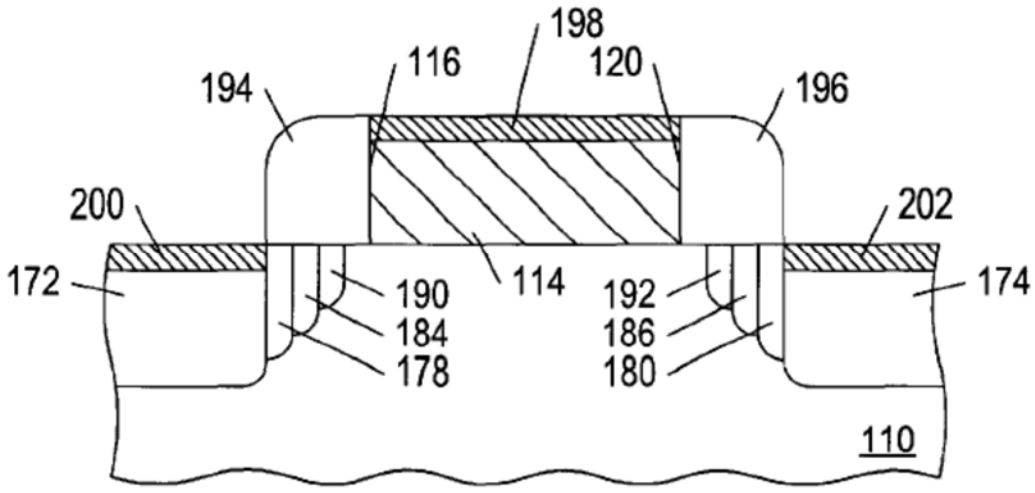
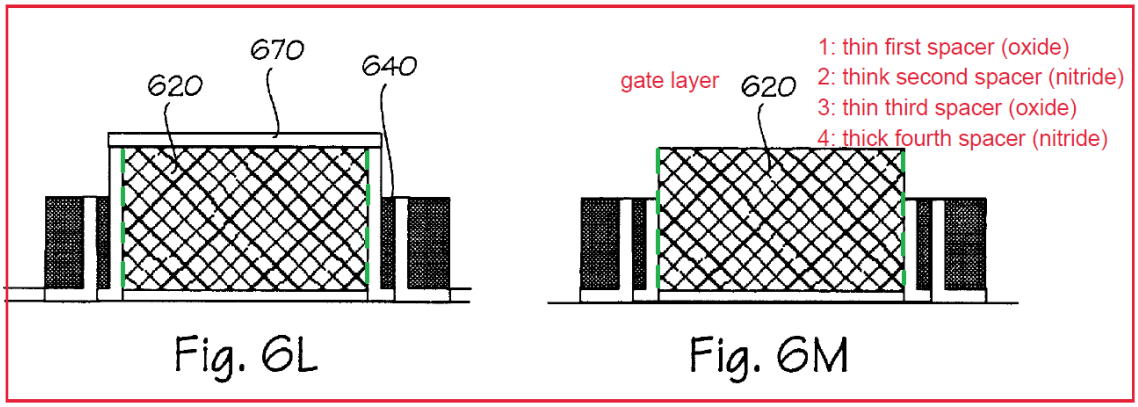


FIG. 17

Intel 598 also discloses this limitation. For example, the figures below show the thin first spacer layer 630 recessed by an etching process to form a gate structure with exposed upper portions of the gate sidewalls. *See* Ex. 1005, ¶200; Ex. 1004, 9:40-55; 10:47-51 & Figs. 6l, 6m:



AMD 680 discloses the limitations recited in claim 16: "forming a fourth nitride spacer adjacent the second nitride spacer." For example, Fig. 11 below shows a fourth nitride spacer 162 formed on the right side of the second nitride spacer 138. *See* Ex. 1005, ¶201; Ex. 1003, 9:4-14 & Fig. 11:

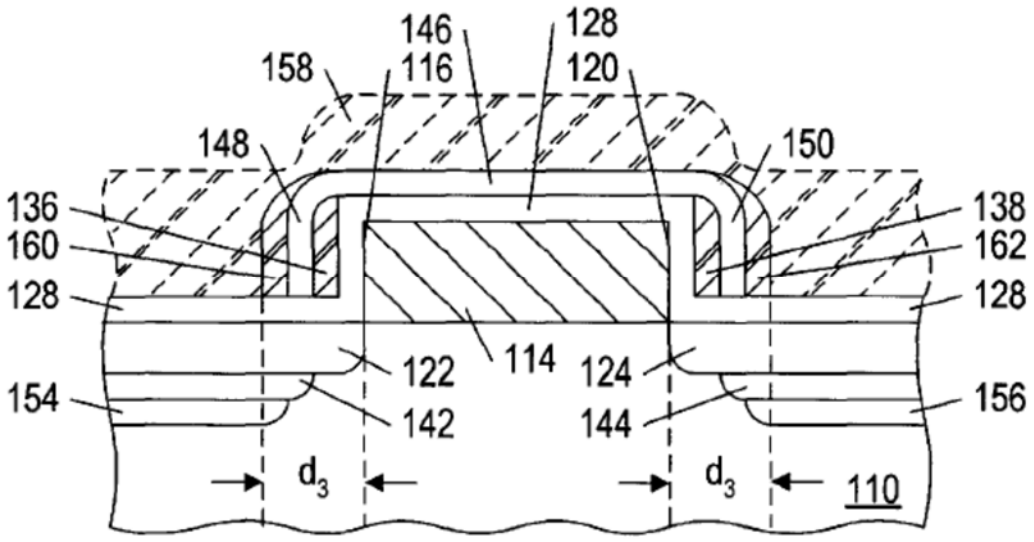


FIG. 11

Intel 598 also discloses this limitation. For example, the figures below show a fourth nitride spacer 660 formed on the right side of a second nitride spacer 640. *See* Ex. 1005, ¶202; Ex. 1004, 8:53-9:2 & Figs. 6f, 6h:

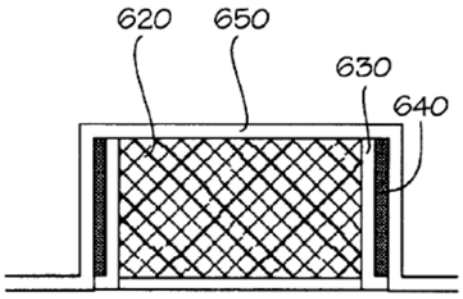


Fig. 6F

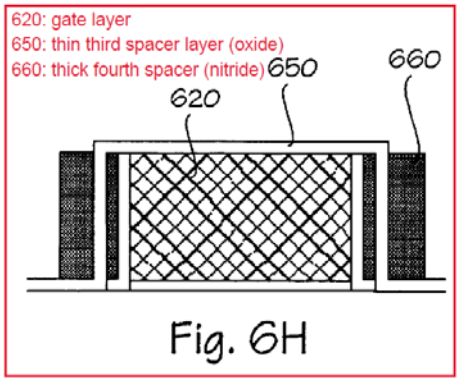


Fig. 6H

AMD 680 discloses the limitations of claim 17: "further including forming the second nitride spacer contemporaneously with the first nitride spacer and forming the fourth nitride spacer contemporaneously with the third nitride spacer." As shown in Figs. 7 and 11 below, AMD 680 discloses forming the first and second nitride spacers 136/138 contemporaneously and forming the third and

fourth nitride spacers 160/162 contemporaneously. *See* Ex. 1005, ¶203; Ex. 1003, 8:23-35, 9:4-14 & Fig. 7, 11:

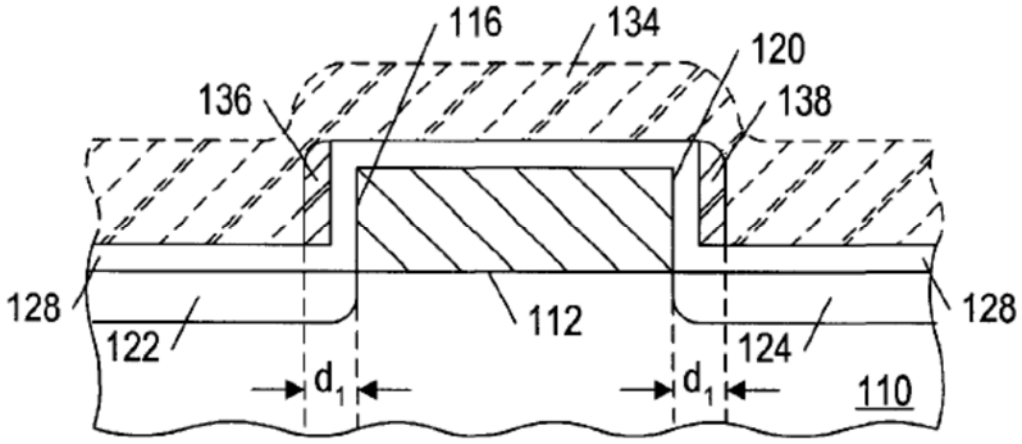


FIG. 7

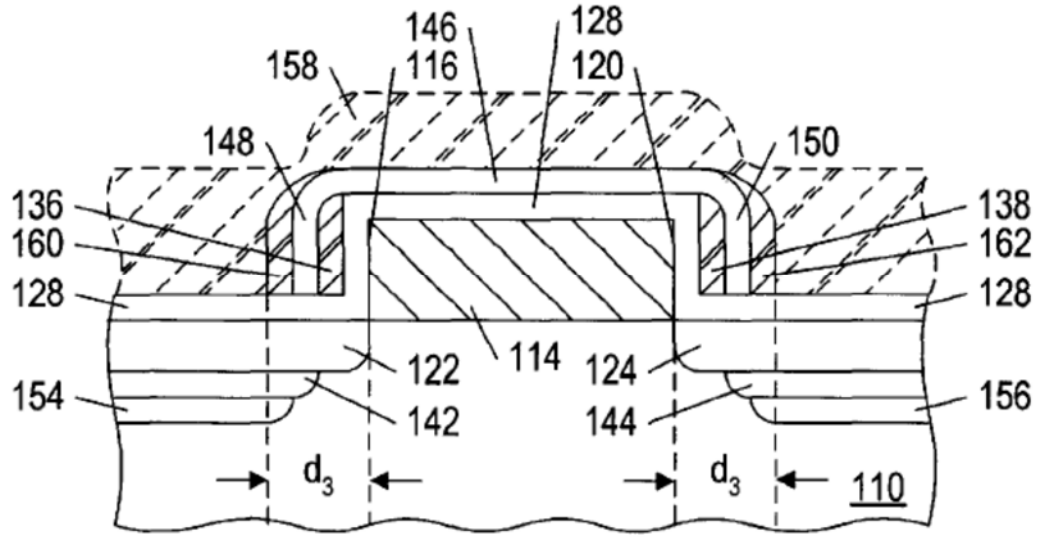


FIG. 11

Intel 598 also discloses this limitation. For example, the figures below show a semiconductor component with the first and second nitride spacers 640 (one on each side) formed contemptuously and the third and fourth nitride spacers 660 formed contemporaneously (one on each side). *See* Ex. 1005, ¶204; Ex. 1004, 8:30-32, 61-64 & Figs. 6c, 6g:

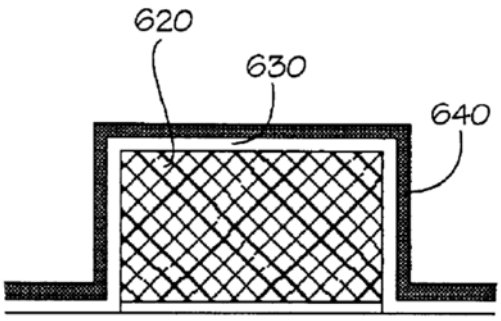


Fig. 6C

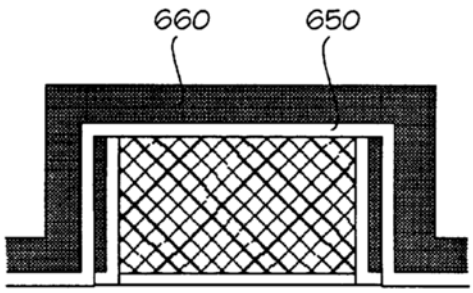


Fig. 6G

AMD 680 discloses the limitations of claim 18: "further including forming the third and fourth nitride spacers using an anisotropic etch technique and wherein anisotropically etching exposes portions of the first and second sides and the top surface of the gate structure." For example, Fig. 17 below shows removal of the nitride spacers 136, 138, 160 and 162, and the oxide layer 128, by an overetching process to expose the gate sidewalls 116/120. *See* Ex. 1005, ¶205; Ex. 1003, 11:10-14, 56-57 & Fig. 17:

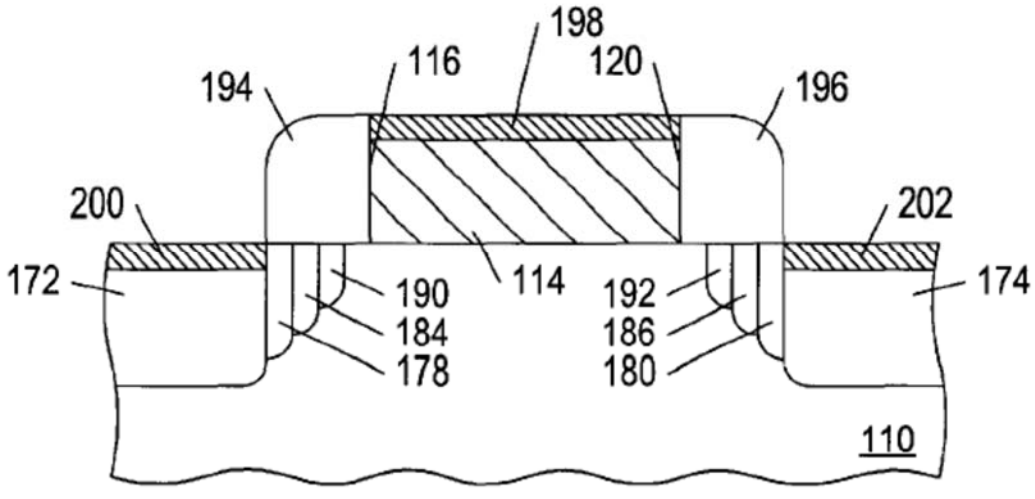
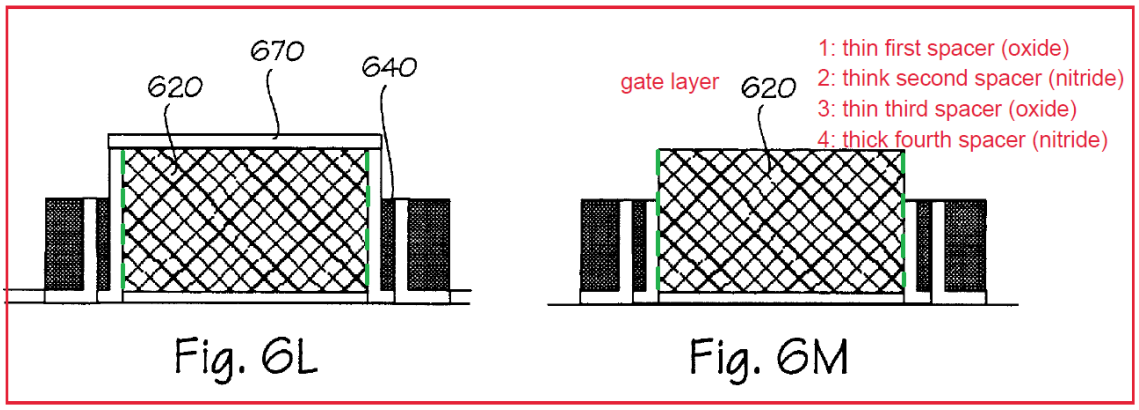


FIG. 17

Intel 598 also discloses this limitation. For example, the figures below show recessing of the nitride spacers 640 and 660, and the thin oxide layer 630 by an etching process to form a gate structure 620 with exposed upper portions of the gate sidewalls. Ex. 1005, ¶206; Ex. 1004, 9:40-55; 10:47-51 & Figs. 6l, 6m:



AMD 680 discloses the limitations of claim 19: "further including forming the fourth doped region adjacent the fourth nitride spacer." For example, Fig. 12 below shows a semiconductor device with a fourth doped region 168 aligned to the fourth nitride spacer 162. Ex. 1005, ¶207; Ex. 1003, 9:20-34 & Fig. 12:

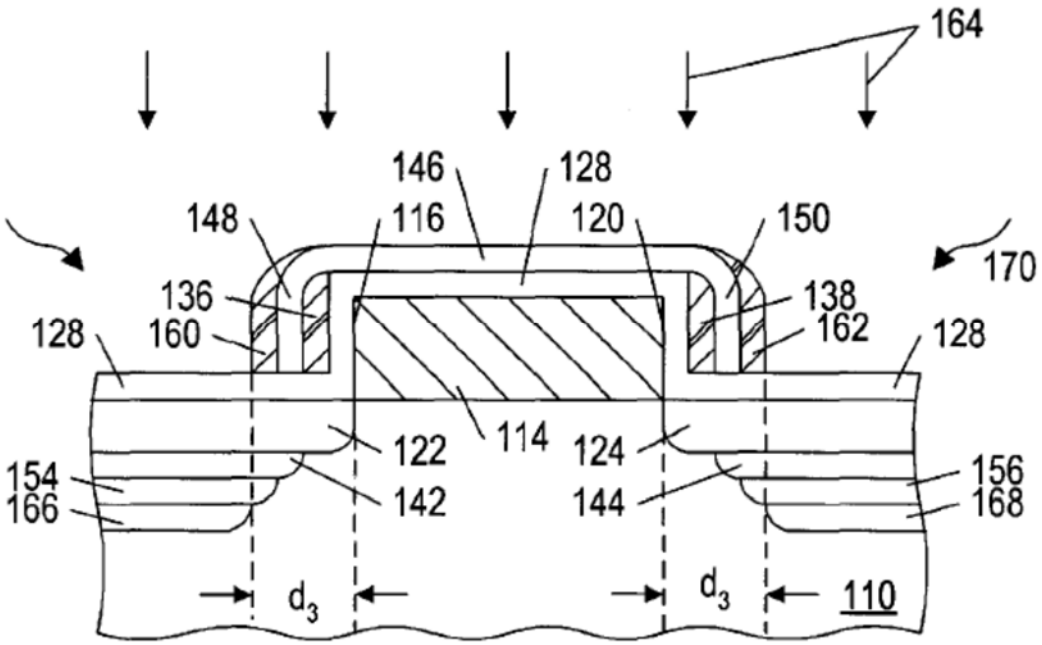


FIG. 12

Thus, the combined teachings of AMD 680 in view of Intel 598 render obvious each and every limitation recited in dependent claims 1-19 of the ’126 patent. A claim chart for AMD 680 in view of Intel 598 and the knowledge of a POSA is attached as Exhibit 1007.

For at least the foregoing reasons, Petitioner respectfully requests the Board find dependent claims 1-19 of the ’126 patent unpatentable.

XI. GROUND 2: CLAIMS 1-2, 4-8, 12, 14, 16-17 AND 19 ARE ANTICIPATED BY AMD 680

If the patented invention was “patented or described in a printed publication in this or a foreign country . . . more than one year prior to the date of the application for patent in the United States,” then the invention is not novel—it is said to be anticipated by the prior art. Anticipation requires a determination of

whether the prior patent or printed publication discloses each and every element of the claimed invention. *In re Paulsen,* 30 F.3d 1475 (Fed. Cir. 1994); *In re Robertson,* 169 F.3d 743, 745 (Fed. Cir. 1999). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

AMD 680 discloses each and every limitation of claims 1-2, 4-8, 12, 14, 16-17 and 19 of the '126 patent, and consequently, anticipates these claims. Like the '126 patent, AMD 680 concerns a method of manufacturing semiconductor devices using a sequence of interposed pairs of oxide layers and nitride spacers formed adjacent to the sidewalls of the gate structure which were used to form a graded junction with a relatively smooth doping profile for the purpose of minimizing the abrupt voltage change at the junction to reduce the intensity of the electric field. *See* Ex. 1001, 1:27-30; Ex. 1003, 3:6-7, 21-33, 4:56-60; Ex. 1005, ¶209. This, in turn, reduced harmful short-channel effects in the semiconductor device. *See* Ex. 1003, 5:1-9. Disbursing the abrupt voltage changes at the junction reduced the intensity of the electric field and associated harmful short-channel effects. *See* Ex. 1003, 3:23-33; Ex. 1005, *id*.

A. AMD 680 Anticipates Independent Claim 1

AMD 680 discloses each and every limitation recited in independent claim 1 of the ’126 patent. As discussed above in section X. E above, AMD 680 discloses the preamble of independent claim 1. *See* Ex. 1005, ¶210; Ex. 1003, 1:11-14 (“This invention relates to semiconductor processing and, more particularly, to a method of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects.”).[8]

AMD 680 discloses limitation 1(a) as discussed in section X. E. above. For example, the semiconductor component disclosed in Fig 6 of AMD 680 included a semiconductor substrate 110 comprising n-type or p-type doped silicon material of a first conductivity type and having a major surface, at least at the intersection of substrate 110 and oxide layer 128. Ex. 1005, ¶211; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

[8] Petitioner’s position in this Petition regarding the ordering of the steps in the challenged method claims of the ’126 Patent is based on Patent Owner’s apparent construction in the related district court litigation that the claimed methods need not be performed in the order listed.

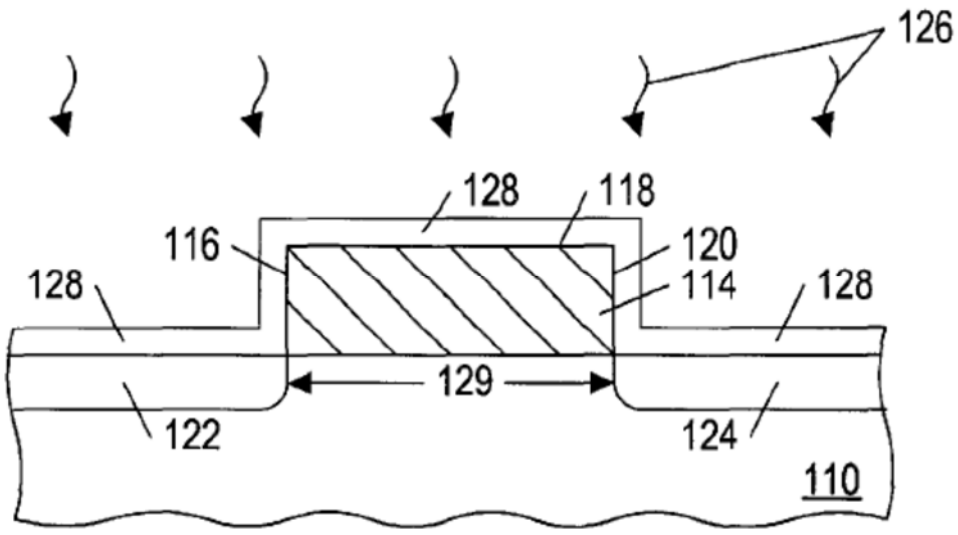


FIG. 6

AMD 680 discloses limitation 1(b) as discussed in section X.E. above. For example, the semiconductor component disclosed in Fig 6 includes a gate structure 114 disposed on substrate 110, the gate structure 114 having a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1003 7:63-67 & Fig. 6; Ex. 1005, ¶212.

AMD 680 discloses limitation 1(c) as discussed in section X.E. above. *See* Ex. 1005, ¶213; Ex. 1003, 8:23-35 & Fig. 7:

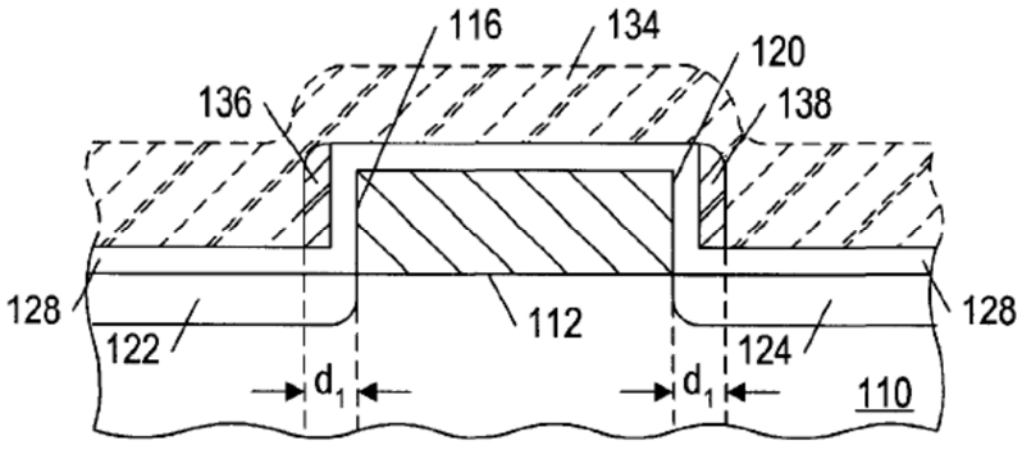


FIG. 7

As shown in Fig. 7 above, AMD 680 discloses a semiconductor component

with a first nitride spacer 136 formed adjacent to gate sidewall 116 and a second nitride spacer 138 formed adjacent to gate sidewall 120.

AMD 680 discloses limitation 1(d) as discussed in section X.E. above. *See, e.g.*, Ex. 1005, ¶¶215-16; Ex. 1003, 8:35-47 & Fig. 8:

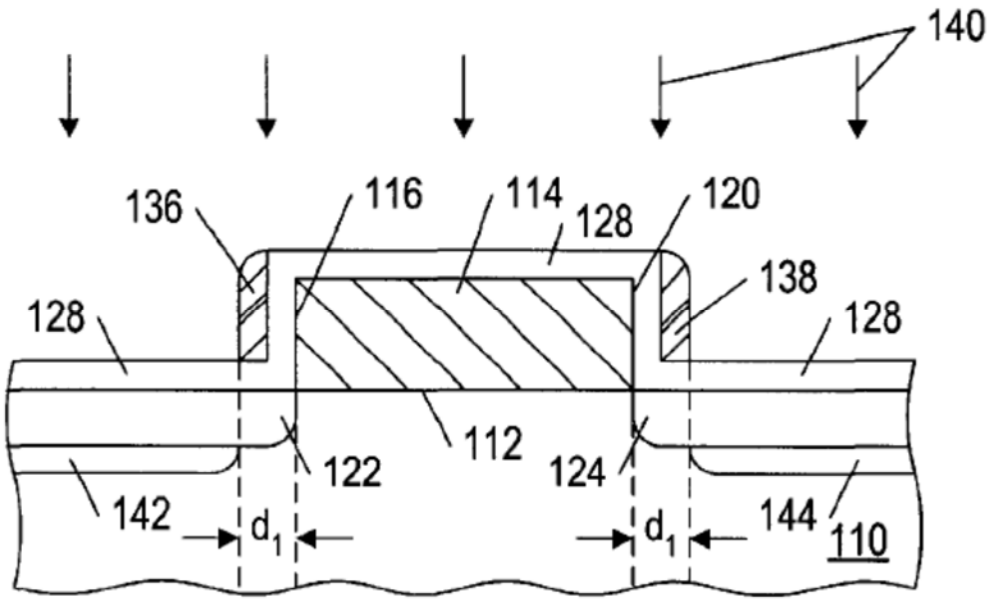


FIG. 8

As shown in Fig. 8 above, the semiconductor component includes a source/drain extension region 142 aligned to the first nitride spacer 136 and a source/drain extension region aligned to the second nitride spacer 138.

AMD 680 discloses limitation 1(e) as discussed in section X. E. above. For example, Fig. 11 below shows a third nitride spacer 160 comprised of a dielectric material that is formed on one side of the first nitride spacer 136 and a fourth nitride spacer 162 comprised of a dielectric material that is formed on the other side of the second nitride spacer 138. *See* Ex. 1005, ¶217; Ex. 1003, 9:4-14 & Fig.

11:

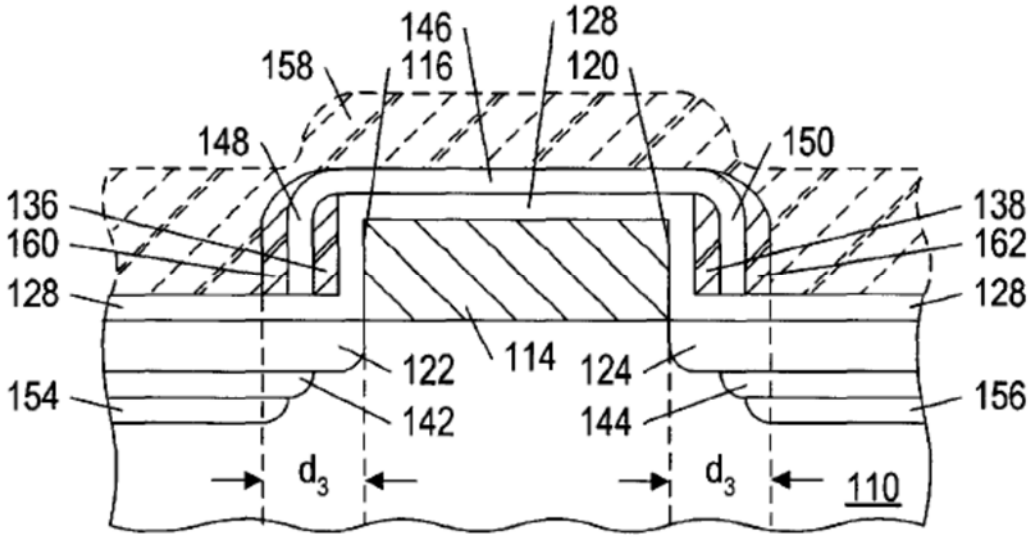


FIG. 11

AMD 680 discloses limitation 1(f) as discussed in section X. E. above. For example, Fig. 17 below shows a semiconductor component wherein the first nitride spacer 136 and the second nitride spacer 138 and the oxide layer 128 have been removed by an overetching process to expose the first gate sidewall 116 and the second gate sidewall 120. *See* Ex. 1005, ¶218; Ex. 1003, 11:10-14, 56-57 & Fig. 17:

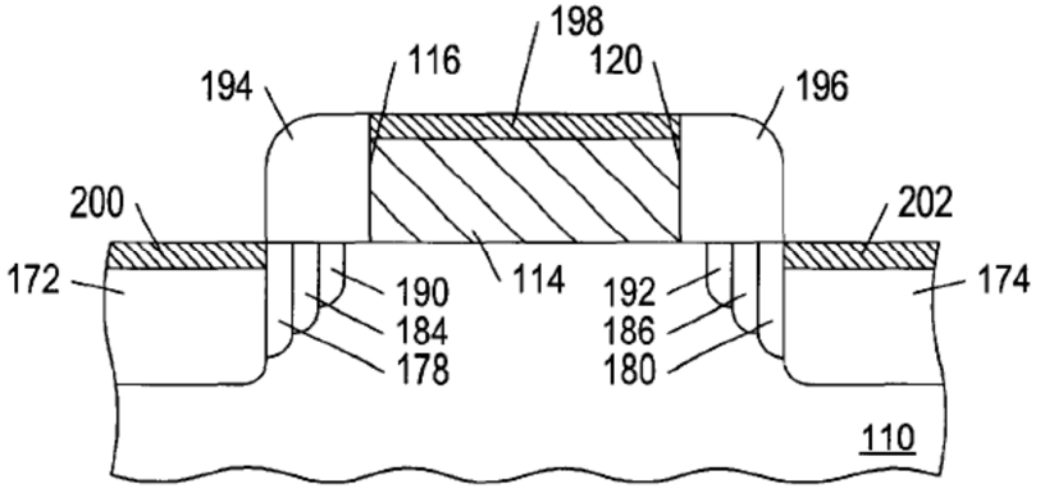


FIG. 17

AMD 680 discloses 1(g) as discussed in section X. E. above. For example, Fig. 12 below shows a semiconductor device with a source/drain region 166 aligned to the third nitride spacer 160 and a source/drain region 168 aligned to the fourth nitride spacer 162. Ex. 1005, ¶219; Ex. 1003, 9:20-34 & Fig. 12:

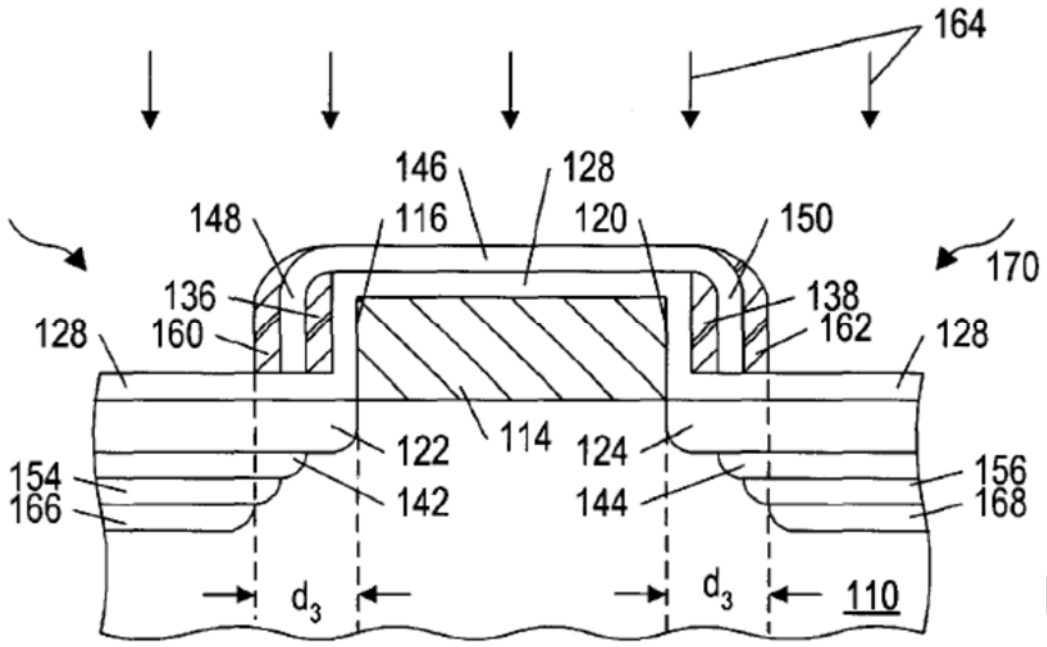


FIG. 12

Thus, AMD 680 discloses each and every limitation recited in independent

claim 1 of the ’126 patent, and as a consequence, anticipates this claim. For at least the foregoing reasons, Petitioner respectfully requests the Board find claim 1 unpatentable.

B. AMD 680 Anticipates Dependent Claims 2 And 4-8

AMD 680 discloses the limitations recited in claim 2 as discussed in section X. F. above. For example, Fig. 7 below shows a semiconductor component with an oxide layer 128 formed between the gate structure 114 and the first and second nitride spacers 136/138. *See* Ex. 1005, ¶¶221-22; Ex. 1003, Fig. 7:

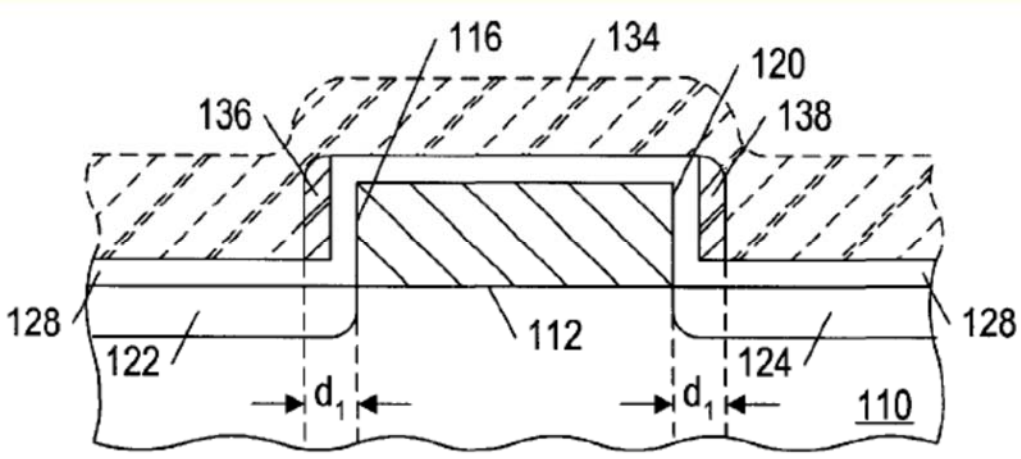


FIG. 7

AMD 680 discloses the limitations of claim 4 as discussed in section X. F. above. For example, AMD 680 discloses thermally growing an oxide layer 128 (*see* Fig. 7 above) on the semiconductor substrate 110, by oxidizing silicon in those areas. Ex. 1005, ¶223; Ex. 1003, 8:11-19. In addition, the ’126 patent acknowledges that a layer of oxide as a gate dielectric material may be formed by

techniques known to those skilled in the art at the time, including thermal oxidation, chemical vapor deposition, and the like. Ex. 1001, 3:22-28.

AMD 680 discloses the limitations of claim 5 as discussed in section X. F. above. *See* Ex. 1003, 8:11-19; Ex. 1004, 8:21-29. And as stated above, the '126 patent acknowledges that oxides may be formed using techniques that were well known in the art at the time, and the particular temperature ranges would have been an obvious design choice. *See* Ex. 1005, ¶224; *See* Ex. 1001, 3:22-28: ("A layer of dielectric material 106 is formed on major surface 104. Dielectric layer 106 serves as a gate dielectric material and may be formed by techniques known to those skilled in the art including thermal oxidation, chemical vapor deposition, and the like.").

AMD 680 discloses the limitations of claim 6 as discussed in section X. F. above. For example, Fig. 7 below shows a semiconductor component with a layer of nitride formed over the gate structure 114 that was anisotropically etched to form the first and second nitride spacers 136 and 138. Ex. 1005, ¶225; Ex. 1003, 8:23-34 & Fig. 7:

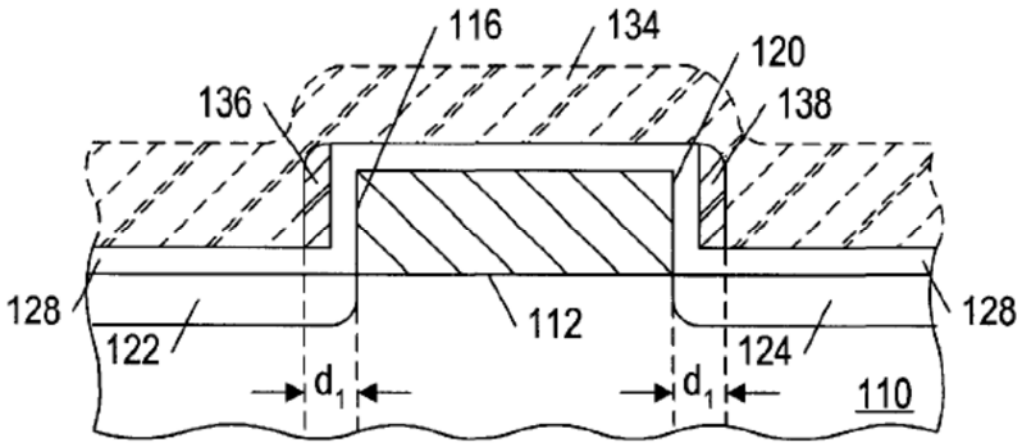


FIG. 7

AMD 680 discloses the limitations of claim 7 as discussed in section X.F. above. For example, Fig. 11 shows a semiconductor component with a second layer of nitride formed over the gate structure 114 and the first and second spacers 136/138 that is anisotropically etched to form the third and fourth nitride spacers 160/162. Ex. 1005, ¶226; Ex. 1003, 9:4-14 & Fig. 11:

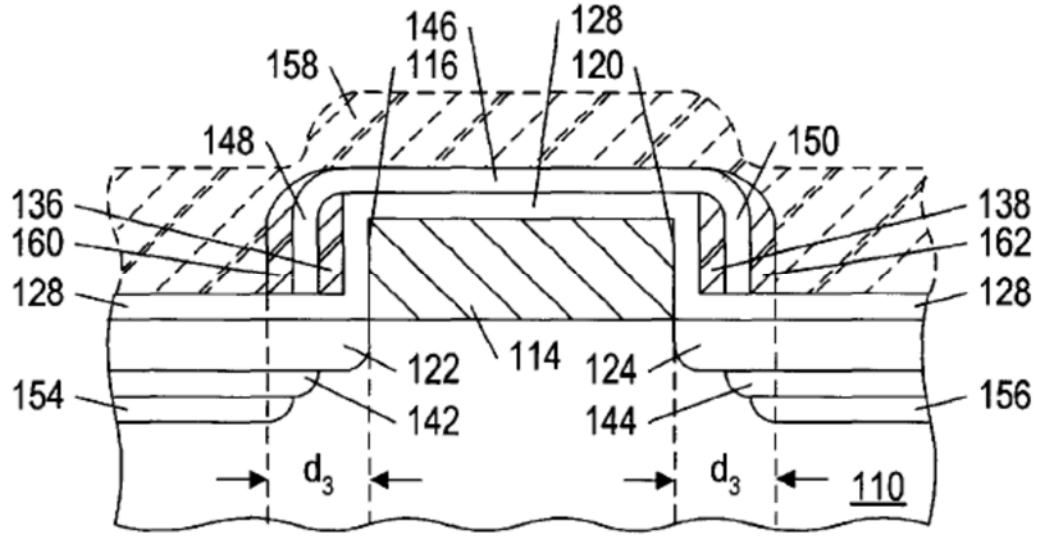


FIG. 11

AMD 680 discloses the limitations of claim 8 as discussed in section X.F. above. For example, Fig. 17 below shows a semiconductor component wherein the

first and second nitride spacers 136/138 and the oxide layer 128 have been removed by an overetching process to expose the first gate sidewall 116 and the second gate sidewall 120. *See* Ex. 1005, ¶227; Ex. 1003, 11:10-14, 56-57, Fig. 17:

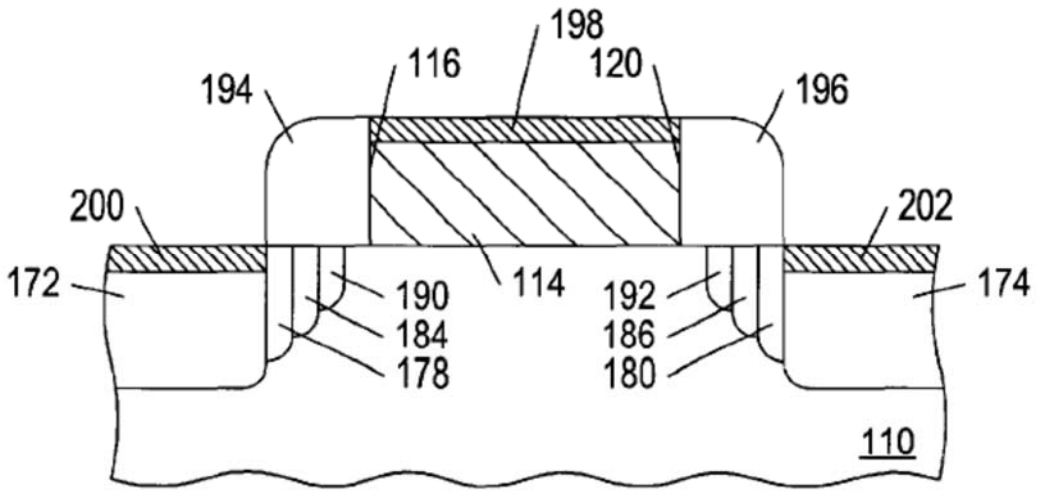


FIG. 17

Thus, AMD 680 discloses each and every limitation recited in dependent claims 2 and 4-8, and as a consequence, anticipates those claims. For at least the foregoing reasons, Petitioner respectfully requests the Board find claims 2 and 4-8 unpatentable.

C. AMD 680 Anticipates Independent Claim 12

AMD 680 discloses each of the limitations recited in independent claim 12 of the ’126 patent. At the outset, AMD 680 discloses the preamble of independent claim 12 as discussed in section X. G. above. *See* Ex. 1003, 1:11-14 (“This invention relates to semiconductor processing and, more particularly, to a method

of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects.").[9]

AMD 680 discloses limitation 12(a) as discussed in section X.G. above. *See, e.g.*, Ex. 1005, ¶230; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

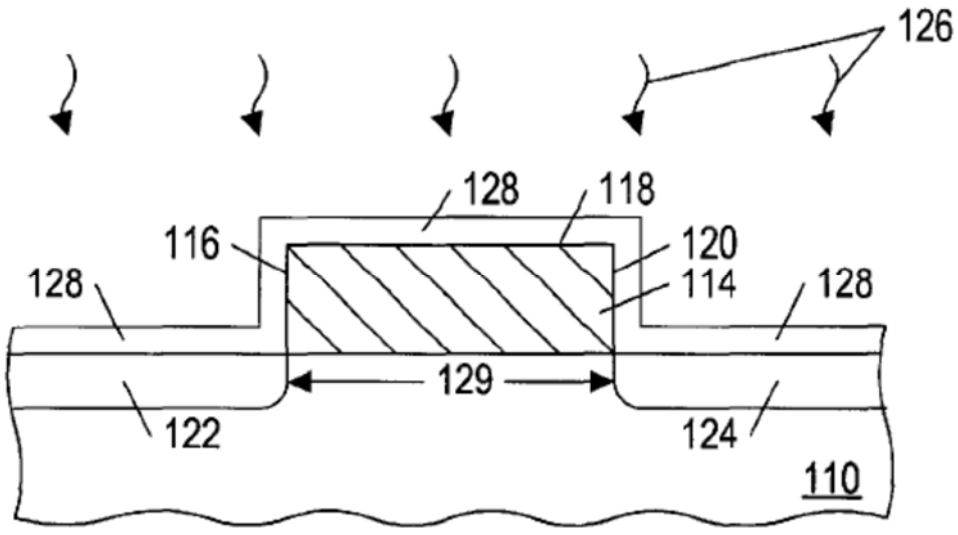


FIG. 6

For example, the semiconductor component disclosed in Fig 6 of AMD 680 above included a semiconductor substrate 110 comprising n-type or p-type doped silicon material of a first conductivity type and having a major surface, at least at the intersection of substrate 110 and oxide layer 128. Ex. 1005, ¶231.

[9] Petitioner's position in this Petition regarding the ordering of the steps in the challenged method claims of the '126 Patent is based on Patent Owner's apparent construction in the related district court litigation that the claimed methods need not be performed in the order listed.

AMD 680 discloses limitation 12(b) as discussed in section X. G. above. For example, the semiconductor component disclosed in Fig 6 above includes a gate structure 114 disposed on substrate 110, the gate structure 114 having a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1003 7:63-67 & Fig. 6 (above); Ex. 1005, ¶232.

AMD 680 discloses limitation 12(c) as discussed in section X. G. above. As shown in Fig. 7 below, AMD 680 discloses a semiconductor component with a first nitride spacer 136 formed adjacent to gate sidewall 116 and a second nitride spacer 138 formed adjacent to gate sidewall 120. *See* Ex. 1005, ¶233; Ex. 1003, 8:23-35 & Fig. 7:

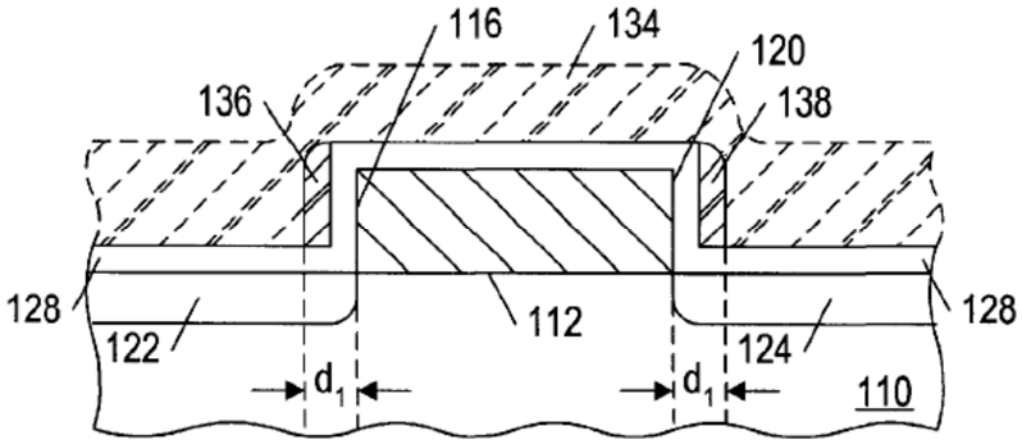


FIG. 7

AMD 680 discloses limitation 12(d) as discussed in section X. G. above. For example, as shown in Fig. 8 below, the semiconductor component includes a first doped region 142 aligned to the first nitride spacer 136 and a second doped

region aligned to the second nitride spacer 138. *See* Ex. 1005, ¶234; Ex. 1003, 8:35-47 & Fig. 8:

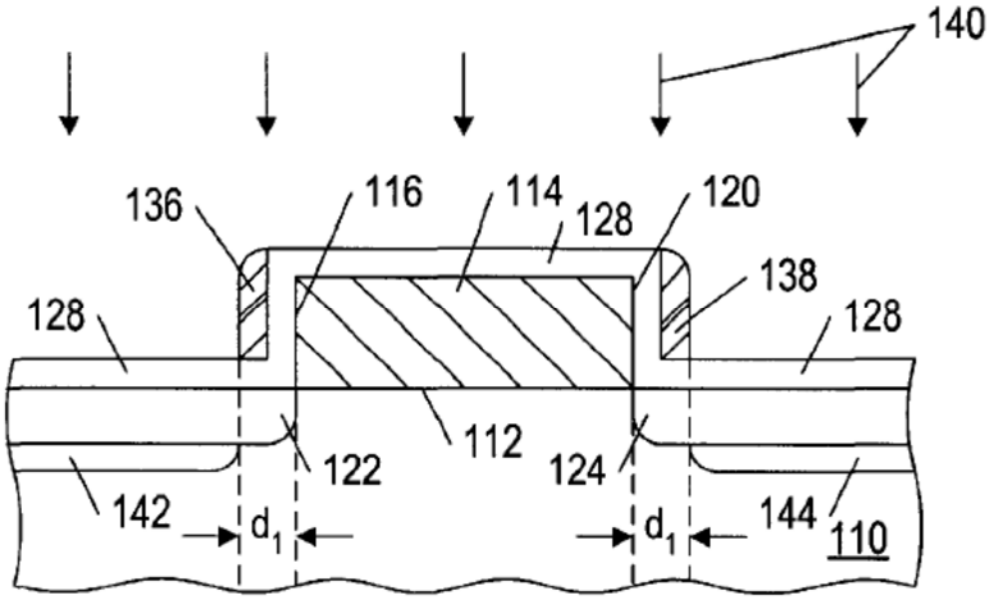


FIG. 8

AMD 680 discloses limitation 12(e) as discussed in section X. G. above. *See* Ex. 1005, ¶235; Ex. 1003, 9:4-14 & Fig. 11:

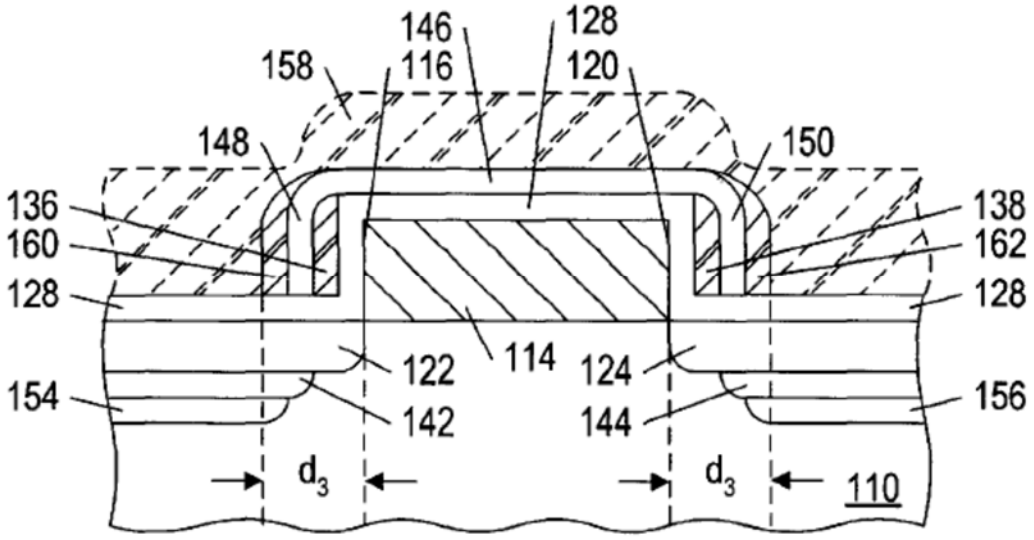


FIG. 11

Fig. 11 above shows a third nitride spacer 160 formed on the side of the first

nitride spacer 136.

AMD 680 discloses limitation 12(f) as discussed in section X.G. above. For example, Fig. 12 below shows a semiconductor device with a third doped region 166 aligned to the third nitride spacer 160. Ex. 1005, ¶236; Ex. 1003, 9:20-34 & Fig. 12:

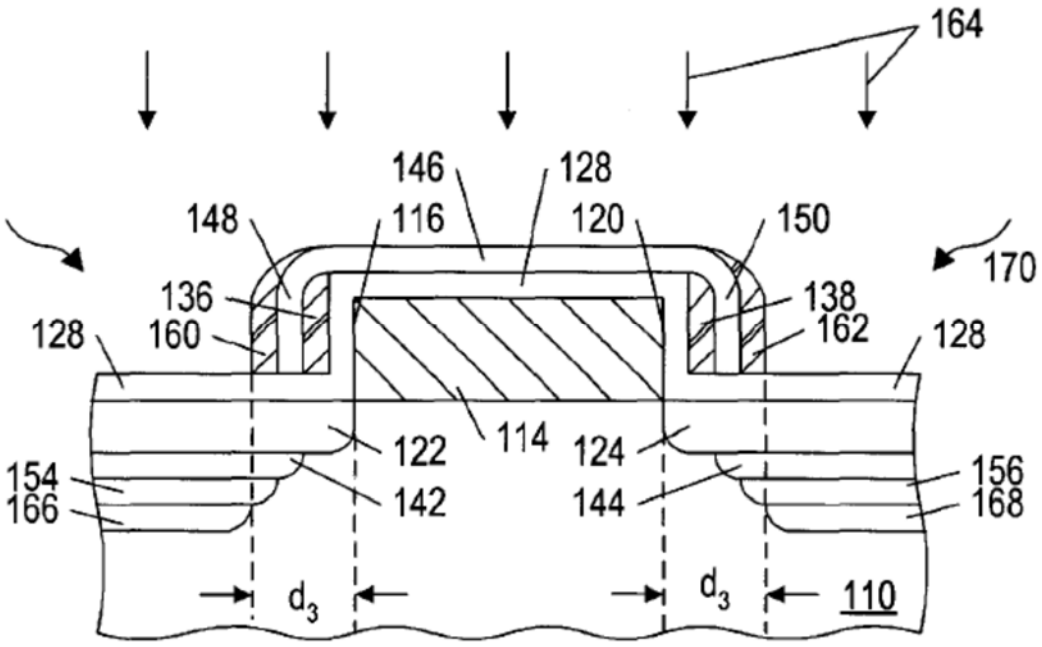


FIG. 12

AMD 680 discloses limitation 12(g) as discussed in section X.G. above. For example, Fig. 12 above shows a semiconductor device with a fourth doped region 168 formed on the right side of the second gate structure 114. Ex. 1005, ¶237; Ex. 1003, 9:20-34 & Fig. 12.

Thus, AMD 680 discloses each and every limitation recited in independent claim 12 of the ’126 patent, and as a consequence, anticipates this claim. For at least the foregoing reasons, Petitioner respectfully requests the Board find claim 12

unpatentable.

D. AMD 680 Anticipates Dependent Claims 14, 16-17 and 19

AMD 680 discloses each and every limitation recited in dependent claims 14, 16-17 and 19 of the ’126 patent. AMD 680 discloses and/or renders obvious the limitations of claim 14. AMD 680 discloses limitation 14(a) as discussed in section X. H. above. *See* Ex. 1003, 8:11-19; Ex. 1004, 8:21-29; Ex. 1005, ¶239. As stated in section X. A. 3. above, forming oxide layers on silicon by growing them in a dry oxygen ambient at temperature ranges between 750ºC and 900ºC was well known at the time of the ’126 patent and would have been an obvious design choice for a POSA. *See* Ex. 1001, 3:22-28: (“A layer of dielectric material 106 is formed on major surface 104. Dielectric layer 106 serves as a gate dielectric material and may be formed by techniques known to those skilled in the art including thermal oxidation, chemical vapor deposition, and the like.”)

AMD 680 discloses the limitations recited in limitations 14(b) and 14(c) as discussed in section X. H. above. For example, as shown in Fig. 7 below, AMD 680 discloses depositing a layer of nitride 134 on the layer of oxide 128 on the gate structure 114 and above the semiconductor substrate 110 which is anisotropically etched to form the first nitride spacer 136 adjacent to the first gate sidewall 116 and the second nitride spacer 138 adjacent to the second gate sidewall 120. *See* Ex. 1005, ¶240; Ex. 1003, 8:23-35 & Fig. 7:

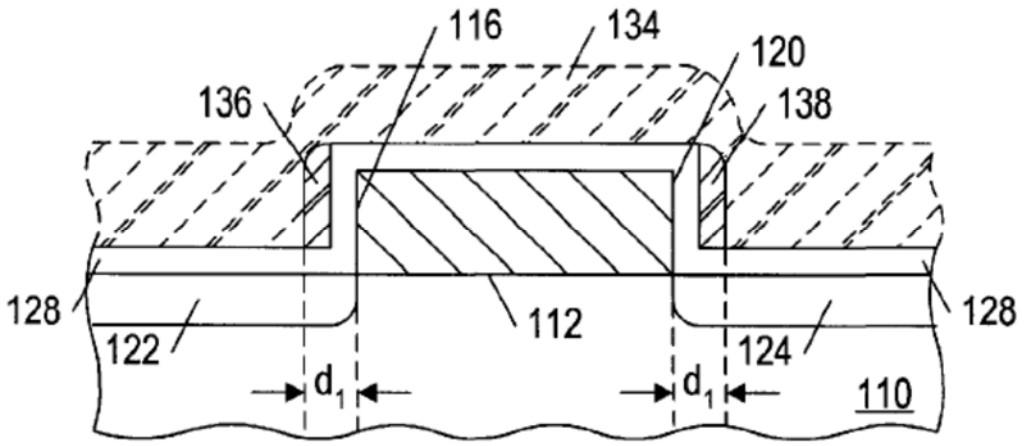


FIG. 7

AMD 680 discloses the limitations recited in claim 16 as discussed in section X. H. above. For example, Fig. 11 below shows a fourth nitride spacer 162 formed on the side of the second nitride spacer 138. *See* Ex. 1005, ¶241; Ex. 1003, 9:4-14 & Fig. 11:

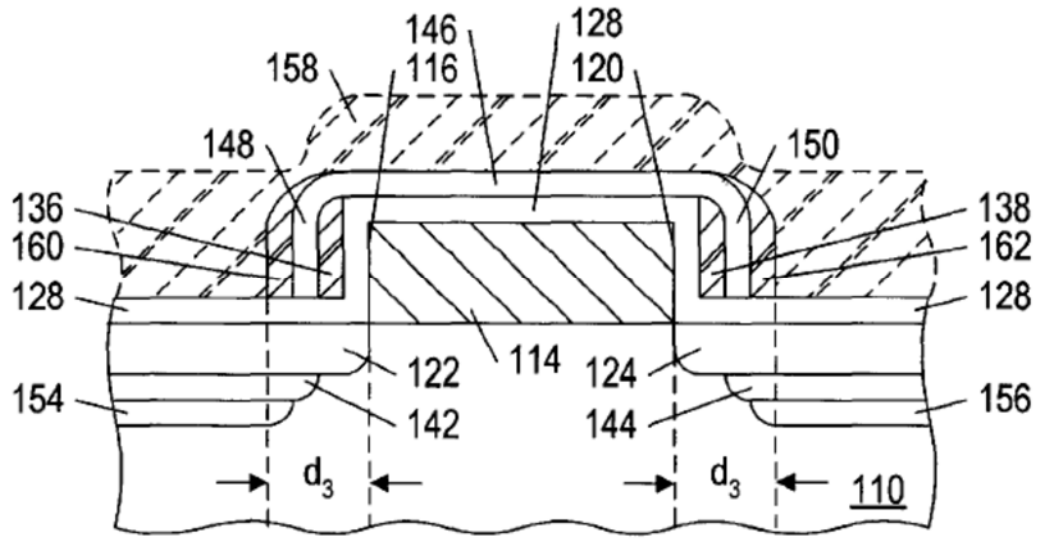


FIG. 11

AMD 680 discloses the limitations of claim 17 as discussed in section X. H. above. For example, Figs. 7 and 11 below show forming the first and second

nitride spacers 136/138 contemporaneously and forming the third and fourth nitride spacers 160/162 contemporaneously.

See Ex. 1005, ¶¶242-43; Ex. 1003, 8:23-35, 9:4-14 & Fig. 7, 11:

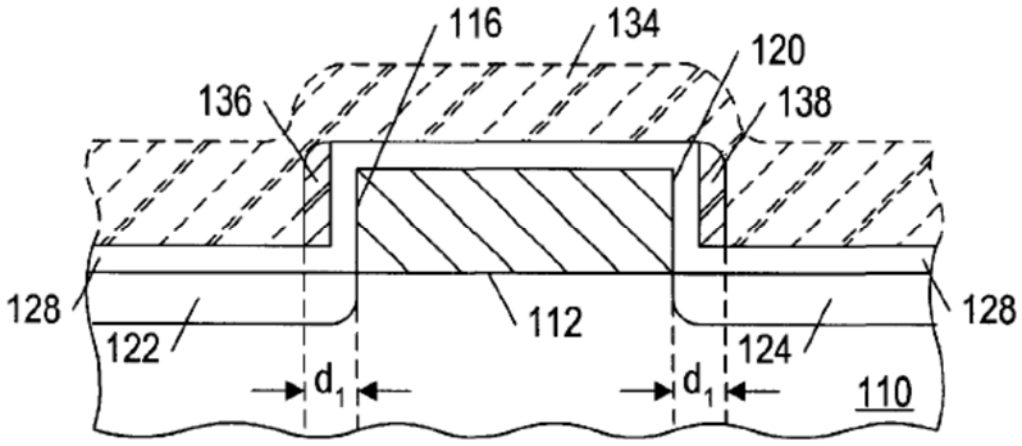


FIG. 7

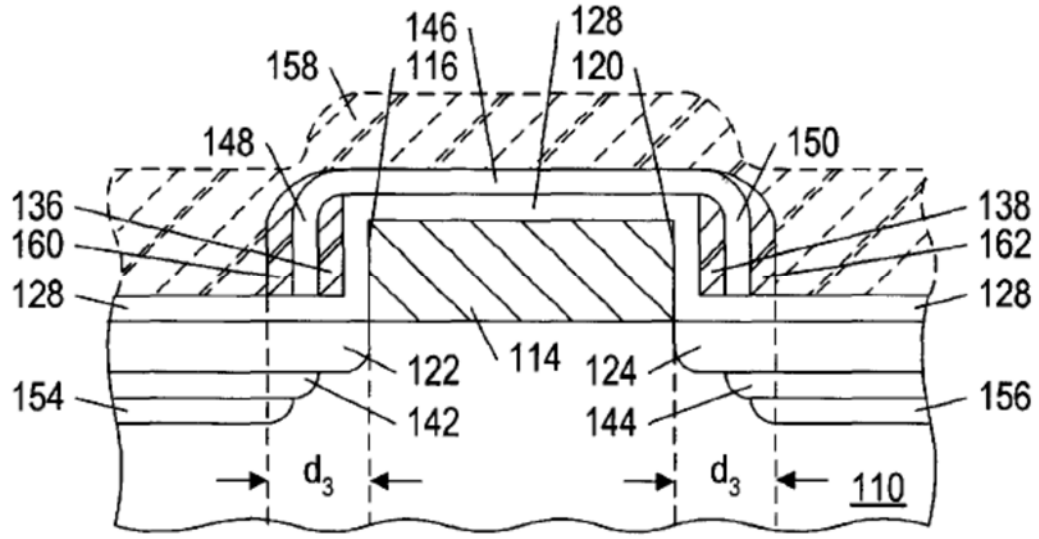


FIG. 11

AMD 680 discloses the limitations of claim 19 as discussed in section X. H. above. For example, Fig. 12 below shows a semiconductor device with a fourth doped region 168 aligned to the fourth nitride spacer 162. Ex. 1005, ¶244; Ex. 1003, 9:20-34 & Fig. 12:

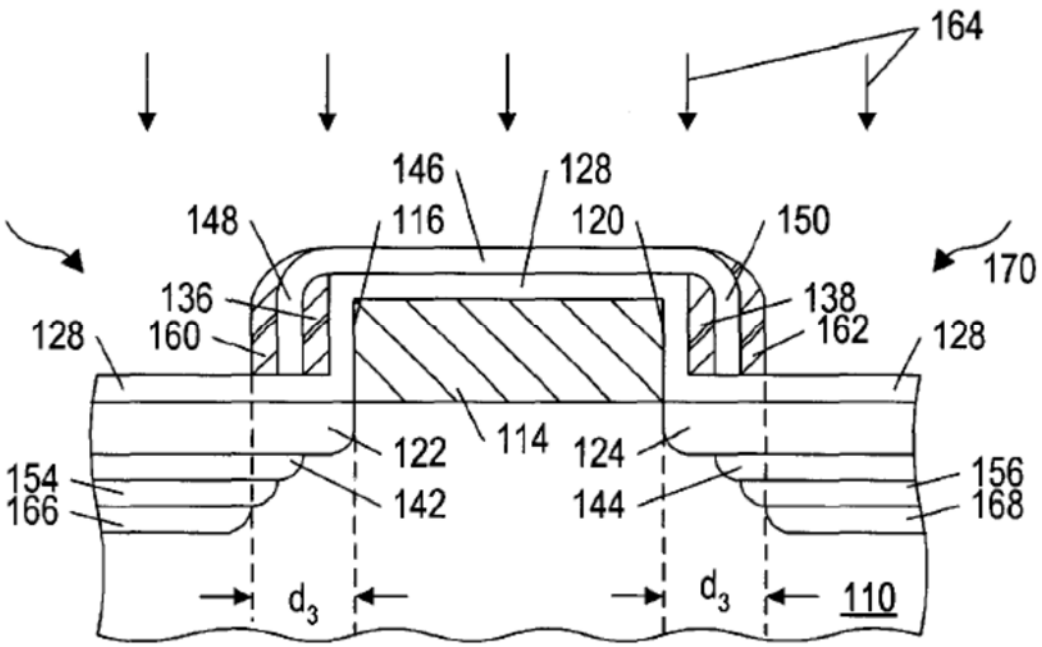


FIG. 12

In accordance with the above, AMD 680 discloses each and every limitation recited in claims 1-2, 4-8, 12, 14, 16-17 and 19, and as a consequence, anticipates those claims. A claim chart for AMD 680 cited against these claims is attached as Exhibit 1008.

For at least the foregoing reasons, Petitioner respectfully requests the Board find dependent claims 1-2, 4-8, 12, 14, 16-17 and 19 of the ’126 patent unpatentable.

XII. ANY SECONDARY CONSIDERATIONS ARE INSUFFICIENT TO OVERCOME THE OBVIOUSNESS OF CLAIMS 1-19.

Patent Owner has the burden of establishing the existence and sufficiency of any secondary considerations of non-obviousness, as well as their nexus and commensurateness with the claims. *Ex parte Gelles*, 22 USPQ2d 1318, 1319 (Bd.

Pat. App. & Inter. 1992); *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731 (Fed. Cir. 2013) ("Where there is a range discloses in the prior art, and the claimed invention falls within that range, the burden of production falls upon the patentee to come forward with evidence that (1) the prior art taught away from the claimed invention; (2) there were new and unexpected results relative to the prior art; or (3) there are other pertinent secondary considerations.) Although secondary considerations must be considered, they do not control the obviousness conclusion. *See Newell Cos., Inc. v. Kenney, Mfg. Co.*, 864 F.2d 757, 768 (Fed. Cir. 1988). And, in cases where a strong *prima facie* obviousness showing exists, the Federal Circuit has repeatedly held that even relevant secondary considerations supported by substantial evidence may not dislodge the primary conclusion of obviousness. *See, e.g., Leapfrog Enters. Inc. v. Fisher-Price Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007). Petitioner is not aware of any secondary considerations that would support the non-obviousness of the challenged claims, and, in any event, the *prima facie* case of obviousness presented herein could not be overcome with any such considerations that Patent Owner may forward. *See id.*

XIII. CONCLUSION

For the foregoing reasons, SMIC respectfully requests *inter partes* review of Claims 1-19 of U.S. Patent No. 6,608,126 and cancellation of those claims as unpatentable.

Respectfully submitted,

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XIV. CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that this Petition complies with the type-volume limitation of 37 C.F.R. § 42.24(a). The word count application of the word processing program used to prepare this Petition indicates that the Petition contains 13,502 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a).

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,806,126, including all exhibits were served on April 14, 2020 via e-mail and Federal Express in its entirety on the correspondence address of record for the '126 Patent shown in USPTO PAIR (no attorney or agent address was listed):

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