UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMIC, AMERICAS,

Petitioner

v.

INNOVATIVE FOUNDRY TECHNOLOGIES, LLC,

Patent Owner

CASE NO.: IPR2020-00839
PATENT NO. 6,933,620

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,933,620

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Exhibit 1016	U.S. Patent No. 6,274,906 to Kim *et al*. ("Samsung 906").
Exhibit 1017	Complaint for Declaratory Judgment, filed on April 2, 2020 in *SMIC, Americas et al. v. Innovative Foundry Technologies, LLC*, No. 3:20-cv-02256-JCS (N.D. Cal.).

I. INTRODUCTION

SMIC, Americas ("SMIC" or "Petitioner") respectfully requests *Inter Partes* Review ("IPR") of claims 1-20 ("Challenged Claims") of U.S. Patent No. 6,933,620 to Luning *et al.*, ("'620 patent") (Ex. 1001) under 35 U.S.C. § 102(b) as anticipated and under 35 U.S.C. §103(a) as obvious in view of the prior art. SMIC is reasonably likely to prevail on the grounds of unpatentability submitted herein with respect to at least one Challenged Claim. The claims of the '620 patent recite nothing more than well-known techniques of (i) using spacers to form graded junctions for the purpose of reducing short-channel effects in semiconductor devices, and (ii) recessing the spacers to increase the amount of exposed silicon surface area for forming silicide on the gate sidewalls of the semiconductor devices for the purpose of reducing gate resistance. The prior art presented in this Petition—U.S. Patent Nos. 6,258,680 ("AMD 680") and 6,235,598 ("Intel 598")—discloses the very same techniques and was not considered during original prosecution. SMIC therefore respectfully requests that the Board institute IPR and cancel claims 1-20 of the '620 patent.

II. MANDATORY NOTICES (37 C.F.R. § 42.8)

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

In accordance with 37 C.F.R. § 42.8(b)(1), Petitioner SMIC is a real party-in-interest. Semiconductor Manufacturing International Corporation, at P.O. Box 2681, Cricket Square, Hutchins Drive, George Town, Grand Cayman KY1-111,

Cayman Islands, ("SMIC Cayman") is a named defendant in the related, co-pending litigation, discussed below, and is a holding company without any operations and does not manufacture, use, sell, offer to sell, or import into the United States any products accused of infringement in the related litigation. Petitioner does not believe that SMIC Cayman qualifies as a real party-in-interest. However, Petitioner identifies SMIC Cayman under 37 CFR § 42.8(b)(1) and confirms that SMIC Cayman is willing to be treated as a real party-in-interest in both this IPR and the related district court litigation, but only because it is a named defendant in that litigation. Petitioner also identifies the following entities as real parties-in-interest: Semiconductor Manufacturing International (Shanghai) Corporation ("SMIC Shanghai"); Semiconductor Manufacturing International (Beijing) Corporation ("SMIC Beijing"); Semiconductor Manufacturing International (Tianjin) Corporation ("SMIC Tianjin"); Semiconductor Manufacturing International (BVI) Corporation ("SMIC BVI"); Semiconductor Manufacturing North China (Beijing) Corporation ("SMNC"); Semiconductor Manufacturing South China Corporation ("SMSC"); Semiconductor Manufacturing International (Shenzhen) Corporation; Broadcom Incorporated and Broadcom Corporation (because they are named defendants in the related litigation and customers of Petitioner); and Cypress Semiconductor Corporation (because it is a named defendant in the related litigation and customer of Petitioner).

B. Related Judicial and Administrative Matters (37 C.F.R. § 42.8(b)(2))

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner states that the '620 patent is currently the subject of the following lawsuit: *Innovative Foundry Technologies, LLC v. SMIC, et al*., No. 6:19-cv-00719-ADA (W.D. Texas), filed December 20, 2019.[1] Petitioner is also filing concurrently herewith a Petition for *Inter Partes* Review of U.S. Patent No. 6,806,126 ("the '126 patent"), which is the parent of the '620 patent. In addition, Petitioner SMIC and SMIC Shanghai, SMIC Beijing, SMIC Tianjin, SMIC BVI, SMNC, and SMSC filed a complaint for a declaratory judgment of non-infringement for the '126 and '620 patents (among others) on April 2, 2020 in *SMIC, Americas et al. v. Innovative Foundry Technologies, LLC*, No. 3:20-cv-02256-JCS (N.D. Cal.).[2]

C. Lead and Back-Up Counsel (37 C.F.R. § 42.8(b)(3)) and Service Information (37 C.F.R. § 42.8(b)(4))

In accordance with 37 C.F.R. § 42.8(b)(3), Petitioner provides the following designation of counsel. Concurrently filed is a Power of Attorney pursuant to 37 C.F.R. § 42.10(b). In accordance with 37 C.F.R. § 42.8(b)(4), Petitioner identifies the following service information:

[1] A copy of the Complaint is attached as Exhibit 1010.

[2] A copy of the Complaint is attached as Exhibit 1017.

Lead Counsel	Back-up Counsel
Cheng (Jack) Ko (Reg. No. 54,227) PILLSBURY WINTHROP SHAW PITTMAN LLP Suite 4201, Bund Center 222 Yan An Road East Huangpu District, Shanghai 200002 China Telephone: +86.21.6137.7999 Facsimile: +86.21.6137.7900 Email: jack.ko@pillsburylaw.com	**Christopher Kao** (*Pro hac vice* motion to be filed once authorized) **Brock S. Weber** (*Pro hac vice* motion to be filed once authorized) PILLSBURY WINTHROP SHAW PITTMAN LLP Four Embarcadero Center, 22nd Floor San Francisco, CA 94111 Telephone: 415.983.1000 Facsimile: 415.983.1200 Email: christopher.kao@pillsburylaw.com brock.weber@pillsburylaw.com **Matthew W. Hindman** (Reg. No. 57,396) PILLSBURY WINTHROP SHAW PITTMAN LLP 2550 Handover Street Palo Alto, CA 94304 Telephone: 650.233.4087 Facsimile: 650.233.4545 Email: matthew.hindman@pillsburylaw.com

SMIC consents to electronic service.

III. GROUNDS FOR STANDING (37 C.F.R. § 42.104(a))

Pursuant to 37 C.F.R. § 42.104(a), SMIC certifies that the ’620 patent is available for IPR and that SMIC is not barred or estopped from requesting IPR challenging claims 1-20 of the ’620 patent on the grounds identified in this Petition.

IV. PAYMENT OF FEES (37 C.F.R. § 42.15(a) and § 42.103)

The required fees are submitted herewith in accordance with 37 C.F.R. §§ 42.103(a) and 42.15(a). If any additional fees are due during this proceeding, the Office is authorized to charge such fees to Deposit Account No. 033975 (058559.0000002). Any overpayment or refund of fees may also be deposited into this Deposit Account.

V. BACKGROUND OF THE TECHNOLOGY

For decades semiconductor manufacturers have sought new ways to reduce device sizes so that more devices can be formed on a single silicon wafer. *See* Ex. 1005, ¶70; Ex. 1001 ('620 patent), 1:16-20 ("Semiconductor device manufacturers are constantly improving device performance while lowering their cost of manufacture. One way manufacturers have reduced costs has been to shrink the sizes of the devices so that more devices can be made from a single semiconductor wafer."). Reducing semiconductor device sizes generally results in improved performance and lower manufacturing costs. *Id*., 1:21-27.

However, there are adverse effects that come with shrinking device sizes. These adverse effects include effects referred to as "short channel effects." Ex. 1001, 1:21-27; Ex. 1005, *id*. Some examples of short-channel effects include (i) a decrease in source-drain breakdown voltage of the semiconductor device and (ii) an increase in junction capacitance of the device. *Id*. Each of these effects can

be harmful and degrade device performance, potentially resulting in instability of the device's threshold voltage. *Id*.

One method of mitigating short-channel effects in semiconductor devices is to configure spacers along the sidewalls of the gate structures in these devices to form a graded junction between the drain and channel regions. *See* Ex. 1005, ¶71; Ex. 1003 (AMD 680), 3:48-4:7, 8:35-47 & Fig. 8. The spacers are used as masks for implanting or depositing different doping concentration profiles into different areas of the semiconductor substrate beneath the spacers in these devices. *Id*. The different doping concentrations are spaced apart at different offsets from the gate structure to form a graded junction. *Id.* The different spaced offsets are delineated by the relative thicknesses of the spacers. *Id.* As a result, a graded junction is formed having higher doping concentration regions formed outside of lower concentration regions, relative to the channel region of the device. *Id.*, 4:65-5:1; Ex. 1005, *id.* A graded junction is used for the purpose of reducing short-channel effects in these devices. *Id.*, 4:55-60.

This technique of using spacers to form graded junctions in semiconductor devices was well-known and conventional in the field at the time of the '620 patent. Ex. 1005, ¶72. For example, U.S. Patent No. 6,274,906 ("Samsung 906" – Ex. 1016) discloses a semiconductor manufacturing process using spacers formed along the gate sidewalls of a metal-oxide-semiconductor ("MOS") transistor to

create a graded junctions in the same configuration as disclosed in the ’620 patent. *See id.* *See* Ex. 1016, Abstract, 3:11-45 & Fig. 1:

FIG. 1

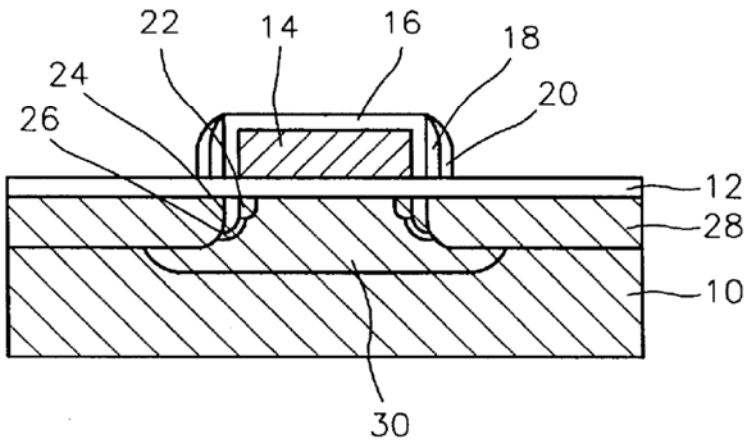


Fig. 1 above shows a first pair of spacers 18 formed around the gate electrode 14 in contact with the gate sidewalls and a second pair of spacers 20 in contact with the first pair of spacers 18. The spacers are used as masks for implanting different doping concentration profiles 22, 24 and 26 into different areas of the semiconductor substrate 10. *Id.* The doping concentrations 24 and 28 are aligned with spacers 18 and 20 respectively at different offsets from the gate structure to form a graded junction. *Id.* As a result, a graded junction is formed having higher doping concentration regions formed outside of lower concentrations regions relative to the channel region of the device.

U.S. Patent No. 6,498,067 ("TSMC 067" – Ex. 1011) also discloses a semiconductor manufacturing process for forming multi-layer nitride spacers on the sidewalls of a gate structure of a MOSFET[3] device to form graded junctions in the same configuration as disclosed in the '620 patent. Fig. 7 below shows a gate structure 3, oxide layers 5 formed on the gate sidewalls, a first pair of nitride spacers 6b in contact with the oxide layers, and a second pair of nitride spacers 8b in contact with the first pair of nitride spacers 6b. *See* Ex. 1005, ¶74; Ex. 1011, Fig. 7:

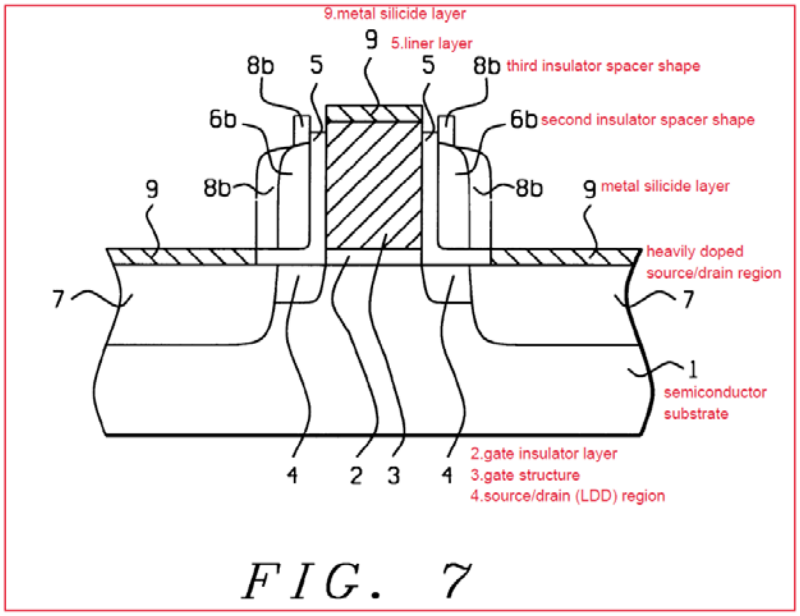


FIG. 7

The spacers are used to form a graded junction comprised of lightly doped source/drain (LDD) regions (4) adjacent to heavily doped source/drain regions (7).

[3] Metal-oxide-semiconductor field-effect transistor (MOSFET).

See id., 3:43-50, 5:5-12 & Fig. 7; Ex. 1005, ¶75. The spacers also reduce the risk of gate leakage or short circuits that can occur during salicide formation. Ex. 1001, Abstract; Ex. 1005, *id.*

U.S. Patent No. 6,596,576 ("AMI 576" – Ex. 1012) also relates to a semiconductor manufacturing process for forming multi-layer nitride spacers on the sides of a MOSFET gate structure in a configuration very similar to the one in the '620 patent. As shown in Fig. 12 below, AMI 576 discloses a method of fabricating a semiconductor device with a gate structure 401-403, a pair of silicon dioxide liners 404 formed against the gate structure, a first pair of silicon nitride layers 405 in contact with the silicon dioxide liners 404, and a second pair of silicon nitride layers 406 in contact with the first silicon nitride layers 405. *See, e.g.*, Ex. 1005, ¶¶76-77; Ex. 1012, Abstract, 5:20-64 & Fig. 12:

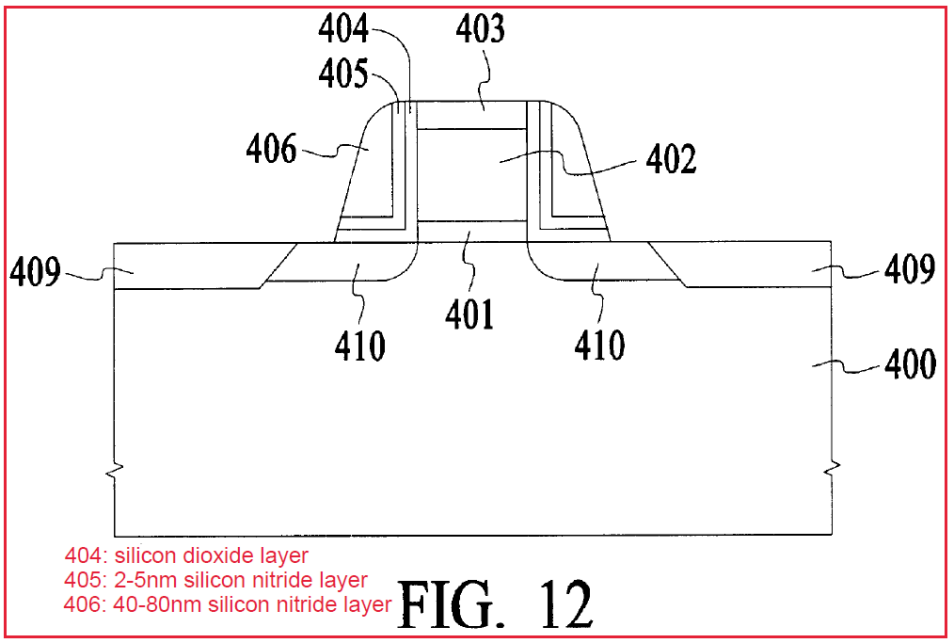


FIG. 12

In AMI 576, a barrier layer is formed over the oxide layer 404 before the silicon nitride spacers 405 and 406 are formed to reduce, or prevent altogether, diffusion of the hydrogen absorbed by the silicon nitride spacers into the gate oxide and channel during low temperature chemical vapor deposition of the silicon nitride. *Id.*

Further, U.S. Patent No. 6,225,176 ("AMD 176" – Ex. 1013) concerns a method of manufacturing a semiconductor device with multiple nitride spacers for reducing short-channel effects in the same manner as the '620 patent. *See* Ex. 1005, ¶78; Ex. 1013, Fig. 1:

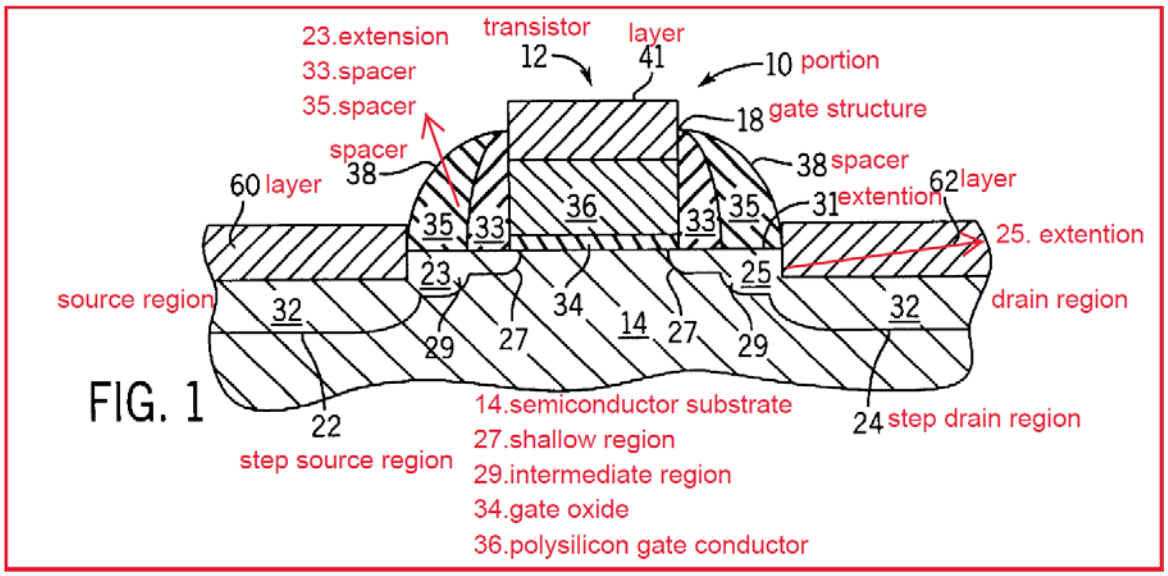


Fig. 1 above shows a semiconductor transistor device 12 having two pairs of nitride spacers 33/35 adjacent to a gate structure 36 and source/drain doped regions (22, 23, 24, 25 and 27) of varying depths forming a graded junction. *See* Ex. 1001, 3:59-4:25 & Fig. 1; Ex. 1005, ¶79. The multiple nitride spacers are used to form a

graded junction for the purpose of reducing short-channel effects in the semiconductor transistor device. *Id*.

The adverse effects that come with shrinking semiconductor device sizes also include increased difficulty in forming silicide on the smaller gate structures in such devices which leads to increased gate resistance because gate resistance is dependent upon the amount of gate silicon surface area available for silicide formation. Ex. 1001, 1:34-40, 62-65; Ex. 1005, ¶80.

U.S. Patent No. 6,383,882 ("Samsung 882" – Ex. 1014) concerns a method of manufacturing a metal-oxide-semiconductor (MOS) semiconductor transistor device that includes recessed nitride spacers to increase the exposed area of the gate silicon surface area for silicide formation in the same manner as in the '620 patent. Ex. 1005, ¶81; Ex. 1014, Abstract & Fig. 11:

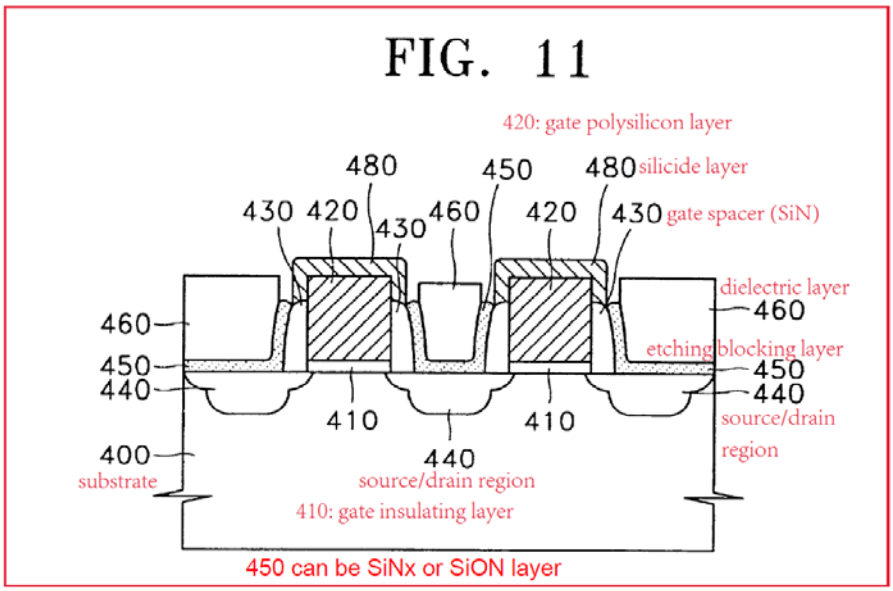


Fig. 11 above shows a MOS transistor device with two gate structures 420 having pairs of nitride spacers 430 that are recessed from the top surface of the gate structure to increase the silicon surface area for improved silicide formation 480. Ex. 1001, *id*.; Ex. 1005, ¶82.

U.S. Patent No. 6,291,354 ("UMC 354" – Ex. 1015) also concerns a method of manufacturing a semiconductor device with recessed nitride spacers to increase the exposed silicon surface area on the gate electrode for improved silicide formation. *See* Ex. 1005, ¶83; Ex. 1015, Figs. 4D & 4E:

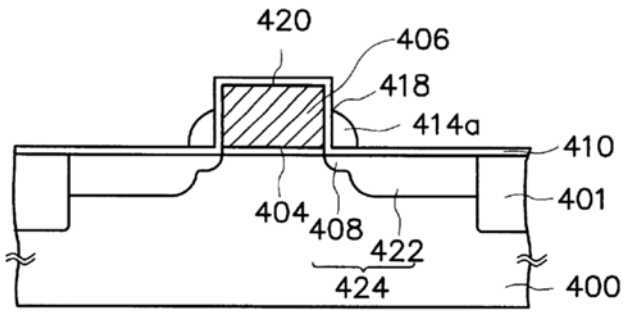


FIG. 4D

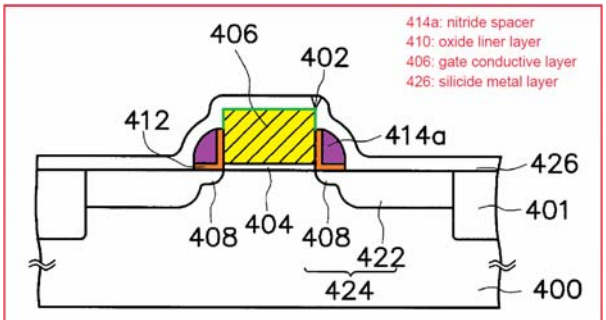
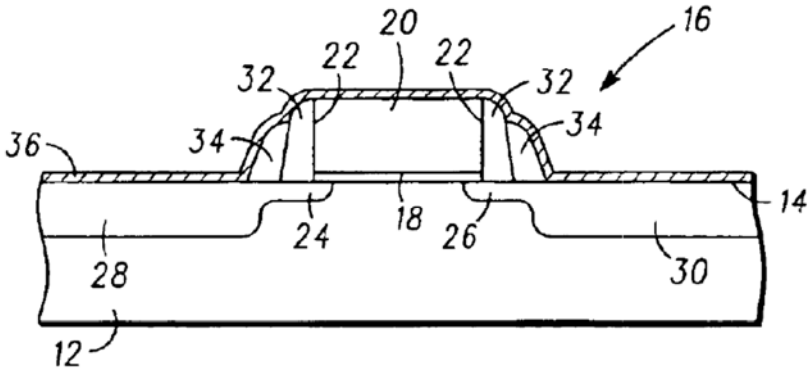


FIG. 4E

As shown in Figs. 4D and 4E above, a pair of nitride spacers 414a and oxide liner layers 410 are recessed from the top surface of the sidewalls of the gate structure 406, thereby exposing the upper portions of the sidewalls and increasing the gate silicon surface area for silicide formation 426. *See* Ex. 1001, *id*.; Ex. 1005, ¶84.

VI. THE ’620 PATENT

The ’620 patent relates to a known technique for reducing short-channel effects. Fig. 1 of the ’620 patent shows that a prior art solution to these short-channel effects was to position spacers made of oxide and/or nitride adjacent to the gate structure of a semiconductor device and to implant doping agents of different concentrations in the substrate beneath the spacers at different offsets from the gate structure to form a graded junction in the semiconductor device. *See* Ex. 1005, ¶86; Ex. 1001, 1:40-55 & Fig. 1:



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-Prior Art-
Fig. 1

As shown above, the semiconductor device 16 includes a gate 20, gate oxide 18, oxide spacers 32 adjacent to gate 20, nitride spacers 34 adjacent oxide spacers 32, and graded source regions 24/28 and graded drain regions 26/30. Ex. 1001, *id*. A layer of refractory metal 36 is formed on gate structure 20, source region 28, and drain region 30. *Id.* Silicide forms on the exposed portions of the gate 20 and source and drain regions 28 and 30 in contact with the metal layer 36. *See id.*, 1:55-60; Ex. 1005, ¶87. The pairs of spacers 32/34 act as masks for the purpose of

implanting doping agents of different concentrations into the semiconductor substrate 12 beneath the spacers at different offsets from the gate structure 20 to form a graded junction in the semiconductor device. Ex. 1005, *id.*

Prior art solutions used graded junctions to soften the abruptness of the change in electric field between the drain and channel regions of semiconductor devices. *See, e.g.*, Ex. 1003, 3:6-7, 21-33, 5:1-9; Ex. 1005, ¶88. A graded junction introduces a more gradual change in the doping concentration profile in drain regions 24/28 and source regions 26/30 that reduces the electric field near the drain side of the channel area. *Id*. A smoother doping profile produces a smoother voltage drop at the channel/drain junctions, thus reducing the electrical field. *Id*. The graded junction arrangement acts to minimize the peak drain-to-channel electric field, and thus mitigates short-channel effects. *See* Ex. 1001, 1:27-30 & Fig. 1; Ex. 1005 *id*.

Referring back to Fig. 1 above, the spacers 32/34 are used in forming the graded junction to isolate the different regions of the device so that different doping concentration profiles can be applied at different offsets a spaced distance apart from the sidewalls of the gate structure 20. *Id*., 1:48-55 & Fig. 1; Ex. 1005, ¶89. Spacers 32/34 act as a mask to offset different doping concentrations for different regions of the device. *See, e.g. id.*, claims 18-19 (8:34-45).

The spaced distances of these offsets are delineated by the thickness of each of the pairs of spacers. Ex. 1001, *id.;* Ex. 1005, ¶90. This method results in the structure shown in Fig. 1 of the ’620 patent, wherein the source/drain regions 24/26 aligned with oxide spacers 32 have a lower doping concentration profile than the source/drain regions 28/30 aligned with the nitride spacers 34. *Id*.

The other problem the ’620 patent purports to address is the one that arises with reduced silicon surface area on gate structures in semiconductor devices resulting from reduced semiconductor device sizes. *See id.*, 1:34-40; Ex. 1005, ¶91. The ’620 patent purports to focus specifically on lowering gate resistance in semiconductor devices that have reduced gate widths. *See* Ex. 1001, 1:66-2:3; Ex. 1005 *id.* Any decrease in device gate width results in less surface area of exposed silicon, which makes it more difficult to form silicide on the gate structure. *Id*., 1:34-40, 1:62-65; Ex. 1005, *id*. Silicide formation is important because it facilitates conduction of charge carriers across the gate, thus lowering gate resistance and improving device performance. *Id.*

According to the ’620 patent, this problem is compounded in semiconductor devices that use spacers to form graded junctions because spacers obstruct silicide formation on the gate sidewalls, further reducing the exposed silicon available for silicide formation. In such cases, the silicide can only form on the top of the gate structure. Ex. 1001, 1:60-65; Ex. 1005, ¶92.

The ’620 patent concerns a method of manufacturing semiconductor devices that purports to solve this problem by recessing the spacers to reduce their obstruction of the gate sidewalls to increase the surface area of exposed gate silicon available for silicide formation. Ex. 1005, ¶93; Ex. 1001, 3:1-6, 4:66-5:1.

The ’620 patent uses spacers made of the same material so they can be recessed together with a single over-etch step. Ex. 1005, ¶94; Ex. 1001, 4:65-5:6; 5:2-10 & Fig. 7 (below). In Fig. 7, spacers 118/128 disposed adjacent to gate 108A are recessed to expose additional silicon gate material on the upper portion of sidewalls 115 and 117. *Id.* Silicide can then be formed thereon to reduce the overall gate resistance. *Id.*, 2:41-46; Ex. 1005, *id.*

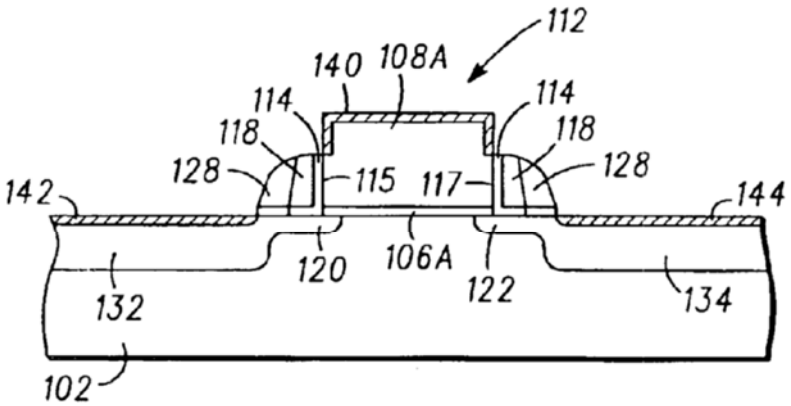


Fig. 7

VII. PROSECUTION HISTORY OF THE ’620 PATENT

The ’620 patent issued from U.S. Patent Application No. 10/915,638 (“the ’638 application”) filed on August 9, 2004, and claims priority as a division of application No. 10/236,200 (“200 application) filed September 6, 2002, now U.S.

Patent No. 6,806,126 ("the '126 patent"). Ex. 1001. The earliest effective filing date for the '620 patent is September 6, 2002, which Petitioner uses for this Petition only, while reserving the right to contest this claim to priority in the related litigation. A copy of the prosecution history of the '620 patent is attached as Exhibit 1002.

On August 9, 2004, the applicant filed an information disclosure statement. *See* Ex. 1002 ('620 Pat. Pros. History), Information Discl. Stmt. dated 8/9/04. On that same day, the applicant also filed a preliminary amendment. *See id*., Prelim. Amendment dated 3/30/05. The preliminary amendment set forth amendments to address a few minor issues in the claims and added new claims 26-39.

A first Office Action issued on January 13, 2005. The Office Action objected to pending claims 24, 31 and 35-36 and rejected pending clams 20-23, 25-34 and 37-39 under 35 U.S.C. §103(a) on grounds of being unpatentable over U.S. Patent No. 5,879,999 to Park et al. ("Park") in view of U.S. Patent No. 6,770,516 to Wu et al. ("Wu"). *See id.*, Office Action dated 1/13/05.

The applicant filed an Amendment on March 30, 2005 in which the rejections of claims 20-21, 25, 27-28, 32 and 37-39 were traversed. *See id.*, Amendment dated 3/30/05. The applicant argued in support of the patentability of claim 20 over the combination of Park and Wu—asserting that the references failed to disclose (i) a first nitride spacer spaced apart from the gate structure by an

oxide layer having a thickness of less than 100 Angstroms, (ii) a first doped region in the semiconductor material aligned to the first nitride spacer, and (iii) a second nitride spacer adjacent to the first nitride spacer. *Id*.

A Notice of Allowance issued on April 19, 2005 in which all pending claims 20-39 were allowed and the '638 application issued as the '620 patent on August 23, 2005. *See id*., Notice of Allowance dated 4/19/05. The Examiner stated that the Park and Wu references failed to teach a first nitride spacer spaced apart from the gate structure by an oxide layer having a thickness of less than 100 Angstroms. *See* Examiner's Stmt. of Reasons for Allowance:

> None of the references of record teaches or suggests the claimed Semiconductor Component and Method of Manufacture having a first nitride spacer spaced apart from the gate structure by an oxide layer.

Id., 2.

The '620 patent issued on August 23, 2005. A request for a certificate of correction was later submitted on September 6, 2005 to change the word "suicide" to "silicide" in issued dependent claim 11.

The prior art presented in this Petition—AMD 680 (Ex. 1003) and Intel 598 (Ex. 1004)—were not cited or discussed during prosecution of the '620 patent.

VIII. CLAIM CONSTRUCTION

The claim construction standard used for claims subject to IPR is the standard set forth in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) and its

progeny, which is the same standard used to construe claims in civil actions in federal district court. 37 C.F.R. § 42.100(b). Petitioner contends that, unless otherwise specifically noted herein, the terms and phrases recited in the claims of the '620 patent are accorded their ordinary and customary meaning that they would have to one of ordinary skill in the art at the time of the invention.

Petitioner's interpretation of the claim terms in the '620 patent is further explained for each claim limitation in relation to the prior art discussed in the proposed grounds for invalidity, below. Under the *Phillips* standard and for clarity, Petitioner provides the following proposed claim construction believed to be relevant to this Petition.[4]

A. "silicide" means "silicide, salicide and/or polysilicide"

Dependent claims 4, 10 and 15 recite the claim term "silicide." A person of ordinary skill in the art ("POSA") would understand the term "silicide" in the context of the '620 patent to refer to "silicide, salicide and/or polysilicide." Silicides can be self-aligning or non-self-aligning. Ex. 1005, ¶101. If a silicide is self-aligning, it may be called "salicide." *Id*. "Salicide" is a compaction of the phrase "self-aligned silicide." *Id*. Self-aligned means that the electrical contacts

[4] Petitioner does not concede that the challenged claims are valid under 35 U.S.C. § 112.

can be formed on the semiconductor component without requiring a photolithography patterning process, as opposed to a non-aligned technology such as "polycide" (also referred to as "polysilicide"). *Id*. The term refers to microelectronics technology used to form electrical contacts between semiconductor components and their metal interconnections. The silicide process involves a reaction of a metal thin film with silicon material, forming a metal silicide contact through a series of annealing (i.e., heating at high temperatures) and/or etch processes. *See* Ex. 1001, 5:43-48, 57-59; Ex. 1005, *id*.

IX. STATEMENT OF PRECISE RELIEF REQUESTED FOR EACH CLAIM CHALLENGED

A. Claims for Which Review is Requested

SMIC requests IPR under 35 U.S.C. § 311 of claims 1-20 of the '620 patent and cancellation of those claims as unpatentable.

B. Statutory Grounds of Challenge

SMIC requests IPR of claims 1-20 of the '620 patent in view of the following references, each of which is prior art to the '620 patent under 35 U.S.C. § 102(b):

Ground	Proposed Rejections for the ’620 patent	Exhibit Number(s)
1	Claims 1-20 would have been obvious under 35 U.S.C. §103 over AMD 680 (Ex. 1003) in view of Intel 598 (Ex. 1004).	**1003, 1004**
2	Claims 7-9, 12, 14 and 16-20 are anticipated by AMD 680 (Ex. 1003) under 35 U.S.C. § 102(b).	**1003**
3	Claims 1-3, 7-9, 12-14 and 16-20 would have been obvious under 35 U.S.C. §103 over AMD 680 (Ex. 1003) in view of the knowledge of one of ordinary skill in the art.	**1003**

C. Level of Ordinary Skill in the Art

A POSA concerning the ’620 patent would have had an undergraduate degree in electrical engineering or related field with two to four years of experience in semiconductor process technology, or a master’s degree with one or more years of experience in the field, or equivalent combination of education and experience. Ex. 1005, ¶69.

D. Overview of the Challenge of the Patentability of Claims 1-20

As set forth above, using spacers to form graded junctions for the purpose of reducing short-channel effects in semiconductor devices was not new at the time of the’620 patent; nor was recessing the spacers for the purpose of increasing the amount of exposed silicon surface area on the gate sidewalls to improve silicide formation for the purpose of reducing gate resistance in the semiconductor device.

Prior art that was not considered by the Examiner during prosecution discloses the very same claimed configuration of nitride spacers used for reducing short-channel effects and gate resistance in semiconductor devices.

X. GROUND 1: CLAIMS 1-20 ARE OBVIOUS OVER AMD 680 IN VIEW OF INTEL 598

Obviousness is a question of law based upon several factual inquires; namely, the scope and content of the prior art, the differences between the prior art and the claimed invention, the level of ordinary skill in the art, and secondary considerations of nonobviousness. *Graham v. John Deere Co*., 383 U.S. 1, 17-18 (1966); *see also Al-Site Corp. v. VSI Int'l Inc*., 174 F.3d 1308 (Fed. Cir. 1999). To prove obviousness, a challenger must show "prior art references which alone or combined with other references would have rendered the invention obvious to one of ordinary skill in the art at the time of invention." *Al-Site Corp.*, 174 F.3d at 1323. The combined references must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991), *see also In re Royka*, 490 F.2d 981 (C.C.P.A. 1974).

The U.S. Supreme Court decision in *KSR International Co. v. Teleflex Inc., et al*., 127 S. Ct. 1727 at 1739 (2007) ("*KSR*") held that a claimed invention can be obvious even if there is no teaching, suggestion, or motivation for combining the prior art to produce that invention. *KSR* holds that patents that are based on combinations of elements or components already known in a technical field may

be found to be obvious. In *KSR*, the Supreme Court emphasized the principle that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id*., 1739. A key inquiry is whether the "improvement is more than the predictable use of prior art elements according to their established functions." *Id.*, 1740.

Using this legal framework established by the Supreme Court in both *Graham v. Deere* and *KSR*, Petitioner submits that the challenged claims 1-20 represent nothing more than a known prior art technique of using spacers to reduce short-channel effects in semiconductor devices.

A. The Scope And Content Of The Prior Art

1. AMD 680 (Ex. 1003)

U.S. Patent No. 6,258,680 ("AMD 680") qualifies as prior art to the '620 patent under 35 U.S.C. § 102(b). Ex. 1003. AMD 680 discloses a method of manufacturing a semiconductor device comprised of a sequence of interposed pairs of oxide and nitride spacers formed on either side of the sidewalls of the gate structure that were used to form a graded junction with a relatively smooth doping concentration profile. *See* Ex. 1003, at 4:56-5:9, 9:48-53; Ex. 1005, at ¶103. The purpose of smoothing the doping profile is to minimize the abruptness of the voltage change at the junction, thus reducing the electric field at the junction. *Id.*, 3:6-7, 21-33. This, in turn, reduces the short-channel effects in the device. *Id.*,

5:1-9, 25-28; 9:53-55. Dispersing abrupt voltage changes reduces the strength of the electric field and the associated harmful short-channel effects. *See id*., 3:23-23, 9:56-59; Ex. 1005, *id*.

In AMD 680, nitride spacers are used as a mask for an ion implantation doping process to produce devices with a graded junction profile. *See id.*, 9:20-33, 48-53 & Fig. 12:

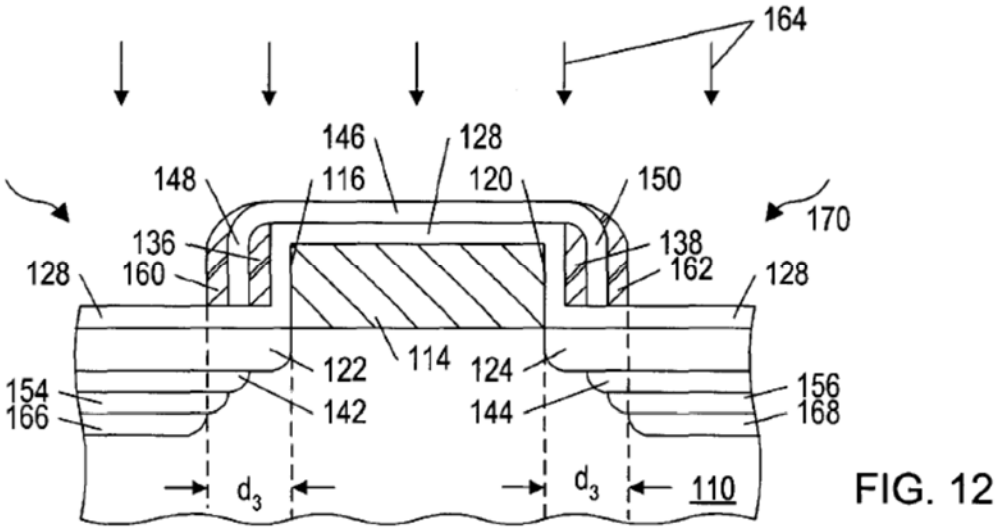


FIG. 12

As depicted above, the device includes a thermal oxide liner 128, nitride spacers 136/138 and 160/162 formed on either side of gate 114, and oxide spacers 148/150 interposed among the nitride spacers. *Id*., 5:42-45. Dielectrics of dissimilar etch characteristics are interposed among the nitride spacers, allowing the pairs of spacers to be individually removed using a selective etch process. *Id.*, 5:57-65, 6:1-4; Ex. 1005, at ¶105.

The source/drain regions are doped with n-type or p-type doping agents. *Id.*,

1:36-37; Ex. 1005, at ¶106. Doping agents of different concentration profiles are implanted into the source/drain regions of the semiconductor substrate 110 at different spaced distances offset from the gate sidewalls 116/120 in accordance with the relative thicknesses of the nitride spacers. *Id.*, at Abstract, 5:47-50; 6:4-9. As a result, a graded junction is formed having higher doping concentration regions formed outside of lighter doping concentration regions to form a graded junction for the purpose of reducing short-channel effects in the semiconductor component. *Id*., Abstract, 4:65-6:1; Ex. 1005, *id*.

Fig. 12, depicted above shows the ion implanted doping concentration profiles 142/144 and 166/168 aligned with the nitride spacers 136/138 and 160/162, respectively. *See id*., Fig. 12 (reproduced above).

2. Intel 598 (Ex. 1004)

U.S. Patent No. 6,235,598 ("Intel 598") qualifies as prior art to the '620 patent under 35 U.S.C. § 102(b). Ex. 1004. Intel 598 discloses a method of manufacturing semiconductor devices for improved polycide resistance. *Id*., 1:6-11. Like the '620 patent, the solution in Intel 598 concerns lowering the increased gate resistance in devices with reduced gate widths resulting from inadequate silicide formation on the gate structure. *See* Ex. 1004, 1:44-52, 2:21-23; Ex. 1005, at ¶108. Inadequate formation of a gate silicide layer is attributed to reduced reaction area for the conductive layer to form on, leading to increased gate

resistance. *Id*., 2:21-30. "This is detrimental to the efficiency of the semiconductor device, as higher resistance decreases the speed of the semiconductor circuitry." *Id*., 1:52-54. The reduced gate structural dimensions lead to a reduction in the available nucleation sites on which the conductive layer can form. *See id.*, 2:21-30; Ex. 1005, *id*.

To solve this problem, Intel 598 discloses a method of manufacturing semiconductor devices with a gate structure like the ones taught in the '620 patent and AMD 680—namely, gate structures comprised of pairs of interposed oxide and nitride spacers formed on either side of the gate sidewalls. *See id*., Fig. 6m & 6e:

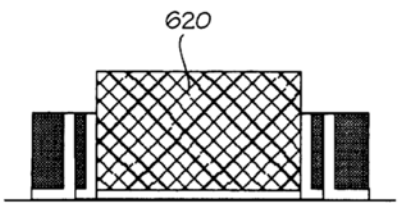


Fig. 6M

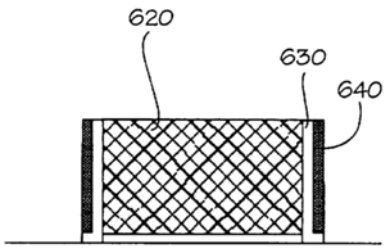


Fig. 6E

Spacers 640 are positioned on either side of the gate structure 620 to prevent transfer of electric current between the gate 620 and surrounding structures in the semiconductor substrate 600. *Id.*, 1:37-40 & Fig. 6a & 6e:

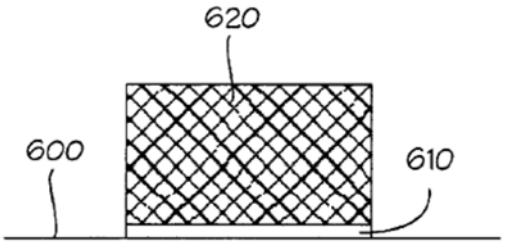


Fig. 6A

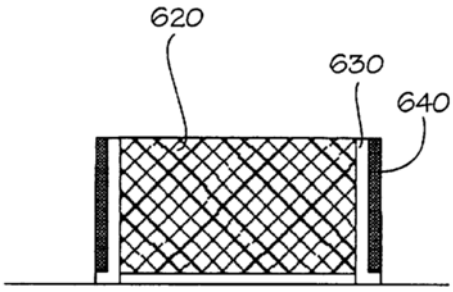


Fig. 6E

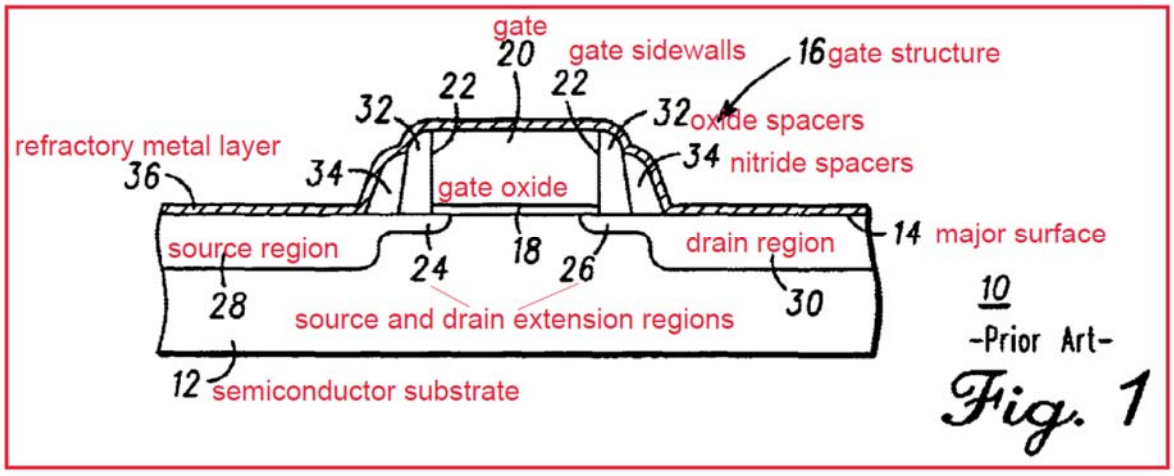
As shown, a thin first spacer layer 630 is deposited on gate layer 620 and substrate 600. The thin first spacer layer 630 can be an oxide layer (hereinafter "oxide layer 630"). *Id.* In one embodiment, Intel 598 discloses that the thickness of the oxide layer 630 is approximately 50-150 Angstroms (Å). *Id*., 8:21-29. The oxide layer 630 is deposited using deposition techniques that were well known in the art at the time. Ex. 1004, *id.*; Ex. 1005, at ¶111.

Like in the '620 patent, Intel 598 discloses using an etch process to recess the spacers to expose the upper portions of the gate sidewalls, thus creating a larger reaction surface area for silicide formation. *Id.*, at 9:39-54 & Fig. 6m (above). An anisotropic etching process was used to remove the nitride spacers, but not the oxide (*see id.*, 9:40-43), and an isotropic etching process was used to remove the oxide spacers, but not the nitride (*see, id*., 8:45-49). Ex. 1005, at ¶112.

3. Knowledge Of One Of Ordinary Skill In The Art

The knowledge of a POSA is deemed to at least include any admitted prior art disclosed in a patent's Background of the Invention. Thus, in terms of the '620

patent, the knowledge of a POSA includes the device shown in Fig. 1 below. *See* Ex. 1005, at ¶113; Ex. 1001, 1:40-62 & Fig. 1 (below):



In addition, the knowledge of a POSA would have also included known techniques for forming a dielectric material of a specified thickness. Indeed, the '620 patent acknowledges that forming a dielectric material with a thickness ranging from 10 to 100 Å could be carried out using techniques known to those skilled in the art. *See* Ex. 1001, 3:30-36. Thus, forming a dielectric layer with a thickness less than 100 Å would have been an obvious design choice within the knowledge of a POSA at the time. Ex. 1005, ¶114 *see also* Ex. 1004, 8:27-29.

B. Potential Differences Between The Prior Art And The Challenged Claims

AMD 680 discloses a semiconductor component comprised of a gate structure that has an oxide layer 128 formed on the gate sidewalls, but AMD 680 does not explicitly specify any particular thickness for the oxide layer. Ex. 1003,

Fig. 6 (oxide layer 128). Claims 1, 2 and 13 of the ’620 patent expressly recite an oxide layer having a thickness in a range of less than 100 Å.

Further, AMD 680 does not explicitly disclose recessing the spacers to expose more gate silicon surface area for silicide formation. Claims 4, 10 and 15 of the ’620 patent expressly recite limitations related to this feature.

As noted above, techniques for forming dielectric layers (e.g., oxide layers) of a specified thickness were well-known in the art. Therefore, specifying an oxide layer with a thickness in the range of less than 100 Å would have been an obvious design choice for a POSA. And regardless, Intel 598 discloses using a selective etch process for recessing oxide/nitride spacers to expose more gate silicon surface area for silicide formation in the same manner as in the ’620 patent. *See* Ex. 1004, 9:39-55 & Fig. 6m & 6e:

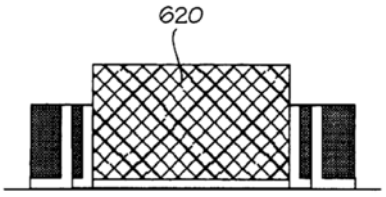


Fig. 6M

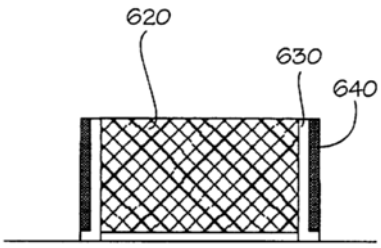


Fig. 6E

In addition, Intel 598 explicitly discloses forming the thin oxide layer 630 with a thickness of less than 100 Å. *See* Ex. 1004, 8:21-29.

Thus, a POSA would have had both of the prior art techniques disclosed in AMD 680 and Intel 598 at his or her fingertips for use in designing gate structures

for semiconductor devices with small gate widths. A POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with more exposed gate silicon surface area for silicide formation to improve gate resistance (Intel 598) and with spacers used for forming a graded junction to reduce short-channel effects (AMD 680). Ex. 1005, ¶121.

Thus, the potential difference between AMD 680 and the challenged claims is expressly disclosed by Intel 598, and a POSA would have clearly been motivated to combine AMD 680 with Intel 598.

C. The Level Of Skill In The Art

Petitioner provides the level of ordinary skill in the art, in Section IX.C. above.

D. There Would Have Been A Motivation To Combine AMD 680 With Intel 598

The rationale to combine or modify prior art references is significantly stronger when the references seek to solve the same problem, come from the same field, and correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001). It would have been obvious to a POSA to have combined the teachings of AMD 680 with those of Intel 598. Ex. 1005, ¶116. AMD 680 and Intel 598 both concern the same field of semiconductor processing, solve similar problems relating to reduced gate widths in semiconductor devices, and their respective teachings correspond remarkably well. *See* Ex. 1005, *id*.

Both AMD 680 and Intel 598 concern forming silicide on gate structures. For example, Fig. 17 of AMD 680 depicts silicide layers 198, 200 and 202 formed on the top of gate structure 114. *See* Ex. 1003, 11:56-63 & Fig. 17:

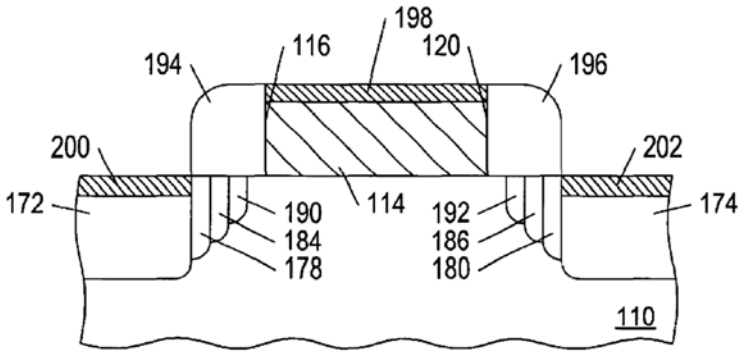


FIG. 17

Fig. 6n of Intel 598 discloses using an etch process for selectively recessing the thin oxide layer 630 and nitride spacers 640 to expose more gate silicon surface area on the upper portions of the gate structure 126 for silicide to form on. Ex. 1004, 9:39-63 & Fig. 6n:

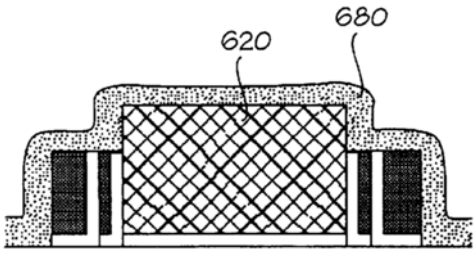


Fig. 6N

AMD 680 and Intel 598 are fully compatible, as there is nothing taught in AMD 680 that would exclude using Intel 598's method of recessing spacers for increased gate silicon surface area for silicide to form on. Ex, 1005, ¶120. The spacers disclosed in AMD 680 could be recessed in the same manner disclosed in

Intel 598 at any point in the fabrication process without effecting the principle of operation of the method. *Id*. Likewise, there is nothing disclosed in Intel 598 that would exclude using AMD 680's method of using oxide/nitride spacers for forming graded junctions in the source/drain regions of the device to reduce short-channel effects. *Id*. The spacers disclosed in Intel 598 could have also been used as masks for selective doping of different regions in the semiconductor device at various offsets from the gate structure to form a graded junction in the same manner as disclosed in AMD 680. *Id*.

Thus, a POSA would have had both of these prior art techniques readily available for use in designing gate structures for semiconductor devices having shrunk device sizes with smaller gate widths. Ex. 1005, ¶121. A POSA would have been motivated to use these combined teachings to manufacture semiconductor devices with more exposed gate silicon surface area for silicide formation to improve gate resistance (Intel 598) and with oxide/nitride spacers for forming a graded junction to reduce short-channel effects (AMD 680). *Id*.

As explained in more detail below, there is no difference between the scope and content of this combined prior art and the subject matter of the challenged claims. Thus, the combination of AMD 680 and Intel 598 render the challenged claims obvious. Ex. 1005, ¶122.

E. Independent Claim 1

AMD 680 discloses each of the limitations recited in independent claim 1 of the ’620 patent except for the limitation specifying that the oxide layer thickness is less than 100 Å. But, as noted above, a POSA would have understood the thickness of the oxide layer material to be an obvious design choice. Regardless, Intel 598 discloses this feature, as set forth more fully below, and thus renders obvious claim 1 in view of AMD 680.

AMD 680 discloses a “semiconductor component,” as recited in the preamble of independent claim 1. *See* Ex. 1003, 1:11-14 (“This invention relates to semiconductor processing and, more particularly, to a method of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects.”). Intel 598 also discloses a semiconductor component. *See* Ex. 1004, 1:6-7 (“The present invention relates to the field of semiconductor devices.”). *See* Ex. 1005, ¶124.

AMD 680 discloses claim limitation 1(a): “a semiconductor material of a first conductivity type and having a major surface.” For example, the semiconductor component disclosed in Fig 6 of AMD 680 included a semiconductor substrate 110 comprising n-type or p-type doped silicon material of a first conductivity type and having a major surface, at least at the intersection of

substrate 110 and oxide layer 128. Ex. 1005, ¶125; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

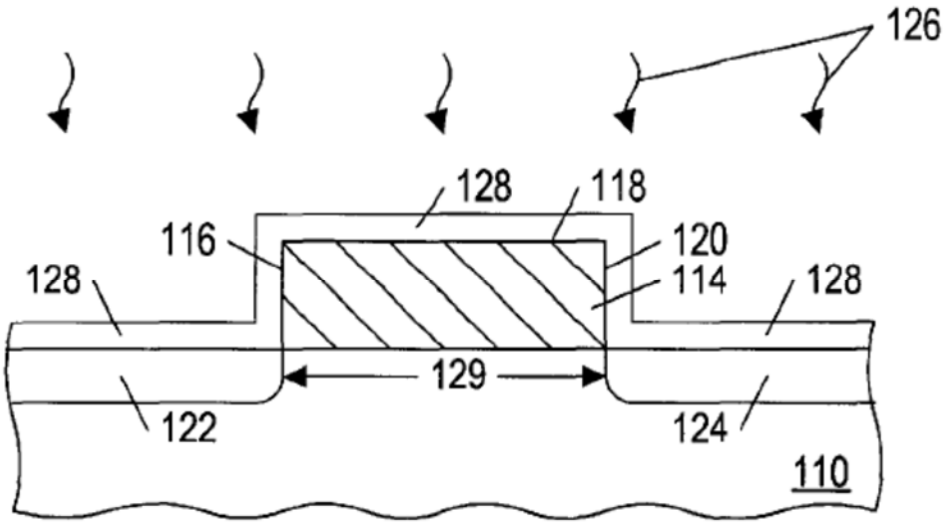
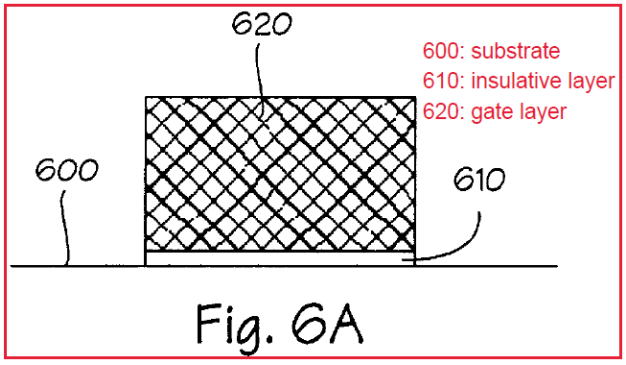


FIG. 6

Intel 598 also discloses this limitation. For example, Fig. 6a below shows a semiconductor substrate 600 having a major surface and made from a material with a first conductivity type. *See* Ex. 1005, ¶126; Ex. 1004 8:15-20 & Fig. 6a:



AMD 680 discloses 1(b): "a gate structure over a portion of the major surface, the gate structure having a top surface and first and second sides." For example, the semiconductor component disclosed in Fig 6 includes a gate structure

114 formed over a portion of semiconductor substrate 110. The gate structure 114 includes a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1003 7:63-67 & Fig. 6 (above); Ex. 1005, ¶127.

Intel 598 also discloses this limitation. For example, Fig. 6a below discloses a gate structure 620 on a substrate 600 with a top surface and sidewalls. *See* Ex. 1005, ¶128; Ex. 1004, 8:15-20 & Fig. 6a:

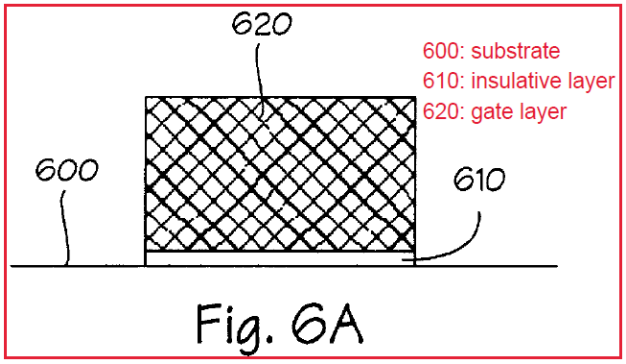


Fig. 6A

The combined teachings of AMD 680 and Intel 598 disclose the limitations of 1(c): "a first nitride spacer adjacent the first side of the gate structure, the first nitride spacer spaced apart from the gate structure by an oxide layer having a thickness of less than 100 Angstroms."[5] As shown in Fig. 7 below, AMD 680 discloses a semiconductor component with a nitride spacer 136 formed adjacent to

[5] Petitioner's position in this Petition with respect to the "adjacent" claim term is based on Patent Owner's apparent construction of that term in the related district court litigation.

gate sidewall 116 and spaced apart by an oxide layer 128. *See* Ex. 1005, ¶129; Ex. 1003, 8:23-32 & Fig. 7:

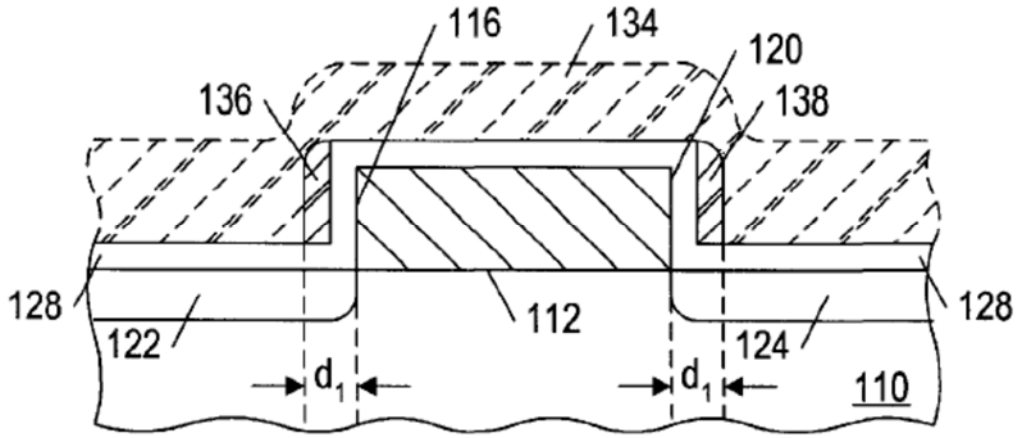


FIG. 7

As noted above, although AMD 680 did not explicitly disclose an oxide layer thickness of less than 100 Å, it would have been an obvious design choice for a POSA to do so. And, regardless, Intel 598 discloses this limitation. For example, Intel 598's Fig. 6d discloses a thin oxide layer 630 formed between gate 114 and a first nitride spacer 640 with a thickness in the range of 50-150 Å. *See* Ex. 1005, ¶130; Ex. 1004, 8:21-30 & Fig. 6d:

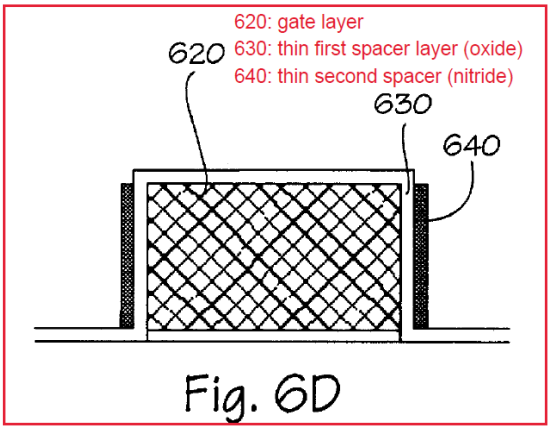


Fig. 6D

It would have been obvious for a POSA to modify AMD 680 and/or combine the teachings of AMD 680 with Intel 598's specific disclosure of the thickness of a dielectric layer (oxide layer 630) in the range of 100 Å or less. *See* Ex. 1005, ¶131. These combined teachings render obvious the limitations in 1(c).

AMD 680 discloses 1(d): "a first doped region in the semiconductor material and aligned to the first nitride spacer." For example, as shown in Fig. 8 below, the semiconductor component in AMD 680 includes a first doped region 142 aligned to the first nitride spacer 136. *See* Ex. 1005, ¶132; Ex. 1003, 8:35-37 & Fig. 8:

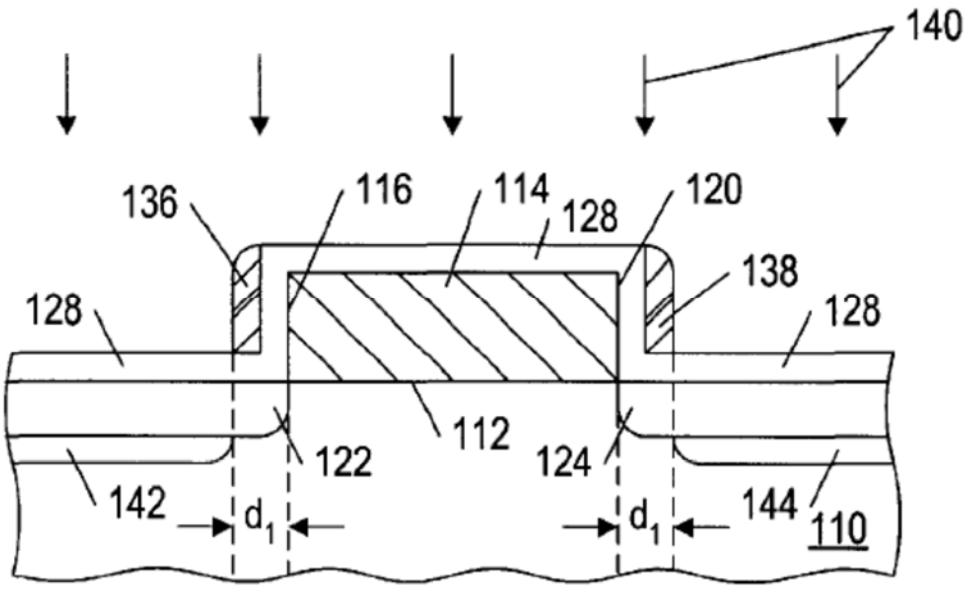


FIG. 8

AMD 680 discloses 1(e): "a second nitride spacer adjacent the first nitride spacer." For example, Fig. 12 below shows a second nitride spacer 160 formed on either side of the first nitride spacer 136. *See* Ex. 1005, ¶133; Ex. 1003 9:8-11 & Fig. 12:

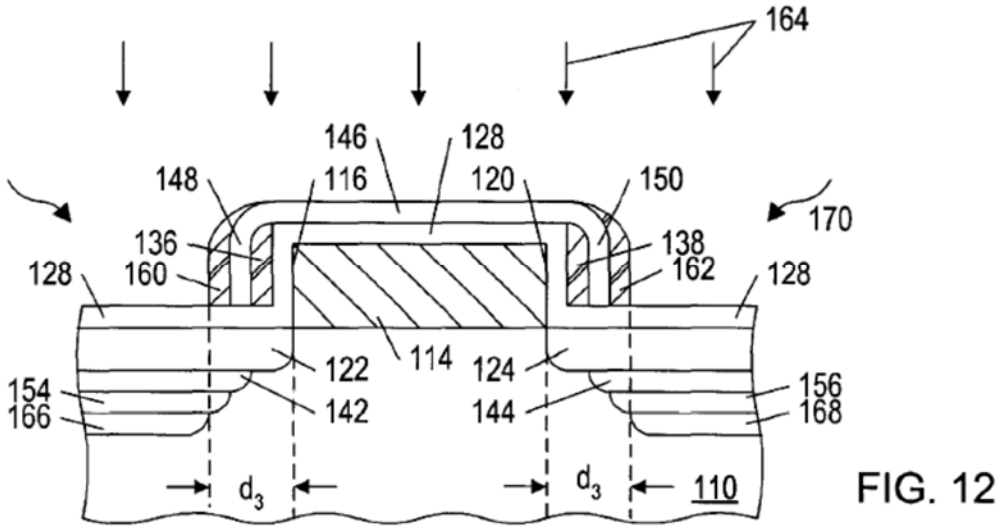


FIG. 12

Intel 598 also discloses first and second nitride spacers on either side of the gate structure. For example, Figs. 6g below shows a first nitride spacer 640 and a second nitride spacer 660 formed on either side of the gate structure 620. *See, e.g.*, Ex. 1005, ¶134; Ex. 1004, 8:61-64 & Figs. 6e, 6g:

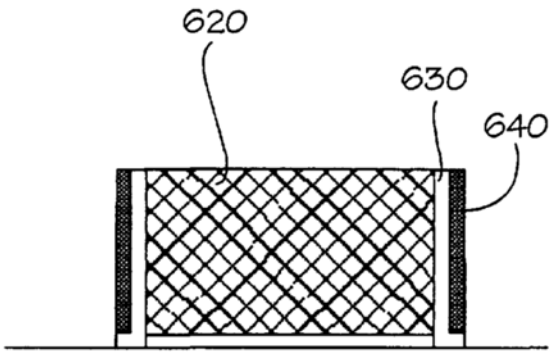


Fig. 6E

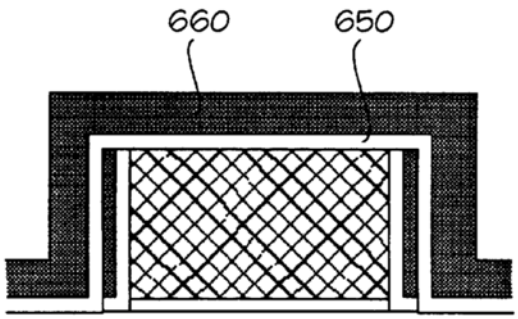


Fig. 6G

AMD 680 discloses 1(f): "a second doped region in the semiconductor material and aligned to the second nitride spacer." For example, Fig. 12 below

shows a semiconductor component with a second doped region 166 aligned to the second nitride spacer 160. *See* Ex. 1005, ¶135; Ex. 1003 9:20-34 & Fig. 12:

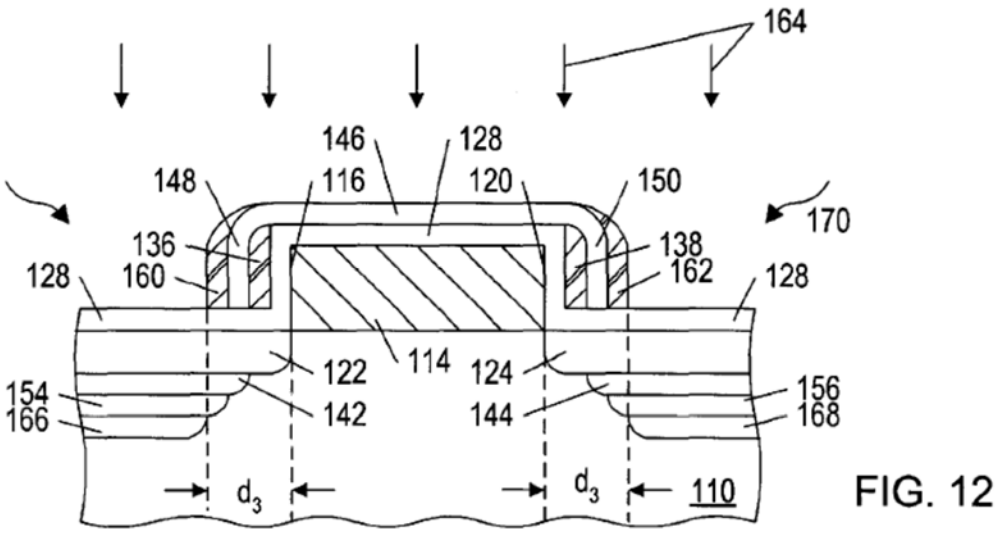


FIG. 12

AMD 680 discloses 1(g): "a third doped region in the semiconductor material and aligned to the second side of the gate structure." For example, Fig. 12 above shows a semiconductor component comprised of a third doped region 124 aligned to gate sidewall 120 of gate structure 114. *See* Ex. 1005, ¶136; Ex. 1003, 8:1-8 & Fig. 12.

Thus, AMD 680 in view of Intel 598 renders obvious each and every limitation recited in independent claim 1 of the '620 patent. For at least the reasons set forth above, Petitioner respectfully requests the Board find claim 1 unpatentable.

F. Dependent Claims 2-6

The combined teachings of AMD 680 and Intel 598 disclose all the limitations of claim 2: "a third nitride spacer adjacent the second side of the gate structure, the third nitride spacer spaced apart from the gate structure by the oxide layer having a thickness less than 100 Angstroms." For example, Fig. 7 below shows a semiconductor component with a third nitride spacer 138 formed adjacent to gate sidewall 120 (second side of the gate structure) and spaced apart from the gate structure by the oxide layer 128. *See* Ex. 1005, ¶138; Ex. 1003 Fig. 7:

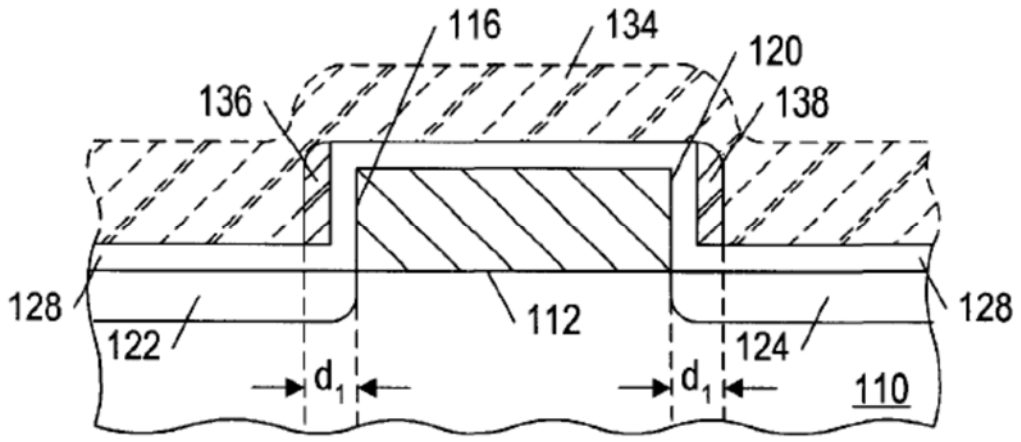
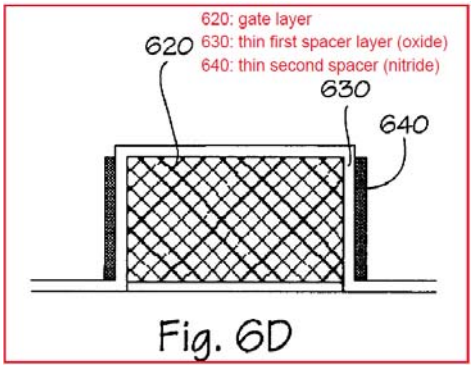


FIG. 7

As noted above, although AMD 680 does not explicitly disclose an oxide layer with a thickness in the range of less than 100 Å, it would have been an obvious design choice to do so. Ex. 1005, ¶139. And, regardless, Intel 598 discloses a gate structure with a thin oxide layer formed between the gate structure and a third nitride spacer that had a thickness in a range less than 100 Å. For example, Fig. 6d below shows a thin oxide layer 630 formed between the gate 620

and the third nitride spacer 640 that had a thickness in the range of "50-150 Å, for example, 50 Å." *See* Ex. 1005, *id.*; Ex. 1004, 8:21-27 & Fig. 6d:



It would have been obvious for a POSA to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer with Intel 598's specific disclosure of forming oxide layers with a thickness less than 100 Å. *See* Ex. 1005, ¶140. These combined teachings render obvious the limitations recited in claim 2 of the '620 patent.

AMD 680 discloses claim 3: "a fourth nitride spacer adjacent the third nitride spacer." For example, Fig. 12 below shows a semiconductor component comprised of a fourth nitride spacer 162 formed on the side of the third nitride spacer 138. *See* Ex. 1005, ¶141; Ex. 1003 Fig. 12:

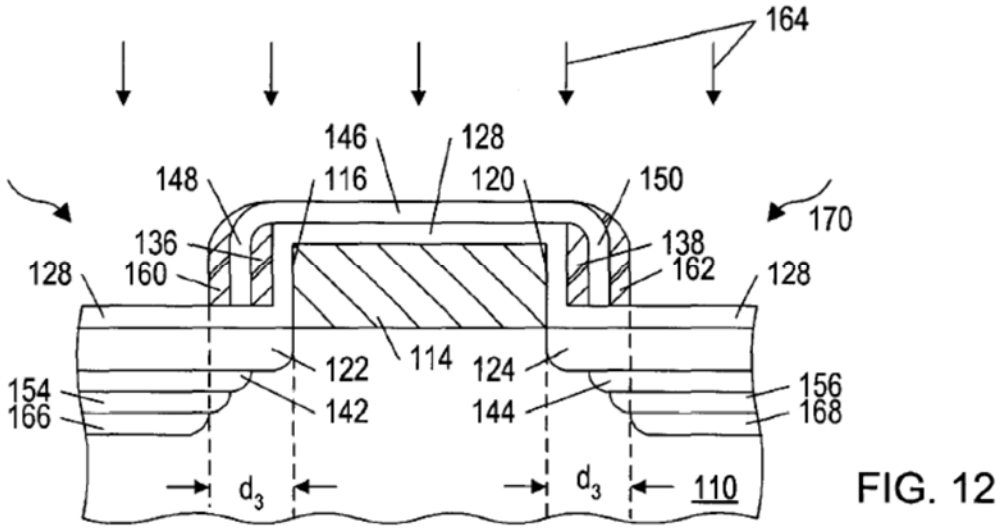


FIG. 12

Intel 598 also discloses claim 3. For example, the figures below show a semiconductor component comprised of second and fourth nitride spacers 660 (one on each side) formed on either side of the first and third nitride spacers 640 (one on each side), respectively. *See, e.g.*, Ex. 1005, ¶142; Ex. 1004, Fig. 6e, 6h:

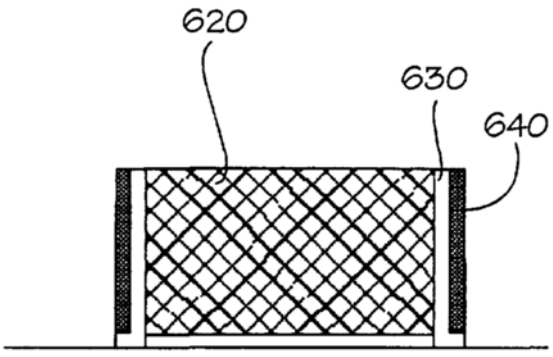


Fig. 6E

620: gate layer
650: thin third spacer layer (oxide)
660: thick fourth spacer (nitride)

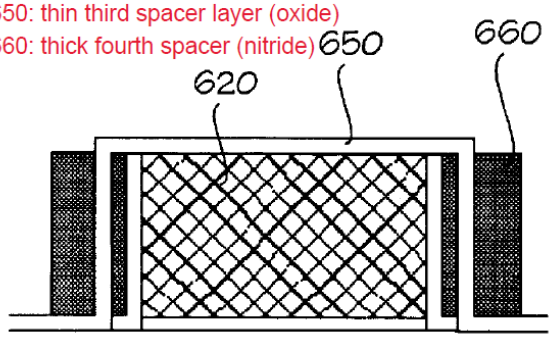


Fig. 6H

The combined teachings of AMD 680 and Intel 598 disclose all the limitations of dependent claim 4: "including silicide along a portion of the first side and a portion of the second side of the gate structure and silicide on the top surface

of the gate structure." Ex. 1005, ¶143. While AMD 680 describes forming silicide on the source region, drain region, and on top of the gate region of a semiconductor device, AMD 680 does not explicitly disclose forming silicide on a portion of the gate sidewalls. But Intel 598 discloses using an etch process for selectively recessing the oxide layer and nitride spacers to expose more gate silicon surface area for silicide formation on the upper portions of the gate structure. Fig. 6n below shows the results of the etch process that recessed thin oxide layer 630 and nitride spacers 640 (and 660 not shown) to expose more silicon surface area of gate 620 for the reactant layer 680, which forms silicide on the upper portion of the sidewalls of gate 620. *See, e.g.*, Ex. 1005 *id.*; Ex. 1004, 9:39-10:1 & Fig. 6e, 6n:

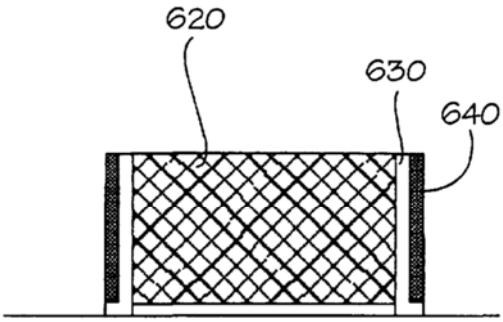


Fig. 6E

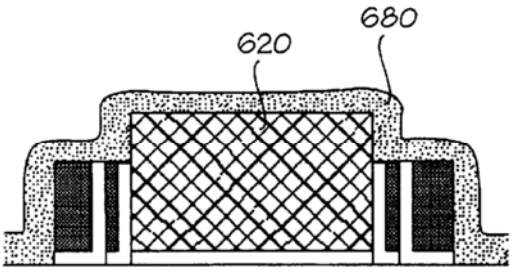


Fig. 6N

As explained above, it would have been obvious for a POSA to combine the disclosures of AMD 680 concerning using spacers to form graded junctions in semiconductor devices with the teachings of Intel 598 concerning recessing oxide and nitride spacers for increased gate surface area for silicide formation. Ex. 1005, ¶144. A POSA would have been motivated to use these combined teachings to

manufacture semiconductor devices with improved gate resistance (Intel 598) and reduced short-channel effects (AMD 680). *Id*. Therefore, these combined teachings render the limitations recited in claim 4 obvious. Thus, these combined teachings render obvious the limitations recited in claim 4. *Id*.

AMD 680 discloses the limitations of claim 5: "the first nitride spacer is spaced apart from the second nitride spacer by a first portion of an oxide layer and wherein the third nitride spacer is spaced apart from the fourth nitride spacer by a second portion of the oxide layer." For example, Fig. 12 below shows a gate structure 114 with first and second nitride spacers 136/160 spaced apart by a first portion of an oxide layer 148 and third and fourth nitride spacers 138/162 spaced apart by a second portion of oxide layer 150. *See, e.g.*, Ex. 1005, ¶145; Ex. 1003, 8:29-34 & Fig. 12:

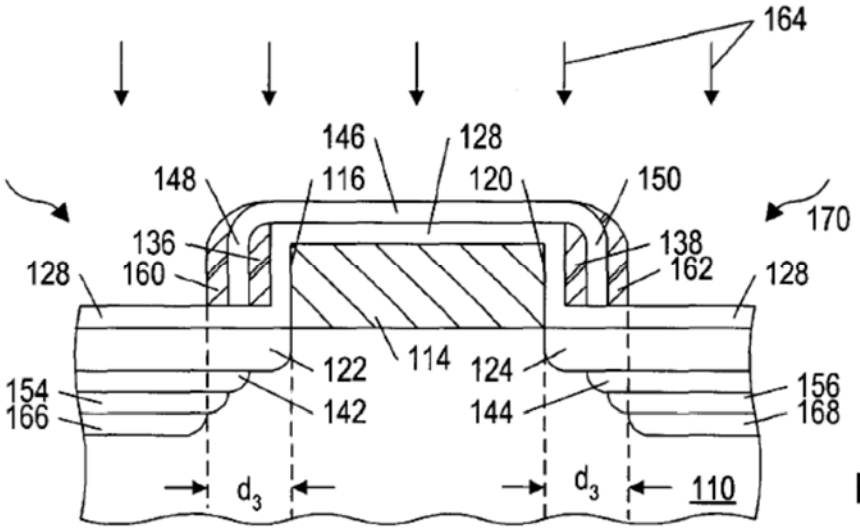
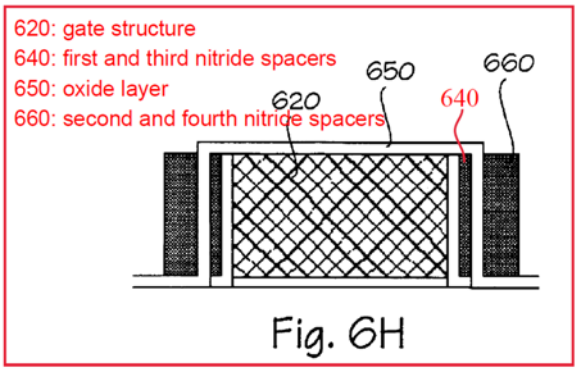


FIG. 12

Intel 598 also discloses this limitation. For example, Fig. 6h below shows a gate structure 620 with first and third nitride spacers 640 (one on each side) spaced apart from the second and fourth nitride spacers 660 (one each side) by a first and second portion of oxide layer 650. *See* Ex. 1005, ¶146; Ex. 1004, Fig. 6h:



AMD 680 discloses dependent claim 6: "the third doped region is adjacent the third nitride spacer and further including a fourth doped region, the fourth doped region adjacent the fourth nitride spacer." For example, Fig. 12 shows a third doped region 144 aligned with the third nitride spacer 138 and fourth doped region 168 formed aligned with the fourth nitride spacer 162. *See* Ex. 1005, ¶147; Ex. 1003, 9:20-33 & Fig. 12 (reproduced above).

Thus, AMD 680 in view of Intel 598 renders obvious each and every limitation recited by dependent claims 2-6. For at least the reasons set forth above, Petitioner respectfully requests the Board find claims 2-6 unpatentable.

G. Independent Claim 7

AMD 680 discloses each and every limitation of independent claim 7 of the '620 patent. AMD 680 discloses a "semiconductor component having sidewall

spacers" recited in the preamble of independent claim 7. *See* Ex. 1003, 1:11-14 ("This invention relates to semiconductor processing and, more particularly, to a method of forming layers of sidewall spacers upon a gate conductor to produce a graded junction which minimizes hot-carrier effects."). Intel 598 also discloses a semiconductor component. *See* Ex. 1004, 1:2-4 (title: "METHOD OF USING THICK FIRST SPACERS TO IMPROVE SALICIDE RESISTANCE ON POLYSILICON GATES."). Ex. 1005, ¶149.

AMD 680 discloses 7(a): "a semiconductor material having a gate structure disposed thereon, the gate structure having a top surface and first and second sides." For example, Fig. 6 below shows a semiconductor component with a gate structure 114 disposed over the substrate 110 and having a top surface 118 and sidewalls 116 and 120. *See* Ex. 1005, ¶150; Ex. 1003, 7:63-67 & Fig. 6:

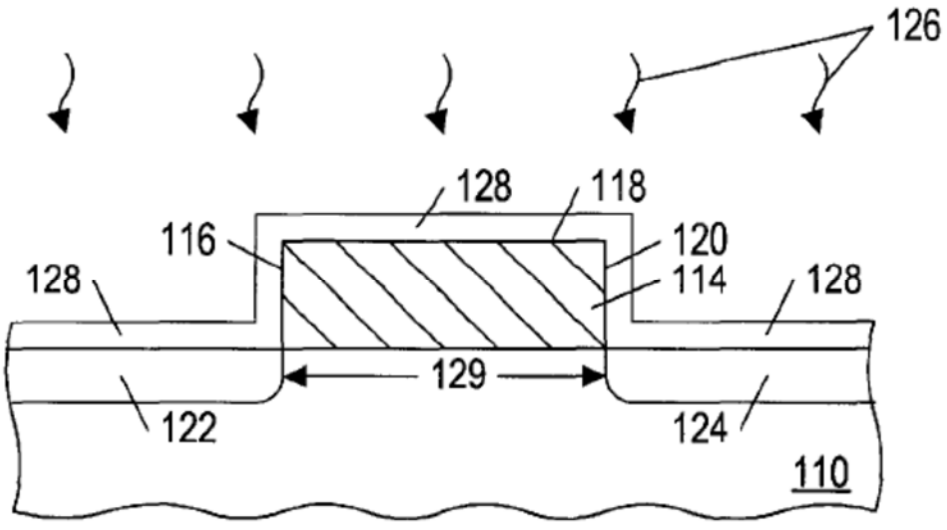


FIG. 6

Intel 598 also discloses this limitation. For example, Fig. 6a below shows a semiconductor component with a gate structure 620 disposed over the substrate 600 and having a top surface and sidewalls. *See* Ex. 1005, ¶151; Ex 1004, Fig. 6a:

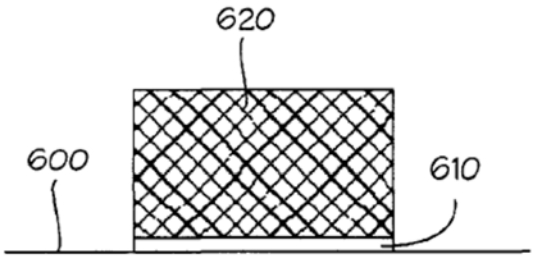


Fig. 6A

AMD 680 discloses 7(b): "a first oxide layer on the first side of the gate structure and a second oxide layer on the second side of the gate structure." For example, Fig. 6 above shows a first portion of oxide layer 128 formed on a first sidewall 116 of the gate 114 and a second portion of oxide layer 128 formed on a second sidewall 120 of the gate structure 114. *See* Ex. 1003, Fig. 6. Intel 598 also discloses limitation 7(b). For example, Intel 598's Fig. 6b below shows a first portion of oxide layer 630 formed on a first sidewall of gate structure 620 and a second portion of oxide layer 630 formed on a second sidewall on the opposite side of the gate structure 620. *See* Ex. 1005, ¶152; Ex. 1004 8:15-20 & Fig. 6b:

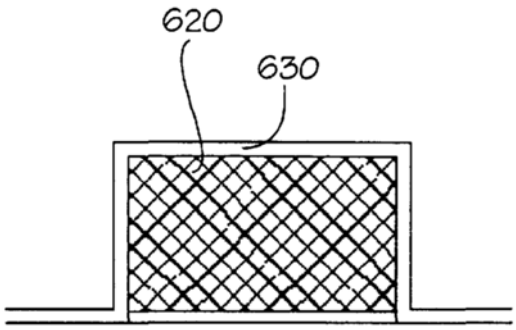


Fig. 6B

AMD 680 discloses 7(c): "a first nitride spacer in contact with the first oxide layer and a second nitride spacer in contact with the second oxide layer." For example, Fig. 12 below shows a semiconductor component with first nitride spacer 136 in contact with a first portion of oxide layer 128 and a second nitride spacer 138 in contact with a second portion of oxide layer 128. *See*, Ex. 1005, ¶153; Ex. 1003 Fig. 12:

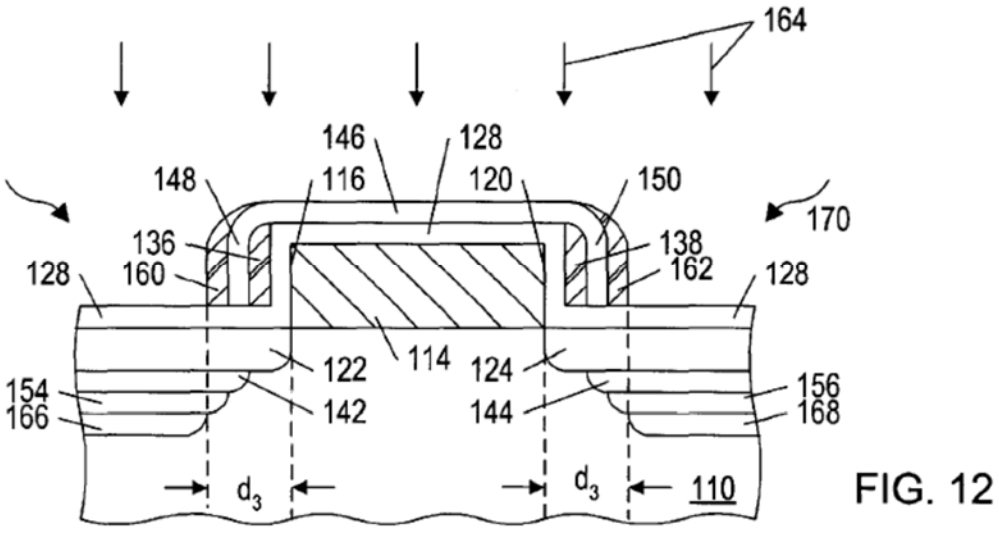


FIG. 12

Intel 598 also discloses this limitation. For example, Fig. 6d shows a pair of nitride spacers 640 in contact with first and second portions of oxide layer 630. *See* Ex. 1005, ¶154; Ex. 1004 Fig. 6d:

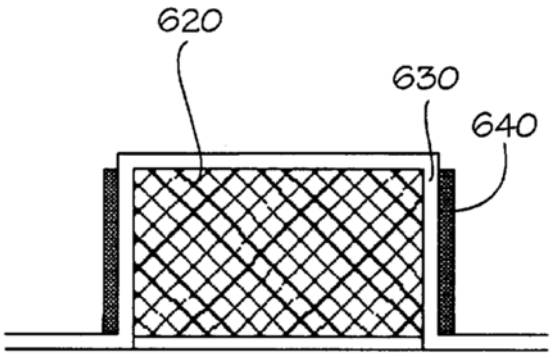


Fig. 6D

AMD 680 discloses the limitations in 7(d) and 7(e): "a third nitride spacer adjacent the first nitride spacer. … a fourth nitride spacer adjacent the second nitride spacer." For example, Fig. 11 below shows a semiconductor component with a third nitride spacer 160 formed on the side of the first nitride spacer 136 and fourth nitride spacer 162 formed on the side of the second nitride spacer 138. *See* Ex. 1005, ¶155; Ex. 1003, Fig. 11:

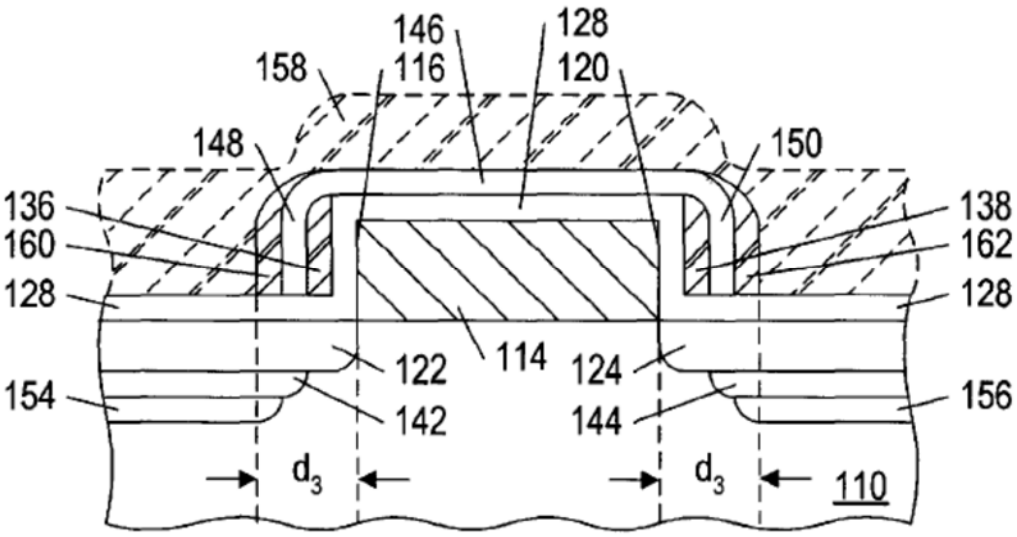


FIG. 11

Intel 598 also discloses 7(d) and 7(e). For example, Fig. 6j below shows a pair of first and second nitride spacers 640 formed on either side of a pair of third and fourth nitride spacers 660. *See* Ex. 1005, ¶156; Ex. 1004 Fig. 6h:

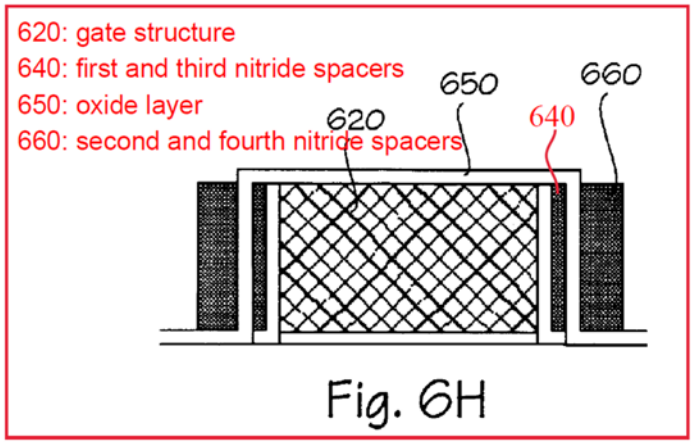


Fig. 6H

Thus, AMD 680 in view of Intel 598 renders obvious each and every limitation recited in independent claim 7 of the '620 patent. Ex. 1005, ¶157. For at least the reasons set forth above, Petitioner respectfully requests the Board find claim 7 unpatentable.

H. Dependent Claims 8-13

AMD 680 discloses dependent claim 8: "a first doped region aligned to the first nitride spacer; and a second doped region aligned to the second nitride spacer." For example, Fig. 8 below shows a semiconductor component with a first doped region 142 aligned to first nitride spacer 136 and a second doped region 144 aligned to second nitride spacer 138. *See* Ex. 1005, ¶158; Ex. 1003, 8:35-37, 45-47 & Fig. 8:

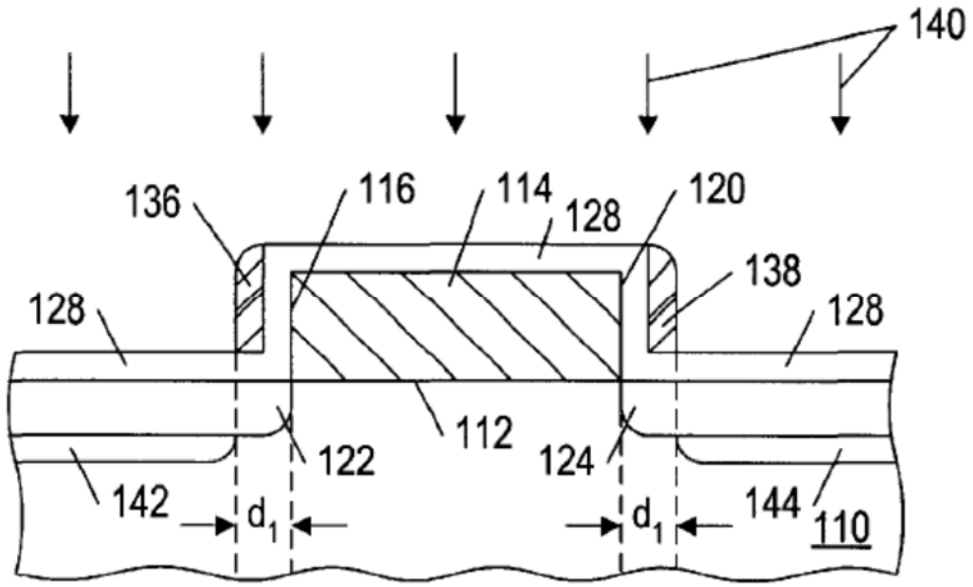


FIG. 8

AMD 680 discloses dependent claim 9: "a third doped region aligned to the third nitride spacer; and a fourth doped region aligned to the fourth nitride spacer." For example, Fig. 12 below shows a semiconductor component with a third doped region 166 aligned to third nitride spacer 160 and a fourth doped region 168 aligned to fourth nitride spacer 162. *See* Ex. 1005, ¶159; Ex. 1004, Fig. 12:

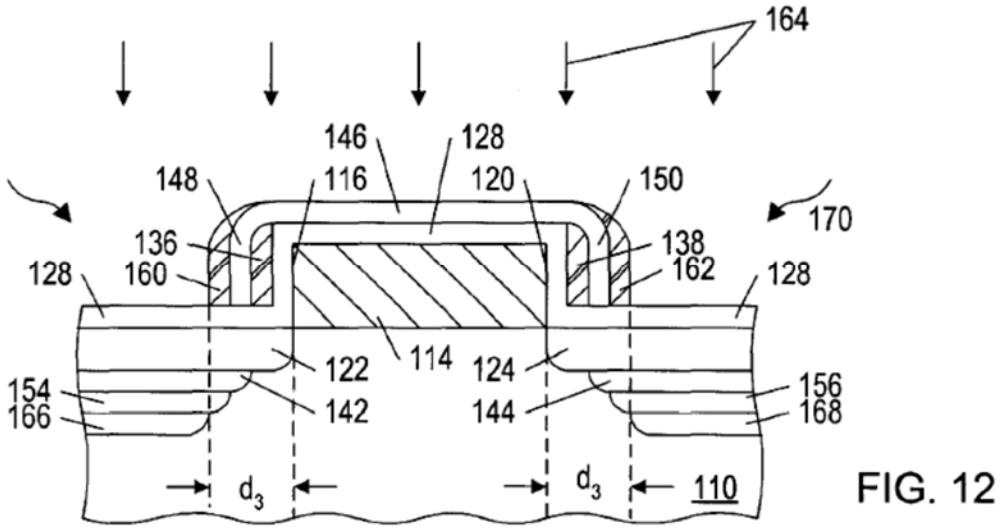


FIG. 12

The combined teachings of AMD 680 and Intel 598 disclose all the limitations of dependent claim 10: "including silicide formed from the top surface of the gate structure, a portion of the first side of the gate structure, and a portion of the second side of the gate structure." While AMD 680 describes forming silicide on the source, drain, and gate regions of a semiconductor device, it does not explicitly disclose forming silicide on the gate sidewalls. But Intel 598 discloses this limitation. In particular, Intel 598 discloses using an etch process for recessing the oxide layer and nitride spacers to expose more gate silicon surface area for silicide formation on the upper portions of the gate sidewalls. *See*, *e.g.*, Ex. 1005, ¶160; Ex. 1004, 9:39-10:1 & Fig. 6n:

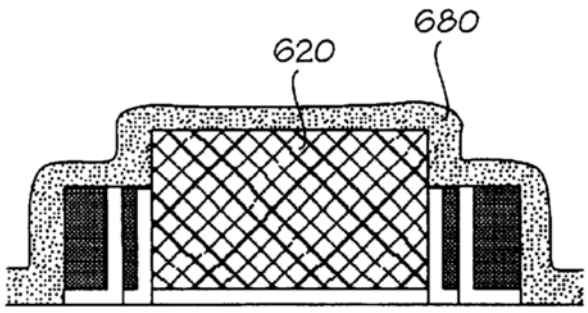


Fig. 6N

As noted above, it would have been obvious for a POSA to combine the teachings of AMD 680 with those of Intel 598. *See* Ex. 1005, ¶161. Thus, these combined teachings render obvious the limitations recited in claim 10 of the '620 patent.

The combined teachings of AMD 680 and Intel 598 disclose the limitations of dependent claim 11: "the silicide is a silicide selected from the group of silicides consisting of cobalt silicide, titanium silicide, platinum silicide, and nickel silicide." While AMD 680 describes forming silicide areas on the source region, drain region, and gate region of a semiconductor device, AMD 680 does not explicitly identify which types of silicide could be used. Intel 598 discloses this limitation. In particular, Intel 598 discloses titanium salicide ($TiSi_2$) selected from the claimed group. *See* Ex. 1005, ¶162; Ex. 1004 1:33-34.

AMD 680 discloses dependent claim 12: "including a third oxide layer between the first and third nitride spacers and a fourth oxide layer between the second and fourth nitride spacers." For example, as shown in Fig. 12 below, a

third oxide layer 148 is shown interposed between the first nitride spacer 136 and the third nitride spacer 160 and a fourth oxide layer 150 is shown interposed between the second nitride spacer 138 and fourth nitride spacer 162. *See* Ex. 1005, ¶163; Ex. 1003, Fig. 12:

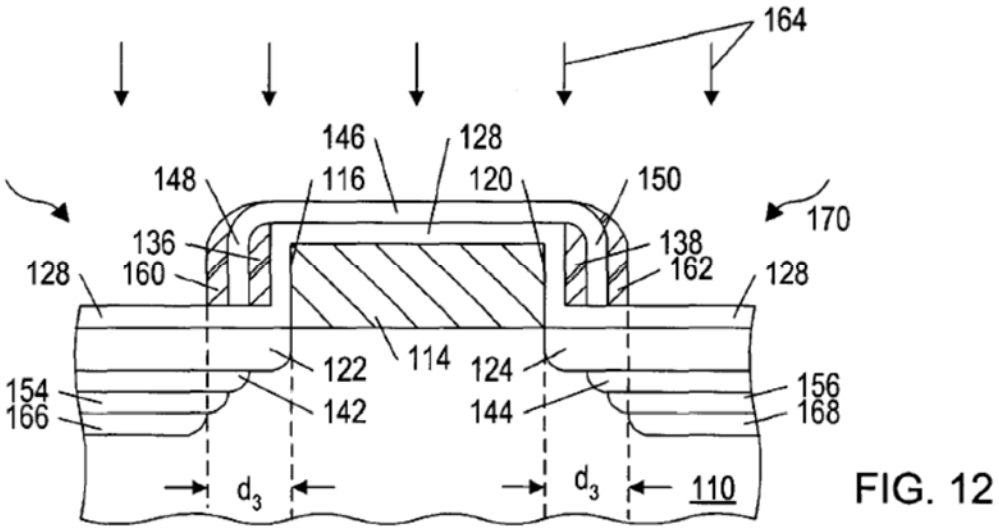


FIG. 12

The combined teachings of AMD 680 and Intel 598 disclose the limitations of claim 13: "the first oxide layer and the second oxide layer each have a thickness ranging from 10 Angstroms to 60 Angstroms." As noted above, a POSA at the time would have understood the thickness of the oxide layer to be an obvious design choice. Ex. 1005, ¶164. It would have been obvious to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer on the gate structure with Intel 598's specific disclosure of the thickness of the oxide layer being in the range of 100 Å or less. *Id.*

Thus, the combined teachings of AMD 680 in view of Intel 598 render

obvious each and every limitation recited by dependent claims 8-13 of the ’620 patent. For at least the foregoing reasons, Petitioner respectfully requests the Board find claims 8-13 unpatentable.

I. Independent Claim 14

AMD 680 discloses each and every limitation recited in independent claim 14 of the ’620 patent. To begin with, AMD 680 discloses a “semiconductor component,” as recited in the preamble of claim 14, as established above for claim 1. *See* Ex. 1003, 1:11-14. Intel 598 also discloses a semiconductor component, as established for claim 1. *See, e.g.*, Ex. 1005, ¶167; Ex. 1004, 1:6-7.

AMD 680 discloses 14(a): “a semiconductor material having a major surface, the semiconductor material of a first conductivity type.” For example, Fig. 6 below shows a semiconductor component manufactured on a semiconductor substrate 110 and having at least one major surface. *See* Ex. 1005, ¶168; Ex. 1003, Fig. 6:

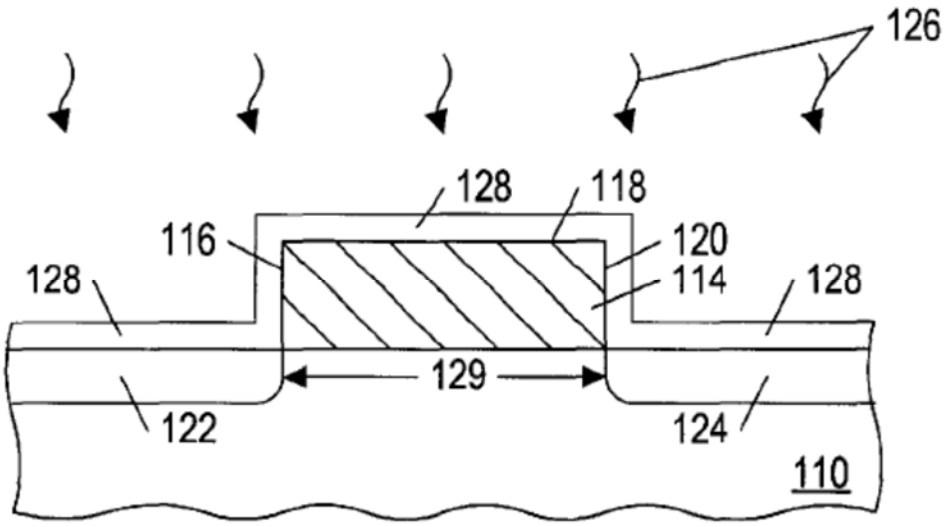


FIG. 6

The substrate is comprised of a lightly doped n-type or p-type silicon material (first conductivity type). *Id.*, 1:16-18, 7:60-63.

AMD 680 discloses 14(b): "a gate structure disposed on the major surface, the gate structure having a top surface and first and second sides." For example, Fig. 6 above shows a semiconductor component with a gate structure 114 disposed over the substrate 110 and having a top surface 118 and sidewalls 116 and 120. *See* Ex. 1005, ¶170; Ex. 1003, 7:63-67 & Fig. 6 (above).

Intel 598 also discloses 14(b). *See* Ex. 1005, ¶171; Ex. 1004, 8:15-20 & Fig. 6a:

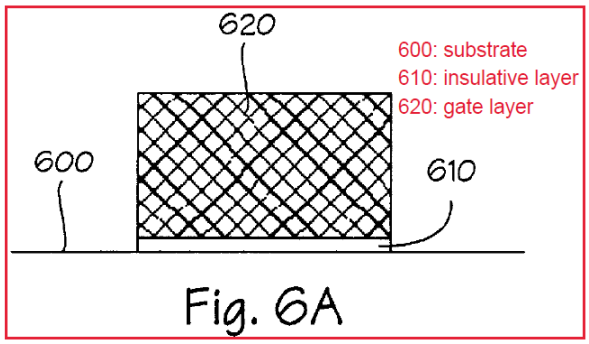


Fig. 6A

AMD 680 discloses 14(c): "a first dielectric material disposed on a first portion of the first side of the gate structure." For example, Figs. 6, 8 and 12 (reproduced above) show a semiconductor component with a first portion of oxide layer 128 formed on a portion of gate sidewall 116. *See* Ex. 1005, ¶172; Ex. 1003, Figs. 6, 8 and 12.

AMD 680 discloses 14(d): "a second dielectric material disposed on a first portion of the second side of the gate structure." For example, Figs. 6, 8 and 12 above show a semiconductor component with a second portion of oxide layer 128 disposed on a portion of gate sidewall 120 on the other side of gate 114. *See* Ex. 1005, ¶173; Ex. 1003, Figs. 6, 8 and 12 (above).

AMD 680 discloses the limitations recited in 14(e), (f), (g) and (h): "a first nitride spacer adjacent the first dielectric material. … a second nitride spacer adjacent the second dielectric material. … a third nitride spacer adjacent the first dielectric material. … a fourth nitride spacer adjacent the second nitride spacer." For example, Fig. 12 below shows a semiconductor component having a first nitride spacer 136 formed adjacent to a first portion of oxide layer 128 (first

dielectric material), a second nitride spacer 138 formed adjacent to a second portion of the oxide layer 128 (second dielectric material), a third nitride spacer 160 formed on one side of the first portion of oxide layer 128, and a fourth nitride spacer 162 formed on the other side of the second nitride spacer 138. *See* Ex. 1005, ¶174; Ex. 1003, 8:23-32, Fig. 12:

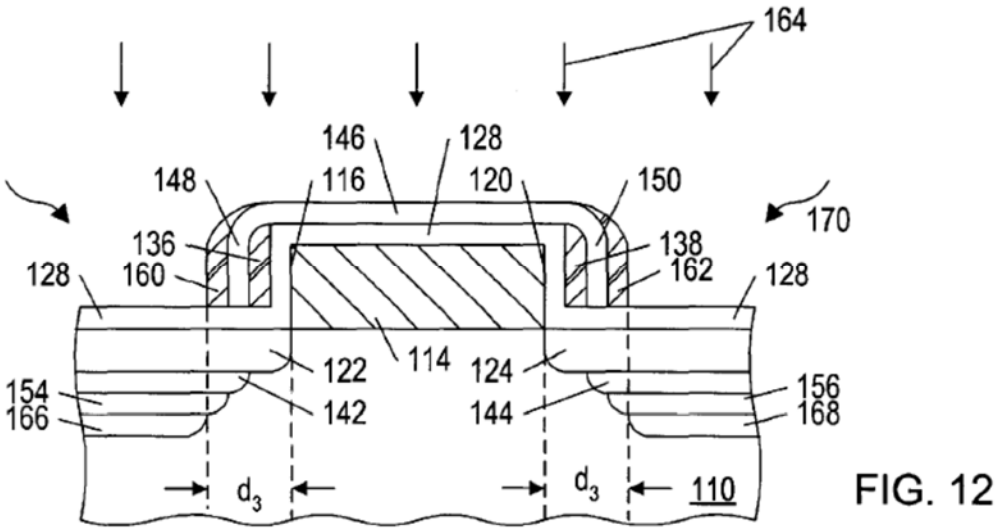


FIG. 12

Thus, the combined teachings of AMD 680 in view of Intel 598 render obvious each and every limitation recited in independent claim 14 of the ’620 patent. For at least the foregoing reasons, Petitioner respectfully requests the Board find claim 14 unpatentable.

J. Dependent Claims 15-20

AMD 680 in combination with Intel 598 disclose the limitations recited in claim 15: “including silicide formed from the top surface of the gate structure and from a second portion of the first side of the gate structure and a second portion of

the second side of the gate structure, the first and second portions adjacent the top surface of the gate structure." As noted above, while AMD 680 describes forming silicide areas on the source, drain, and gate regions of a semiconductor device, it does not explicitly disclose forming silicide on the exposed upper portions of the gate sidewalls. Intel 598 discloses this limitation. In particular, Intel 598 discloses using an etch process to selectively recess the oxide layers 630 and 650 and the nitride spacers 640 and 660 to expose more silicon surface area for silicide formation on the upper portions of the sidewalls of gate 620 in the same manner as in the '620 patent. *See, e.g.*, Ex. 1005, ¶176; Ex. 1004, 9:39-10:1 & Fig. 6n:

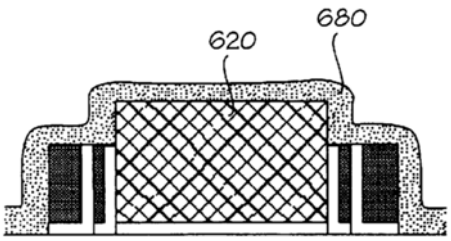


Fig. 6N

It would have been obvious to a POSA to combine the teachings of AMD 680 with those of Intel 598. Ex. 1005, ¶177.

AMD 680 discloses the limitations recited in dependent claims 16 and 17: "including oxide between the first and third nitride spacers. … oxide between the second and fourth nitride spacers." For example, Fig. 12 below shows an oxide 148 interposed between a first nitride spacer 136 and a third nitride spacer 160 and

an oxide 150 interposed between a second nitride spacer 138 and a fourth nitride spacer 162. *See* Ex. 1005, ¶178; Ex. 1003, Fig. 12:

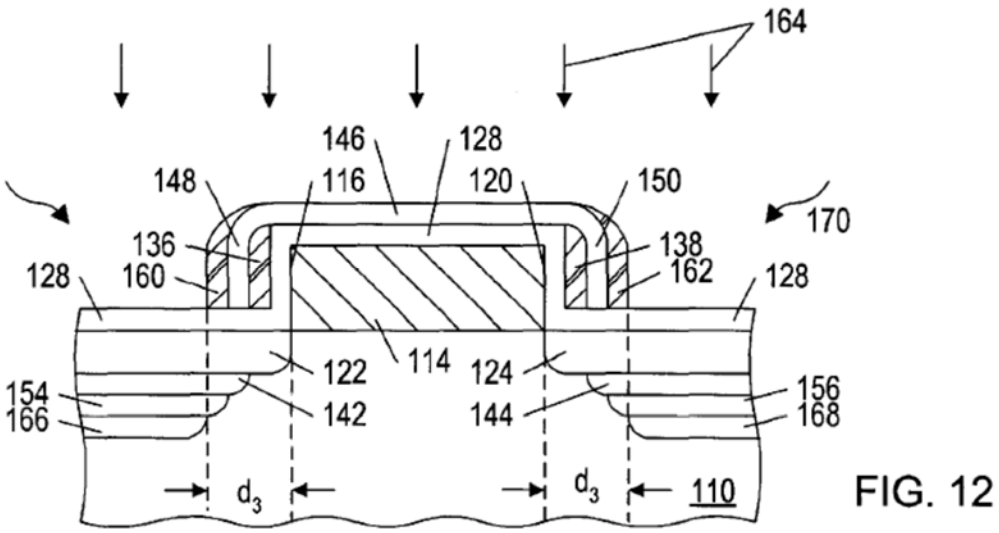


FIG. 12

Intel 598 also discloses this limitation. For example, in Figs. 6f and 6l below show a first portion of oxide 650 interposed between a first nitride spacer 640 and a third nitride spacer 660 on a first side of gate structure 620, and a second portion of oxide 650 interposed between a second nitride spacer 640 and a fourth nitride spacer 660 on a second side of gate structure 620. Ex. 1005, ¶179; Ex. 1004, Figs. 6f & 6l:

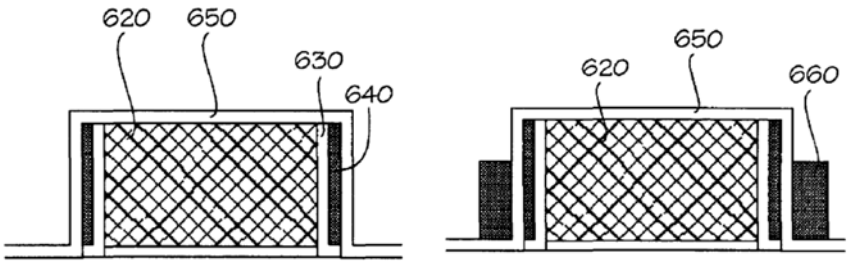


Fig. 6F Fig. 6l

AMD 680 discloses claim 18: "including first and second doped regions in the semiconductor material, the first doped region aligned to the first nitride spacer, the second doped region aligned to the second nitride spacer, and wherein the first and second doped regions are of a second conductivity type." For example, Fig. 12 above shows a first doped region 142 aligned with first nitride spacer 136 and a second doped region 144 aligned with second nitride spacer 138. *See* Ex. 1005, ¶180; Ex. 1003, Fig. 12 (above). The first and second doped regions 142 and 144 are of a second conductivity type different from the first conductivity type of the semiconductor substrate 110. *Id.*

AMD 680 discloses dependent claim 19: "including third and fourth doped regions in the semiconductor material, the third doped region aligned to the third nitride spacer, the fourth doped region aligned to the fourth nitride spacer, and wherein the third and fourth doped regions are of the second conductivity type." For example, Fig. 12 above shows a semiconductor component with a third doped region 166 aligned with the third nitride spacer 160 and a fourth doped region 168 aligned with the fourth nitride spacer 162. *See* Ex. 1005, ¶181; Ex. 1003, Fig. 12 (above). The third and fourth doped regions were comprised of a second conductivity type different from the first conductivity type of the semiconductor substrate 110. *Id.*

AMD 680 discloses claim 20: "wherein the first and second dielectric material are oxide." For example, Fig. 7 below shows the first and second dielectric materials that are formed on the gate 114 comprise oxide layer 128. *See* Ex. 1005, ¶182; Ex. 1003, 8:23-32 & Fig. 7:

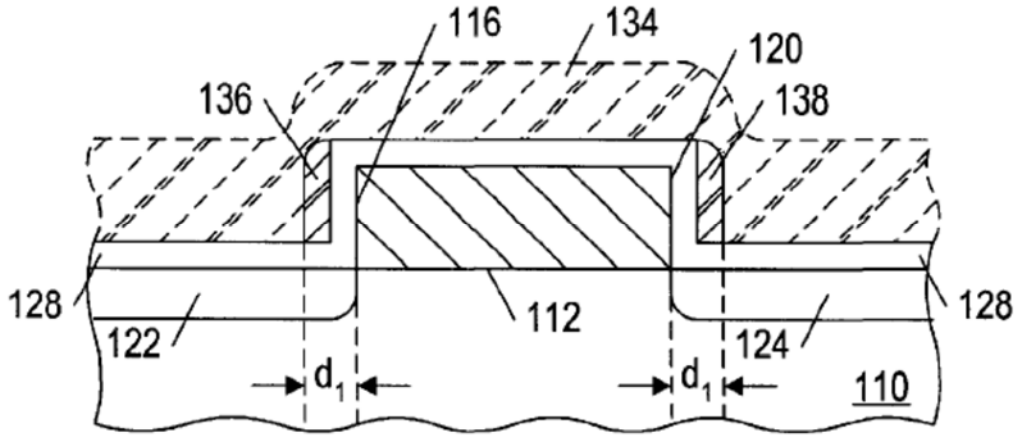


FIG. 7

Thus, the combined teachings of AMD 680 in view of Intel 598 render obvious each and every limitation recited in claims 1-20 of the '620 patent. *See* Ex. 1005, ¶183. A claim chart for AMD 680 is attached as Exhibit 1006.

For at least the foregoing reasons, Petitioner respectfully requests the Board find challenged claims 1-20 of the '620 patent unpatentable.

XI. GROUND 2: CLAIMS 7-9, 12, 14 AND 16-20 ARE ANTICIPATED BY AMD 680

A POSA at the time of the earliest effective filing date of the '620 patent would have understood that AMD 680 discloses each and every limitation of claims 7-9, 12, 14 and 16-20 of the '620 patent, and consequently, anticipates these

claims. Like the ’620 patent, AMD 680 concerns a method of manufacturing semiconductor devices using a sequence of interposed pairs of oxide layers and nitride spacers formed adjacent to the sidewalls of the gate structure. These pairs of spacers were used to form graded junction with a relatively smooth doping profile for the purpose of minimizing the abrupt voltage change at the junction to reduce the electric field at the junction. *See* Ex. 1001, 1:27-30; Ex. 1003, 3:6-7, 21-33, 4:56-60; Ex. 1005, ¶184. This, in turn, reduced harmful short-channel effects in the semiconductor device. *See* Ex. 1003, 5:1-9. Disbursing the abrupt voltage changes at the junction reduced the intensity of the electric field and associated harmful short-channel effects. *See* Ex. 1003, 3:23-33; Ex. 1005, *id*.

A. AMD 680 Anticipates Independent Claim 7

If the patented invention was “patented or described in a printed publication in this or a foreign country . . . more than one year prior to the date of the application for patent in the United States,” then the invention is not novel—it is said to be anticipated by the prior art. Anticipation requires a determination of whether the prior patent or printed publication discloses each and every element of the claimed invention. *In re Paulsen*, 30 F.3d 1475 (Fed. Cir. 1994); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or

inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

AMD 680 discloses the preamble of independent claim 7 as discussed in section X. G. above.

AMD 680 discloses 7(a) as discussed in section X. G. above. For example, Fig. 6 below shows a semiconductor component with a gate structure 114 having a top surface 118 and first and second gate sidewalls 116/120. *See* Ex. 1005, ¶186; Ex. 1003, 7:63-67 & Fig. 6:

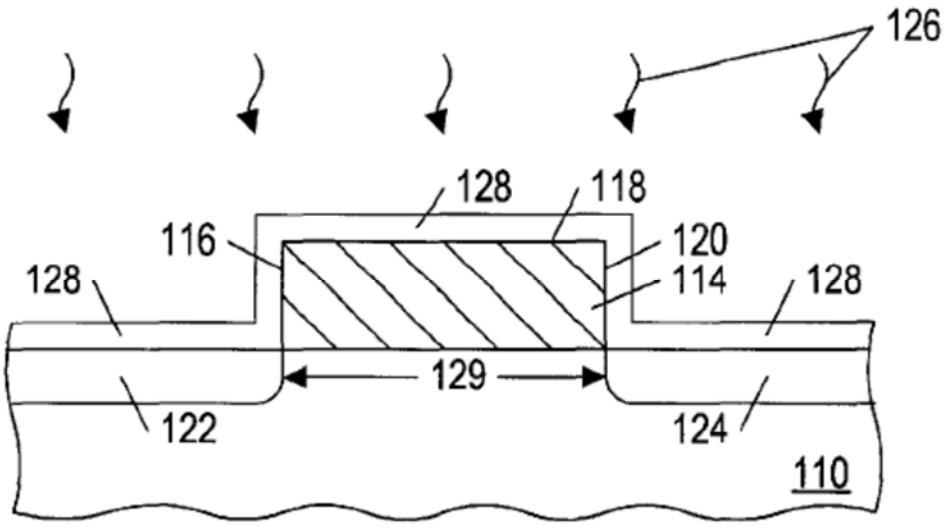


FIG. 6

AMD 680 discloses 7(b) as discussed in section X. G. above. For example, Fig. 6 shows a semiconductor component with a first and second portions of oxide layer 128 formed on first and second gate sidewalls 114/116 of gate 114. *See* Ex. 1005, ¶187.

AMD 680 discloses 7(c) as discussed in section X. G. above. For example, Fig. 12 below shows a semiconductor component with a first nitride spacer 136 in contact with a first portion of oxide layer 128 and a second nitride spacer 138 in contact with a second portion of the oxide layer 128. Ex. 1003, Fig. 12; Ex. 1005, ¶188.

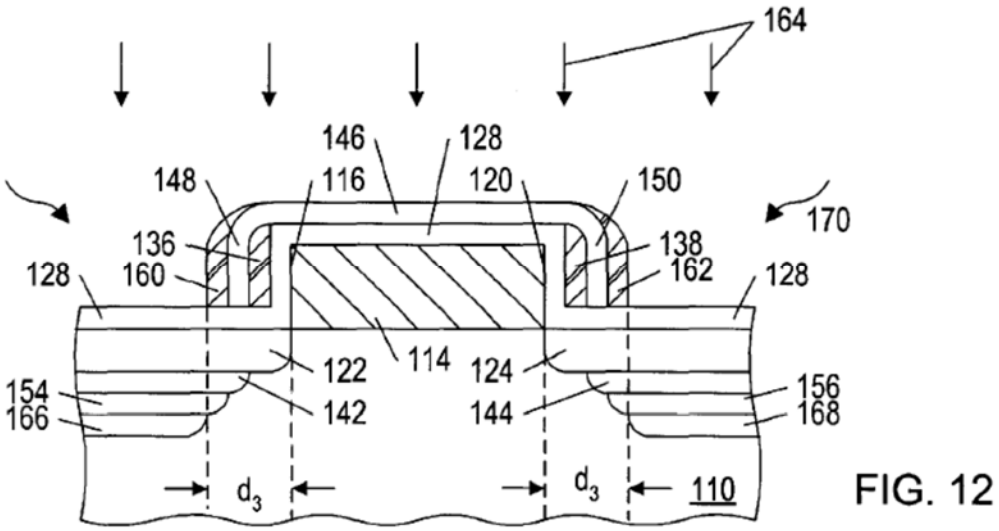


FIG. 12

AMD 680 discloses 7(d) and 7(e) as discussed in section X. G. above. For example, Fig. 12 shows a semiconductor component with a third nitride spacer 160 formed on one side of the first nitride spacer 136 and a fourth nitride spacer 162 formed on the other side of the second nitride spacer 138. *See* Ex. 1005, ¶189; Ex. 1003 Fig. 12.

Thus, a POSA would have understood that AMD 680 discloses each and every element recited in independent claim 7, and as a consequence, anticipates that claim.

B. AMD 680 Anticipates Dependent Claims 8, 9 And 12

AMD 680 discloses dependent claim 8 as discussed in section X. H. above. For example, Fig. 8 below shows a semiconductor device with a first doped region 142 aligned to first nitride spacer 136 and a second doped region 144 aligned to second spacer 138. *See* Ex. 1005, ¶191; Ex. 1003, 8:35-37; 8:45-47 & Fig. 8:

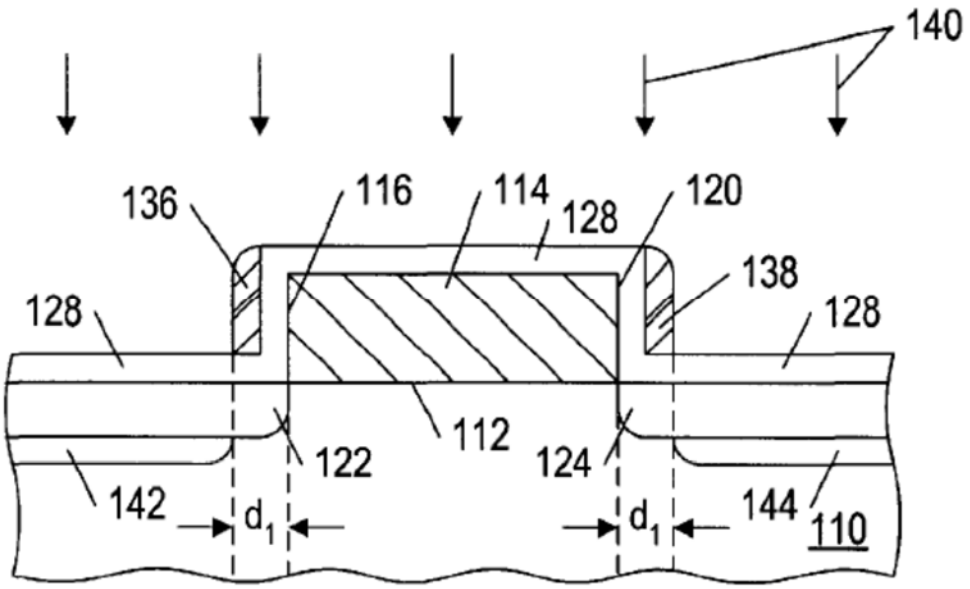


FIG. 8

AMD 680 discloses claim 9 as discussed in section X. H. above. For example, Fig. 12 below shows a semiconductor component with a third doped region 166 aligned to third nitride spacer 160 and a fourth doped region 168 aligned to fourth nitride spacer 162. *See* Ex. 1005, ¶192; Ex. 1003, Fig. 12:

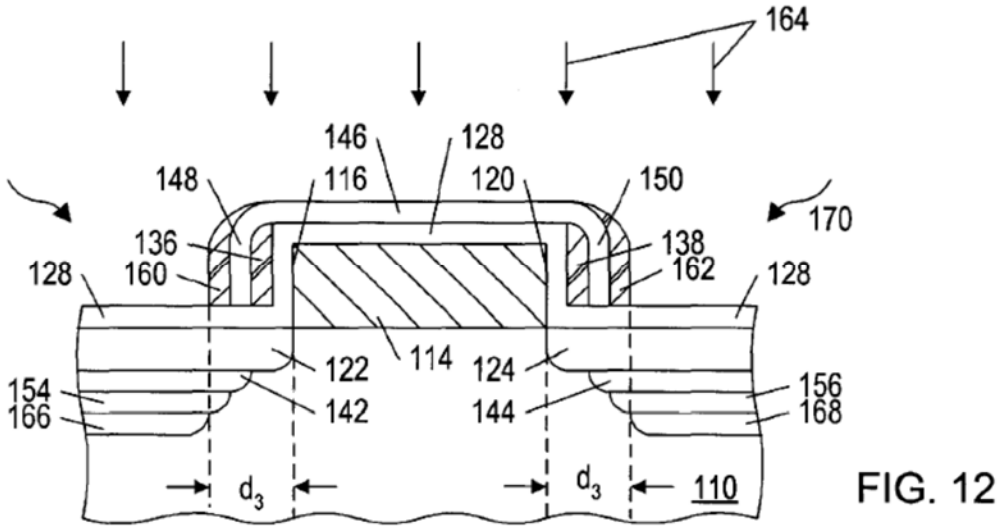


FIG. 12

AMD 680 discloses claim 12 as discussed in section X. H. above. For example, Fig. 12 shows a semiconductor component with a third oxide layer 148 interposed between first and third nitride spacers 136/160 and a fourth oxide layer 150 interposed between second and fourth nitride spacers 138/168. *See* Ex. 1005 ¶193; Ex. 1003, *id*.

Thus, a POSA would have understood that AMD 680 discloses each and every limitation recited in dependent claims 8, 9 and 12, and as a consequence, anticipates those claims.

C. AMD 680 Anticipates Independent Claim 14

AMD 680 discloses each and every limitation recited in independent claim 14, and as a consequence, anticipates that claim. AMD 680 discloses the preamble of claim 14 as discussed in section X. I. above.

AMD 680 discloses 14(a) as discussed in section X. I. above. For example, Fig. 6 below shows a semiconductor component manufactured on a semiconductor substrate 110 comprised of a lightly doped n-type or p-type silicon material having a major surface. *See* Ex. 1005, ¶197; Ex. 1003, 1:16-18, 7:60-63 & Fig. 6:

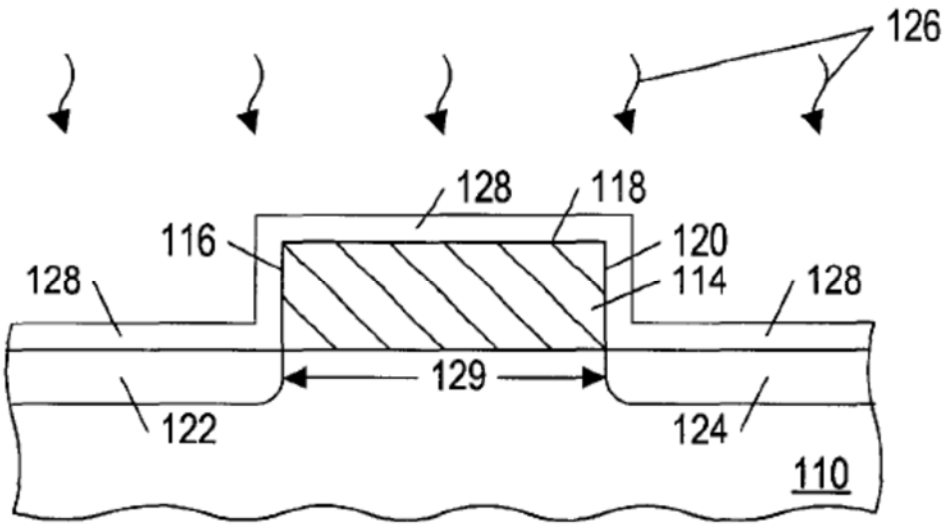


FIG. 6

AMD 680 discloses 14(b) as discussed in section X. I. above. For example, Fig. 6 above shows a semiconductor component with a gate structure 114 disposed over the substrate 110 and having a top surface 118 and gate sidewalls 116 and 120. *See* Ex. 1005, ¶198; Ex. 1003, 7:63-67 & Fig. 6.

AMD 680 discloses 14(c) and 14(d) as discussed in section X. I. above. For example, Figs. 6, 8 and 12 above show a semiconductor component with a first portion of oxide layer 128 formed on a portion of gate sidewall 116 and a second portion of oxide layer 128 formed on a portion of gate sidewall 120. *See* Ex. 1005, ¶199; Ex. 1003, Figs. 6, 8 & 12 (reproduced above).

AMD 680 discloses 14(e), (f), (g) and (h) as discussed in section X. I. above. For example, Fig. 12 below shows a semiconductor component having a first nitride spacer 136 formed adjacent to a first portion of oxide layer 128 (first dielectric material), a second nitride spacer 138 formed adjacent to a second portion of the oxide layer 128, a third nitride spacer 160 formed on one side of the first portion of oxide layer 128, and a fourth nitride spacer 162 formed on the other side of the second nitride spacer 138. *See* Ex. 1005, ¶200; Ex. 1003, 8:23-32, 9:20-22 & Fig. 12:

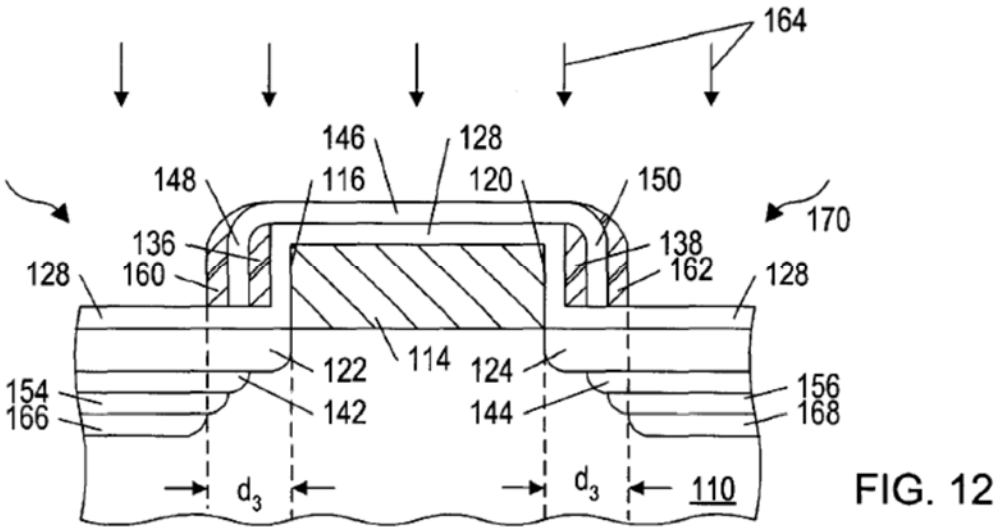


FIG. 12

Accordingly, a POSA would have understood that AMD 680 discloses each and every limitation recited in independent claim 14 of the '620 patent, and as a consequence, anticipates that claim. *See* Ex. 1005, ¶201.

For at least the reasons set forth above, Petitioner respectfully requests the Board find claim 14 unpatentable.

D. AMD 680 Anticipates Dependent Claims 16-20

AMD 680 discloses claim 16 and 17 as discussed in section X. J. above. For example, Fig. 12 above shows an oxide layer 148 interposed between the first nitride spacer 136 and the third nitride spacer 160 and an oxide layer 150 interposed between the second nitride spacer 138 and the fourth nitride spacer 162. *See* Ex. 1005, ¶202; Ex. 1003, Fig. 12 (above).

AMD 680 discloses claim 18 as discussed in section X. J. above. For example, Fig. 12 above shows a semiconductor component with a first doped region 142 aligned to the first nitride spacer 136 and second doped region 144 aligned to the second nitride spacer 138. *See* Ex. 1003, Fig. 12. The first and second doped regions 142/144 are of a second conductivity type different from the first conductivity type of the semiconductor substrate 110. *See* Ex. 1005, ¶203; Ex. 1003 *id*.

AMD 680 discloses dependent claim 19 as discussed in section X .J. above. For example, Fig. 12 above shows a semiconductor component comprised of a third doped region 166 aligned with the third nitride spacer 160 and a fourth doped region 168 aligned with the fourth nitride spacer 162. *See* Ex. 1005, ¶204; Ex. 1003, Fig. 12. The third and fourth doped regions comprised of a second conductivity type different from the first conductivity type of the semiconductor substrate 110. *Id*.

AMD 680 discloses claim 20 as discussed in section X.J. above. The first and second portions of oxide layer 128 are made of oxide. *See* Ex. 1005, ¶205; Ex. 1003, 8:13-17 & Fig. 7. Oxide layer 128 may be a thermally grown oxide or chemical vapor deposited oxide. *Id.* 5:37-42.

Thus, a POSA would have understood that AMD 680 discloses each and every limitation of claims 7-9, 12, 14 and 16-20 of the '620 patent, and as a consequence, anticipates those claims. A claim chart for AMD 680 is attached as Exhibit 1007.

For at least the foregoing reasons, Petitioner respectfully requests the Board find claims 7-9, 12, 14 and 16-20 unpatentable.

XII. GROUND 3: CLAIMS 1-3 AND 13 ARE OBVIOUS OVER AMD 680 IN VIEW OF THE KNOWLEDGE OF ONE OF ORDINARY SKILL IN THE ART

AMD 680 combined with the knowledge of one of ordinary skill in the art renders obvious each of the limitations recited in claims 1-3 and 13 of the '620 patent.

A. The Scope And Content Of The Prior Art

AMD 680 and the knowledge of one of ordinary skill in the art are discussed in Section X. A. above.

B. The Level Of Skill In The Art

Petitioner provides the level of ordinary skill in the art in Section IX. C. above.

C. The Potential Differences Between AMD 680 And Claims 1-3 And 13 Of The ’620 Patent Would Have Been Obvious In View Of The Knowledge Of One Of Ordinary Skill In The Art

AMD 680 discloses all of the limitations recited in independent claim 1 of the ’620 patent except it does not explicitly disclose the claim limitation specifying the thickness of the oxide layer. But as noted above, forming a dielectric layer (e.g., oxide layer) having a particular thickness would have been an obvious design choice to a POSA. Ex. 1005, ¶207. Further, the ’620 patent acknowledges that forming dielectric layers of a specified thickness was within the knowledge of a POSA at the time. *See* Ex. 1001, 3:30-36; Ex. 1005, *id*.

D. Claim 1

AMD 680 discloses the preamble of claim 1 as discussed in section X.A.7. above. Ex. 1003, 1:11-14.

AMD 680 discloses 1(a) as discussed in section X. E. above. *See,* Ex. 1005, ¶209; Ex. 1003, Fig. 6:

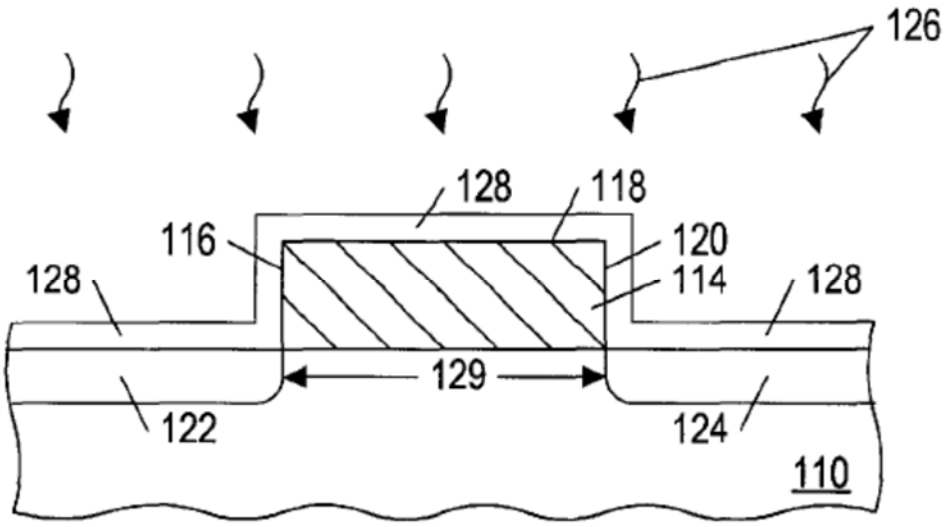


FIG. 6

Fig. 6 above shows a semiconductor component made from a semiconductor material of a first conductivity type and having a major surface. In particular, the semiconductor component is manufactured on a semiconductor substrate 110 comprised of a lightly doped n-type or p-type silicon material that includes at least on major surface. Ex. 1005 ¶210; Ex. 1003, 1:16-18 & 7:60-63.

AMD 680 discloses 1(b) as discussed in section X. E. above. For example, Fig. 6 above shows a semiconductor component with a gate structure 114 disposed over the substrate 110 and having a top surface 118 and sidewalls 116 and 120. *See* Ex. 1005 ¶211; Ex. 1003, 7:63-67 & Fig. 6.

The combined teachings of AMD 680 and the knowledge of one of ordinary skill in the art disclose all the limitations of 1(c). *See* Ex. 1005, ¶212; Ex. 1003, 8:23-32 & Fig. 7. AMD 680 discloses all of the limitations of 1(c) except it does not explicitly disclose the thickness of the oxide layer is less than 100 Å. For

example, Fig. 7 below depicts a semiconductor component having a first nitride spacer 136 disposed adjacent to sidewall 116 of the gate structure 114. The first nitride spacer 136 is spaced apart from the gate structure 114 by an oxide layer 128 interposed between the first nitride spacer 136 and the gate structure 114.

Ex. 1005 ¶212; Ex. 1003, Fig. 7:

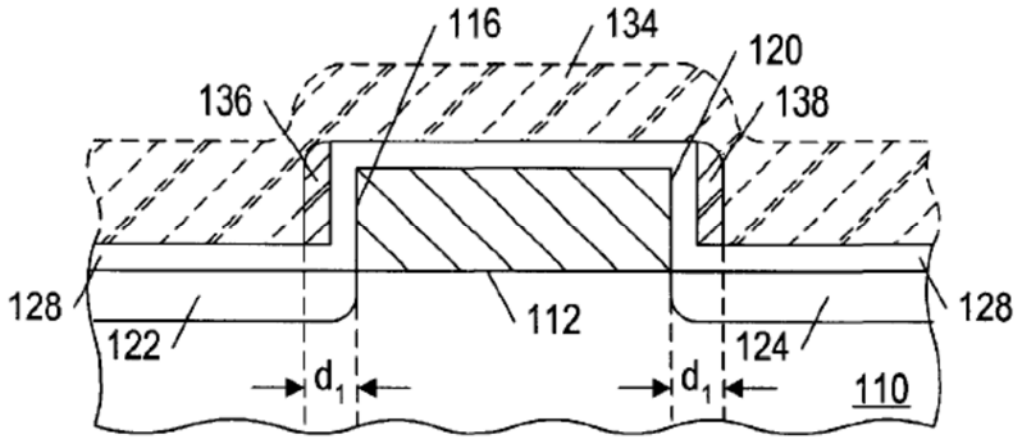


FIG. 7

As discussed previously, although AMD 680 does not explicitly disclose the thickness of the oxide layer is less than 100 Å, a POSA would have understood the thickness of the oxide layer to be an obvious design choice. Ex. 1005, ¶213. AMD 680 teaches depositing a conformal oxide layer on a semiconductor material using a Chemical Vapor Deposition (CVD) process. *Id*. CVD is commonly used to deposit conformal films and augment substrate surfaces. *Id*. CVD is very useful in the process of atomic layer deposition for depositing extremely thin layers of material. *Id*.

The'620 patent specification makes clear that those skilled in the art would have been apprised of known techniques for forming oxides, including thermal oxidation and CVD. *See* Ex. 1001, 8:23-32. Thermally growing a thin layer of dielectric material such as oxide (or, alternatively, depositing it using a CVD process) with a thickness less than 100 Å using a CVD process was within the knowledge of one skilled in the art the time, and such person would have known thermal oxidation or CVD to be useful specifically for that purpose. *See* Ex. 1005, ¶214.

Thus, it would have been obvious to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer with the knowledge of a POSA concerning the various known techniques for specifying the thickness of an oxide layer to be, e.g., less than 100 Å. These combined teachings rendered obvious the limitations recited in 1(c). *See* Ex. 1005, ¶215.

AMD 680 discloses 1(d) as discussed in section X. E. above. For example, Fig. 8 below depicts a semiconductor device with a first doped region 142 that is aligned to the first nitride spacer 136. *See* Ex. 1005, ¶216; Ex. 1003, Fig. 8:

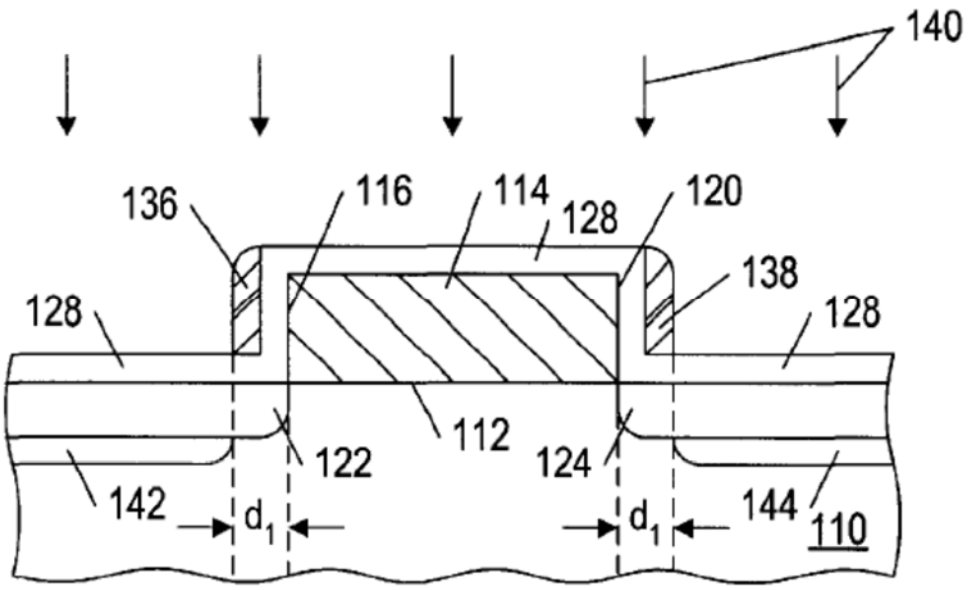


FIG. 8

See also id., 8:35-37 ("FIG. 8 illustrates a second concentration of dopants 140 implanted into semiconductor substrate 110 to form second implant regions 142 and 144 within the junctions."); 8:45-47 ("Dopants 140 are implanted into semiconductor substrate 110 a spaced distance d1 from sidewall surfaces 116 and 120 due to masking incurred by nitride spacers 136 and 138.")

AMD 680 discloses 1(e) as discussed in section X. E. above. For example, Fig. 12 below shows a semiconductor component with a second nitride spacer 160 formed on the left side of the first nitride spacer 136. Ex. 1005, ¶217; Ex. 1003, Fig. 12:

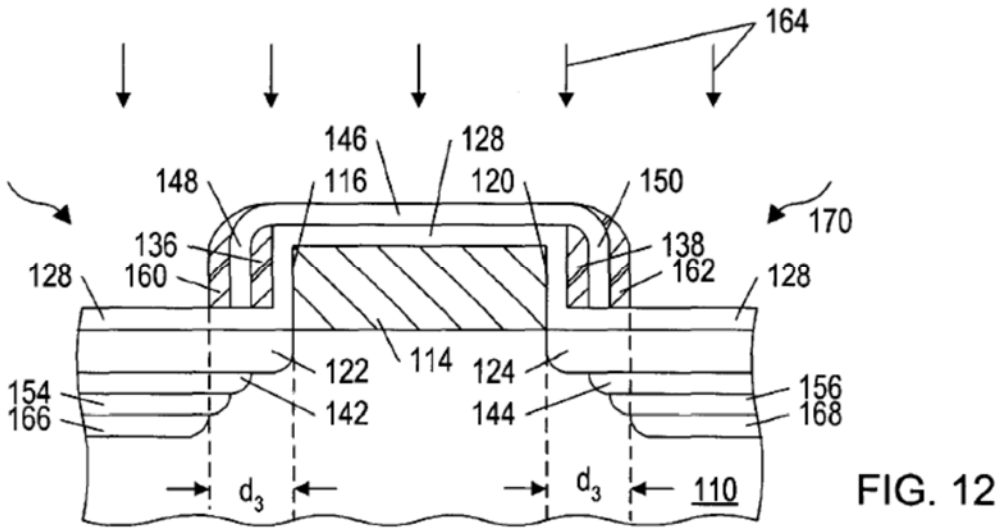


FIG. 12

AMD 680 discloses 1(f) as discussed in section X. E. above. For example, Fig. 12 above shows a semiconductor component with a second doped region 166 that is aligned to the second nitride spacer 160. *See* Ex. 1005, ¶218; Ex. 1003 9:20-34 & Fig. 12.

AMD 680 discloses 1(g) as discussed in section X. E. above. For example, Fig. 12 above shows a semiconductor component with a third doped region 124 aligned to gate sidewall 120. *See* Ex. 1005, ¶219: Ex. 1003, Fig. 12 & 8:1-8 ("A first concentration of dopants is implanted into semiconductor substrate 110 to form a first implant area within the junctions of the ensuing transistor. The first implant area is henceforth referred to as LDD regions 122 and 124. LDD implants 122 and 124 are substantially adjacent to gate conductor 114 and, more specifically, adjacent to channel area 129 underneath gate conductor 114.").

Accordingly, the combination of AMD 680 with the knowledge of a POSA renders obvious each and every limitation recited in independent claim 1 of the '620 patent. For at least the reasons set forth above, Petitioner respectfully requests that this Board find claim 1 unpatentable.

E. Claim 2

The combined teachings of AMD 680 and the knowledge of a POSA disclose the limitations of claim 2. As discussed in section X. F. above, AMD 680 discloses all of the limitations of claim 2 except it does not explicitly disclose the thickness of the oxide layer is less than 100 Å. *See* Ex. 1005, ¶221; Ex. 1003, Fig. 12:

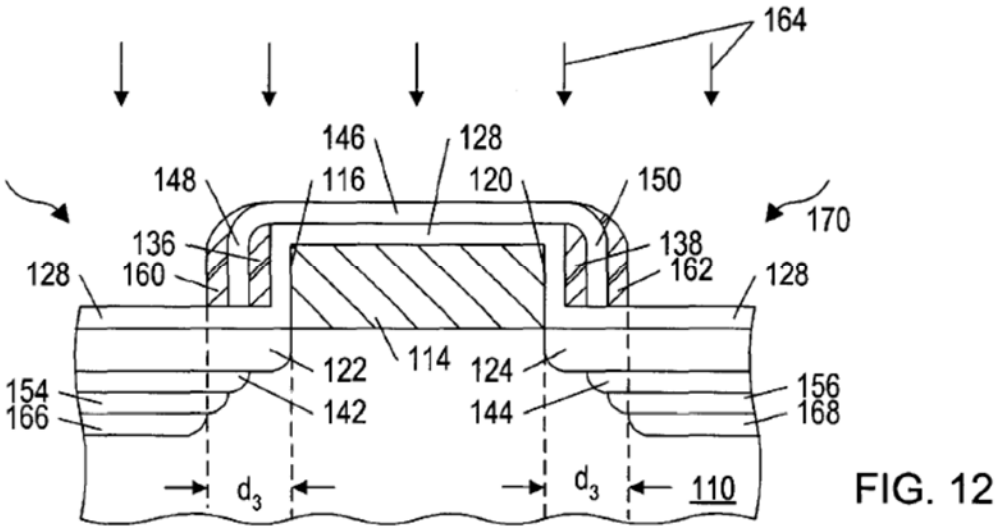


FIG. 12

Fig. 12 above depicts a third nitride spacer 138 adjacent to sidewall 120 of gate structure 114 that is spaced apart from the gate structure by oxide layer 128. It would have been obvious to modify AMD 680 and/or combine the teachings of

AMD 680 concerning formation of an oxide layer with the knowledge of a POSA concerning the various techniques used for specifying the thickness of dielectric materials, such as oxides to be, e.g., less than 100 Å, as established above for claim 1. *See* Ex. 1005, ¶222. These combined teachings render obvious the limitations recited in claim 2. *Id.*

F. Claim 3

AMD 680 discloses claim 3 as discussed in section X. F. above. For example, Fig. 12 above shows a fourth nitride spacer 162 formed on the side of the third nitride spacer 138. *See* Ex. 1005, ¶223; Ex. 1003 Fig. 12 (above).

G. Claim 13

AMD 680 in view of the knowledge of a POSA discloses the limitations of dependent claim 13. As discussed in section X. H. above, AMD 680 discloses all of the limitations of claim 13 except it does not explicitly disclose the thickness of the oxide layer is in the range from 10 to 60 100 Å. But, as noted above, a POSA would have understood the thickness of the oxide layer to be an obvious design choice. *See* Ex. 1005, ¶224.

Thus, it would have been obvious to modify AMD 680 and/or combine the teachings of AMD 680 concerning formation of an oxide layer with the knowledge of a POSA concerning the various known techniques for specifying the thickness

of the oxide layer. These combined teachings render obvious the limitations recited in claim 13 of the '620 patent. *See* Ex. 1005, ¶225.

Accordingly, a POSA would have understood that the combined teachings of AMD 680 in view of the knowledge of a POSA render obvious each and every limitation recited in claims 1-3 and 13 of the '620 patent. A claim chart for AMD 680 in view of the knowledge of a POSA is attached as Exhibit 1008.

For at least the foregoing reasons, Petitioner respectfully requests that the Board find claims 1-3 and 13 unpatentable.

XIII. ANY SECONDARY CONSIDERATIONS ARE INSUFFICIENT TO OVERCOME THE OBVIOUSNESS OF CLAIMS 1-20.

Patent Owner has the burden of establishing the existence and sufficiency of any secondary considerations of non-obviousness, as well as their nexus and commensurateness with the claims. *Ex parte Gelles*, 22 USPQ2d 1318, 1319 (Bd. Pat. App. & Inter. 1992); *Galderma Labs., L.P. v. Tolmar, Inc.*, 737 F.3d 731 (Fed. Cir. 2013) ("Where there is a range discloses in the prior art, and the claimed invention falls within that range, the burden of production falls upon the patentee to come forward with evidence that (1) the prior art taught away from the claimed invention; (2) there were new and unexpected results relative to the prior art; or (3) there are other pertinent secondary considerations.) Although secondary considerations must be considered, they do not control the obviousness conclusion. *See Newell Cos., Inc. v. Kenney, Mfg. Co.*, 864 F.2d 757, 768 (Fed. Cir. 1988).

And, in cases where a strong *prima facie* obviousness showing exists, the Federal Circuit has repeatedly held that even relevant secondary considerations supported by substantial evidence may not dislodge the primary conclusion of obviousness. *See, e.g., Leapfrog Enters. Inc. v. Fisher-Price Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007). Petitioner is not aware of any secondary considerations that would support the non-obviousness of the challenged claims, and, in any event, the *prima facie* case of obviousness presented herein could not be overcome with any such considerations that Patent Owner may forward. *See id*.

XIV. CONCLUSION

For the foregoing reasons, SMIC respectfully requests *inter partes* review of Claims 1-20 of U.S. Patent No. 6,933,620 and cancellation of those claims as unpatentable.

Respectfully submitted,

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XV. CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that this Petition complies with the type-volume limitation of 37 C.F.R. § 42.24(a). The word count application of the word processing program used to prepare this Petition indicates that the Petition contains 13,273 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,933,620, including all exhibits were served on April 14, 2020 via e-mail and Federal Express in its entirety on the correspondence address of record for the '620 Patent shown in USPTO PAIR (no attorney or agent address was listed):

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