UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NICHIA CORPORATION,
Petitioner

v.

DOCUMENT SECURITY SYSTEMS, INC.,
Patent Owner

Case No. IPR2020-00908
Patent No. 6,879,040

Petition for *Inter Partes* Review

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1001	U.S. Patent No. 6,879,040
1002	File History of U.S. Patent No. 6,879,040
1003	Declaration of Dr. James Richard Shealy
1004	Japanese Unexamined Patent Application Publication No. 10-200038 ("Kim") with certified English translation
1005	Japanese Unexamined Patent Application Publication No. 6-350206 ("Adachi") with certified English translation
1006	Japanese Unexamined Patent Application Publication No. 2000-77725 ("Nagayama") with certified English translation
1007	Japanese Unexamined Patent Application Publication No. 6-90026 ("Okazaki") with certified English translation
1008	U.S. Patent No. 5,821,615 ("Lee")
1009	Plaintiff Document Security Systems, Inc.'s Opposition to Defendants' Motion to Dismiss Plaintiff's Complaint Under Fed. R. Civ. P. 12(b)(6), *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172 (C.D. Cal.) (Dkt. No. 23)
1010	Exhibit A to Plaintiff Document Security Systems, Inc.'s Disclosure of Asserted Claims and Infringement Contentions, *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172 (C.D. Cal.)
1011	Joint Claim Construction and Prehearing Statement (N.D. Cal. P.R. 4-3), *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172 (C.D. Cal.) (Dkt. No. 39)
1012	Excerpt from Butterfield, A., Szymanski, J., *A Dictionary of Electronics and Electrical Engineering* (5th ed.), OUP Oxford, United Kingdom (2018)
1013	Excerpt from *The Authoritative Dictionary of IEEE Standards Terms*, Seventh Edition, IEEE Press (2000)
1014	Excerpt from Merriam-Webster Dictionary, available at https://www.merriam-webster.com/dictionary/conform

Exhibit No.	Description
1015	Excerpt from *The American Heritage Dictionary of the English Language*, available at https://www.ahdictionary.com/word/search.html?q=conform
1016	*The American Heritage Dictionary of the English Language* (4th ed.) (2006)
1017	Letter dated April 3, 2020 to P. Colsher from Brian Ledahl, counsel for Patent Owner in related case, *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172 (C.D. Cal.)
1018	Letter dated April 10, 2020 to P. Colsher from Brian Ledahl, counsel for Patent Owner in related case, *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172 (C.D. Cal.)
1019	Japanese Examined Patent Publication No. 7-50754B2 ("Shirahata") with certified English translation
1020	U.S. Patent No. 5,428,248 ("Cha")
1021	Excerpt from Microelectronics Packaging Handbook, edited by Tummala, R. R., Rymaszewski, E. J., and Klopfenstein A. G., Van Nostrand Reinhold, New York (1989)
1022	Japanese Unexamined Patent Application Publication No. 10-116952 ("Kuwabata") with certified English translation
1023	Japanese Unexamined Patent Application Publication No. 2001-077277 ("Makimoto") with certified English translation

Nichia Corporation ("Petitioner") respectfully requests *Inter Partes* Review ("IPR") of claims 1-4, 8, and 11 (the "Challenged Claims") of U.S. Patent No. 6,879,040 (Ex. 1001, "the '040 patent"), currently assigned—according to Patent Office records—to Document Security Systems, Inc. ("Patent Owner"). There is a reasonable likelihood Petitioner will prevail on at least one challenged claim.

I. Mandatory Notices (37 C.F.R. §42.8)

A. Real Parties in Interest (37 C.F.R. §42.8(b)(1))

The real parties in interest are Nichia Corporation and Nichia America Corporation.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The Challenged Claims constitute the entirety of the claims asserted by Patent Owner against Nichia Corporation and Nichia America Corporation in *Document Security Systems, Inc. v. Nichia Corporation, et al.*, No. 2:19-cv-08172, pending in the United States District Court for the Central District of California ("the Related Court Case"). In this case, discovery has just begun, every significant case deadline remains (including claim construction briefing and the *Markman* hearing), and trial is set for about one and a half years from now. Petitioner and Nichia America Corporation are filing a motion to stay the Related Court Case.

C. Counsel and Service Information (37 C.F.R. §§42.8(b)(3)-(4))

Petitioner designates the following lead and back-up counsel:

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Petitioner consents to e-mail service at the above e-mail addresses and nichia-dss@shearman.com.

II. Payment of Fees (37 C.F.R. §42.103)

The Director is authorized to charge the filing fee for this Petition, as well as any other fees that may be required in these proceedings, to Deposit Account 500324.

III. Requirements for *Inter Partes* Review (37 C.F.R. §42.104)

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the ’040 patent is available for IPR, and that Petitioner is not barred or estopped from requesting an IPR challenging the claims on the identified grounds.

B. Identification of Challenge (37 C.F.R. §42.104(b)(1)-(2)) and Relief Requested (37 C.F.R. §42.22.(a)(1))

Petitioner requests the Board institute IPR on the Challenged Claims because they are anticipated or obvious under pre-AIA 35 U.S.C. §§102 and 103 on the following grounds:

Ground	Prior Art	Basis	Claims Challenged
1	Japanese Unexamined Patent Application Publication No. 10-200038 (“Kim”)	§102	1-3, 11
2	Kim in view of Japanese Examined Patent Publication No. 7-50754B2 (“Shirahata”)	§103	8

Ground	Prior Art	Basis	Claims Challenged
3	Japanese Unexamined Patent Application Publication No. 6-350206 ("Adachi")	§102	1-4, 8
4	Japanese Unexamined Patent Application Publication No. 2000-77725 ("Nagayama")	§102	1-4, 8
5	Japanese Unexamined Patent Application Publication No. 6-90026 ("Okazaki")	§102	1-4, 8, 11

IV. Relevant Information Concerning the Contested Patent

A. Overview of the '040 Patent

The '040 patent relates to widely-used "[s]urface mount technology (SMT), where devices are mounted directly onto a surface…." Ex. 1001, 1:10-12.

The patent explains that "light emitting diode (LED) devices … based on surface mount technology are very small in size and are assembled onto a printed circuit board (PCB)," and that "usage of [LEDs] has increased (in indoor and outdoor applications) in the area of backlighting, electronic signs/symbols such as variable message signs, or large full color video screens etc." *Id.*, 1:10-22. In these applications, LEDs are "assembled in packages"; and, "the larger the package size, the fewer the devices that can be mounted and the lower the display resolution." *Id.*, 1:30-39.

According to the patent, prior-art surface mount LED devices, *e.g.*, those presented in Figures 1A and 2A (below), limit display resolution, because "the soldered [joints, 111 and 211, respectively] and the electrically conductive members [102 and 202, respectively] extend outside the edges of the plastic body [106 and 206, respectively]." *Id.*, 2:15-17; *see also* 1:42-2:14.

Figure 1A (Prior Art)

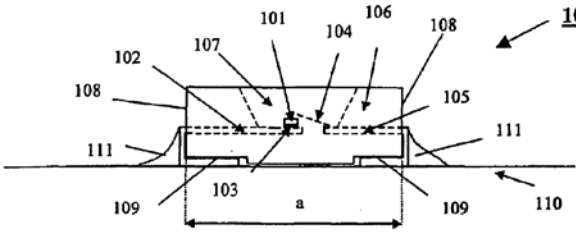
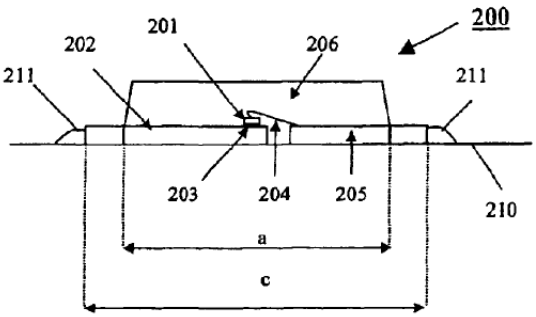


Figure 2A (Prior Art)



Id., Figs. 1A, 2A.

Further, in the prior art, "the extended electrically conductive members and solder joints are visibly exposed to an observer and because of their high reflectivity, cause an undesirable disturbance to the eyes." *Id.*, 2:39-43.

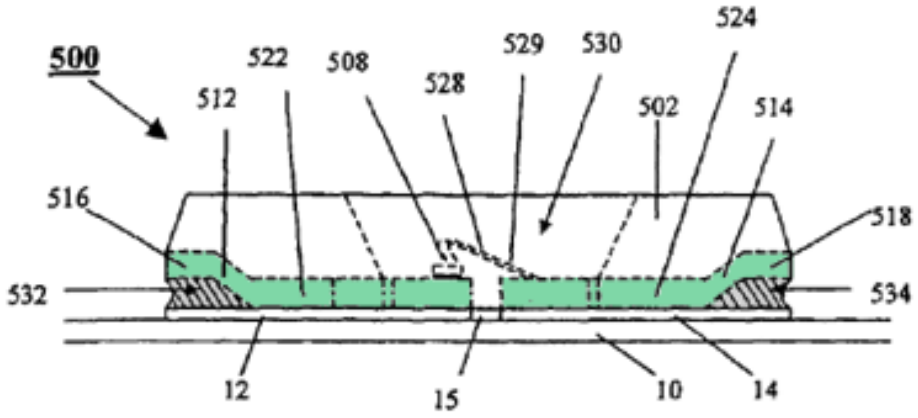
To allegedly address these deficiencies, the '040 patent is directed to "a surface mountable electronic device that includes: a body with a first, mounting surface for mounting the device. The first surface is recessed with recessed portions in it. There are also at least two electrical contacts in the

first surface. The electrical contacts include first portions [with] gaps beneath them when the device is mounted." *Id.*, 2:55-62. These gaps, *i.e.*, "the space[s] between a planar surface and the first portions [of the electrical contacts], when the device is mounted on a planar surface, can be filled [*e.g.*, with solder] to adhere the device to the planar surface." *Id.*, 4:23-26.

According to the patent, the resulting greater surface area for solder contact allows for a "strong bond." *Id.*, 10:1-4.

A representative embodiment is depicted in Figure 10 (below), and includes a body (502), an LED (508) on a first electrical contact (which includes portions 516, 512, and 522), a second electrical contact (which includes portions 518, 514, and 524) and solder fillets (532 and 534). *Id.*, 5:37-65, 8:58-59, 8:66-9:20.

Figure 10



Id., Fig. 10 (annotation shows electrical contacts shaded green and solder

shaded gray);[1] *see also* Figs. 5A-5B (also depicting device 500); Ex. 1003, ¶¶ 52-53.[2]

B. Overview of the ’040 Patent Prosecution History

The application leading to the ’040 patent was filed August 26, 2003, and claims priority to a foreign application filed September 18, 2002. Originally filed claims 1 and 2 are instructive:

> 1. A surface mountable electronic device, comprising:
>
> a body with a first surface for mounting the device;
>
> recessed portions within the first surface; and
>
> a plurality of electrical contacts in said first surface, said electrical contacts including first portions which form at least a portion of at least one inner surface of said recessed portions.
>
> 2. The device of claim 1, wherein (1) each of the electrical contacts extends, at least partially, along said first surface; and (2) if said first surface were mounted on a planar surface, the first portions would be spaced apart from said planar surface.

Ex. 1002, 2.

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[1] All coloring to figures has been added.

[2] Declaration of Dr. James Shealy, an expert in semiconductor—including LED—packaging. Ex. 1003, ¶¶ 7-16; *see also* CV attached to same.

Original claim 1 was directed to a "surface mountable electronic device," and specifically required that that "device" have "a body with a first surface for mounting the device." The claim further required "recessed portions within the first surface; and a plurality of electrical contacts in said first surface." Last, the claim required that "said electrical contacts includ[e] first portions which form at least a portion of at least one inner surface of said recessed portions." In short, original claim 1 described a device having a body whose mounting surface ("the first surface") has recessed portions, and wherein electrical contacts form at least one inner surface of those recessed portions.

Original claim 2 added to original claim 1 the concept of a second "***planar*** surface," as well as a space between the electrical contacts and that surface—the space being the result of the recessed portions of the mounting surface: "if said first surface were mounted on a planar surface, the first portions [of the electrical contacts] would be spaced apart from said planar surface."

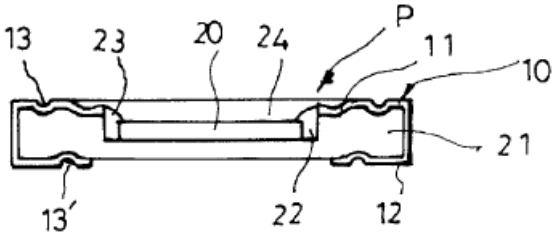
On June 25, 2004, the examiner rejected original claims 1, 2, 4, 8, 9, 11, and 14 as anticipated by U.S. 5,821,615 ("Lee") (Ex. 1008), and rejected all remaining claims as obvious over Lee in combination with other

references. Ex. 1002, 77, 79, 81. With respect to original claim 1, the examiner stated:

> Lee discloses a surface mountable electronic device (SMD- Fig. 2) comprising:
>
> - a body with a first/bottom surface (see the bottom of 21 in Fig. 2) for mounting the device
> - recessed/crooked portions within/on the first surface (see recessed surfaces ***on the bottom of 21*** in Fig. 2), the recessed portions having crooked/staple shape
> - a plurality of electrical contacts on/in the first surface (***see 13' and 12*** in Fig. 2), the electrical contacts ***including*** the first recessed portions which form a portion of the inner surface of the recessed portions of the body (see 13' in Fig. 2)….

Id., 77 (emphasis added) (referencing Lee, Fig. 2 (below)).

FIG. 2



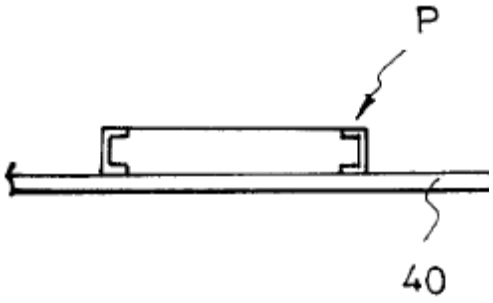
Ex. 1008, Fig. 2.

With respect to original claim 2, the examiner added:

> Lee further teaches:

- each of the electrical contacts extending along said first surface, and
- when the first surface is mounted on a planar surface, the first portions would be spaced apart from the planar surface due to the presence of the recessed portions (see Fig. 4A in combination with the device of Fig. 2; Col. 3, line 63).

Ex. 1002, 78 (referencing Lee, Fig. 4A (below)).



Ex. 1008, Fig. 4A; *see also* 2:39-42.

In a September 24, 2004 response, the applicants amended claim 1 "to recite that a mounting surface of the device has 'recesses ***at side edges*** of the device', [and] that each of a plurality of electrical contacts '***extends from an interior portion*** of the mounting surface and ***terminates in one of said recesses***…'" Ex. 1002, 95 (emphasis added). These amendments directly address Lee's recesses—which, at least in cross-sectional view, are not at the side edges—and Lee's electrical contacts—which wrap around the sides and continue past the recesses. Ex. 1003, ¶¶ 66-69. In that same response, the

applicants cancelled claim 2 and further amended claim 1 "to recite … that 'said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts,'" essentially incorporating some of the concepts of claim 2 into claim 1. Ex. 1002, 95; Ex. 1003, ¶ 70.

The resulting claim 1 read:

> A surface mountable electronic device, comprising:
> a body ~~with a first surface for mounting the device;~~
> ~~recessed portions within the first surface~~ <u>having a mounting surface, the mounting surface having a plurality of recesses at side edges of the device</u>; and
> a plurality of electrical contacts ~~in said first surface, said electrical contacts including first portions which form at least a portion of at least one inner surface of said recessed portions~~<u>, each of which extends from an interior portion of the mounting surface and terminates in one of said recesses, and each of which conforms to one of said recesses, wherein said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts</u>.

Ex. 1002, 92.

The applicants also cancelled original claims 8-12 and 14; amended original claims 3-7; and added claims 16-21 (which issued as claims 9-14).

Id., 92-94. The applicants asserted that "[s]upport for the[] amendments [to claim 1] is found, at least, on p. 8, lines 2-8, and in FIGS. 4A-12." *Id.*, 95.

Claim 18 was written to read:

> Claim 18 (new): The device of claim 1, wherein one or more of the recesses is bounded on three sides by said mounting surface.

Id., 94.

To show written description support, the applicants stated: "New claim 18 reads on FIGS. 4A, 5A, 8A & 9A." *Id.*, 95.

Figure 4A is below, along with Figure 4B, showing a top view of the same embodiment.

Figure 4A

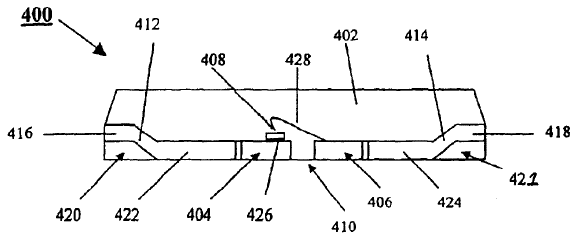
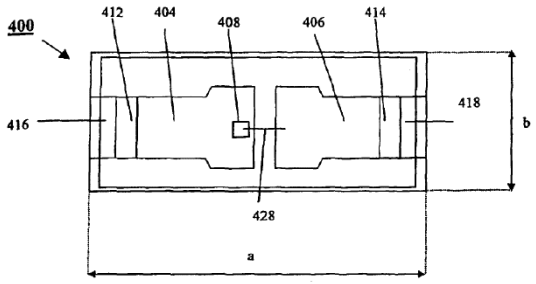


Figure 4B



Ex. 1001, Figs. 4A-4B.

Claim 1 was allowed after an Examiner's amendment:

> A surface mountable electronic device, comprising:
> a packaged body having a mounting surface, the mounting surface having a plurality of recesses at side edges of the [device] body; and….

Ex. 1002, 105.

Claim 18 was allowed, and issued as claim 11, after an Examiner's amendment deleting "by said mounting surface." *Id*.

C. Person of Ordinary Skill in the Art

Several factors may be considered in determining the proper skill level:

> The person of ordinary skill … is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill … may include: (A) "type of problems encountered in the art;" (B) "prior art solutions to those problems;" (C) "rapidity with which innovations are made;" (D) "sophistication of the technology; and" (E) "educational level of active workers in the field."

M.P.E.P. §2141.03.

Here, the level of skill is apparent from the cited art. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Petitioner submits that a person of ordinary skill in the art ("POSA") would have had at least a B.S. in mechanical or electrical engineering or a related field, and four years' experience designing or developing semiconductor—including LED—packages. Ex. 1003, ¶ 31. This description is approximate—a higher

education or skill level might make up for less experience, and vice-versa. *Id*.

D. Claim Construction (37 C.F.R. §42.104(b)(3))

This Petition construes terms consistent with the understanding a POSA would have had, at the time of the invention, in view of the '040 patent's intrinsic evidence and, where appropriate, extrinsic evidence. *See* 83 Fed. Reg. 51340, Vol. 83, No. 197 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*). Only terms subject to a legitimate dispute need to be construed for the purposes of IPR. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs.* in context of IPR). Terms not expressly construed should be given their plain and ordinary meaning.

Petitioner perceives two contrasting sets of possible understandings of the overall structure of the claimed device. These understandings arise—at least in part—from the above-described amendments to original claim 1, as described in more detail below.

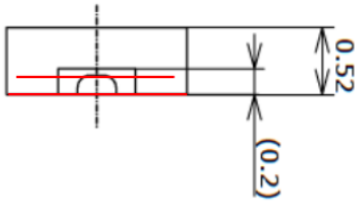
While ***original*** claims 1 and 2 set forth two distinct surfaces—(i) a "first surface for mounting the device," which surface has "recessed portions" and "electrical contacts" within, and (ii) a "planar surface," from

which surface the contacts in the recesses "would be spaced apart"—***issued*** claim 1 sets forth only a single "mounting surface," which ***both*** has "recesses" to which portions of the "electrical contacts" conform ***and*** is spaced apart from those contacts by "offsets." Ex. 1001, 11:17-27; Ex. 1003, ¶¶ 81-89.

In the Related Court Case, Petitioner asserts that the Challenged Claims are indefinite for various reasons, including impossibility. Ex. 1011, 7-9. The main indefiniteness argument is that, if the electrical contacts must ***conform to*** the recesses of the mounting surface of the body, there cannot also be ***offsets*** between those contacts and the mounting surface. *Id.* The other indefiniteness arguments are closely related.

Patent Owner proposes that the apparent "offset" impossibility is resolved if "[t]he mounting surface is the bottom surface of the device," (Ex. 1017, 2), and "the 'recess[es]' … are at the side edges of the packaged body and correspond to the space between the indented portion of the metal electrode and the bottom of the packaged body, ***as viewed from the side***,"

(Ex. 1018 (emphasis added)).[3] Similarly, in responding to Petitioner's motion to dismiss (on the pleadings) for indefiniteness (ultimately denied in the Related Court Case), Patent Owner alleged that a "gap" underneath the electrical contact could constitute the recited "offset…." Ex. 1009, 13-14. Consistently, in its infringement contentions in that case, Patent Owner identified the "offset" between the "mounting surface" (the lower red line) and the "electrical contacts" (indicated by the upper red line), as seen in a side view of the allegedly infringing product:



Ex. 1010, 2 (red line annotations made by Patent Owner).[4]

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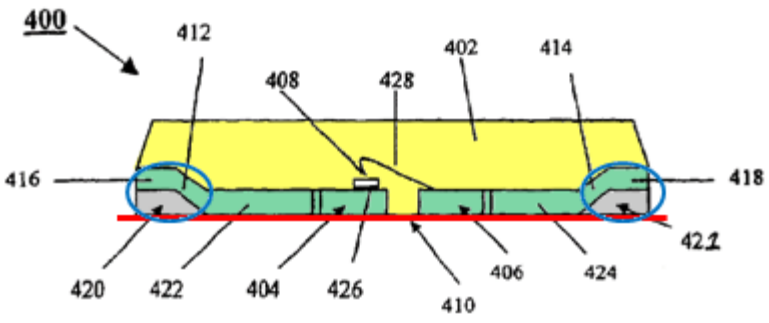
[3] Likewise, in the parties' Joint Claim Constructions and Prehearing Statement in the Related Court Case, Patent Owner alleges that "recesses" are "indentations or clefts that provide room for solder to mount the device." Ex. 1011, 3-4.

[4] In the parties' Joint Claim Constructions and Prehearing Statement in the Related Court Case, Patent Owner alleges that "offset" is "a portion of the electrical contact set apart from the mounting surface." Ex. 1011, 6.

In short, according to Patent Owner, the apparent impossibility is resolved if the "mounting surface" is a ***planar surface at which the device is mounted***, which surface is essentially co-planar with the planar bottom surface of the body, and which surface ***does not follow the contours of its recesses***. *See* Ex. 1003, ¶¶ 90-95.

And, indeed, with this understanding, the "recesses and electrical contacts" could be "sized to provide offsets between said mounting surface and said electrical contacts," as can be seen in Figure 4A, below. Ex. 1003, ¶ 96. The "packaged body" is yellow; the "mounting surface" (per Patent Owner's interpretation) is indicated by a red line; the "recesses" are the depressions or indentations at the side edges of the body (area defined by the recesses circled in blue); the "plurality of electrical contacts" are green, and terminate in the recesses; and the "offsets" are the gray regions between the green contacts and the mounting surface. Ex. 1003, ¶ 97.

Figure 4A

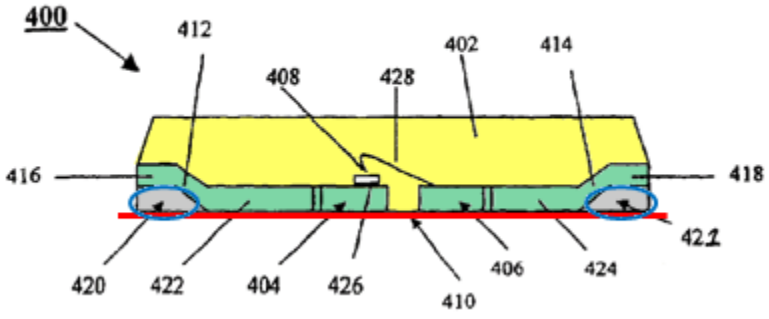


Ex. 1001, Fig. 4A; Ex. 1003, ¶¶ 96-97.

Therefore, in accordance with 37 C.F.R. §42.104(b)(3), Petitioner asks the Board—for the reasons described above—to construe the claims in a manner such that the "mounting surface" is a ***planar surface at which the device is mounted***, which surface is essentially co-planar with the planar bottom surface of the body, and which surface ***does not follow the contours of its recesses***.

From the Related Court Case, it seems that Patent Owner may also argue that the "recesses" are the depressions or indentations in the ***device as a whole*** (including the electrical contacts), as opposed to in the body. Ex. 1009, 13-14; Ex. 1010, 1-2; Ex. 1011, 3-4; Ex. 1017, 1; Ex. 1018. That would mean, with respect to Figure 4A, that the blue circles indicating the areas defined by the recesses would be adjusted as follows:

Figure 4A



Ex. 1001, Fig. 4A; Ex. 1003, ¶¶ 99-102. The "offsets" would be the gray areas (or the vertical heights thereof). Ex. 1003, ¶ 102.

Petitioner disagrees. Ex. 1003, ¶¶ 103-104. But, this "alternative" construction does not affect the Grounds below, as the prior art teaches both "recesses" in the body, as well as conforming electrical contacts, such that the contacts also have "recesses." Ex. 1003, ¶ 105. This "alternative" construction is addressed in footnotes below.

In addition, Petitioner asks the Board to construe the following terms in this IPR.

1. "packaged body"/"body"

The terms "packaged body" and "body" should be construed as a "protective shell to hold a semiconductor and electrical contacts."

This construction—which treats the "body" as distinct from the "electrical contacts"—is apparent from the structure (including the paragraphing structure) of claim 1, which is directed to a "surface mountable electronic device, comprising: a packaged body … and a plurality of electrical contacts…." Ex. 1001, 11:17-28; Ex. 1003, ¶¶ 108-110.

This construction would also be the understanding of a POSA in view of the specification, which distinguishes between the "body" and the "contacts" and "LED" that it protects, *e.g.*:

> ….Both contacts 102, 105 extend horizontally through the body 106 of the device 100 (in the orientation shown in FIG. 1A). Most of the body 106 is optically opaque, except for an inverted

frusto-conical cavity 107, in which the LED 101, bond wire 104 and inner ends of the two contacts 102, 105 are encased in an optically clear plastic….

* * *

….The whole body 206 of the device 200 is optically clear plastic. The two contacts 202, 205 extend horizontally outwards along the underside of the body 206, ending with horizontal portions outside the body 206.

* * *

….[T]he electrical contacts extend outwardly along the underside of the body, and the first portions are positioned towards the outside of the underside of said body....

* * *

….Such a device may then include at least one light emitting means provided within the body and electrically connected to the electrical contacts.

* * *

A surface mountable opto-electronic device 400 of a first embodiment is shown in FIGS. 4A-4B, with an optically transparent body 402, two generally flat electrical contacts, 404, 406 and an LED 408. The body 402 is generally rectangular in plan view…. The two electrical contacts 404, 406 are mounted in the underside 410 of the body 402….

* * *

….[T]he body 402 is an optically clear plastic that encapsulates the LED 408 and the top surfaces of the two contacts 404, 406.

* * *

….[T]he body 502 is an optically opaque plastic that encapsulates much of the top surfaces of the three electrical contacts 504, 506, 507….

* * *

….[T]he bodies of the devices are shown extending down to either the top surfaces of the contacts or to the bottom of the surfaces of the contacts[.] However, the bodies could extend to any level between the top surfaces of the electrical contacts and the bottom surfaces of the contacts…. Thus the contacts are, in effect, provided in recesses along the lengths of the bodies.

* * *

The contacts are shown with parallel top and bottom surfaces. Whilst preferred, this is not essential…. They could undulate, or have patterned surfaces to improve adhesion, whether to the body or to a solder….

* * *

The recesses are formed by the shape of the mould used during the molding of the body…. The recesses could extend across more or less than those widths…. The amount would be determined by the moulds used in molding the bodies.

Ex. 1001, 1:49-59, 2:4-11, 4:27-34, 4:35-39, 4:60-5:3, 5:26-28, 6:12-19, 9:50-61, 10:18-23, 10:30-38; *see also* Figs. 1-2, 4-12; Ex. 1003, ¶ 111.

Consistently, when criticizing prior art, *e.g*., those in Figures 1A and 2A, the ’040 patent refers to the electrical contacts and the bodies of the prior devices as distinct components: “the soldered [joints, 111 and 211, respectively] and the electrically conductive members [102 and 202, respectively, *i.e.*, the electrical contacts] extend outside the edges of the plastic body [106 and 206, respectively].” Ex. 1001, 2:15-17; *see also* 1:42-2:14; Ex. 1003, ¶ 112.

Extrinsic dictionary evidence is in accord. According to *A Dictionary of Electronics and Electrical Engineering* (5th ed.), a “package” is defined as: “The protective shell of material in which an integrated circuit and its electrical contacts are encapsulated….” Ex. 1012, 5. And, *The Authoritative Dictionary of IEEE Standards Terms* (7th ed.), defines “package” as: “An external container, substrate, or platform used to hold a semiconductor or circuit....” Ex. 1013, 11; Ex. 1003, ¶ 113.

2. “conforms to”

The claim term “conforms to” should be construed as “is adapted to and follows the shape of.”

This construction would be the understanding of a POSA in view of the specification, *e.g.*:

> ….The first surface is recessed with recessed portions in it. There are also at least two electrical contacts in the first surface.

> The electrical contacts include first portions which form at least a portion of at least one inner surface of the recessed portions....
>
> * * *
>
> An embodiment of a surface mount opto-electronic device of the present invention is provided with two electrically conductive members along its underside (first surface).
>
> * * *
>
> ….The first surface is recessed with recessed portions in it. There is also a plurality of contacts (usually two or three) in the first surface. The electrical contacts include first portions, surfaces of which form at least part of the inner surface of each recessed portion. Normally, the contacts extend along the first surface….
>
> * * *
>
> The three electrical contacts 504, 506, 507 are mounted in the underside, the mounting surface 510 of the body 502, such that the undersides of the contacts are accessible from below.

Ex. 1001, 2:54-62, 3:40-42, 3:60-4:4, 5:48-51; *see also* Figs. 4-7, 10-11; Ex. 1003, ¶¶ 115-16.

Extrinsic dictionary evidence is in accord. According to Merriam-Webster, "conforms" means "to give the same shape, outline, or contour to…"; and, according to *The American Heritage Dictionary of the English Language*, it means "to be similar in form or pattern: a windy road that

conforms to the coastline…." Ex. 1014, 1; Ex. 1015; *see also* Ex. 1016, 5 (defining "conform" as "1. To correspond in form or character; be similar …. 3. To act in accordance with current customs or modes. See synonym at adapt. —*tr*. To bring into agreement or correspondence; make similar."); Ex. 1003, ¶ 117.

3. "offset"

The claim term "offset" should be construed as "space."

This construction would be the understanding of a POSA in view of the specification, *e.g.*:

> ….[T]here is provided a surface mountable electronic device that includes: a body with a first, mounting surface for mounting the device. The first surface is recessed with recessed portions in it. There are also at least two electrical contacts in the first surface. The electrical contacts include first portions which form at least a portion of at least one inner surface of the recessed portions. Thus, there are gaps beneath them when the device is mounted.
>
> * * *
>
> Thus the invention provides a surface mountable electronic device that includes: a body with a first, mounting surface for mounting the device. The first surface is recessed with recessed portions in it. There is also a plurality of contacts (usually two or three) in the first surface. The electrical contacts include first portions, surfaces of which form at least part of the inner surface

of each recessed portion. Normally, the contacts extend along the first surface. If the first surface were mounted on a planar surface, the contacts would be in contact with that planar surface, whereas the first portions would be spaced apart from that planar surface.

* * *

The present devices are ideally constructed such that the space between a planar surface and the first portions, when the device is mounted on a planar surface, can be filled to adhere the device to the planar surface.

* * *

The device of the invention may be mounted on a printed circuit board…. Adhesive would fill the recesses between said first portions and the printed circuit board....

* * *

….[T]he recesses provide room for solder to mount the device to a PCB….

* * *

Solder fillets 532, 534 fill the recesses 520, 521 and electrically and adhesively connect the device contacts 504, 506, 507 to the solder pad terminals 12, 14. In this way, the Surface Mounted Device is effectively mounted on the PCB 10….

Ex. 1001, 2:54-62, 3:60-4:4, 4:23-26, 4:44-53, 5:29-38, 6:20-28, 9:18-24; Ex. 1003, ¶¶ 118-20; *see also* Ex. 1001, 6:62-7:2, 7:39-47, 8:11-18, 8:50-57, 9:62-10:4.

V. The Specific Grounds of Unpatentability

As evidenced by the prior art described herein, and the declaration of Dr. Shealy (Ex. 1003), surface mountable packages having recesses and electrical contacts sized to provide offsets between a mounting surface and the electrical contacts, in the manner claimed, were well known. The prior art teaches the claimed configurations, rendering the Challenged Claims anticipated and/or obvious.

A. Prior Art

No prior art relied upon was cited during prosecution.

1. Kim

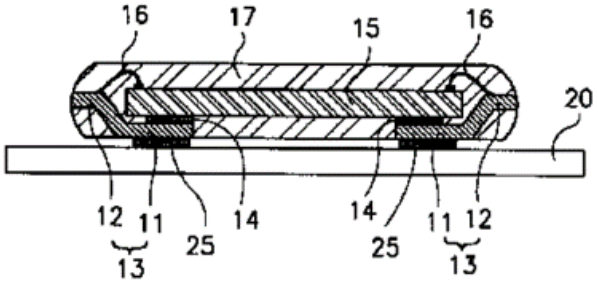
Kim, entitled "Bottom-lead semiconductor package and method for manufacturing the same," published July 31, 1998. Ex. 1004. It is prior art under 35 U.S.C. §102(b).

Kim is directed to "providing a bottom-lead semiconductor package [(BLP)] and a method for manufacturing the same, in which, in mounting the bottom-lead semiconductor package on a board such as a printed circuit board, a strong solder joint is made, the mounting height of the package can

be minimized, and the bottom leads can be arranged at a high density." *Id.*, ¶ 0007; Ex. 1003, ¶¶ 123-26.

Kim explains that prior art small outline packages (SOP), and small outline J-lead (SOJ) semiconductor chip packages, suffer from the disadvantage that "the external leads are exposed to the exterior of the lateral faces of the package body, [such that] when the package is mounted on the board, the occupied area ratio of the package, with respect to the board, is increased…." Ex. 1004, ¶¶ 0002-3. Kim then explains that prior art BLPs, such as depicted in Kim's Figure 5 below, solved the problem of protruding outer leads (*id.*, ¶¶ 0004-5), but that—when this prior art BLP is mounted on a printed circuit board (20 in Figure 5 below) by forming a solder (25 in Figure 5 below) connection between the board and the bottom leads at the lower face of the package—"a strong joint cannot be obtained." *Id.*, ¶ 0006.

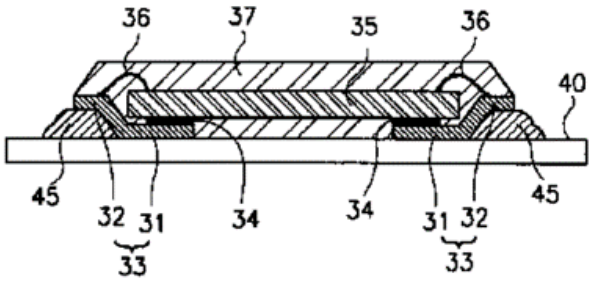
[FIG. 5]



Id., Fig. 5.

To improve the strength and reliability of the solder joint, Kim discloses a modified bottom-lead semiconductor package. *Id.*, ¶¶ 0007, 0020. This modified BLP is depicted in Kim's Figures 1 and 2, as well as Figure 3 (below).

[FIG. 3]



Id., Fig. 3; *see also* [Brief Description of the Drawings] ("[FIG. 3] This is a longitudinal cross-sectional view showing the situation in which one example of the bottom-lead semiconductor package of the present invention is mounted on a printed circuit board.").

Kim explains that the modified bottom-lead package offers an advantage over external lead designs, in that "the occupied area ratio of the package with respect to the board [is] reduced" and solder joint reliability is improved. *Id.*, ¶ 0006; *see also* ¶¶ 0019 ("[E]lectrical connection to this board is made by way of solder 45, which is injected into the grooves 38 respectively formed below each internal lead 32 in the package body."), 0020 ("[S]ince the board and the lower face of each internal lead are adhered

over a wide area by way of the solder, a good electrical join can be obtained. Further, since the solder is injected into the groove parts formed in the lower face of the package body, under each internal lead, electrical joining of the package and the board can be performed safely and reliably."); Ex. 1003, ¶¶ 127-30.

2. Adachi

Adachi, entitled "Three-dimensional circuit board and method of producing the same," published December 22, 1994. Ex. 1005. It is prior art under 35 U.S.C. §102(b).

Adachi is directed to "a three-dimensional circuit board used for mounting an element such as a light emitting diode." *Id.*, Abstract, ¶ 0001. Adachi further explains that its use of the term "three-dimensional circuit board" merely "denotes a broad concept including a chip component in which a circuit pattern is formed three-dimensionally, and a substrate for mounting the chip component." *Id.*, ¶ 0006; Ex. 1003, ¶ 132.

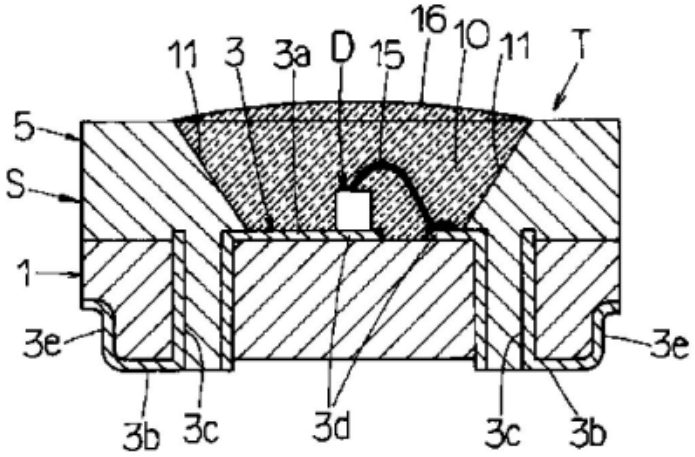
Adachi notes that conventional LED packages include a resin case with a recess. Ex. 1005, ¶¶ 0002-3. The walls of the recess and top of the case are plated with metals to form a "reflecting surface" for an LED mounted within the recess, and to form an electrode pattern for the device.

Id. Because the electrode pattern is exposed on this top surface, there is risk of damage. *Id.*, ¶ 0004.

To address this concern, Adachi discloses an LED device having a circuit pattern on the surface of a primary molding, and having a secondary molding that protects the circuit pattern. *Id.*, ¶¶ 0005-6; Ex. 1003, ¶¶ 133-36.

Adachi's Figure 10 (below) shows "a cross-sectional view of a chip-type light emitting electronic component manufactured by mounting an LED element on a three-dimensional circuit board of the present invention." Ex. 1005, [Brief Description of Drawings].

[FIG. 10]



Id., Fig. 10; *see also* ¶¶ 0024-25, 0030, Fig. 7 (showing through holes 8 lined with plating 3c for electrically connecting plated regions 3e and 3b to regions 3a and 3d); Ex. 1003, ¶ 137.

Adachi describes Figure 10 as follows:

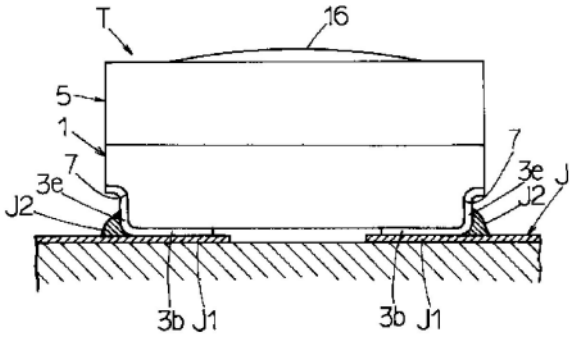
> In the three-dimensional circuit board S manufactured … as shown in FIG. 10, the body of the LED element D is fixed on one terminal part 3d of the circuit pattern 3, making an electrical connection at the same time, by way of silver paste, the other terminal part 3d is bonded with gold wire 15, and lastly the interior of the recess 10 is molded with a transparent epoxy resin 16 for the purpose of improving the light extraction efficiency and protecting the LED element D, so as to manufacture a chip-type light emitting electronic component T on which the LED element D is mounted.

Ex. 1005, ¶ 0040; *see also* ¶¶ 0032-33 ("[C]ircuit patterns 3 made of conductive material are formed on the top face side and the bottom face side of the primary molding 1 and on the inner surfaces of the through holes 8 …. Then … a secondary molding 5 made of a light-reflective secondary-side resin is unitedly laminated and molded, so as to provide an exposed part 4 [of primary molding 1] at the pair of terminal parts 3d, 3d in the circuit patterns 3, on the top face side of the primary molding 1 on which the circuit patterns 3 have been formed, such that the main portion of the circuit part 3a is covered and protected."), 0025 ("lead electrode part 3b for connection to another circuit board is formed on the bottom face side, and the circuit part 3a and the lead electrode part 3b are electrically connected by a connection

part 3c formed on the inner surfaces of the through holes 8"), Fig. 7; Ex. 1003, ¶¶ 138-43.

Adachi's Figure 11 (below) presents a side view of the chip-type light emitting electronic component T mounted to a mounting board J. Ex. 1005, ¶¶ 0040-41, [Brief Description of Drawings].

[FIG. 11]



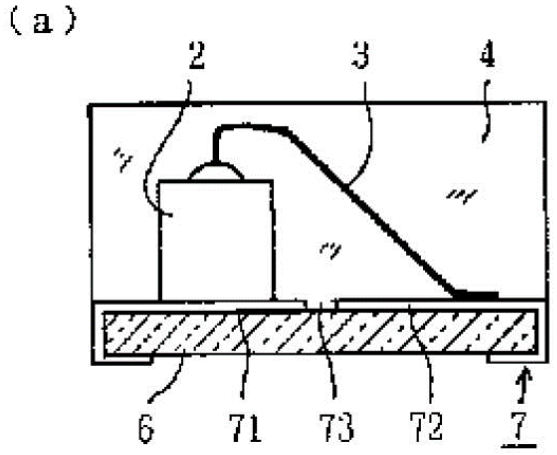
With respect to Figure 11, Adachi discloses that, "since the solder J2 is located in the cutaway portions 7, the bonding strength is high and the mounting density can be improved." *Id.*, ¶ 0041 Ex. 1003, ¶¶ 144-45.

3. Nagayama

Nagayama, entitled "Semiconductor package and method for manufacturing the same," published March 14, 2000. Ex. 1006. It is prior art under 35 U.S.C. §102(b).

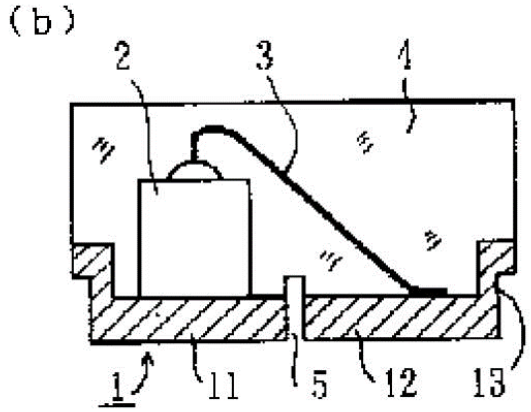
Nagayama is directed to "a semiconductor package structure in which a semiconductor is mounted and resin sealed on a board and a manufacturing method for the same." *Id.*, ¶ 0001; Ex. 1003, ¶¶ 147-49.

According to Nagayama, conventional LED semiconductor packages—such as depicted in Nagayama's Figure 2(a) below—have poor heat dissipation characteristics and high manufacturing cost because the "thermal conductivity of the insulating resin [6] constituting the circuit board is low" and because "an electrode pattern must be formed on the surface." Ex. 1006, ¶ 0007.



Id., Fig. 2(a).

To improve heat dissipation and reduce cost, (*id.*, ¶ 0008), Nagayama discloses semiconductor package embodiments—including a second embodiment depicted in Nagayama's Figure 1(b) (below)—having a semiconductor die, LED element 2, bonded to one portion of a metal board 11 with conductive adhesive and to another portion of the metal board 12 by a wire bond, and sealed in a sealing resin 4. *Id.*, ¶¶ 0009, 0016-18.



Id., Fig. 1(b).

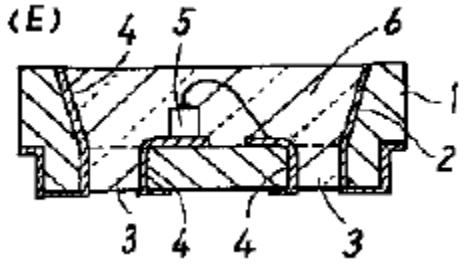
In Nagayama's second embodiment above, portions 13 are formed by pressing metal board 1 in a pre-processing step, which is followed by a surface treatment, *e.g.*, metal plating, to improve solderability. *Id.*, ¶ 0018. As a result, solder wetting at the sides of the metal board portions 11 and 12 is improved over that of a first embodiment, (*see*, *e.g.*, *id.*, Fig. 1(a)), that does not utilize a pressing step and that exposes only bare, untreated, cut metal surfaces at the sides of the metal board. *Id.*, ¶ 0018; Ex. 1003, ¶¶ 150-52.

4. Okazaki

Okazaki, entitled "Light emitting device and method for manufacturing the same," published March 29, 1994. Ex. 1007. It is prior art under 35 U.S.C. §102(b).

Okazaki "relates to light emitting devices … and particularly concerns chip type light emitting devices for surface mounting and a method for manufacturing the same." *Id.*, ¶ 0001; Ex. 1003, ¶ 154. While Okazaki is primarily directed toward cost reduction and solder wettability improvements over the prior art, (Ex. 1007, ¶ 0006), the disclosure most directly relevant to this petition relates to Okazaki's description of the prior art. Ex. 1003, ¶¶ 155-56.

For example, Okazaki's Figure 5(E), below, depicts a prior art surface mount package in which a wiring pattern 4 is plated on an insulating block body 1 having through holes 3, and a light emitting element (LED) 5 is mounted on the three-dimensional wiring pattern. Ex. 1007, ¶ 0002.



Id., Fig. 5(E).

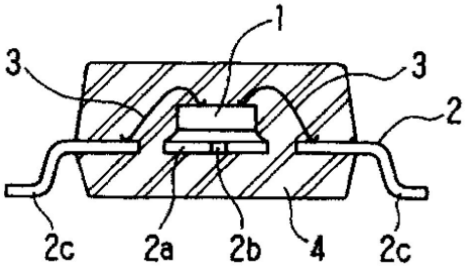
5. Shirahata

Shirahata, entitled "Resin-molded type light-receiving semiconductor device," published May 31, 1995. Ex. 1019. It is prior art under 35 U.S.C. §102(b).

Shirahata is directed to "a resin-molded type light-receiving semiconductor device such as a photodiode, or a phototransistor," and further explains that, "resin-molded type semiconductor devices, in which a light receiving semiconductor chip and a lead frame are sealed with a transparent resin by methods such as transfer molding or casting molding, have often recently been used with the aim of reducing costs." *Id.*, 4 [Field of industrial application], [Prior art]; Ex. 1003, ¶¶ 158-59.

Shirahata further states that "the structure of a conventional resin-molded type light-receiving semiconductor device [is shown] in FIG. 4 [below]." Ex. 1019, 4 [Prior Art].

[FIG. 4]



Id., Fig. 4; *see also* 5 [Brief Description of Drawings]; Ex. 1003, ¶ 160.

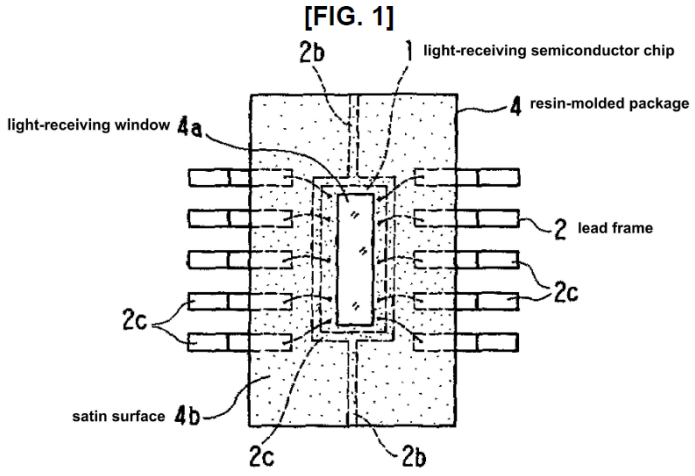
Shirahata describes Figure 4 as follows:

> [I]n the drawing: 1 is a light-receiving semiconductor chip; 2 is a lead frame, in which a die pad 2a, on which the chip 1 is mounted, a support pin 2b, lead fingers 2c, and the like are formed by punching; 3 are bonding wires connected between the chip 1 and the lead fingers 2c; and 4 is a resin-molded

> package of transparent resin, wherein the resin-molded package 4 is molded by casting a transparent resin with the chip 1 and the lead frame 2 set in a cavity of a molding die.

Ex. 1019, 4-5 [Prior Art].

While Shirahata's Figure 4 depicts a cross-section in which only two terminal lead fingers 2c, one on either side, are visible, Shirahata further discloses that, "in FIG. 1 and FIG. 2, [] the basic structure of the light-receiving semiconductor device is identical to that in FIG. 4," (*id.*, 5 [Examples]) and a POSA would understand the plan view of Shirahata's Figure 1 (below) as confirming that a plan view of the conventional light-receiving device in Fig. 4 would similarly show multiple terminal lead fingers 2c, wire bonded to the light-receiving semiconductor chip 1, and extending from opposite sides of the package. Ex. 1003, ¶¶ 161-62. Such configurations were also conventional, *e.g.*, to interface with light-receiving semiconductor chips having multiple light receiving elements or pixels. *Id.*



Ex. 1019, Fig. 1.

Shirahata also discloses a modification to the conventional light-receiving semiconductor device depicted in Shirahata's Figure 4 above. The modification is intended to enhance durability and to "prevent stray light from the surroundings from being incident on the light-receiving semiconductor chip." *Id.*, 5 [Problems to be solved by the invention]; Ex. 1003, ¶ 163.

B. Ground 1: Kim Anticipates Claims 1-3 and 11

1. Claim 1

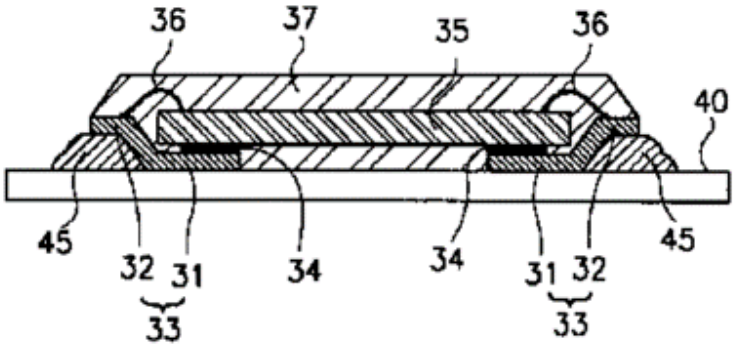
1[preamble] "A surface mountable electronic device, comprising:"

If the preamble is limiting, it is disclosed by Kim. Ex. 1003, ¶¶ 168-74.

Kim discloses a bottom-lead semiconductor package (BLP) housing a semiconductor chip 35 adhered to bottom leads 31 and wire bonded to inner leads 32 that are soldered to a printed circuit board, (Ex. 1004, ¶¶ 0018-19), so as to reliably mount the BLP to a planar printed circuit board 40. *Id.*, Fig. 3, ¶ 0007 ("[T]he present invention is directed to providing a bottom-lead semiconductor package … in which, in mounting the bottom-lead semiconductor package on a board such as a printed circuit board, a strong solder joint is made…."). Ex. 1003, ¶¶ 168-170.

Kim's bottom-lead semiconductor package—which is a "surface mountable electronic device"—is shown in cross-sectional view, surface-mounted to a printed circuit board 40 via solder 45 in Kim's Figure 3 (below). Ex. 1003, ¶¶ 171-74.

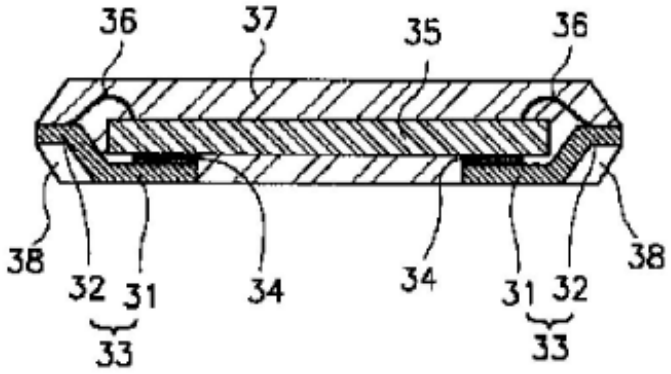
[FIG. 3]



Ex. 1004, Fig. 3; *see also* [Brief Description of the Drawings] ("[FIG. 3] is a longitudinal cross-sectional view showing the situation in which one example of the bottom-lead semiconductor package of the present invention is mounted on a printed circuit board.").

Kim further discloses that, when the BLP "is mounted on a printed circuit board" 40, the "lower faces of the bottom lead groups 31 are directly adhered to the upper face of the printed circuit board 40, and electrical connection to this board is made by way of solder 45, which is injected into the grooves 38 [shown in Kim's Figure 1] respectively formed below each internal lead 32 in the package body." *Id.*, ¶ 0019; Ex. 1003, ¶ 173.

[FIG. 1]



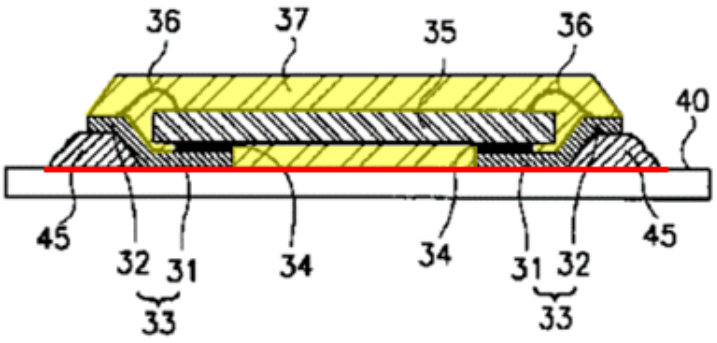
Ex. 1004, Fig. 1.

1[a] "a packaged body having a mounting surface"

Kim discloses that its bottom-lead semiconductor package includes "a packaged body," *i.e.*, molded resin package body 37 (Ex. 1004, Figs. 1-3) (yellow in Kim's Figure 3, below), having "a mounting surface" (shown by the red line in Figure 3 at the bottom of lead portions 31 and molded resin 37). *Id.*, ¶¶ 0008 (The BLP comprising "a semiconductor chip 35 adhered to the upper faces of the bottom lead groups by way of an insulating adhesive 34; conductive wires 36 that respectively electrically connect the semiconductor chip to each internal lead; and a molding part 37 molded so as to seal the bottom lead frame, the semiconductor chip, and the conductive wire groups"), 0015 ("[A] package body (in which the space occupied by resin or the like is a molding part 37) is made in a predetermined shape, by sealing the basic constituent unit with an epoxy resin or the like. Here, the

lower faces of the lead groups are exposed to the exterior of the package body."), 0018 ("[A] molding-forming substance such as epoxy resin is injected into the mold and cured to form a package body having a molding part 37 … so that each lower face in the lead groups is ultimately exposed to the exterior."); Ex. 1003, ¶¶ 175-78.

[FIG. 3]



Ex. 1004, Fig. 3; *see also* ¶ 0019 (A BLP "according to the present invention is mounted on a printed circuit board. The lower faces of the bottom lead groups 31 are directly adhered to the upper face of the printed circuit board 40, and electrical connection to this board is made by way of solder 45, which is injected into the grooves 38 [shown in Kim's Figure 1] respectively formed below each internal lead 32 in the package body.").

1[b] "the mounting surface having a plurality of recesses at side edges of the body"

Kim discloses that the "mounting surface" of its bottom-lead semiconductor package body has "a plurality of recesses" (*i.e.*, the

depressions or indentations in molded resin package body 37, occupied by "internal leads 32, which first extend obliquely upward … then extend horizontally," (Ex. 1004, ¶ 0008, Fig. 1), and also occupied by the grooves 38 under the internal leads[5]) at "side edges of [that] body":

> [The] package body (… molding part 37) is made in a predetermined shape…. [T]he lower faces of the lead groups are exposed to the exterior of the package body. A specific mode of exposure is represented by a groove part indicated by reference numeral 38, wherein this groove part is constituted by a bottom plane, which is the bottom plane of the internal leads 32, and faces (two faces) perpendicular to the bottom plane, which extend as far [as] the line of intersection with a plane of the internal lead projected to a virtual plane including the bottom plane of the bottom lead 31 that corresponds to the internal lead. Thus, adjacent leads are electrically isolated by wall-like molding parts that separate each groove part [38].

Id., ¶ 0015; Ex. 1003, ¶¶ 179-80, 182-83.

---

[5] If the "recesses" are the depressions or indentations ***in the device as a whole***, then, in Kim, the "recesses" would define "grooves 38" below the internal leads 32. Ex. 1003, ¶ 184.

Kim further explains that the wall-like molded resin that separates the groove parts 38 under the internal leads 32 (Ex. 1004, Figs. 1, 3) at the side edges of the molded resin body 37 is formed using:

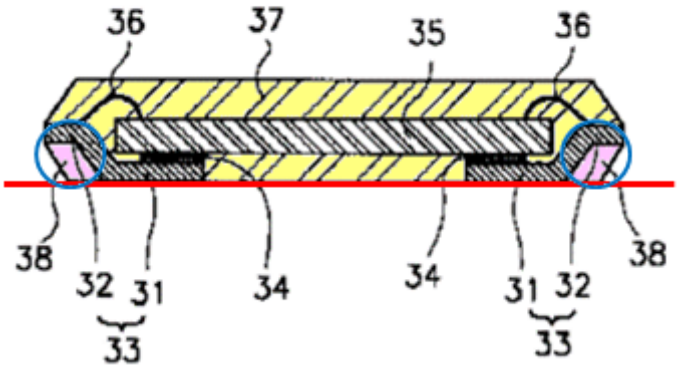
> [A] male mold having a shape corresponding to the shapes of the groove parts 38, which are formed below each of the internal leads 32, the width thereof being the width of the internal lead, the length thereof being the length of the internal lead projected in the same plane as the lower face of the bottom lead group 31 of the internal lead, and the bottom plane thereof being the same plane as the lower face of the bottom lead group (here, the expression, male mold having a shape corresponding to the shapes of the groove parts 38, refers to a male mold having a shape capable of filling the groove parts, which is to say, the voids). As a result of this, when the molding is completed, a package body will be obtained in which voids, which is to say groove parts 38, are formed beneath each of the lead groups 33 in the package body.

Id., ¶ 0018; Ex. 1003, ¶ 181.

Kim's groove parts 38 under each internal lead 32 at the side edges of the package body are pink in Kim's Figures 1 and 2 (below); the mounting surface is indicated by red annotation; the molded resin packaged body 37,

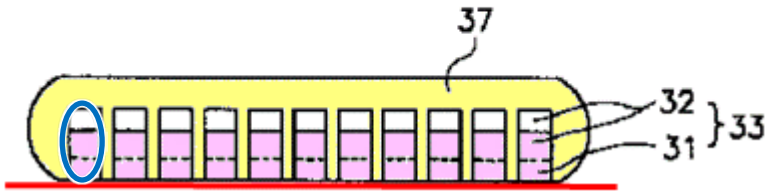
including wall-like portions separating the groove parts, is yellow; and the areas defined by the recesses are circled in blue.[6] Ex. 1003, ¶ 184.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view).

[FIG. 2]



Id., Fig. 2 (side view, annotated with one circled "recess").

[6] If the "recesses" are the depressions or indentations ***in the device as a whole***, then, in Kim, the "recesses" would define the groove parts 38 (pink). Ex. 1003, ¶ 184.

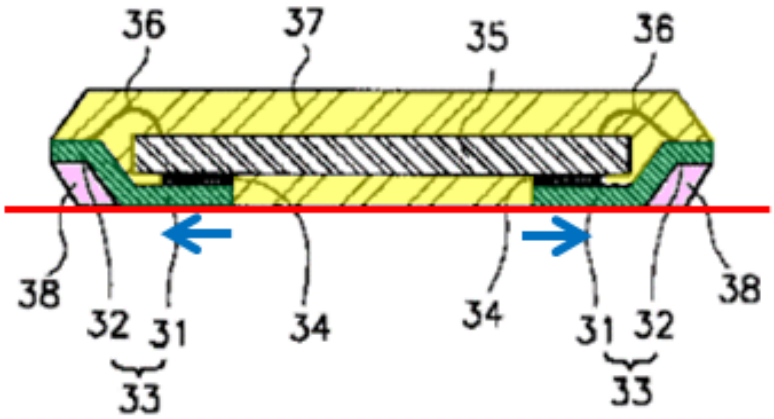
1[c] "a plurality of electrical contacts, each of which extends from an interior portion of the mounting surface and terminates in one of said recesses, and each of which conforms to one of said recesses"

Kim discloses that its BLP package has leads 33 consisting of a bottom lead part 31 and internal lead part 32. Ex. 1004, ¶ 0015. These leads 33 are electrically connected to electrode pads on the semiconductor chip 35 by bonding wires 36, (*id.*), and are electrically connected to a printed circuit board during mounting using solder in grooves 38, (*id.*, ¶¶ 0016, 0019 ("lead groups 31 are directly adhered to the upper face of the printed circuit board 40, and electrical connection to this board is made by way of solder 45")). Thus, Kim's leads 33 disclose and constitute the claimed "plurality of electrical contacts." *Id.*, Figs. 1-2; Ex. 1003, ¶¶ 185-87.

As shown in Kim's Figures 1 and 2 below, each of Kim's "electrical contacts," *i.e.*, leads 33 (green), "extends from an interior portion of the mounting surface" (the "extending" indicated with blue arrows below) and "terminates in one of said recesses" (*i.e.*, the depressions or indentations in the yellow package body, which depressions or indentations are also occupied by grooves 38, pink), and each of which "conforms to" one of said

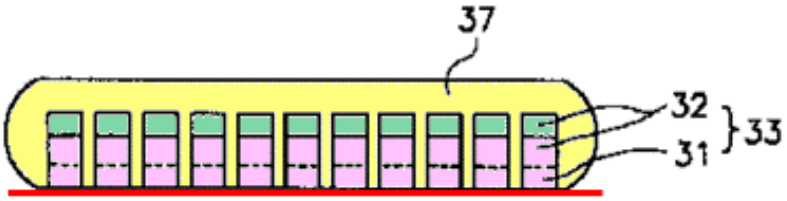
recesses" (*i.e.*, the leads are adapted to, and follow, the depressions or indentations in the yellow packaged body).[7] Ex. 1003, ¶¶ 188-89.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view).

[FIG. 2]



Id., Fig. 2 (side view).

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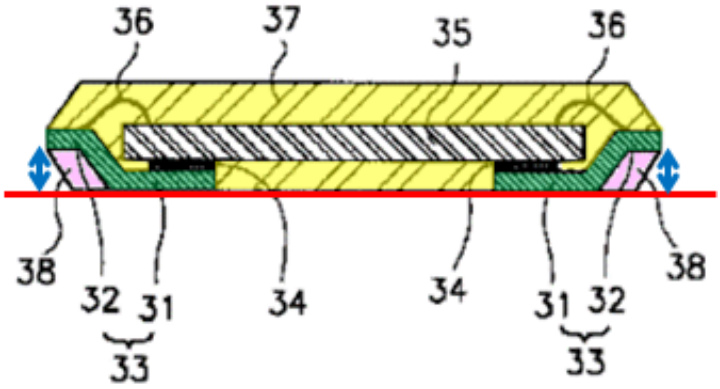
[7] If the "recesses" are the depressions or indentations in the ***device as a whole*** (including the contacts, *i.e.*, internal leads 32), the leads conform to the "recesses," at least under Patent Owner's proposed construction of "conforms to" as "gives the same shape, outline, or contour to." Ex. 1011, 5; Ex. 1010, 2; Ex. 1003, ¶ 189.

1[d] "wherein said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts"

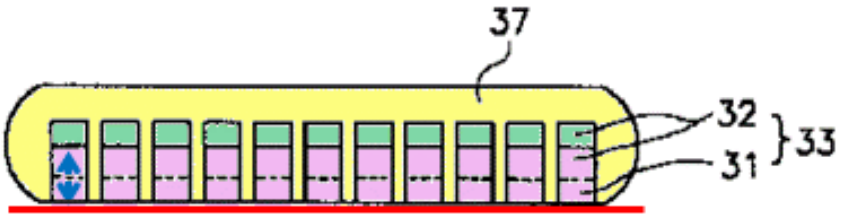
As shown in Kim's Figures 1 and 2, below, Kim discloses that "said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts." Ex. 1003, ¶ 190.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view).

[FIG. 2]



Id., Fig. 2 (side view, annotated to highlight one "offset").

As shown by the blue bidirectional arrows above, the offsets (the pink spaces) are the result of the sizing of the recesses and the electrical contacts.[8] Ex. 1003, ¶ 191.

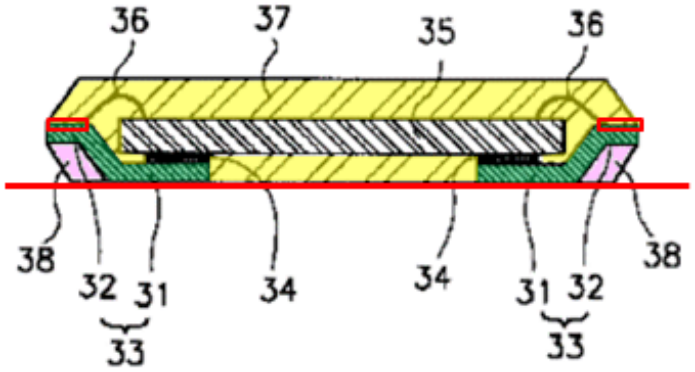
2. Claim 2

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is substantially parallel to said mounting surface."

As shown in Kim's Figures 1 and 2 below, Kim discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is substantially parallel to said mounting surface [red line]." Ex. 1003, ¶ 192.

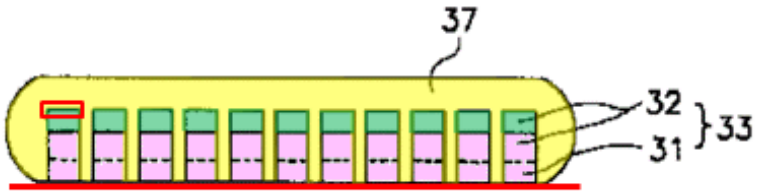
[8] This is true (i) whether the recesses are the depressions or indentations in the yellow packaged body, which include therein the contacts colored green, in which case the offsets are the spaces colored pink; or (ii) whether the recesses are the depressions or indentations in the ***device as a whole***, in which case the offsets would be those same pink spaces (or the vertical components thereof). Ex. 1003, ¶ 191.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view); *see also* ¶ 0018 ("internal leads 32 … extend[] in the outward horizontal direction").

[FIG. 2]



Id., Fig. 2 (side view, annotated to highlight one "recess").[9]

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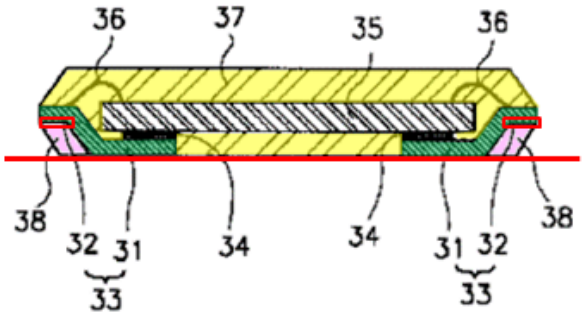
[9] Or, if the recesses are the depressions or indentations in the ***device as a whole***:

[FIG. 1]

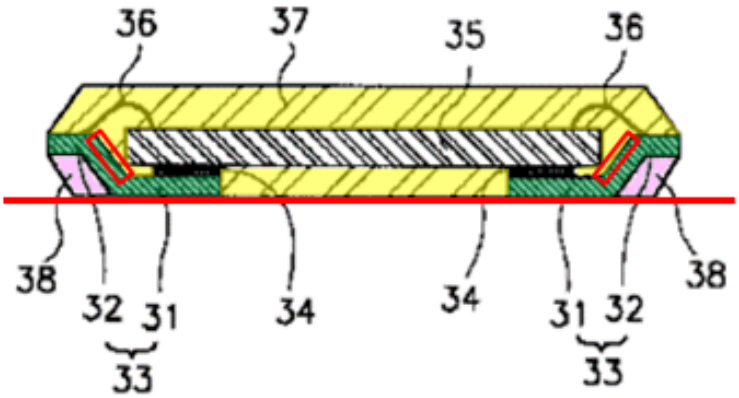


3. Claim 3

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is not parallel to said mounting surface."

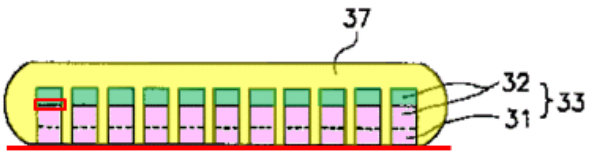
As shown in Kim's Figures 1 and 2 below, Kim discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is not parallel to said mounting surface [red line]." Ex. 1003, ¶ 193.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view).

[FIG. 2]



Id., Fig. 2 (side view, annotation highlights one "recess"); Ex. 1003, ¶ 192.

Ex. 1004, Fig. 1 (longitudinal cross-sectional view); *see also* ¶ 0018 ("internal leads 32 … extend[] obliquely upward").[10]

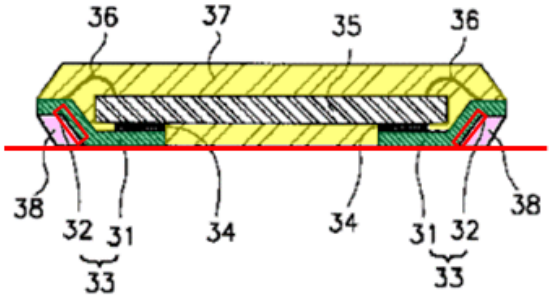
4. Claim 11

"The device of claim 1, wherein one or more of the recesses is bounded on three sides."

Kim's Figures 1 and 2 (below) have been annotated with red arrows, numbered consistently to indicate surfaces that are the same in each figure, to show that Kim's bottom-lead semiconductor package provides recesses having boundaries on three sides. Four sides are identified, any three of which meet this limitation. Ex. 1003, ¶¶ 194-99.

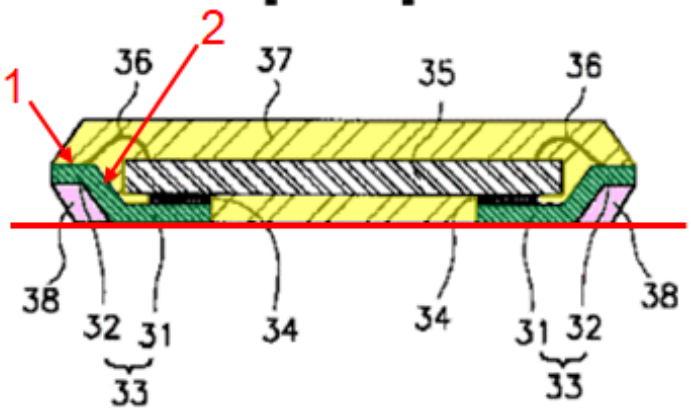
[10] Or, if the recesses are the depressions or indentations in the ***device as a whole***:

[FIG. 1]



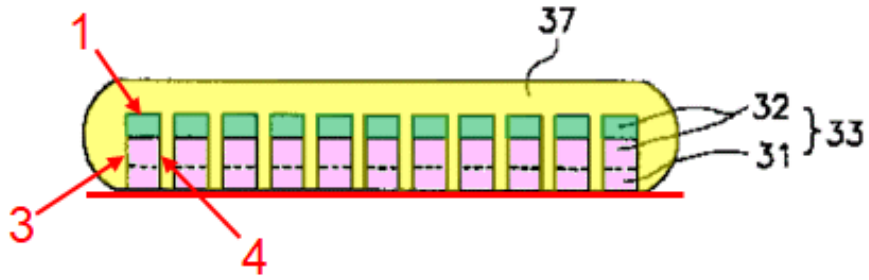
Ex. 1004, Fig. 1 (longitudinal cross-sectional view); Ex. 1003, ¶ 193.

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view, annotation shows the boundaries on one "recess").

[FIG. 2]

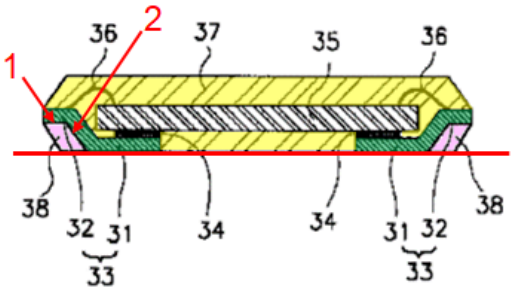


Id., Fig. 2 (side view, annotation shows the boundaries on one "recess");[11] *see also* ¶¶ 0015 ("Thus, adjacent leads are electrically isolated by wall-like

[11] Or, if the recesses are the depressions or indentations in the ***device as a whole***:

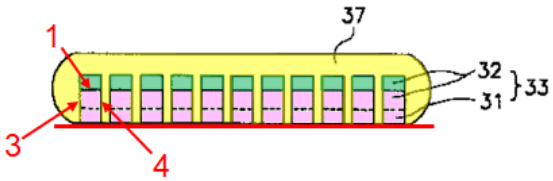
molding parts that separate each groove part."), 0009 ("[A] groove part 38 is formed below each of the internal leads 32, the width thereof being the width of the internal lead … and the bottom plane thereof being the same plane as the lower face of the bottom lead group. This is because, in mounting the package on a board, short circuits due to contact with solder can be easily avoided and electrical contact with the board can be reliably performed."), 0019 ("solder 45, which is injected into the grooves 38 respectively"), 0020 ("since the solder is injected into the groove parts").

[FIG. 1]



Ex. 1004, Fig. 1 (longitudinal cross-sectional view, annotation shows the boundaries on one "recess").

[FIG. 2]



Id., Fig. 2 (side view, annotation shows the boundaries on one "recess"); Ex. 1003, ¶ 199.

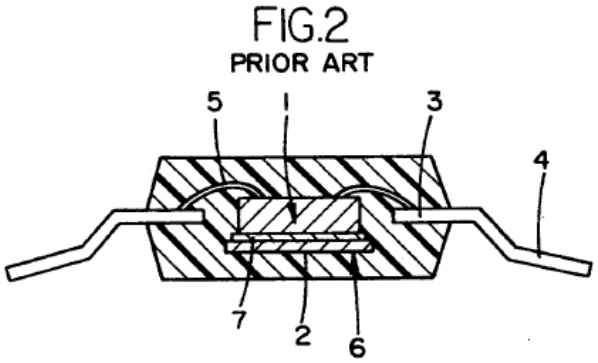
C. Ground 2: Kim in View of Shirahata Renders Claim 8 Obvious

1. Claim 8

"The device of claim 1, wherein the device is selected from a group comprising an opto-electric device and a light-emitting device."

As discussed in Section V.A.1, above, Kim explains that its BLP surface mountable electronic device was designed to be an improvement over pre-existing small outline packages (SOP), and small outline J-lead (SOJ) semiconductor chip packages, that suffer from the disadvantage of having exposed external leads that increase the area occupied by the package. Ex. 1004, ¶¶ 0002-3.

The SOP package referenced by Kim is illustrated below in cross-section:

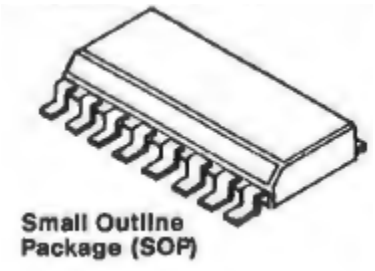


U.S. 5,428,248 (Ex. 1020) (cited at Ex. 1004, ¶ 0004); *see also* Ex. 1020, 2:9-13 ("[K]nown semiconductor packages are generally classified into a

small outline J-lead package such as shown in FIG. 1, a small outline package (SOP) package such as shown in FIG. 2 and a dual inline package (not shown).").

Though not shown in the above cross-sectional view, the conventional SOP package has multiple leads extending from the sides of the package. *See* Ex. 1020, Fig. 3, 1:35-2:13; Ex. 1003, ¶¶ 202-206.

An exemplary perspective view of an SOP is shown below:



Ex. 1021, 14.

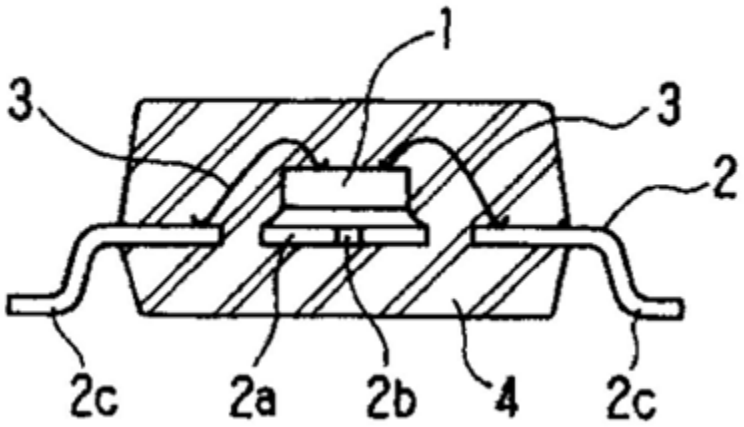
Kim explains that its modified bottom-lead package offers an advantage over external-lead SOP designs, in that "the occupied area ratio of the package with respect to the board [is] reduced" and solder joint reliability is improved. Ex. 1004, ¶¶ 0005-6; *see also* ¶¶ 0019 ("[E]lectrical connection to this board is made by way of solder 45, which is injected into the grooves 38 respectively formed below each internal lead 32 in the package body."), 0020 ("[S]ince the board and the lower face of each internal lead are adhered over a wide area by way of the solder, a good

electrical join can be obtained. Further, since the solder is injected into the groove parts formed in the lower face of the package body, under each internal lead, electrical joining of the package and the board can be performed safely and reliably.").

Kim does not expressly disclose placing an opto-electronic circuit, *e.g.*, a photoelectric conversion device, in its BLP package. However, Kim does not place any restrictions on the type of semiconductor chip 35 that is contained in its package. In view of Kim's broad and non-limiting disclosure, a POSA would understand Kim's BLP as being generally compatible with any chip that might otherwise be contained in an SOP-like package. Ex. 1003, ¶¶ 207-209.

As noted in Section V.A.5, above, and shown in cross-section in Figure 4 (below), Shirahata discloses a conventional prior art light-receiving semiconductor device package with rows of terminal lead fingers extending from the sides of a transparent resin body 4, which body houses a light-receiving semiconductor chip 1 containing, *e.g.*, photodiodes or phototransistors. Ex. 1019, 4 [Field of industrial application], 4-5 [Prior art], Figs. 1, 4; Ex. 1003, ¶ 210.

[FIG. 4]



Ex. 1019, Fig. 4; *see also* Fig. 1.

Shirahata's conventional photoelectric conversion device, as can be seen by comparison with the Figures above (Ex. 1020, Fig. 2; Ex. 1021, 14), is an example of an SOP. Ex. 1003, ¶ 211.

It would have been obvious to construct Kim's BLP package, a package intended as an improvement over SOPs, with light-receiving semiconductor chip as "semiconductor chip 35," and to select a transparent resin, as taught by Shirahata, for constructing Kim's molding part 37. Ex. 1003, ¶¶ 212-13. This modified device meets the limitations of claim 8, *i.e.*, it is an optoelectronic device and meets the limitations of claim 1. Ex. 1003, ¶ 213.

A POSA would have understood that this combination would yield the benefits taught by Kim, *i.e.*, (1) reduced package size, thereby allowing for

device miniaturization, a well-established design objective prior to the '040 patent; (2) reduced potential for damage to the exposed terminal leads at the sides of Shirahata's conventional SOP light receiver, (Ex. 1004, ¶ 0006 (noting that the BLP design discussed in Kim avoids damage that can be caused in prior art packages having exposed leads); Ex. 1020, 2:31-35 ("Another problem of the known semiconductor packages is that the outer leads are apt to be undesirably bent when the packages are mounted on the printed circuit board or transported, thereby causing quality inferiority.")); and (3) improved solder joint strength when surface mounting the device, another well-established design objective prior to the '040 patent. Ex. 1003, ¶ 214.

And, POSAs had already expressly recognized that these motivations were applicable to photoelectric conversion devices, such as described in Shirahata. For instance, Kuwabata discloses that SOP packages (Ex. 1022, Fig. 4, ¶ 0008, [Brief Description of Drawings]) can be modified to eliminate external leads, thereby reducing the occupied area of the package and preventing damage (*id.*, Fig. 8, ¶¶ 0019, 0039-40), and that this modified design can be advantageously used to house, *e.g.*, solid-state imaging semiconductor chips (*id.*, ¶¶ 0015, 0036). Similarly, Makimoto discloses that conventional external-lead light receiving semiconductor chip packages

are not suitable for high-density mounting (Ex. 1023, ¶¶ 0002, 0005, Fig. 8), and can be improved by adopting internal lead designs (*id.*, ¶¶ 0019, 0027, Fig. 1). Ex. 1003, ¶¶ 215-18.

Further, the above modifications to Kim would have required no undue experimentation; indeed, Kim discloses that its molding part 37 can be constructed of "epoxy resin or the like," (Ex. 1004, ¶ 0015). Ex. 1003, ¶ 219. And, light-transparent resin compounds were commonly used to form such molded-body parts. Ex. 1003, ¶ 219; Ex. 1019, 4 [Prior Art]; Ex. 1006, ¶¶ 0004, 0017; Ex. 1001, 2:4-8, Fig. 2.

D. Ground 3: Adachi Anticipates Claims 1-4 and 8

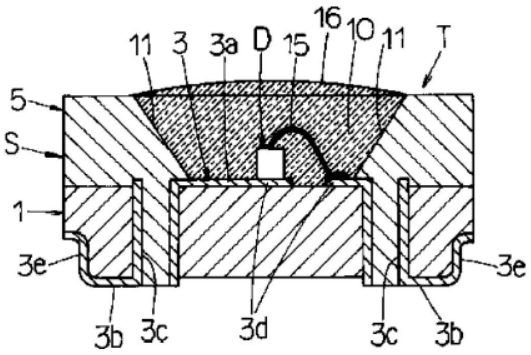
1. Claim 1

1[preamble] "A surface mountable electronic device, comprising:"

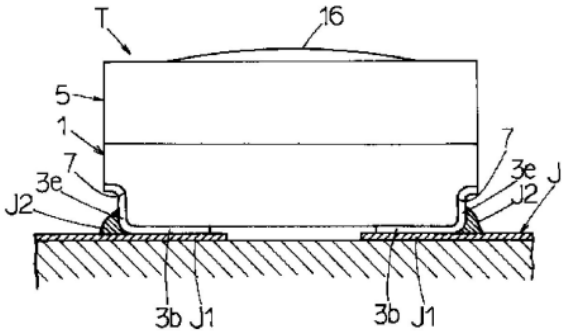
If the preamble is limiting, it is disclosed by Adachi. Ex. 1003, ¶¶ 221-25.

Adachi discloses a "chip-type light emitting electronic component T" (*i.e.*, an electronic device), depicted in cross-sectional view in Adachi's Figure 10, and in side view mounted to the surface of a mounting board J in Adachi's Figure 11 (both below). Ex. 1005, ¶ 0040, [Brief Description of Drawings].

[FIG. 10]



[FIG. 11]



Id., Figs. 10-11.

In particular, Adachi discloses that "the chip-type light emitting electronic component T is mounted by placing the lead electrode parts 3b on electrode parts J1 of another mounting board J and molding molten solder J2 at the connection terminal parts 3e." *Id.*, ¶ 0041; *see also* ¶ 0014 ("[T]he electrode parts of the circuit pattern exposed on the bottom face and the lateral faces of the primary molding can be soldered, when an electronic component manufactured by [the methods taught herein] is installed on a mounting board."). Ex. 1003, ¶ 224.

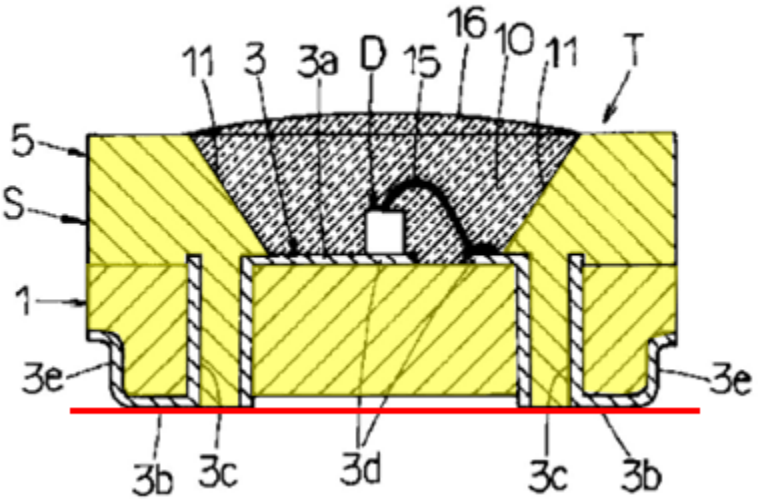
1[a] "a packaged body having a mounting surface"

Adachi discloses that the "chip-type light emitting electronic component T" depicted in Adachi's Figures 10 and 11, *i.e.*, the surface mountable electronic component, has "a packaged body having a mounting surface." Ex. 1003, ¶¶ 226-30.

The packaged body of Adachi's component T includes primary molded resin body 1 and secondary molded resin body 5. Ex. 1005, ¶¶ 0022 ("primary molding 1 is molded into a desired shape, with an ordinary injection molding method, using a primary-side resin"), 0033 ("the secondary-side resin is injection molded in a space formed by the mold and the primary molding 1, so as to form the secondary molding 5 united with the primary molding 1"), 0011 ("[I]t is necessary that the secondary-side resin is of the same type as the primary-side resin, or [that a] combination is selected with which insert molding the primary molding is possible."); Ex. 1003, ¶ 226. The secondary molded resin body 5 is integrally formed by insert molding of the primary molded resin body 1 (Ex. 1005, ¶¶ 0009, 0016, 0021), the two moldings preferably being made of the same resin to promote adhesion (*id.*, ¶¶ 0011, 0018), and both molded resin bodies collectively function as the protective shell (*id.*, ¶¶ 0034, 0040, 0044). Ex. 1003, ¶ 227.

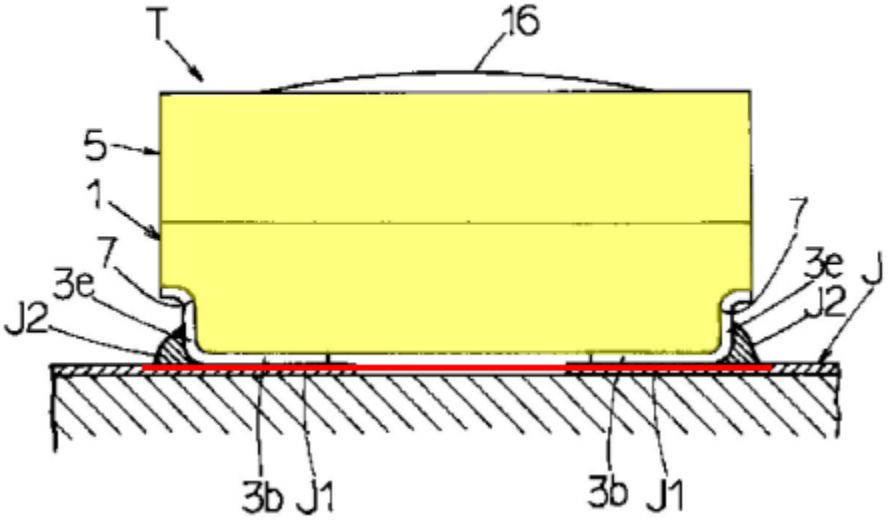
The packaged body is yellow, and its mounting surface, which is essentially co-planar with the planar bottom of lead electrode parts 3b, secondary molding 5, and primary molding 1, is identified in red in Adachi's Figures 10 and 11 below. *Id.*, ¶ 229.

[FIG. 10]



Ex. 1005, Fig. 10 (cross-sectional view).

[FIG. 11]



Id., Fig. 11 (front-side view).

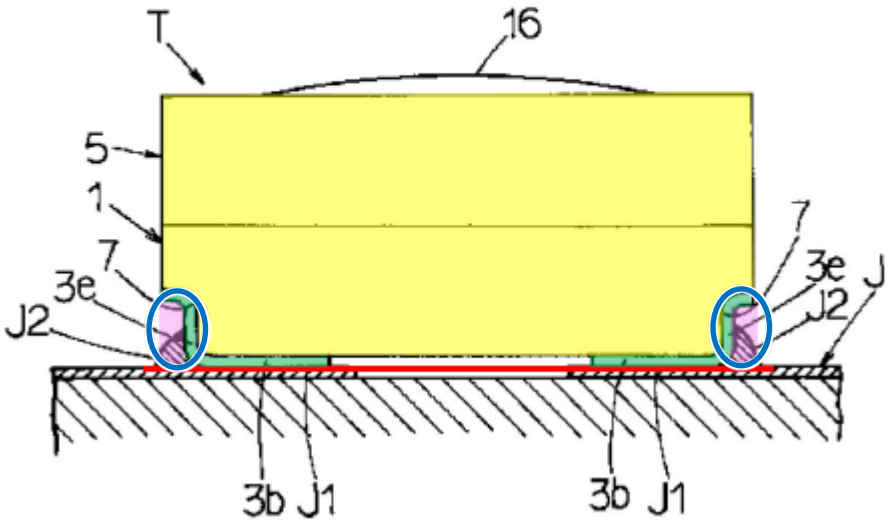
1[b] "the mounting surface having a plurality of recesses at side edges of the body"

Adachi discloses that the mounting surface of the packaged body of LED device T has "a plurality of recesses at side edges of the body." Ex. 1003, ¶¶ 231-33.

These recesses—the areas defined thereby circled in blue—are depressions or indentations in the yellow packaged body in Adachi's Figure 11 (Ex. 1005, ¶ 0041 ("cutaway portions 7")), occupied by the "terminal parts 3e" (*id.*) (green), as well as the spaces beneath (pink):[12]

[12] If the claimed "recesses" are the depressions or indentations in the ***device as a whole***, then in Adachi, the "recesses" would define just the pink-shaded regions. Ex. 1003, ¶ 233.

[FIG. 11]



Id., Fig. 11; Ex. 1003, ¶¶ 231-33.

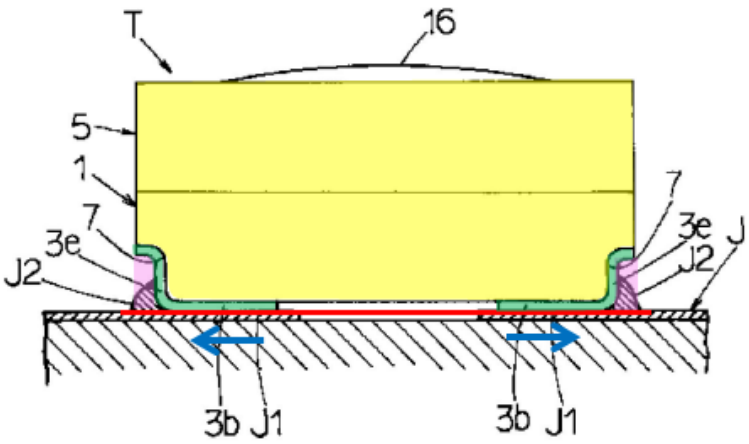
1[c] "a plurality of electrical contacts, each of which extends from an interior portion of the mounting surface and terminates in one of said recesses, and each of which conforms to one of said recesses"

Adachi discloses that the surface mountable electronic device T depicted in Adachi's Figures 10 and 11 includes "a plurality of electrical contacts." Ex. 1003, ¶¶ 234-36.

The plurality of electrical contacts disclosed by Adachi are comprised of "lead electrode parts 3b [and] connection terminal parts 3e," *i.e.*, the metal plating on the underside of the primary molding 1, (Ex. 1005, ¶ 0041), and are identified by green annotation in Adachi's Figure 11 below. The

figure includes a yellow packaged body and the mounting surface in red. Ex. 1003, ¶¶ 234-35.

[FIG. 11]



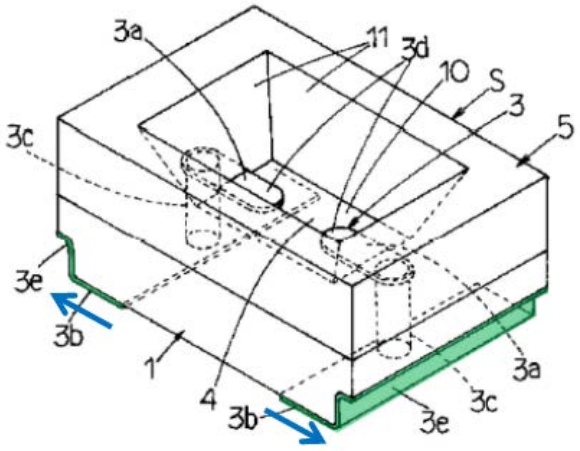
Ex. 1005, Fig. 11; *see also* ¶ 0025 ("[E]nd portions of the lead electrode part 3b reach the undercut parts 7, and portions corresponding these undercut parts 7 constitute connection terminal parts 3e.").

As can be seen in Figure 11, above, each of the "electrical contacts" (green) "extends from an interior portion of the mounting surface" ("extending" shown with blue arrows) and "terminates in one of said recesses" (*i.e.*, the depressions or indentations in the yellow package body) and "each of which conforms to one of said recesses" (*i.e.*, the leads are adapted to, and follow, the depressions or indentations in the yellow

packaged body). Ex. 1003, ¶ 237.[13]

By way of further illustration, Adachi's Figure 7 (below with the recited electrical contacts shaded green) shows a perspective view of the device before the LED chip has been mounted ("extending" shown with blue arrows). Ex. 1005, ¶ 0036; Ex. 1003, ¶ 238.

[FIG. 7]



Ex. 1005, Fig. 7; *see also* ¶ 0030 (explaining that a first method for manufacturing the surface mountable electronic LED device of Figure 11 is illustrated in Adachi's Figures 4-7).

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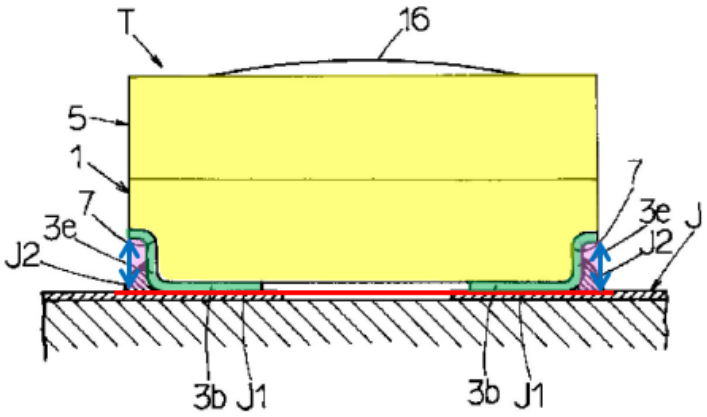
[13] If the claimed "recesses" are the depressions or indentations in the ***device as a whole***, the leads conform to the "recesses," at least under Patent Owner's proposed construction of "conforms to" as "gives the same shape, outline, or contour to." Ex. 1011, 5; Ex. 1010, 2; Ex. 1003, ¶ 237.

1[d] "wherein said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts"

Adachi's Figure 11, below, discloses "recesses" (depressions or indentations in the yellow packaged body) and "electrical contacts" (green) that "are sized to provide offsets [indicated by blue arrows] between said mounting surface [red line] and said electrical contacts." Ex. 1003, ¶¶ 239-40.

[FIG. 11]



Ex. 1005, Fig. 11.

As shown by the blue bidirectional arrows above, the offsets (the pink spaces) are the result of the sizing of the recesses and the electrical contacts.[14] Ex. 1003, ¶ 240.

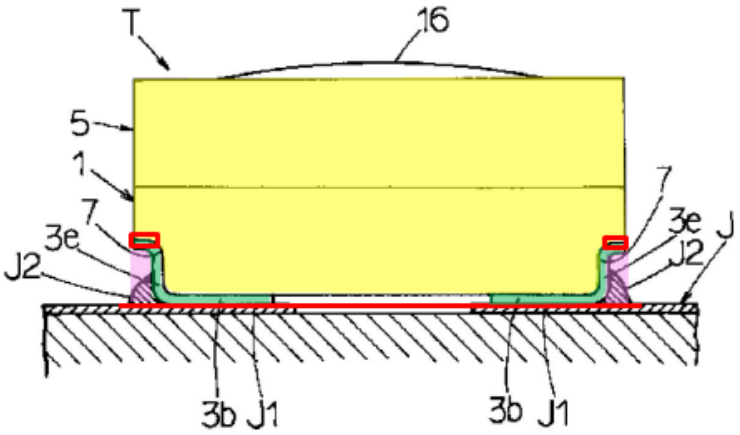
[14] This is true (i) whether the recesses are the depressions or indentations in the yellow packaged body, which include therein the contacts colored green,

2. Claim 2

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is substantially parallel to said mounting surface."

Adachi's Figure 11 surface mountable LED device, below, discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is substantially parallel to said mounting surface [red line]." Ex. 1003, ¶ 241.

[FIG. 11]



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in which case the offsets are the spaces colored pink; or (ii) whether the recesses are the depressions or indentations in the ***device as a whole***, in which case the offsets would be those same pink spaces (or the vertical components thereof). Ex. 1003, ¶ 240.

Ex. 1005, Fig. 11.[15]

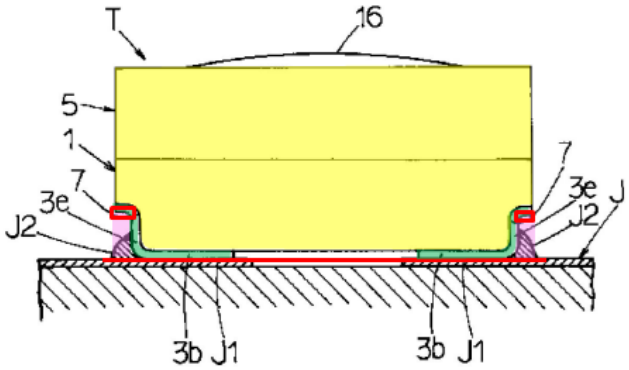
3. Claim 3

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is not parallel to said mounting surface."

Adachi's Figure 11 surface mountable LED device, below, discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is not parallel to said mounting surface [red line]." Ex. 1003, ¶ 242.

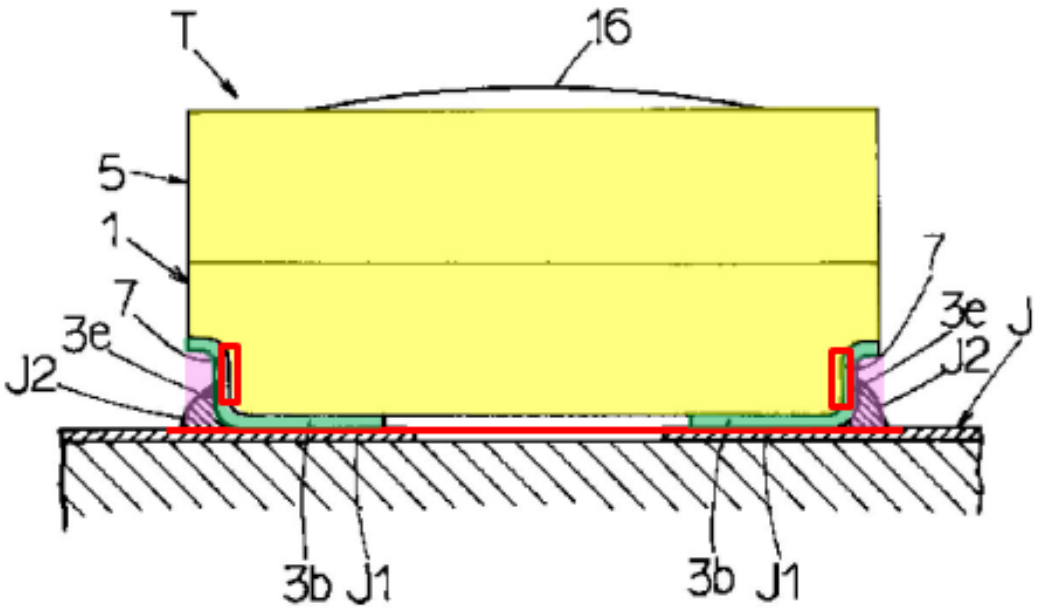
[15] Or, if the recesses are depressions or indentations in the ***device as a whole***:

[FIG. 11]



Ex. 1005, Fig. 11; Ex. 1003, ¶ 241.

[FIG. 11]



Ex. 1005, Fig. 11.[16]

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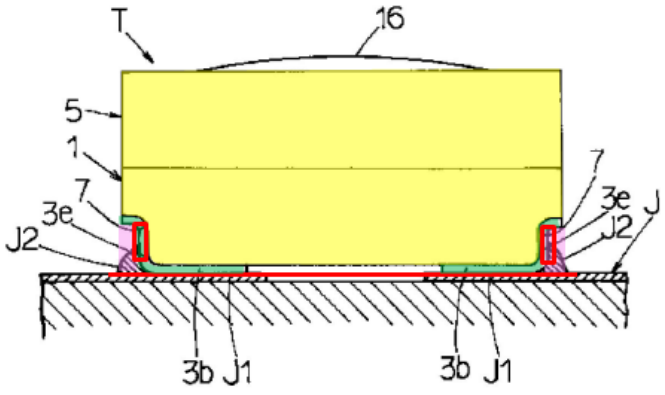
[16] Or, if the recesses are depressions or indentations in the ***device as a whole***:

[FIG. 11]



Ex. 1005, Fig. 11; Ex. 1003, ¶ 242.

4. Claim 4

"The device of claim 3, wherein said portions of the recesses that are not parallel to said mounting surface are orthogonal to said mounting surface."

The disclosure in Adachi cited with respect to claim 3 also discloses the limitations of claim 4. Ex. 1003, ¶ 243.

5. Claim 8

"The device of claim 1, wherein the device is selected from a group comprising an opto-electric device and a light-emitting device."

The surface mountable electronic device disclosed by Adachi contains LED element D, (Ex. 1005, ¶¶ 0040-41 ("chip-type light emitting electronic component T"), 0042, Fig. 10, [Explanation of symbols] ("D light emitting diode (LED) element")), and therefore is "an opto-electric device and a light-emitting device." Ex. 1003, ¶¶ 244-45.

E. Ground 4: Nagayama Anticipates Claims 1-4 and 8

1. Claim 1

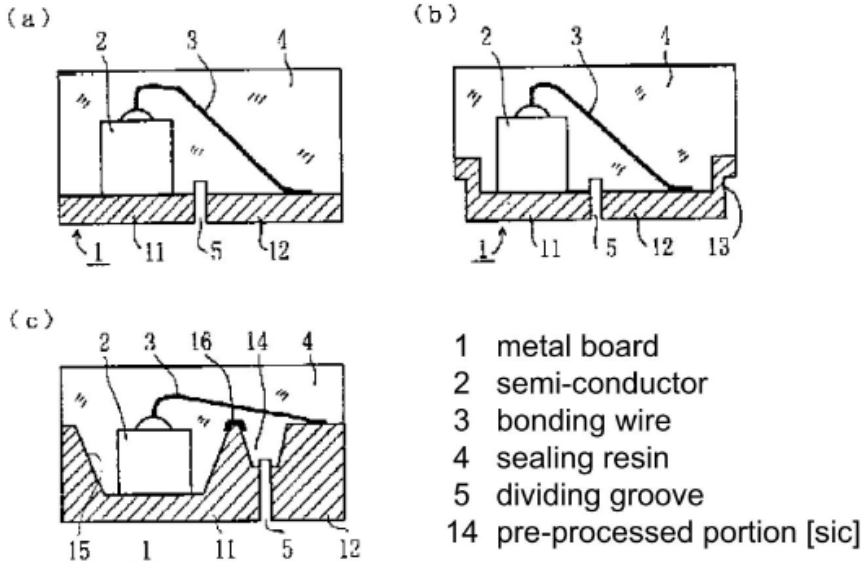
1[preamble] "A surface mountable electronic device, comprising:"

If the preamble is limiting, it is disclosed by Nagayama. Ex. 1003, ¶¶ 247-50.

Nagayama discloses three embodiments of a surface mountable LED package (*i.e.*, an electronic device), each illustrated in Nagayama's Figure 1,

below, which embodiments include a metal board 1 containing electrical contact portions for surface mounting, *e.g.*, to a printed circuit board. Ex. 1006, ¶¶ 0003 ("SMD (surface mounted devices)"), 0016 ("The semiconductor 2 [shown in Figure 1], which is an LED element, is die bonded with a conductive adhesive (silver paste or the like) in an area that becomes the first portion 11 of the metal board 1."), 0017 ("The bottom face[s] of the first portion 11 and the second portion 12 of the metal board 1 [shown in Figure 1] are used as-is for SMD surface electrodes."), 0018 ("[A] surface treatment (for example performing metal plating with good wettability by solder, applying flux or the like)[,] to further improve the solderability[,] can be performed on the metal board 1.").

[FIG. 1]



Id., Fig. 1.

1[a] "a packaged body having a mounting surface"

Nagayama discloses that its surface mountable LED packages (shown in Nagayama's Figure 1 above) have "a packaged body having a mounting surface." Ex. 1003, ¶¶ 251-57.

For example, Nagayama discloses that reference numeral "4 is sealing resin, the main component of which is, for example, epoxy resin, which has high transparency with respect to the wavelength of the emitted LED light, this [sealing resin] being hardened after filling around the semiconductor 2 and the bonding wire 3, to protect the device." Ex. 1006, ¶ 0017; *see also* ¶ 0023; Ex. 1003, ¶ 251.

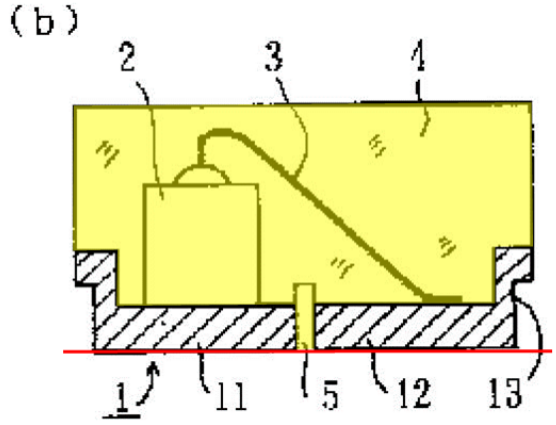
Nagayama further discloses that "dividing groove 5," also shown in Nagayama's Figure 1 above, is formed by a "half-dicing" step during manufacturing that separates the metal board into two portions, and that this dividing groove is subsequently filled with adhesive for improved strength. Ex. 1006, ¶ 0023 (Describing, with reference to Nagayama's Figure 3, a manufacturing method for Nagayama's surface mountable LED devices in which "a half-dicing groove 101 is machined by suitably adjusting the cutting depth of a dicing saw (dicer), and areas 111 that become the first portion of the metal board and areas 112 that become the second portion are divided. This is the situation shown in [Figure 3(c).] The strength can be

improved by filling the half-dicing groove 101 with adhesive as necessary."), Fig. 3.

Nagayama's sealing resin 4 and the adhesive filling dividing groove 5 together constitute a "packaged body," as they both provide the strength necessary to protect the LED and other electrical components therein. Ex. 1003, ¶¶ 252-54.

As detailed with respect to the preamble of claim 1, above, Nagayama further discloses that the packaged body of its surface mountable LED device has a "mounting surface." Ex. 1006, ¶¶ 0017 ("The bottom face[s] of the first portion 11 and the second portion 12 of the metal board 1 [shown in Figure 1] are used as-is for SMD surface electrodes."), 0018 ("[A] surface treatment (for example performing metal plating with good wettability by solder, applying flux or the like)[,] to further improve the solderability[,] can be performed on the metal board 1."); Ex. 1003, ¶ 255.

The "packaged body" (yellow shading) and "mounting surface" (red line at the bottom of electrode portions 11 and 12 and adhesive filled groove portion 5) are shown in Nagayama's Figure 1(b), below.

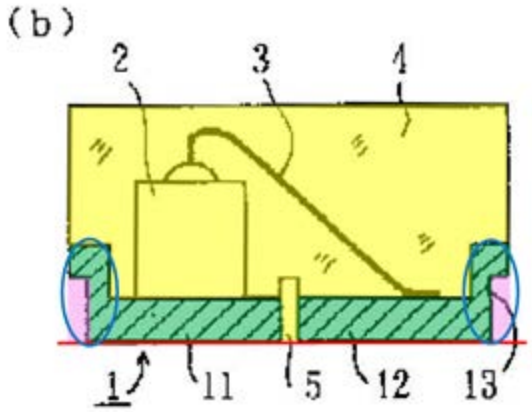


Ex. 1006, Fig. 1(b); Ex. 1003, ¶ 256.

1[b] "the mounting surface having a plurality of recesses at side edges of the body"

Nagayama discloses that the mounting surface of the second embodiment of its surface mountable LED device (depicted in Nagayama's Figure 1(b) above) has "a plurality of recesses," that are "at side edges of the body." Ex. 1003, ¶ 258.

The recesses are depressions or indentations in the yellow packaged body, at side edges thereof; and the areas defined by the recesses are circled in blue in Figure 1(b) of Nagayama, below. Those areas are occupied by metal board portions 11 and 12 (green), as well as the pink spaces beneath. *Id.*, ¶ 259.

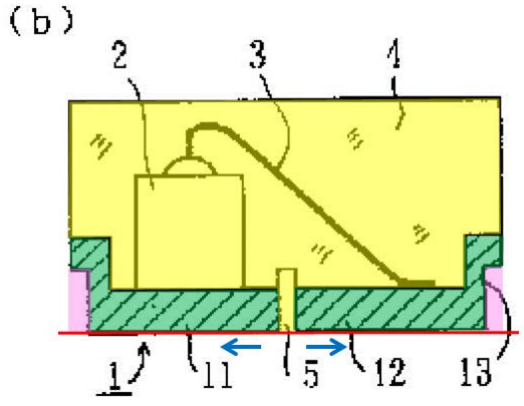


Ex. 1006, Fig. 1(b); *see also* ¶ 0018 ("the pre-processed portions 13 that contact the solder have a pre-treated surface").[17]

[17] If the "recesses" are the depressions or indentations in the ***device as a whole***, then, in Nagayama, the "recesses" would define just the pink-shaded regions. Ex. 1003, ¶ 259.

1[c] "a plurality of electrical contacts, each of which extends from an interior portion of the mounting surface and terminates in one of said recesses, and each of which conforms to one of said recesses"

Nagayama discloses "a plurality of electrical contacts," *i.e.*, metal board portions 11 and 12 (green in Nagayama's Figure 1(b) below). Ex. 1006, ¶¶ 0016 ("The semiconductor 2 [shown in Figure 1], which is an LED element, is die bonded with a conductive adhesive (silver paste or the like) in an area that becomes the first portion 11 of the metal board 1. The upper electrode of the same and an area that becomes the second portion 12 of the metal board 1 are connected with a gold bonding wire 3, for example."), 0017 ("The bottom face[s] of the first portion 11 and the second portion 12 of the metal board 1 are used as-is for SMD surface electrodes."). Ex. 1003, ¶¶ 260-62.



Ex. 1006, Fig. 1(b).

As further shown in Nagayama's Figure 1(b) above, each of the metal portions 11 and 12 (green), *i.e.*, "the electrical contacts," "extends from an interior portion of the mounting surface" ("extending" shown with blue arrows) and "terminates in one of said recesses" (*i.e.*, the depressions or indentations in the yellow package body), and "each of which conforms to one of said recesses" (*i.e.*, the electrical contacts are adapted to, and follow, the depressions or indentations in the yellow packaged body).[18] Ex. 1003, ¶ 263.

1[d] "wherein said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts"

As shown in Figure 1(b), below, Nagayama discloses "recesses [depressions or indentations in the yellow packaged body] and electrical contacts [green]" that "are sized to provide offsets [indicated by blue arrows] between said mounting surface [red line] and said electrical contacts." Ex. 1003, ¶ 264.

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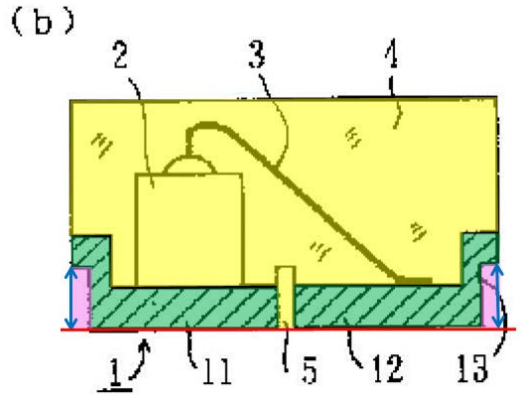
[18] If the "recesses" are the depressions or indentations in the ***device as a whole***, the electrical contacts conform to the "recesses," at least under Patent Owner's proposed construction of "conforms to" as "gives the same shape, outline, or contour to." Ex. 1011, 5; Ex. 1010, 2; Ex. 1003, ¶ 263.



Ex. 1006, Fig. 1(b).

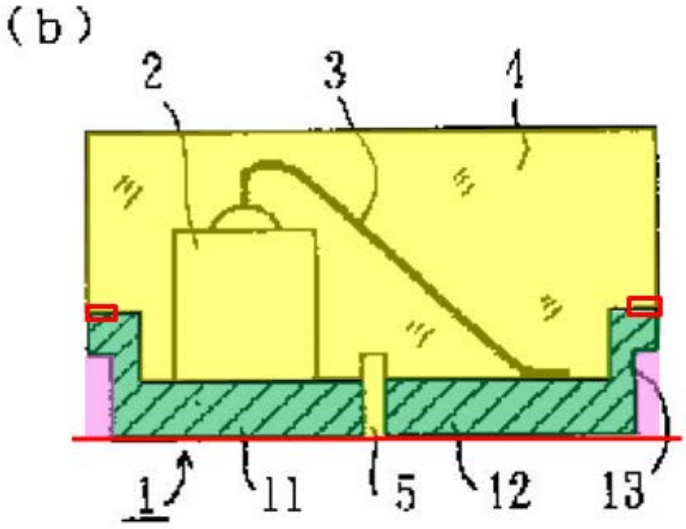
As shown by the blue bidirectional arrows above, the offsets (the pink spaces) are the result of the sizing of the recesses and the electrical contacts.[19] Ex. 1003, ¶ 265.

[19] This is true (i) whether the recesses are the depressions or indentations in the yellow packaged body, which include therein the contacts colored green, in which case the offsets are the spaces colored pink; or (ii) whether the recesses are the depressions or indentations in the ***device as a whole***, in which case the offsets would be those same pink spaces (or the vertical components thereof). Ex. 1003, ¶ 265.

2. Claim 2

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is substantially parallel to said mounting surface."

Nagayama's Figure 1(b) surface mountable LED package embodiment, below, discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is substantially parallel to said mounting surface [red line]." Ex. 1003, ¶ 266.



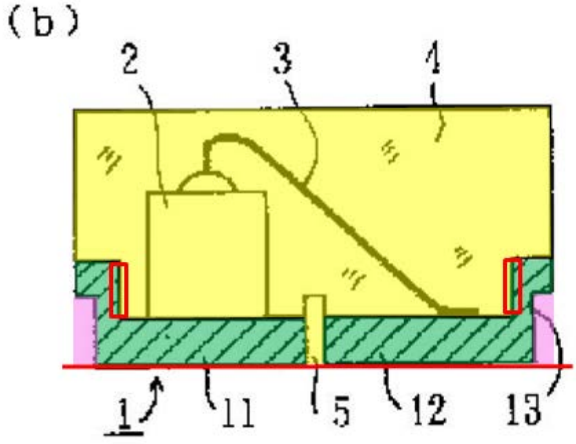
Ex. 1006, Fig. 1(b).[20]

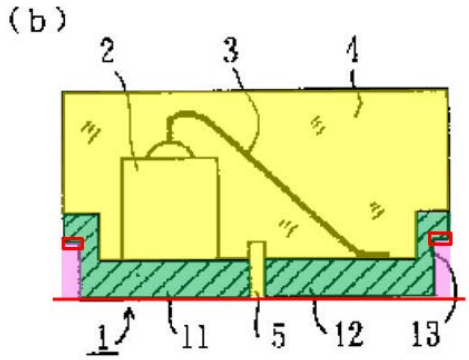
[20] Or, if the recesses are depressions or indentations in the ***device as a whole***:

3. Claim 3

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is not parallel to said mounting surface."

Nagayama's Figure 1(b) surface mountable LED package embodiment, below, discloses that "at least a portion [red boxes] of each electrical contact [green] conforms to at least a portion of a recess that is not parallel to said mounting surface [red line]." Ex. 1003, ¶ 267.





Ex. 1006, Fig. 1(b); Ex. 1003, ¶ 266.

Id., Fig. 1(b).[21]

4. Claim 4

"The device of claim 3, wherein said portions of the recesses that are not parallel to said mounting surface are orthogonal to said mounting surface."

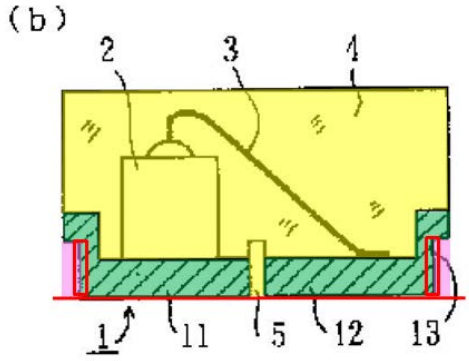
The disclosure in Nagayama cited with respect to claim 3 also discloses the limitations of claim 4. Ex. 1003, ¶ 268.

5. Claim 8

"The device of claim 1, wherein the device is selected from a group comprising an opto-electric device and a light-emitting device."

The surface mountable electronic device disclosed by Nagayama contains an LED semiconductor die 2, (Ex. 1006, ¶¶ 0016-17), and therefore

[21] Or, if the recesses are depressions or indentations in the ***device as a whole***:



Ex. 1006, Fig. 1(b); Ex. 1003, ¶ 267.

is "an opto-electric device and a light-emitting device." Ex. 1003, ¶¶ 269-70.

F. Ground 5: Okazaki Anticipates Claims 1-4, 8, and 11

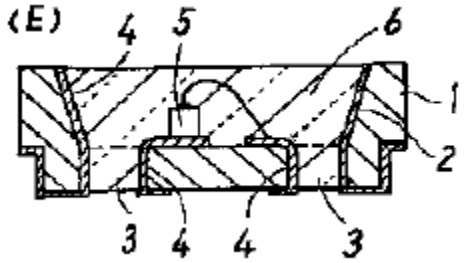
1. Claim 1

1[preamble] "A surface mountable electronic device, comprising:"

If the preamble is limiting, it is disclosed by Okazaki. Ex. 1003, ¶¶ 272-75.

Okazaki discloses a prior art surface mountable electronic device containing an LED chip. Ex. 1007, ¶¶ 0001 ("The present invention relates to light emitting devices used for backlights in liquid crystal display devices and light source arrays in facsimile devices and the like, or for displays in various operating panels, and to a method for manufacturing the same, and particularly concerns chip type light emitting devices for surface mounting…."), 0002 ("Proposal Example 2 shown in FIG. 5 (A) through (E)."); *see also* ¶¶ 0006 ("an object of the present invention is to provide a light emitting device allowing for cost reductions, and with which solder wettability when soldering can be improved"), 0014 ("mounting by soldering on the external mounting board"), 0032 ("in the embodiment described above, one through hole is formed for each device, but there may also be two, as shown in FIG. 5"); Ex. 1003, ¶¶ 273-74.

This prior art device, depicted in cross-sectional view in Okazaki's Figure 5(E) below, includes three-dimensional wiring patterns 4 plated on an insulating block body 1 having through holes 3, and a light emitting element 5 mounted on the three-dimensional wiring pattern. Ex. 1007, ¶ 0002, [Brief Description of the Drawings]; Ex. 1003, ¶ 275.



Ex. 1007, Fig. 5(E).

1[a] "a packaged body having a mounting surface"

Okazaki discloses that its surface mountable electronic LED device includes "a packaged body," *i.e.*, "insulating block body 1," having a "mounting surface." Ex. 1003, ¶¶ 276-78.

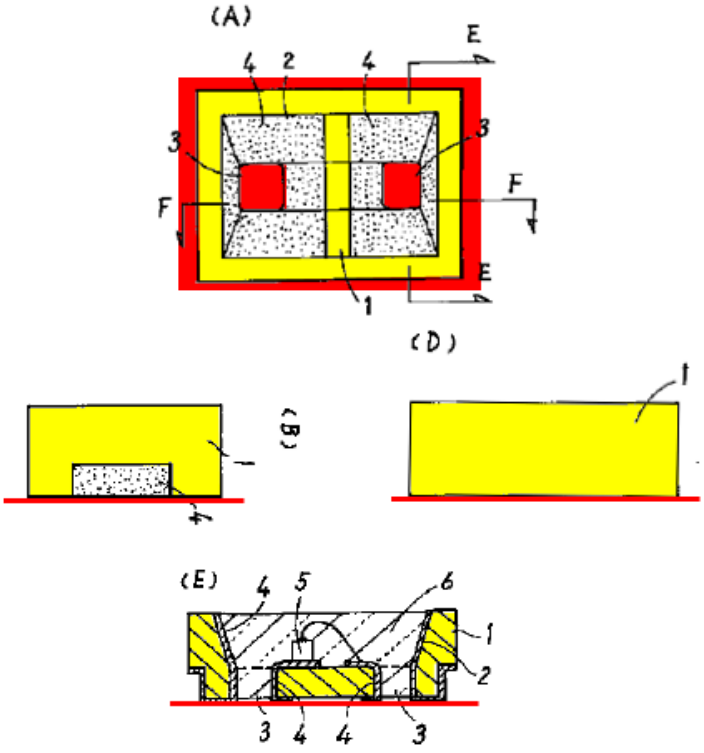
In particular, Okazaki discloses:

> In the field of chip component type light emitting devices, recent leadless types include those in which a three-dimensional wiring pattern is formed by plating on an insulating substrate and a light emitting element is mounted thereon. Furthermore, in particular, the applicant considered Proposal Example 1 shown in FIG. 4 (A) through (F) and Proposal Example 2 shown in FIG. 5 (A) through (E). No

> lead frames are used in either of these, but rather a recess 2 is provided in an insulating block body 1, a through hole 3 is formed in the bottom surface of the recess 2, three-dimensional wiring patterns 4 (plating layers) are formed directly thereon by a metal plating treatment, and a light emitting element 5 (LED) is mounted using this as a substrate.

Ex. 1007, ¶ 0002.

Okazaki's "packaged body" is yellow in Okazaki's Figures 5(A) (plan view), 5(B) (right-side view), 5(D) (front view), and 5(E) (cross-sectional view along line F-F in Fig. 5(A)) below, and its "mounting surface," which is essentially co-planar with the plated bottom of insulating block body 1, is identified in red. Ex. 1003, ¶ 279.

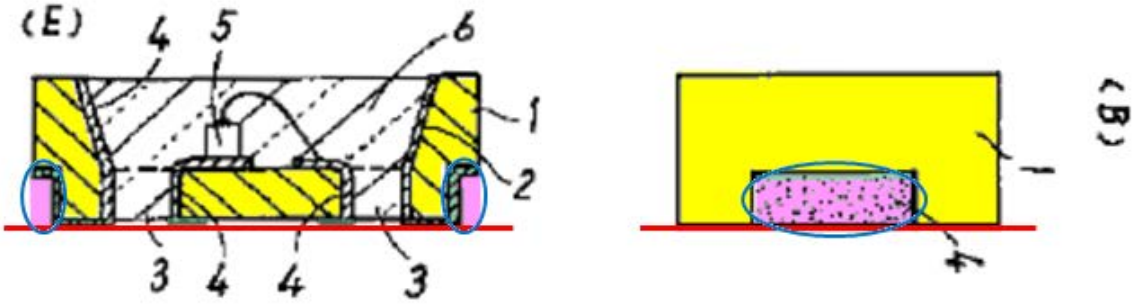


Ex. 1007, Fig. 5 (excerpt, annotation shows mounting surface as red line at bottom of metal plating 4 and body 1 in side and cross-sectional views, and as a planar red surface in the plan view of Fig. 5(A), including portions visible inside through-holes 3); *see also* [Brief Description of the Drawings], ¶¶ 0002, 0005 ("if silver plating, which has good reflection efficiency, is used for the plating layers 4, in order to improve the adhesion (hereafter, referred to as solder wettability) of the plating layers 4 when soldering" to an external mounting board), 0014 ("mounting by soldering on the external mounting board").

1[b] "the mounting surface having a plurality of recesses at side edges of the body"

Okazaki discloses that "the mounting surface" of its surface mountable electronic LED device has "a plurality of recesses at side edges of the body." Ex. 1003, ¶¶ 280-82.

The recesses at side edges of the body are the depressions or indentations in the yellow packaged body, and the areas defined thereby are identified by blue circles in Okazaki's Figures 5(B) and 5(E) below. They are occupied by portions of metal plating 4 (green), as well as the pink spaces beneath. Ex. 1003, ¶¶ 280-82.



Ex. 1007, Figs. 5(B), 5(E) (excerpt, in Figure 5(B), wherein the area shaded pink represents space behind which a vertical wall of metal plating 4 is located, as shown in cross-sectional view 5(E)).[22]

1[c] "a plurality of electrical contacts, each of which extends from an interior portion of the mounting surface and terminates in one of said recesses, and each of which conforms to one of said recesses"

Okazaki discloses that its surface mountable electronic LED device has a "plurality of electrical contacts," *i.e.*, bottom portions of plating layer 4, "formed … by a metal plating treatment," that may be made of gold or silver, (Ex. 1007, ¶¶ 0002-3), and that provide electrical connection to the LED terminals via conductive paste and a wire bond (*id.*, ¶¶ 0015-16, Fig. 5(E)). Ex. 1003, ¶ 283.

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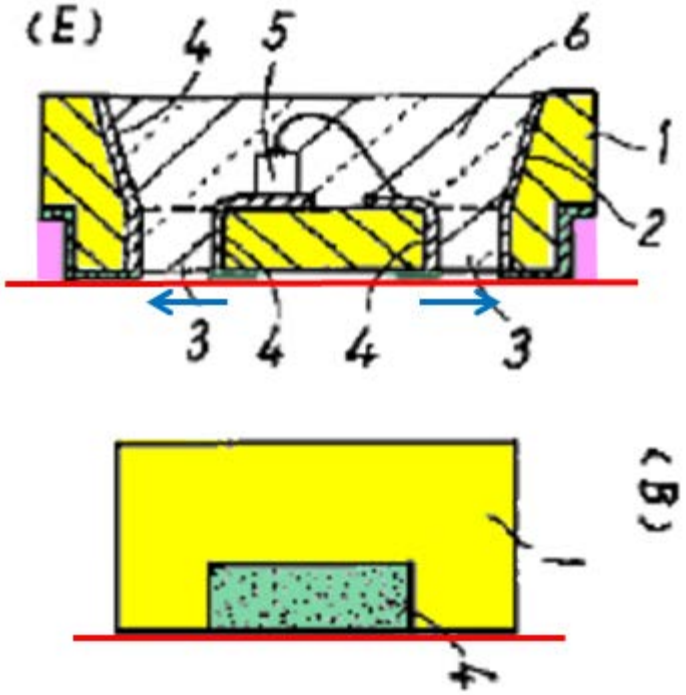
[22] If the claimed "recesses" are the depressions or indentations in the ***device as a whole***, then, in Okazaki, the "recesses" would define just the pink regions. Ex. 1003, ¶ 282.

As further disclosed by Okazaki, these electrical contacts, green in Okazaki's Figures 5(B) and 5(E), below, each "extend[] from an interior portion of the mounting surface [as indicated by blue arrows] and terminate[] in one of [the] recesses," (*i.e.*, the depressions or indentations in the yellow packaged body) and "conform to one of [the] recesses" (*i.e.*, the contacts are adapted to, and follow, the depressions or indentations in the yellow packaged body).[23] Ex. 1003, ¶¶ 285-86. A POSA would have understood the green contact portions, separated by through-holes 3 in the cross-sectional view of Figure 5(E), to be electrically connected by plating that extends around the circumferences of the respective through-holes. Ex. 1003, ¶ 284; Ex. 1007, Figs. 5(A), 5(C).

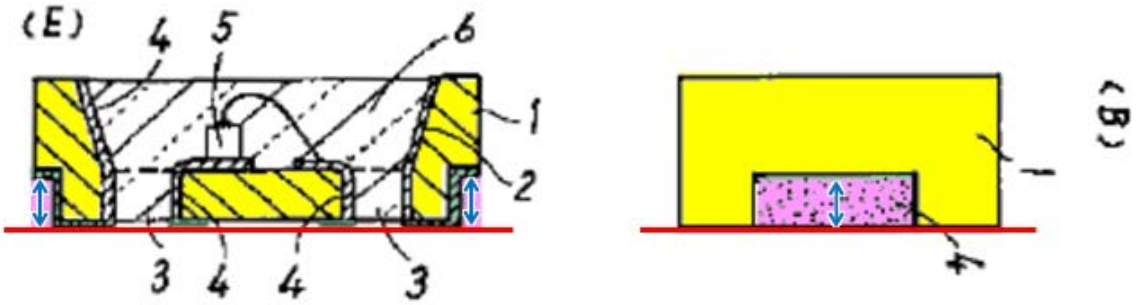
[23] If the claimed "recesses" are the depressions or indentations in the ***device as a whole***, the electrical contacts conform to the "recesses," at least under Patent Owner's proposed construction of "conforms to" as "gives the same shape, outline, or contour to." Ex. 1011, 5; Ex. 1010, 2; Ex. 1003, ¶ 286.



Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view, omitting the pink shading indicating the space in front of the metal plating (green)).

1[d] "wherein said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts"

As shown in Okazaki's Figures 5(B) and 5(E) below, Okazaki discloses that "said recesses and electrical contacts are sized to provide offsets between said mounting surface and said electrical contacts." Ex. 1003, ¶ 287.



Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view).

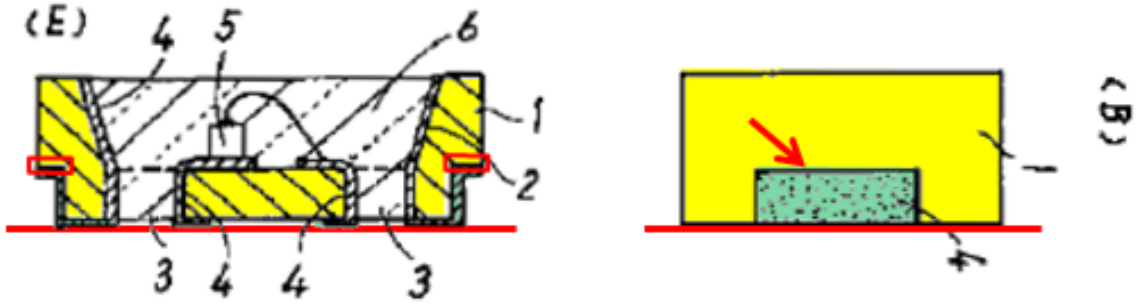
As shown by the blue bidirectional arrows above, the offsets (the pink spaces) are the result of the sizing of the recesses and the electrical contacts.[24] Ex. 1003, ¶ 288.

[24] This is true (i) whether the recesses are the depressions or indentations in the yellow packaged body, which include therein the contacts colored green, in which case the offsets are the spaces colored pink; or (ii) whether the recesses are the depressions or indentations in the ***device as a whole***, in which case the offsets would be those same pink spaces (or the vertical components thereof). Ex. 1003, ¶ 288.

2. Claim 2

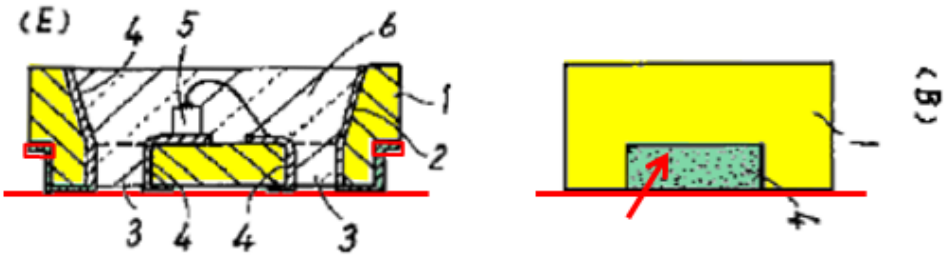
"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is substantially parallel to said mounting surface."

As indicated by red boxes and a red arrow in Okazaki's Figures 5(B) and 5(E), Okazaki discloses that "at least a portion of each electrical contact [green] conforms to at least a portion of a recess that is substantially parallel to said mounting surface [red line]." Ex. 1003, ¶ 289.



Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view).[25]

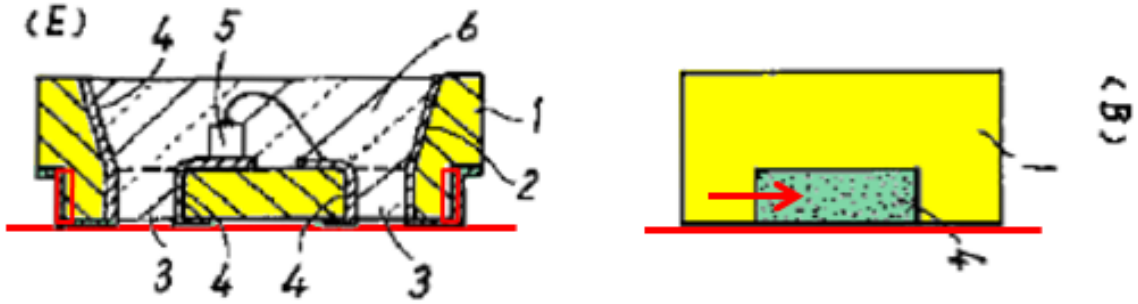
[25] Or, if the recesses are depressions or indentations in the ***device as a whole***:



3. Claim 3

"The device of claim 1, wherein at least a portion of each electrical contact conforms to at least a portion of a recess that is not parallel to said mounting surface."

As indicated by red boxes and a red arrow in Okazaki's Figures 5(B) and 5(E), below, Okazaki discloses that "at least a portion of each electrical contact [green] conforms to at least a portion of a recess that is not parallel to said mounting surface [red line]." Ex. 1003, ¶ 290.



Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view).[26]

Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view); Ex. 1003, ¶ 289.

[26] Or, if the recesses are depressions or indentations in the ***device as a whole***:

4. Claim 4

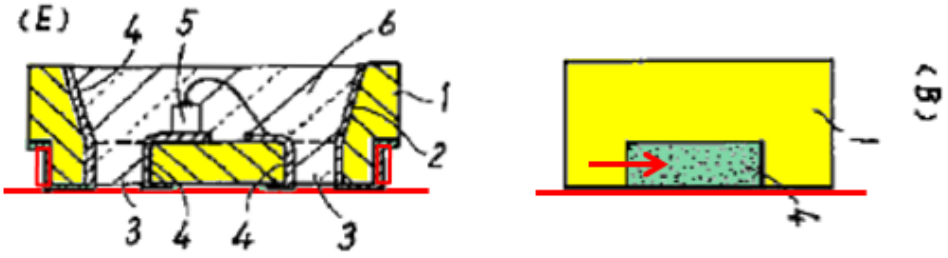
"The device of claim 3, wherein said portions of the recesses that are not parallel to said mounting surface are orthogonal to said mounting surface."

The disclosure in Okazaki cited with respect to claim 3 also discloses the limitations of claim 4. Ex. 1003, ¶ 291.

5. Claim 8

"The device of claim 1, wherein the device is selected from a group comprising an opto-electric device and a light-emitting device."

The surface mountable electronic LED device disclosed by Okazaki contains an LED chip 5, (Ex. 1007, ¶¶ 0001-2 ("a light emitting element 5 (LED) is mounted"), 0004, Fig. 5), and therefore is "an opto-electric device and a light-emitting device." Ex. 1003, ¶¶ 292-93.

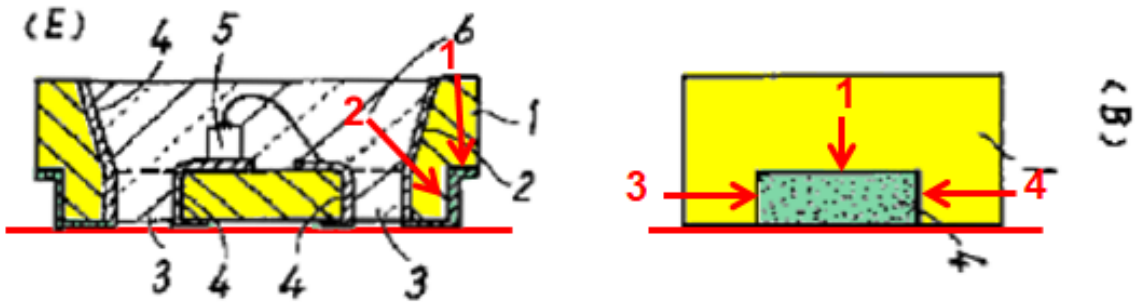


Ex. 1007, Figs. 5(E) (cross-sectional view), 5(B) (right-side view); Ex. 1003, ¶ 290.

6. Claim 11

"The device of claim 1, wherein one or more of the recesses is bounded on three sides."

Okazaki's Figures 5(B) and 5(E) (below) have been annotated with red arrows, numbered consistently to indicate surfaces that are the same in each figure, to show that Okazaki's surface mountable electronic LED device provides recesses having boundaries on three sides. Four sides are identified, any three of which meet this limitation. Ex. 1003, ¶¶ 294-95.



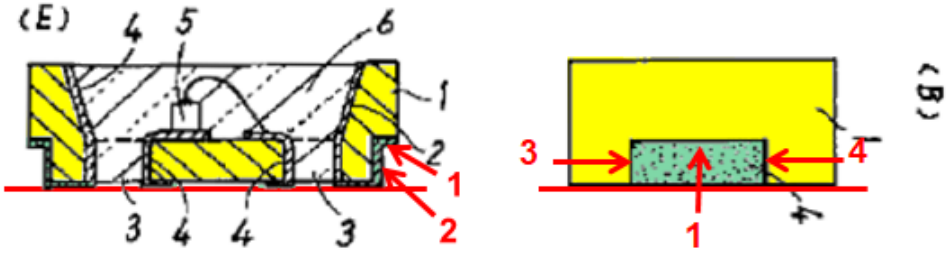
Ex. 1007, Figs. 5(E) (cross-sectional view, annotation shows the boundaries in one "recess"), 5(B) (right-side view).[27]

[27] Or, if the recesses are the depressions or indentations in the ***device as a whole***:

By way of further clarification, Okazaki's Figure 5(D) (depicting the front view of the device as a rectangle) confirms that the green contact depicted in the side view of Okazaki's Figure 5(B) is recessed into the packaged body (yellow), and that bounding surfaces exist at the locations marked "3" and "4" in Okazaki's Figure 5(B) above. Ex. 1003, ¶¶ 296-97. Okazaki's Figure 5(D) may also be compared with Okazaki's Figure 4(D), which shows the front view of a different prior-art device lacking analogous boundaries at locations "3" and "4." Ex. 1003, ¶ 297.

VI. Conclusion

Claims 1-4, 8, and 11 are unpatentable. Petitioner requests cancellation.



Ex. 1007, Figs. 5(E) (cross-sectional view, annotation shows the boundaries in one "recess"), 5(B) (right-side view); Ex. 1003, ¶ 295.

Respectfully submitted,

SHEARMAN & STERLING LLP

Dated: May 18, 2020

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CERTIFICATE OF COMPLIANCE

I hereby certify that this paper complies with the type-volume limitation of 37 C.F.R. §42.24 (as determined by the Microsoft Word word-processing system used to prepare this paper) because it contains 13,985 words, excluding the parts of the paper exempted by 37 C.F.R. §42.24(a).

Dated: May 18, 2020

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CERTIFICATE OF SERVICE

I hereby certify that the foregoing Petition for *Inter Partes* Review and the Exhibits listed on the List of Exhibits were served on May 18, 2020, via Federal Express overnight upon the following:

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