UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC.,
Petitioner

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,651,134

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I. INTRODUCTION

Advanced Micro Devices, Inc. ("Petitioner") requests *inter partes* review ("IPR") of Claims 1-21 of U.S. Patent No. 6,651,134 ("the '134 Patent") (Ex-1001), currently assigned to Monterey Research, LLC ("Patent Owner").

The '134 Patent discloses neither a new memory circuit design, a new memory addressing technique, nor a new data transfer technique. Indeed, the patent admits that conventional memories can be accessed in both single address mode and in "burst" mode, wherein multiple data locations are accessed in response to a single initial address. Ex-1001 at 1:14-16. The claims of the '134 Patent merely combine techniques and memory architectures already well known in the art.

The claimed improvement of the '134 Patent is to read and write data from a memory using a burst of internal address signals wherein the generation of internal address signals is "non-interruptible." Specifically, the '134 Patent notes that while conventional systems employing static random access memory (SRAM) can operate in a burst mode that can be started and stopped in response to a control signal (*Id.* at 1:16-18), conventional systems employing dynamic random access memory (DRAM) are required to periodically interrupt burst transfers in order to refresh the charge on the memory cells, which slowly leaks away. *Id.* at 1:19-24. Nevertheless, the claims of the '134 Patent are written to encompass not only

DRAM systems, configured to hide refresh cycles behind burst reads of other memory partitions, but also SRAM systems, which do not need to be interrupted because they do not require refresh. *Compare, e.g.,* claims 1, 8, and 9. So it is not surprising that the claims were rejected multiple times during prosecution over prior art disclosing generating internal addresses in a continuous burst. The applicant finally overcame those rejections after filing an appeal brief and arguing that while the primary prior art reference did disclose continuous burst transfers using internally generated addresses, it also disclosed that there was a way for a burst to be terminated, so it was not non-interruptible. *See, e.g.,* Ex-1004 (File History) at 115.

Prior art presented in this Petition, which was not considered during prosecution, teaches an apparatus and method for generating a predetermined number of internal address signals for reading from and writing to memory wherein the burst of internal address signals is non-interruptible. The primary reference, Wada, anticipates the independent claims, disclosing memory burst transfers that are not interrupted. Nevertheless, because of the patentee's narrowing arguments during prosecution, Petitioners also present the combination of Wada and Barrett, which expressly teaches bursts that are non-interruptible. Thus, for the reasons set forth in this Petition, Claims 1-21 of the '134 Patent are unpatentable. These grounds are likely to prevail, and this Petition should be

granted and the challenged claims cancelled.

II. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner Advanced Micro Devices, Inc. and ATI Technologies ULC are the real parties-in-interest. ATI Technologies ULC is an indirect, wholly owned subsidiary of Advanced Micro Devices, Inc.

Related Matters:

- Patent Owner has asserted the '134 Patent against Petitioner in *Monterey Research, LLC v. Advanced Micro Devices, Inc.*, No. 1:19-cv-02149-CFC (D. Del.).
- The '134 Patent was previously asserted in the International Trade Commission in *In the Matter of Certain Static Random Access Memories and Products Containing the Same*, Inv. No. 337-TA-792 (U.S.I.T.C., hereinafter the "792 Investigation") and in District Court in *Cypress Semiconductor Corp. v. GSI Tech., Inc.*, No. 13-cv-02013-JST (N.D. Cal).

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III. FEE AUTHORIZATION

Pursuant to 37 C.F.R. §42.15(a) and §42.103(a), the PTO is authorized to charge $34,400 (or other fees required for this filing) to Deposit Account No. 50-0639.

IV. GROUNDS FOR STANDING

Under 37 C.F.R. §42.102(a)(2), §42.104(a), Petitioner certifies that the '134 Patent is available for IPR, this Petition is timely filed, and Petitioner is not barred or estopped from requesting IPR review on the grounds presented.

V. PRECISE RELIEF REQUESTED

Petitioner respectfully requests review and cancellation of all 21 claims of

the '134 Patent under 35 U.S.C. §102 and/or §103 based on the following grounds:

Ground 1: Claims 1-3, 8, 12-13, 16, and 17 are anticipated by US 6,115,280 ("Wada");

Ground 2: Claims 1-4, 8, 12-14, 16, and 17 are rendered obvious by Wada in view of the knowledge of a person of ordinary skill in the art ("POSITA");

Ground 2a: Claims 1-4, 8, 12-14, 16, and 17 are rendered obvious by Wada and US 5,584,033 ("Barrett") in view of the knowledge of a POSITA;

Ground 3: Claims 4-7, and 18-20 are rendered obvious by Wada and U.S. 6,185,149 ("Fujioka") in view of the knowledge of a POSITA.

Ground 3a: Claims 4-7, and 18-20 are rendered obvious by Wada, Barrett, and Fujioka in view of the knowledge of a POSITA

Ground 4: Claims 9-10, 14, and 21 are rendered obvious by Wada and US 6,226,755 ("Reeves") in view of the knowledge of a POSITA;

Ground 4a: Claims 9-10, 14, and 21 are rendered obvious by Wada, Barrett, and Reeves in view of the knowledge of a POSITA;

Ground 5: Claims 11 and 15 are rendered obvious by Wada and US 5,784,331 ("Lysinger") in view of the knowledge of a POSITA; and

Ground 5a: Claims 11 and 15 are rendered obvious by Wada, Barrett, and Lysinger in view of the knowledge of one a POSITA.

None of the references relied upon in this Petition was cited by the Examiner

during prosecution of the ’134 Patent. Ex-1001, 1.

VI. THE CHALLENGED PATENT

The ’134 Patent is directed to a system and method for addressing a memory circuit with a burst of internal address signals that may be non-interruptible. Ex. 1001 at Abstract. A device reads data from memory by asserting an address and receiving data from the memory location specified by that address. In “burst” mode, however, a controller asserts a single address, and memory circuit logic generates a series of internal addresses, typically offset from the initial address as address+0, address+1, address+2, etc., and returns data from multiple memory locations specified by those internal addresses in response to one external addresses. Ex-1002 ¶35.

An embodiment of the alleged invention is “configured to transfer a fixed number of words of data with each access (e.g., read or write).” Ex-1001 at 2:28-30. An array of memory cells may be addressed by a “burst address counter” circuit that receives an external address (ADDR_EXT), a clock (CLK), and control signals (*e.g.*, LOAD, ADV) and that outputs a burst of internal addresses ADDR_INT that access the memory cells. *See id.* at 2:31-46. Figure 1, for example, depicts “Burst Address Counter / Register” 102, which latches in external address ADDR_EXT when the LOAD signal is asserted. *Id.* at 3:14-19. When ADV is asserted, a fixed number of internal addresses (ADDR_INT) are generated

in response to the CLK signal. *Id.* at 3:19-24. "Once the circuit 102 has started generating the fixed number of addresses, the circuit 102 will generally not stop until the fixed number of addresses has been generated (*e.g.*, a non-interruptible burst)." *Id.* at 3:25-29.

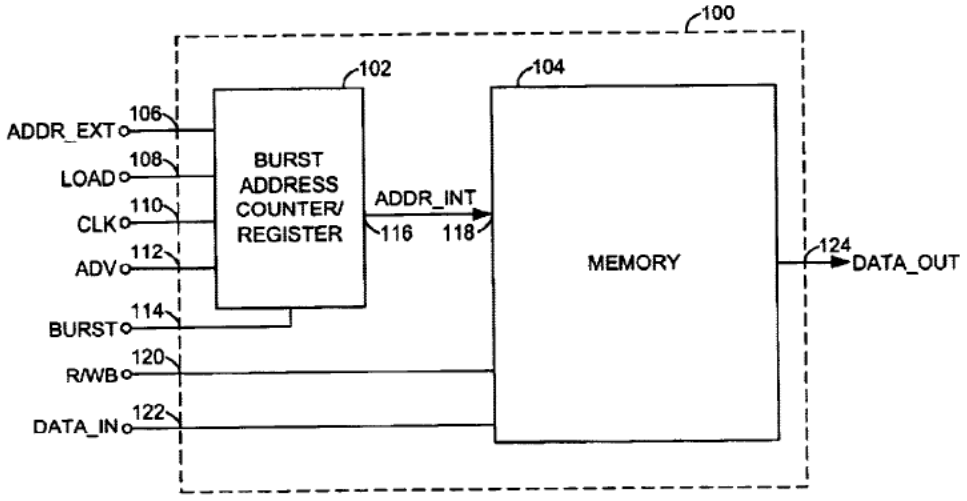


FIG. 1

The '134 Patent discloses two embodiments of the "Burst Address Counter" 102, depicted in Figures 2 and 3. In Fig. 2, below, an initial address (ADDR_EXT) is latched into the address counter register 126 when LOAD is asserted. *Id.* at 4:6-8. When ADV is asserted, the BURST_CLK signal is generated in response to CLK and increments the address in the address counter register 126 to produce a predetermined number of internal address values ADDR_INT (116). *Id.* at 4:6-14.

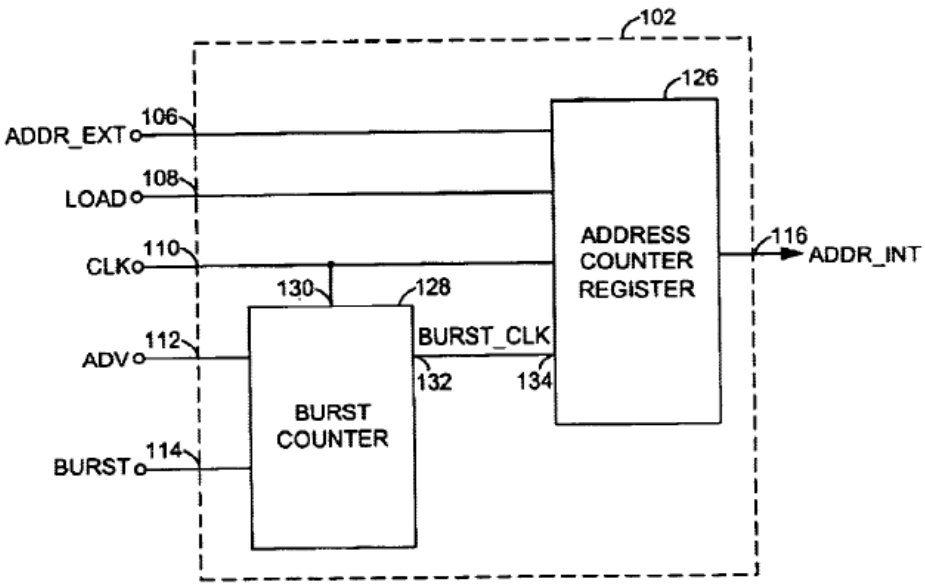


FIG. 2

In Figure 3, an n-bit external address (ADDR_EXT) is divided into an m-bit portion and a k-bit portion. *Id.* at 4:18-25. The k-bit portion is sent to counter (138) and is incremented by the CLK signal when ADV is asserted. *Id.* at 4:28-33. A multiplexer (136) selects either the latched k-bit portion of the external address (142) or the k-bit output of the counter (138) and concatenates it with the latched m-bit portion of the address to create the internal addresses (ADDR_INT) that are used to address the memory array. *Id.* at 4:34-39; Ex-1002 ¶¶35-38

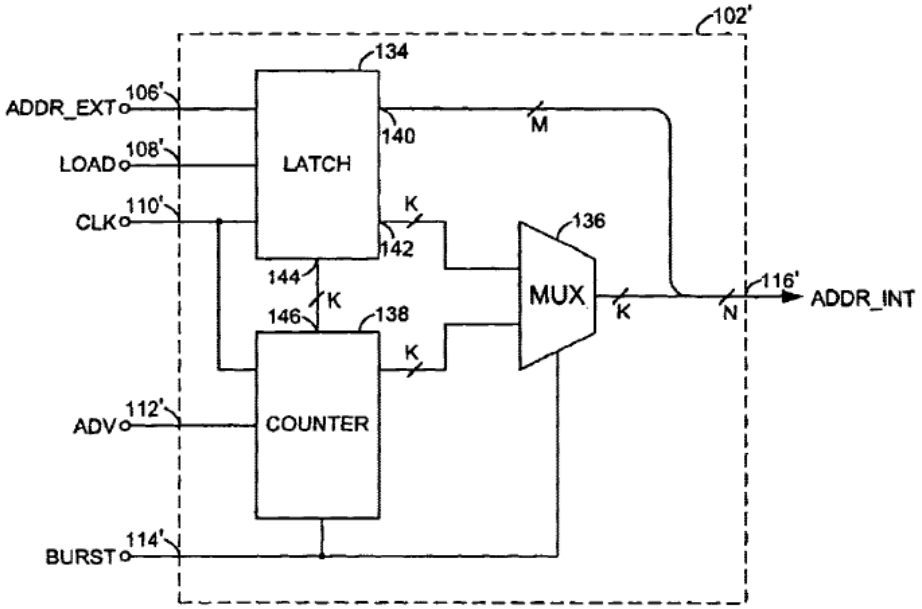


FIG. 3

VII. PATENT PROSECUTION HISTORY

The application that became the '134 Patent was repeatedly rejected during prosecution and eventually allowed after the Examiner did not file a response to the applicant's appeal brief.

On 10/1/2001, the Examiner rejected the 17 pending claims, rejecting dependent claims 6 and 15 (which recite that the burst length is programmed by "bond options") under 35 U.S.C. §112 paragraph 1 because the specification did not sufficiently support that concept. Ex. 1004 (File History) at 42. All claims were also rejected as anticipated by Yip (U.S. 6,289,138). *Id.* at 42-44. The applicant responded on 2/4/2002, and with respect to the Section 112 rejections, stated:

> Support for claims 5 and 15 may be found on page 8, lines 3-8 of the specification. Furthermore, bond options are well known in the art and, therefore, one skilled in the art would understand how to make and/or use bond options. Copies of U.S. patents 6,188,636 (issued February 13, 2001), 5,900,021 (issued May 4, 1999) and 5,360,992 (issued November 1, 1994) from the USPTO web site (www.uspto.gov) are attached as evidence of bond options being well known in the art.

Id. at 62. Regarding the 102 rejections, the applicant argued that Yip did not disclose "the generation of a predetermined number of internal address signals that is non-interruptible, as presently claimed." *Id.* at 63. Specifically, the patentee argued that Yip discloses a write burst "can be interrupted when there is a cycle request from a higher priority port…" *Id.* at 64. The applicant added three additional claims.

On 4/25/2002, the Examiner rejected claims 1-20 as anticipated by Cowles (US 5,729,504). *Id.* at 70-73. The applicant responded on 6/26/2002, arguing the internal address bursts were not non-interruptible, and added an additional claim. *Id.* at 83. The applicant asserted that "Cowles teaches that a low to high transition of the WE* signal within a burst write access to the memory array 112 will ***terminate*** the burst access, preventing further writes from occurring . . . ." *Id.* at 84 (emphasis original).

On 10/22/2002, the Examiner repeated and made final the Cowles rejection. *Id.* at 89. In response, the applicant argued that Cowles did not teach that the burst memory accesses were non-interruptible. *Id.* at 115. The Examiner rejected those

arguments in an Advisory action, and the applicant appealed, raising the same arguments on appeal. *Id.* at 14-16. The Examiner filed no responsive brief but instead issued a Notice of Allowance, conceding that Cowles disclosed "to terminate a continuous burst read operation, the WE signal merely has to transition high prior to a falling edge of the CAS signal (see, for example, Cowles). [T]hus prior art of record does not teach or fairly suggest the non-interruptible generation of a predetermined number of internal address signals." *Id.* at 172 (emphasis original); Ex-1002 ¶¶39-42.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

At the time the '134 Patent was filed, a person of ordinary skill in the art would have had a bachelor's degree in electrical or computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of memory circuits, related hardware design, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002 ¶43.

IX. CLAIM CONSTRUCTION

Petitioner interprets the '134 Patent's claims according to *Phillips*. 83 Fed. Reg. 51340, 51340-44 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). Certain terms of the '134 Patent were previously construed in the 792 Investigation (Order No. 29, Feb. 9, 2012) and in *Cypress Semiconductor*

Corp. v. GSI Tech., Inc., No. 13-cv-02013-JST (N.D. Cal July 29, 2014), attached hereto as Exhibits Ex-1011 and Ex-1012, respectively. The construction of the following claim terms may be relevant to this proceeding.

A. "non-interruptible" (claims 1, 16, 17)

The '134 Patent specification defines "non-interruptible" as follows:

> Once the circuit 102 has started generating the fixed number of addresses, the circuit 102 ***will generally not stop*** until the fixed number of addresses has been generated (e.g., ***a non-interruptible burst***).

Ex. 1001 ('134 Patent) at 3:3:36-28.[1] During prosecution, however, the applicant distinguished prior art disclosing a ***generally continuous*** address burst, arguing that any disclosure describing the possibility of terminating a burst rendered that burst not "non-interruptible," as was discussed above in the summary of the file history, suggesting a narrower construction. In the 792 Investigation, the parties agreed that "non-interruptible" means "cannot be stopped or terminated once initiated until the fixed number of internal addresses has been generated." Ex-1011 at 12-13.

Nevertheless, the Board need not resolve that issue here, as the prior art applied to the claims discloses this limitation under the narrower construction (cannot be stopped). Ex-1002 ¶¶44-46.

[1] Emphasis is added unless stated otherwise.

B. "means for reading data . . . / means for generating a predetermined number of said internal address signals" (claim 16)

During prosecution, the applicant agreed that claim 16 (then claim 12) should be construed as means-plus-function under pre-AIA 35 U.S.C. §112(6), although the applicant did not identify the claimed function or corresponding structure. Ex. 1004 (File History) at 129, 131, 146, 167. Claim 16 includes two "means" clauses: (a) "means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals," and (b) "means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal, and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible."

The function recited in element (a) is "reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals." The corresponding disclosed structure is the memory array 104 depicted in Figure 1 (annotated below) and described as "a static random access memory (SRAM), a dynamic random access memory (DRAM), or other appropriate memory to meet the design criteria of a particular implementation." Ex. 1001 ('134 Patent) at 2:34-38. The memory array 104 includes an address input 118 that receives a plurality of internal address signals, and a DATA_OUT line 124, and a

DATA_IN line 122 for reading data from and writing data to the memory. *Id.* at 2:44-29.

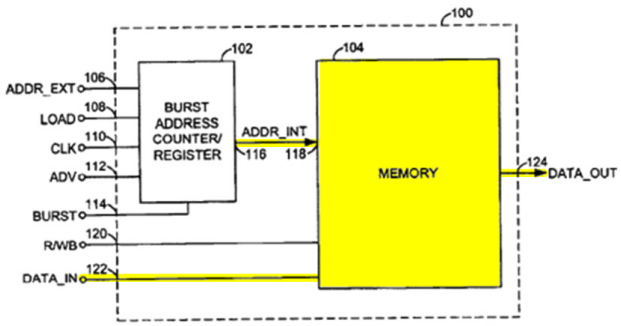


FIG. 1

The function in element (b) is "generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal, and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible." The corresponding structure is the "burst address counter/register 102" implemented either as shown in (1) Figure 2, described at 3:62-4:14 or (2) Figure 3, described at 4:15-39, or their equivalents. In annotated Figures 2 and 3 below, the logic blocks highlighted in yellow generate a predetermined number of internal address signals (ADDR_INT) in response to (i) an external address signal (green) (ii) a clock signal (blue) and (iii) one or more control signals (red). While Figure 2 uses a counter that increments the entire n-bit address, Figure 3 splits the address into two parts and increments only the bottom k bits, concatenating them with the m top bits to generate the n-bit internal address signals. Ex-1002 ¶¶47-49.

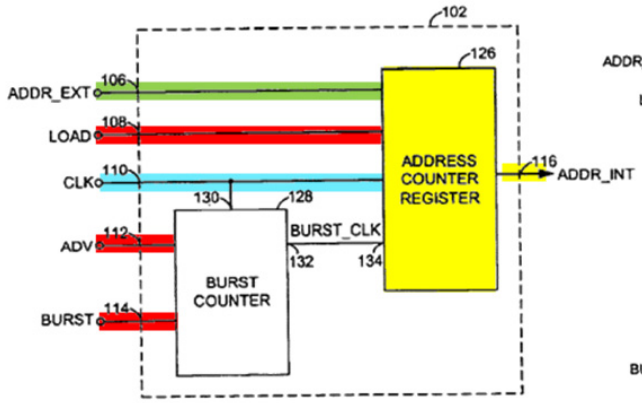


FIG. 2

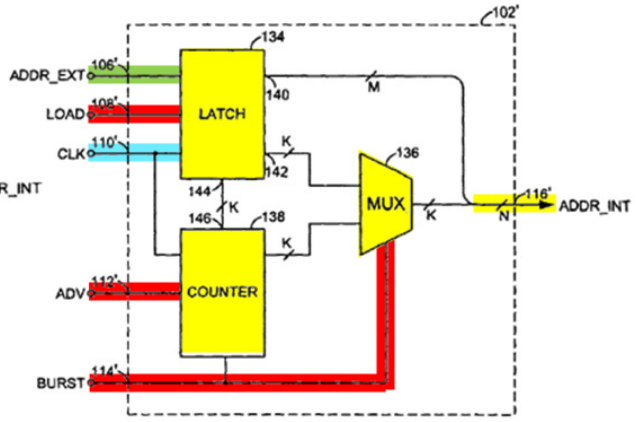


FIG. 3

C. "external address signal" (claims 1, 13, 15-17)

In the 792 Investigation, the parties agreed that "external address signal" means "an address signal that originates outside of the circuit." Ex-1011 at 12. Petitioner applies the prior art here consistent with that construction. Ex-1002 ¶50.

D. "burst" (claim 2)

In the 792 Investigation, the parties agreed that "burst" means "a number of words transferred as a group." Ex-1011 at 13. Petitioner applies the prior art here consistent with that construction. Ex-1002 ¶51.

E. "internal address signal" (claims 1, 2, 12, 15-17)

In the 792 Investigation, the ALJ construed this term to mean "an address signal that is generated within the circuit claimed by the preamble." *Id.* at 15. The order was referring to claim 1, in which the preamble reads "a circuit comprising." Thus, the "internal address signal" is generated within the circuit, as opposed to arriving from outside. Petitioner applies the prior art here consistent with that

construction. Ex-1002 ¶53.

F. "logic circuit" (claims 1, 12)

In the 792 Investigation, the ALJ construed this term to mean "a circuit that is designed to perform one or more logic operations or to represent logic functions." Petitioner applies the prior art here consistent with that construction. Ex-1002 ¶53.

G. "predetermined number of [said] internal address signals" (claims 1-4, 12, 15-17)

In the 792 Investigation, the ALJ construed this term to mean "a fixed number of internal address signals for a burst access." The Commission later affirmed a narrower reading by the ALJ, finding that a prior-art reference fixing the burst length before a data transfer by using a mode register did not disclose a "predetermined number" because it could be programmed. Ex-1013 at 24-25. This implied construction appears overly narrow, given that dependent claim 5 requires that "the fixed burst length is programmable." The ITC's construction limits the claims to programming at manufacture time, such as by bond options or voltage levels (*see* claims 6 and 7). However, the Board need not resolve this issue, as Petitioner relies on prior art disclosing "predetermined number" under the narrower interpretation adopted by the ITC (fixed or programmable at manufacture time using bond options or voltage levels). Ex-1002 ¶54.

H. "memory" (claims 1, 8-9, 14, 17)

In the *Cypress* District Court litigation, this term was construed to mean "addressable storage." Ex-1012 at 3, 8. Petitioner applies the prior art here consistent with that construction. Ex-1002 ¶55.

I. "address signal" (claims 1-4, 10-13, 16-17)

In the *Cypress* District Court litigation, this term was construed to mean "a signal for determining the address location in the memory array from which data is read to [*sic*] or to which data is written." Ex-1012 at 4, 8. Petitioner applies the prior art here consistent with that construction. Ex-1002 ¶56.

X. SPECIFIC EXPLANATION OF GROUNDS

A. Ground 1: Claims 1-3, 8, 12-13, 16, and 17 are anticipated by US 6,115,280 ("Wada")

1. Wada

Wada was filed April 4, 1997 and issued September 5, 2000, qualifying as prior art under at least pre-AIA 35 U.S.C. §102(e). Ex-1005 (Wada) at 1.

Wada is entitled "Semiconductor memory capable of burst operation." *Id.* at 1. Wada discloses numerous embodiments of "a semiconductor memory operating in burst mode" comprising "a semiconductor memory comprising a memory cell array, a plurality of output registers, an output register selecting circuit, a counter circuit, a data output pin, and an output data transfer circuit." *Id.* at 5:67, 6:14-17. "This makes it possible to output a plurality of target data items in burst mode

without interruption therebetween." *Id.* at 6:59-61.

Wada discloses "a typical conventional SRAM operating in burst mode." *Id.* at 1:22-23; Figs. 12-14. Figure 12 (annotated below) includes a "memory cell array 1" with a "plurality of memory cells" (yellow) (*id.* at 1:28-32), addressed by an internal address signal INT.ADD (orange). *Id.* at 2:58-61. The internal address signals are generated by a "burst counter unit 80" (green) that latches in an external address (EXT.ADD 100) (*id.* at 2:16-17) and increments the lower k bits in a burst counter (84) to generate the burst of internal addresses. *Id.* at 2:22-28. Other inputs to "burst counter unit 80" include clock signal CLK (91) and control signals ADV (93) and ADS (94). *Id.* at 1:65-67. "[W]hen the advance signal ADV is brought High, the address on the burst counter 84 is incremented ***every time a leading edge of the clock signal CLK is encountered***. As the internal address signal INT.ADD is incremented in this manner, the decoder selects different word lines 11 successively." *Id.* at 2:55-61.

FIG. 12 PRIOR ART

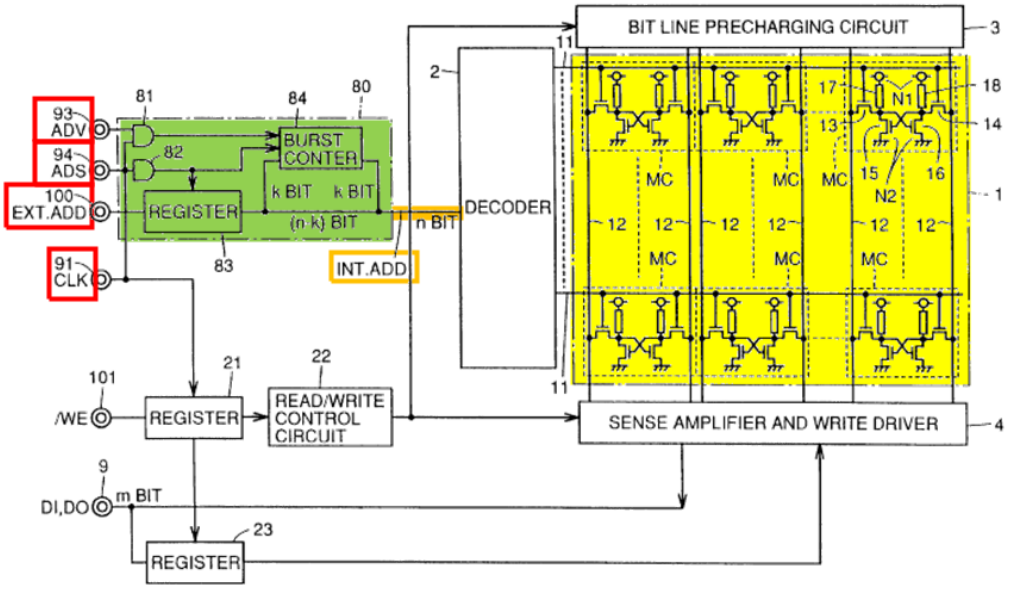


Figure 13 (below) is a timing diagram showing a burst read operation using the system of Wada's Figure 12. The external address An is latched when ADS goes high. Thereafter, "***every time*** the clock signal CLK is at a leading edge and the advance signal ADV is High, the address indicated by the internal address signal INT.ADD based on the address An given by the external address EXT.ADD ***is incremented by the burst counter*** 84." *Id.* at 3:5-9.

FIG. 13
PRIOR ART

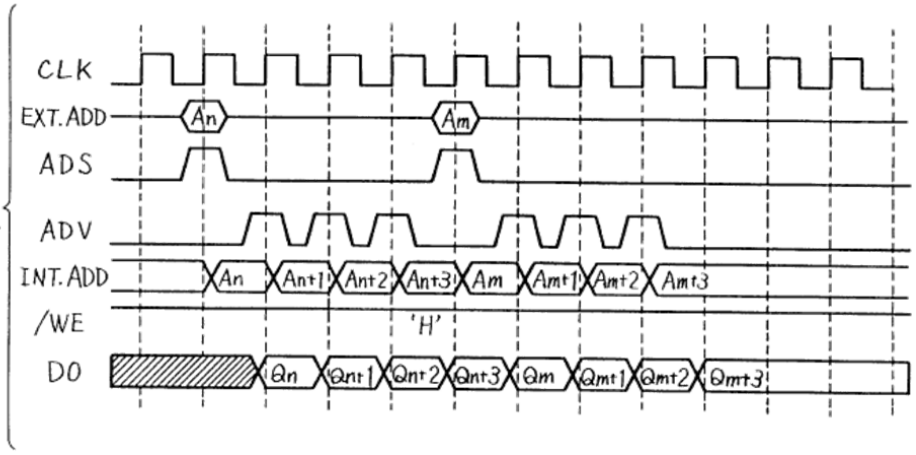
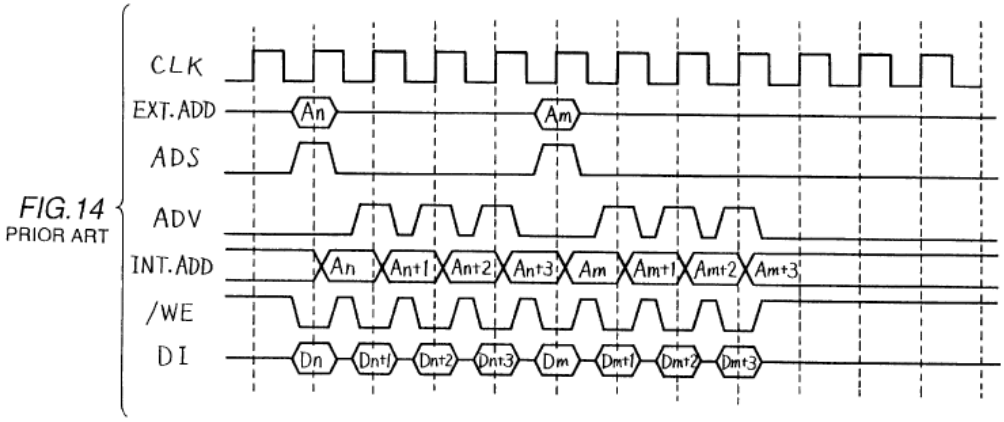


Figure 14 (below) depicts a burst write operation. "In the write operation, the internal address INT.ADD based on the address An designated by the external address signal EXT.ADD varies in the same manner as in the read operation." *Id.* at 3:27-30. Ex-1002 ¶¶57-61.



Wada discloses a "second embodiment of the invention and capable of operating in burst mode." Ex-1005 at 14:58-59; Figs. 3-4. Highlighted in yellow below, "[t]he memory cell array 1 has a plurality of memory cells . . . divided into a plurality (e.g., four) memory blocks M0 through M3. . . ." *Id.* at 3:48-50. (Note that like elements appearing in Figure 3 are described with respect to Figures 1 and/or 15. *Id.* at 12:32-35; 14:59-62.) External memory address MADD and external chunk address EXT.CHA are input to the circuit. *Id.* at 3:56-62; 4:14-16. Register 20 latches MADD to present internal address INT.ADD to a decoder, where it is used to simultaneously read data from memory blocks M0 through M3 at the addressed word line. *Id.* at 3:58-62; 4:1-5. External chunk address

EXT.CHA is presented to a burst counter 8 (green). "The burst counter unit 8 is identical in structure to the burst counter unit 80 in Figure 12, except that the external address EXT.ADD of Figure 12 is replaced by the external chunk address EXT.CHA." *Id.* at 4:17-21. The "burst counter unit 8 admits an address AC stemming from the external chunk address signal EXT.CHA." *Id.* at 4:60-62. Then, "the internal chunk address signal varies in the sequence of Ac, Ac+1, Ac+2, etc." *Id.* at 4:64-65. "Given the internal chunk address signal INT.CHA sent from the burst counter unit 8, the multiplexer 7 [orange] successively transfers to the data input/output pin 9 the data fed from the multiplexers 60a through 63a. This allows the data input/output pin 9 to output the data in burst mode." *Id.* at 15:66-16:3.

Thus, INT.ADD, latched from external memory address MADD, acts as the top n-2 bits of a memory address, transferring four modules worth of data to registers. The burst counter then increments external chunk address EXT.CHA from 0 to 4 at each CLK edge, providing the bottom 2 bits of the data address that pull the corresponding data from the registers by successively connecting each input of multiplexer 7 to its output. *Id.* at 14:54-16:55. The exemplary selection of four memory blocks (M0 - M3) and a four-input multiplexer (7) fix the burst length at four.

FIG.3

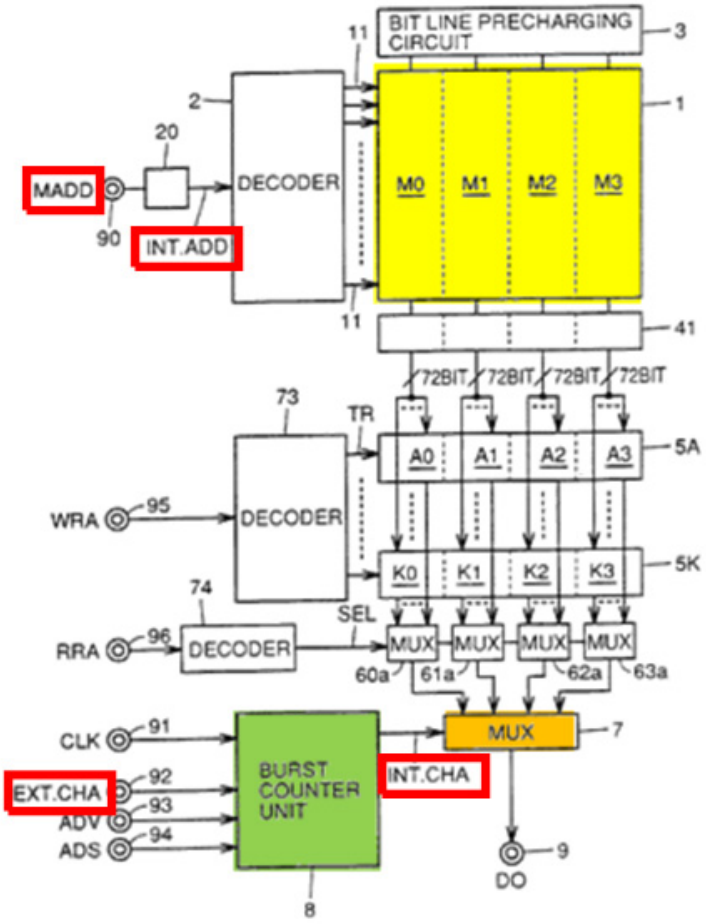
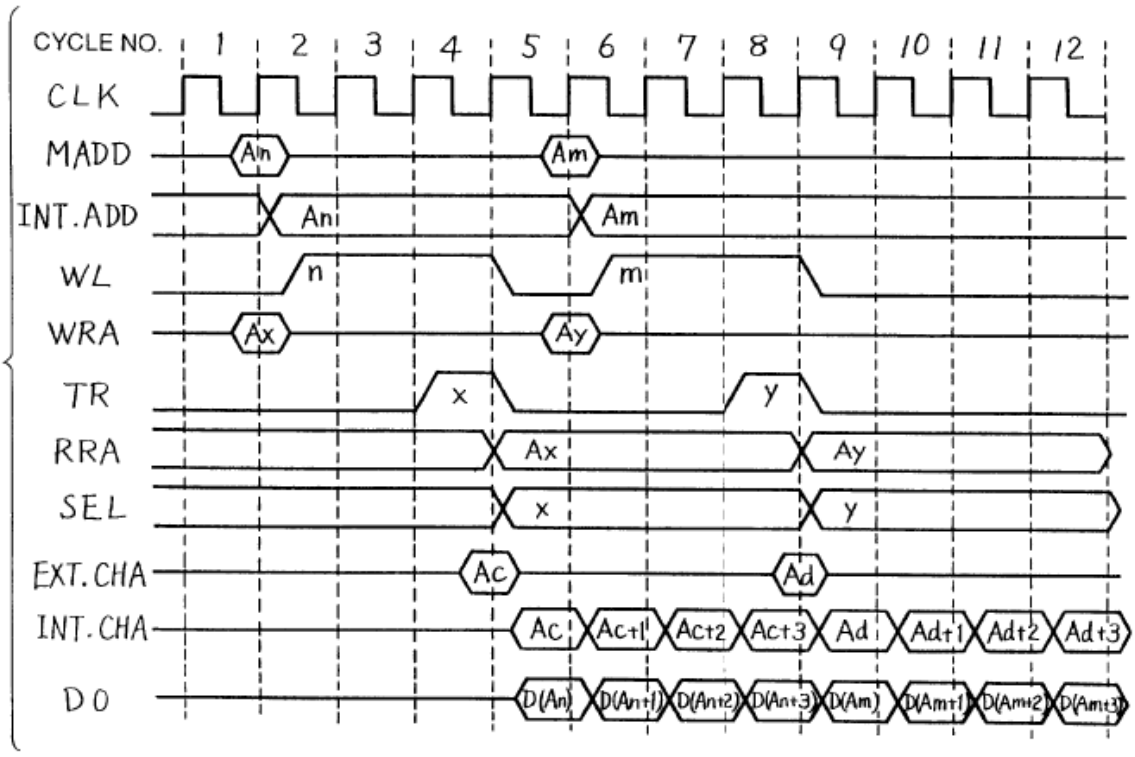


Figure 4 shows operation of embodiment 2. External address An is latched in from MADD and held as INT.ADD. External chunk address Ac is the incremented to form a burst of addresses on INT.CHA of Ac, Ac+1, Ac+2, and Ac+3. These addresses fetch data corresponding to offsets from the address An latched in from MADD, namely, D(An), D(An+1), D(An+2), and D(An+3). *Id.* ar Fig. 4 (Do line). This is repeated with the next address Am. "In response to these addresses, the above-described actions are carried out ***continuously***. This allows the data corresponding to the address Am to be ***output uninterrupted in burst***

mode." *Id.* at 16:7-10. "This constitution provides one advantage identical to that of the first embodiment, i.e., the ability to ***execute data burst output in uninterrupted fashion***." *Id.* at 16:14-15; Ex-1002 ¶¶62-64.

FIG.4



Wada discloses multiple embodiments, including two it calls "conventional" and an additional six it refers to as the first through sixth embodiments. Ex-1005 at 11:43-12:23. All of these embodiments are similar, and Petitioner discusses two of them in the analysis that follows: a "conventional" embodiment illustrated in Figures 12-14, and the "second embodiment" illustrated in Figures 3-4. However, Wada's other embodiments also anticipate or render obvious claims of the '134 Patent, and Petitioner reserves the right to rely on them. Ex-1002 ¶65.

2. Independent Claim 1

a. 1[pre]: A circuit comprising:

Conventional Embodiment: Wada discloses "Fig. 12 is a block diagram of the conventional SRAM capable of operating in burst mode." Ex-1005 at 12:10-11; Figs. 12-14.

Second Embodiment: Wada discloses "FIG. 3 is a block diagram of an SRAM practiced as a second embodiment of the invention and capable of operating in burst mode." *Id.* at 11:49-51; Figs. 3-4.

Wada's first, third through sixth, and second conventional embodiments all operate similarly to the second embodiment, have common structure described with reference to one another, and also disclose claim 1 of the '134 Patent. *See* Ex-1005 (Wada) at 3:37-5:64, Figs. 15-16 (second conventional embodiment); 12:49-14:52, Figs. 1-2 (first embodiment); 16:51-19:6, Figs. 5-6 (third embodiment); 19:7-34, Figs. 7-8 (fourth embodiment); 19:35-20:60, Figs. 9-10 (fifth embodiment); 20:61-21:38. Fig. 11 (sixth embodiment). Thus, Petitioner reserves the right to rely on those additional embodiments disclosed in Wada to the extent they operate similarly or provide additional insight into the operation of the embodiments discussed in detail herein. Ex-1002 ¶¶66-67.

b. 1[a]: a memory comprising a plurality of storage elements each configured to read and write data in response to an internal address signal; and

Conventional Embodiment: Wada discloses an SRAM comprising "a memory cell array" that is "addressable storage," as construed in the *Cypress* litigation, which is read from or written to in response to "internal address signal INT.ADD." Ex-1005 at 1:22-32. *See also* 3:5-15:

> Thereafter, every time the clock signal CLK is at a leading edge and the advance signal ADV is High, the address indicated by the internal address signal INT.ADD based on the address An given by the external address signal EXT.ADD is incremented by the burst counter 84. The incremented address occurs as An, An+1, An+2, etc. This causes a different word line 11 to be selected in each cycle of the clock signal CLK. As a result, the output data DO varies in the sequence of Qn, Qn+1, Qn+2, etc. This in turn allows data to be output in burst mode from memory cells MC, MC, etc. in the memory cell array 1.

See also id. at 3:26-28 ("In the write operation, the internal address INT.ADD based on the address An designated by the external address signal EXT.ADD varies in the same manner as in the read operation."). The address signals, as described above, determine the address location in the memory array from which data is read or to which data is written.

Second Embodiment: Wada discloses a memory array of addressable storage (Fig. 3, element 1) read from and written to using internal addresses INT.ADD and INT.CHA, created internal to the circuit:

> Given the internal chunk address signal INT.CHA sent from the burst counter unit 8, the multiplexer 7 successively transfers to the data

> input/output pin 9 the data fed from the multiplexers 60a through 63a. This allows the data input/output pin 9 to output the transferred data in burst mode.

Id. at 15:66-16:3. *See also id.* at 16:46-50 ("[C]ontrol is made possible by externally supplying the memory with the write register address signal WRA and the read register address signal RRA."); 17:9-24 (describing read/write control signal R/WRC). *See also id.* at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶69-70.

c. 1[b]: a logic circuit configured to generate a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control Signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

Conventional Embodiment: Wada's conventional embodiment discloses a circuit designed to perform logic operations (Fig. 12, circuit 80) configured to generate a predetermined number of internal address signals. The number of address signals is fixed at manufacture time by selecting the number of bits split off from the address. For example, Wada discloses a k-bit-wide portion of the address is split off and used by the burst counter (Fig. 12, element 84), which increments the k-bit subaddress that is tacked onto an (n-k)-bit MSB portion to create internal address INT.ADD. Thus, the predetermined number of internal

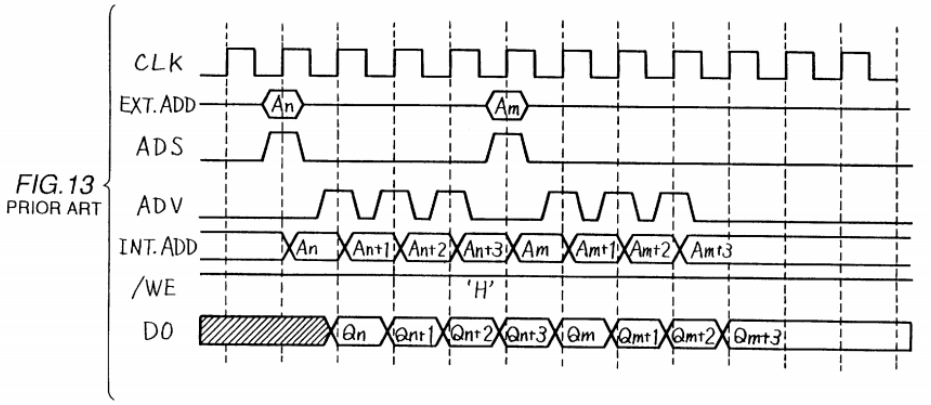
address signals is 2^k, and those internal address signals are generated within the circuit (80) by the burst counter (84). *See* Ex-1005 at 2:18-28:

> The n-bit address admitted into the register 83 is separated into a k-bit address and an (n-k)-bit address.
>
> The burst counter 84 is a binary counter that receives the output signals of the AND gates 81 and 82, and the k-bit address following the address separation. In operation, the burst counter 84 loads the k-bit address by responding to the output signal of the AND gate 82, and increments the value of the k-bit address in reply to the output signal of the AND gate 81.

The internal addresses are generated in response to an external address signal EXT.ADD (100), which originates outside of the circuit. *Id.* at 2:15-19; Fig. 12. They are also generated in response to a clock signal CLK (91). *Id.* at 1:64-65 ("An input pin 91 admits a clock signal CLK from the outside"); 2:57-60 ("the address on the burst counter 84 is incremented every time a leading edge of the clock signal CLK is encountered."). And they are also generated in response to one or more control signals. *Id.* at Fig. 12, *e.g.*, ADV (93), ADS(94); 2:56-61 ("when the advance signal ADV is brought High, the address on the burst counter 84 is incremented every time a leading edge of the clock signal CLK is encountered."); *see also* 3:21-36, 3:56-4:40.

The address burst is non-interruptible, or "cannot be stopped once initiated," as previously construed: "The conventional SRAM of the above constitution typically works as follows: when the advance signal ADV is brought High, the

address on the burst counter 84 is ***incremented every time a leading edge of the clock signal CLK is encountered***. As the internal address signal INT.ADD is incremented in this manner, the decoder 2 selects different word lines 11 ***successively***." *Id.* at 2:55-61. *See also id.* at Fig. 13 (continuous generation of INT.ADD values):

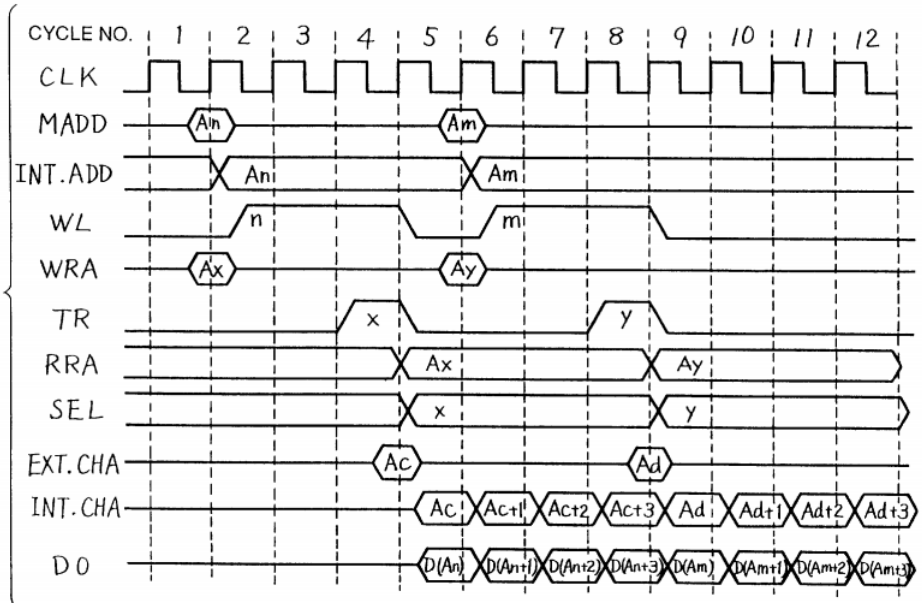


See also id. at 6:3-8 ("It is another object of the present invention to provide a semiconductor memory working in burst mode for a high-speed read operation irrespective of the operating speed of its memory cell array and ***without causing data output interruptions***."). Unlike the prior art considered during prosecution (*see* Section VII, above), Wada discloses no method of terminating a burst before it has completed. Ex-1002 ¶¶71-73.

Second Embodiment: Wada's second embodiment discloses a circuit designed to perform logic operations (Fig. 3, circuit 8) configured to generate a fixed number of internal address signals. Internal address "INT.CHA," generated by circuit 8 of Figure 3, selects one of four inputs of multiplexer 7 to sequentially

extract data from four stored memory locations. Thus, the burst length is fixed by the choice of a four-input multiplexer and the choice of dividing the memory into four blocks (M0-M3). Figure 4 show signal INT.CHA takes on four values, Ac through Ac+3, for the first external addresses An (arriving as signal MADD from outside the circuit) and Ac (arriving as signal EXT.CHA from outside the circuit), and then take on the four values Ad through Ad+3 for the next external address Am (MADD) and Ad (EXT.CHA):

FIG.4



The address burst is generated in response to external address signals MADD and EXT.CHA (which arrive from outside the circuit) and clock signal CLK. Ex-1005 at 15:37-40 ("Referring to FIG. 4, the address An designated by the memory address signal MADD is admitted into the internal register 20 at a first leading edge of the clock signal CLK in the second cycle."); 4:17-21 ("burst

counter unit 8 admits an address AC stemming from the external chunk address signal EXT.CHA."). It is also generated in response to one or more control signals. *Id.* at Fig. 3 (e.g., ADV(93), ADS(94), RRA(96), WRA(95), TR); 12:60-65 (TRA transfers data to/from output registers); 2:55-3:15 (ADV enables incrementing of burst counter); 1:64-2:13 (ADS address strobe latches in external address); 14:57-15:36 (RRA causes multiplexers to designate a register from which to read data; WRA causes multiplexer to designate registers to receive data.)

Wada discloses that the address burst is non-interruptible. *Id.* at 16:5-10:

> In the sixth cycle, the address Am designated by the memory address signal MADD and the address signal Ay designated by the write register address signal WRA are admitted. In response to these addresses, the above-described actions ***are carried out continuously***. This allows the data corresponding to the address Am to be o***utput uninterrupted in burst mode***.

See also id. at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶74-76.

3. Dependent Claim 2

a. 2: The circuit according to claim 1, wherein said predetermined number of internal address signals is determined by a fixed burst length.

In the 792 Investigation, the parties agreed that "burst" means "a number of words transferred as a group." In other words, burst length is the number of internal address signals generated in response to an external address. Ex-1002 ¶77.

Conventional Embodiment: Wada discloses a predetermined number of

internal address signals determined by a fixed burst length: For example, a k-bit-wide portion of the address is split off and used by the burst counter, which increments the k-bit subaddress that is tacked onto the (n-k)-bit MSB portion of the internal address. In other words, the predetermined number of internal address signals is 2^k, which is the limit of a k-bit counter, and the burst length. *See* Ex-1005 (Wada) at 2:18-28:

> The n-bit address admitted into the register 83 is separated into a k-bit address and an (n-k)-bit address.
>
> The burst counter 84 is a binary counter that receives the output signals of the AND gates 81 and 82, and the k-bit address following the address separation. In operation, the burst counter 84 loads the k-bit address by responding to the output signal of the AND gate 82, and increments the value of the k-bit address in reply to the output signal of the AND gate 81.

See also id. at 1:22-2:61, 3:5-15, 3:20-36; Ex-1002 ¶78.

Second Embodiment: Wada discloses a predetermined number of internal address signals set to four, which is a fixed value corresponding to the length of each burst. Ex-1005 (Wada) at 3:48-50. For example, in Figure 3, the "INT.CHA" internal address selects one of four inputs of MUX 7 to sequentially extract data from four stored memory locations corresponding to memory blocks M0 to M3. *Id.* at 15:66-16:3; *see also id.* at 14:57-15:29, 15:44-65, 16:4-50. Figure 4 shows INT.CHA takes on four values Ac through Ac+3 for a first burst and Ad through Ad+4 for a second burst. *See also id.* at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs.

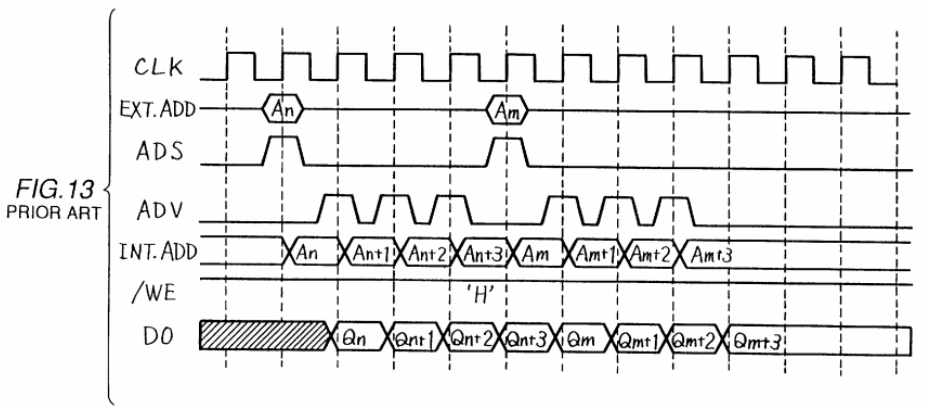
1-2, 5-10, 15-16; Ex-1002 ¶79.

4. Dependent Claim 3

a. 3: The circuit according to claim 1, wherein said predetermined number of internal address signals is at least 4.

Applying the ITC's prior construction, a "predetermined number of internal address signals" to mean "a fixed number of internal address signals for a burst access," Wada discloses claim 3.

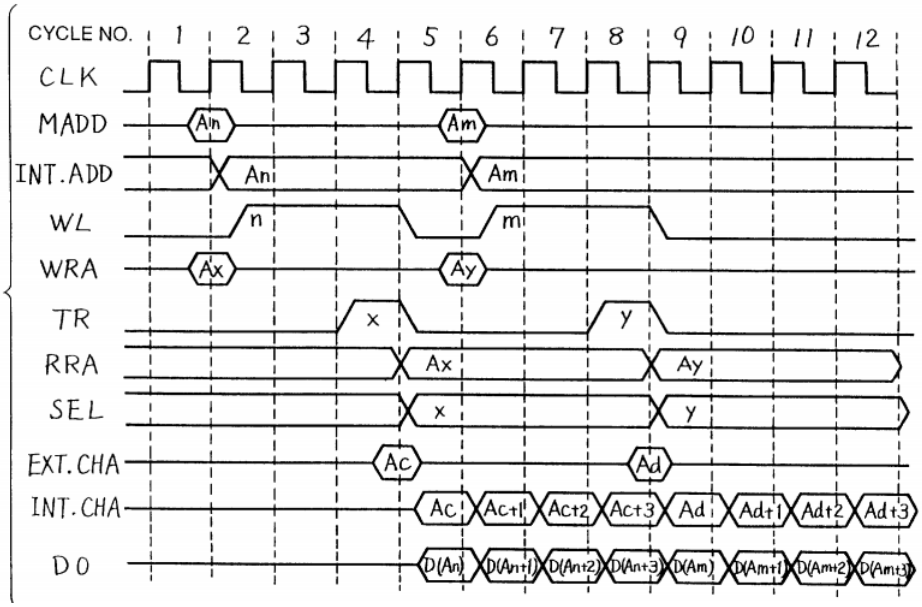
Conventional Embodiment: Wada illustrates generating a burst using k-bit counter 84 of Figure 12 (see claim 2 above), and the corresponding waveforms. Figure 13 shows that the burst length is set to 4 (*i.e.,* k=2). *Id.* at 2:16-28; 2:58-61. *See also id.* at 2:6-14, 2:29-65; 3:5-36. Figure 13 shows internal address signal INT.ADD takes on four values per burst: An to An+3:



Second Embodiment: Wada's "INT.CHA" internal address takes on four values to output data extracted from four memory blocks M0 to M3. *Id.* at 15:66-16:3; *see also id.* at 14:56-15:36, 15:44-65; Fig. 3 (M0-M3). Thus, the burst length

is set to four by configuring the memory as four blocks. Figure 4 shows INT.CHA takes on the values Ac through Ac+3 for a first burst and Ad through Ad+4 for a second burst. *Id.* at 4:64-65.

FIG.4



See also Wada's embodiments 1, 3-6, and second conventional embodiment, each of which use a fixed burst length of four. *Id.* at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶80-82.

5. Dependent Claim 8

a. 8: The circuit according to claim 1, wherein said memory comprises a static random access memory.

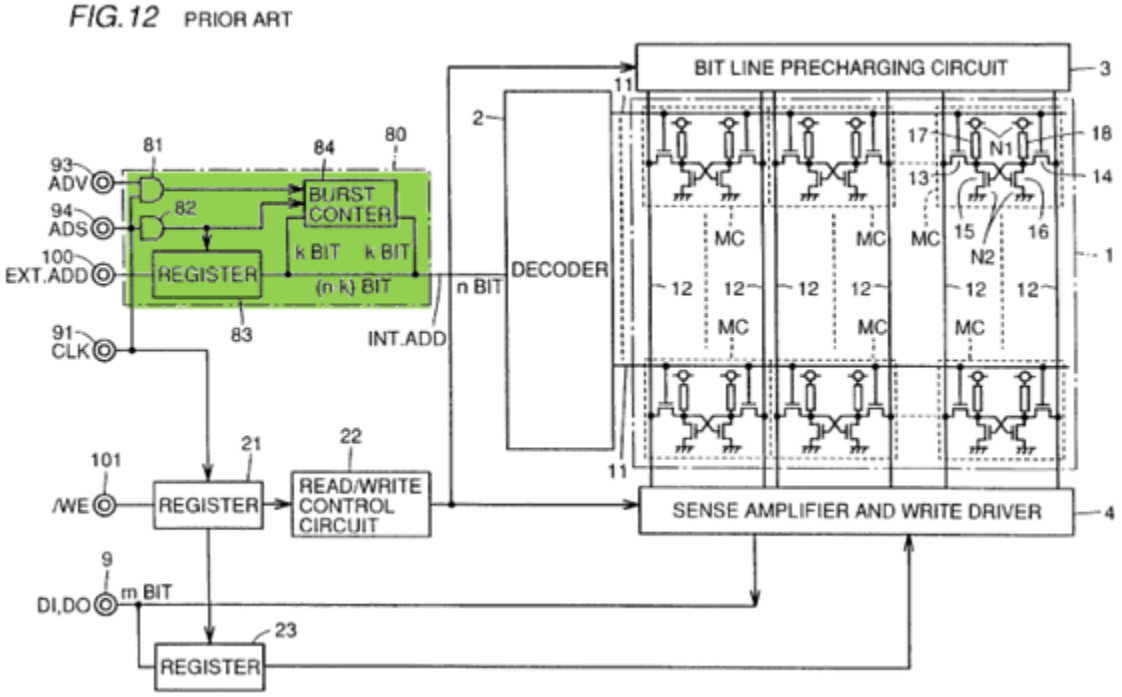
Conventional Embodiment: Wada discloses "FIG. 12 is a block diagram of a typical conventional ***SRAM*** capable of operating in burst mode." Ex-1005 at 1:22-23; 2:55-61; 12:10-11.

Second Embodiment: Wada discloses "FIG. 3 is a block diagram of an ***SRAM*** practiced as a Second embodiment of the invention and capable of operating in burst mode." *Id.* at 11:49-51. Wada further discloses "FIG. 3 is a block diagram of an ***SRAM*** practiced as the Second embodiment of the invention and capable of operating in burst mode." *Id.* at 14:57-59. *See also* Wada's embodiments 1, 3-6, and second conventional embodiment, each of which uses SRAM. *Id*. at 11:41-12:22; 12:29-39, 14:5-11, 14:28-34, 14:57-67, 16:11-15, 16:56-63, 17:48-51, 18:53-63, 19:36-40, 19:52-55, 20:37-21:11, 21:33-38; Ex-1002 ¶¶83-84.

6. Dependent Claim 12

a. 12: The circuit according to claim 1, wherein said logic circuit comprises a counter configured to generate said predetermined number of internal address signals.

Conventional Embodiment: Wada discloses a k-bit burst counter that generates the predetermined number of internal address signals. *See, e.g.,* Ex-1005 at Fig. 12 (elements 80, 84) (green):



See also id. at 2:55-62 ("The conventional SRAM of the above constitution typically works as follows: when the advance signal ADV is brought High, the address on the burst counter 84 is incremented every time a leading edge of the clock Signal CLK is encountered. As the internal address signal INT.ADD is incremented in this manner, the decoder 2 selects different word lines 11 successively."); *see also id.* at 1:22-2:54; 4:17-28.

Second Embodiment: Wada discloses a burst counter in Figure 3 (element 8) that generates four internal address signals. *Id.* at 1:22-2:62; 4:17-23 ("The burst counter unit 8 is identical in structure to the burst counter unit 80 in FIG. 12, except that the external address signal EXT.ADD of FIG. 12 is replaced by the external chunk address signal EXT.CHA."). *See also id.* at 3:37-5:64, 12:49-

14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶85-86.

7. Dependent Claim 13

a. 13: The circuit according to claim 1, wherein said external address signal comprises an initial address for data transfers to and from said memory.

Conventional Embodiment: External address EXT.ADD is latched into register 83, as shown in the excerpt of Figure 12 below. Ex-1005 at 2:16-17. The bottom k bits of the EXT.ADD are incremented in burst counter 84 and concatenated with the upper (n-k) bits to form internal address INT.ADD. *Id.* at 2:22-28, 2:58-61. Thus, the initial address carried on INT.ADD is the external address.

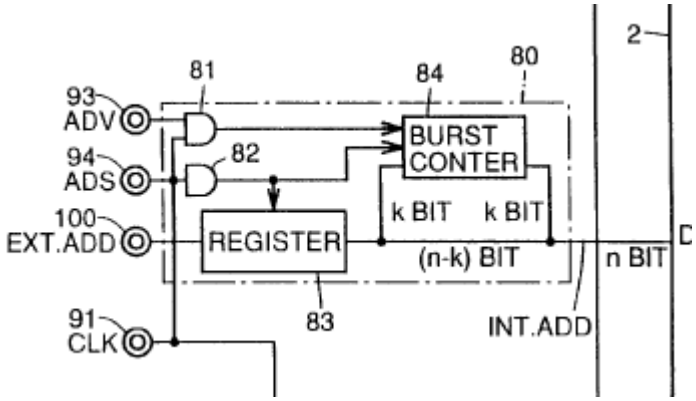


Figure 14 shows initial EXT.ADD address An is also the first value of INT.ADD (compare shaded elements below). *Id.* at 2:58-61.

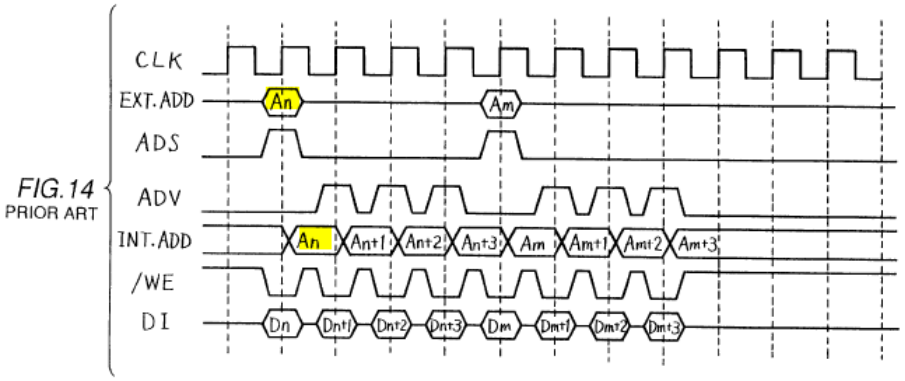
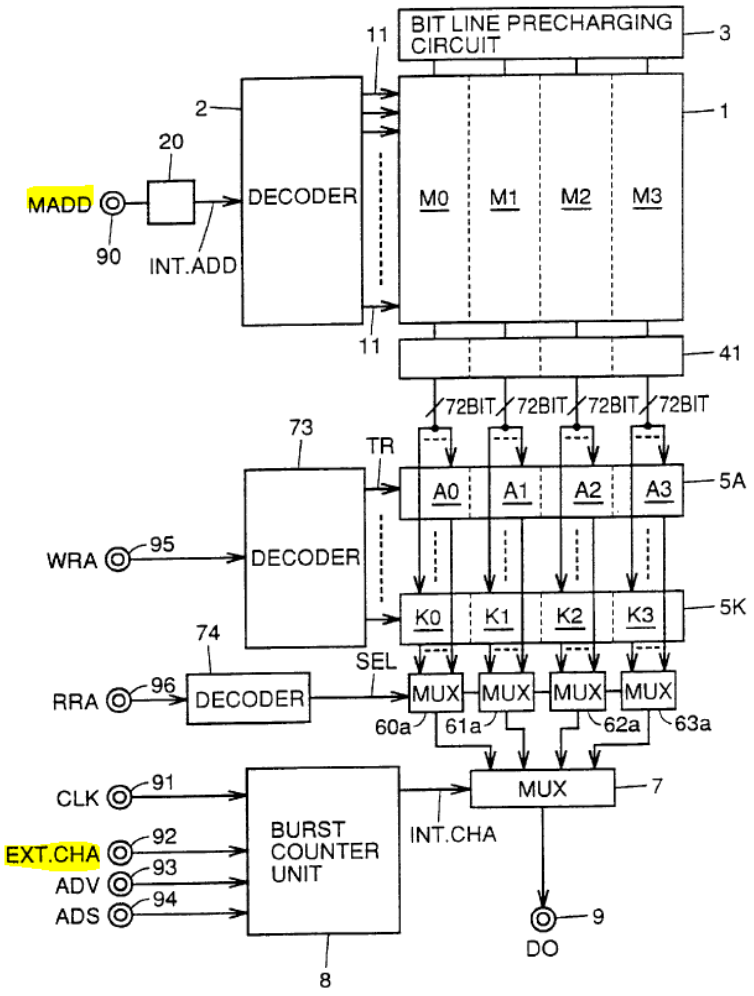


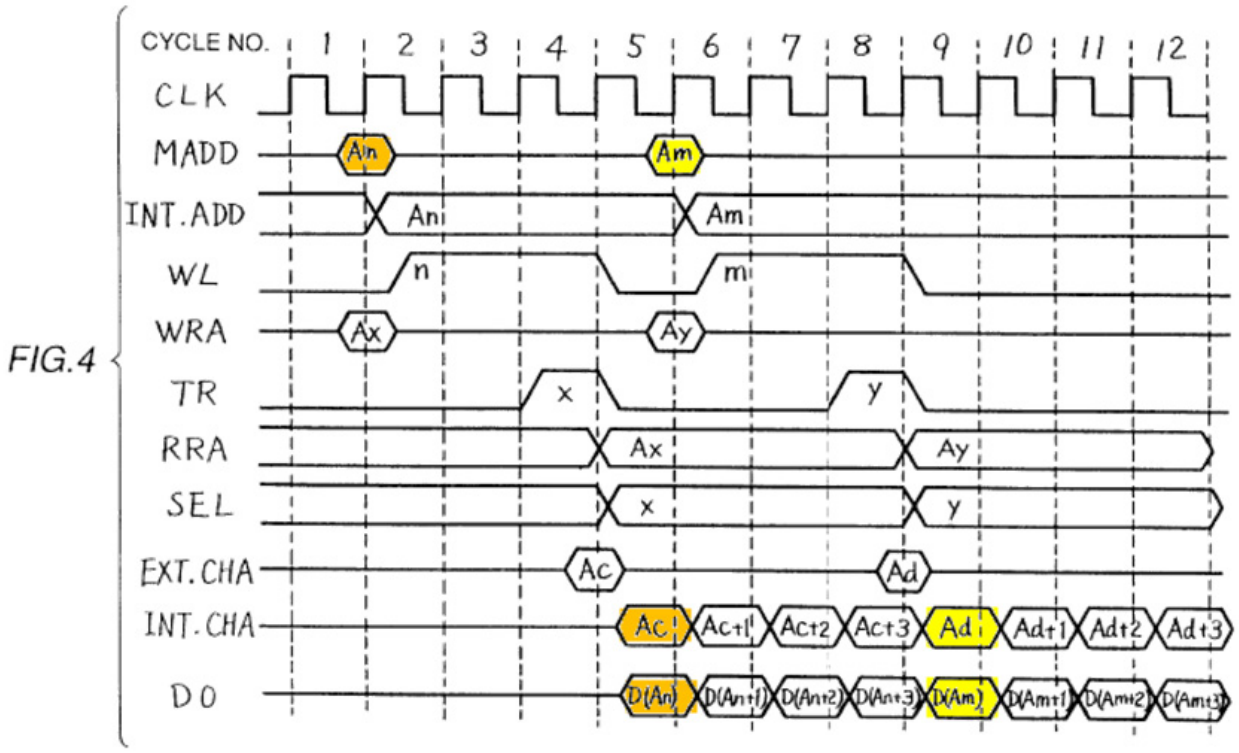
FIG.14
PRIOR ART

Second Embodiment: Figure 3 shows external address MADD and external chunk address EXT.CHA used to initiate the burst data transfer, as highlighted below.

FIG.3



When MADD is Am, for example, "the data corresponding to the address Am [is] output uninterrupted in burst mode." *Id.* at 16:43-10. Figure 4, annotated below, shows external address MADD set to An, and the initial value of the internal address set to select data corresponding to address An, *i.e.,* D(An). *Id.* at 3:56-62; 4:14-16. Similarly, when MADD is Am, the initial internal address selects data corresponding to address Am, *i.e.*, D(Am). *Id.*



See also id. at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶87-91.

8. Independent Claim 16

a. 16[pre]: A circuit comprising:

See claim 1[pre] above.

b. 16[a]: means for reading data from and writing data to a plurality of storage elements in response to a plurality of internal address signals; and

Wada discloses this means-plus-function element. As discussed above with respect to claim construction, the corresponding structure in the ’134 Patent is shown in Figure 1, highlighted below:

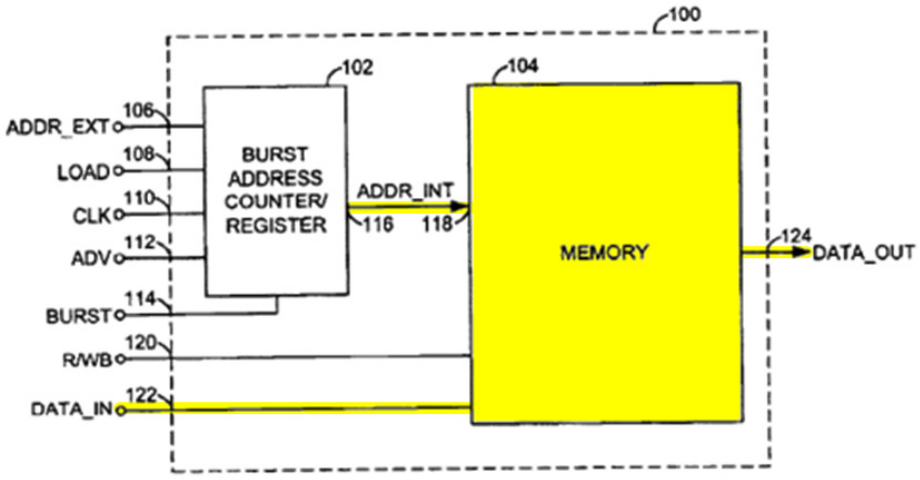
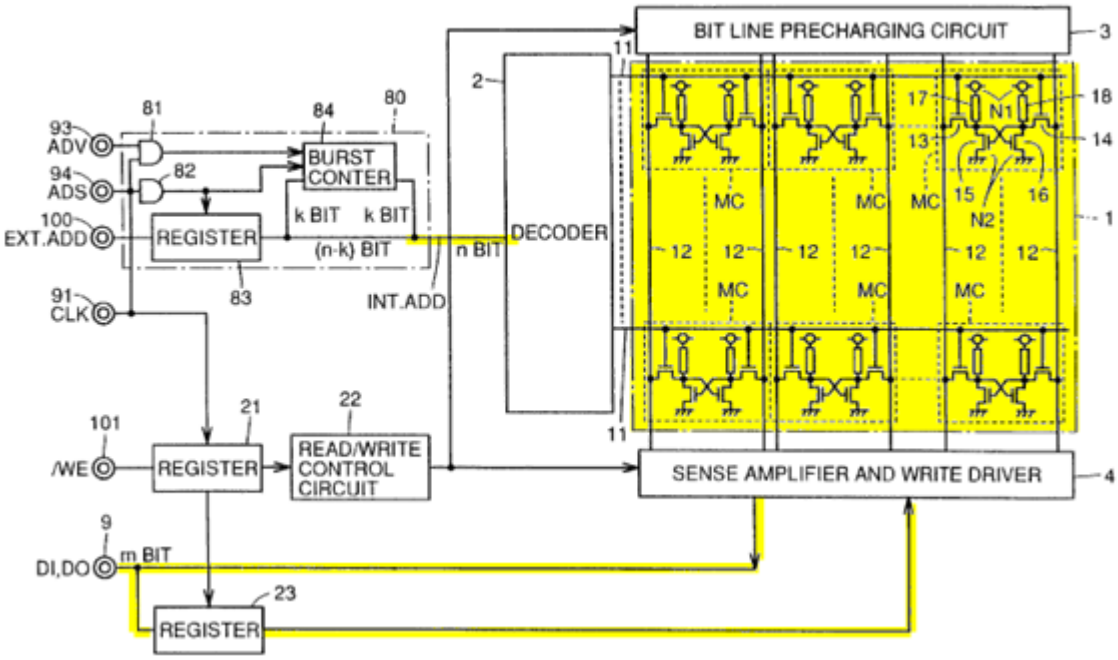


FIG. 1

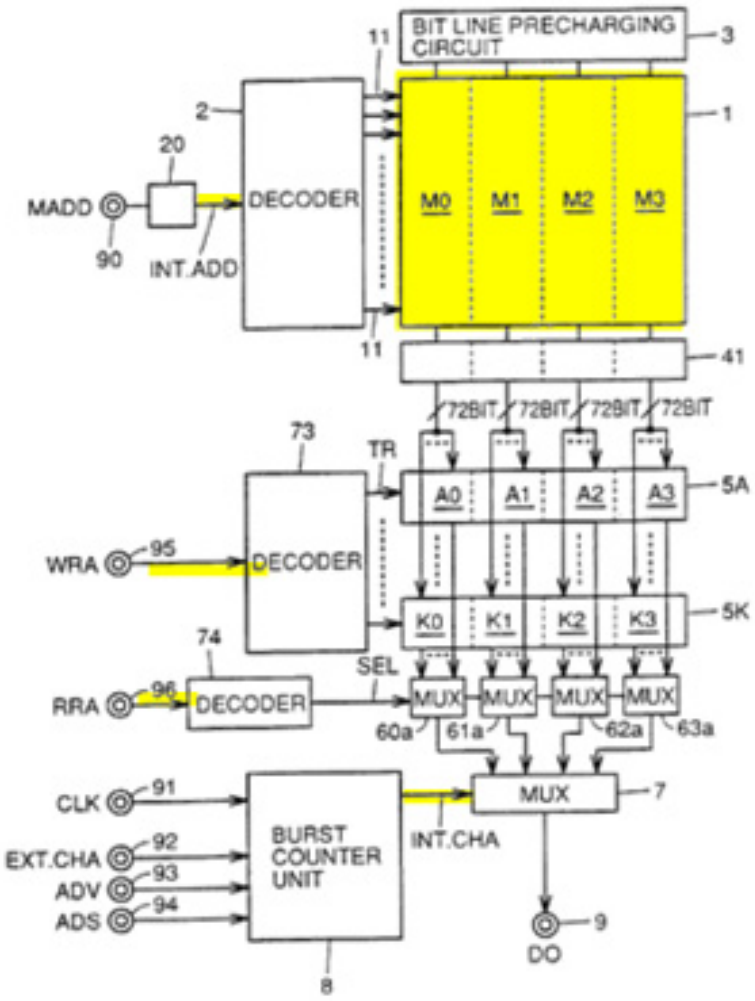
Wada Conventional Embodiment: In Figure 12, highlighted below, Wada discloses a plurality of storage elements (1) from which data can be read and to which data can be written (DI, DO lines), in response to an internal address INT.ADD. *Id.* at 1:28-32; 2:58-61. The operation of these structures is mapped to the recited function in the discussion of claim element 1[a] above.

FIG. 12 PRIOR ART



Wada Second Embodiment: In Figure 3, highlighted below, Wada discloses a plurality of storage elements (1) from which data can be read and to which data can be written (WRA, RRA control lines, "data ***input/output*** pin 9"). *Id.* at 15:66-16:2, 15:7-9, 15:15-16. The operation of these structures is mapped to the recited function in the discussion of claim element 1[a] above.

FIG.3



See also Wada's embodiments 1, 3-6 and conventional embodiment 2, *id.* at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16; Ex-1002 ¶¶92-95.

c. 16[b]: means for generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) one or more control signals, wherein said generation of said predetermined number of internal address signals is non-interruptible.

Wada discloses this means-plus-function element. As discussed above with respect to claim construction, the corresponding structure in the '134 Patent is

either (1) the structure shown in Figure 2, or (2) the structure shown in Figure 3, highlighted below:

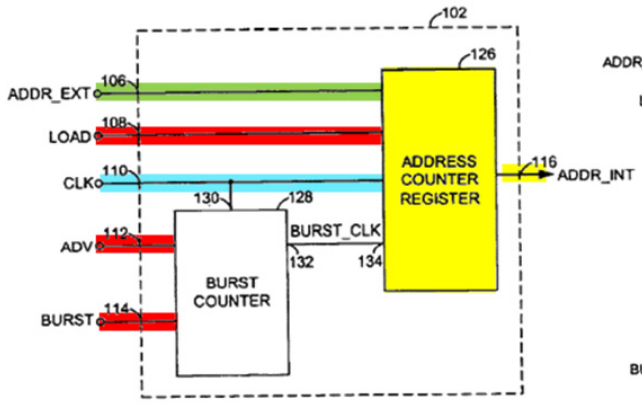


FIG. 2

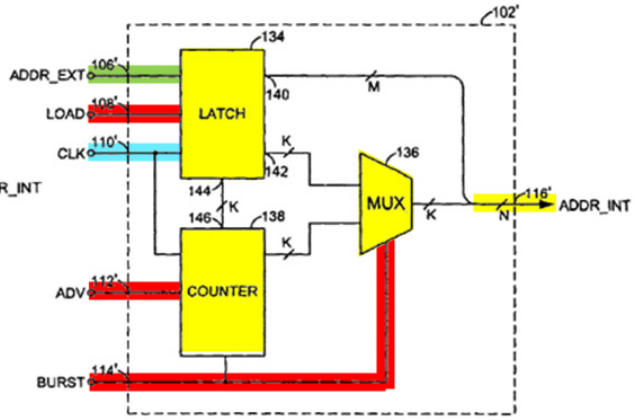


FIG. 3

Wada Conventional Embodiment: Figure 12, excerpted below, shows the same structure shown in '134 Patent Figure 2. The control signal ADV (93) is logically ANDed with the CLK signal (91) to enable incrementing the address value EXT.ADD that is latched into register 83 by the ADS control signal. Ex-1005 at 1:64-2:28. Burst counter 84 increments the address in response to the CLK edges to produce output internal address signal INT.ADD. *Id.* at 2:29-61. This structure is identical to the '134 Patent's CLK / ADV signals that are combined into a BURST_CLK signal that increments the address latched into the counter on the LOAD signal.

This structure performs the recited function, as described in detail above with respect to claim element 1[b].

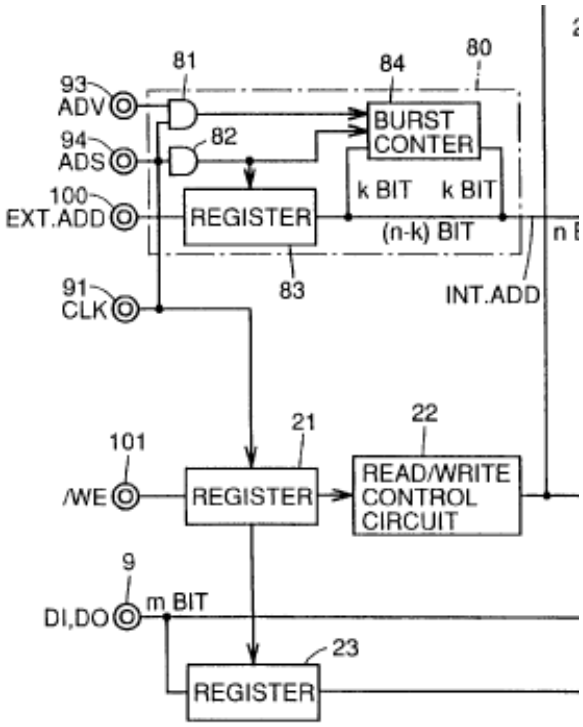


Fig. 12 (excerpt)

Wada Second Embodiment: Wada's Figure 3, below, shows the equivalent structure of '134 Patent Figure 3. While Figure 3 of the '134 Patent uses a multiplexer to reassemble the lower bits of internal address before addressing the memory array, Wada's Figure 3 addresses four memory blocks and then uses the multiplexer to select which of the four words is indicated by the lower address bits. Thus Wada uses the same structural elements in an equivalent manner to perform the same function.

In Wada, the most significant bits of the external address are latched in by latch 20 and used to simultaneously address four memory modules M0 to M3. *Id.* at 15:66-16:3. The lowest significant bits enter the burst counter unit 8 as the

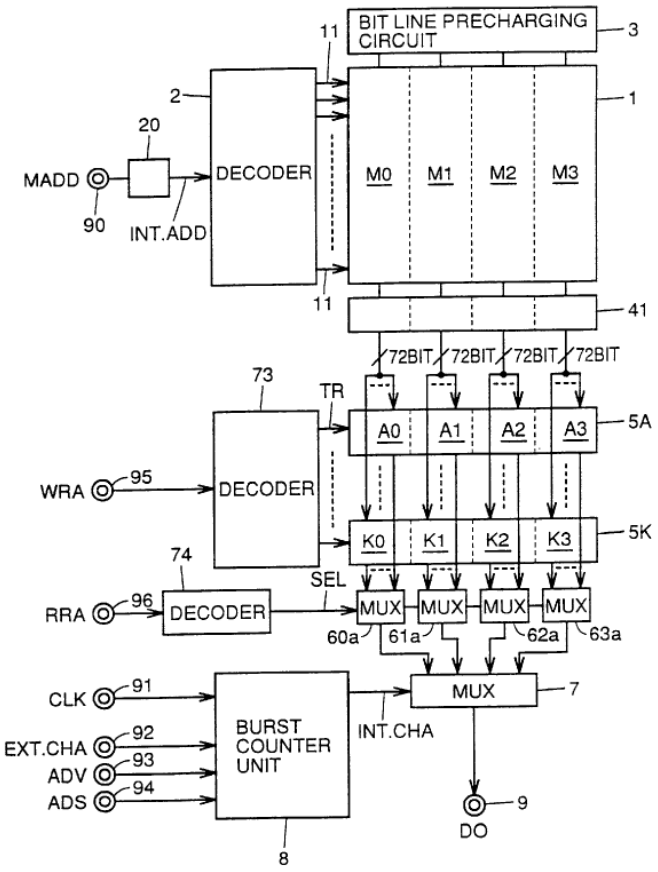
chunk address EXT.CHA and are incremented to address a MUX that successively pulls data from locations having the same base address MADD (INT.ADD). *Id.* at 4:60-65.

This structure is equivalent to Figure 3 of the '134 Patent. There, the M most significant bits of the ADDR_EXT are latched into latch 134. The k least significant bits are input to a counter 138, and MUX 136 is switched from the base address (k bits from 142) to the incremented address (k bits from 138) to address the memory.

Although Wada pulls four blocks of data from memory using the MADD address and then uses a MUX to select between those blocks, while the '134 Patent uses the MUX to separately address the memory, the structure is equivalent because it achieves substantially the same result in substantially the same way, *i.e.,* by separating the address into parts, incrementing the lower address bits, and using a multiplexer to select the data corresponding to the full internal address.

The structure of Wada's Figure 3 performs the recited function as described above in detail with respect to claim 1[c].

FIG.3



See also id. at 3:37-5:64, 12:49-14:52, 16:51-21:38; Figs. 1-2, 5-10, 15-16. Thus, Wada anticipates claim 16 for the reasons described above and with respect to claim 1. Ex-1002 ¶¶96-102.

9. Independent Claim 17

a. 17[pre]: A method of providing a fixed burst length data transfer comprising the steps of:

See discussion of claim element 1[pre] and claim 2, above, in Sections X.A.2.a and X.A.3.

b. 17[a]: accessing a memory in response to a plurality of internal address signals; and

See discussion of claim element 1[a], above, in Section X.A.2.b.

c. 17[b]: generating a predetermined number of said internal address signals in response to (i) an external address signal, (ii) a clock signal and (iii) a control signal, wherein said generation of said predetermined number of internal address signals is non-interruptible.

See discussion of claim element 1[b], above, in Section X.A.2.c. Ex-1002 ¶¶103-05.

B. Ground 2: Claims 1-4, 8, 12-14, 16, and 17 are obvious over Wada in view of the knowledge of a POSITA

1. Independent Claims 1 and 16

Unlike the prior art distinguished during prosecution, Wada discloses no method of interrupting an address burst once it has been initiated. But to the extent Patent Owner argues Wada's control signals might be manipulated to terminate a burst (even though there is no such teaching), it would have been obvious to a POSITA not to do so and to keep the generation of internal address signals non-interruptible, because Wada teaches against interrupting a burst: "it is another object of the present invention to provide a semiconductor memory working in burst mode for a high speed read operation irrespective of the operating speed of its memory cell array and ***without causing data output interruptions***." Ex-1005 (Wada) at 6:3-8. Thus, Wada renders claims 1 and 16 obvious. Ex-1002 ¶106.

2. Dependent Claims 2-3, 8, 12-13, and 17

Dependent Claims 2-3, 8, 12-13, and 17 are rendered obvious by Wada in light of the discussion of claims 1 and 16 above, and the discussion in Section X.A above. Ex-1002 ¶107.

3. Dependent Claim 4

a. 4: The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

Wada discloses claim 1 in exemplary embodiments having a fixed burst length of four. Section X.A.4; Ex-1005 (Wada) at 3:48-51 ("memory cell array 1 has a plurality of memory cells . . . divided into a plurality (***e.g., four***) memory blocks M0 through M3."). When Wada was filed, it was well known in the prior art that memory systems commonly employed burst lengths of 2, 4, or 8. *See, e.g.,* Ex-1008 (Reeves) at 2:15-17 ("Conventional SDRAMs can be programmed to read or write a burst of one, two, four, eight, or more bits."); Ex-1006 (Fujioka) at 15:7-8 ("the FCRAM with the burst length fixed to 4 or 8 can be obtained."); Ex-1014 (Ryan) at 6:4-6 ("Burst length options of 2, 4, 8 and full page… may be provided."). Because a longer burst transfers more data for a given read or write command, a POSITA would have been motivated to modify the exemplary embodiments of Wada to set a burst length of eight to further Wada's stated goal "to provide a semiconductor memory operating in burst at a sufficiently high speed

irrespective of the operating speed of its memory cell array." *Id.* at 5:66-6:2; Ex-1002 ¶108.

As discussed in Section A.3.a, the first conventional embodiment of Wada sets a burst length of 2^k. *See* Ex-1005 (Wada) at 2:18-28. Thus, choosing k to be three would set the burst length to eight. Ex-1002 ¶108. Wada's Second embodiment could be modified to a burst length of eight by dividing the memory cells into eight banks (M0-M7) instead of four and selecting an 8-input, rather than 4-input, multiplexer. *See* Ex-1005 (Wada) at 3:48-55; 15:66-16:3; Ex-1002 ¶108. Thus Wada renders claim 4 obvious.

4. Dependent Claim 14

a. 14: A memory device according to claim 1, wherein said circuit is an integrated circuit.

Wada discloses a "semiconductor memory capable of operating in burst mode." Ex-1005 at 1:9-10. Wada further states "This eliminates the need for the memory to use illustratively the so-called ***bipolar CMOS LSI technology***, an expensive process technique for enhancing the operation speed of the memory cell array 1. As a result, the invention allows semiconductor memories adopting ***low-cost process techniques*** to perform high-speed read operations." *Id.* at 14:47-53. One of ordinary skill would have understood these process technologies relate to integrated circuits. Ex. 1002 ¶110. Thus, Wada renders claim 14 obvious.

To the extent necessary, Wada and Reeves renders this claim obvious, as

discussed below in Ground 4.

C. Ground 2a: Claims 1-4, 8, 12-14, 16, and 17 are rendered obvious by the combination of Wada and US 5,584,033 ("Barrett") in view of the knowledge of a POSITA

1. Barrett

Barrett was filed November 7, 1994 and issued December 10, 1996, qualifying as prior art under at least pre-AIA 35 U.S.C. §102(b). Ex-1010 (Barrett) at 1.

Barrett is entitled "Apparatus and Method for Burst Data Transfer Employing a Pause At Fixed Data Intervals" and discloses a "plurality of devices attached to a communication bus observe a burst transfer protocol which allows pausing only at pre-determined, fixed intervals of n data words, where a word is the width of the bus." *Id.* at Abstract. Further, "system 100 may comprise multiple CPUs and ***memory units*** communicating with other units via system I/O bus 101." *Id.* at 4:46-48. Accordingly, "once burst transfer is initialized the sending device ***transmits an uninterrupted stream*** of n data words over the communications bus . . . ." *Id.* at Abstract. Indeed, "[t]he essential feature of burst communication is that the data transfer takes place at high speed and ***without interruption***." *Id.* at 1:64-66.

Barrett's system operates as follows:

> In the data transfer phase, the sender transmits 32 words of data in successive cycles, ***without interruption***, at step 404. Each word is the

> amount of data the bus can support in a single cycle, i.e. the number of parallel data lines in the bus.

Id. at 6:8-15. Furthermore, Barrett discloses:

> In the preferred embodiment, the number of words in transferred in an ***uninterrupted stream*** before any pause can take place is fixed for a particular hardware and software release of computer system 100. In an alternative embodiment, it would be possible to dynamically vary the predetermined length n of the ***uninterrupted data stream*** from time to time.

Id. at 9:17-24. Barrett claims a system including "means for initializing a burst data transmission comprised of a plurality of ***uninterruptible streams of n data transfer cycles***, where n is a predetermined integer greater than one . . . ." *Id.* at claim 1. *See also id.* at claims 2, 8, 13, 19, 24, and 27 (reciting "uninterruptible streams" or "uninterrupted streams"). Ex. 1002 ¶¶110-14.

a. Motivation to combine Wada and Barrett

As discussed above, Wada discloses that the generation of the predetermined number of internal address signals is non-interruptible. However, to the extent Patent Owner argues Wada's control signals could be manipulated (in some undisclosed manner) to terminate a burst data transfer, Wada could be combined with Barrett.

One of ordinary skill would have been motivated to combine Wada and Barrett because both are directed to achieving the same purpose. Wada discloses that "[i]t is another object of the present invention to provide a semiconductor

memory working in burst mode for a ***high speed read*** operation irrespective of the operating speed of its memory cell array and ***without causing data output interruptions***." Ex-1005 (Wada at 6:3-7). And Wada's invention is directed to making it "possible to output a plurality of target data items in burst mode ***without interruption*** therebetween." *Id.* at 7:65-67. Specifically, Wada discloses "the data corresponding to the address Am [can] be ***output uninterrupted in burst mode***." *Id.* at 16:5-10. And Wada notes that uninterrupted data transmission is an advantage: "This constitution provides one advantage identical to that of the first embodiment, i.e., the ability to ***execute data burst output in uninterrupted fashion***." *Id.* at 16:12-15. Ex. 1002 ¶¶115-16.

Similarly, Barrett claims "a burst data transmission comprised of a plurality of ***uninterruptible*** streams of n data transfer cycles." Ex-1010 (Barrett) at claim 1. Barret further states, "In effect, allowing a pause at any point ***defeats the purpose of burst transmission***, which is to send data as rapidly as possible in ***an uninterrupted stream***." *Id.* at 2:39-41. A POSITA would realize that applying Barrett's teachings to Wada to render bursts uninterruptible would result in improved transmission efficiency by minimizing overhead associated with terminating and initiating packets. *See id.* at 2:20-22, 3:44-50; Ex. 1002 ¶117. Thus, to the extent Wada's disclosure leaves open any possibility that a burst data transmission could be interrupted, one of ordinary skill would have been motivated

to apply the teachings of Barrett to achieve an ***uninterruptible*** data transmission stream.

2. Claims 1-4, 8, 12-14, 16, and 17

The combination of Wada and Barrett, ensuring that the generation of internal address signals cannot be interrupted once initiated, can be applied to render claims 1-4, 8, 12-14, 16, and 17 obvious for the same reasons discussed above with respect to Grounds 1 and 2. Ex. 1002 ¶118.

D. Ground 3: Claims 4-7, and 18-20 are rendered obvious by the combination of Wada and U.S. 6,185,149 ("Fujioka") in view of the knowledge of a POSITA.

1. Fujioka

Fujioka is directed to "semiconductor integrated circuit memories" (Ex. 1006 at 1:6-7) read in burst mode without interruption: "when the burst length is equal to 4, the 4-bit parallel data read from the sense amplifiers are converted into serial data, so that data can be consecutively read and output without any interruption. *Id.* at 8:1-4. Fujioka notes "Recently, semiconductor memory devices such as DRAM (Dynamic Random Access Memory) devices have been required to input and output data at higher frequencies in accordance with speeding up of CPUs so that the data transmission rate can be increased." *Id.* at 1:10-15. And, "as the number of bits of data to be simultaneously read in parallel increases, the burst length increases." *Id.* at 3:65-67. To increase the data throughput,

Fujioka discloses that multiple memory cell blocks can be activated to transfer data in longer bursts:

> As described above, a plurality of memory cell blocks (banks) can be selectively activated in response to one read command. Hence, it is possible to select the memory cell blocks based on the burst length BL. When the burst length BL is equal to 8, two memory cell blocks (the memory cell block 12a of the bank-0 circuit 7 and the memory cell block 12a of the bank-1 circuit 8) are selectively activated…

Id. at 9:49-59. The burst length can be programmed late in the manufacturing process by using laser-cut fuses to tie circuits to Vcc or ground or by using bond options:

> FIG. 10A shows a method which uses a circuit such as an inverter, which is connected to a 30 power supply VCC via a fuse. The input of the circuit is coupled to another power supply VSS such as ground via a high resistor. The output of the circuit forms the burst length information b18. The burst length BL is set during the fabrication process.

Id. at 14:52-57; Figs 10A, 10D:

FIG. 10A

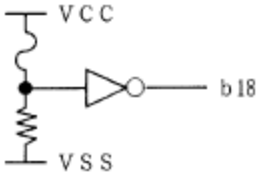


FIG. 10D

FUSE	b18	BURST LENGTH
NOT CUT	L	4
CUT	H	8

> FIG. 10B shows a method which employs a circuit such as an inverter associated with a VCC pad and a VSS pad. As shown in FIG. 10E, when the burst length BL is set equal to 4, the input terminal of the inverter is connected to the VCC pad by wire bonding a. When the burst length is set equal to 8, the input terminal of the inverter is connected to the VSS pad by bonding wire b. Hence, the FCRAM with the burst length fixed to 4 or 8 can be obtained. It is possible to set an increased

number of lengths equal to, for example, 4, 8, 16 and 32.

Id. at 15:1-10; Figs. 10B, 10E:

FIG. 10B

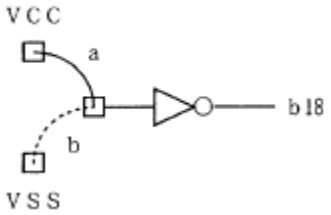


FIG. 10E

BONDING	b18	BURST LENGTH
a	L	4
b	H	8

a. Motivation to combine Wada and Fujioka

Wada is directed to improving speed and data throughput in a memory system. *See, e.g.*, Ex-1005 (Wada) at 5:66-6:2 ("It is therefore an object of the present invention to provide a semiconductor memory operating in burst at a sufficiently high speed irrespective of the operating speed of its memory cell array."). Fujioka discloses increasing data throughput by increasing the burst length. Ex-1006 at 3:65-67. Fujioka discloses that the burst length can be increased from 4 to 8 by increasing the number of memory cell blocks (banks) that are activated during each read command. *Id.* at 9:49-59. Thus, a POSITA would understand that the higher throughput suggested by Fujioka could be achieved by increasing the number of Wada's memory blocks from four to eight (or higher) to increase the burst length. Ex. 1002 ¶¶119-20. And, following Fujioka, one could enhance the flexibility by activating those additional blocks by programming the burst length late in manufacturing by bond options or by making selective connections to voltage levels. Ex-1006 (Fujioka) at 14:50-15:24; Figs. 10A-10E.

Programming burst length at manufacturing time satisfies the "predetermined number of said internal address signals" recited in claim 1, even under the Commission's narrow interpretation of "predetermined" in the 792 Investigation. Ex. 1002 ¶120.

Moreover, during prosecution, the applicant overcame a Section 112 rejection regarding programming burst length using bond options by arguing:

> [B]ond options are well known in the art and, therefore, one skilled in the art would have understood how to make and/or use bond options. Copies of U.S. patents 6,188,636 (issued February 13, 2001), 5,900,021 (issued May 4, 1999) and 5,360,992 (issued November 1, 1994) from the USPTO web site (www.uspto.gov) are attached as evidence of bond options being well known in the art."

Ex-1004 ('134 File History) at 42; *see also* Section VII, above. U.S. 5,900,021 ("Tiede"), cited by the applicant, states "Bond options are an increasingly important feature in many modern semiconductor devices, especially memory devices." Ex-1007 (Tiede) at 3:29-31. Further, "[u]sing bond options configuration, a mode select signal can be permanently provided to the IC by selectively bonding mode configuration pads to ground or power busses." *Id.* at 3:17-20. And U.S. 5,360,992 ("Lowrey"), also cited by the applicant, further explains that "any of the bond options can be connected with any of the pinouts," (Ex-1014 (Lowrey) at 3:16-18), allowing "pinouts and bond options to be selected late in the manufacturing process." *Id.* at 7:5-6. Thus, a POSITA would have been motivated to modify Wada to add the mode-selection circuitry of Fujioka to allow

burst length to be programmed late in the manufacturing process by using bond options or voltages on external pins tied to the mode setting circuits. Ex-1002 ¶121.

2. Dependent Claim 4

a. 4: The circuit according to claim 1, wherein said predetermined number of internal address signals is 8.

Wada discloses claim 1, as discussed above in Sections X.A.2, and X.B. A POSITA would have been motivated to add the mode-selection circuitry of Fujioka, for the reasons described above, which teaches fixing the burst length to eight by, for example, by using the circuit of Figure 10B with the pad bonded to Vss. Ex-1006 (Fujioka) at 14:50-15:24; Figs. 10A-10E. Ex. 1002 ¶122

FIG. 10B

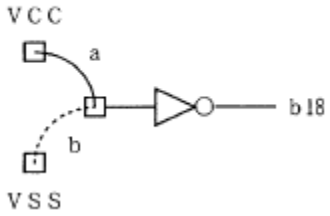


FIG. 10E

BONDING	b18	BURST LENGTH
a	L	4
b	H	8

3. Dependent Claim 5

a. 5: The circuit according to claim 2, wherein said fixed burst length is programmable.

Wada discloses claim 2, as discussed above in Sections X.A.3 and X.B.2. When combined with Fujioka for the reasons discussed above, the combined system would have a burst length that is programmable late in the manufacturing

process by, for example, bond options for tying a mode-selection circuit to a Vcc or Vss voltage or to external pins. Ex. 1002 ¶123.

4. Dependent Claim 6

a. 6: The circuit according to claim 5, wherein said fixed burst length is programmed by bond options.

The combination of Wada and Fujioka discloses claim 5, as described above. Fujioka discloses programming the fixed the burst length to either four or eight using bond options as shown in Figures 10B and 10E, wherein the option for bonding the pad to Vcc programs a burst length of 4 and bonding the pad to Vss programs a burst length of 8. Ex-1006 (Fujioka) at 14:50-15:24; Figs. 10A-10E. Ex. 1002 ¶124.

FIG. 10B

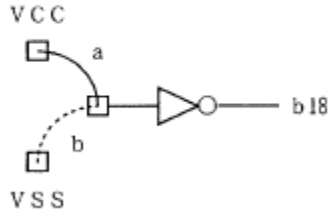


FIG. 10E

BONDING	b18	BURST LENGTH
a	L	4
b	H	8

5. Dependent Claim 7

a. 7: The circuit according to claim 5, wherein said fixed burst length is programmed by voltage levels on external pins.

The combination of Wada and Fujioka discloses claim 5, as described above. Fujioka discloses programming the fixed the burst length to either four or eight by

tying circuit pads to voltage levels, such as Vcc and Vss as shown in Figures 10A and 10D:

FIG. 10A

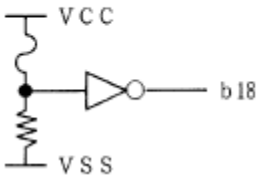


FIG. 10D

FUSE	b18	BURST LENGTH
NOT CUT	L	4
CUT	H	8

In addition, the applicant cited Lowrey during prosecution for the premise that bond options and their uses were well known by those of ordinary skill in the art, and Lowrey teaches that "any of the bond options can be connected with any of the pinouts." Ex-1014 (Lowrey) at 3:16-18; Ex-1004 (File History) at 42. Thus, the combination of Wada and Fukioka in light of what the applicant admits was well known in the art renders claim 7 obvious. Ex-1002 ¶¶125-26.

6. Dependent Claim 18

a. 18: The method according to claim 17, further comprising the step of programming said predetermined number.

Wada discloses claim 17, as discussed above in Sections X.A.9 and X.B.2. The combination of Wada and Fujioka renders claim 18 obvious for the same reasons discussed with respect to claim 5, in Section X.D.3, above.

7. Dependent Claim 19

a. 19: The method according to claim 18, wherein said programming step is performed using bond options.

Wada and Fujioka disclose claim 18, as discussed in Section X.D.6. The combination of Wada and Fujioka renders claim 19 obvious for the same reasons discussed with respect to claim 6 in Section X.D.4, above.

8. Dependent Claim 20

a. 20: The method according to claim 18, wherein said programming step is performed using voltage levels.

Wada and Fujioka disclose claim 18, as discussed in Section X.D.6. The combination of Wada and Fujioka renders claim 20 obvious for the same reasons discussed with respect to claim 7 in Section X.D.5, above.

E. Ground 3a: Claims 4-7, and 18-20 are rendered obvious by the combination of Wada, Barrett, and Fujioka in view of the knowledge of a POSITA.

The motivation to combine Wada and Barrett to ensure that the generation of internal addresses cannot be interrupted was discussed above in Section X.C. The combination of Wada, Barrett, and Fujioka renders claims 4-7, and 18-20 obvious for the same reasons discussed in Section X.D above. Ex. 1002 ¶¶127-30.

F. Ground 4: Claims 9-10, 14, and 21 are rendered obvious by the combination of Wada and US 6,226,755 ("Reeves") in view of the knowledge of a POSITA

1. Reeves

Reeves was filed January 26, 1999 and issued May 1, 2001, qualifying as prior art under at least pre-AIA 35 U.S.C. §102(e). Ex-1008 (Reeves) at 1.

Reeves is entitled "Apparatus and Method for Enhancing Data Transfer to or from a SDRAM System." *Id.* at 1. Reeves discloses a synchronous dynamic random access memory system configured for burst mode access. *See, e.g.*, *id.* at 4:3-5 ("The first set of SDRAM chips is coupled to read a data burst of N clock cycles initiated from a first read request."). Reeves notes there is a speed limitation in conventional DRAM systems:

> An important requirement of DRAM technology is that the RAS control signal must be maintained during the time in which access is desired. If a burst of data is to be read, then the amount of time at which the RAS control signal is maintained asserted is limited by the need to periodically pre-charge the row being read.

Id. at 1:29-34. To circumvent this problem, Reeves discloses hiding these refresh cycles behind a burst read of another partition:

> Accordingly, the present transfer mechanism employs a hidden refresh technique whereby refresh occurs without any latency on the data transfer and therefore without requiring a hold, interrupt, or stall on the multiple burst requesting device.

Id. at 9:32-36. Specifically, making the burst sufficiently long will hide the memory refresh cycle:

> At clock 6 a pre-charge can still occur and at clock 10 occurs, and the refresh of partition Y would still be hidden during the bursts occurring between read requests of partition X (i.e., between clocks 4 and 12). Thus, ***if the burst of data is long enough*** (e.g., 8 clock cycles as shown in partition X), then ***a refresh can be hidden during a single burst read*** of data from a single partition.

Id. at 9:46-52. Reeves further discloses that this technique can be applied to any

DRAM system:

> The SDRAM system employing the present hidden refresh technique is one which can be extended to any dynamic random access memory which must be refreshed and operates from control signals synchronized with the processor or system clock. Such synchronous memory systems include double data rate SDRAMs ("DDR SDRAM"), SyncLink DRAM ("SLDRAM"), and Rambus DRAM ("RDRAM").

Id. at 10:1-8. Ex. 1002 ¶131.

a. Motivation to combine Wada and Reeves

Wada is directed to improving speed and data throughput in a memory system employing SRAM. *See, e.g.*, Ex-1005 (Wada) at 5:66-6:2 ("It is therefore an object of the present invention to provide a semiconductor memory operating in burst at a sufficiently high speed irrespective of the operating speed of its memory cell array."). One of ordinary skill in the art at the time the '134 Patent was filed would have been well aware that DRAM systems offer the advantage of high memory density and lower cost as compared to SRAM. Ex-1002 ¶132. Thus, it would have been desirable to modify Wada's system to operate with DRAM. However, as discussed above, Reeves recognizes that a problem with DRAM systems is that the memory must be periodically refreshed, which tends to slow down data transfer operations. However, in a system capable of burst mode, such as Wada's, Reeves recognizes that speed can be maintained even in a DRAM system if the refresh cycles are properly aligned with the data bursts: "Careful placement of the hidden refresh cycles encountered by one partition relative to read

cycles on other partitions ensures the data flow resulting therefrom will be optimized to sustain peak bandwidth on a synchronous DRAM memory bus." Ex-1008 (Reeves) at Abstract. Thus, one of ordinary skill would have realized that Wada's high-speed burst-access architecture could be advantageously adapted to use DRAM, which would provide for much larger storage capacity for a given chip size, by following the teachings of Reeves, *i.e.*, setting the burst length sufficiently long to ensure that refresh cycles could be hidden behind the burst transfers in order to maintain high speed data transfer. Ex-1002 ¶132.

2. Dependent Claim 9

a. 9: The circuit according to claim 1, wherein said memory comprises a dynamic random access memory.

Wada discloses claim 1, as discussed above at Sections X.A.2 and X.B.1. As described above, Reeves teaches how to modify the system of Wada to use DRAM by configuring DRAM refresh cycles to be hidden behind a sufficiently long burst data transfer. Ex-1008 (Reeves) at 1:29-34; 7:16-27; 9:25-10:12; 10:13-12:27. One of ordinary skill would have been motivated to combine Wada and Reeves to take advantage of the higher storage density and lower cost of DRAM, as described above. Ex. 1002 ¶133. Thus, Wada and Reeves renders claim 9 obvious.

3. Dependent Claim 10

a. 10: The circuit according to claim 9, wherein said predetermined number of internal address signals is chosen to provide time for at least one writeback or refresh cycle.

Wada and Reeves disclose claim 9, as discussed above. Reeves discloses that the burst length, *i.e.*, the number of predetermined internal address signals, is chosen to be long enough to mask a refresh cycle. *Id.* at 9:46-52 ("***if the burst of data is long enough*** (e.g., 8 clock cycles as shown in partition X), then ***a refresh can be hidden during a single burst read*** of data from a single partition."). *See also* 1:29-34; 7:16-27; 9:25-10:12; 10:13-12:27. Thus, claim 10 is obvious. Ex. 1002 ¶134.

4. Dependent Claim 14

a. 14: A memory device according to claim 1, wherein said circuit is an integrated circuit.

As discussed above in Section X.B.4, Wada alone renders claim 14 obvious. However, because Wada does not expressly state that the disclosed memory circuit is an integrated circuit, Wada can be combined with Reeves for the reasons discussed above. Reeves expressly refers to its memory circuits as integrated circuits. *See, e.g.,* Ex-1008 (Reeves) at 3:67-4:2 ("The clocking circuit forwards the clocking cycles to a first, second, and third set of SDRAM ***integrated circuits*** . . ."); 4:36-39 ("FIG. 2 is a block diagram of a partitioned SDRAM system which includes a group of data lines associated with at least one ***SDRAM integrated***

circuit . . .”); claim 3 (“3. The computer System as recited in claim 1, wherein the first, second and third partitions each comprise at least one synchronous ***DRAM integrated circuit***.”). Thus, claim 14 is obvious. Ex. 1002 ¶135.

5. Dependent Claim 21

a. 21: The method according to claim 17, further comprising the step of selecting said predetermined number to provide time for at least one writeback or refresh cycle.

Wada discloses claim 17, as discussed in Sections X.A.9 and X.B.2. The combination of Wada and Reeves renders claim 21 obvious for the same reasons discussed with respect to claim 10 in Section X.F.3, above.

G. Ground 4a: Claims 9-10, 14, and 21 are rendered obvious by the combination of Wada, Barrett, and Reeves in view of the knowledge of one of ordinary skill in the art

The motivation to combine Wada and Barrett to ensure that the generation of internal addresses cannot be interrupted was discussed above in Section X.C. The combination of Wada, Barrett, and Reeves renders claims 9-10, 14, and 21 obvious for the same reasons discussed in Section X.F, above. Ex. 1002 ¶¶136-37.

H. Ground 5: Claims 11 and 15 are rendered obvious by the combination of Wada and US 5,784,331 (“Lysinger”) in view of the knowledge of one of ordinary skill in the art

1. Lysinger

Lysinger was filed December 31, 1996 and issued July 21, 1998, qualifying as prior art under at least pre-AIA 35 U.S.C. §102(b). Ex-1009 (Lysinger) at 1.

Lysinger is entitled "Multiple Access Memory Device" and discloses memory with a "burst counter which increments the input and memory address under the control of a clock without requiring new address to be input." *Id.* at 2:5-7. While this speeds data readout, a challenge of this approach is that "all address transitions must still propagate through the address decoder. The speed at which address signals can propagate through the address decoder may become a limiting factor at faster cycle times." *Id.* at 2:16-20. Thus, Lysinger proposes to use the flexibility of freeing up the address bus during burst reads to allow a new address to propagate through the decoder and for the controller to perform other functions, such as addressing other memory devices or interfacing with the microprocessor:

> Further, there is a timing window over which the cache controller 572 may have the option to present this new address data and still continuously operate at the high speed. Assume for the moment that the burst count is for eight clock cycles. The new address data can be presented over the time interval from the first clock cycle until the seventh clock cycle. Thus, if the new address data is not provided until the third or seventh clock cycle, it will still have sufficient time to propagate through the address decoders so that the new address data arrives at the storage latch 409 in sufficient time for the new burst sequence to start at the end of the old burst count sequence. Thus, after the cache controller 572 loads a first burst address into a memory device 50, it may proceed to perform other functions such as accessing other memory devices or interfacing with the microprocessor 570. This may continue for one, two or as many burst cycles as available, depending upon the tasks being performed by the cache controller 572. . . . This is particularly advantageous if a single cache controller 572 is controlling an entire bank of memory chips because the cache controller may conveniently provide the new address data on its own timing sequence within the window interval to the various banks of memory devices or the individual memory devices.

Id. at 26:34-27:3.

a. Motivation to combine Wada and Lysinger

Wada discloses that burst transfers are desirable to improve speed and data throughput. *See, e.g.*, Ex-1005 (Wada) at 5:66-6:2 ("It is therefore an object of the present invention to provide a semiconductor memory operating in burst at a sufficiently high speed irrespective of the operating speed of its memory cell array."). During a burst, the system memory is addressed by an internal address generated by a counter (*e.g., id.* at Fig. 3 (burst counter unit 8); Fig. 12 (burst counter 84)) instead of by an external address and control signals asserted by an external controller. Thus, Wada's system frees up the address and control busses during a burst because they do not have to change state. *See, e.g.*, Fig. 13 (EXT.ADD, ADS, WE signals need not toggle during a burst); Fig. 4 (MADD, INT.ADD, WRA, RRA need not toggle during a burst). Wada, however, addresses a single memory array and does not disclose using the freed up address and control capacity to perform other tasks.

Lysinger points out that the freed-up capacity could be used to address an additional memory array, for example: "Thus, after the cache controller 572 loads a first burst address into a memory device 50, it may proceed to perform other functions such as ***accessing other memory devices*** or interfacing with the microprocessor 570." Ex-1009 (Lysinger) at 26:45-49. One of ordinary skill

would have understood the advantage of being able to address additional memory arrays while address and control busses were freed up because that would provide even greater data throughput, which is a goal both Wada and Lysinger are trying to achieve. Ex-1002 ¶¶138-41. Thus, one of ordinary skill would have understood that the system of Wada could be modified to add an additional memory array that could be addressed using the freed-up address and control capacity as taught by Lysinger. Lysinger further teaches that doing so would be successful because the length of the burst creates a timing window during which the system has time for a new address to propagate through the decoders. Ex-1009 at 26:37-45:

> Assume for the moment that the burst count is for eight clock cycles. The new address data can be presented over the time interval from the first clock cycle until the seventh clock cycle. Thus, if the new address data is not provided until the third or seventh clock cycle, it will still have sufficient time to propagate through the address decoders so that the new address data arrives at the storage latch 409 in sufficient time for the new burst sequence to start at the end of the old burst count sequence.

Wada discloses that the length of the burst is simply the number of blocks the memory is chosen to be organized into, *e.g.,* four. Ex-1005 at 3:49-55. Thus, one of ordinary skill in the art would have understood that the burst length of Wada could be set by selecting the number of memory blocks such that the burst was sufficiently long to allow the controller to address as many memories as desired and such that the address still had time to propagate through the controller, as taught by Lysinger, and would have expected the combination of Wada and

Lysinger to be successful. Ex-1002 ¶¶140-42.

2. Dependent Claim 11

a. 11: The circuit according to claim 1, wherein said predetermined number of internal address signals is chosen to meet predetermined criteria for sharing address and control busses.

Wada discloses claim 1, as discussed above in Section X.A.2. One of ordinary skill would have been motivated to combine Wada with Lysinger as discussed above. As described above, predetermined criteria could be a number of memories desired to be accessed by the controller. The combination of Wada and Lysinger would choose the number of internal address signals, or burst length, to be sufficient that the address bus and control lines of Wada, which are idle during a burst, could be shared to address the additional memories, as Lysinger discloses. *See* Ex-1009 at 2:4-20, 26:34-27:3. Thus, claim 11 is obvious. Ex-1002 ¶143.

3. Dependent Claim 15

a. 15[a]: The circuit according to claim 1, further comprising address and control busses configured to present said external address signal and said one or more control signals,

Wada discloses claim 1, as discussed above in Sections X.A.2 and X.B.1. Wada discloses address and control busses configured to present said external address signal and one or more control signals. For example Wada's conventional embodiment discloses an external address bus EXT.ADD (100). Ex-1005 (Wada) 2:15-19; Fig. 12. That embodiment further discloses control signals. *Id.* at Fig. 12,

e.g., ADV (93), ADS(94); 2:56-61 ("when the advance signal ADV is brought High, the address on the burst counter 84 is incremented every time a leading edge of the clock signal CLK is encountered.").

Wada's second embodiment also discloses external address busses MADD and EXT.CHA. *Id.* at 15:37-40 ("Referring to FIG. 4, the address An designated by the memory address signal MADD is admitted into the internal register 20 at a first leading edge of the clock signal CLK in the second cycle."); 4:17-21 ("burst counter unit 8 admits an address AC stemming from the external chunk address signal EXT.CHA."). It also discloses control signals. *Id.* at Fig. 3 (e.g., ADV(93), ADS(94), RRA(96), WRA(95), TR); 12:60-65 (TRA transfers data to/from output registers); 2:55-3:15 (ADV enables incrementing of burst counter); 1:64-2:13 (ADS address strobe latches in external address); 14:57-15:36 (RRA causes multiplexers to designate a register from which to read data; WRA causes multiplexer to designate registers to receive data). Ex-1002 ¶¶144-45.

b. 15[b]: wherein said busses are freed up during the generation of said predetermined number of internal address signals.

Wada discloses that the busses are freed up during the generation of internal address signals, as can be seen in Figure 13 (waveform for conventional embodiment, showing EXT.ADD and control signals ADS and /WE not toggling during bursts) and Figure 4 (waveform for second embodiment, showing MADD

and EXT.CHA and control signals WRA, TR, RRA not toggling during bursts):

FIG.13
PRIOR ART

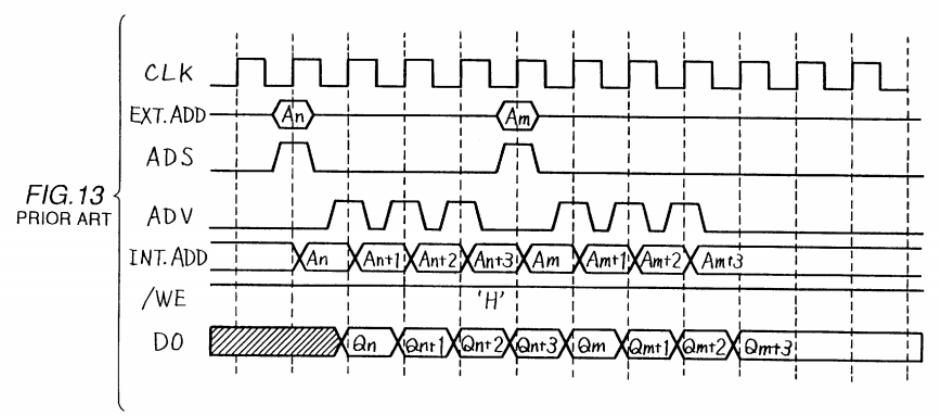
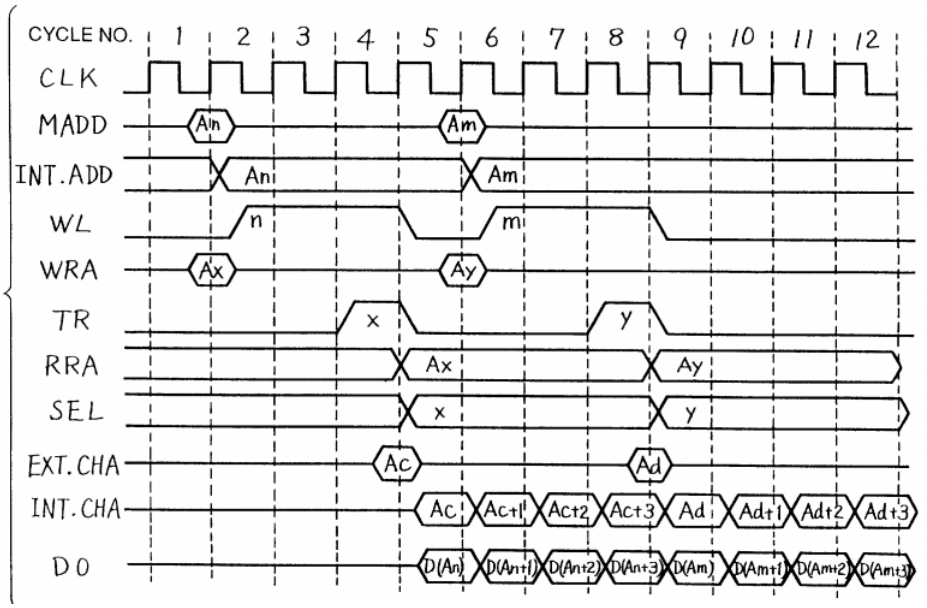


FIG.4



Lysinger further discloses that this timing window can be used to take advantage of the freed up capacity of the address and control circuitry. Ex-1009 at 26:34-27:3. Thus, claim 15 is obvious. Ex-1002 ¶¶146-47.

I. Ground 5a: Claims 11 and 15 are rendered obvious by the combination of Wada, Barrett, and Lysinger in view of the knowledge of one of ordinary skill in the art

The motivation to combine Wada and Barrett to ensure that the generation of internal addresses cannot be interrupted was discussed above in Section X.C. The combination of Wada, Barrett, and Lysinger renders claims 11 and 15 obvious for the same reasons discussed in Section X.H above. Ex-1002 ¶148.

XI. CONCLUSION

The invalidity grounds presented above are reasonably likely to prevail, and thus *inter partes* review should be instituted.

Respectfully Submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Petitioner certifies that this petition includes 13,783 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under §42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §42.6(e) and §42.105 that on May 26, 2020, a true and correct copy of the Petition for *Inter Partes* Review of U.S. Patent No. 6,651,134 challenging claims 1-21 was served via express mail on the Patent Owner at the below correspondence address of record:

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