UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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ADVANCED MICRO DEVICES, INC.,
Petitioner

v.

MONTEREY RESEARCH, LLC,
Patent Owner.

# PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,373,455

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| Ex-1004 | Prosecution History of U.S. Patent No. 8,373,455 |
| Ex-1005 | Prosecution History of U.S. Application Ser. No. 11/904,901 (Parent of U.S. Patent No. 8,373,455) |
| Ex-1006 | U.S. Patent No. 6,037,811 ("Ozguc") |
| Ex-1007 | U.S. Patent No. 7,170,324 ("Huber") |
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| Ex-1010 | U.S. Patent No. 6,414,516 ("Labram") |
| Ex-1011 | "CMOS Circuit Design, Layout, and Simulation," IEEE textbook, R. Jacob Baker (1998) ("Baker") |
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# I. INTRODUCTION

Advanced Micro Devices, Inc. ("Petitioner") requests *inter partes* review of claims 1-14 of U.S. 8,373,455 ("the '455 Patent") (Ex-1001).

The '455 Patent is directed to a buffer circuit with variable current supplies for controlling the rise and fall times of signal output. An output buffer is positioned at the output of an integrated circuit to selectively control the transfer of signals to signal lines connected to other circuits. Ex-1007, 1:11-35; Ex-1001, 1:15-21. When switched on, the buffer transfers information by generating an "output [signal] … that follows the input signal." Ex-1007, 1:36-44.

The '455 Patent purports to improve known buffer designs. Ex-1001, 1:22-47, Fig. 5. It discloses a buffer that allegedly "can meet performance requirements over a range of operating voltages" and provide an output signal that meets "a desired signal profile." *Id.*, 2:11-20. During prosecution, claim 1 was allowed because it was amended to require a "variable current supply … configured to control the rise time." Ex-1004, 110. Independent claims 7 and 11 were allowed because they each recite a "selectable current source." *Id.*, 111-13.

Prior art presented herein, which was not considered during prosecution, discloses a buffer having selectable, variable current supplies for controlling the output's rise and fall times. For the reasons stated below, all 14 claims are unpatentable.

## II. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

**Real Parties-in-Interest**: Advanced Micro Devices, Inc. and ATI Technologies ULC (AMD's indirect, wholly-owned subsidiary).

**Related Matters**:

- Patent Owner has asserted the '455 Patent against Petitioner in *Monterey Research, LLC v. Advanced Micro Devices, Inc.*, No. 1:19-cv-02149-CFC (D. Del.).

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## III. FEE AUTHORIZATION

Under 37 C.F.R. §42.15(a), §42.103(a), the PTO is authorized to charge $30,500 (or other required fees) to Deposit Account 50-0639.

## IV. STANDING

Under 37 C.F.R. §42.102(a)(2), §42.104(a), Petitioner certifies that the '455 Patent is available for IPR, this Petition is timely filed, and Petitioner is not barred or estopped from requesting IPR review on the grounds presented.

## V. RELIEF REQUESTED

Petitioner requests review and cancellation of all 14 claims of the '455 Patent under 35 U.S.C. §102 and/or §103 based on the following grounds.

- **Grounds 1-2**: Claims 7, 8, 10, and 13 are anticipated by or obvious over US 6,037,811 ("Ozguc")[1];
- **Ground 3**: Claims 7, 8, and 10-13 are obvious over Ozguc and US 7,170,324 ("Huber");
- **Ground 4**: Claim 9 is obvious over Ozguc and US 5,994,945 ("Wu");

[1] The grounds for claims 7 and 11 and their dependents involve fewer references and are addressed before the grounds for claim 1 and its dependents.

- **Ground 5**: Claim 9 is obvious over Ozguc, Huber, and Wu;
- **Grounds 6-7**: Claims 11 and 12 are anticipated by or obvious over Huber;
- **Ground 8**: Claims 1-6 and 14 are obvious over Ozguc, Huber, and Wu;

None of the references relied upon in this Petition was cited during prosecution. Ex-1001, 1.

## VI. TECHNOLOGY BACKGROUND

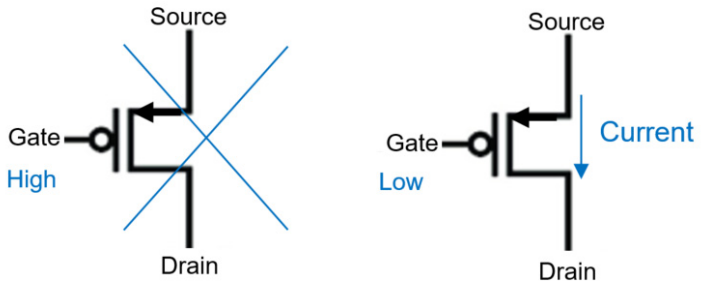
### A. Impedance

Impedance measures the opposition a circuit presents to a current. Ex-1011, 381. A buffer can change its output signal by drawing an appropriate amount of current, as explained below. Ex-1006, 1:15-35. Impedance is relevant to buffer design because the designed impedance of a buffer's circuit affects the current flow through the circuit. *Id.*; Ex-1002, ¶19; Ex-1007, 2:13-22, 2:59-3:28.

### B. Field-effect transistors (FETs)

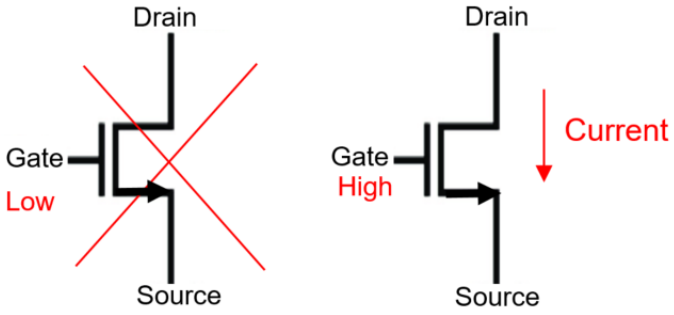
An FET acts as an on/off switch by using an electric field to control current flow. Ex-1011, 83-103, 192-95, 719. The FET can be switched on/off by changing the voltage applied to its gate terminal, which controls the impedance exhibited by the path between its source and drain terminals. *Id.*

A p-type FET (PMOS) allows current flow by providing a low-impedance source-to-drain path when the gate voltage is low and prohibits flow when the voltage is high. *Id.,* 226, 381.




Ex-1002, ¶¶20-21 (citing Ex-1011, 83 (Fig. 5.1))

An n-type FET (NMOS) allows current flow when the gate voltage is high and prohibits flow when the voltage is low. *Id.*; Ex-1011, 83-103; Ex-1012, 3:24-26.




Ex-1002, ¶22 (citing Ex-1011, 83 (Fig. 5.1))

For both FET types, the source-drain impedance depends on the voltage difference between gate and source ($V_{GS}$) and the FET's physical dimensions. *Id.*, ¶23; Ex-1011, 83-103; Ex-1012, 3:24-26.

### C. Buffer circuits

A buffer drives its output to follow its input, by pulling up the output (*e.g.*, increasing the output voltage) when the input rises and pulling down the output

(*e.g.*, decreasing the output voltage) when the input falls. Ex-1002, ¶¶24-25; Ex-1007, 1:35-45, 2:23-32; Ex-1006, Abstract, 1:16-35.

Figure 5 of the '455 Patent shows a prior art buffer (500). Ex-1001, 2:7. During pull-up (blue), the "IN[PUT]" rises and the pull-up driver (512) draws a current from the gate of a "p-channel output transistor 515" to enable it to "drive[]" "the output" "high" after a rise time. Ex-1001, 1:22-47; Ex-1002, ¶¶27-30. During pull-down (red), the "IN[PUT]" falls and the pull-down transistor (517) is enabled to "drive[]" "the output" "low." *Id*.

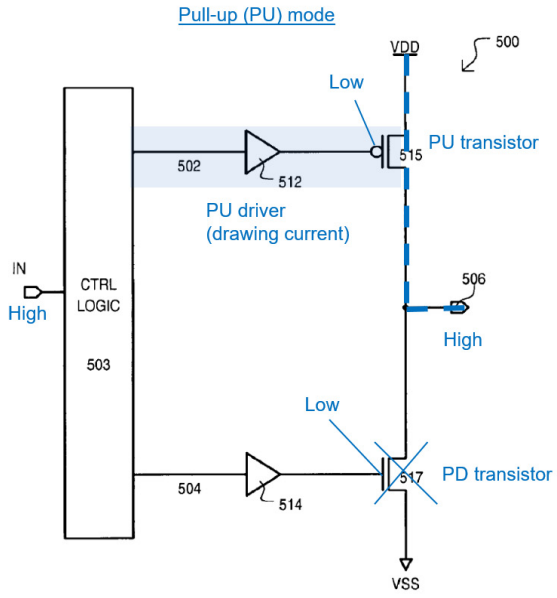



FIG. 5 (BACKGROUND ART)

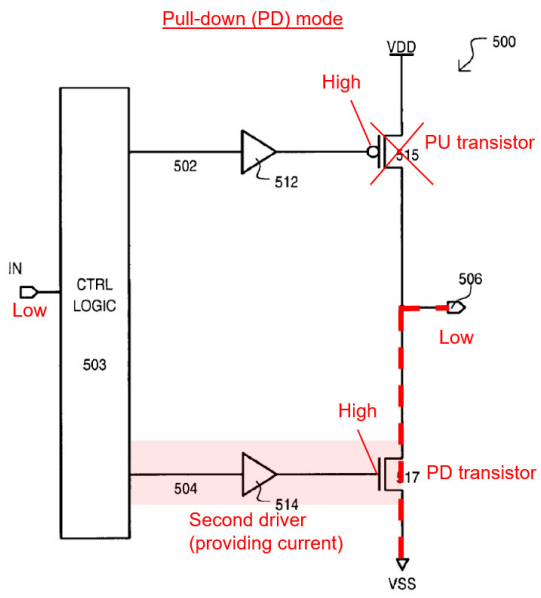



FIG. 5 (BACKGROUND ART)

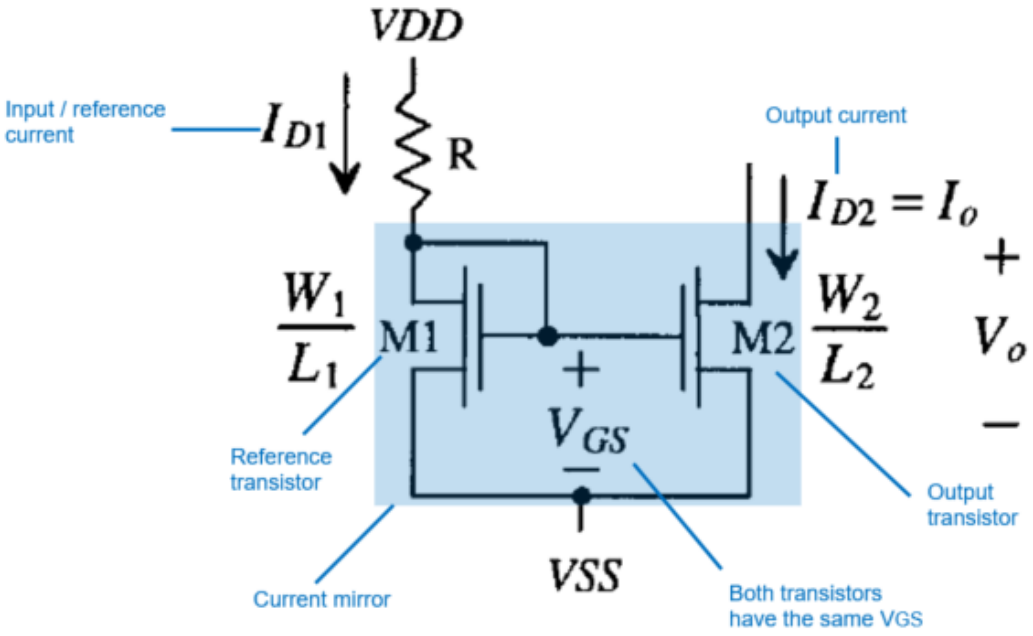
Ex-1001, Fig. 5[2]

[2] All color annotations are added.

In both cases, the output (506) changes to follow the state of the input ("IN"). *Id.* The time it takes for the output to change between high/low states after a change in the input—*i.e.,* the rise and fall times—affect the buffer's performance attributes. *E.g.,* Ex-1007, 1:17-2:32; Ex-1002, ¶30. For example, while a low rise/fall time improves the buffer's speed of data/signal transfer, it may distort the output signal. *Id.*

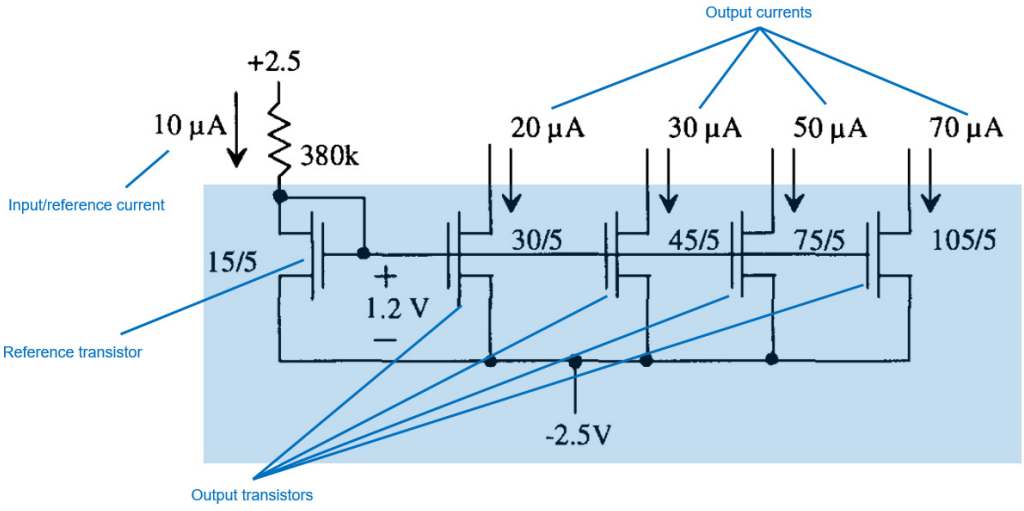
### D. Current mirrors

A current mirror is a circuit that produces one or more output currents that are each proportional to the input current. Ex-1002, ¶¶31-33. A "basic current mirror" is shown below. Ex-1011, 427-29. The output transistor's (M2's) output current ("$I_{D2}=I_O$") is proportional to the input current ("$I_{D1}$") at the reference transistor (M1) because M1 and M2 have the same gate-source voltage ($V_{GS}$). *Id*. The output-to-input current ratio depends on the relative sizes of M1 and M2. Ex-1011, 427-42.




Ex-1011, 428 (Fig. 20.1)

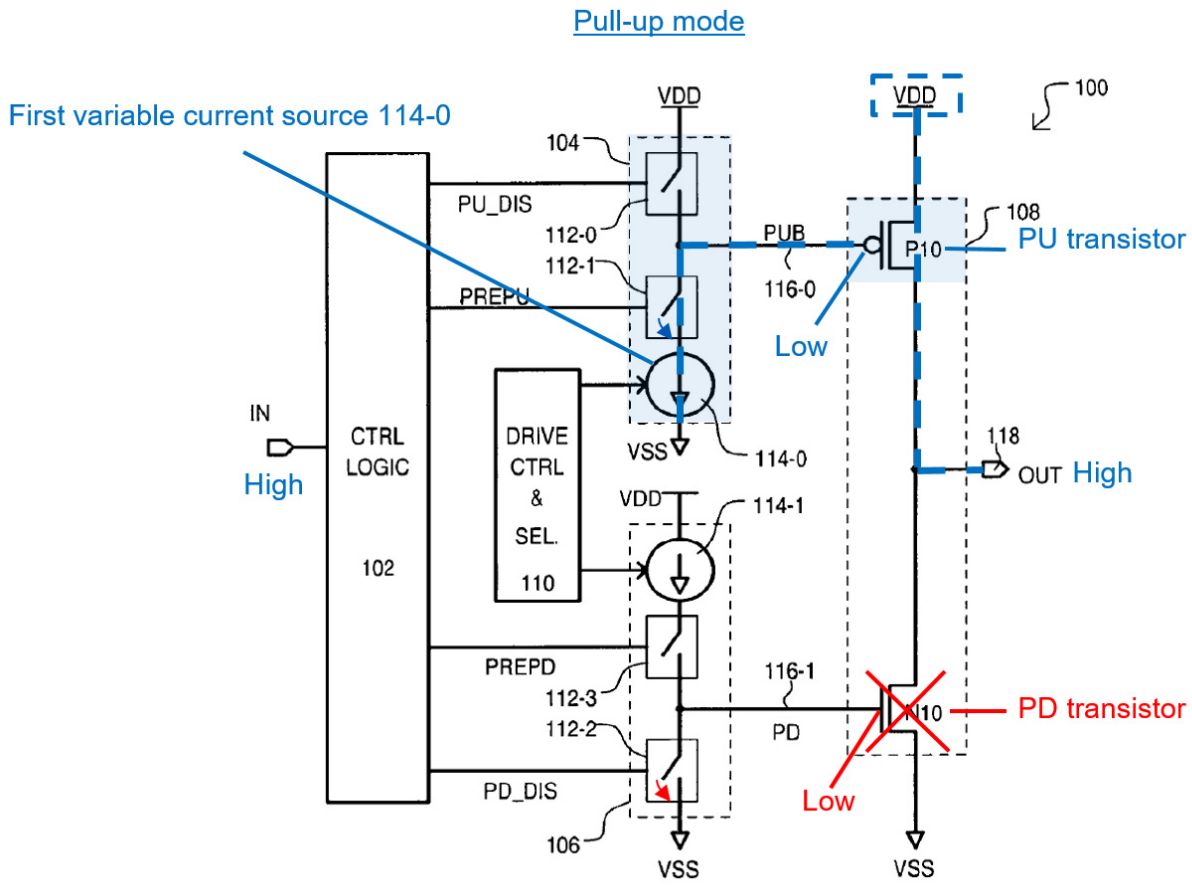
As shown below, a mirror may have multiple output transistors to output multiple currents that are each proportional to the input current. *Id.*, 431-37.




*Id.*, Fig. Ex20.2

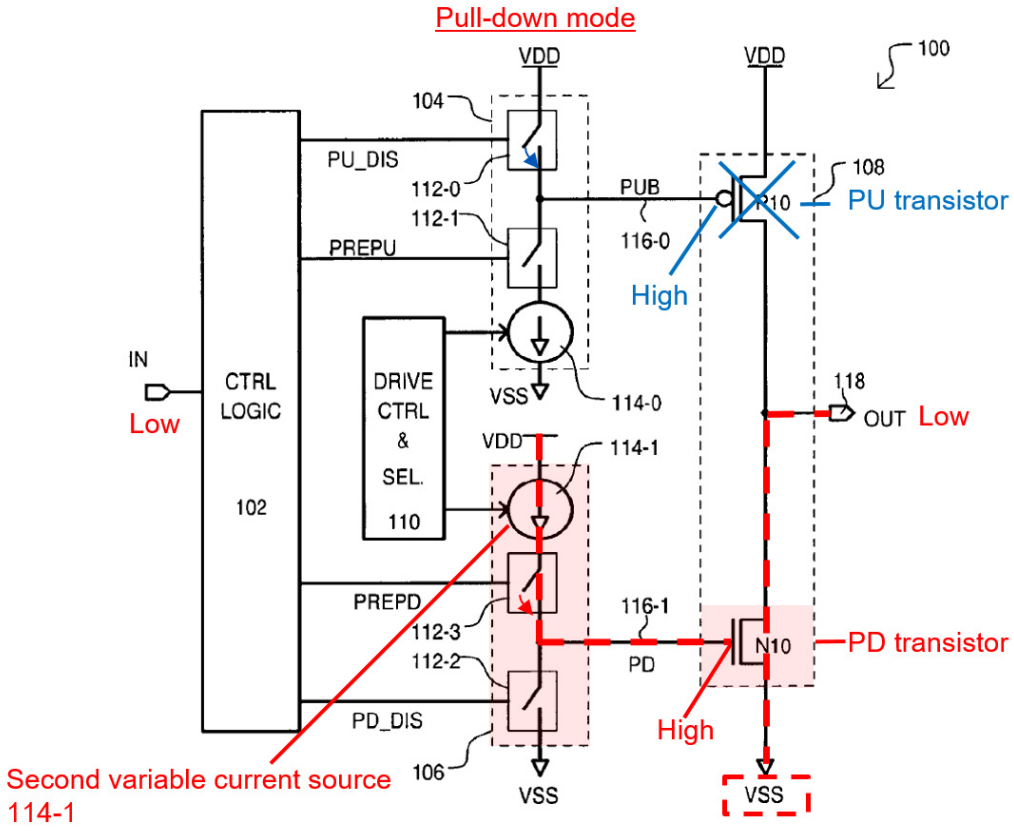
## VII. THE '455 PATENT

The '455 Patent discloses a buffer circuit having a variable current supply for controlling the rise and fall times. Ex-1001, 6:27-31. Figure 1 illustrates a buffer (100) having a "first variable current source 114-0" for controlling "the rise time." *Id.*, 2:32-36. When the input rises, "a potential at the gate of PFET P10 fall[s] according to the current drawn by first variable current source 114-0." *Id.*, 2:62-3:5, 3:31-37, 6:32-36. The pull-up driver transistor (108) pulls up the output after a "rise time" that depends on the variable current. *Id.*




Ex-1001, Fig. 1

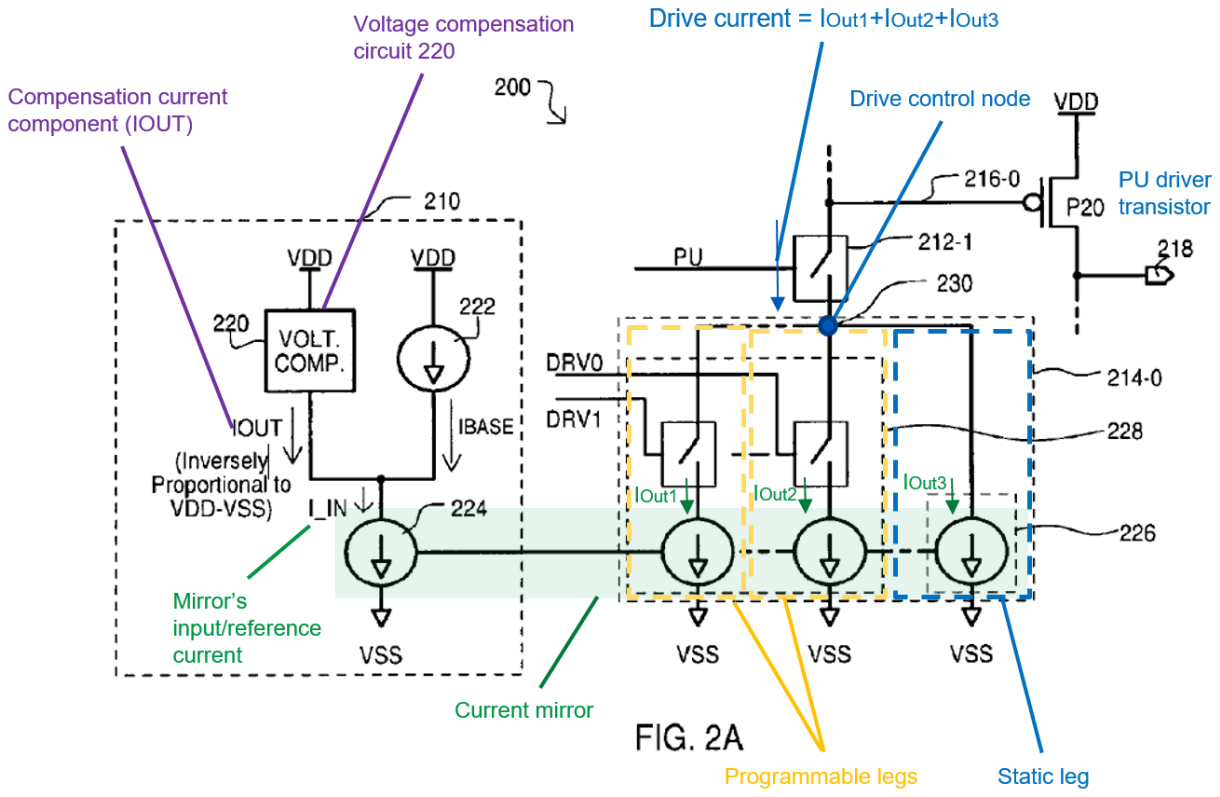
When the input falls, the output is pulled down after a "fall time" that depends on the current provided by the "second variable current source" (114-1). *Id.,* 2:49-61, 3:14-37; Ex-1002, ¶¶34-35.




Ex-1001, Fig. 1

Figure 2A illustrates details of the "pull-up path." Ex-1001, 3:40-41. Changes in the operating conditions (*e.g.,* temperature) can affect the supply voltage and therefore the current in the path. *Id.*, 1:55-62. The '455 Patent purports to address this problem by generating the current using a reference current (I_IN) having a component (I_OUT) that "varies inversely with power supply

voltage" (*i.e.*, decreases when the "supply voltage increases"). *Id.*, 3:44-59; *see also* 1:55-62, 4:45-48. The circuit includes a "current mirror" (highlighted) that uses the reference current (I_IN) to generate output currents ($I_{Out1}$, $I_{Out2}$, and $I_{Out3}$) for controlling the pull-up transistor (P20). *Id.,* 3:44-63. The sum of these output currents at the "drive control node 230" is a "drive current" because it drives the pull-up transistor (P20) to turn it on and thus drive the output high. *Id.,* 3:64-4:21, 5:11-16; Ex-1002, ¶36.




Ex-1001, Fig. 2A

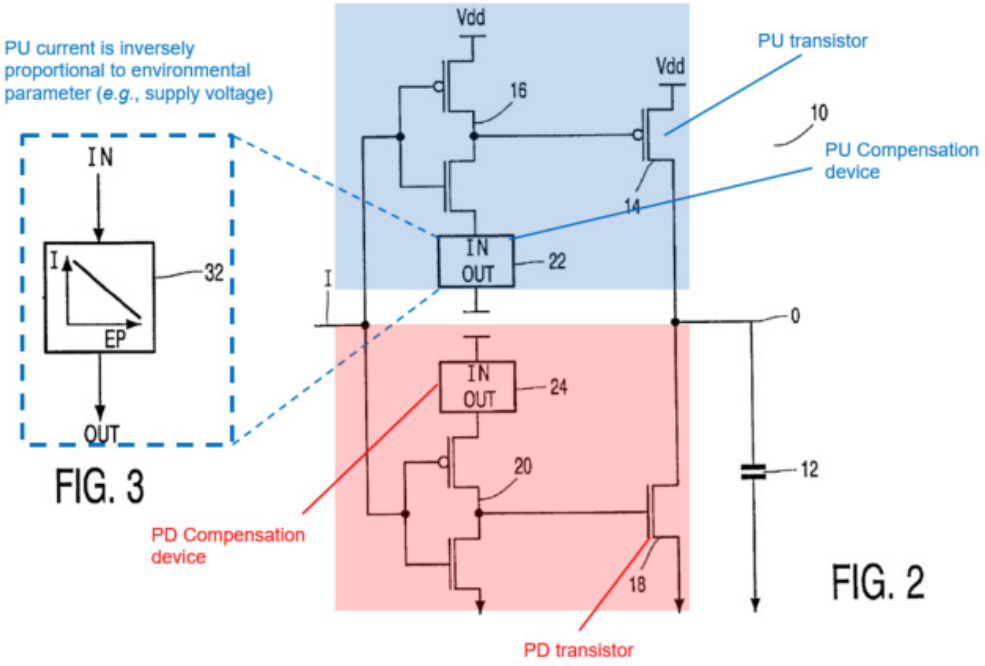
The amount of drive current controls how fast the output switches—a higher current leads to a "relatively fast switching speed." Ex-1001, 6:32-43. To change

the "rise time," "the first variable current source" (214-0) can vary the total drive current by using different combinations of the current mirror's components ($I_{Out1}$, $I_{Out2}$, and $I_{Out3}$). *Id*., 1:55-62, 3:31-37, 5:11-16; Ex-1002, ¶37. The source (114-0) includes one "static" current leg (226) that remains on and two "programmable" current legs (228) that can be selectively turned on/off by drive "signals DRV0 and DRV1." Ex-1001, 3:31-41, 3:64-4:21. The total drive current can therefore be "var[ied]," to change "the rise time," by turning on or off the currents in the selectable legs. *Id*.; *see also* 3:13-30, 6:27-43.

## VIII. PATENT PROSECUTION HISTORY

The '455 Patent issued from Application 13/013,725, a continuation of Application 11/904,901 (issued as U.S. 7,876,133 (Ex-1009)). The two patents have similar claim 1's. *Compare* Ex-1001, claim 1 *with* Ex-1009, claim 1.

During prosecution of the '901 application, the Examiner rejected all claims as being anticipated by U.S. 6,414,516 ("Labram") (Ex-1010). Ex-1005, 154-56; Ex-1010, 3:66-67. The Examiner found that Labram discloses, in Figures 2-3, a buffer circuit having a compensation circuit (22) that serves as a "variable current supply" because its current "is inversely proportional to a power supply voltage." Ex-1005, 156; Ex-1010, 3:35-4:39. Claim 1 was allowed after it was amended to require a first variable current supply "configured to control a rise time and a fall time of the output driver circuit." Ex-1005, 90, 139-45.




Ex-1010, Figs. 2-3

During prosecution of the ’725 application, the applicant overcame a similar rejection of claim 1 by amending it to require a “variable current supply … configured to control a rise a time of the output driver circuit.” Ex-1004, 100, 110, 122-27. Claims 7 and 11 were allowed because each recites a “selectable current source.” *Id.*, 19, 100, 110-16.

## IX. LEVEL OF ORDINARY SKILL IN THE ART

When the ’455 patent was filed, a POSITA would have had a bachelor’s degree in electrical or computer engineering, applied physics, or a related field, and at least two years of experience in design, development, and/or testing of circuits,

related hardware design, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002, ¶52.

## X. CLAIM CONSTRUCTION

Petitioner interprets the '455 Patent's claims according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). To resolve the grounds presented in this Petition, Petitioner does not believe any term requires explicit construction.[3]

## XI. EXPLANATION OF GROUNDS

### A. Claims 7, 8, 10, and 13 are anticipated by (Ground 1) or obvious over (Ground 2) Ozguc

#### 1. Ozguc

Ozguc issued on March 14, 2000 and qualifies as §102(b) art. Ozguc discloses "an ***output driver or buffer circuit with current-controlled output rise and fall times***."[4] Ex-1006, 1:17-19.

Figure 1 is annotated below to show a pull-up state. Ozguc discloses an "output buffer" having a "charging circuit" 120 (blue) for pulling up the output. Ex-1006, 2:8-32; Ex-1002, ¶56. "When the input signal 101 is high," the "first adjustable source 122" draws an adjustable current ($I_1$) from MP1's gate and turns

[3] Petitioner reserves its rights to assert in litigation claim constructions not asserted here and assert that certain terms are indefinite.

[4] All emphases are added.

on MP1. *Id.* A current mirror (green) uses the adjustable current ($I_1$) as a reference current to "supply a charging current $I_{chg}$ to the OUT[PUT] terminal" to pull up the output after a "rise time." Ex-1006, 2:8-44; Section VI.D. The "rise time [is] proportional to the amount of current $I_{chg}$, which is, in turn determined by" the amount of adjustable current ($I_1$). *Id.;* Ex-1006, 4:5-16.

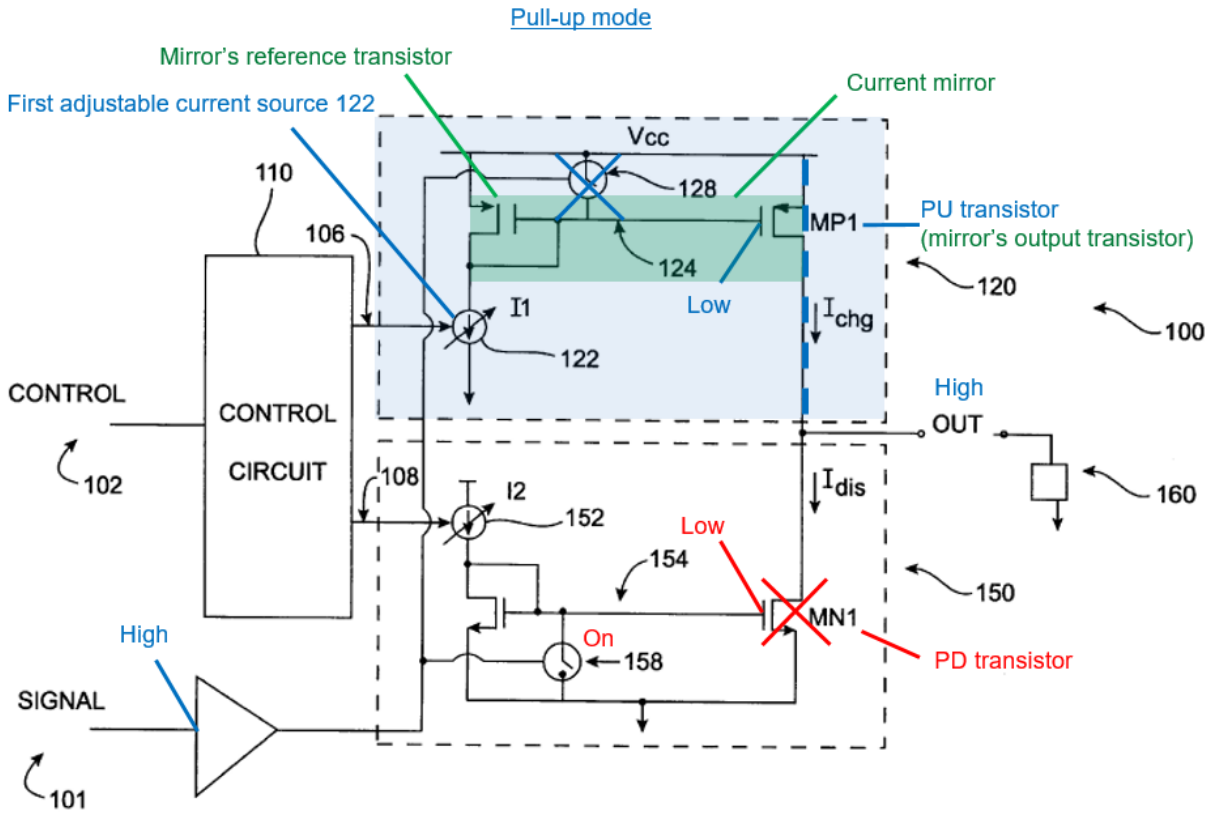



FIG. 1

Ex-1006, Fig. 1

Figure 1 is annotated below to show the pull-down state: when the input falls, the current supplied by the second adjustable source 152 ($I_2$) controls the "fall time." Ex-1006, 2:15-20, 2:33-44, 3:30-42; Ex-1002, ¶57.

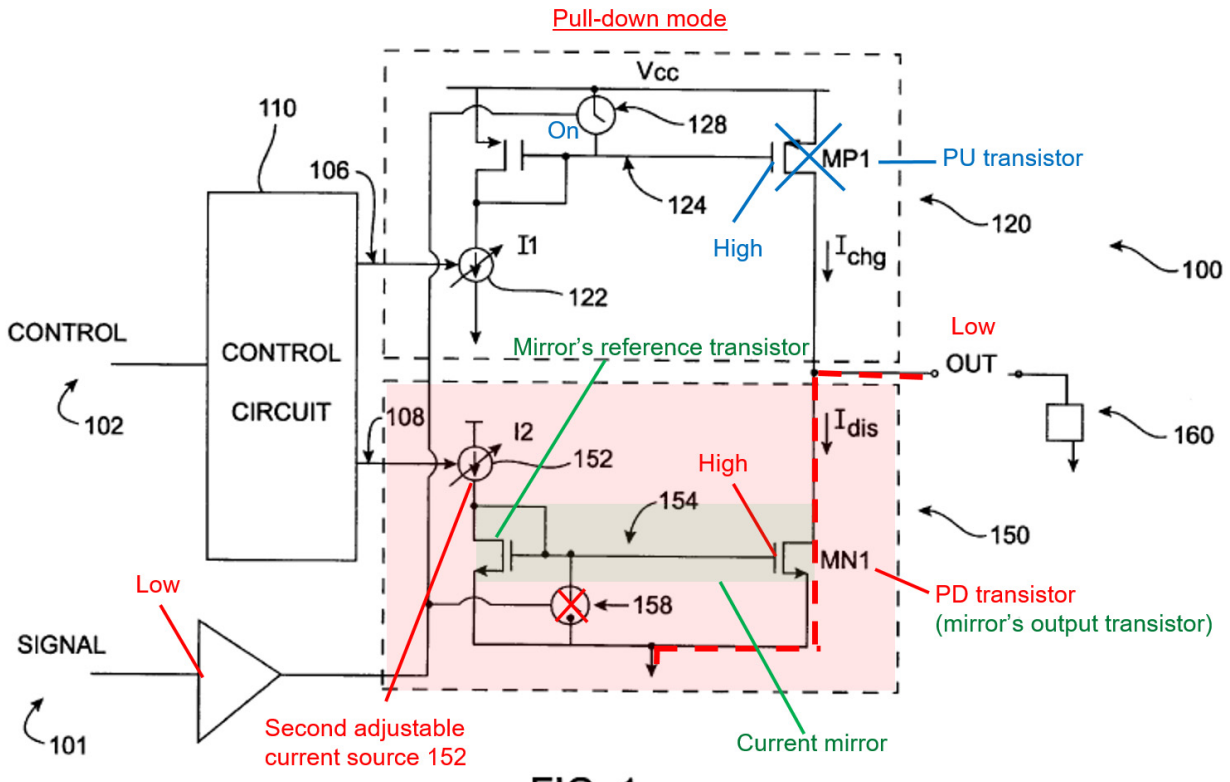
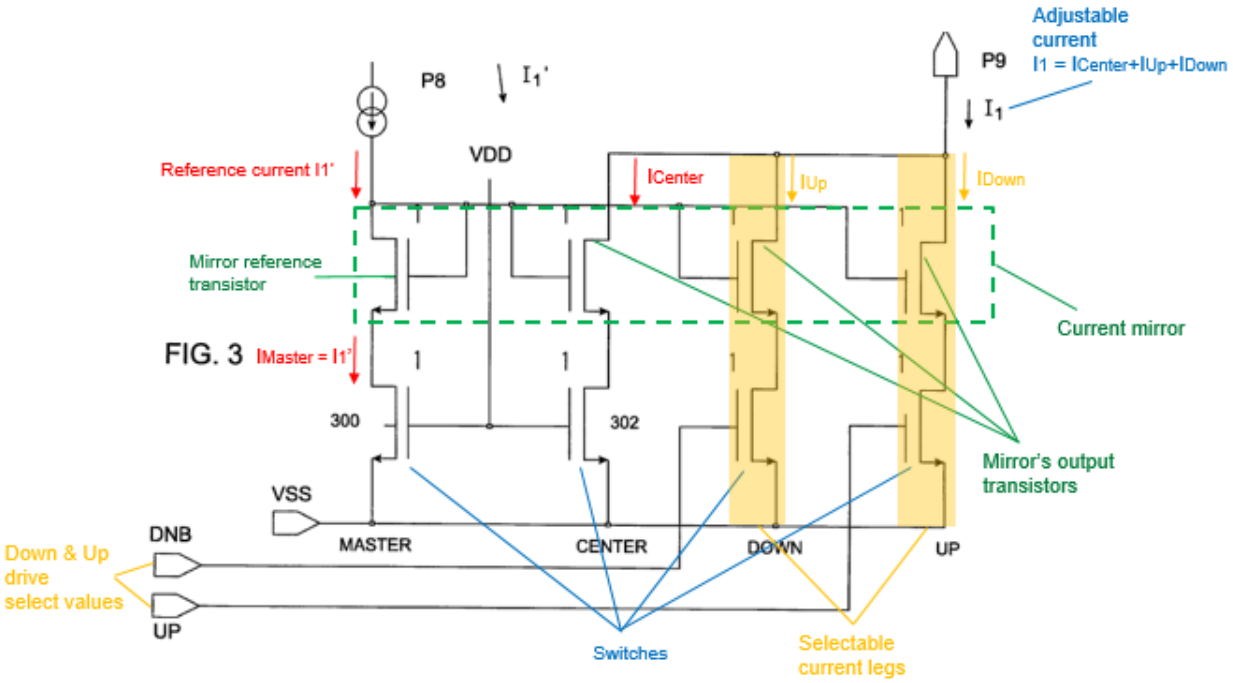



FIG. 1

Ex-1006, Fig. 1

Ozguc discloses that "FIG. 3 illustrates one embodiment of the adjustable current source," in which the source may include four current paths (Master, Center, Up, Down). Ex-1006, 4:10-39. A POSITA would have understood that one or both of the "adjustable current sources" (122 and 152 in Figure 1) may include the current paths shown in Figure 3. Ex-1006, 1:60-61, 4:10-14, 4:42-46. In Figure 3, Ozguc discloses that the upper transistors form a current "mirror" having a reference transistor (Master leg's upper transistor) and three output transistors (the upper transistors of Center, Up, and Down legs) that output three currents ($I_{Center}$, $I_{Up}$, $I_{Down}$) each mirroring the input/reference current ($I_1'$). Ex-1006,

4:10-46; Section VI.D; Ex-1002, ¶58. The three output currents are added to produce the adjustable current $I_1$. *Id*.




Ex-1006, Fig. 3

Each leg's lower (NMOS) transistor serves as a switch for turning on/off the current in the same leg. Ex-1006, 4:17-36; Ex-1002, ¶¶59-60. Master and Center legs' lower transistors "remain on" because their gates are connected to the supply voltage. Ex-1006, 4:17-22. Up and Down legs' lower transistors are connected to "DNB" and "UP" to selectively turn on/off the current flow in those legs. Ex-1006, 4:24-44. Ozguc teaches an embodiment in which the transistors all have "similar size[s]," resulting in the current in each leg being equal to the reference current ($I_1$'), and the total adjustable current ($I_1$) being once, twice, or three times the reference current ($I_1$') depending on whether one or both of "Up and "Down"

are selected. Ex-1006, 4:10-46; Ex-1002, ¶¶59-60; *see* Section VI.D. "Thus … the current $I_1$, and accordingly, the rise time can be adjusted" using drive select values "DNB" and "UP." Ex-1006, 4:42-46, 5:10-11.

Ozguc calls the above-described structure of parallel current legs as "cascode pairs of NMOS FETs." Ex-1006, 4:10-17.

**2. Independent Claim 7**

**a. 7[pre]: An output driver circuit, comprising:**

To the extent limiting, Ozguc discloses "***an output driver*** or buffer ***circuit***." Ex-1006, 1:17-51, Figs. 1-3[5]; Section XI.A.1; Ex-1002, ¶61.

[5] Ozguc discloses four embodiments: (1) Figure 1's output driver circuit; (2) Figure 2's output driver circuit; (3) Figure 1's circuit with one or both of the adjustable current sources 128/158 include the current mirror structure in Figure 3, as described in Section XI.A.1; (4) Figure 2's circuit with one or both of the adjustable current sources 222/252 include the current mirror structure in Figure 3. Ex-1006, 1:60-62, 4:10-16; Ex-1002, ¶61. Unless stated otherwise, each embodiment independently discloses all claim limitations.

**b. 7[a]: a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;**

Ozguc discloses a first driver transistor ("charging transistor MP1") providing a low-impedance path to an "OUT[PUT]" node in response to a voltage applied at MP1's gate terminal. Ex-1006, Figs. 1-2.

MP1 is a "driver transistor" because it "suppl[ies] a charging current $I_{chg}$" that "drive[s]" "the OUT[PUT] terminal" to a high voltage—$V_{CC}$ in Fig. 1 or $V_{25}$ in Fig. 2—"when the input signal 101 is high." Ex-1006, 2:8-32, Figs. 1-2; *see also* 1:55-60, 2:45-3:13; Ex-1002, ¶¶62-63; Section XI.A.1; *compare with* Ex-1001, Fig. 1 (P10). Ozguc describes "MP1" as a PMOS. *Id.*; Ex-1006, 2:55-58. Based on the operation of a PMOS, a POSITA would have understood that as the "current $I_1$" pulls down MP1's gate voltage, MP1 "conduct[s]" (turns on) and provides a low-impedance path from its source power supply node ($V_{CC}$/$V_{25}$) to its drain ("OUT") node, as annotated in Figure 1. Ex-1006, 2:8-65, 3:62-4:9; *see also* 1:66-2:8, Fig. 2; Sections VI.B, XI.A.1; Ex-1002, ¶¶63-64.

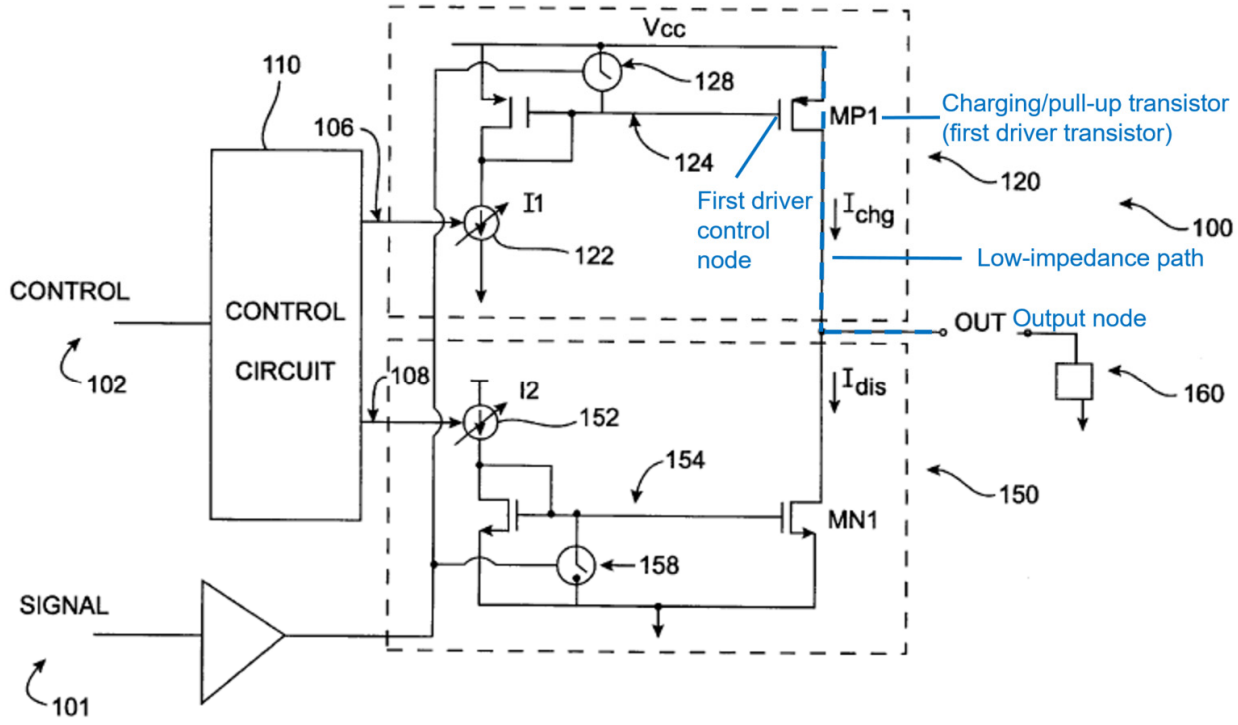



FIG. 1

Ex-1006, Fig. 1

The '455 Patent describes a "driver control node" as a node at which a driver of the output can be controlled (*e.g.,* switched on/off). Ex-1001, 2:62-3:13. MP1's gate is a "first driver control node" because MP1 can be switched on/off by changing its gate voltage. Ex-1006, 2:8-32; 2:22-32, 2:45-65, 3:62-4:9; Ex-1002, ¶64. Thus, Ozguc discloses Element 7[a].

**c. 7[b]: a first switch element coupled between the first driver control node and a first power supply node;**

Ozguc discloses a first switch element (128 in Fig. 1, 228 in Fig. 2) coupled between the first driver control node (MP1's gate) and a first power supply node ($V_{CC}$/$V_{25}$). Ex-1006, 1:66-2-65, 3:7-10, Figs. 1-2; Ex-1002, ¶65. "When the input

signal 101 is high, switch 128 is turned off, allowing the charging transistor MP1 to conduct." *Id.*, 2:24-28.

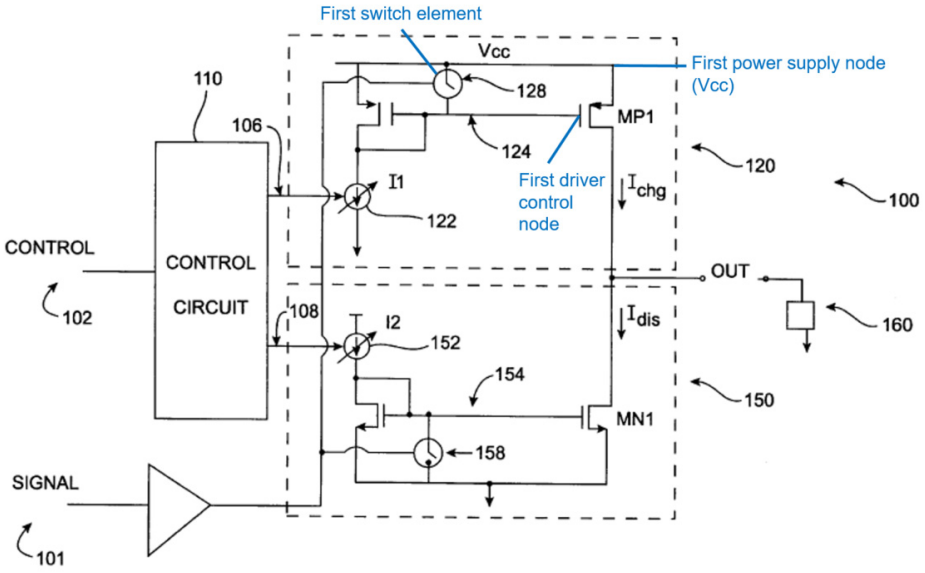



FIG. 1

Ex-1006, Fig. 1

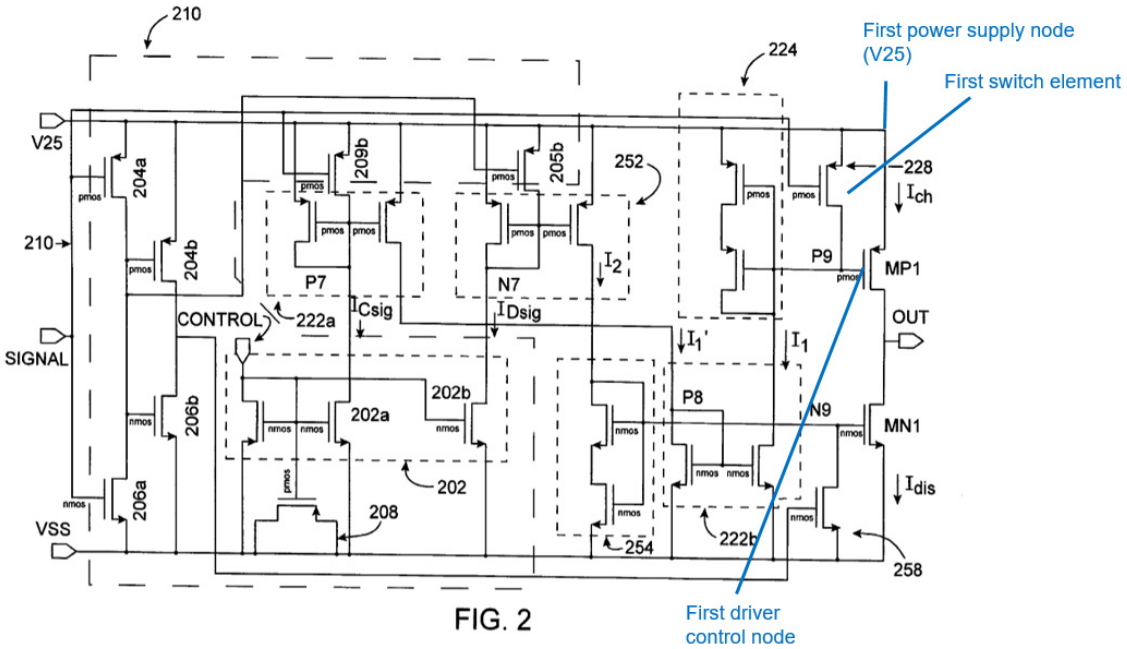



FIG. 2

Ex-1006, Fig. 2

**d. 7[c]: a selectable current source coupled between the first driver control node and a second power supply node, the selectable current source generating a drive current that varies in response to a drive select value,**

Ozguc also discloses a "first adjustable current source" (122 in Fig. 1, 222 in Fig. 2) coupled between the first driver control node (MP1's gate) and a second power supply node (Ground/$V_{SS}$). Ex-1006, 2:1-7, 2:45-3:13, Figs. 1-2.

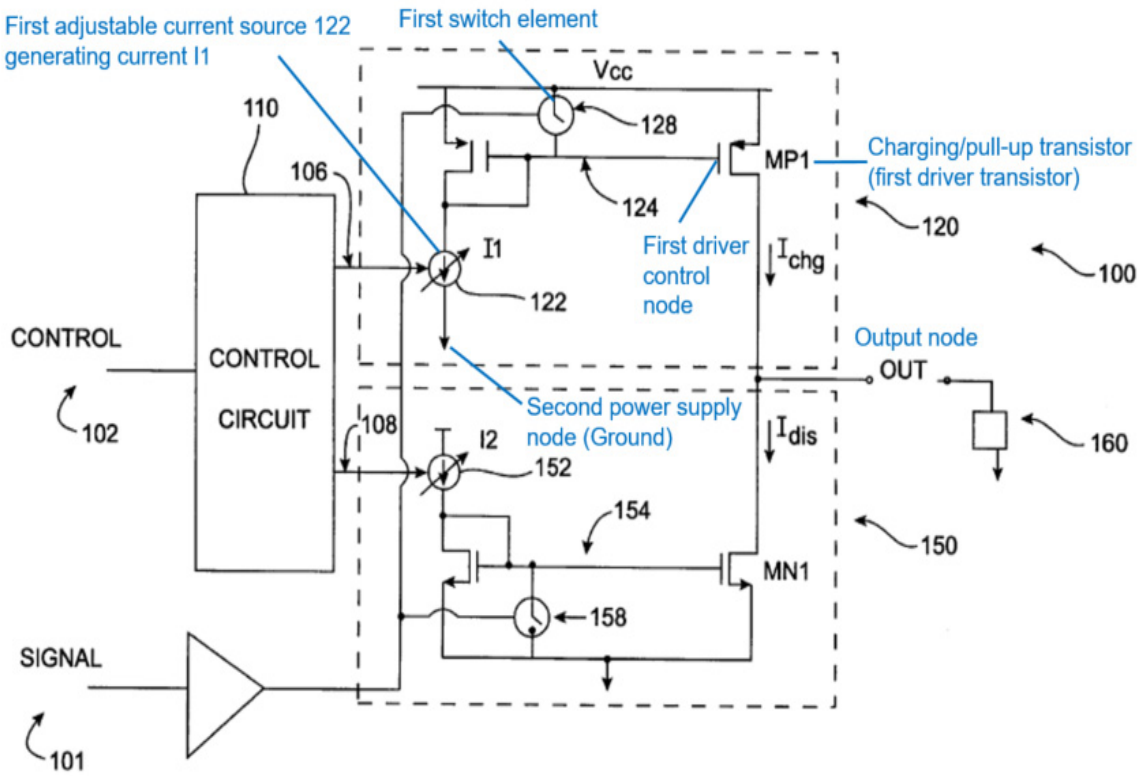


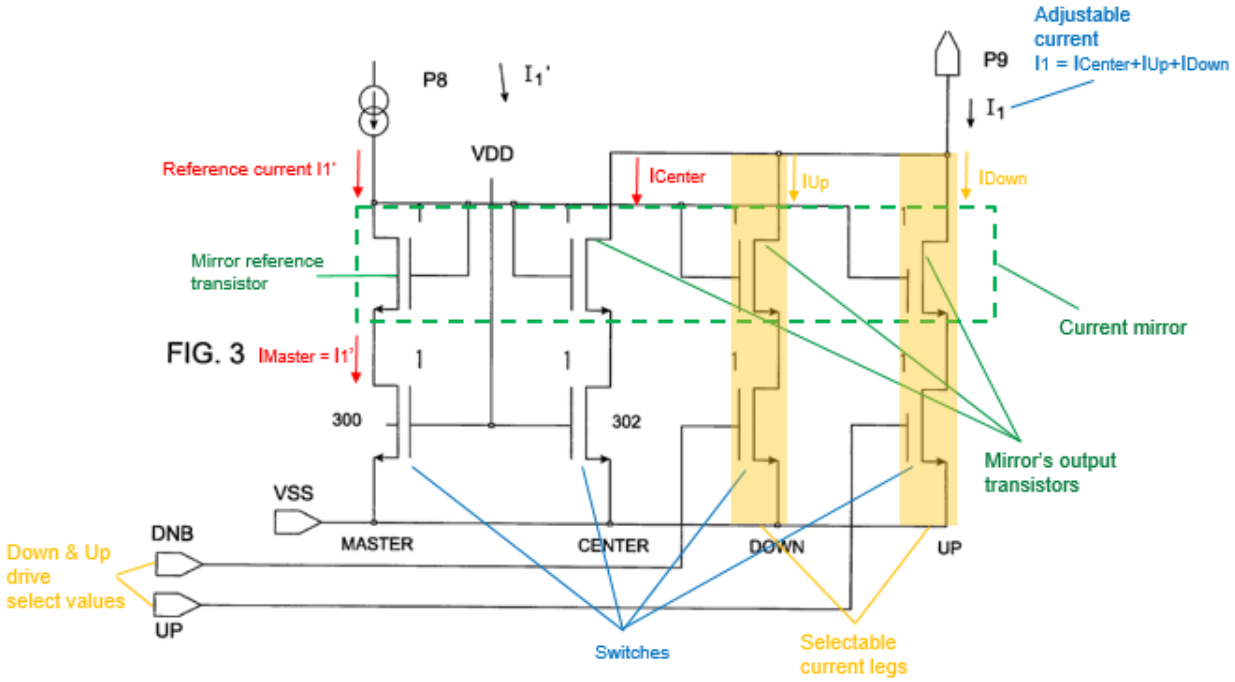

FIG. 1

Ex-1006, Fig. 1

Ozguc discloses that the first adjustable current source 222 (Figure 2) may include the Figure 3 structure. Ex-1006, 3:44-52, 4:10-12. Thus, Ozguc discloses

or renders obvious that the "first adjustable current source 122" (or 222) may include the parallel current legs shown in Figure 3, to adjust the source's generated current ($I_1$) by selectively turning on or off current paths that contribute to $I_1$. *See* Section X.A.1; Ex-1006, 1:55-62, 4:10-12, 4:37-46; Ex-1002, ¶¶67-68. Therefore, Ozguc discloses a "selectable current source" (122/222) because the current ($I_1$) generated by the source (122/222) can be selectively adjusted. *Id.*

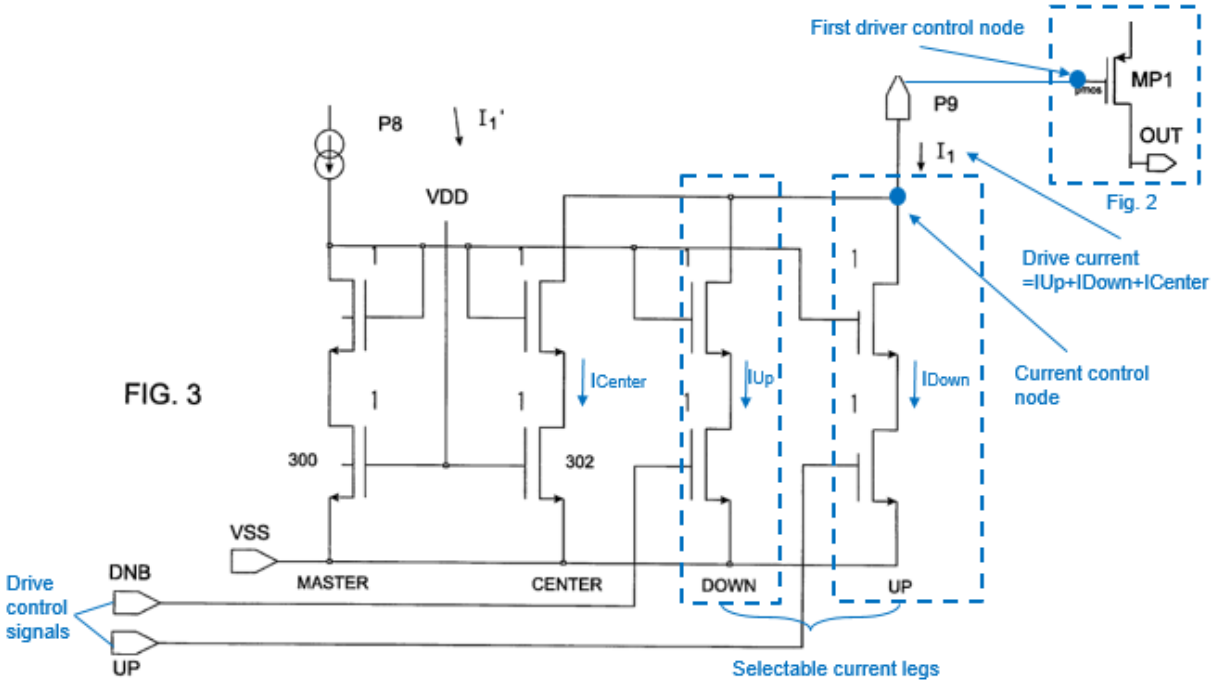
The '455 Patent describes a "drive current" as a current generated by its selectable current source for controlling the first driver transistor to drive the output to a desired value. Ex-1001, 5:11-16, 5:54-6:3. Current $I_1$ shown in Ozguc's Figures 1-3 is a "drive current" because it is generated by the "first adjustable current source" 122/222 and directed to the drive control node (MP1's gate) for controlling the first driver transistor (MP1). Ex-1006, 2:10-14, 4:14-15; *see also* 1:66-2:21, 2:45-3:43, 3:62-4:9, 4:10-58; Ex-1002, ¶¶69-70; Section XI.A.1. Therefore, Ozguc discloses a selectable current source (122/222) that generates a drive current ($I_1$) that varies in response to a drive select value ("DNB" or "UP").




Ex-1006, Fig. 3

**e. 7[d]: wherein the selectable current source includes a plurality of selectable current legs, each connected to a current control node and enabled to provide a current to the current control node in response to a corresponding drive control signal.**

As explained in Section XI.A.1 and for Element 7[c], Ozguc discloses that the selectable current source (*e.g.,* 122/222 in Figs. 1-2) includes selectable current legs (Figure 3, Down and Up legs). Ex-1006, 4:10-36; Ex-1002, ¶71.




Ex-1006, Fig. 3

Element 7[d] further requires that each selectable current leg be connected to "a current control node." The '455 Patent discloses that "a current control node" may be a node (*e.g.,* 230 in Figure 2A) from which the selectable current source (*e.g.,* 114-0) "draw[s]" a variable amount of current to change the "rise time." Ex-1001, 3:40-4:13; Section VII. Ozguc discloses in Figure 3 (above) that the selectable Down and Up current legs merge at a node at the first adjustable current source's output to provide a total current (drive current) that is the sum of the currents flowing through the legs. Ex-1006, 4:10-36, Fig. 3; Ex-1002, ¶¶72-73. This node is a "current control node" because the current ($I_1$) controlled by the

adjustable source is output from this node to the first driver control node (MP1's gate) to turn on MP1 and control it to drive the output to a high voltage value. *Id*.

Accordingly, Ozguc discloses that the first adjustable current source (selectable current source) includes selectable current legs (Up and Down) connected to a current control node (annotated blue dot) and enabled to provide a current ($I_{Up}$ and $I_{Down}$) to the current control node in response to a corresponding drive control signal ("DNB"/"UP" select values). Ex-1006, 4:10-36, Fig. 1 (122), Fig. 2 (222); Ex-1002, ¶¶74-75.

Thus, Ozguc anticipates or renders obvious claim 7.

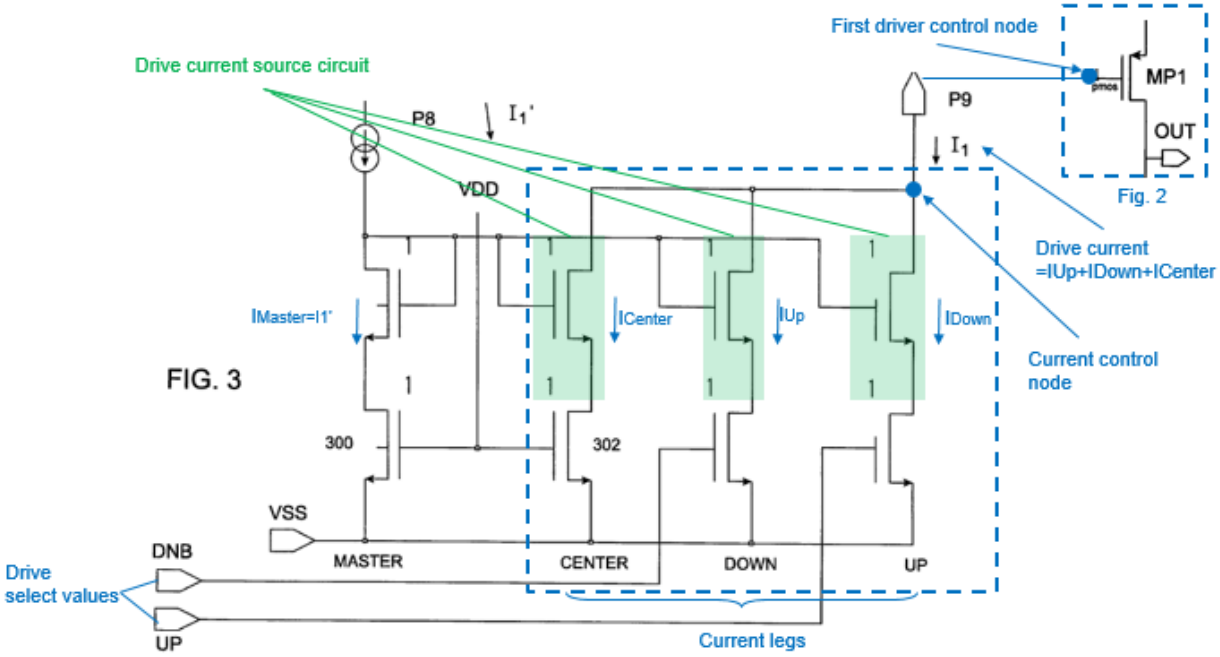
### 3. Claim 8

#### a. 8[a]: The output driver circuit of claim 7, wherein: the selectable current source includes a drive current source circuit,

To the extent this limitation meets Section 112, it is disclosed by or obvious over Ozguc.[6] The upper transistors in Ozguc's Center, Upper, and Down legs form a "drive current source circuit" because each leg provides a current ($I_{Center}$, $I_{Up}$, and $I_{Down}$) that serves as a source current contributing to the total drive current ($I_1$) generated by the first adjustable current source 122/222 (selectable current source)

[6] Because certain terms of claim 8 do not appear in the specification, Petitioner reserves the argument that claim 8 fails to meet Section 112.

for driving the "charging transistor MP1" (first driver transistor). Ex-1006, Fig. 3, 4:10-36; Ex-1002, ¶¶76; Section XI.A.1.




Ex-1006, Fig. 3

Thus, Ozguc discloses or renders obvious Element 8[a].

**a. 8[b]: a first drive current switch element coupled in series with the current source circuit between the first driver control node and the second power supply node.**

As shown below, the '455 Patent describes a switch in each selectable current leg (228) for controlling a component of the drive current ($I_{Out1}$/$I_{Out2}$) in response to drive select values (DRV0/DRV1). Ex-1001, 3:64-4:13.

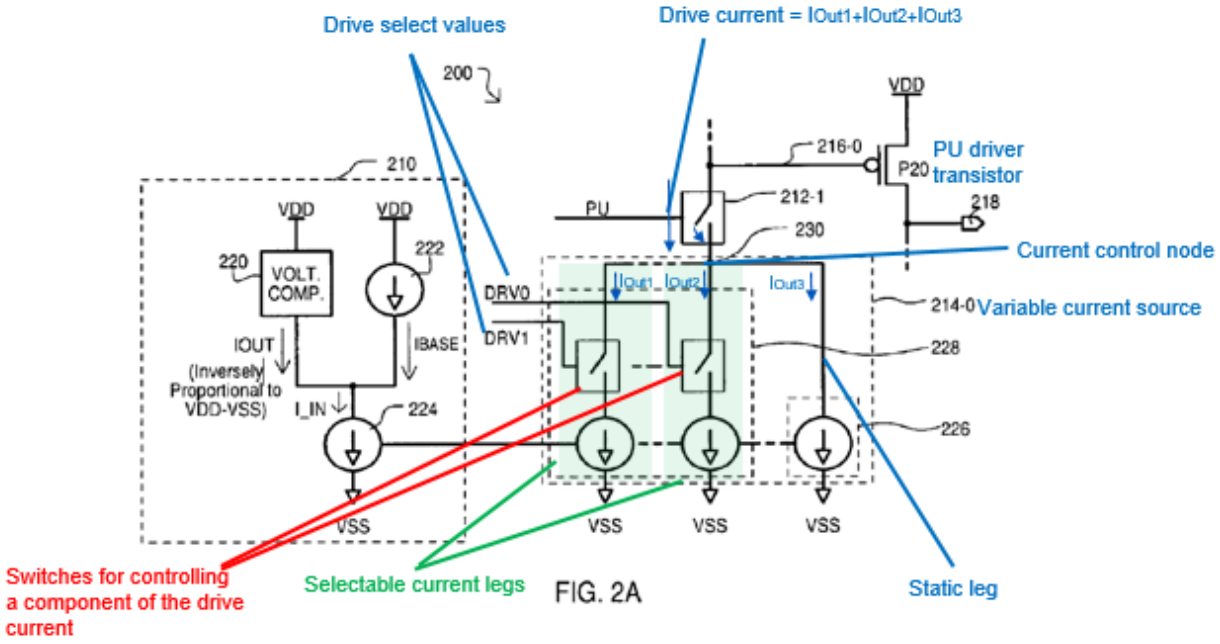
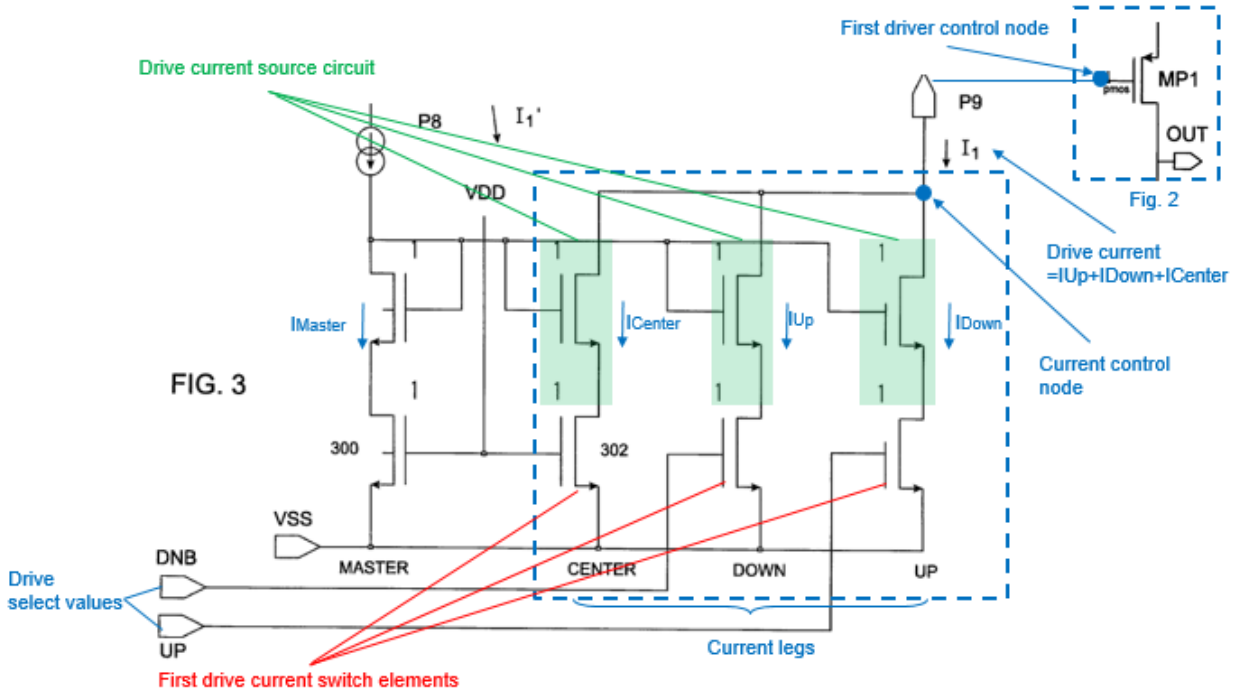



FIG. 2A

Ex-1001, Fig. 2A

Similarly, each lower transistor of Ozguc's Down, Up, and Center legs is "a first drive current switch element" because each can control at least a component (*e.g.*, $I_{Down}$, $I_{Up}$, $I_{Center}$) of the drive current. Ex-1006, Fig. 3, 4:10-36; Ex-1002, ¶¶77-78; Section XI.A.1. Each lower transistor is coupled in series with the current source circuit (the three upper transistors) and positioned between the first driver control node (MP1's gate) and the second power supply node ($V_{SS}$). *Id.* Therefore, claim 8 is anticipated by or obvious over Ozguc.




Ex-1006, Fig. 3

### 4. Claim 10

#### a. 10[a]: The output driver circuit of claim 7, wherein: the plurality of selectable current legs includes a drive current leg that provides a pre-drive current to a drive node,

To the extent this limitation satisfies Section 112, "a drive current leg" can refer to the middle selectable leg shown in the '455 Patent's Figure 2A, "a pre-drive current" can refer to the current in that leg ($I_{Out2}$) which contributes to the

total drive current ($I_{drive}$) output, and "a drive node" can refer to the output node (230) of the source.[7] Ex-1001, 3:44-5:12.

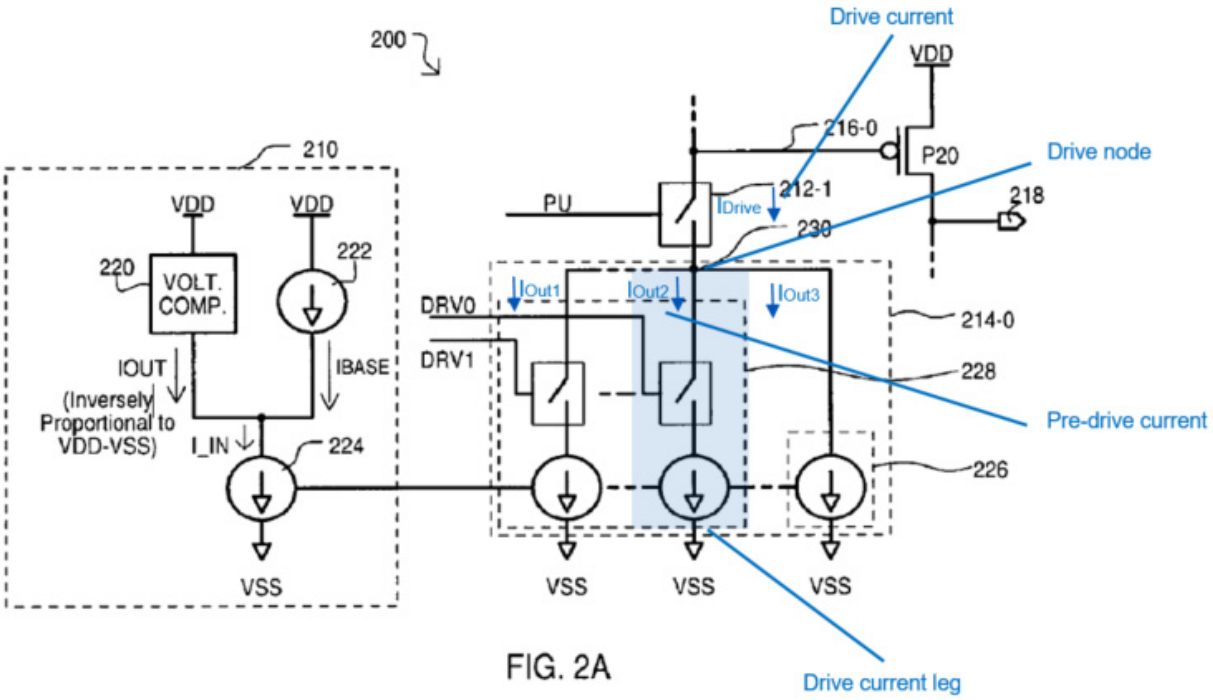



FIG. 2A

Ex-1001, Fig. 2A

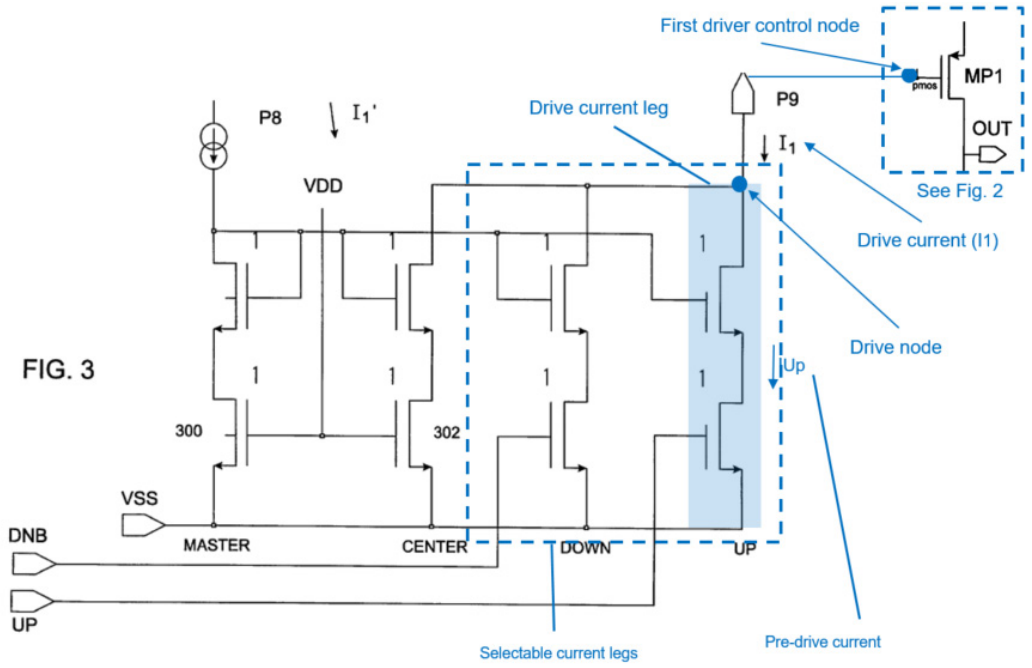
Ozguc discloses a current-leg structure similar to the '455 Patent's Figure 2A structure. Ex-1002, ¶¶79-80. As explained in Section XI.A.1, Ozguc discloses in Figure 3 an adjustable current source that provides an adjustable drive current ($I_1$) that is the sum of the currents in three legs, at least two of which (Down and

[7] Because certain terms of claim 10 do not appear in the specification, Petitioner reserves the argument that claim 10 fails to meet Section 112.

Up) being selectable. At least the Up leg is "a drive current leg" because it provides a current ($I_{Up}$) that is selectable and "contributes to … [the drive] current $I_1$." Ex-1006, 4:17-46; Figs. 2-3; Ex-1002, ¶¶79-80. $I_{Up}$ is a "pre-drive current" because it is generated before generation of the drive current ($I_1$) and "contribute[s]" to the drive current. *Id.*

The source's output node (blue dot in Figure 3)—at which the currents in the Center, Up, and Down legs are added—is a "drive node" because a total "drive current" is formed at this node for driving the first driver transistor (MP1). Ex-1002, ¶¶81-82; Ex-1006, 4:10-36, Figs. 1-2.

Therefore, Ozguc discloses Element 10[a].




Ex-1006, Fig. 3

**b. 10[b]: a drive strength modulator that selectively shunts current from the drive node in response to a drive strength control signal, and**

The '455 Patent discloses an example of "a drive strength modulator" (408) in Figure 4. Ex-1001, 5:17-6:3. Modulator 408 is shown as a selectable current leg that selectively changes (modulates) the drive current ("$I_d/I_{drive}$") used for driving the output (422) to a desired value.[8] Ex-1001, 5:54-6:3, 6:24-26. The drive current ($I_d$) output from drive node 420 is the net sum of the current provided to the node (input current $I_2$) and the current ($I_{DSM}$) drawn by modulator 408 from the node. *Id.* Modulator 408 includes "NFETs N49 and N50 arranged in series with one another between node 420 and a low power supply node [VSS]." *Id.*, 5:61-6:3. N49's gate is connected to a drive mode select value ("DRIVEMODE"), which selectively enables the modulator to shunt (draw) a current ($I_{DSM}$) from the drive node (420), which in turn changes the total drive current ("$I_d/I_{drive}$"). *Id.*; Ex-1002, ¶83. For example, "when drive strength modulator [408] is disabled (NFET N49 off)," $I_d$ is equal to the input current ($I_2$), and therefore "$I_{drive}$ can essentially mirror [input]

[8] A current mirror formed by transistors N47 and N48 uses $I_d$ as a reference current to output a proportional current ($I_{drive}$) that is directed to the "output driver section 416." Ex-1001, 5:54-6:3, 6:24-26; Ex-1002, ¶83. $I_{drive}$ is equal to $I_d$ if the transistors (N47 and N48) have the same size. *Id.*; *see also* Section VI.D.

current $I_2$." Ex-1001, 5:62-6:3. "In contrast, when drive strength modulator is enabled (NFET N49 on), … $I_{drive}$ can be reduced" ($I_{drive} = I_2 - I_{DSM}$). *Id.*

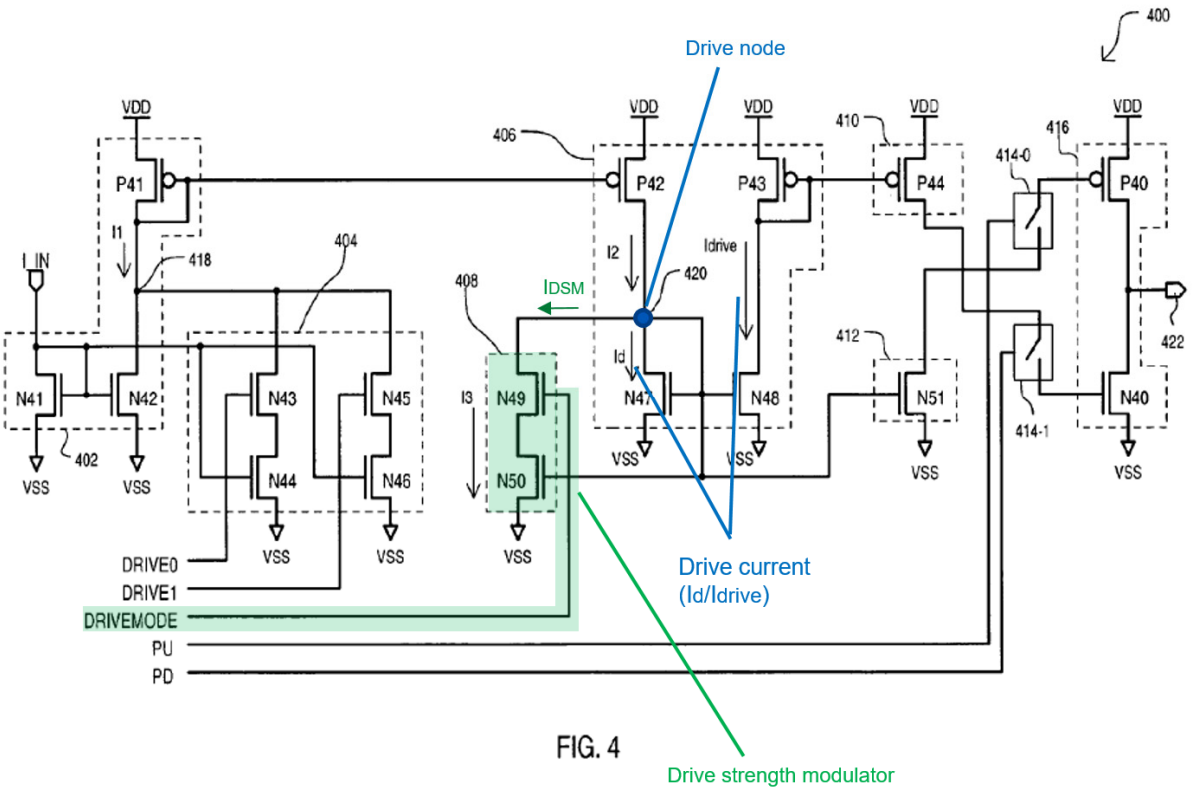
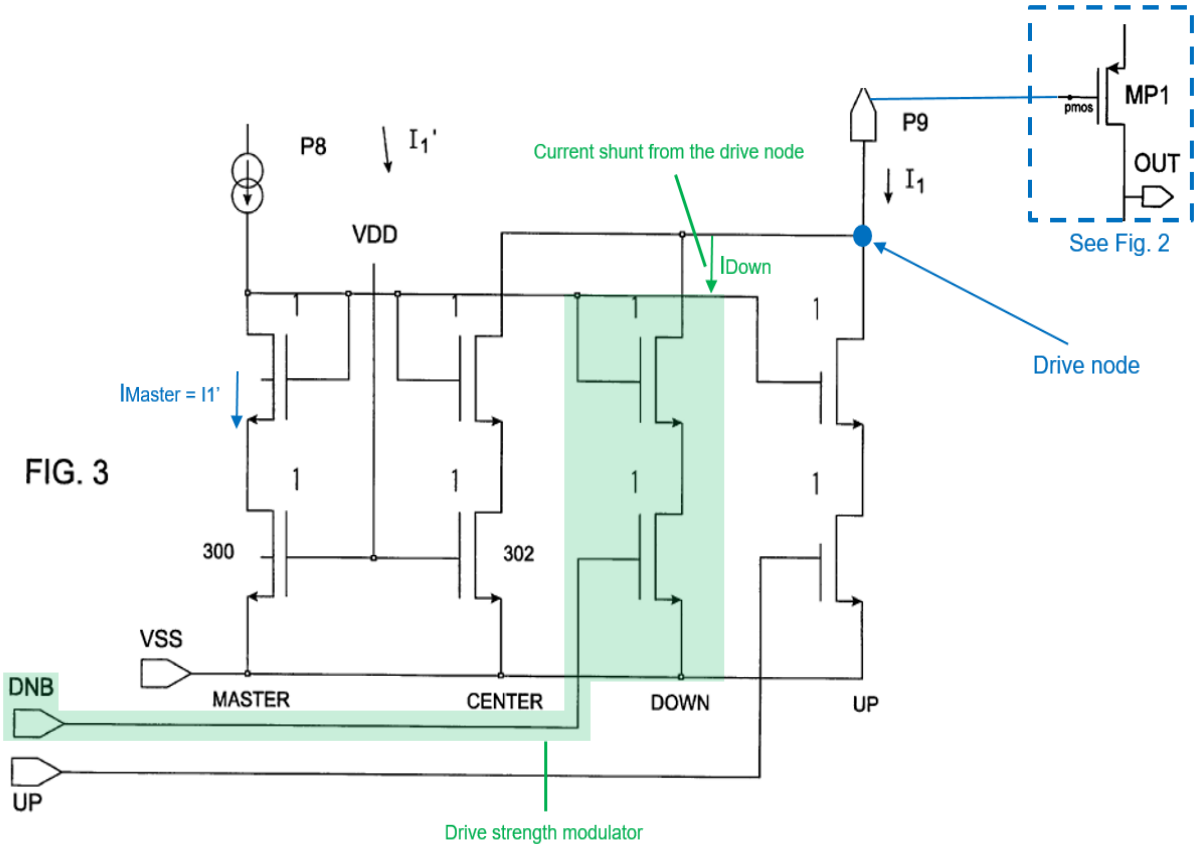



FIG. 4

Ex-1001, Fig. 4

Ozguc discloses that at least its Down leg has the same structure and functions as the drive strength modulator disclosed in the '455 Patent. Ex-1006, Fig. 3, 4:10-36; Ex-1002, ¶84. Similar to the structure shown above, Ozguc's Down leg includes two NMOS transistors in series between the drive node (annotated blue dot) and a low power supply node (VSS). Ex-1006, 4:23-46, Fig. 3. The bottom NMOS's gate is connected to a drive mode select value ("DNB") to selectively enable the Down leg to draw a current ($I_{Down}$) from the drive node. *Id.*

The current in the Down leg ($I_{Down}$) is selectively turned on or off using the "DNB" value, which in turn modifies the drive current $I_1$. *Id.* Thus, the Down leg and DNB drive select circuit collectively constitute a "drive strength modulator" because they selectively modulate (change) the drive strength (*e.g.*, the current for driving the output to a desired value). *Id.*, 4:10-36, Figs. 1-3; Ex-1002, ¶84.




Ex-1006, Fig. 3

Because the Down current is drawn from the drive node and can be selectively adjusted, Ozguc discloses that its drive strength modulator selectively shunts current ($I_{Down}$) from the drive node in response to a drive strength control

signal (DNB select value). Ex-1002, ¶85. Therefore, Ozguc discloses Element 10[b].

**c. 10[c]: the drive current is proportional to the current at the drive node.**

To the extent this limitation satisfies Section 112, it is disclosed by or obvious over Ozguc. "[T]he current at the drive node" lacks antecedent basis.[9] It can refer to the "pre-drive current [provided] to a drive node" of Element 10[a], or to the selectable currents, *e.g.,* $I_{Out1}$ or $I_{Out2}$, in Figure 2A below. Ex-1001, 3:44-4:13. Ozguc discloses Element 10[c] under any interpretation because it discloses a selectable circuit that performs the same function as the one shown in '455 Patent's Figure 2A. Ex-1002, ¶86.

[9] Petitioner reserves the argument that this limitation fails to meet Section 112.

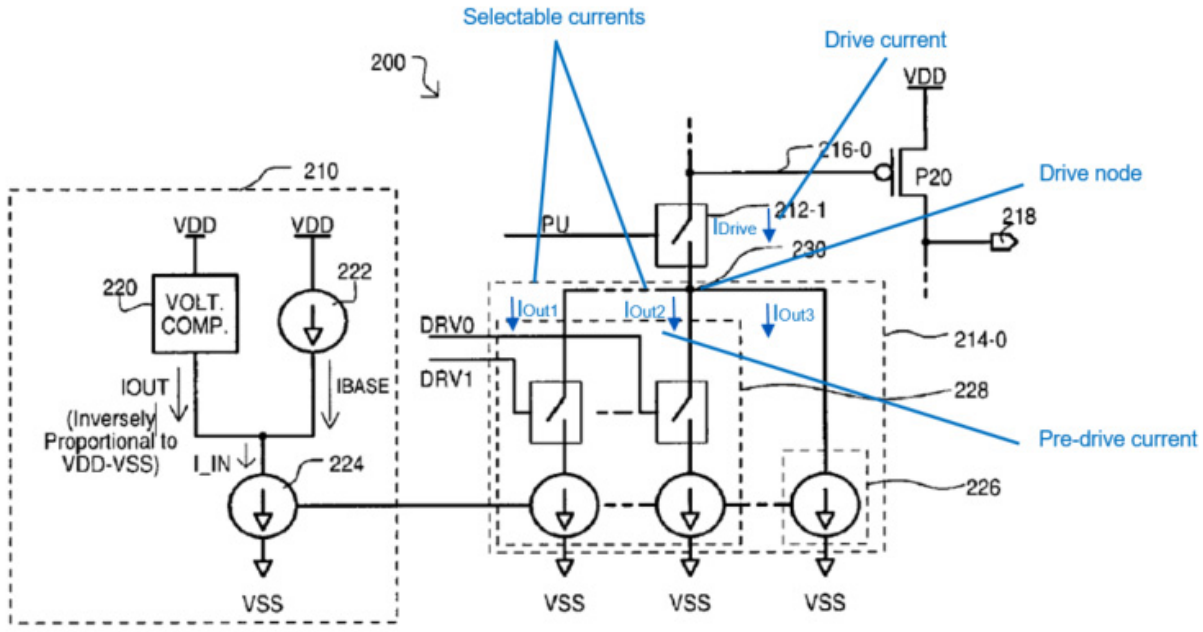



FIG. 2A

Ex-1001, Fig. 2A

Ozguc discloses that the drive current ($I_1$) is the sum of currents in Down, Up, and Center legs, and each leg may mirror the reference current $I_1'$. Ex-1006, 4:10-44. If "the current at the drive node" refers to the "pre-drive current" of Element 10[a], $I_{Up}$ meets this limitation, as described above. Because $I_{Up}$ mirrors reference current $I_1'$, and because the drive current ($I_1$) is proportional to $I_1'$, $I_1$ is also proportional to $I_{Up}$ ("the pre-drive current"). Ex-1002, ¶87.

If "the current at the drive node" refers to the selectable currents at the drive node, each selectable current ($I_{Up}$ and $I_{Down}$) drawn from the drive node is a "current at the drive node." Because each of $I_{Up}$ and $I_{Down}$ is proportional to $I_1'$, and

because the drive current ($I_1$) is proportional to $I_1$', $I_1$ is also proportional to each of $I_{Up}$ and $I_{Down}$. Ex-1002, ¶¶88-89.

Therefore, claim 10 is anticipated by or obvious over Ozguc.

**5. Claim 13**

**a. 13: The output driver circuit of claim 7, further including: a control logic circuit that selectively enables the first switch element and selectable current source in response to at least one input signal.**

Ozguc discloses a control circuit (*e.g.*, 110/210 in Figs. 1-2) that selectively enables the first switch element (128/228) and first adjustable current source (122/222) in response to at least one input signal generated by the control circuit. Ex-1006, 2:9-14, 2:45-3:29, 4:10-36, Figs. 1-3; Ex-1002, ¶90.

First, as shown below, the control circuit 210 selectively enables (switches on/off) PMOS switch 228 (first switch element) in response to the input "SIGNAL." Ex-1006, 3:7-13; Ex-1002, ¶91. In the pull-up example below, the control circuit (210) shuts off switch 228 by pulling up its gate voltage as the input rises. *Id.*; Ex-1006, 3:64-4:12.

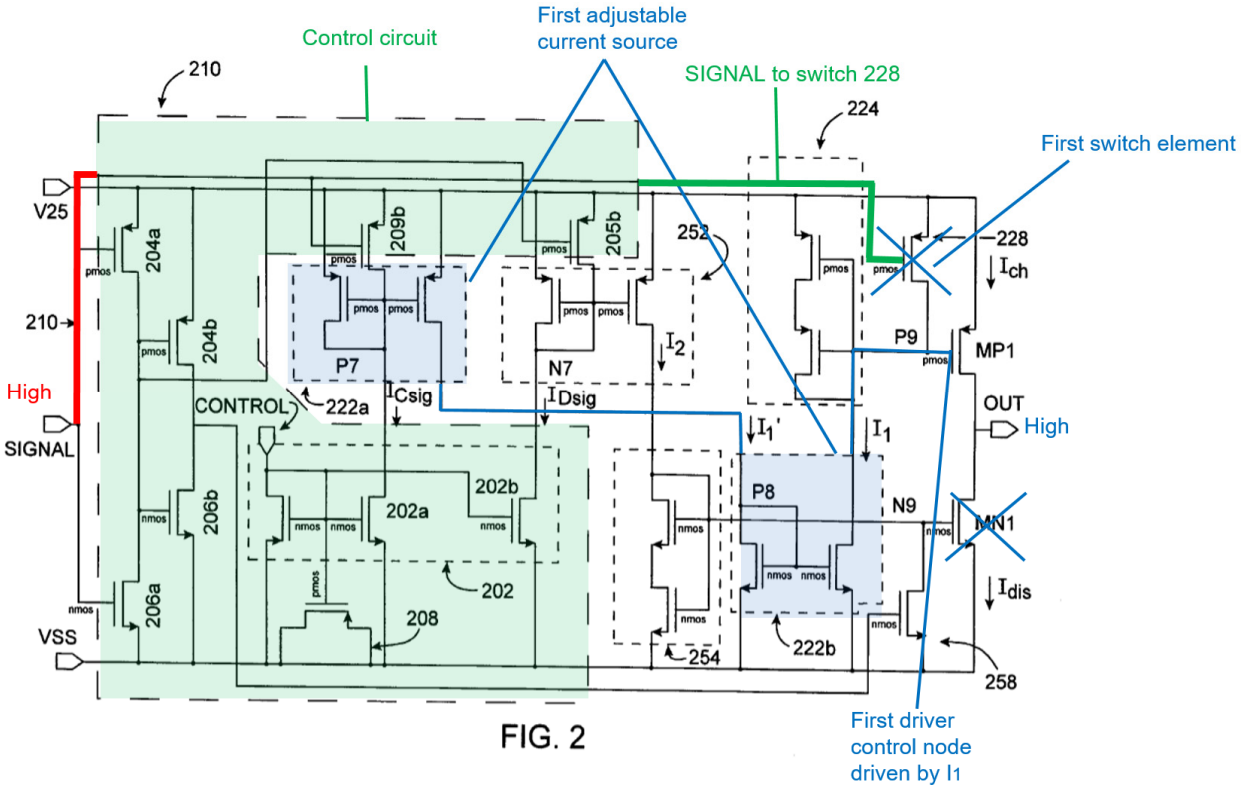



FIG. 2

Ex-1006, Fig. 2

Ozguc also discloses that "the control circuit 110 [Figure 1] receives a control [current] signal 102, and in response, produces a charging signal 106" "supplied to the first adjustable current source 122" to selectively enable it to "produce[] a first reference current $I_1$." Ex-1006, 2:8-14; Ex-1002, ¶¶92-94. The control circuit 220 in Figure 2 similarly enables the first adjustable current source 222 in response to a received "CONTROL" current signal. *Id.*, 2:66-3:13, 3:20-3:29; 3:44-4:9.

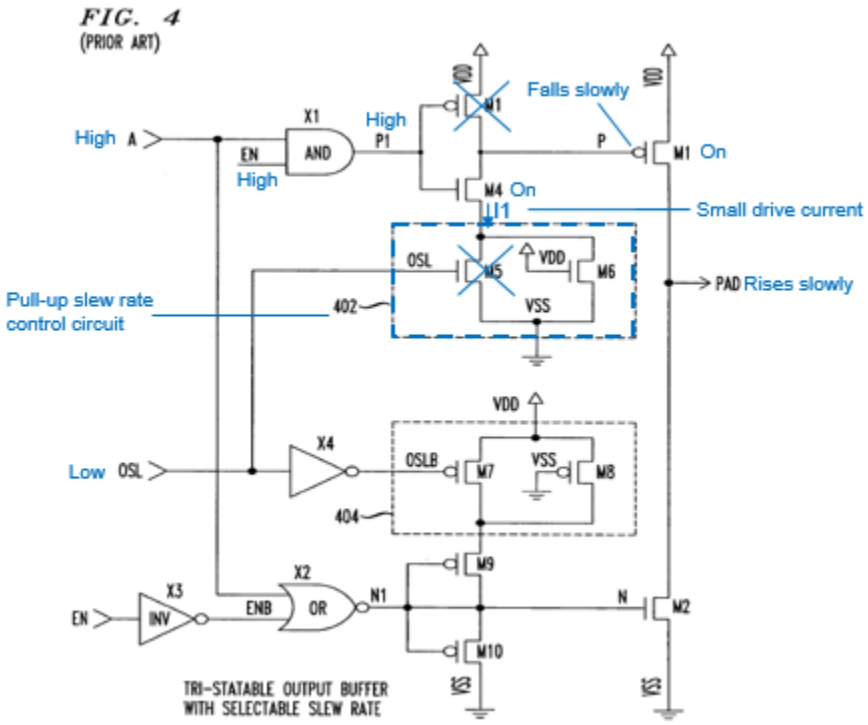
Thus, claim 13 is anticipated by or obvious over Ozguc.

## B. Ground 3: Claims 7, 8, and 10-13 are obvious over Ozguc and Huber

### 1. Huber

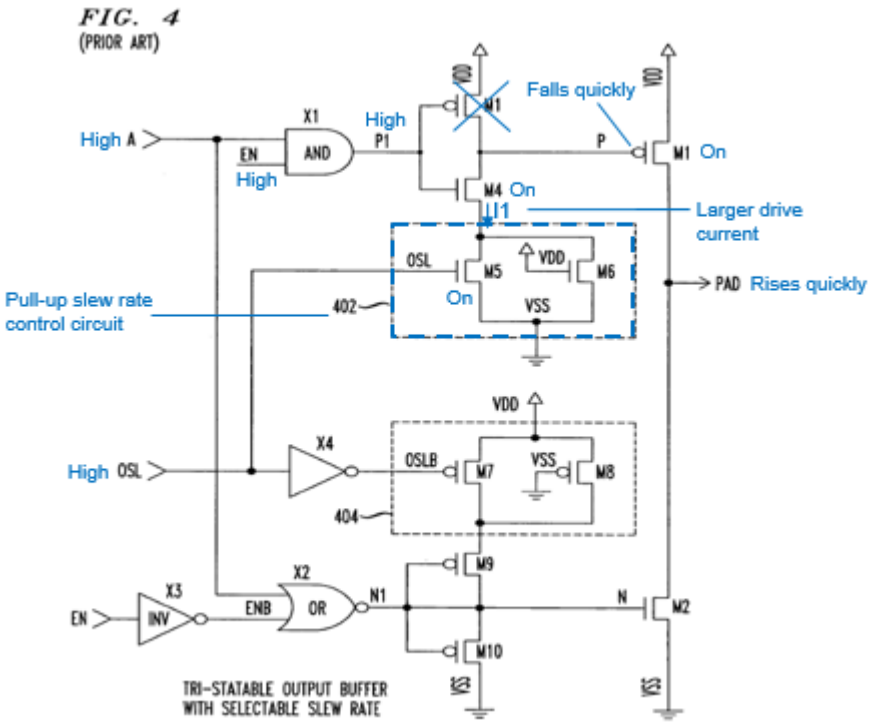
Huber was filed July 15, 2004, qualifying as §102(e) art.

Huber discloses a "buffer" that adjusts the slew rate or transition time of the output. Ex-1007, Abstract. Figure 4 below is annotated to show the pull-up operation when the buffer is enabled (EN=high) and selected to operate with a slower slew rate ("OSL"=low). *Id.*, 2:56-58. Because both inputs of the AND gate (X1) are high, M4 turns on to allow the pull-up "slew rate control circuit" (402) to draw current. *Id.*, 1:55-2:12, 2:44-3:6. Because the gate of a large NMOS transistor (M5) is connected to OSL that is set to low, M5 turns off. Ex-1007, 2:51-3:28. A small "transistor M6" draws a small current from the gate of the pull-up transistor (M1). *Id.*, 3:1-6. Thus, M1 slowly turns on and pulls up the output (PAD) after a relatively long rise time. *Id.*, 3:17-28; Ex-1002, ¶95.



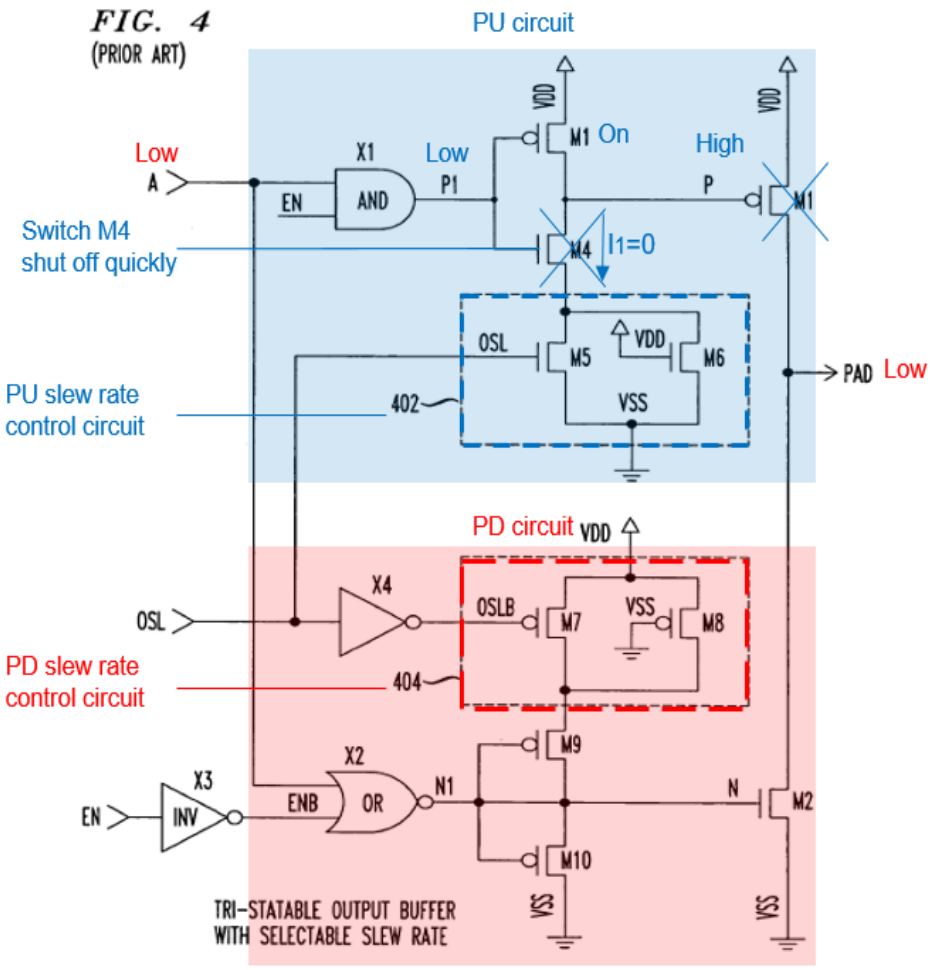

Ex-1007, Fig. 4

As shown below, when OSL is set to high, a larger transistor M5 turns on to draw a greater current, resulting in a shorter rise time. Ex-1007, 2:5-3:28; Ex-1002, ¶96.




Ex-1007, Figure 4

As shown below, during pull-down, switch (M4) quickly turns off and shuts off the current generated by the pull-up slew rate control circuit (402) to prevent interference with the pull-down operation. Ex-1007, Fig. 4, 3:7-28; 1:53-2:22; Ex-1002, ¶97.




Ex-1007, Fig. 4

The M9 switch in the pull-down circuit is similarly configured to quickly shut off the pull-down current during the pull-up operation. Ex-1007, 1:55-2:10, 2:13-22, 2:47-50, 3:50-57, Figure 4; Ex-1002, ¶98.

### 2. Obviousness Combination of Ozguc and Huber

Ozguc and Huber are in a common field of endeavor ("design of integrated circuits") and are directed to the same type of circuit ("buffer circuit"). *Compare* Ex-1006, Abstract, 1:17-19 *with* Ex-1007, Abstract, 1:7. Both use similar circuit

components (*e.g.,* selectable current legs) and techniques (*e.g.,* current adjustment) to achieve similar objectives (*e.g.,* adjusting the output transition rate). *Compare* Ex-1006, Fig. 3, 4:28-36 *with* Ex-1007, Fig. 4; 2:44-3:57; Ex-1002, ¶99. Given these similarities, a POSITA would have found it obvious to combine Ozguc and Huber because such a combination represents the application of a known technique to a similar device that yields predictable results. *Id*.

A POSITA would have also been motivated to modify Ozguc's buffer circuit in view of Huber to improve performance, including (1) the buffer's ability to control the rise and fall times of the output without unintended delays, and (2) power efficiency. Ex-1002, ¶100.

These performance benefits depend on how fast a buffer can alternate between the pull-up and pull-down operations. *Id.*, ¶101. Because the pull-down and pull-up circuits pull the output in opposite directions, it is desirable to alternate between pull-down and pull-up operations with minimal overlap. *Id.* For example, if after the input falls, the pull-up circuit is not completely shut off until after an unintended delay ("shut-off delay"), the pull-up circuit may interfere with the pull-down operation causing an unintended delay to the transition of the input to a low value. *Id.* This delay also generates an unnecessary pull-up current and wastes power. *Id.*

A POSITA would have understood that Ozguc's switching mechanism shuts off the pull-up and pull-down currents after a delay following transition of the input to low and high values, respectively, as explained below. Ex-1002, ¶¶102-103. Thus, a POSITA would have been motivated to apply Huber's efficient shut-off design to Ozguc's buffer to reduce its shut-off delay. *Id.*

**a. Ozguc's Shut-off Delay**

An example of the shut-off delay of Ozguc's switching mechanism is explained using annotated Figure 2 below. When the input ("SIGNAL") falls, the switching mechanism shuts off the pull-up drive current ($I_1$) by performing the steps annotated below. Ex-1002, ¶103; Ex-1006, 1:66-2:43; 2:44-3:61; 4:10-4:46. First, PMOS transistor (209b) turns on. Ex-1006, 3:14-4:9; Figs. 1-3. Second, PMOS transistor (209b) pulls up the gates of both transistors of the "first current mirror" (222a) to turn both off. *Id.* Third, as the "first current mirror" (222a) switches off, its output current (reference current $I_1'$) is shut off. *Id.* Lastly, $I_1$ shuts off as it mirrors $I_1'$. *Id.; see also* 4:10-46; Ex-1002, ¶103. Because Ozguc's switching mechanism involves a chain of circuit elements, the pull-up drive current ($I_1$) does not shut off immediately. *Id.* This shut-off delay leads to potential power waste and unintended delays in output transition. *Id.*

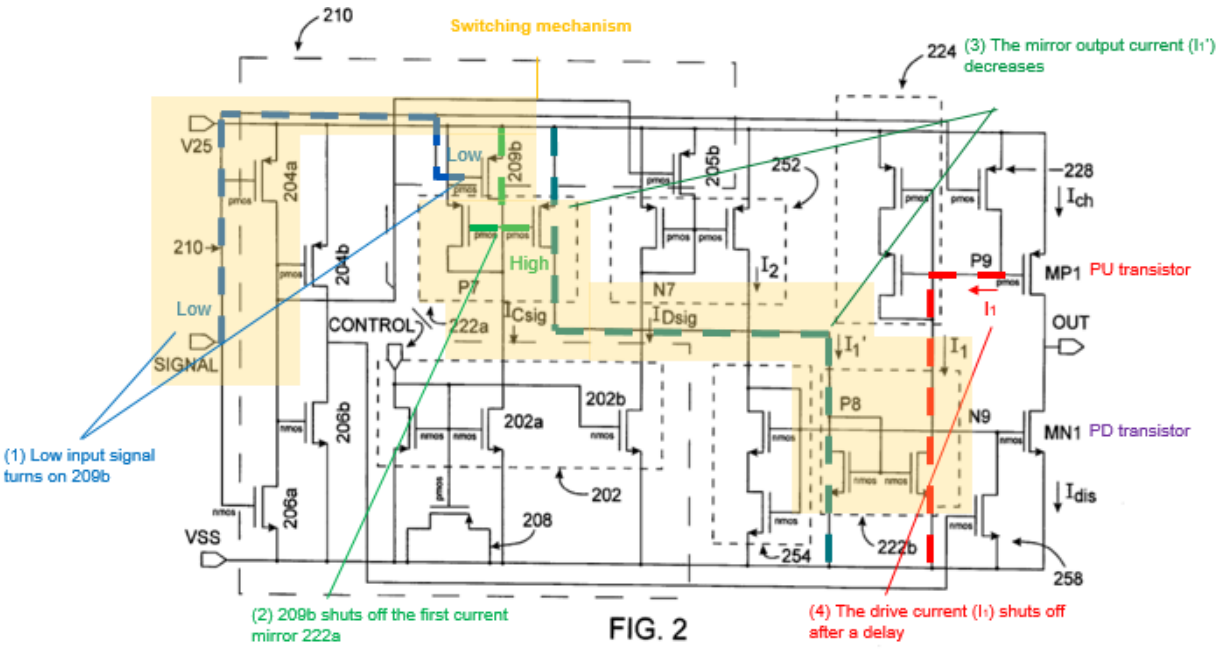



FIG. 2

Ex-1006, Fig. 2

**b. Adding Huber's M4 Switch to Ozguc to Minimize Shut-off Delay**

Huber discloses a switch (M4) that "quickly" shuts off the pull-up current ($I_1$) when the input falls, which (1) minimizes interference with the pull-down circuit, allowing it to "***pull[] the output signal PAD LOW quickly***"; and (2) reduces the pull-up circuit's power waste by avoiding a pull-up current during pull-down. Ex-1007, 6:6-12, Fig. 4; *see also* 1:53-2:22, 3:17-3:57, Figs. 1-3; Ex-1002, ¶104. Accordingly, a POSITA would have been motivated to add Huber's switch to Ozguc's pull-up circuit to reduce power consumption and minimize shut-off delay. *Id.*

Examples of the Ozguc-Huber modification are annotated in Ozguc's Figures 1-3 below. Because Huber discloses positioning the M4 switch at the output of the pull-up slew rate control circuit to "quickly" shut off the pull-up current, a POSITA would have been motivated to similarly place the M4 switch at the output of Ozguc's first adjustable current supply (122/222) to shut off the pull-up current ($I_1$) with minimal delay. Ex-1007, 6:6-12, Fig. 4; 1:52-2:32, 3:17-28, Figs. 1-3; Ex-1002, ¶105.[10] In view of Huber, a POSITA would have also been motivated to connect the M4 switch's gate directly (or via a logic gate) to the input ("SIGNAL") of Ozguc's buffer to minimize delay in controlling the switch. *Id.*

[10] Ozguc's existing switching mechanism is not removed because it is used for other purposes during the pull-up operation (*e.g.,* for adjusting the pull-up drive current ($I_1$)), as described in Section XI.A.1. Ex-1002, ¶105.

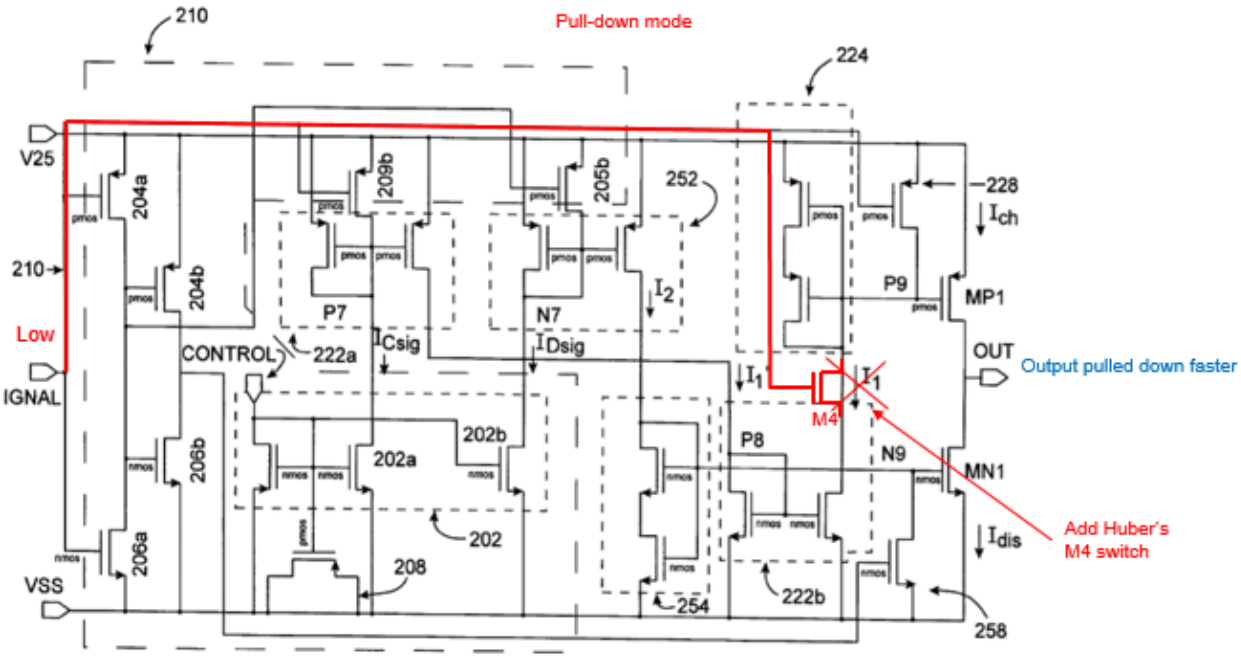



FIG. 2

Ex-1006, Fig. 2 (modified)

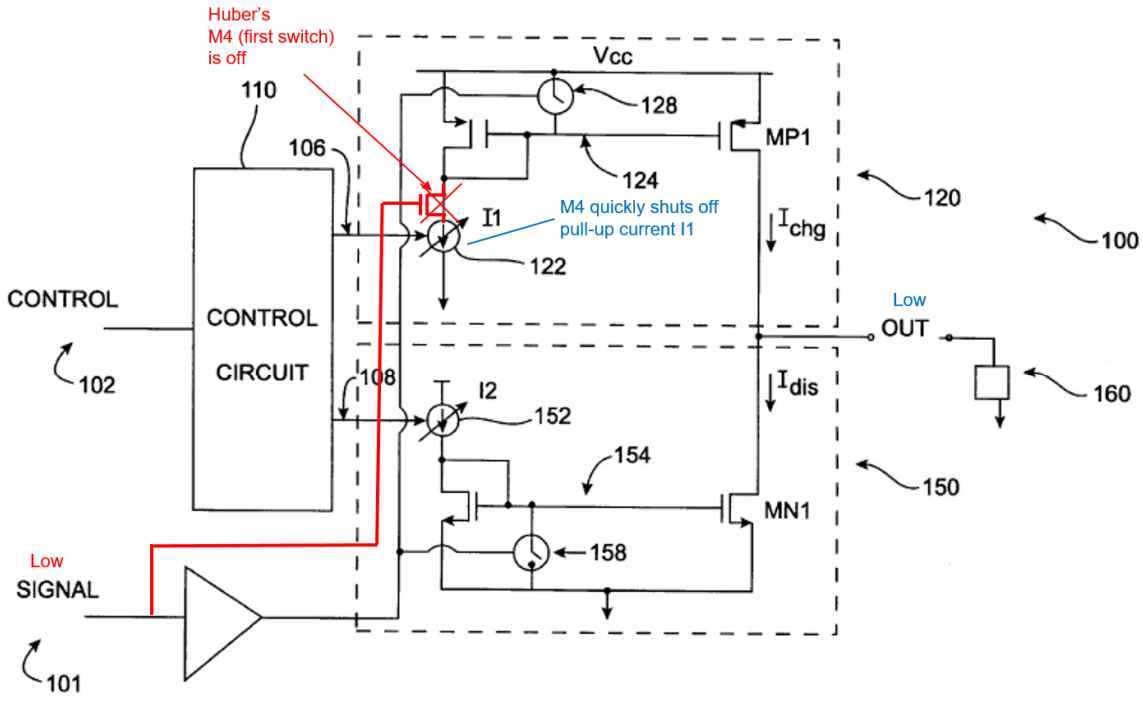
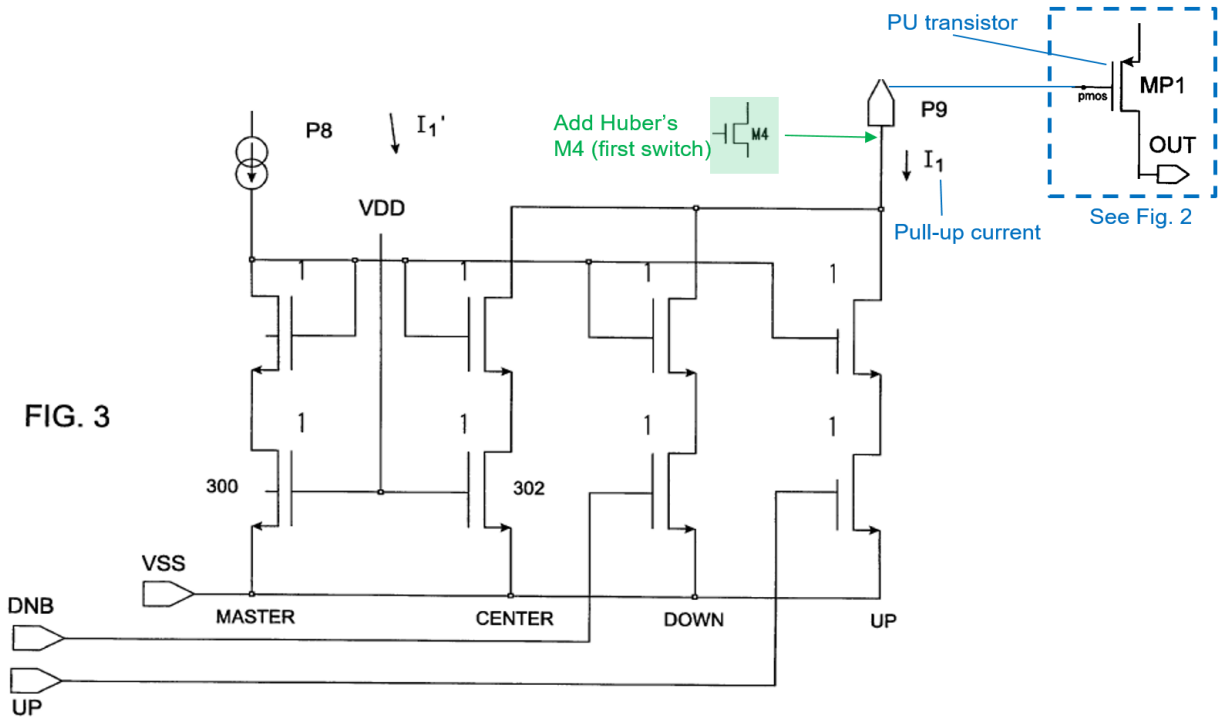



FIG. 1

Ex-1006, Fig. 1 (modified)




Ex-1006, Fig. 3 (modified)

A POSITA would have been motivated to modify Ozguc's buffer circuit in view of Huber to add a switch at the adjustable current supply's output to improve (1) the buffer's ability to control the fall time without unintended delays and (2) the pull-up circuit's power efficiency. Ex-1002, ¶106.

### c. Adding Huber's M9 Switch to Ozguc to Minimize Shut-off Delay

For the same reasons, a POSITA would have been motivated to add Huber's pull-down switch (M9) at the output of Ozguc's second/pull-down adjustable current source (152) to allow the buffer to quickly shut off pull-down current ($I_2$) when the input ("SIGNAL") rises, as shown in Ozguc's modified Figure 1-2 below. Ex-1007, 1:55-2:10, 2:13-22, 2:47-50, 3:50-57, Figs. 3-4; Ex-1002, ¶107.

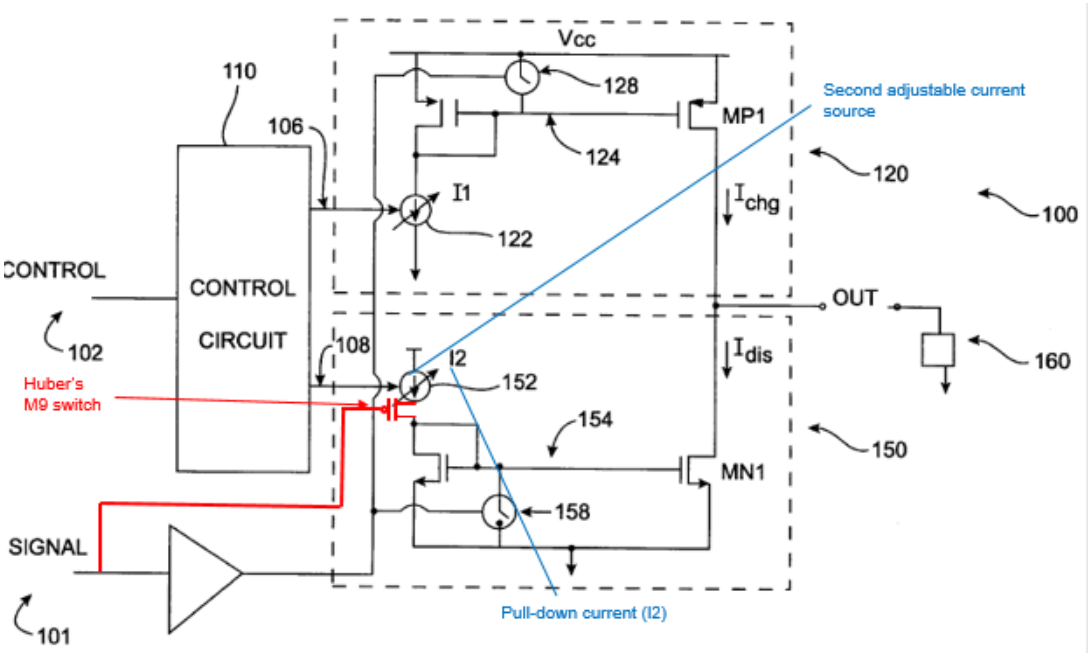



FIG. 1

Ex-1006, Fig. 1 (modified)

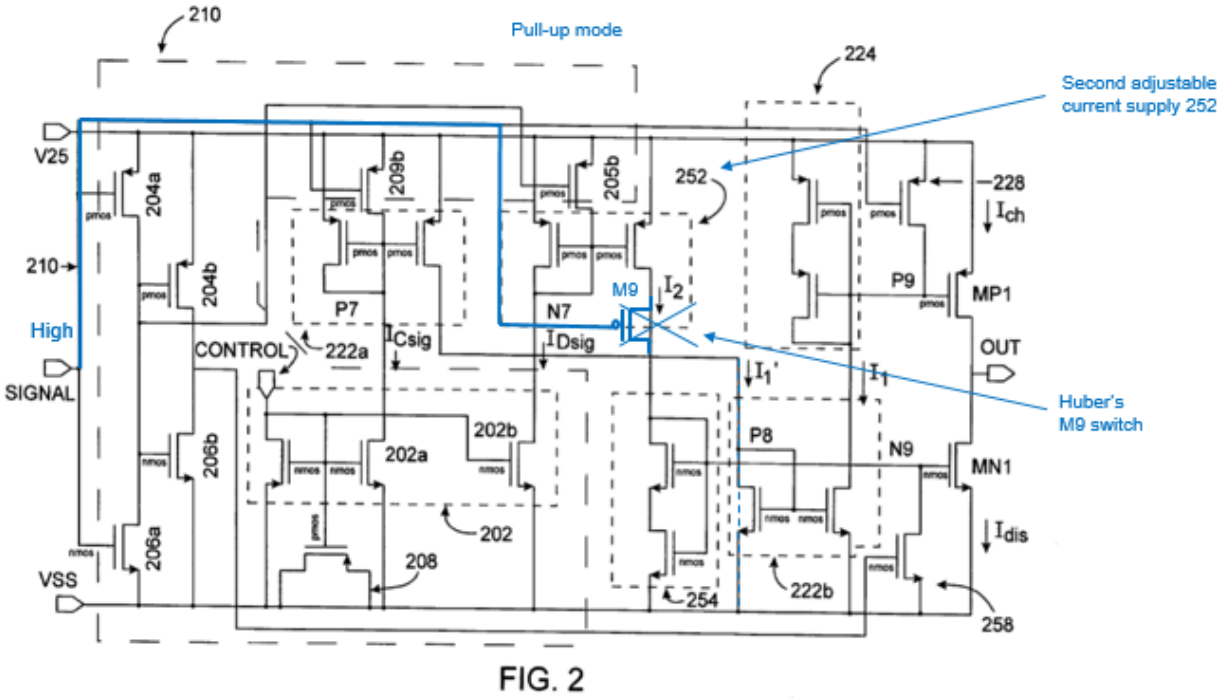



FIG. 2

Ex-1006, Fig. 2 (modified)

### 3. Claim 7

Ozguc discloses Elements 7[pre]-[d] as explained above in Section XI.A.2.

In the event Patent Owner argues that Element 7[d]'s "current control node" must be separated from the "first driver control node" by a circuit element (*e.g.,* switch 212-1 in Figure 2A below), Element 7[d] is obvious over Ozguc and Huber. As explained in Section XI.B.2, a POSITA would have found it obvious to add Huber's M4 switch above the current control node. Ex-1002, ¶109; Ex-1006, Fig. 3. Under this modification, Ozguc's "current control node" is separated from the "first driver control node" by Huber's M4 switch. Thus, under Patent Owner's potential interpretation, Element 7[d] is obvious over Ozguc and Huber.

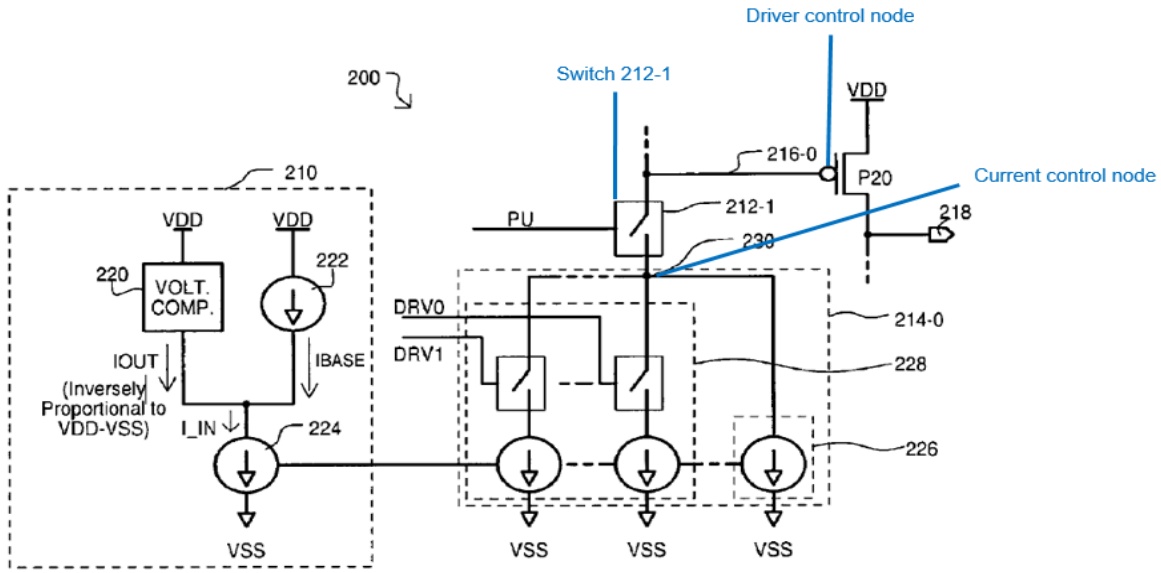
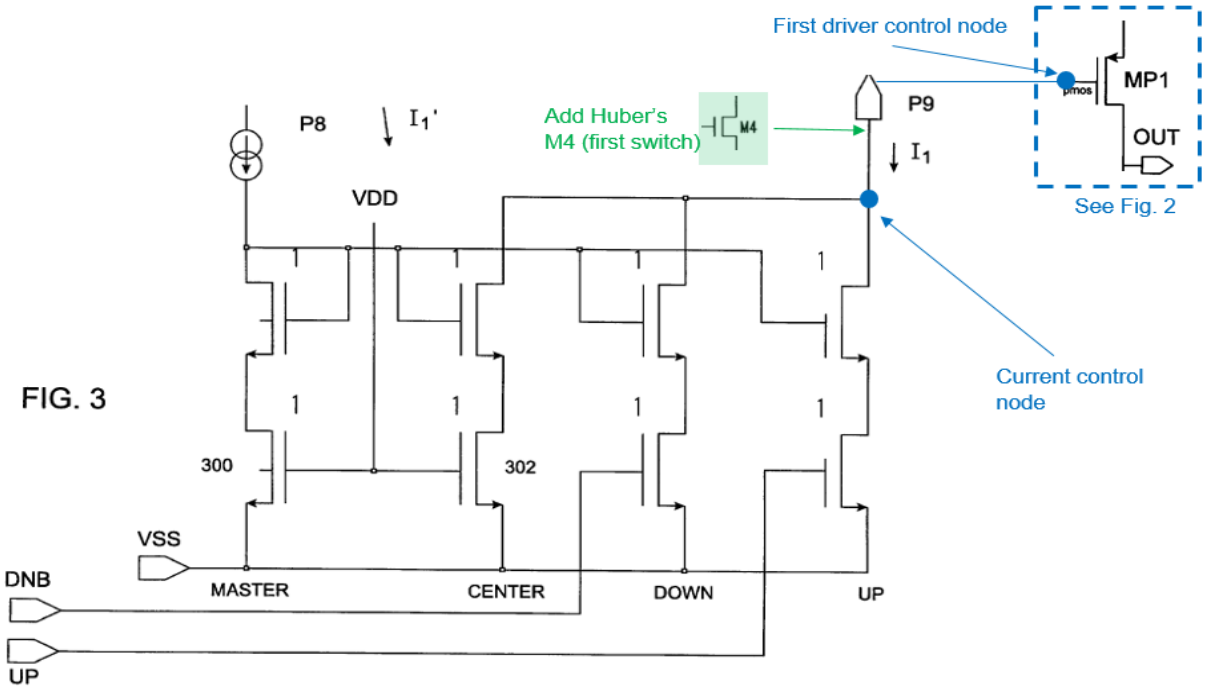



FIG. 2A

Ex-1001, Fig. 2A




Ex-1006, Fig. 3

#### 4. Claims 8, 10, and 13

Ozguc discloses the limitations recited by dependent claims 8, 10, and 13, for the reasons stated for Grounds 1 and 2 in Sections XI.A.3-5. Thus, these claims are obvious over Ozguc and Huber.

#### 5. Claim 11

##### a. 11[pre]: An output driver circuit, comprising:

To the extent limiting, Ozguc discloses an output driver circuit as explained in Section XI.A.2.a for Element 7[pre].

**b. 11[a]: a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;**

Ozguc discloses a first driver transistor (MP1) that provides a low-impedance path from $V_{CC}/V_{25}$ to an output node (OUT) in response to a voltage at a first driver control node (MP1's gate) as explained in Section XI.A.2.b for Element 7[a]. *E.g.,* Ex-1006, Figs. 1-2; Ex-1002, ¶112.

**c. 11[b]: a second driver transistor that provides a low impedance path to the output node in response to a voltage at a second driver control node; and**

Ozguc discloses a "discharging transistor MN1" having a source-drain path coupled between a second power supply node (Ground) and an output node ("OUT") as shown in Figures 1-2. Ex-1006, 2:14-65, 3:5-42, 3:62-4:9. MN1 is a "driver transistor" because when the input "SIGNAL" is low, MN1 "sink[s] a discharging current $I_{dis}$ from the load 160 coupled to OUT terminal" to drive the output voltage to a low value. Ex-1002, ¶113; Ex-1006, 2:15-20, 2:21-44, 2:45-65, 3:5-19, 3:30-42, 3:62-4:9; *compare with* Ex-1001 (Fig. 1, N10). MN1's gate is a "second driver control node" because MN1 can be controlled by changing its gate voltage. Ex-1006, 2:8-65; *see also* 3:62-4:9. Because MN1 is an NMOS, it provides a low-impedance between from its source (Ground) to its drain ("OUT[PUT]" node) in response to a high voltage at its gate (the second driver

control node). Ex-1002, ¶¶114-15; Section VI.B. Therefore, Ozguc discloses Element 11[b].

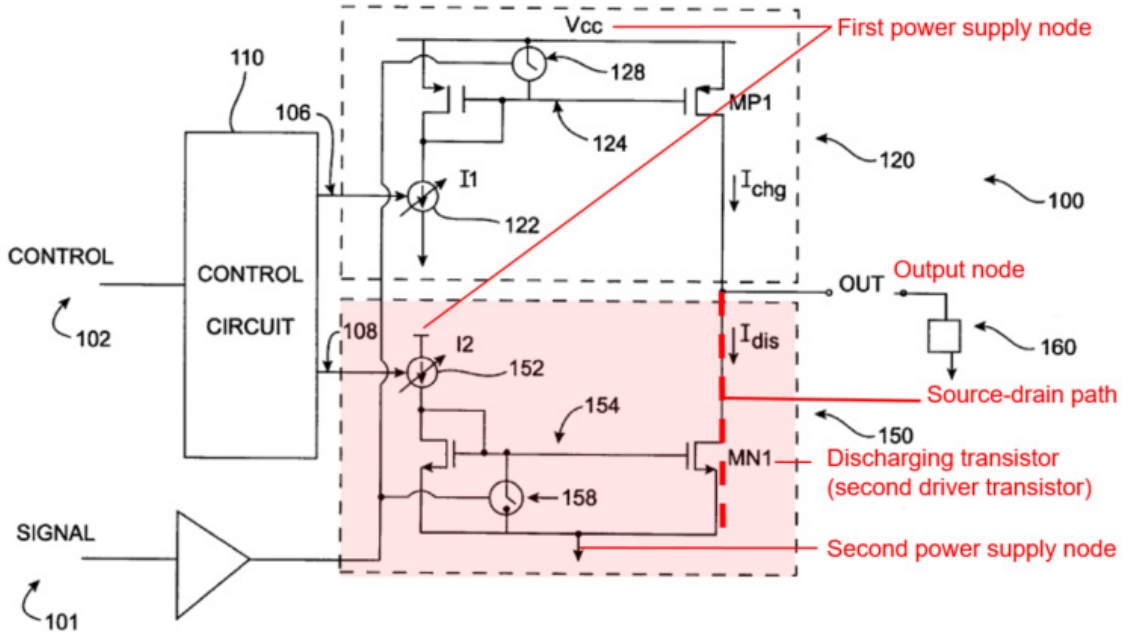


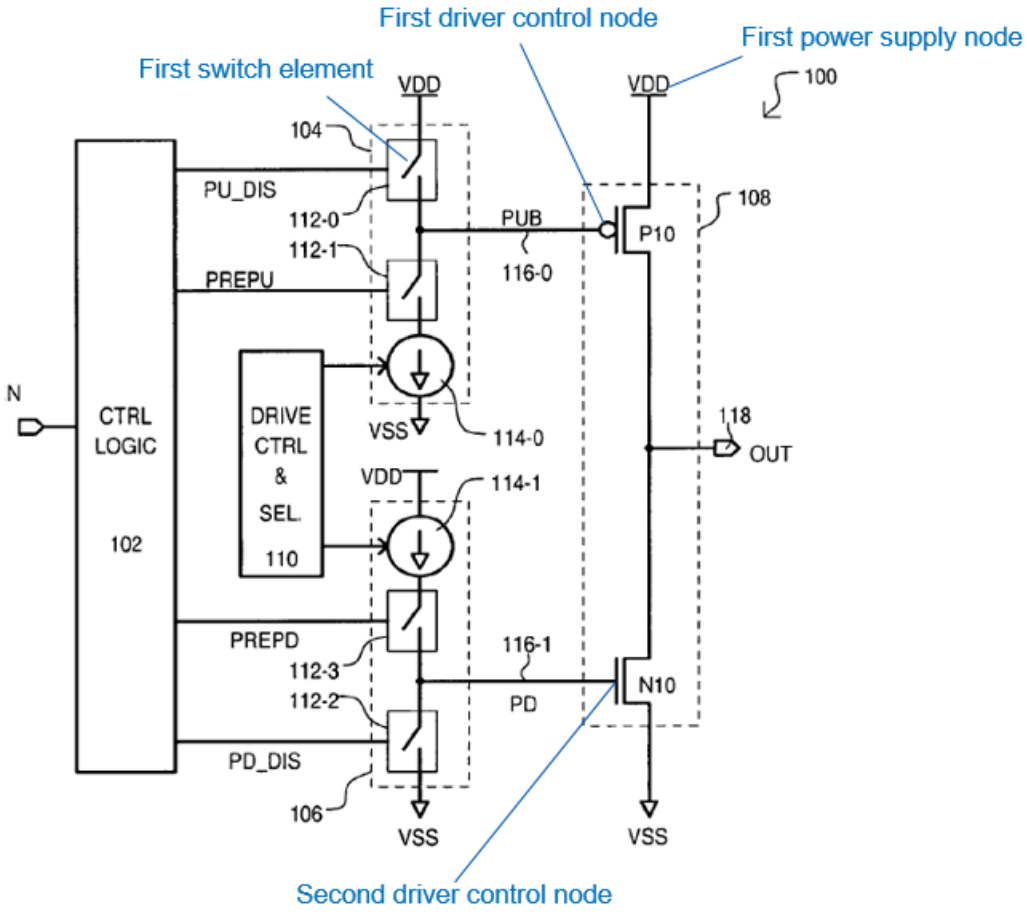

FIG. 1

Ex-1006, Fig. 1

**d. 11[c]: a first switch element coupled between the first driver control node and a first power supply node, and between the second driver control node and the first power supply node,**

The '455 Patent specification discloses a "first switch element 112-0" coupled between the first driver control node (P10's gate) and the first power supply node ($V_{DD}$), but does not disclose that the switch is coupled between the

second driver control node (N10's gate) and the first power supply node ($V_{DD}$).[11] Ex-1001, 2:33-48; 2:62-3:13; Fig. 1.




Ex-1001, Fig. 1

To the extent Patent Owner argues that two switches (*e.g.,* 112-0 and 112-3 in Fig. 1 of the '455 Patent) collectively constitute a "first switch element," the combination of Ozguc and Huber discloses Element 11[c]. As explained in

[11] Petitioner reserves the argument that Claim 11 fails to meet Section 112.

Section XI.B.2, a POSITA would have found it obvious to add Huber's switch (M9) at the output of Ozguc's second adjustable current source (152/252), *e.g.,* as shown below. Ex-1002, ¶¶117-18. Accordingly, Ozguc in view of Huber discloses that 128 and M9 collectively constitute "a first switch element" coupled between the first driver control node (MP1's gate) and a first power supply node ($V_{CC}$), and between the second driver control node (MN1's gate) and the first power supply node ($V_{CC}$). Thus, the combination of Ozguc and Huber discloses Element 11[c].

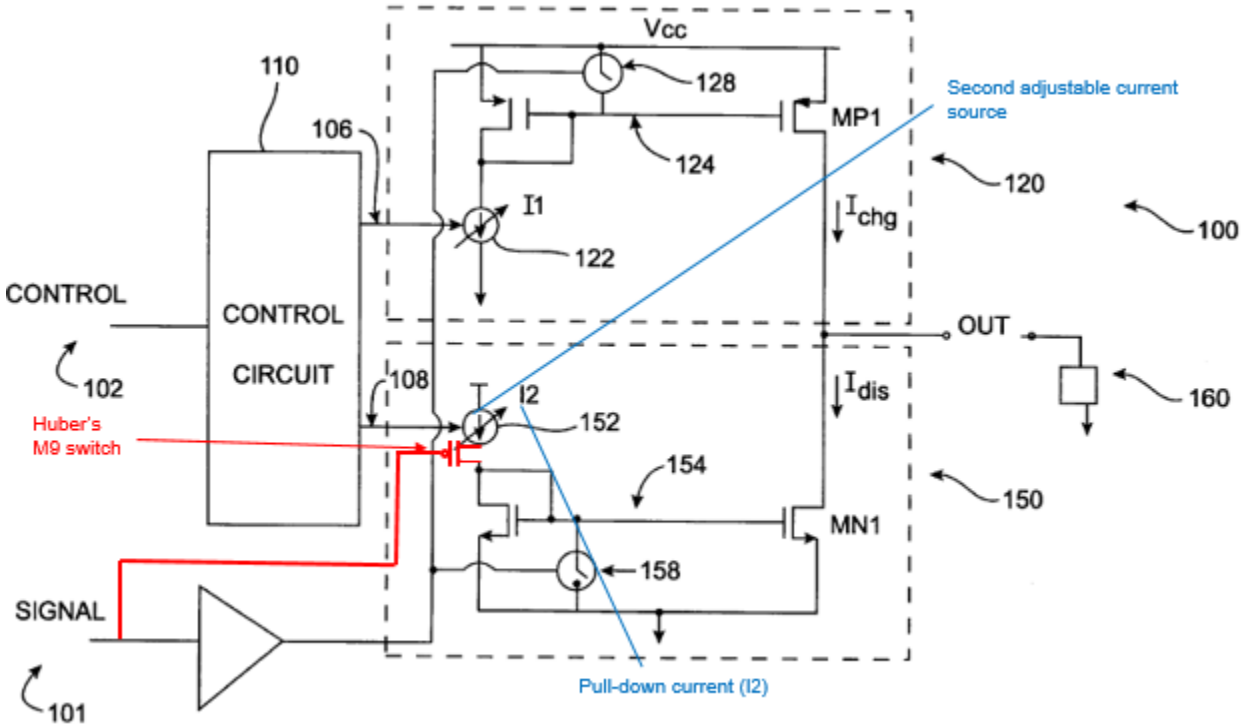



FIG. 1

Ex-1006, Fig. 1 (modified)

**e. 11[d]: the selectable current source generating a drive current that varies in response to a drive select value.**

Ozguc discloses that the first adjustable current source (122/222 in Figs. 1-2) generates a drive current ($I_1$) that varies in response to a drive select value (*e.g.,* "UP"/"DNB" values), as explained in Section XI.A.2.d for Element 7[c]; Ex-1002, ¶119.

Thus, Ozguc and Huber render obvious claim 11.

**6. Claim 12**

**a. 12: The output driver circuit of claim 11, further including: a second switch element coupled between the second driver control node and the second power supply node.**

Ozguc discloses a second switch element (158/258 in Figs. 1-2) coupled between the second driver control node (MN1's gate) and the second power supply node (Ground). Ex-1006, Figs. 1-2, 2:22-65; Section XI.A.1; Ex-1002, ¶120.

Thus, the combination of Ozguc and Huber renders claim 12 obvious.

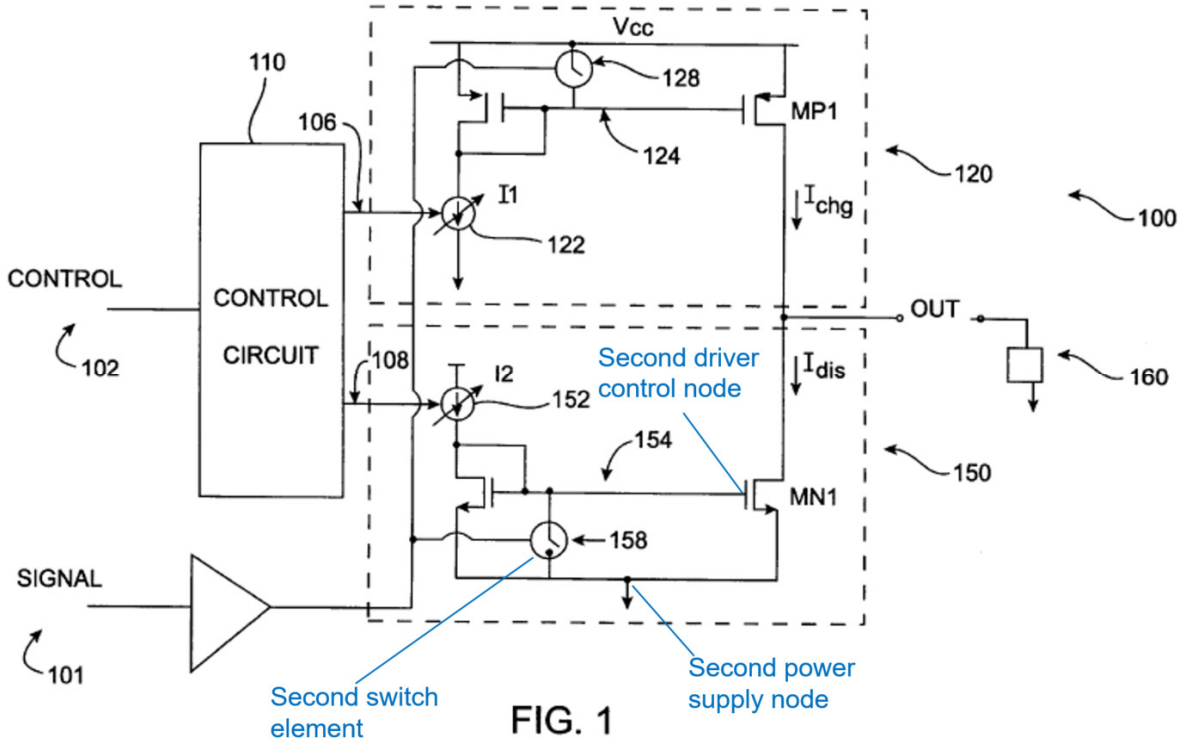



FIG. 1

Ex-1006, Fig. 1

### C. Ground 4: Claim 9 is obvious over Ozguc and Wu

#### 1. Wu

Wu issued on November 30, 1999, qualifying as §102(b) art.

Wu discloses that currents used to drive a circuit can "undesirably" change due to variations in "the temperature and $V_{CC}$ supply voltage." Ex-1008, 1:32-46, 2:34-40. Wu discloses "a current compensation circuit" for maintaining the currents at a desired level, "regardless of the temperature or the supply voltage." *Id.,* Abstract, 2:15-39.

In Figure 2 below, Wu discloses a compensation circuit 230 that provides a compensated current ($I_{Total}$) as input to a circuit that needs to be driven by a current (*e.g.,* a "buffer circuit" or "an inverter circuit"). Ex-1008, 2:27-40, 3:24-4:15.

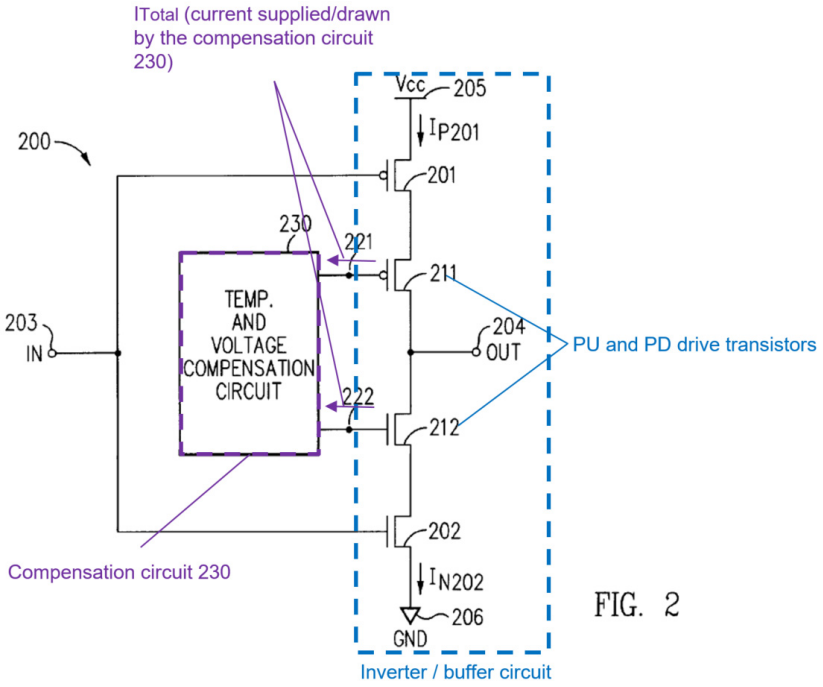



FIG. 2

Ex-1008, Fig. 2

In Figures 3 and 4C below, Wu discloses that the total current at the driver control node of an inverter circuit is provided by a "summing circuit 310" that adds compensation current components ($I_A$, $I_B$, $I_C$, $I_D$), one of which ("$I_C$") ***"is inversely proportional to the $V_{CC}$ supply voltage," (e.g., "increases" "when $V_{CC}$ … decreases" and "is relatively insensitive to variations in temperature***." Ex-1008, 6:28-57; Ex-1002, ¶¶121-23.

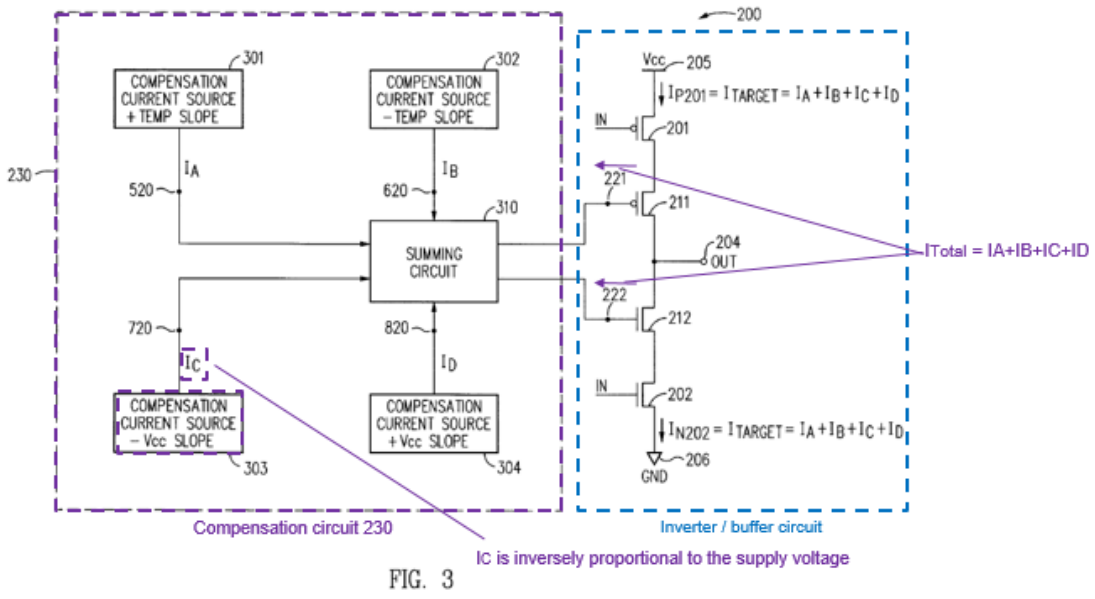



FIG. 3

Ex-1008, Fig. 3

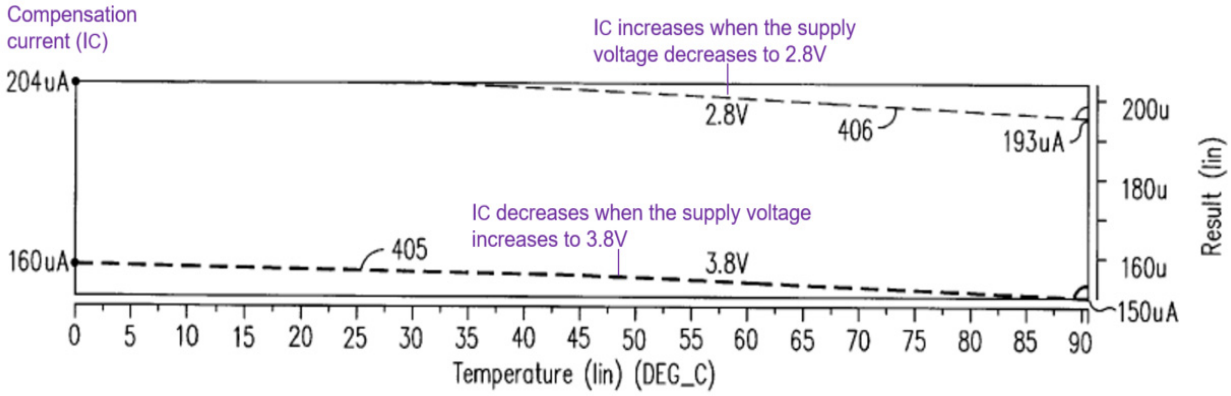



FIG. 4C

Ex-1008, Fig. 4C

### 2. Obviousness Combination of Ozguc, Huber and Wu

Ozguc, Huber, and Wu are in a common field of endeavor (IC design) and directed to adjusting the drive current of the same types of circuits (a buffer circuit). Ex-1006, Abstract, 1:17-18, 4:5-9; Ex-1007, Abstract, 1:7, 2:44-3:57; Ex-

1008, Abstract, 2:28-40, 4:9-15. Given these similarities, a POSITA would have looked to Wu to further improve Ozguc's buffer circuit modified in view of Huber as described above in Section XI.A.3. *Id.*; Ex-1002, ¶124.

Wu discloses that, without compensation, a buffer's performance can undesirably vary when the operating conditions (*e.g.,* temperature) and/or the supply voltage change. Ex-1008, 1:32-46, 2:28-40. An input to Ozguc's circuit is a reference/"CONTROL" current. Ex-1006, Figs. 1-2. Ozguc does not disclose how this current is generated, leaving a POSITA to select a suitable circuit. Ex-1002, ¶125. A POSITA would have been motivated to select Wu's circuit which is designed to supply stable currents for I/O buffers, such as Ozguc's. *Id.*; Ex-1008, 2:28-59, 6:42-57.

As described in Section XI.C.1, Wu discloses a "compensation circuit" that "control[s] the charging and discharging currents of the inverter" or "input/output buffer circuits" so that the performance (*e.g., "*the speed of signal propagation") can be "maintained at a desired, pre-determined level, regardless of the temperature or the supply voltage." Ex-1008, 2:15-40, 6:42-57.

In view of these benefits, a POSITA would have been motivated to add Wu's compensation circuit to the Ozguc-Huber buffer to improve the consistency of its performance (*e.g.,* the rise/fall times) under a variety of operating conditions

(*e.g.,* temperature or supply voltage variation). Ex-1002, ¶¶126-27; Ex-1008, 2:28-40.

For example, Wu's compensation circuit can be used to feed a compensated control current ($I_{Total}$) to Ozguc's buffer, as shown in modified Ozguc Figures 1-2 below. As described in Section XI.A.4, the compensated control current has a component ***"$I_C$ [that] is inversely proportional to the $V_{CC}$ supply voltage, and … is relatively insensitive to variations in temperature***." Ex-1008, 6:28-57. As shown in Figures 1-3 below, because Ozguc's adjustable current ($I_1$) is a multiple of the reference current ($I_1$'), which mirrors the compensated control current ($I_{Total}$), $I_1$ also has a component that is inversely proportional to the $V_{CC}$ supply voltage. Ex-1002, ¶128.

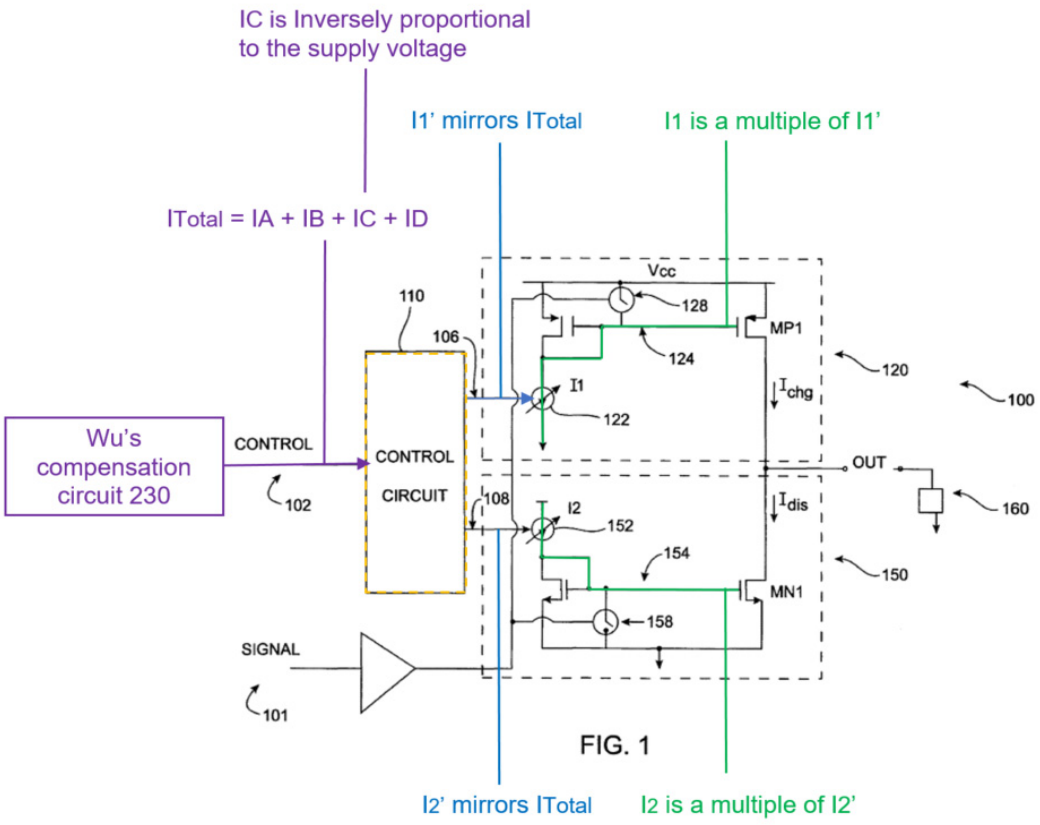



FIG. 1

Ex-1006, Fig. 1 (modified)

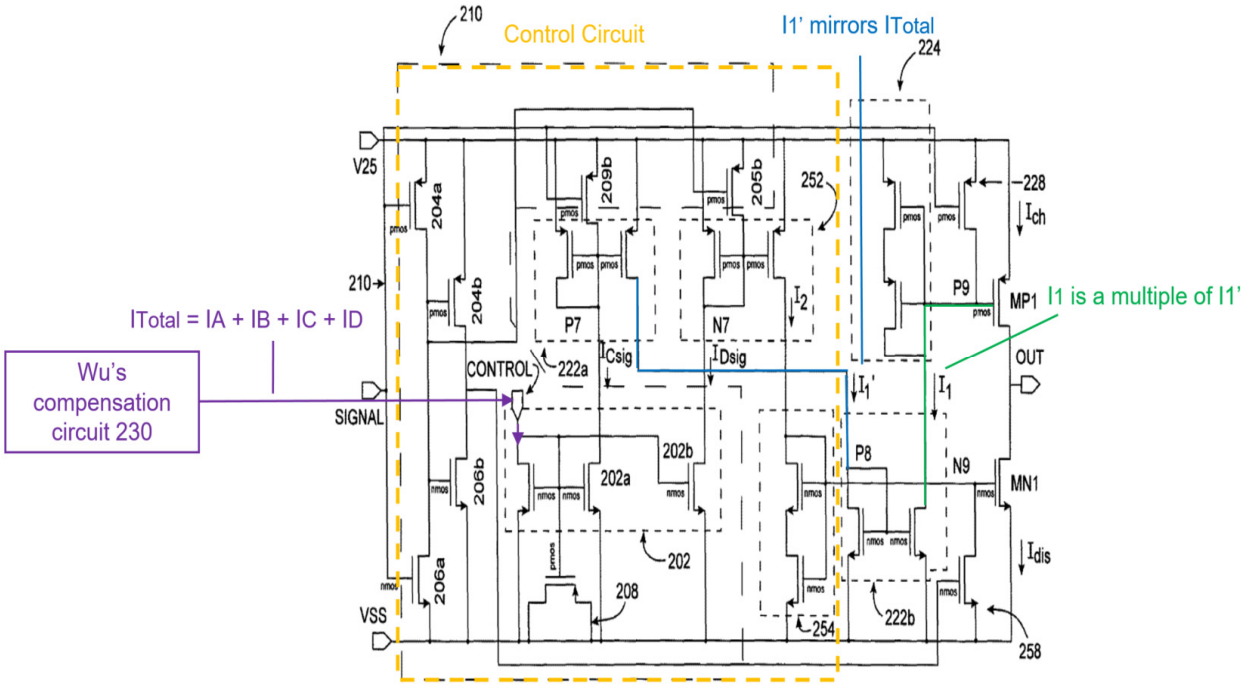


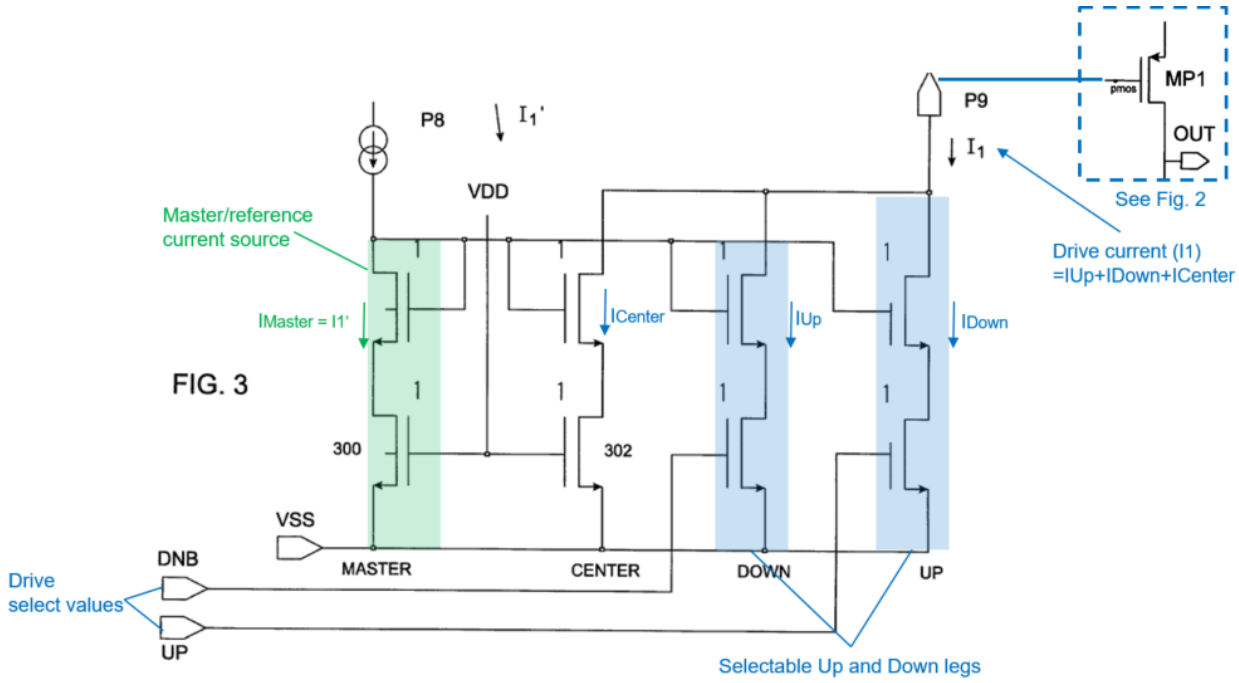

FIG. 2

Ex-1006, Fig. 2 (modified)

Although Ozguc describes an example of using "four cascode pairs of FETs" for adjusting the drive current for the pull-up circuit, it also discloses that "the second adjustable current source" (152/252) can similarly have multiple "cascode pairs of FETs" in order to adjust the fall time. Ex-1006, 4:10-46; Ex-1002, ¶129. As explained in Section XI.A.4, Wu discloses that its compensation current is fed to both upper and lower circuits (equivalents of Ozguc's pull-up and pull-down circuits). Ex-1008, Fig. 3. Therefore, for similar reasons discussed above, it would have been obvious to use Wu's compensated current ($I_{Total}$) as a source for Ozguc's pull-down current $I_2$.

**3. 9[a]: The output driver circuit of claim 7, wherein: the selectable current source further includes a reference current source that provides a reference current having at least one component that is inversely proportional to a power supply voltage, and**

As described above and in Section XI.A.1, Ozguc discloses that the drive current ($I_1$) generated by the first adjustable current source (selectable current source) mirrors the reference current ($I_1$') that passes through the Master current leg, as shown below. The first adjustable current source's Master current leg circuit serves as a "reference current source" circuit because its current ($I_1$') is used as a reference current that is input to the mirror to generate the drive current ($I_1$). Ex-1002, ¶¶130-31; Ex-1006, Fig. 3; 4:10-36.




Ex-1006, Fig. 3

Ozguc in view of Wu discloses that the reference current ($I_1$') has a component ($I_C$) that is inversely proportional to the power supply voltage, as explained in Section XI.C.2. *Id.*

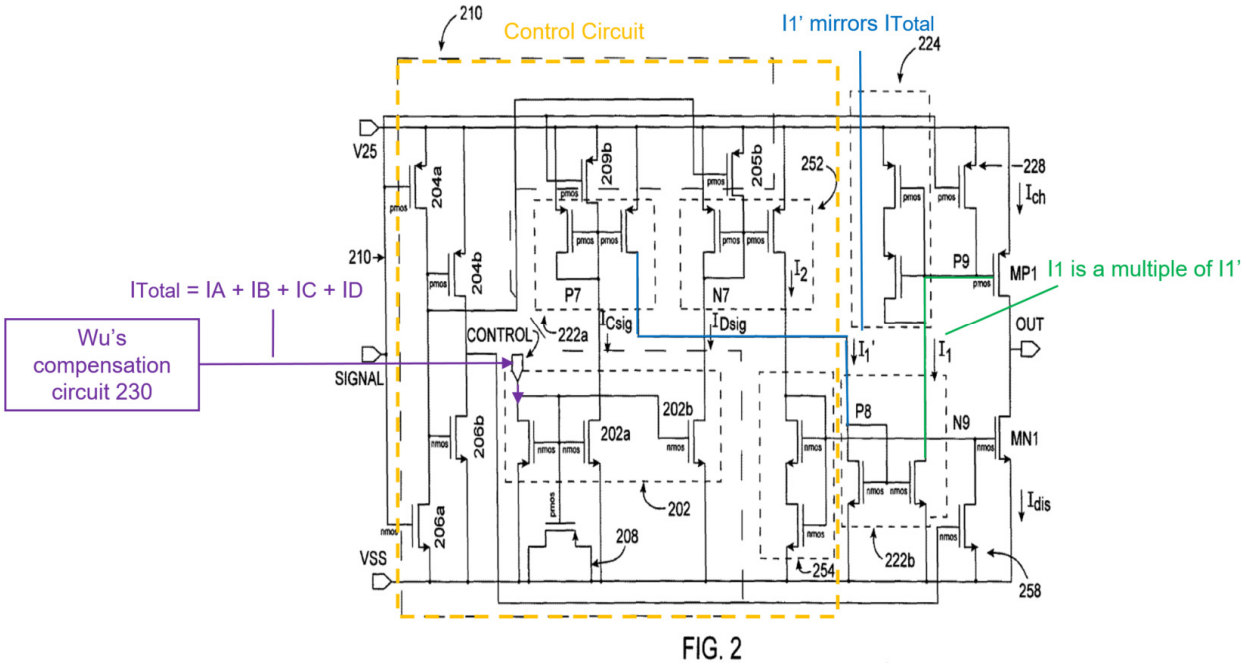



FIG. 2

Ex-1006, Fig. 2 (modified)

Therefore, Ozguc in view of Wu discloses a first adjustable current source 122/222 (selectable current source) including a reference current source (Master leg) that provides a reference current ($I_1$') having a component ($I_C$) that is inversely proportional to a power supply voltage. Ex-1002, ¶¶130-32.

**4. 9[b]: each of the selectable current legs provides a current proportional to the reference current.**

Because each of the selectable current legs disclosed by Ozguc (*e.g.*, Up and Down legs) mirrors the reference current ($I_{Master}$), the current in each selectable

current leg is a "multipl[e]" of the reference current ($I_{Master}$=$I_1$'), as explained in Section XI.A.1. Ex-1006, 4:10-36, Fig. 3. Therefore, Ozguc discloses that each selectable current leg (Up/Down) provides a current ($I_{Down}$/$I_{Up}$) that is proportional to the reference current ($I_{Master}$=$I_1$'). *Id.*; Ex-1002, ¶¶133-34.

Thus, the combination of Ozguc and Wu renders claim 9 obvious.

### D. Ground 5: Claim 9 is obvious over Ozguc, Huber, and Wu

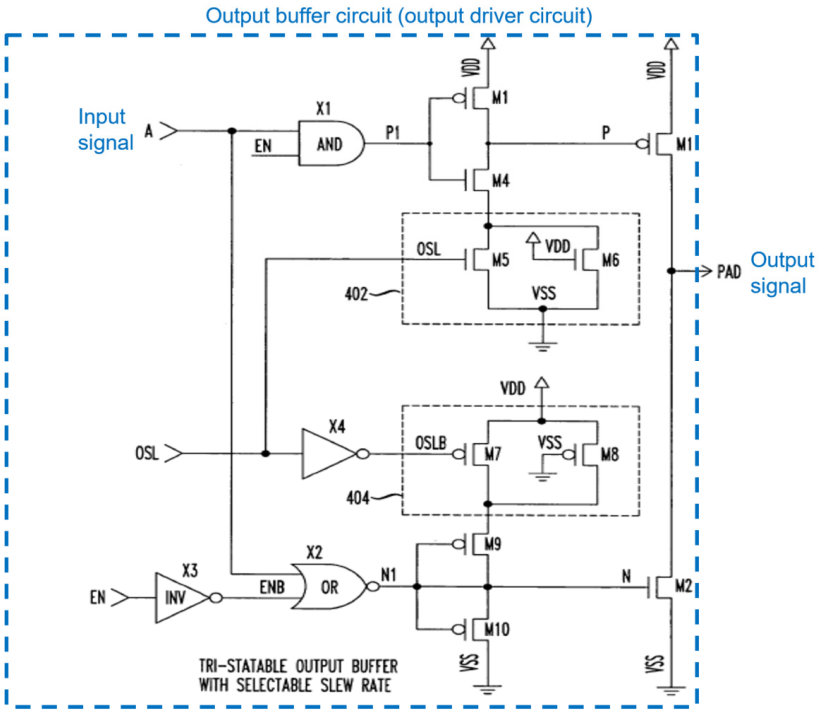
Ozguc in view of Wu discloses each limitation added by dependent claim 9 as explained for Ground 4 in Sections XI.C.3-4. In the event the Board adopts the potential interpretation of Element 7[d] described above in Ground 3, that element is disclosed by Ozguc in view of Huber, as explained in Section XI.B.3, and thus, claim 9 is obvious over Ozguc in view of Huber and Wu.

### E. Claims 11 and 12 are anticipated by (Ground 6) or obvious over (Ground 7) Huber

#### 1. Independent Claim 11

##### a. 11[pre]: An output driver circuit, comprising:

To the extent limiting, Huber discloses an output driver circuit because Huber's "output buffer" "***drives*** an external output," for example, as shown in Figure 4. Ex-1007, 1:53-54, 4:3-30; Ex-1002, ¶¶136-37; *see also* Ex-1001, Title, 1:10-11, 2:11-32.

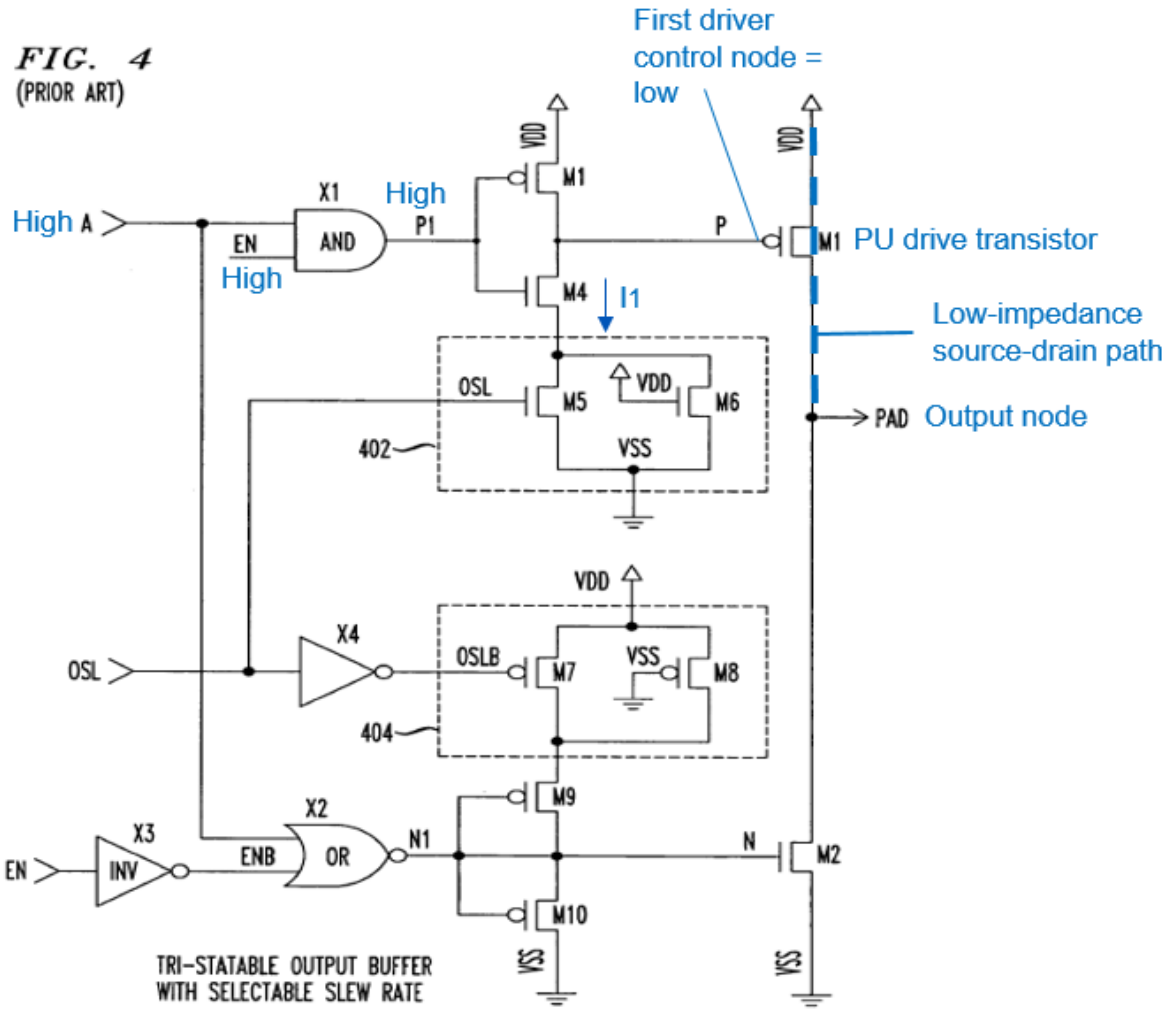



Ex-1007, Fig. 4

**b. 11[a]: a first driver transistor that provides a low impedance path to an output node in response to a voltage at a first driver control node;**

As shown in Figure 4, Huber discloses a first/pull-up "drive[r] transistor" ("p-channel transistor M1" (PMOS)) that "drives an output" (PAD) to a high voltage value ($V_{DD}$). Ex-1007, 1:55-62, 4:4-14; 1:63-2:58, 6:22-25, 7:48-50, claim 1; Ex-1002, ¶¶138-39. Based on the operation of a PMOS, a POSITA would have understood that when the upper slew rate control circuit (402) draws a current ($I_1$) to pull down the voltage at the "drive transistor['s]" gate (first driver control node), the transistor provides a low-impedance source-drain path from $V_{DD}$ to the output

node (PAD). *Id.*; Sections VI.B, XI.A2.b, XI.B.1. Therefore, Huber discloses Element 11[a].

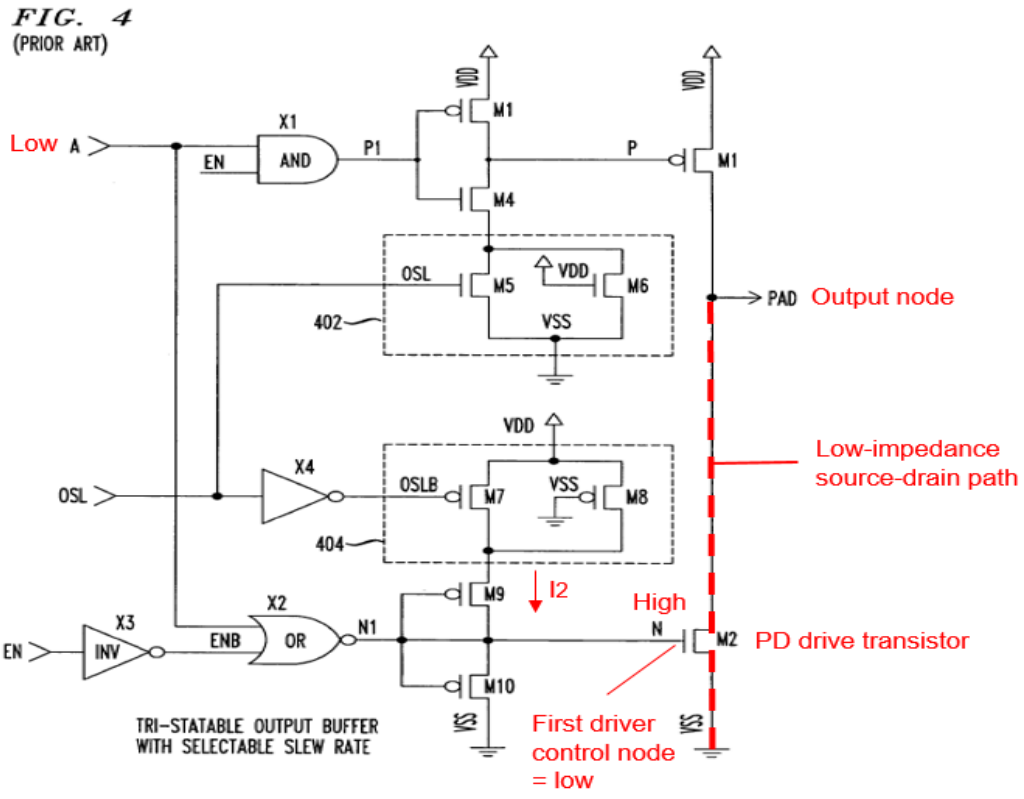



Ex-1007, Fig. 4

**c. 11[b]: a second driver transistor that provides a low impedance path to the output node in response to a voltage at a second driver control node; and**

As shown in Figure 4 below, Huber discloses a second/pull-down "drive[r] transistor" ("n-channel transistor [NMOS] M2" that "drives an output" (PAD) to a

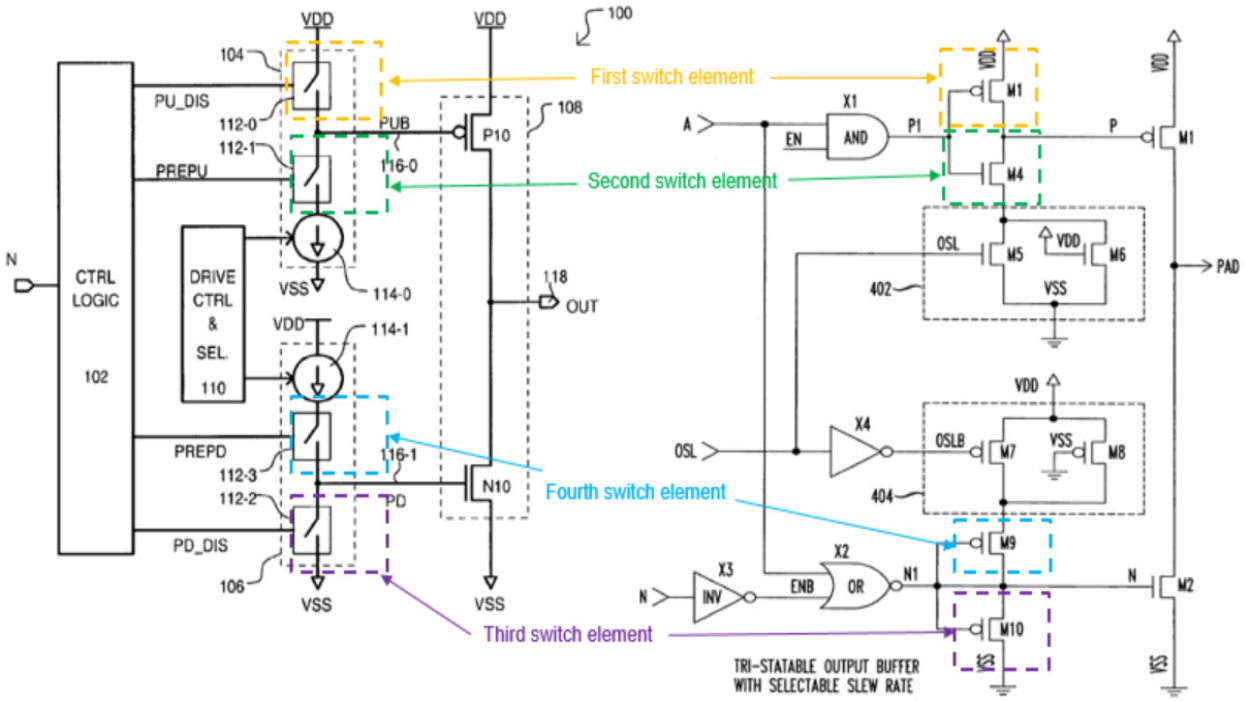
low voltage value ($V_{SS}$). Ex-1007, 1:55-62, 4:4-14; *see also id.*, 1:63-2:22, 2:51-58, 3:30-57, 6:6-31, 7:13-22; Ex-1002, ¶140. Based on the operation of an NMOS, a POSITA would have understood that as the lower slew rate control circuit (402) supplies a current ($I_2$) to pull up the voltage at M2's gate/node N (second driver control node), M2 provides a low-impedance source-drain path from $V_{SS}$ to the output node (PAD), as shown below. *See id.*; Sections VI.B, XI.A2.b, XI.B.1. M2's gate terminal is a "second driver control node" because M2 can be switched on/off by changing its gate voltage. *Id.*; Ex-1007, 1:55-2:22, 2:51-58. Therefore, Huber discloses Element 11[b].




Ex-1007, Fig. 4

**d. 11[c]: a first switch element coupled between the first driver control node and a first power supply node, and between the second driver control node and the first power supply node,**

To the extent Element 11[c] meets Section 112, it is disclosed by Huber under any interpretation because the arrangements of switches in Huber's buffer circuit and '455 Patent embodiments are identical. *Compare* Ex-1007, Fig. 4 *with* Ex-1001, Fig. 1; *see* Section XI.B5. To the extent Patent Owner argues that two switches (*e.g.,* 112-0 and 112-3) collectively constitute a "first switch element," Huber discloses Element 11[c] under that interpretation. Huber discloses two switches (*e.g.,* M1 and M9 in Fig. 4) coupled between the first driver control node (P) and a first power supply node ($V_{DD}$) and between the second driver control node (N) and the first power supply node ($V_{DD}$). Ex-1007, 1:55-62, 1:63-2:58, 3:50-56; *see also id.*, 2:4-22, 5:49-54, 6:6-31, 7:13-22; Ex-1002, ¶141.

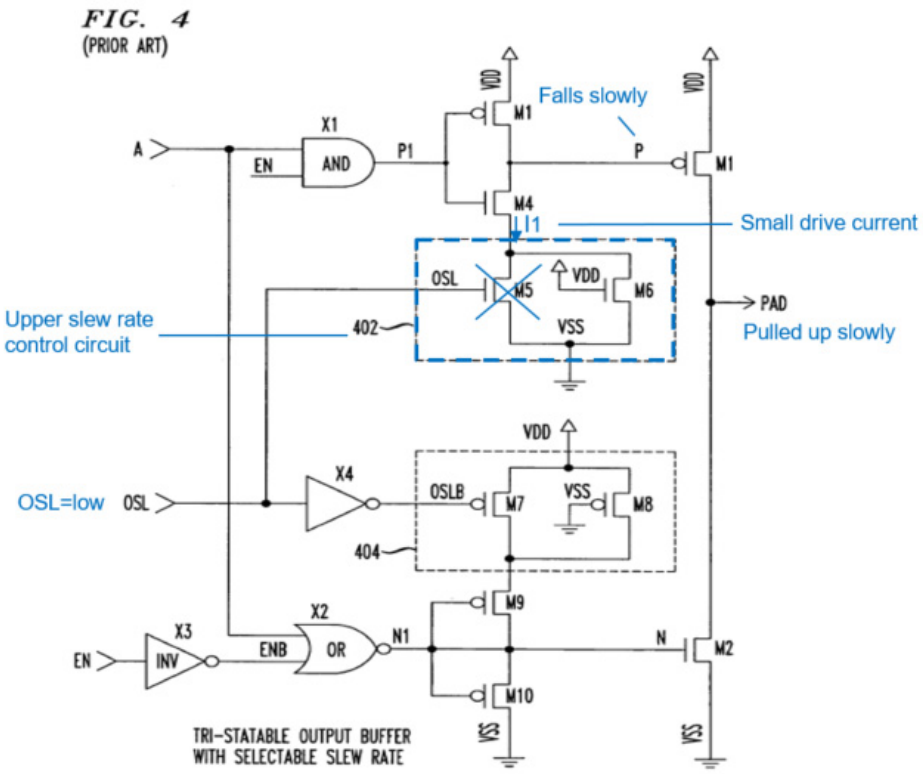



Ex-1001, Fig. 1 Ex-1007, Fig. 4

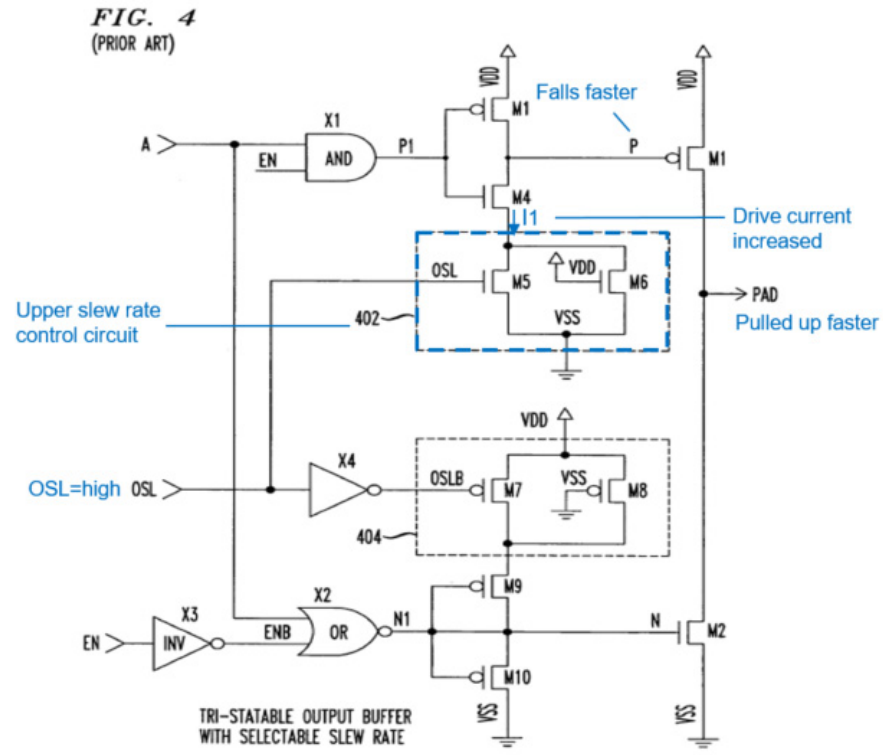
**e. 11[d]: the selectable current source generating a drive current that varies in response to a drive select value.**

As annotated in Figure 4 below, Huber discloses that the slew rate control circuit (402) varies the drive current (for driving the "drive transistor" M1) by selectively adjusting the slew rate control signal (OSL), which turns on or off transistor M5. *See* Section XI.B.1. Accordingly, Huber discloses or renders obvious a selectable current source generating a drive current ($I_1$ at the output of the upper slew rate circuit 402) that varies in response to a drive select value (OSL). Ex-1002, ¶¶142-44.

Therefore, Huber discloses Element 11[d].




Ex-1007, Fig. 4 (slower slew rate)




*Id.* (faster slew rate)

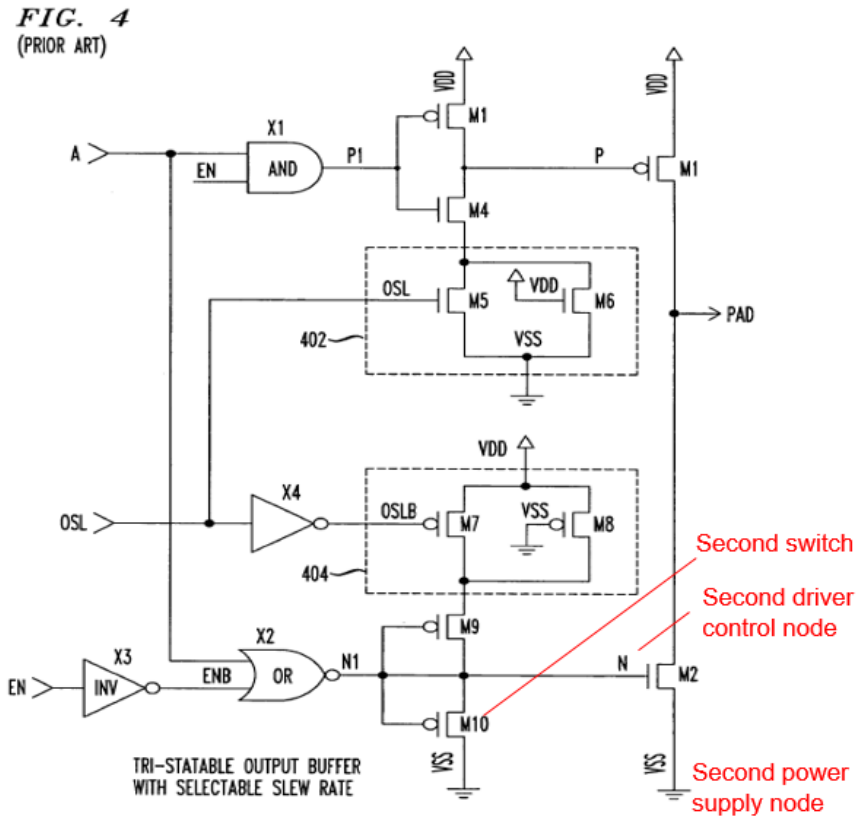
Thus, claim 11 is anticipated by or obvious over Huber.

### 2. Claim 12

#### a. 12: The output driver circuit of claim 11, further including: a second switch element coupled between the second driver control node and the second power supply node.

Huber discloses a second switch element (M10) coupled between the second driver control node (N=M2's gate) and the second power supply node ($V_{SS}$), as shown below. Ex-1007, 1:55-62, 3:50-57; Ex-1002, ¶145.

Thus, claim 12 is anticipated by or obvious over Huber.




Ex-1007, Fig. 4

## F. Ground 8: Claims 1-6 and 14 are obvious over Ozguc, Huber, and Wu

### 1. Independent Claim 1

#### a. 1[pre]: An output driver circuit, comprising:

Ozguc discloses an "output driver circuit." *See* Sections XI.A.1, XI.A.2.a (Element 7[pre]).

#### b. 1[a]: at least a first driver transistor having a source-drain path coupled between a first power supply node and an output node;

As explained in Grounds 1-2 for Element 7[a] in Section X.A.2.b and shown below, Ozguc discloses a "charging transistor MP1" (first driver transistor) having a current path between its source (a first power supply node ($V_{CC}$)) and its drain ("OUT[PUT]" node). Ex-1006, 2:8-32; 2:45-3:13, Fig. 2 (MP1); Ex-1002, ¶148. Therefore, Ozguc discloses Element 1[a].

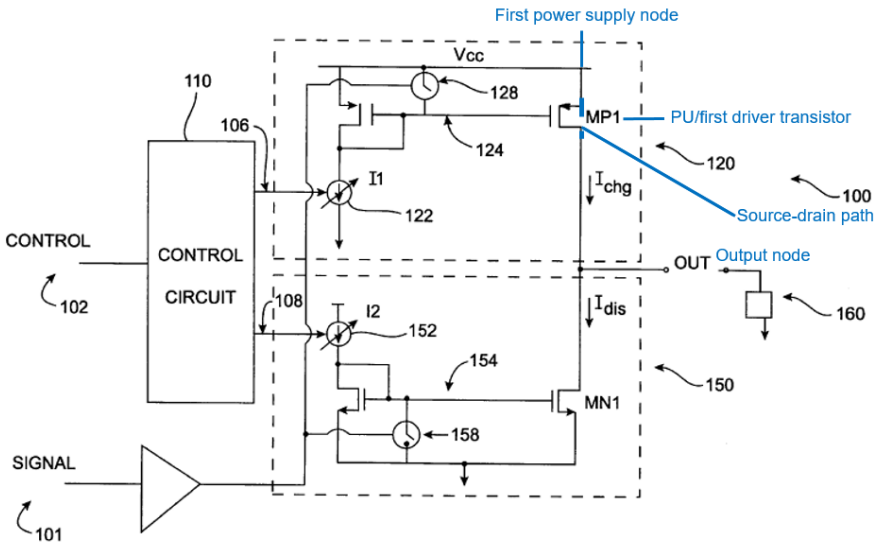



FIG. 1

Ex-1006, Fig. 1

**c. 1[b]: a first variable current supply that generates a current having at least one component that is inversely proportional to a power supply voltage;**

Ozguc discloses that each of the "output driver circuits" includes "a first adjustable current source" (122/222 in Figs. 1-2) generating a current ($I_1$) that changes in response to drive select values (*e.g.,* "UP"/"DNB" select values in Fig. 3), as explained above in Section XI.A.1. Ex-1006, 1:65-2:14, 2:45-65, 2:66-3:43, 3:44-61, 3:62-4:9, 4:10-58; Ex-1002, ¶149. Therefore, Ozguc discloses a "first variable current supply" (122/222) generating a variable current ($I_1$).

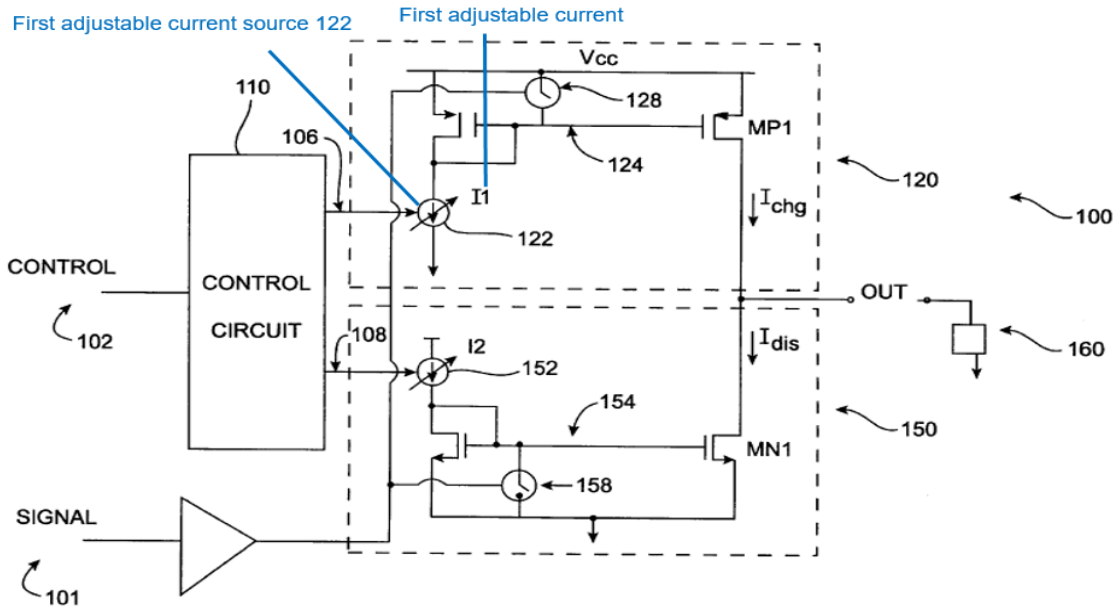



FIG. 1

Ex-1006, Fig. 1

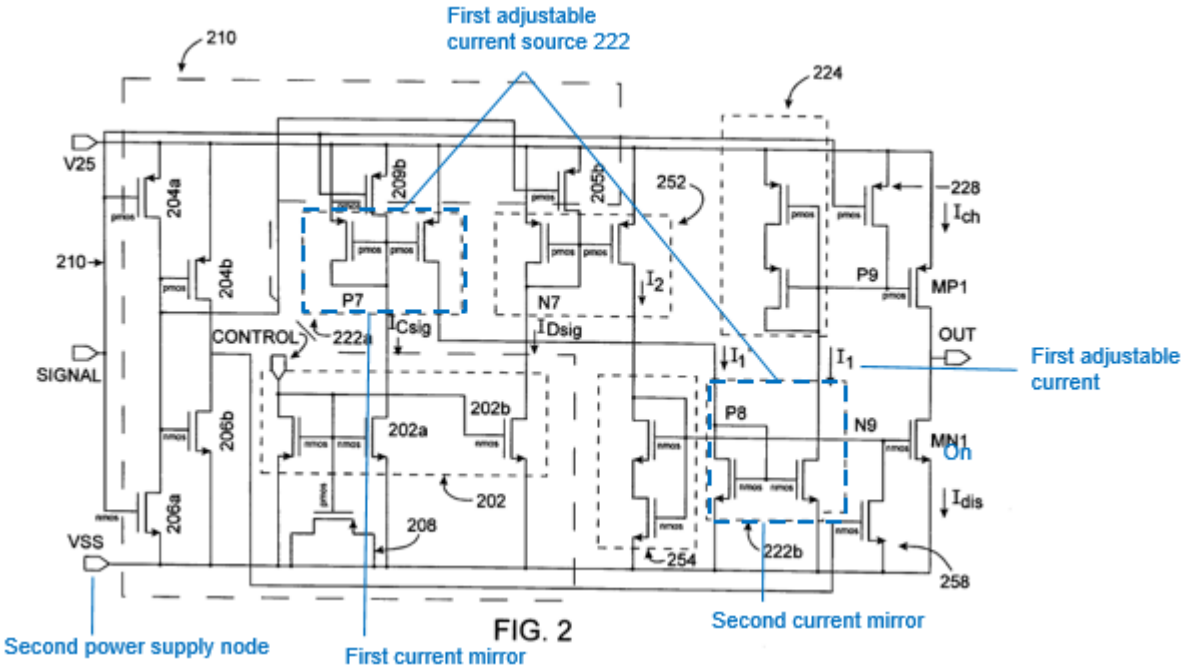



FIG. 2

Ex-1006, Fig. 2

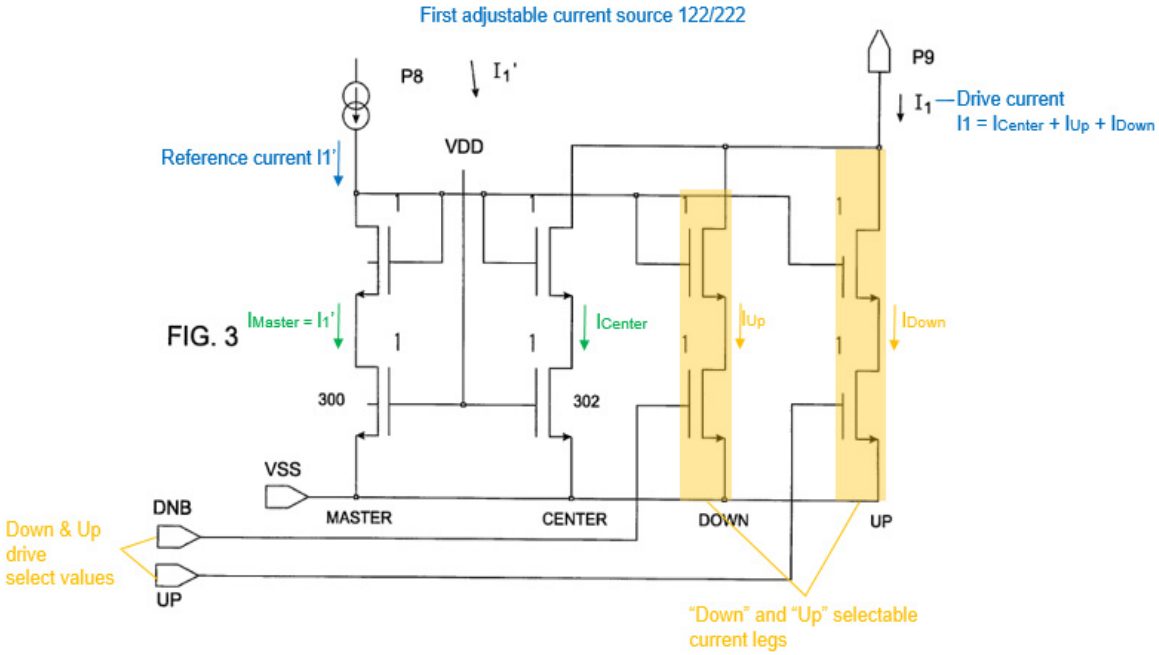



FIG. 3

Ex-1006, Fig. 3

In view of Wu, a POSITA would have found it obvious to modify Ozguc's first adjustable current source (122/222) such that it supplies a variable current ($I_1$) having a component ($I_C$) that is inversely proportional to a power supply voltage ($V_{CC}/V_{25}$) as explained for Ground 4, claim 9 in Sections XI.C.1-2; Ex-1002, ¶150. Therefore, Ozguc in view of Wu discloses Element 1[b].

**d. 1[c]: first driver switch element coupled in series with the first variable current supply between a gate of the at least first driver transistor and a second power supply node, wherein the first driver switch and the first variable current supply are configured to control a rise time of the output driver circuit.**

As shown in modified Figure 1 of Ozguc below, a POSITA would have found it obvious to add Huber's M4 switch at the output of Ozguc's pull-up/first adjustable current supply (122/222 in Figs. 1-2), as explained in Section XI.B.2.b. Huber's M4 switch is coupled in series with the first variable current supply (122/222) and is positioned between a gate of the first driver transistor (MP1) and a second power supply node (Ground/$V_{SS}$). *See* Section XI.B.1-2; Ex-1002, ¶¶151-52. Therefore, Ozguc in view of Huber discloses Element 1[c].

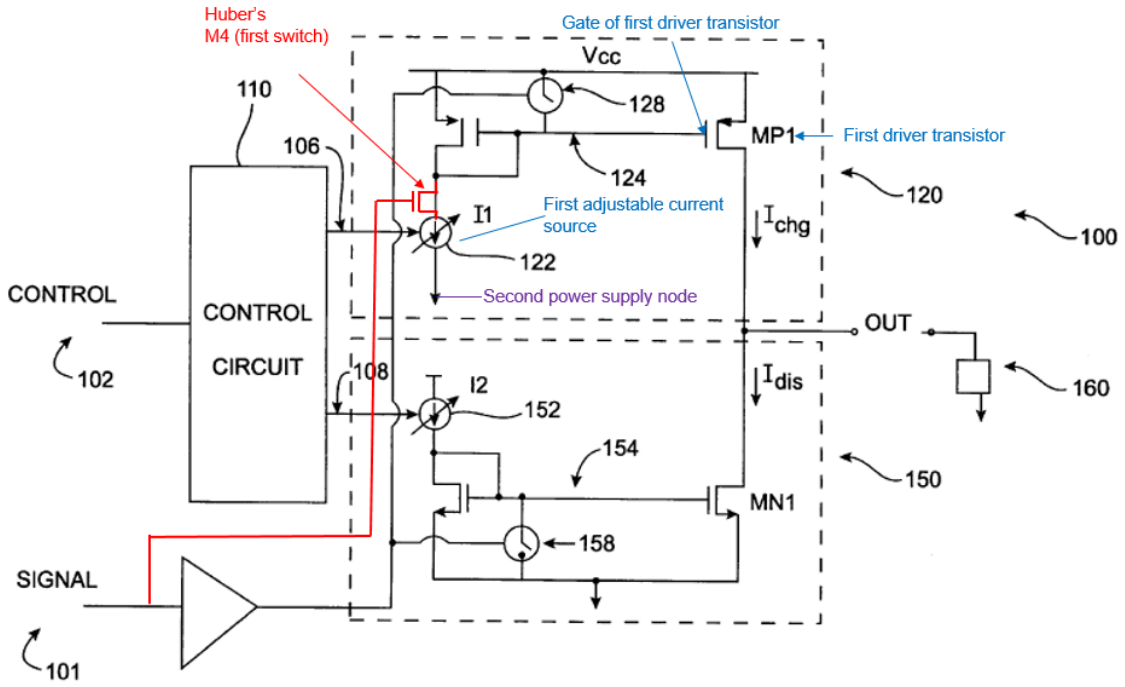



FIG. 1

Ex-1006, Fig. 1 (modified)

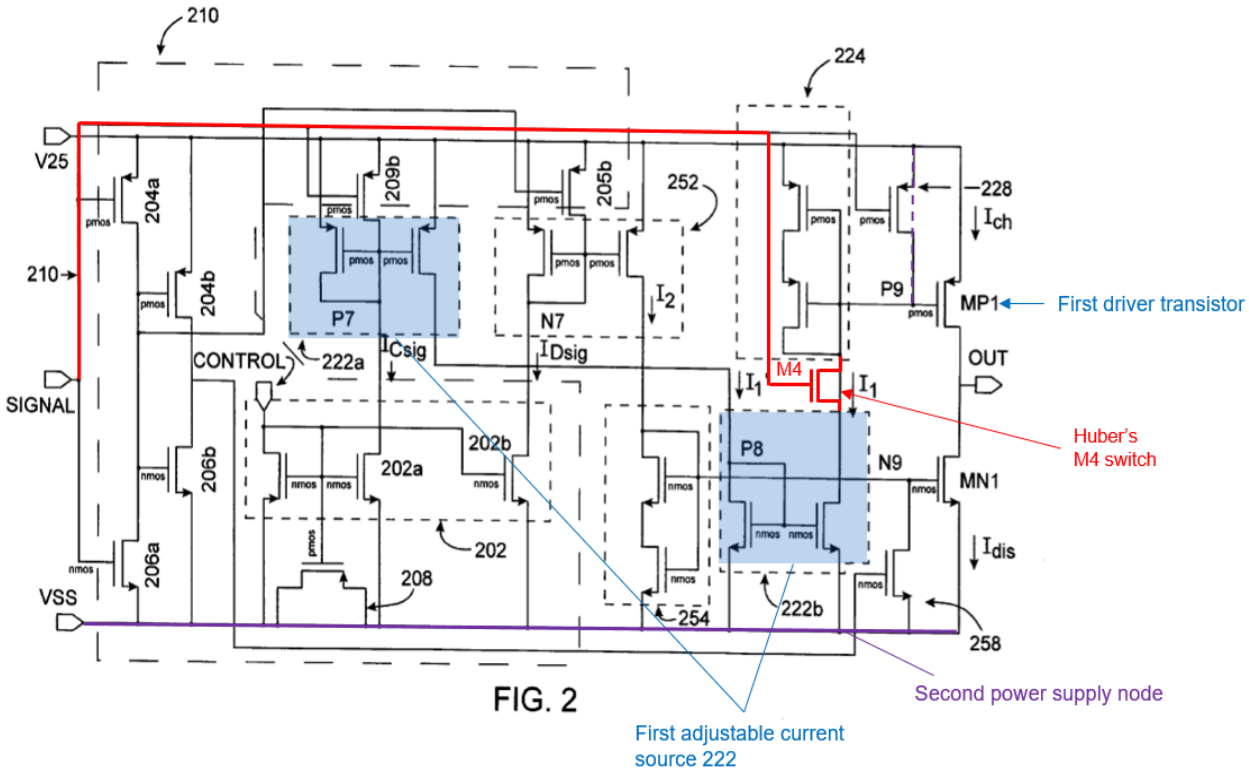



FIG. 2

Ex-1006, Fig. 2 (modified)

Thus, the combination of Ozguc, Huber, and Wu renders claim 1 obvious.

**2. Claim 2**

**a. 2: The output driver circuit of claim 1, wherein: the at least first driver transistor includes a p-channel insulated gate field effect transistor, the first power supply node is a high power supply node and the second power supply node is a low power supply node.**

Ozguc's "charging transistor MP1" (first driver transistor) is a PMOS, as explained in Section XI.A.2.b in Ground 1 for Element 7[a]. A POSITA would have understood that a PMOS is a p-channel insulated gate field effect transistor. Ex-1006, 1:66-2:65; 3:62-4:9, Figs 1-2; Ex-1002, ¶¶153-54.

Ozguc also discloses that the first power supply node ($V_{CC}$/$V_{25}$) is a "high [power] supply" node, and the second power supply node (Ground/$V_{SS}$) is a "low [power] supply" (*e.g.,* "0 V"). Ex-1006, 2:12-15; *see also* 1:66-2:65; 3:62-4:9, Figs. 1-2; Ex-1002, ¶¶154-55; Section XI.A.1.

Thus, the combination of Ozguc, Huber, and Wu renders claim 2 obvious.

**3. Claim 3**

**a. 3[a]: The output driver circuit of claim 1, further including: at least a second driver transistor having a source-drain path coupled between the second power supply node and the output node.**

Ozguc discloses a second driver transistor (MN1) having a source-drain path coupled between the second power supply node (Ground/$V_{SS}$) and the output node

("Out") as shown in Figs. 1-2. Ex-1006, 2:15-44; *see also* 2:45-3:42, 4:10-36; Ex-1002, ¶156.

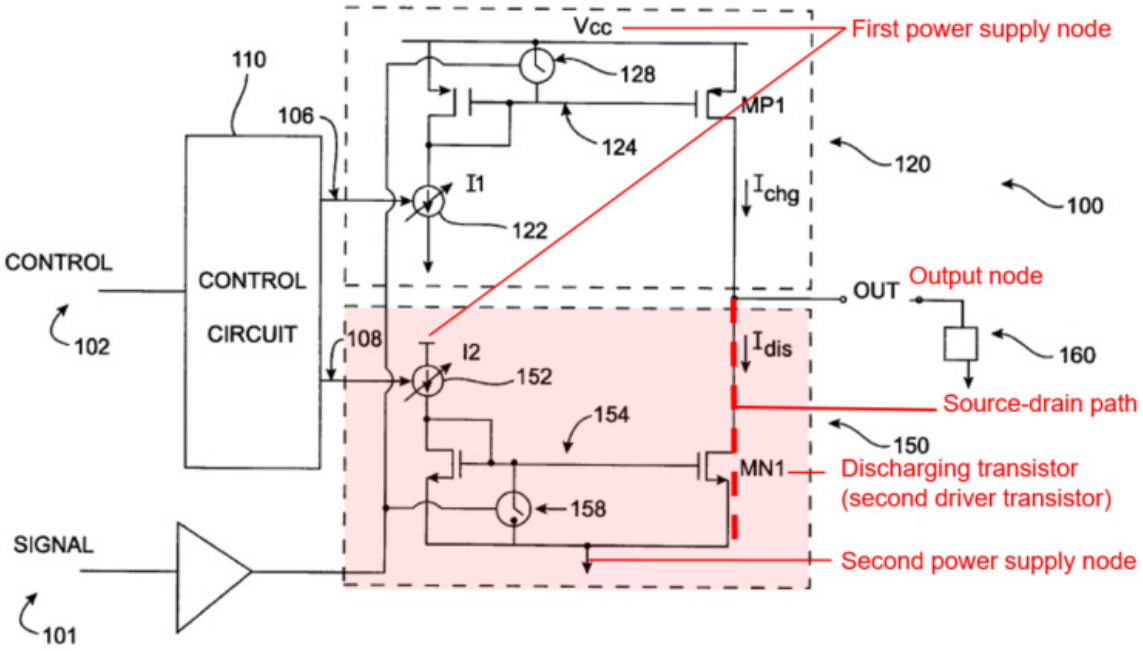



FIG. 1

Ex-1006, Fig. 1

**b. 3[b]: a second variable current supply that generates a current having at least one component that is inversely proportional to the power supply voltage; and.**

Ozguc discloses a second variable current supply (152/252 in Figs. 1-2) generating an adjustable current "$I_2$." Ex-1006, 1:65-2:14; 2:45-4:9, 4:10-36, Fig. 3. In view of Wu, a POSITA would have found it obvious to use Wu's compensated current ($I_{Total}$) as a source for $I_2$ such that $I_2$ would have a component ($I_C$) that is inversely proportional to the power supply voltage ($V_{CC}/V_{25}$), as

explained in Section XI.C.2. Ex-1002, ¶157. Therefore, Ozguc in view of Wu discloses Element 3[b].

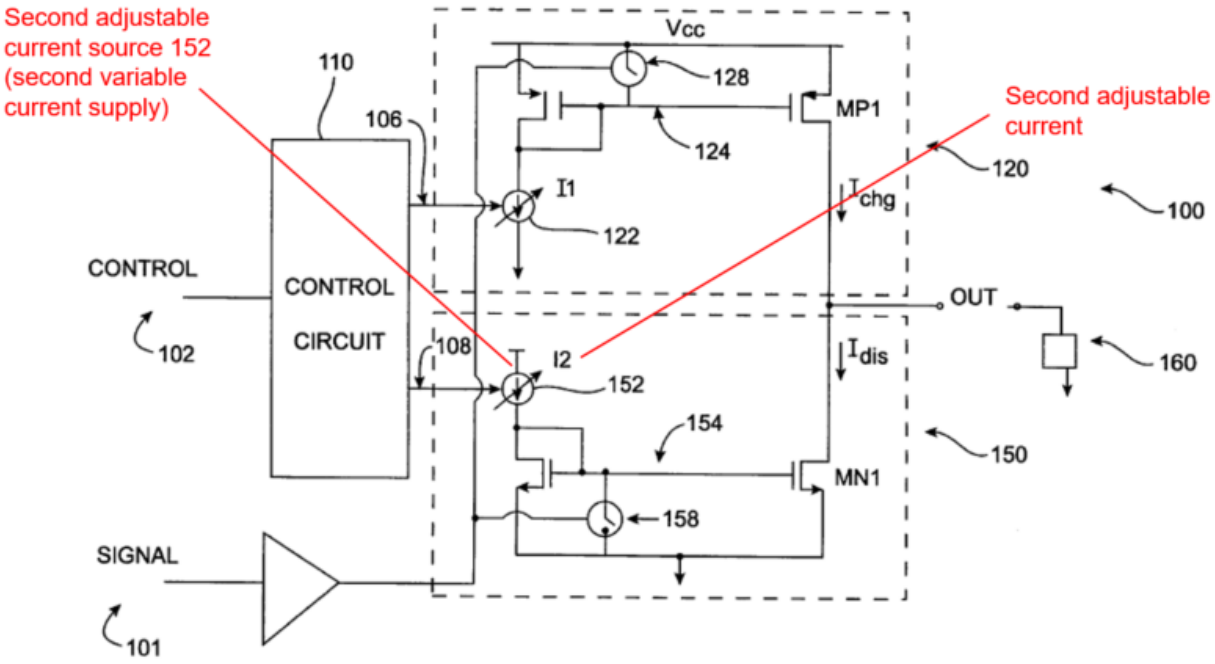



FIG. 1

Ex-1006, Fig. 1

**a. 3[c]: a second driver switch element coupled in series with the second variable current supply between a gate of the at least second driver transistor and the first power supply node, wherein the second driver switch and the second variable current supply are configured to control a fall time of the output driver circuit.**

As explained in Section XI.B.2, it would have been obvious to add Huber's pull-down switch (M9) at the output of Ozguc's second/pull-down adjustable current source (152). Ex-1002, ¶158. Under the modification described in Section

XI.B.2.c, M9 is coupled in series with the second variable current supply (152/252) and positioned between a gate of the second driver transistor (MN1) and the first power supply node ($V_{CC}$/$V_{25}$). M9 is a "driver switch element" because it switches on/off the pull-down drive current ($I_2$). Ex-1002, ¶158; Ex-1007, 2:47-50, Figure 4.

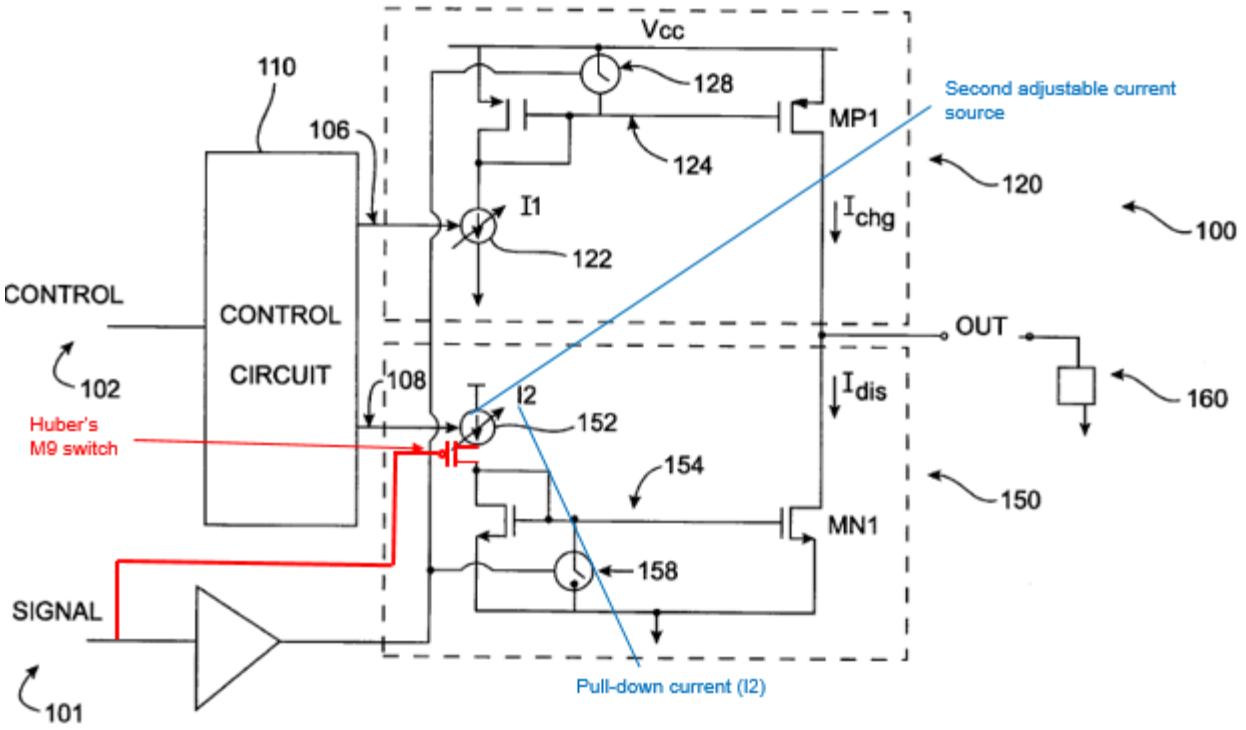



FIG. 1

Ex-1006, Fig. 1 (modified)

The combination of Ozguc and Huber discloses that the second driver switch (M9) and the second variable current supply (152/252) are configured to control the fall time of the output (OUT) of the output driver circuit, as explained below. Ex-1007, 2:47-50, Figure 4; Ex-1002, ¶159. As shown below, when the input

("SIGNAL") rises, M9 switches off and shuts off the pull-down drive current ($I_2$). *Id.*

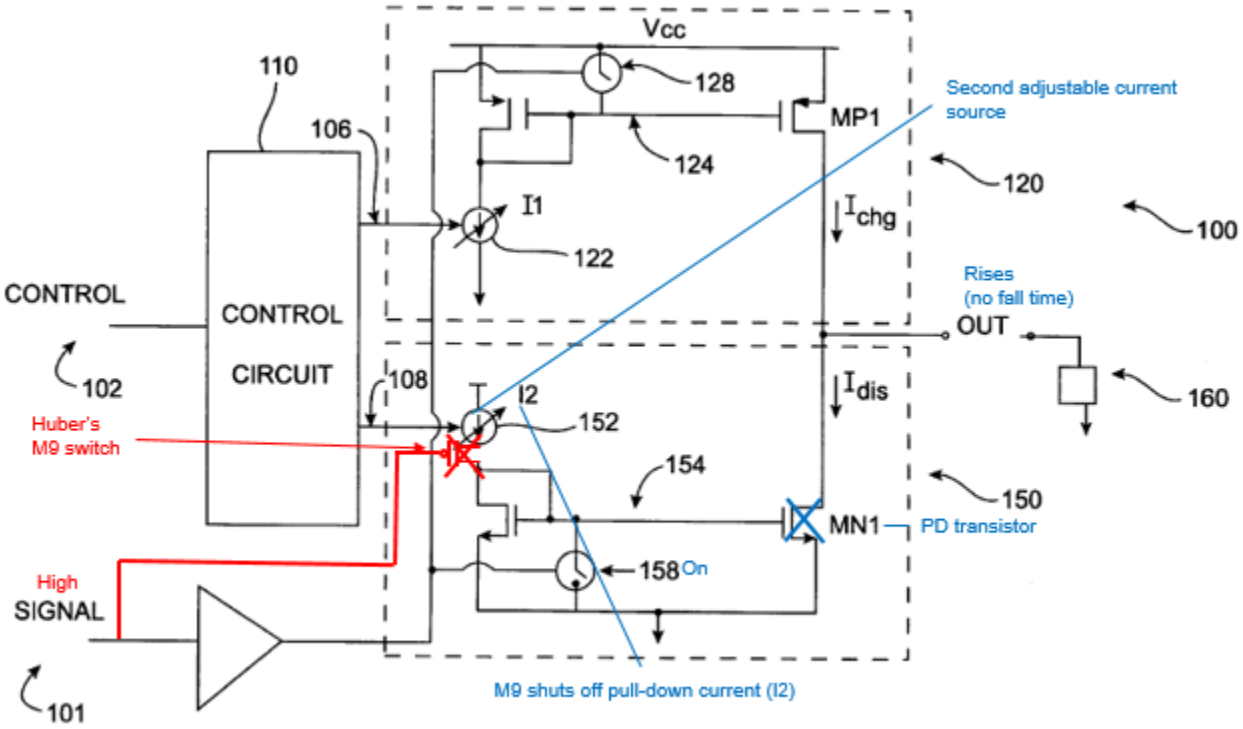



FIG. 1

Ex-1006, Fig. 1 (modified)

As shown in Figure 1 below, when the input ("SIGNAL") falls, M9 turns on and directs the variable pull-down drive current ($I_2$) to the gate of the pull-down/second driver transistor (MN1) to turn on MN1. Ex-1007, Figure 4; Ex-1002, ¶160. The output falls with a fall time depending on the magnitude of $I_2$. Therefore, Ozguc in view of Huber discloses that the second driver switch (M9)

and the second variable current supply (152/252) collectively control the pull-down operation, including the fall time. *Id.*

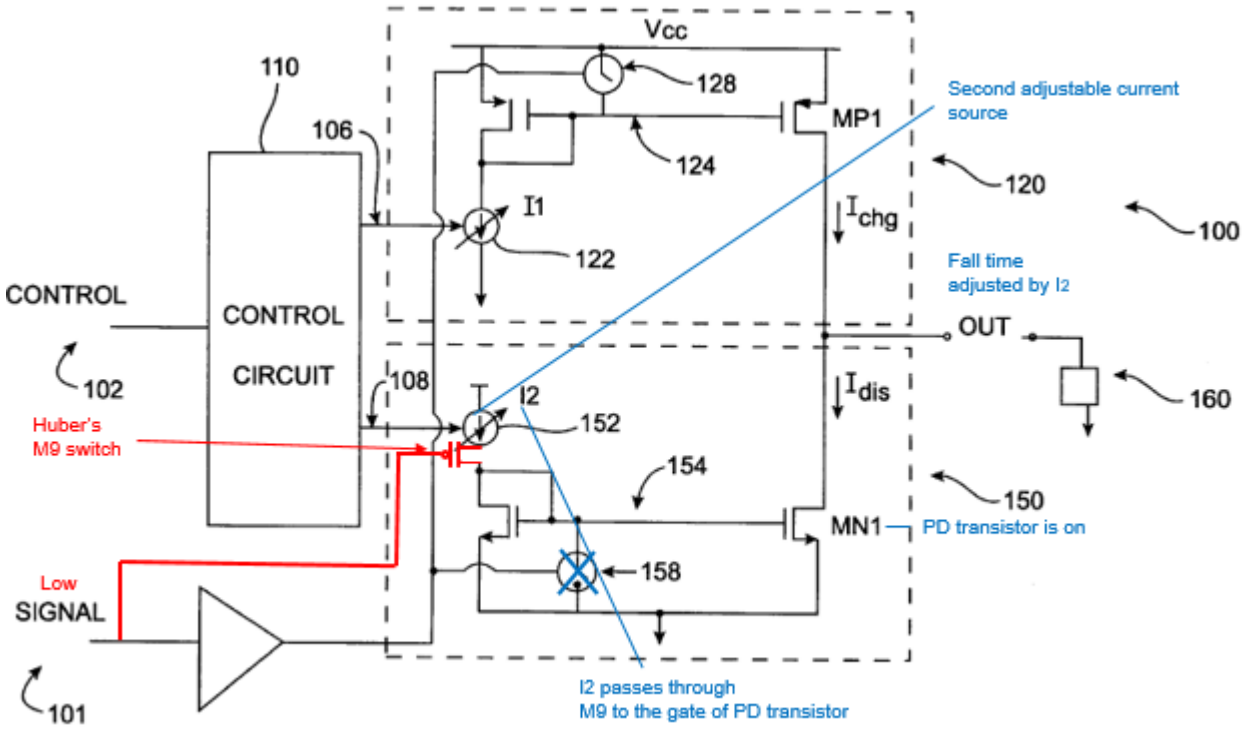



FIG. 1

Ex-1006, Fig. 1 (modified)

Thus, the combination of Ozguc, Huber, and Wu renders claim 3 obvious.

### 4. Claim 4

#### a. 4[a]: The output driver circuit of claim 1, wherein: the first variable current supply comprises a supply current source that provides source current to a reference current node,

To the extent this limitation meets Section 112, it is obvious over Ozguc and Wu.[12]

First, the Ozguc-Wu combination discloses a first variable current supply comprising a compensation current circuit (230) for providing a compensated source current. *See* Section XI.C.2. This combination would have Wu's compensation current circuit (230) provide a compensated control current ($I_{Total}$) to Ozguc's buffer. *Id.* Accordingly, the current ($I_1$) generated by Ozguc's "first adjustable current source" (122/222 in Figs. 1-2) mirrors a total reference current provided by Wu's compensation circuit 230 ($I_1'=I_{CONTROL}=I_{Total}$), as explained in Section XI.C.2. Ex-1006, Fig. 3, 4:10-36; 1:66-2:21, 2:45-65, 2:66-3:43, 3:62-4:9; Ex-1002, ¶¶162-63. Because Wu's compensation circuit (230) modifies the adjustable current generated to drive Ozguc's pull-up transistor (MP1) by supplying Wu's $I_{Total}$ as Ozguc's reference ("CONTROL") current, Wu's

[12] Because "a reference current node" does not appear in the specification, Petitioner reserves the argument that Claim 4 fails to meet Section 112.

compensation circuit (230) would be part of "a first variable current supply" for pull-up, as required by Element 4[a]. *Id.*

Second, the Ozguc-Wu combination discloses that Wu's compensation circuit (230) includes a supply current source (each of "compensation current sources" 301/303/304), as shown in green in Wu's Figure 3 below. Each source (301/303/304) is a "supply current source" because each supplies a source current ($I_A$/$I_C$/$I_D$) that "are added within summing circuit … thereby creating a total compensation [source] current" ($I_{Total}$) that serves as a reference for the first variable drive current (*e.g.*, $I_1$ in Ozguc's Figures 1-3). Ex-1008, 5:23-37, 8:20-44, 10:8-11:3; Ex-1002, ¶164; Section XI.C.2.

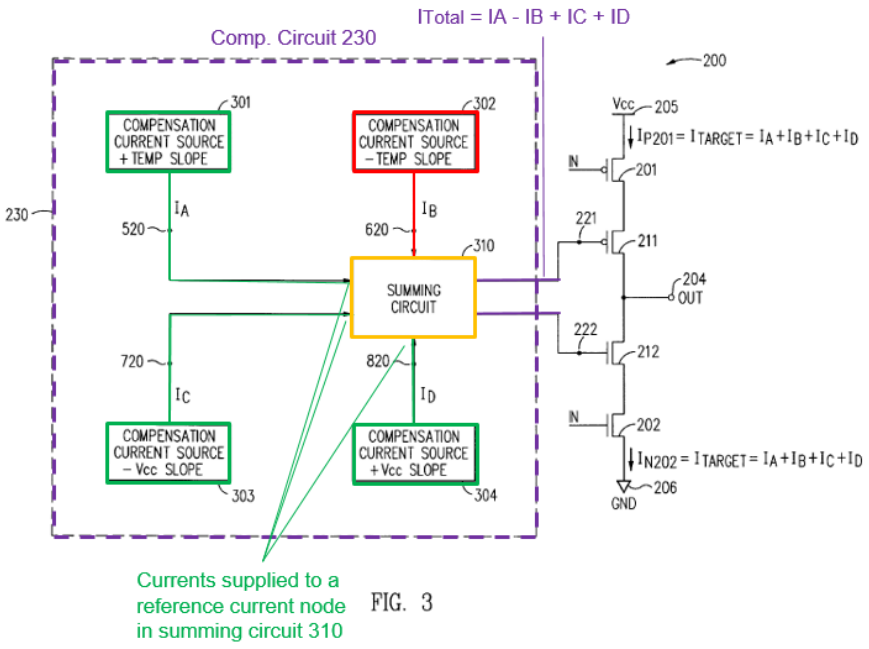



FIG. 3

Ex-1008, Fig. 3

Third, the Ozguc-Wu combination discloses that each supply circuit's compensated current ($I_A$/$I_C$/$I_D$) is provided to a reference current node (annotated dot), shown in Figure 9 of Wu below, which is modified in view of Figure 3. Ex-1002, ¶165. Figure 3 (above) shows that sources 301, 303, and 304 provide the currents ($I_A$, $I_C$, and $I_D$) to nodes 520, 720, and 820, respectively. Figure 9 below is modified to show the connections of sources 301, 303, and 304 to nodes 520, 720, and 820, respectively.

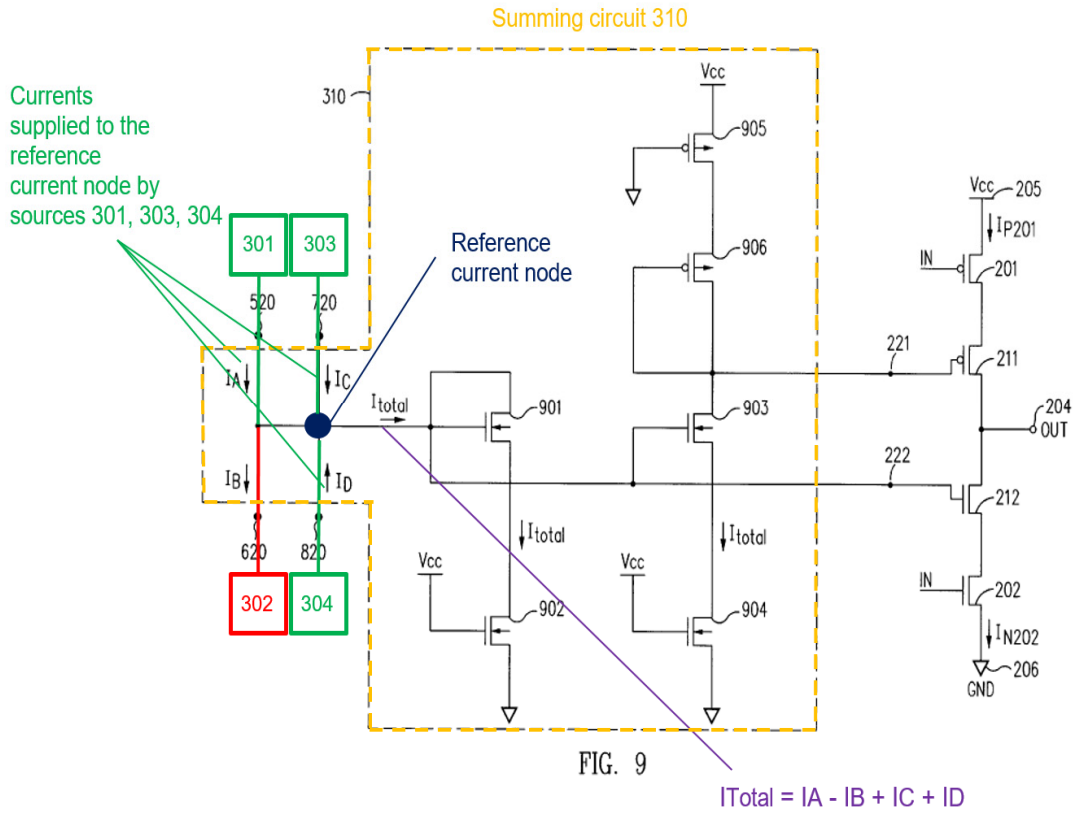



FIG. 9

Ex-1008, Fig. 9 (modified)

In this combination, the current provided by Wu's compensation circuit ($I_{Total}$) would serve as a reference current for Ozguc's adjustable current source (122/152). Ex-1002, ¶166; Section XI.C.2. Accordingly, the node that outputs the total current ($I_{Total}$) is a "reference node." *Id*. Thus, as shown in modified Figure 9 above, the Ozguc-Wu combination discloses that the first variable current supply comprises a supply current source (each of 301, 303, and 304) that provides a source current ($I_A$, $I_C$, and $I_D$, respectively) to a reference current node (annotated above). *Id.*; *see also* Ex-1008, 5:23-33, 8:20-44, 10:8-11:3.

**b. 4[b]: a current mirror that shunts current away from the reference current node**

First, the Ozguc-Wu combination discloses shunting current away from a reference current node. Wu's Figure 9, below, illustrates that compensation current ($I_B$) is drawn away from the reference current node (annotated dot) by an arrow labeled "$I_B$." *See also* 5:66-6:16. Thus, a POSITA would have understood that $I_B$ is shunt from the reference node. Ex-1002, ¶167; Section XI.A.4.b (Element 10(b)).

Second, the Ozguc-Wu combination discloses that the current is shunt away by a current mirror. Wu's Figure 9 shows that the compensation current ($I_B$) is drawn (shunt) away from node 620. Ex-1008, 13:11-58. A POSITA would have understood that $I_B$ is also shunt from the reference current node because the reference current node is connected to node 620. Ex-1002, ¶168. Figure 6 further

discloses that the component of compensation circuit (302) that shunts current ($I_B$) from node 620 is a "current mirror circuit" "form[ed]" by "N-channel FETs 603 and 604." Ex-1008, 10:8-11:8; Section VI.D. To illustrate in one drawing how the circuits in Wu's Figures 6 and 9 are connected, Figure 9 below is modified to show the connection between the output mirror transistor (604) and the summing circuit (310) at node 620. *Id.* As shown in modified Figure 9 below, Ozguc in view of Wu discloses a current mirror (603-604) that shunts current ($I_B$) away from the reference current node, as required by Element 4[b]. Thus, the combination of Ozguc, Huber, and Wu renders claim 4 obvious.

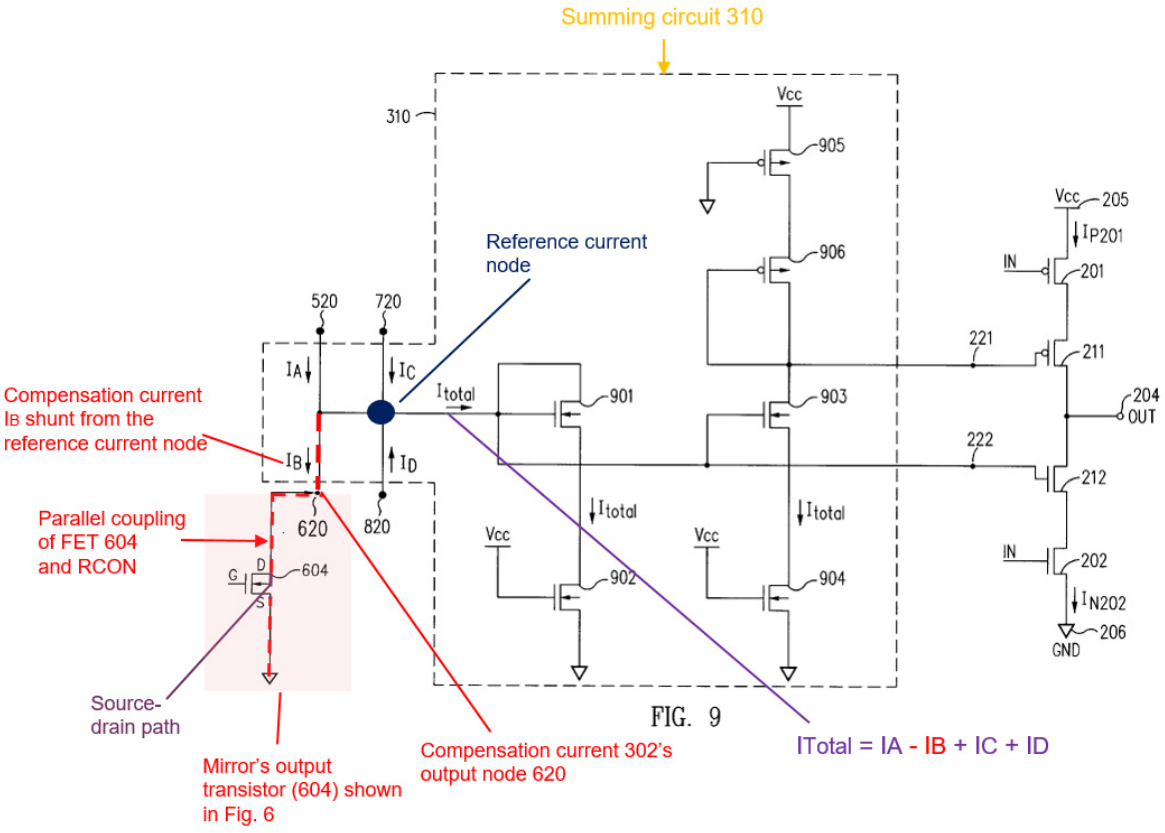



FIG. 9

Ex-1008, Fig. 9 (modified)

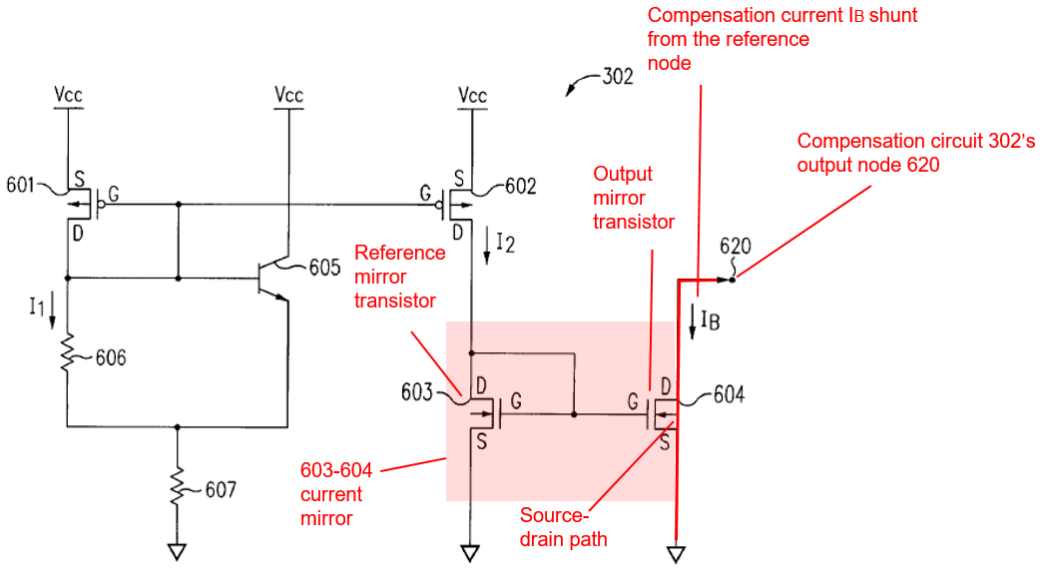



FIG. 6

Ex-1008, Fig. 6

## 5. Claim 5

### a. 5[a]: The output driver circuit of claim 4, wherein: the current mirror includes an output mirror transistor having a source-drain path in series with the supply current source and in parallel with the reference current output node,

To the extent this limitation meets Section 112, it is disclosed by Ozguc in view of Wu.[13]

As shown in Wu's modified Figure 9 and explained below, the output mirror transistor (604) is connected in series with the supply current source 301 and in

[13] Because Element 5[a] recites terms not appearing in the specification, Petitioner reserves the argument that Claim 5 fails to meet Section 112.

parallel with the reference current output node (annotated dot). Ex-1002, ¶¶169-70.

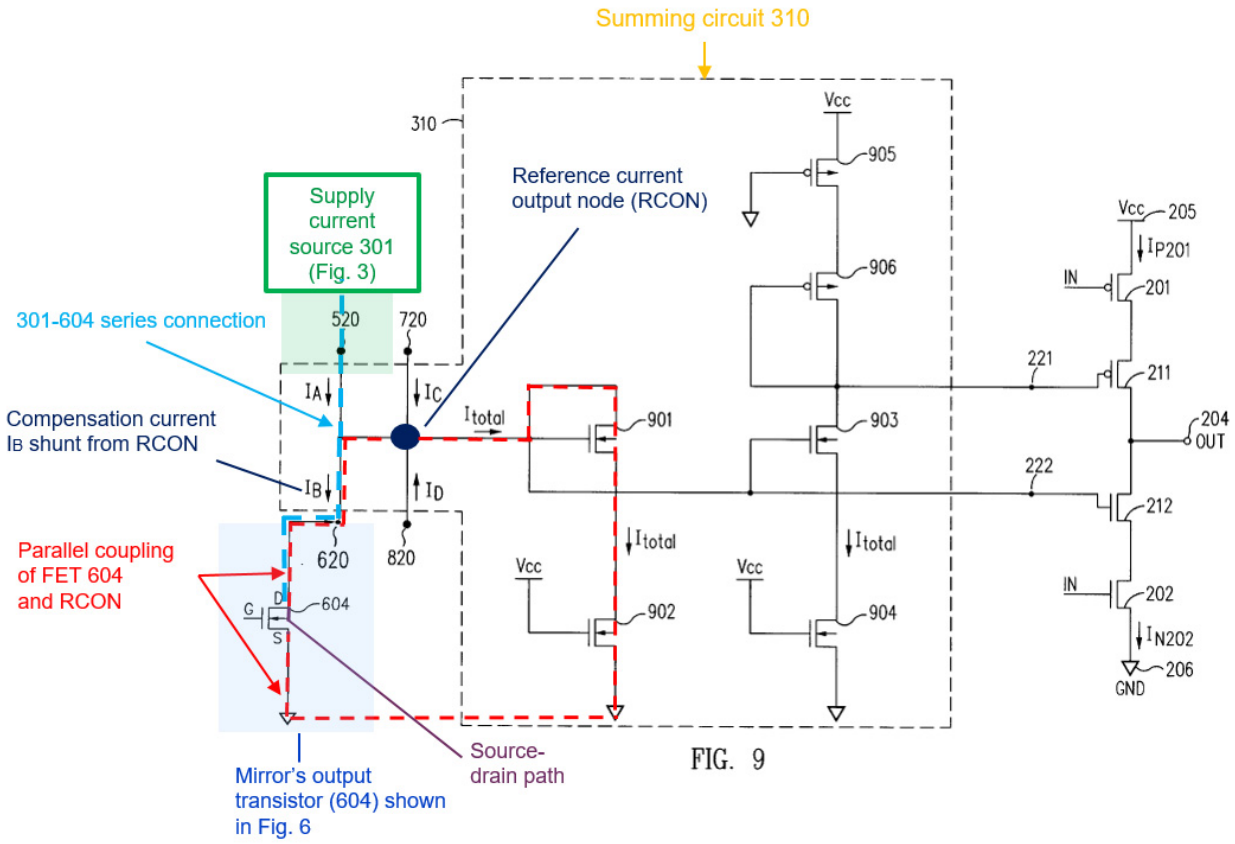



FIG. 9

Ex-1008, Fig. 9 (modified)

Wu's Figure 9 above is modified to show the connections to the circuit components shown in Figure 3 and 6, as explained below. Ex-1002, ¶171. Wu's Figure 9 (annotated below) shows that the summing circuit (310) receives a source current ($I_A$) at node 520. Ex-1008, 13:11-57. As explained for Element 4[a] and shown in Figure 3 below, the Ozguc-Wu combination discloses that a supply current source (*e.g.,* compensation current source 301) is connected via a wire to node 520 to supply $I_A$. Ex-1008, 5:23-53. Figure 9 above is modified to show that

connection. Ex-1002, ¶171. Wu's Figure 9 (annotated below) also shows that current $I_B$ is drawn from node 620 of the summing circuit (310). Ex-1008, 13:11-57. As explained for Element 4[b] and shown in Figure 6 below, the Ozguc-Wu combination discloses that the component of the compensation circuit 302 that draws $I_B$ from node 620 is an output mirror transistor ("FET 604"). *See* Ex-1008, 10:8-65; Section XI.F.4. Figure 9 above is also modified to show that connection.

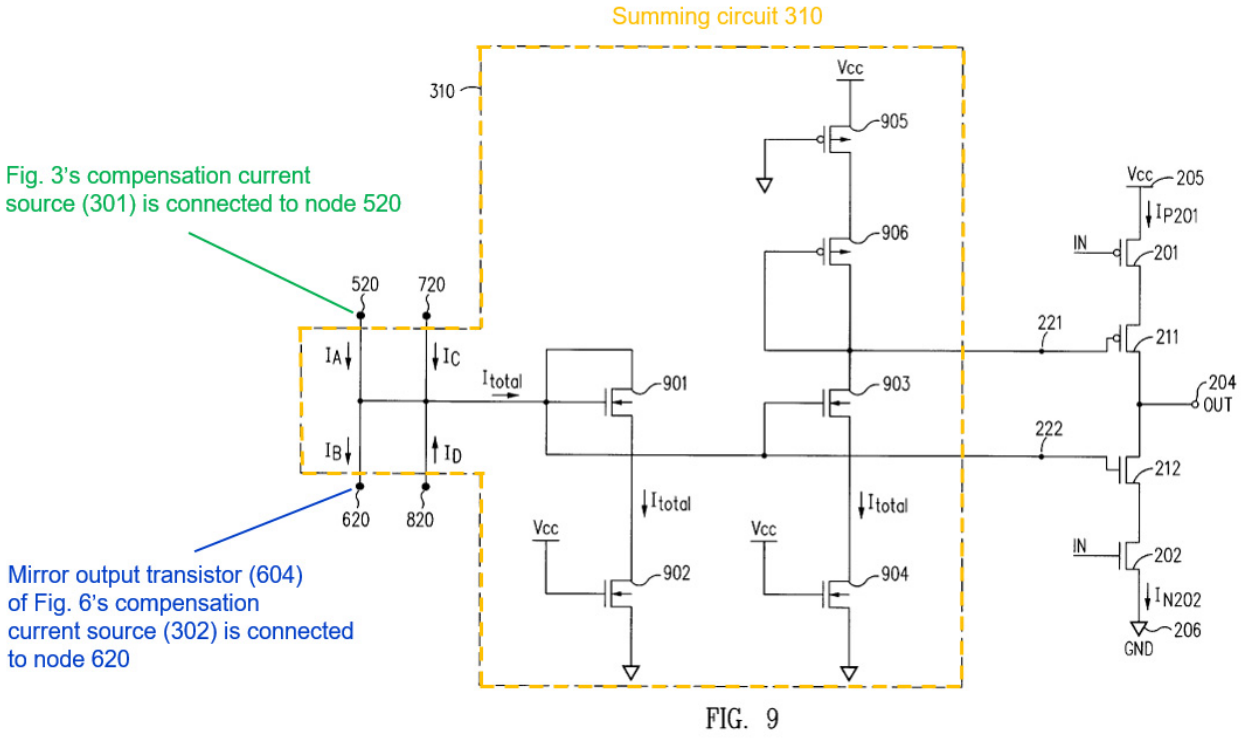



FIG. 9

Ex-1008, Fig. 9 (not modified; only annotated)

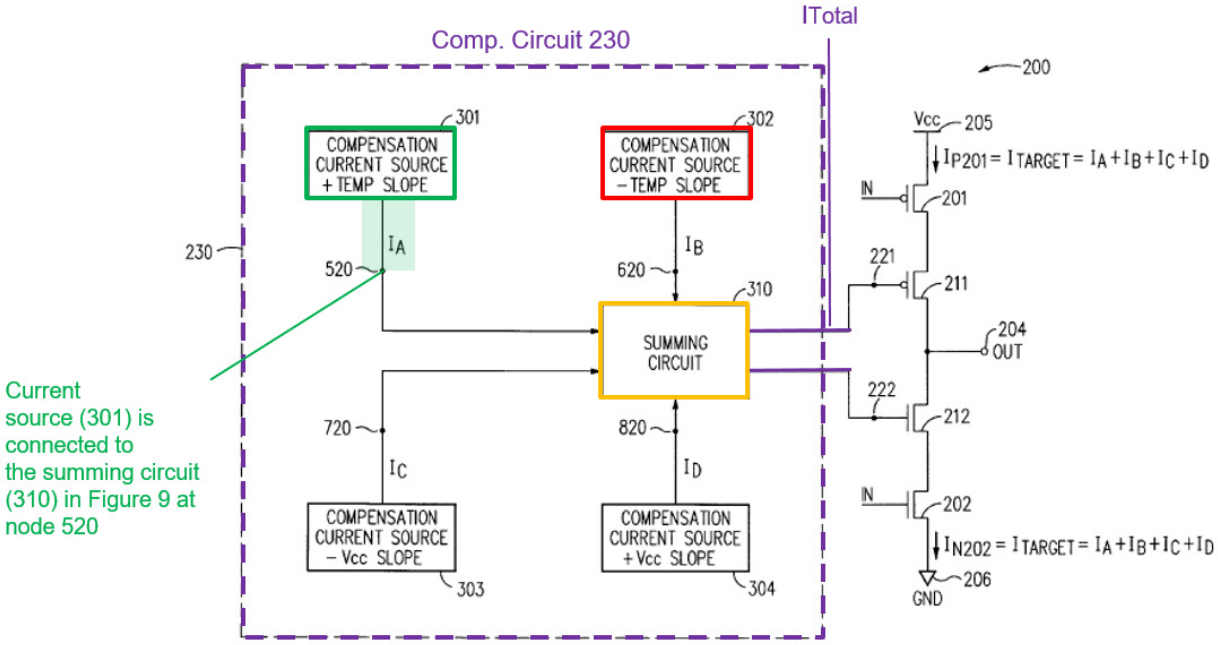



FIG. 3

Ex-1008, Fig. 3

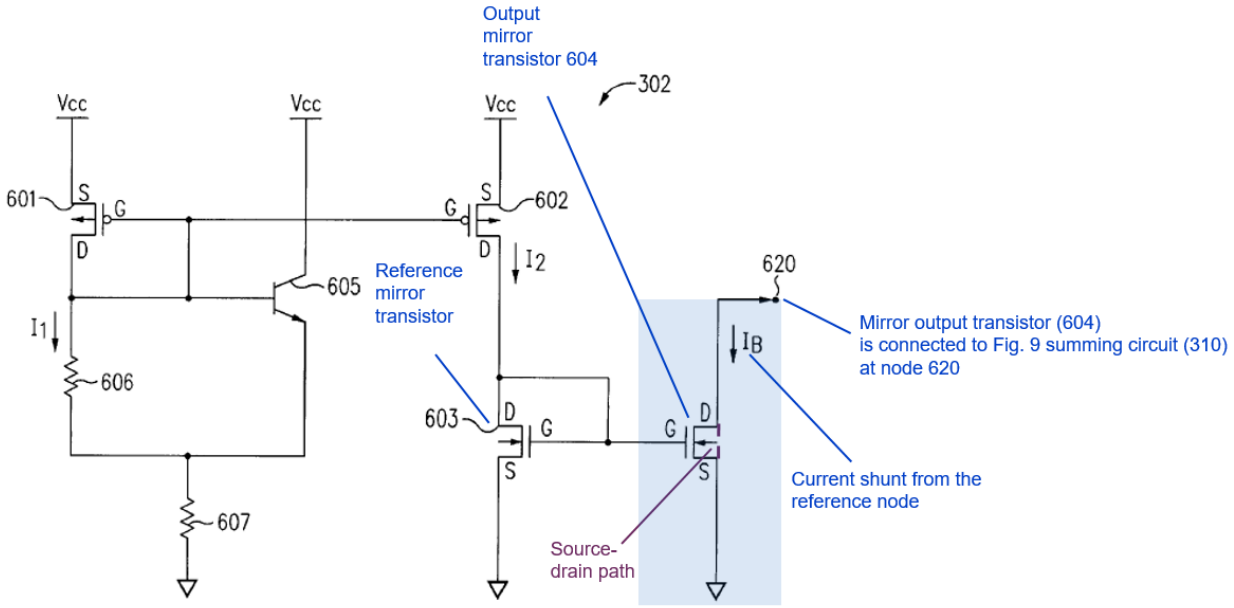
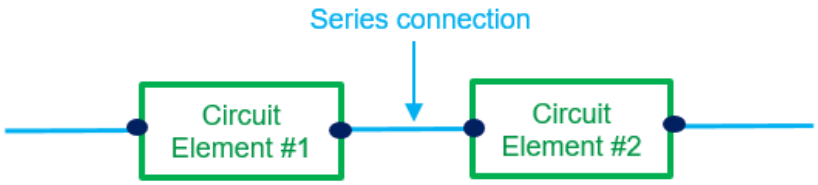



FIG. 6

Ex-1008, Fig. 6

First, the Ozguc-Wu combination discloses that the source-drain path of the output mirror transistor (Wu's FET 604) is connected in series with a supply current source (Wu's current source 301), as explained below. Ex-1002, ¶172. A POSITA would have understood that two circuit elements are connected in series when they are connected along the same conductive path (blue), as shown below. *Id*. As shown in modified Figure 9 above, because the source-drain path of the output mirror transistor (FET 604) and the supply current source 301 are connected along the same path (blue), they are connected in series. *Id.*



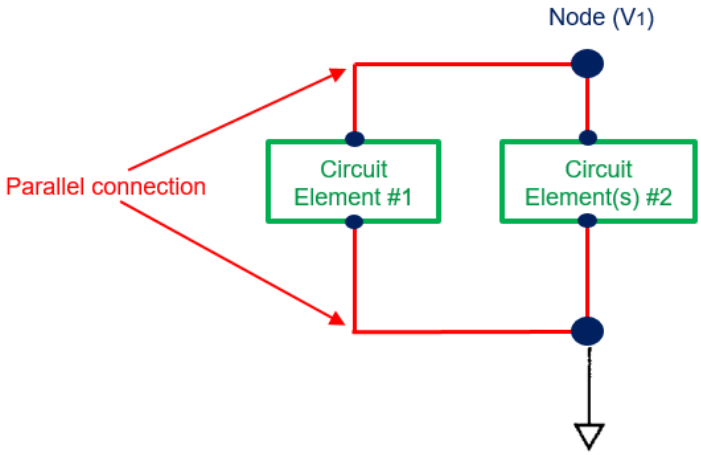

*Id.*

Second, the Ozguc-Wu combination discloses that that output mirror transistor (FET 604)'s source-drain path is in parallel with the reference current output node (as annotated in modified Figure 9 above), as explained below.

The term "reference current output node" lacks antecedent basis. If it refers to "a reference current node" in Element 4[a], Wu discloses this limitation. Wu discloses a reference current output node as annotated in modified Figure 9 above. As shown in modified Figure 9 above, Wu discloses a node that adds the source

currents ($I_A$, $I_C$, and $I_D$) and outputs the total reference current ($I_{Total}$). Ex-1008, 5:23-33, 13:11-20; Ex-1002, ¶¶173-74. As explained above, the Ozguc-Wu combination would use Wu's $I_{Total}$ as a reference current (*e.g.,* "CONTROL" current in Ozguc's Figure 2) for Ozguc's adjustable current source (122/152). *Id.*; Section XI.C.2. Thus, the node that outputs $I_{Total}$ is a "reference current output node." *Id.*

As shown below, a POSITA would have understood that Circuit Element #1 is connected in parallel with a node ($V_1$) that is connected through one or more Circuit Element(s) #2 to Ground because Element #1 provides an alternative path between $V_1$ and Ground without going through Element(s) #2. Ex-1002, ¶175.




*Id.*

As shown in Wu's modified Figure 9 above, FET 604's source-drain path has a parallel connection (in red) with the reference current output node because the FET's drain (the first circuit element's first port) is connected to the node, and

the FET's source (the first circuit element's second port) is connected to Ground, thus the source-drain path providing an alternative path between the node and Ground as compared to the path from the node through other circuit elements (*e.g.*, FETs 901 and 902) to Ground. *Id.*, ¶176; Ex-1008, 10:8-65, 13:11-58. Therefore, Ozguc in view of Wu discloses Element 5[a].

**b. 5[b]: a reference mirror transistor having a gate coupled to a gate of the output mirror transistor and to its drain,**

As shown in Figure 6 above, Wu discloses that "[t]he drain of n-channel [reference mirror] FET 603 is coupled to the gates of n-channel FET[] 603 and [n-channel output mirror FET] 604." Ex-1008, 10:23-27; Ex-1002, ¶177. Therefore, Wu discloses that the current mirror (603-604) includes a reference mirror transistor (FET 603) having a gate coupled to a gate of the output mirror transistor (FET 604) and to its (FET 603's) drain. Thus, Ozguc in view of Wu discloses Element 5[b].

**c. 5[c]: an impedance element coupled to the drain of the reference mirror transistor.**

Wu's Figure 6, below, discloses a transistor (602) coupled to the drain of the reference mirror transistor (603). Ex-1008, 10:9-65. Transistor (602) serves as an "impedance element" because its impedance can be adjusted based on the transistor's gate voltage. *Id.*; Ex-1002, ¶178; Section VI.A-B. Therefore, Wu discloses Element 5[c]. Ex-1001, 2:35-38; 1:45-57, claims 7 and 11.

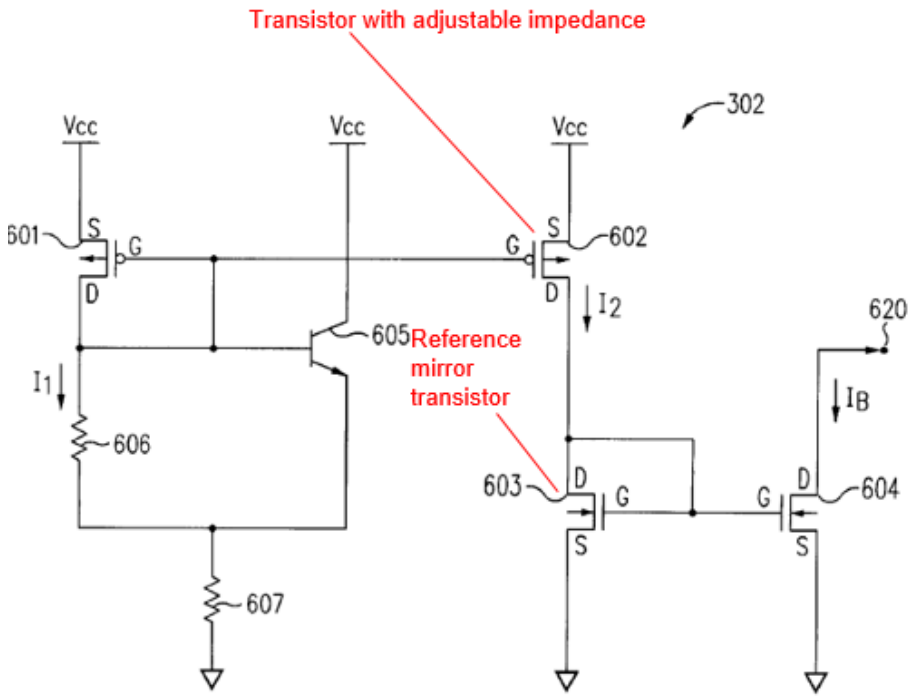



FIG. 6

Ex-1008, Fig. 6

If Patent Owner argues that the "impedance element" is limited to a resistor, that interpretation conflicts with the '455 patent's disclosure that a transistor can provide an "impedance path." *Id.* But even under this interpretation, this limitation is obvious over Ozguc and Wu. Wu discloses two resistors 606 and 607 coupled to the drain of the reference mirror transistor 603. Wu's Figure 6, below, shows resistors 606 and 607 coupled to transistor 602's gate, which is capacitively

coupled to its drain,[14] which in turn is coupled to the reference mirror transistor (603)'s drain. Ex-1002, ¶179.

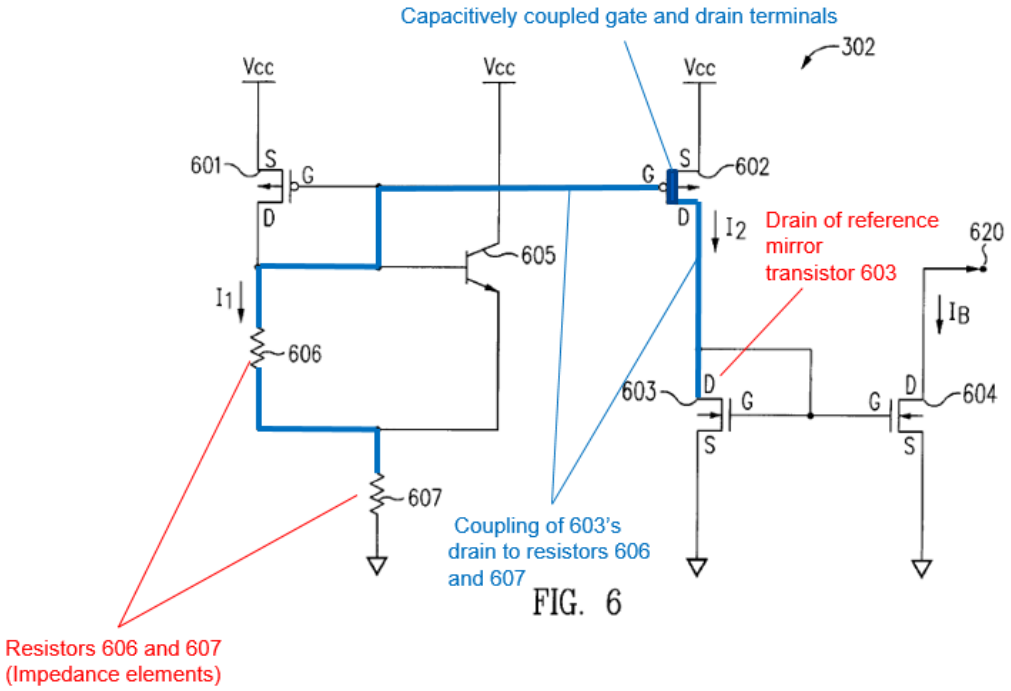



FIG. 6

Ex-1008, Fig. 6

As explained in Section XI.C.2, a POSITA would have been motivated to use the total compensated current ($I_{Total}$) from Wu's compensation circuit 230 as the input ("CONTROL") signal to Ozguc's buffer circuit such that Ozguc's adjustable drive current is stabilized under various operating conditions. Wu discloses that resistors 606/607 are included in the compensation current source

[14] An FET's gate is "capacitively couple[d]" to the source-drain channel. Ex-1011, 207; Ex-1002, ¶179.

circuit (302) of the compensation circuit (230) to allow the designer to adjust a component ($I_B$) of the total compensated current ($I_{Total}$). Ex-1008, 10:46-52, Figs. 3, 6. Accordingly, a POSITA would have been further motivated to include resistors 606/607 in the compensation circuit (230) added to Ozguc's buffer to provide the designer additional flexibility to adjust the reference for the drive current, as taught by Wu. Ex-1002, ¶¶180-81.

Therefore, Ozguc in view of Wu discloses an impedance element (transistor 602, or resistors 606/607) coupled to the drain of the reference mirror transistor (603). Thus, the combination of Ozguc, Huber, and Wu renders claim 5 obvious.

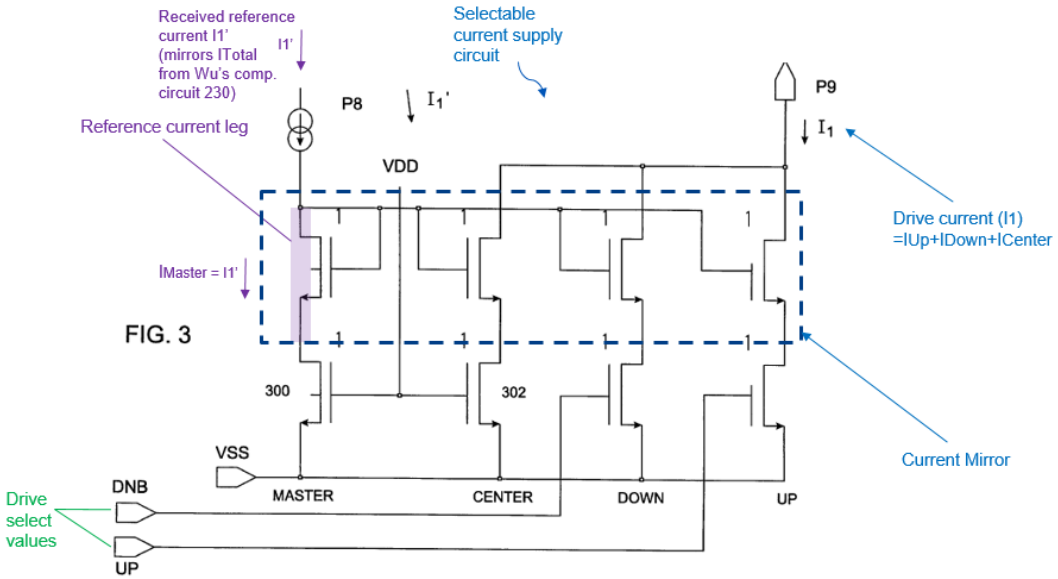
**6. Claim 6**

**a. 6[a]: The output driver circuit of claim 1, wherein: the first variable current supply includes a selectable current supply circuit that includes a current mirror having a reference current leg that receives a current having at least one component that is inversely proportional to the power supply voltage,**

Ozguc discloses that the first adjustable current source (122/222 in Figs. 1-2) includes a selectable section (222b) that may include the current-leg structure shown in Figure 3 below. *See* Section XI.A.1. Ozguc's Figure 3 circuit is a "selectable current supply circuit" because it supplies a current ($I_1$) that can be selectively changed (*e.g.,* using drive select values "UP" and "DNB"). Ex-1002, ¶182; Ex-1006, 4:10-46.

Ozguc further discloses that the upper transistors of the four legs in Figure 3 form a current "mirror" having a mirror reference transistor (the upper transistor of the Master leg) and three output transistors (the upper transistors of the Center, Up, and Down legs). Ex-1006, 4:10-46, Fig. 3; Ex-1002, ¶¶183-84; Section XI.A.1. The source-drain path of Master's upper transistor provides a "reference current leg" as annotated in Figure 3 below because it provides a reference current ($I_{Master}$) for the drive current ($I_1$). *Id.*; Ex-1006, 1:66-2:21, 2:45-65, 2:66-3:43, 3:62-4:9. As shown in Figure 3, the Master/reference current leg receives a reference current ($I_1'$). As explained above in Ground 4 for claim 9, Ozguc in view of Wu discloses that the reference current ($I_1'$) has a component ($I_C$) that is inversely proportional to the power supply voltage ($V_{CC}/V_{25}$). *See* Section XI.C.2-4.

Therefore, Ozguc in view of Wu discloses Element 6[a].




Ex-1006, Fig. 3

**b. 6[b]: a mirror current leg coupled to a selectable drive current node that mirrors the current flowing in the reference current leg,**

To the extent this limitation meets Section 112, an example of "a mirror current leg" may be the static current leg shown in Figure 2A below. Ex-1001, 3:64-4:13. The static leg always provides a current that mirrors the current in the reference current leg. *Id.* An example of "a selectable current node" may be node 230 because the drive current that is output from this node can be selectively adjusted. *Id.*; Section VII.

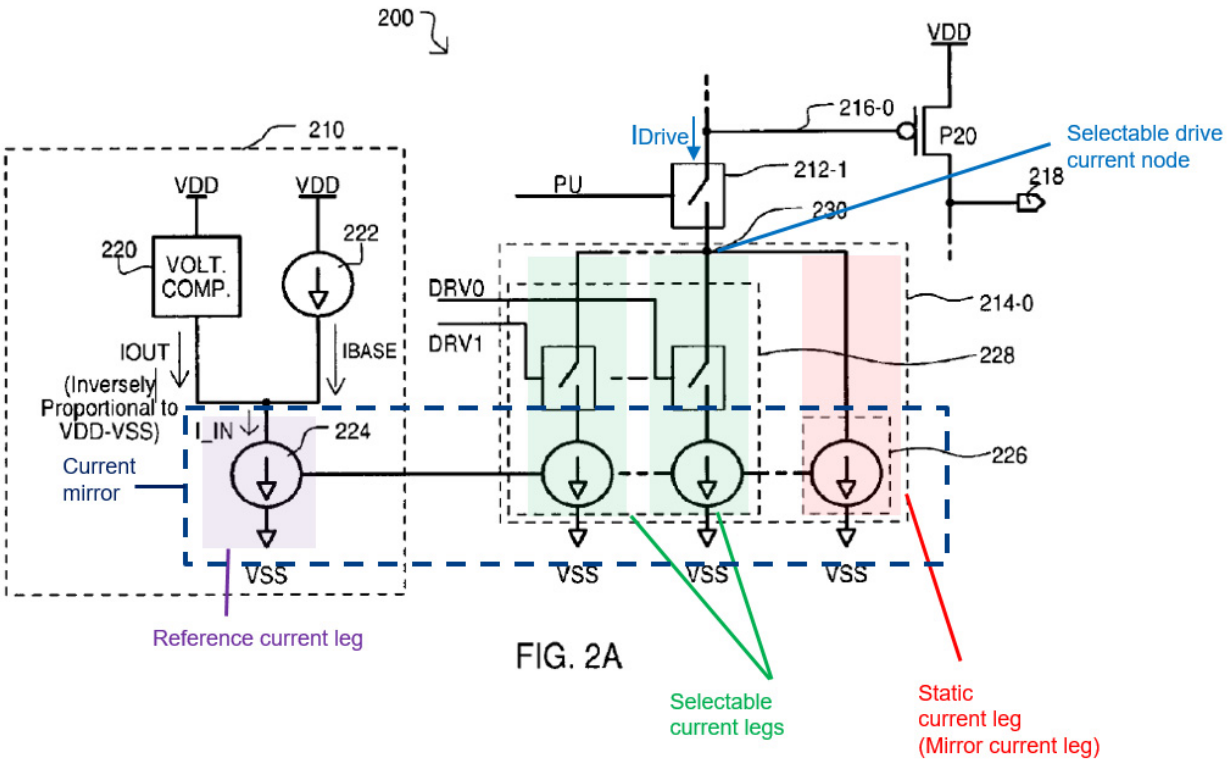
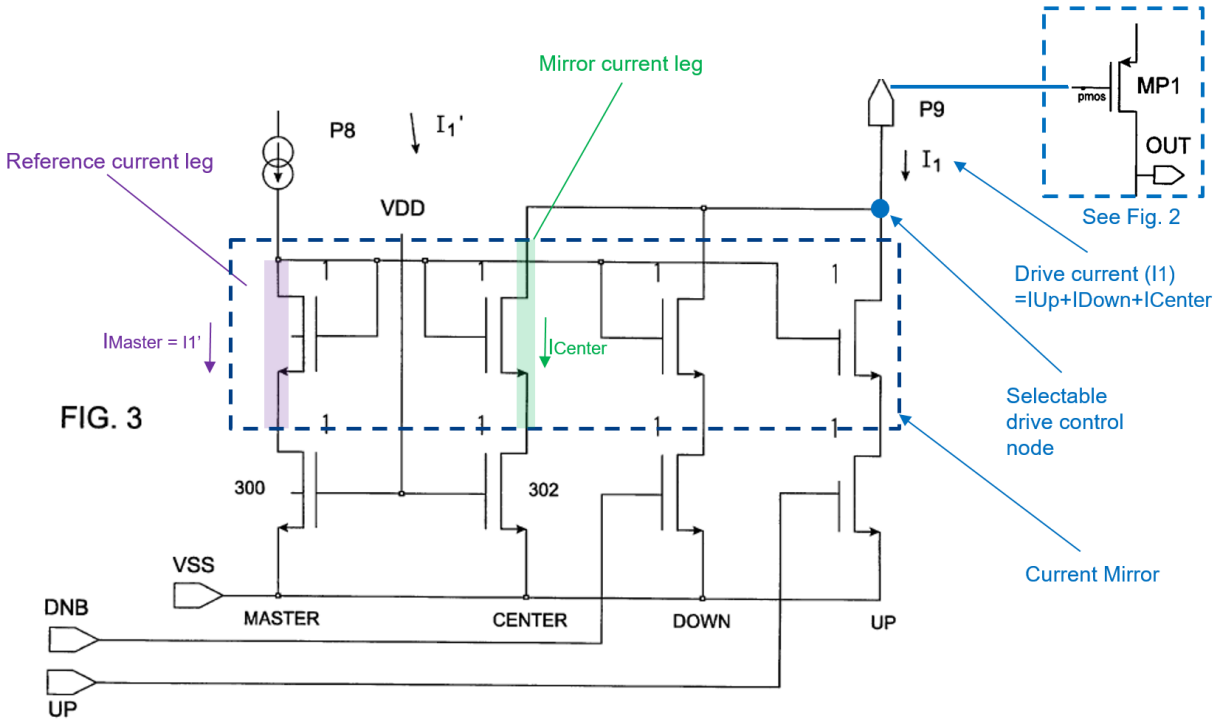



FIG. 2A

Ex-1001, Fig. 2A

Element 6[b] is disclosed by the combination of Ozguc, Huber, and Wu because Ozguc's current-leg structure is very similar to the structure shown in Figure 2A of the '455 Patent.[15] Ozguc's Center leg is a "current mirror leg" because like the static leg of Figure 2A of the '455 Patent, it "remain[s] on" and "mirrors" the reference current ($I_1$') in the Master upper transistor. Ex-1006, 4:10-36; Sections XI.A.1 and XI.A.4 (Element 10[c]). Ozguc also discloses that the Center current mirror leg is connected to the node at which current is output. Ex-1006, Fig. 3; *id.,* 4:10-58; 1:66-2:21, 2:45-65, 2:66-3:43, 3:62-4:9; Ex-1002, ¶¶185-86. This node is "a selectable drive current node" because the drive current output from this node can be selectively adjusted and is provided for driving the first driver transistor (MP1). *Id.* Thus, Ozguc discloses Element 6[b].

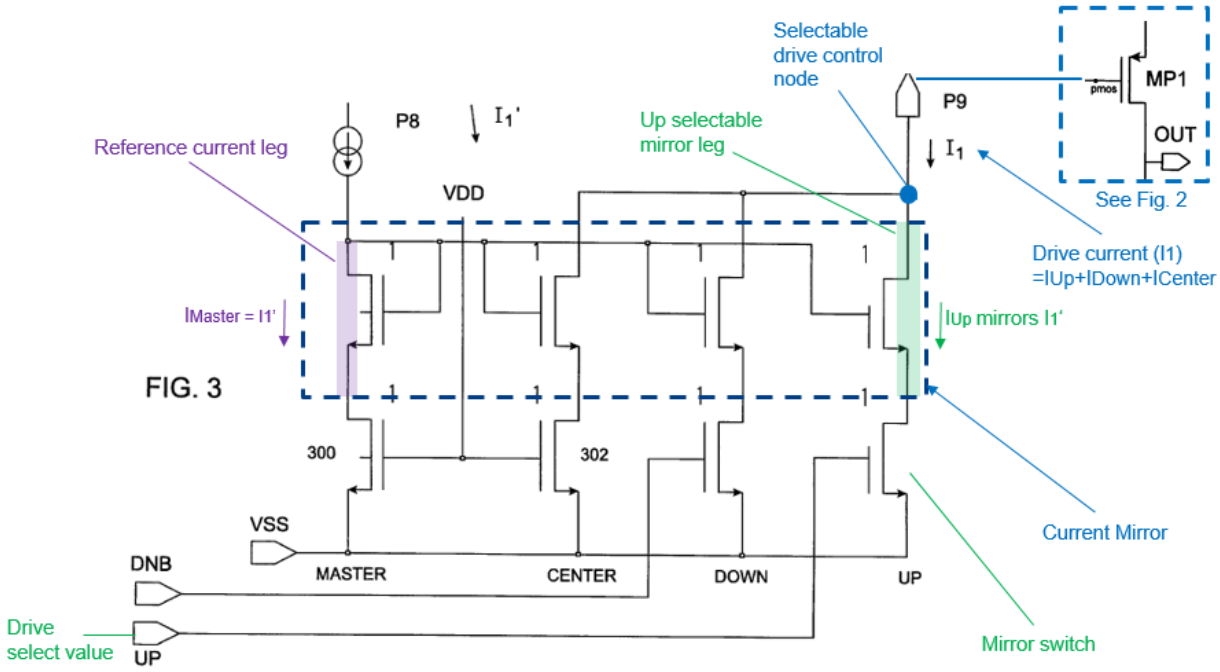
[15] Because "a selectable drive current node" does not appear in the specification, Petitioner reserves the argument that Claim 6 fails to meet Section 112.




Ex-1006, Fig. 3

**a. 6[c]: at least one first selectable mirror leg coupled to the selectable drive current node and coupled to mirror the current flowing in the reference current leg, and**

Ozguc discloses that the first adjustable current source 222 includes an Up leg with an upper transistor that mirrors the current flowing in the Master leg (reference current leg), as shown in Figure 3 below. *See* Section XI.A.1. The source-drain path of Up's upper transistor is a "selectable mirror leg" because the current flowing through it can be selectively turned on or off using the drive select value "UP." Ex-1006, Fig. 3, 4:10-36; Ex-1002, ¶187. Therefore, Ozguc discloses Element 6[c].




Ex-1006, Fig. 3

**b. 6[d]: a mirror switch coupled in series with the at least one selectable mirror leg that is enabled in response to a drive signal.**

Ozguc discloses a switch (bottom MOS transistor) in each leg of its current mirror that turns on or off the current in that leg. *See* Section XI.A.1. Thus, Ozguc discloses a mirror switch (*e.g.,* bottom MOS transistor in Up leg) is coupled in series with the Up selectable mirror leg, as shown in Figure 3. Ex-1006, Fig. 3, 4:10-36; Ex-1002, ¶¶188-89. The switch and the Up leg are enabled in response to a drive signal ("UP"). *Id.* Therefore, Ozguc discloses Element 6[d].

Thus, the combination of Ozguc, Huber, and Wu renders claim 6 obvious.

### 7. Claim 14

#### a. 14: The output driver circuit of claim 3, wherein: the second driver transistor includes an n-channel insulated gate field effect transistor, and the first power supply node is a high power supply node and the second power supply node is a low power supply node.

As explained in Section XI.A.3.a, Ozguc discloses a second driver transistor (MN1) for pulling down the output. A POSITA would have understood that MN1 refers to an NMOS or n-channel insulated gate field effect transistor. Ex-1011, 83; Ex-1002, ¶191. Ozguc discloses the limitations regarding the supply nodes for the reasons stated above for Claim 2.

Thus, the combination of Ozguc, Huber, and Wu renders claim 14 obvious.

## XII. CONCLUSION

The invalidity grounds presented above are reasonably likely to prevail, and thus *inter partes* review should be instituted.

Respectfully Submitted,

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## CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Petitioner certifies that this petition includes 13983 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under §42.8, certificates of service and word count, and exhibit list.

## CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §42.6(e) and §42.105 that on July 16, 2020, a true and correct copy of the Petition for *Inter Partes* Review of U.S. Patent No. 8,373,455 challenging claims 1-14 was served via express mail on the below correspondence address of record:

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