UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

WESTERN DIGITAL CORPORATION, WESTERN DIGITAL TECHNOLOGIES, INC., AND SANDISK, LLC

Petitioners

v.

Martin Kuster

Patent Owner.

Inter Partes Review No. IPR2020-01410

U.S. Patent No. 8,705,243

PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 8,705,243 PURSUANT TO 35 U.S.C. §§ 311-319, 37 C.F.R. § 42

TABLE OF CONTENTS

TABLE OF AUTHORITIES

CASES

STATUTES

OTHER AUTHORITIES

Petitioners Western Digital Corporation ("WDC"), Western Digital Technologies, Inc. ("WDT") and SanDisk, LLC ("SanDisk") (collectively, "Petitioners") respectfully request *inter partes* review ("IPR") in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.* of claims 1-18 of U.S. Patent No. 8,705,243 ("the '243") ("Challenged Claims").

I. INTRODUCTION

The '243 claims well-known prior art mechanical designs for connectors on "external storage devices" such as USB flash drives. The '243 purports to have innovated USB connectors compatible with both the USB 2.0 and USB 3.0 protocols. But the USB 3.0 standard, which issued years earlier, mandates that USB 3.0 connectors be backward-compatible with USB 2.0 and describes in detail the connector design necessary to support both USB protocols.

The '243's alleged "innovation" involves nothing more than providing the two tiers of connector contacts, which are already called for by the USB 3.0 standard, and arranging them exactly as taught by the standard and a host of other prior art references.

The '243 does not teach anything new about the device's dimensions, electronics, or manufacturing. In fact, the '243 claims lack any inventive features.

This is underscored by Hsiao (Ex. 1009) and Chen (Ex. 1010)[1], prior art references disclosing USB flash drives having connectors identical to those claimed in the '243, in addition to the other references cited herein.

Petitioners respectfully request that IPR be instituted and the Challenged Claims canceled as unpatentable.

II. MANDATORY NOTICES (37 C.F.R. § 42.8(b))

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioners WDC, WDT and SanDisk are the real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The '243 was the subject of a civil action in *Kuster v. Western Digital Corporation,* Case No. 3:20-cv-01089, filed in the U.S. District Court for the Northern District of Texas, Dallas Division, which was dismissed by Patent Owner. The '243 is the subject of a civil action in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA, filed June 24, 2020 and currently pending in the U.S. District Court for the Western District of Texas (Waco) ("the Litigation").

[1] The Exhibit List is attached as Appendix B.

Petitioner is simultaneously filing an IPR Petition requesting review of U.S. Patent No. 8,693,206 ("206), a continuation of the '243. *See Western Digital Corporation, et al., v. Kuster*, IPR2020-01391.

C. Lead and Backup Counsel (37 C.F.R. § 42.8(b)(3))

Petitioners provide the following designation of counsel:

Lead Counsel	Backup Counsel
Erica D. Wilson USPTO Reg. No. 42,230 WALTERS WILSON LLP 702 Marshall St., Suite 611 Redwood City, California 94063 Tel.: 650-248-4586 ericawilson@walterswilson.com	Eric S. Walters USPTO Reg. No. 45,422 WALTERS WILSON LLP 702 Marshall St., Suite 611 Redwood City, California 94063 Tel.: 650-817-5625 eric@walterswilson.com

D. Service Information (37 C.F.R. § 42.8(b)(4))

Please address all correspondence and service to lead counsel and back-up counsel at the addresses listed above. Petitioners consent to electronic service by email to ericawilson@walterswilson.com, eric@walterswilson.com.

III. IPR REQUIREMENTS (37 C.F.R. § 42.104)

A. Standing (37 C.F.R. § 42.104(a))

Petitioners certify: (1) the '243 is available for IPR; and (2) Petitioners are not barred or estopped from requesting IPR of the Challenged Claims. The '243

issued April 22, 2014, and this Petition is being filed within one year of service of Complaints against Petitioners alleging infringement of the '243 (*see* Section II.B) and is not barred under 35 U.S.C. § 315(b).

B. Challenge Under 37 C.F.R. § 42.104(b)

Petitioners request IPR of the Challenged Claims on the following grounds:[2]

Ground	Claims	Basis
1. Hsiao	1-4, 9-13, 18	35 U.S.C. § 102
2. Hsiao	1-4, 9-13, 18	35 U.S.C. § 103
3. Hsiao-Sun	1-18	35 U.S.C. § 103
4. Chen-Cheng	1-6, 9-15	35 U.S.C. § 103
5. Chen-Cheng-Hiller	7-8, 16-17	35 U.S.C. § 103
6. Chen-Sun	1-18	35 U.S.C. § 103
7. Chen-Cheng-Wan	18	35 U.S.C. § 103

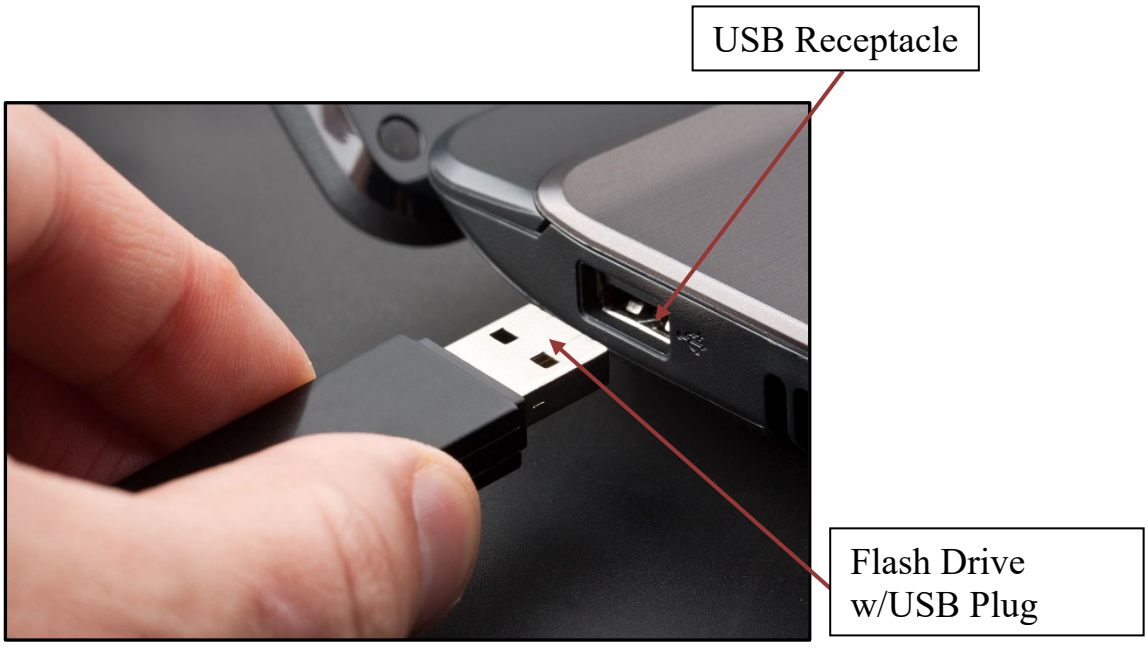
[2] The '243 is a pre-AIA patent; all references to the United States Code are to pre-AIA versions.

IV. STATE OF THE ART

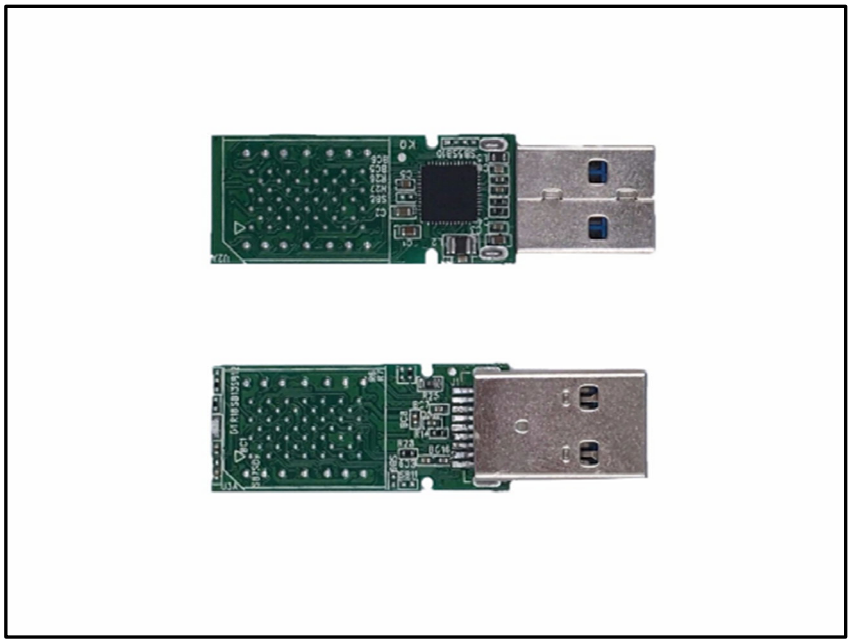
The ’243 is directed to connectors for “external storage device[s]” such as Universal Serial Bus (“USB”) flash drives (termed “USB sticks”) having multiple interfaces, thus allowing them to be connected to more than one type of receptacle—e.g., USB 2.0 and USB 3.0 receptacles. Ex. 1001, 1:22-23, 2:30-32, 1:65-2:2.

A. USB Flash Drives

USB flash drives are data storage devices having USB connection interfaces. Their primary components are memory for data storage, a controller communicating with memory to manage read/write operations and ensure compliance with the USB protocol, and a plug that allows the device to be connected to a USB receptacle on a host device, *e.g.,* a laptop.



The memory, controller and plug connector are mounted on a substrate such as a printed circuit board ("PCB"), as exemplified below:



See Ex. 1005, ¶¶ 50-52.

B. USB 2.0 and 3.0 Standards

The USB standard governs the design of the USB connections. Ex. 1001, 1:33-45. USB standards (termed "Specifications") are issued by the USB Implementers Forum ("USB-IF"). Ex. 1019, ¶¶ 1-10. The USB-IF promulgated

the USB 2.0 and USB 3.0 Specifications in 2000 and 2008, respectively. *Id.*, 1:37-45; Ex. 1019, ¶¶ 1-10.

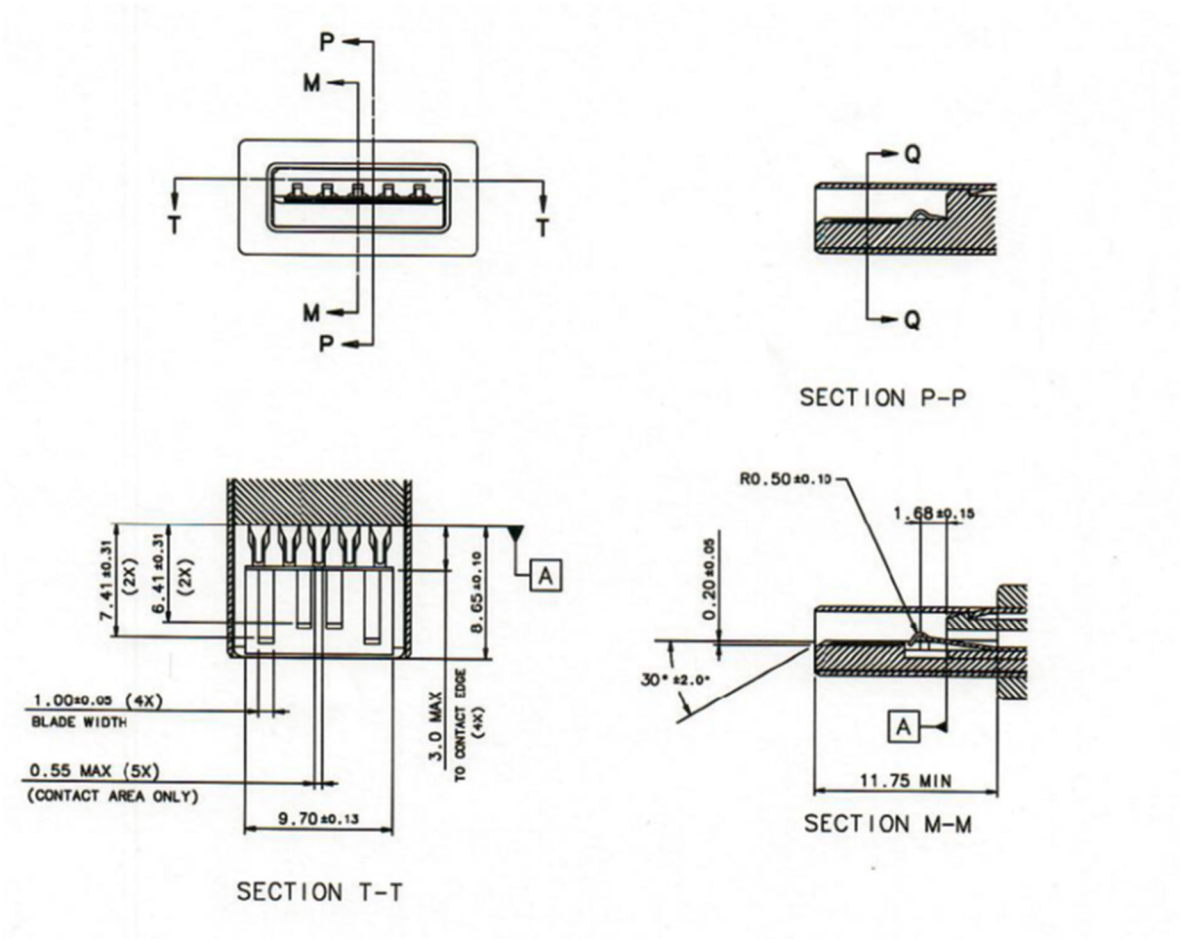
Flash drive USB 2.0 connectors commonly conform to USB Standard-A, and have four non-resilient metal contacts that transfer power, ground, and serial differential data D+ and D- signals. These contacts are embedded in an insulative housing or directly on a PCB or other substrate. Ex. 1005, ¶¶ 53-61.

USB 2.0 supports three bus speeds, and USB 3.0 supports a fourth, faster bus speed termed "SuperSpeed." Ex. 1001, 1:33-47. The USB 3.0 Specification defines a dual-bus architecture with two physical buses – the USB 2.0 bus and the USB 3.0 SuperSpeed bus – operating in parallel. Ex. 1008 at 3-1 through 3-2; Ex. 1005, ¶ 62.

The USB 3.0 Specification identifies backward compatibility as a "key design area[]" (Ex. 1008 at 1-3) and requires USB 3.0 devices to be backward compatible with USB 2.0. *Id.* at 3-1. A USB 3.0 Standard-A compliant plug must fit both USB 2.0 and USB 3.0 receptacles. *Id.* at 5-2, Section 5.2.1.1 and Table 5-1; Ex. 1005, ¶¶ 63-64.

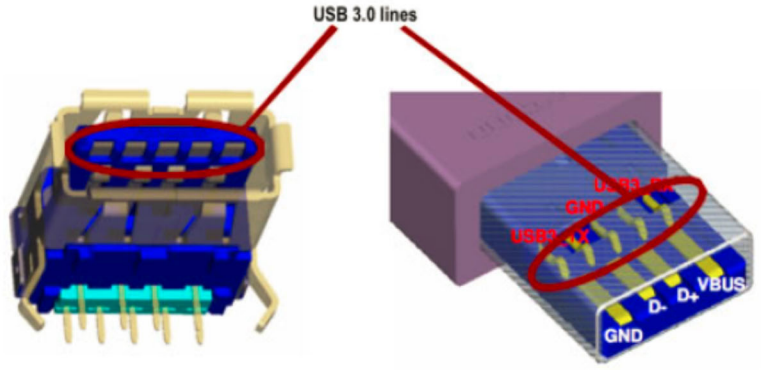
Accordingly, USB 3.0 Standard-A plugs have the same form factor and the same four metal contacts as USB 2.0 Standard-A plugs. Ex. 1008, Section 5.3.1.1. To support SuperSpeed, the USB 3.0 Specification adds five contacts—two signal pairs (denoted StdA_SSTX-, StdA_SSTX+ and StdA_SSRX-, StdA_SSRX+) and

a grounding contact. *Id.* at 5-14; *see also id*, Section 5.3.1.2 and Table 5-2. The contacts are arranged in a two-tier configuration with "SuperSpeed" contacts sitting behind the USB 2.0 contacts and a portion of the SuperSpeed contacts above the USB 2.0 contacts. *Id.* at 5-4, Section 5.3.1; *see also id.*, Fig. 5-2 (showing two-tier contact arrangement) (excerpt reproduced below):



These contacts can be integrated into a plastic housing which the USB 3.0 Specification recommends be colored blue to signal compatibility with USB 3.0. Ex. 1008 at 5-14. *See* Ex. 1005, ¶¶ 65-69.

The contact arrangement is depicted in a 2009 "Techspot" article:



Ex. 1015; Ex. 1005, ¶ 70.

C. Chip-on-Board ("COB") Technology

Prior art flash drives commonly used COB technology to mount components such as controllers and memory on a substrate because it permits miniaturization of the flash drive. With COB, components such as memory dies are wired and bonded to a substrate (*e.g.,* a PCB), without first being encapsulated by electronic packaging. Ex. 1005, ¶ 73.

V. THE '243 PATENT

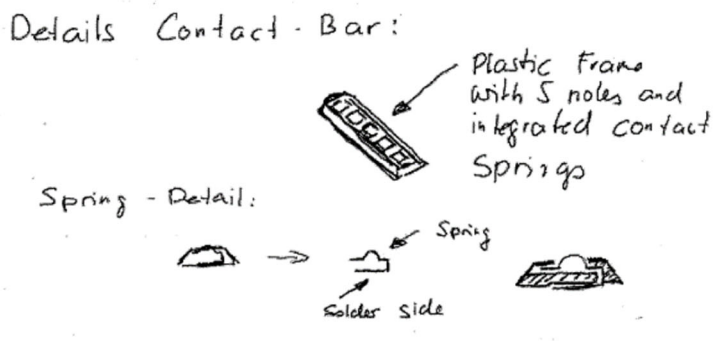
The '243 is directed to connectors for "external storage device[s]" such as "USB sticks" having multiple interfaces, allowing them to be connected to more

than one type of receptacle—e.g., USB 2.0 and USB 3.0 receptacles. *See, e.g.,* Ex. 1001, 1:22-23, 1:65-2:2; 2:30-32; 4:21-23.[3]

The ’243 focuses on the connector’s mechanical interface, adopting the same two-tier contact arrangement as the USB 3.0 Standard-A Plug Specification comprising five resilient contacts (which the ’243 calls “springs”), and four non-resilient contacts (which the ’243 calls “connection fingers”). *See* Ex. 1008 at 5-10. Like the USB 3.0 Specification, the ’243’s “springs” are integrated into an insulative housing, the “contact bar cover **32**.” *See* Ex. 1001, 6:8-10, 8:13-18. Ex. 1005, ¶¶ 74-77.

The ’243 claims require that the storage device have a contact bar comprising a cover and springs, and connection fingers “embedded to be exposed upon the cover of the contact bar.” *See* Appendix A, claims 1, 12, 18 (elements [e] and [f]). Provisional application 61/438,139, incorporated by reference into the ’243 (*id.*, 1:6-12), depicts a “Contact bar” as a “Plastic Frame with 5 holes and integrated contact springs:”

[3] Appendix A hereto lists the ’243 claims. Elements of independent claims 1, 12, and 18 are labeled with letters for ease of reference.



Ex. 1002 at 12; Ex. 1005, ¶¶ 77-78.

The storage devices include a substrate having a "connection surface" and a "component surface" opposite the connection surface. Appendix A, claims 1[b], 12[b], 18[b]. The substrate may be a PCB "used to mechanically support and electrically connect the other components of the device **10**." Ex. 1001, 4:32-35. The contact bar is mounted on the substrate's "connection surface" and the springs have a portion that is a greater distance from the substrate's surface than the distance of the connection fingers from the substrate surface. Appendix A, claims 1, 12, 18 (elements [e] and [f]); Ex. 1005, ¶ 78.

Figure 35, annotated below, provides the sole written description support for the claimed connectors[4]:

[4] The coloring on figures reproduced in this petition was added by Petitioners.

External Storage Device (10)

Contact bar cover (32)

Connection fingers (20)

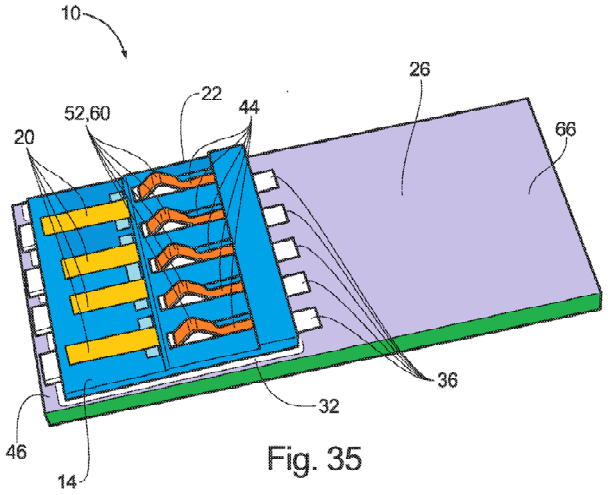


Fig. 35

Springs (52)

Connection surface (26)

See Ex. 1005, ¶ 79.

At least one "memory die stack" is mounted on the substrate. Appendix A, 1[c], 12[c], 18[c]. The "stack" may have only one memory die. Ex. 1001, 3:19-32, 3:39-45, FIGs. 16-19, 22-23 (depicting stacks "having a single die"), 8:36-38

("memory die stack **18** may include **1**, 2, 4, or any suitable number of dies") (emphasis added). A controller configured to access the memory is mounted on the substrate. Appendix A, claims 1[d], 12[d], 18[d]. *See* Ex. 1005, ¶¶ 71-72, 81-82.

The '243 does not claim any new memory or controller designs, leaving it to POSITA to select suitable ones. Ex. 1005, ¶ 83. The '243 dependent claims 4-8 and 13-17 recite well-known limitations regarding (1) memory die stack placement (on the substrate's connection surface, component surface, or both), and (2) the number of dies per stack. Appendix A; Ex. 1005, ¶¶ 84-85.

While the '243 Background mentions the desirability of incorporating USB 3.0 SuperSpeed connections into "existing USB 2.0 COB sticks" (Ex. 1001, 1:65-2:2), the '243 claims are not limited to COB sticks or (except for claim 18) supporting USB 3.0 SuperSpeed. *See* Ex. 1005, ¶ 75.

VI. THE '243 PATENT PROSECUTION HISTORY

The '243 issued April 22, 2014 from U.S. Patent Application No. 13/362,431 ("'431 Application"), filed January 31, 2012. The '243 claims priority to U.S. Provisional Application Nos. 61/438,139 ("'139 Provisional") filed January 31, 2011 (Ex. 1002) and 61/442,379 ("'379 Provisional") filed February 14, 2011 (Ex. 1003) (collectively, "Provisionals"). Ex. 1001, 1:6-10.

The Examiner found the as-filed claims were subject to a restriction/election requirement, and identified two claim groups and twenty species that he categorized by referencing the application's figures. Ex. 1004 at 110-13.

Applicant provisionally elected to pursue "Group II" claims requiring a "contact bar," conditionally elected the Figure 35 species, and identified pending claims that Applicant contended were generic to the species identified by the Examiner. *Id.* at 98-100 (asserting *inter alia* that the independent claims were generic to species having different memory die stacks placements and different numbers of dies per stack).

On July 11, 2013, the Examiner rejected the claims. *Id.* at 79-84. He made no prior art rejections, but rejected as indefinite: (1) claims using the term "mounted on or embedded" finding it unclear "if the recited limitation is required (and) or is optional (or)"; and (2) claims reciting USB standards. *Id.* at 82-83.

The Examiner stated the claims would be allowable if rewritten to overcome the indefiniteness rejections and objections the Examiner had made, reasoning that the prior art of record did not disclose the claimed connectors. *Id.* at 83.

Applicant amended the independent claims to (1) replace "mounted on or embedded within" with "embedded to be exposed upon" and (2) remove references to USB standards. *Id.* at 61-62. Applicant amended pending claim 30 to make it

independent, and claim the USB 2.0 and 3.0 standards "in effect as of January 31, 2011." *Id.* at 62.

On November 22, 2013, the Examiner issued a Notice of Allowance ("11-22-13 NOA"). *Id.* at 32-43. In his reasons for allowance, the Examiner focused on the independent claims' connector arrangements asserting the prior art of record did not disclose them. *Id*. at 40-42.

Over two months later, Applicant submitted a Supplemental Information Disclosure Statement ("SIDS") listing *inter alia* U.S. Patent No. 8,480,435 ("Hsiao") (Ex. 1009). *Id*. at 25-31. On February 24, 2014, Applicant paid the issue fee and requested that the Examiner consider the SIDS and issue a Supplemental Notice of Allowability ("NOA"). *Id.* at 15-24. On March 10, 2014, the Examiner issued a supplemental NOA simply stating that he had considered the references and "[c]laims 12 and 14-30 were still found allowable." *Id.* at 10-13. The '243 issued shortly thereafter.

VII. THE BOARD SHOULD NOT DECLINE REVIEW UNDER SECTIONS 325(D) OR 314

A. The Board Should Not Decline Review Under § 325(d) Because the Office Materially Erred in Its Evaluation of Hsiao and the Petition Relies Heavily on Uncited Art

Hsiao (Ex. 1009) and Hsiao and Sun (Ex. 1014) combined clearly prove that the '243 claims are unpatentable. Hsiao and Sun, however, are prior art under 35

U.S.C. § 102(e); Patent Owner can potentially antedate them. Accordingly, Petitioner provides additional grounds of unpatentability based on Chen (Ex. 1010), a § 102(b) reference, combined with other § 102(b) references which cannot be antedated.

Applicant's eleventh-hour citation of Hsiao – months after the Examiner issued the 11-22-13 NOA – should not dissuade the Board from instituting IPR. The Office materially erred by "overlooking specific teachings" of Hsiao that "impact patentability of the challenged claims"—*i.e.,* Hsiao, Figures 9-10 and accompanying disclosure in Hsiao's specification. *Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GMBH*, IPR2019-01469, Paper 6 at 7-9, n.9 (PTAB Feb. 13, 2020) (Precedential) (establishing § 325(d) analysis "framework"); *see also Mylan Pharm., Inc. v. Merck Sharp & Dohme Corp.*, IPR2020-00040, Paper 21 at 17-20 (PTAB May 12, 2020 (refusing to decline to institute IPR under § 325(d) where Examiner "simply overlooked" relevant teachings of cited prior art); *Medacta USA, Inc., v. RSB Spine, LLC*, IPR2020-00264, Paper 24 at 18 (PTAB May 22, 2020) (same).

The Board considers "*Becton* factors" (c), (e) and (f) in assessing whether Petitioners have shown "material error":

> "(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection"

"(e) whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art"

"(f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments."

Advanced Bionics, IPR2019-01469, Paper 6 at 9-10, n. 10 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG,* IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017)).

Application of these factors leads to the inexorable conclusion that the Examiner overlooked Hsiao's relevant teachings resulting in material error.

The Examiner provided no evaluation of Hsiao (or any art of record), made no rejections based on Hsiao, and, indeed, made no prior art rejections whatsoever. Applicant disclosed Hsiao to the Office in a SIDS months after prosecution on the merits was completed and the Examiner had issued the 11-22-13 NOA. The Examiner's Supplemental NOA provides no explanation for the allowance of the '243 claims over Hsiao. *See* Section VI above.

As Sections IX.C and X.A show, the Examiner's conclusion was erroneous. Figures 9 and 10 of Hsiao and associated text teach a USB COB flash memory device having both USB 2.0 and USB 3.0 interfaces and a connector that is identical to that claimed in the '243. Hsiao discloses every connector feature the Examiner stated in the 11-22-13 NOA was missing from the prior art of record.

(Hsiao was not of record when the 11-22-13 NOA was issued.) *See* Ex. 1004 at 40-41; Sections IX.C, X.A.1 (explaining how Hsiao teaches these features); Ex. 1005, ¶¶ 94-96.

A comparison of Applicant's elected species (Ex. 1001, Figure 35) and Hsiao (Ex. 1009), Figure 10 underscores this:

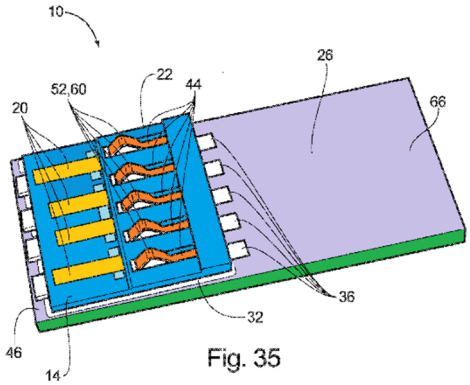


Fig. 35

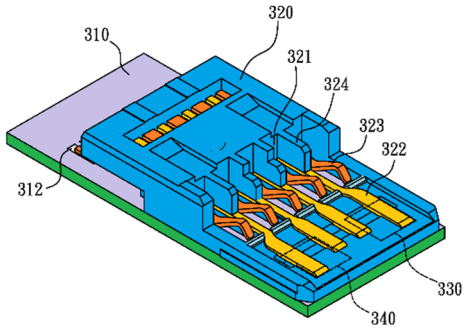


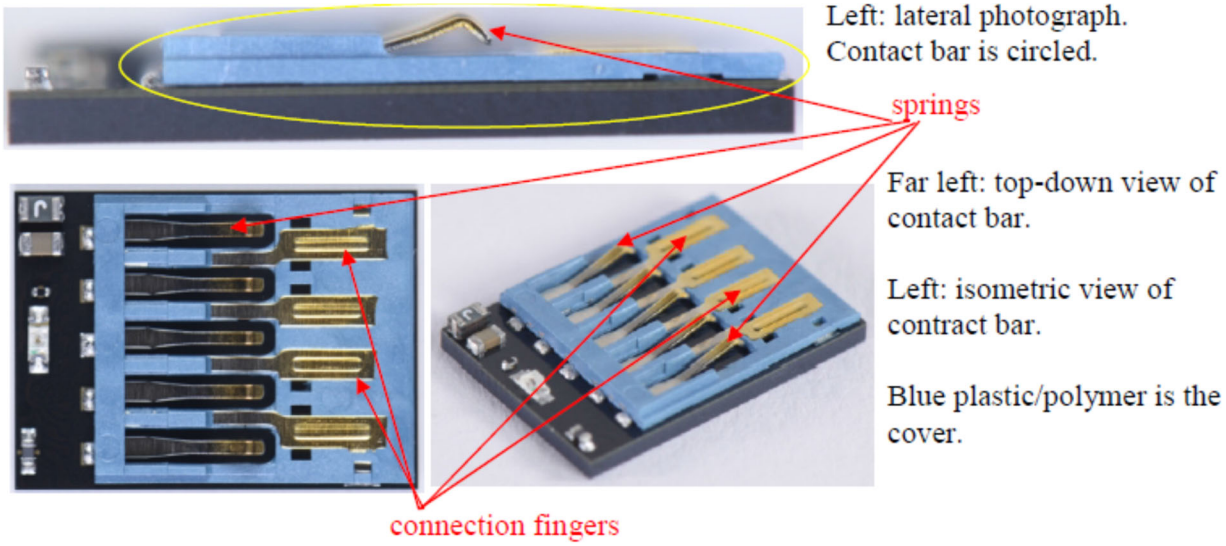
FIG. 10

Hsiao also discloses the "coupling points" (claim 12) and device configured to support USB 2.0 and 3.0 standards (claim 18) the Examiner stated in the 11-22-13 NOA was missing from the prior art. Ex. 1004 at 41-42; Sections X.A.7.b, X.A.9.b.

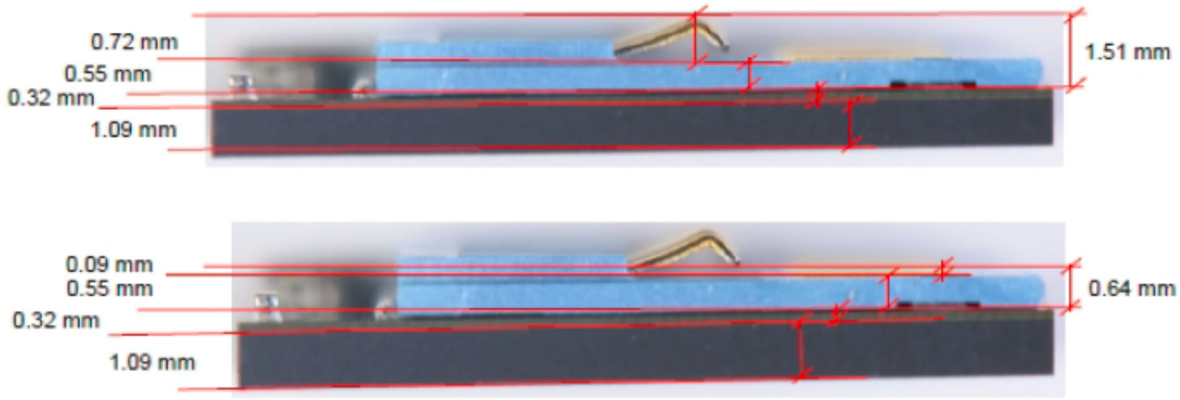
The Petition contains additional evidence not considered by the Examiner—*i.e.,* the expert declaration of Dr. Baker (Ex. 1005), who explains in detail how Hsiao, alone or in combination with Sun (Ex. 1014), invalidates the '243 claims.

Petitioner also provides Patent Owner's infringement contentions filed in the Litigation showing how Patent Owner applies the claims to accused devices. Ex.

1016. These contentions (excerpts reproduced below) underscore Hsiao's relevance because Hsiao's USB flash drive and connector design (shown in Figs. 9-10) mimic that which Patent Owner now alleges is infringing.



The springs and connection fingers are identified above.
This row of the chart shows the rleative distances recited in the claims.
A portion of each spring is located approximately 1.51 mm from the connection surface.
The connection fingers are located approximately 0.64 mm from the connection surface.



Ex. 1016 at 7-8.

In strikingly similar circumstances the Board refused to decline to institute IPR based on art cited during prosecution, finding that the Examiner materially erred in evaluating the art. *See Mylan,* IPR2020-00040, Paper 21 at 17-20. In *Mylan*, the Examiner made no prior art rejections, did not discuss the reference at-issue, and gave no reasons for allowance, leaving the Board "to guess" why the Examiner found the claims patentable. *Id.* at 18. Finding that the reference's disclosure was not subject to reasonable dispute, the Board concluded the "likeliest explanation" was that the Examiner "simply overlooked" the reference's relevant teachings. *Id.*

So too, here. Petitioners and Dr. Baker have shown how Hsiao teaches the alleged inventions. Although Hsiao discloses every feature the Examiner previously found the prior art was missing, the Examiner made no rejection based on Hsiao (when Applicant belatedly cited it), and gave no reasons for allowing the '243 claims over Hsiao. The most likely explanation is that the Examiner overlooked the teachings of Hsiao in figures 9 and 10 and associated text—a material error.

The Office's clear error merits review by the Board.

Moreover, none of the other prior art applied to the claims – including Chen (Ex. 1010), Sun (Ex. 1014), Cheng (Ex. 1012), Hiller (Ex. 1013) and Wan (Ex. 1011) – was before the Examiner during prosecution. Nor was substantially

similar art. Hsiao appears to be the closest art of record, but Chen combined with either Cheng and Wan or Sun differs substantially from Hsiao. For example, although Hsiao teaches connection fingers "embedded to be exposed" upon the contact bar cover, Chen is even more explicit, disclosing that "[a] plurality of plug contact receiving passageways **123** are recessed in the supporting surface **121** of the plug tongue portion **12**" of housing **10** (Ex. 1010, 6:28-30), and the connection fingers (contact **131-134**) are "inserted into" these passageways. *Id.*, 6:58-62. Sections X.D, X.F and X.G show that Chen combined with Cheng or Sun or Cheng and Wan clearly disclose each element of the independent claims.

B. The Board Should Not Decline Review Under Section 314(A)

Consideration of the *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (Precedential) factors favor institution here.

1. Factor 1: The Potential For A Stay in District Court Is Neutral

Petitioner WDT intends to move for a stay of the Litigation if the Board institutes IPR. This factor is neutral because the district court's decision on WDT's motion will come after institution, and is "based on a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Continental Intermodal Group—Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB Jun. 16, 2020) (Informative).

2. Factor 2: Lack Of Trial Date Favors Institution

No trial date has been set in the Litigation, WDT has not yet answered, and a case management conference has not been held. Even if the trial date is set before the Board issues its institution decision, trial dates in the Western District of Texas where the Litigation is pending are uncertain due to the COVID-19 pandemic. *See* Ex. 1020.

In contrast, the Board can adhere to the one-year statutory deadline prescribed by 35 U.S.C. § 316(a)(11), having converted to remote oral hearings early in the pandemic. *See Sand Revolution*, IPR2019-01393, Paper 24 at 9; Ex. 1021.

3. Factor 3: District Court's Minimal Investment In The Merits Of The Litigation Favors Institution

Petitioners filed this petition less than two months after Patent Owner filed the Litigation Complaint, and before Petitioner WDT filed its responsive pleading. The district court has invested no time in the merits of the Litigation. *See* Section II.B; *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper No. 10 at 11 (PTAB Jun. 15, 2020) (finding diligence in filing petition where petition was filed four months before the § 315(b) statutory bar date).

4. Factor 4: The Minimal Overlap Between Issues In This Proceeding And The Litigation Favors Institution

Petitioner WDT has not served invalidity contentions in the Litigation. However, the invalidity positions in the Litigation will be vastly different from the grounds submitted in this petition. The USB 3.0 Specification (Ex. 1008) issued several years before the priority date, and many companies had products on the market before the '243 priority date. Consequently, Petitioner WDT has identified and expects to rely upon a significant amount of system art in the Litigation. Further, Petitioners will stipulate that they will not pursue invalidity on the same grounds in the Litigation if the Board institutes trial in this proceeding. *See Fintiv*, IPR2020-00019, Paper No. 11 at 12-13 (use of different prior art in IPR petition than in district court favors institution).

Lastly, the Petition challenges claims 1-18, but Patent Owner's Litigation Complaint only alleges infringement of claims 1-4, 9-13, and 18. Ex. 1022. Accordingly, the Board will resolve claims which the district court will not address, while the opposite is not true. *See Seven Networks*, IPR2020-00156, Paper 10 at 17 (fact that Board will resolve claims that district court will not address weighs in favor of institution).

5. Factor 5 Is Neutral

Only Patent Owner and Petitioner WDT are parties both in this proceeding and the Litigation; Petitioners WDC and SanDisk are not. However, given the corporate relationship between Petitioners, this factor is neutral.

6. Factor 6: Additional Factors Favor Institution.

Petitioners' Grounds are strong (*see* Section X), further favoring institution. *Fintiv*, IPR2020-00019, Paper 11 at 14–15 (Where merits "seem particularly strong on the preliminary record, this fact has favored institution.").

VIII. CLAIM CONSTRUCTION AND LEVEL OF ORDINARY SKILL

A. Claim Construction

Petitioners submit that all terms should be given their plain meaning as understood by POSITA in view of the intrinsic evidence, but reserve the right to respond to any constructions that may be offered by Patent Owner or adopted by the Board. Petitioners are not waiving any arguments concerning indefiniteness or claim scope that may be raised in the Litigation.

Petitioners offer the following constructions of selected terms:

1. "Mounted on" Means "Securely Attached, Affixed or Fastened To"

The term "mounted on," used in all the claims, refers to a physical object that is "mounted on" another physical object. "Mounted on" has no specialized

meaning in the art and the '243 ascribes no specialized meaning to it. Ex. 1005, ¶¶ 103-104.

The Federal Circuit has held that the "ordinary meaning" of "mounted on" is "securely attached, affixed, or fastened to." *Asyst Techs. v. Emtrak, Inc.*, 402 F.3d 1188, 1193 (Fed. Cir. 2005); *see also Felix v. Am. Honda Motor Co*., 562 F.3d 1167, 1177-78 (Fed. Cir. 2009) ("mounted on" is "securely affixed or fastened to"). Here, "mounted on" should be afforded its ordinary meaning of "securely attached, affixed or fastened to."

"Mounted on" as used in the claim phrase "a contact bar mounted on the connection surface of the substrate" does not require that the contact bar be mounted *entirely* on the substrate's connection surface. *See Netlist, Inc. v. Diablo Techs., Inc.*, 701 F. App'x 1001, 1004 (Fed. Cir. 2017) ("Nothing in the claim language or specification requires the 'entire circuit' to be mounted on the memory module.") *See* Ex. 1005, ¶¶ 105-107.

2. "Embedded to Be Exposed Upon the Cover of the Contact Bar"

Section VI explains that during prosecution, in response to the Examiner's indefiniteness rejection, Applicant amended "mounted on or embedded within" to read "embedded to be exposed upon" as shown below:

a plurality of connection fingers ~~mounted on or embedded within~~ embedded to be exposed upon the cover of the contact bar,

Id. at 56.

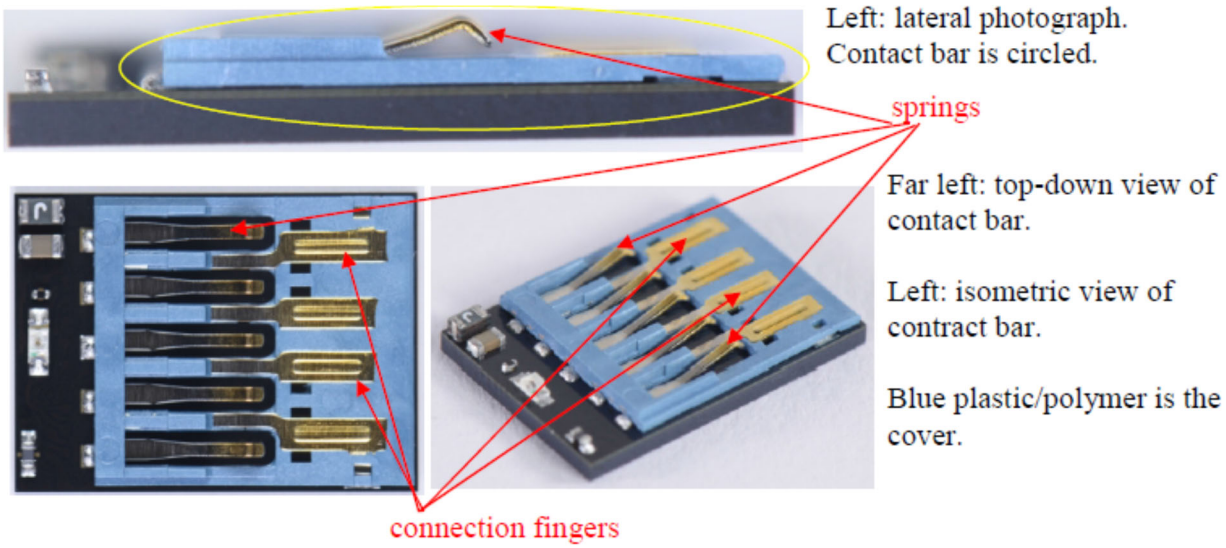
Thus, the claimed "external storage device" comprises embedded connection fingers that are exposed upon the contact bar cover. "Embedded" has no specialized meaning in the art or in the '243. Ex. 1005, ¶¶ 110-111. The term should be afforded its ordinary dictionary definition of "set firmly into a mass or material." *See* https://www.merriam-webster.com/dictionary/embedded; *see also* https://ahdictionary.com/word/search.html?q=embedded ("embed" means "to fix firmly in a surrounding mass: *embed a post in concrete*." *See* Ex. 1005, ¶ 111.

3. Memory Die Stack

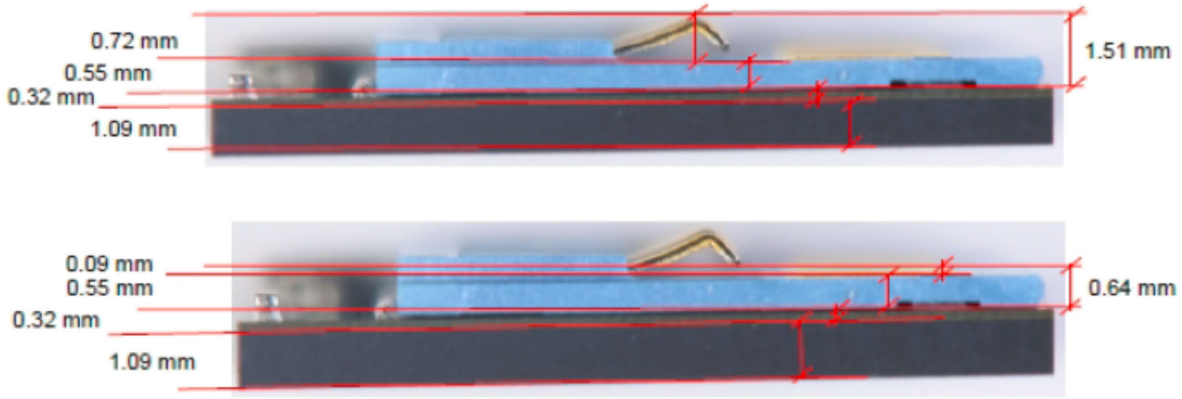
The '243 claims all require a "memory die stack," mounted on the claimed substrate. As Section IV explains, the "stack" may have only one memory die. Ex. 1005, ¶¶ 71-72, 81, 112.

4. Patent Owner's Construction of "Springs" "Connection Fingers", "Contact Bar Cover" and First and Second Distances

Patent Owner's Litigation Complaint (excerpt below) shows Patent Owner's construction of springs, connection fingers, contact bar cover and first and second distances.



The springs and connection fingers are identified above.
This row of the chart shows the rleative distances recited in the claims.
A portion of each spring is located approximately 1.51 mm from the connection surface.
The connection fingers are located approximately 0.64 mm from the connection surface.



Id. at 7-8. *See* Ex. 1005, ¶¶ 113-114.

B. Persons of Ordinary Skill in the Art

The ’243 is directed to a simple mechanical modification of external storage device connectors. For purposes of this IPR, POSITA would have had (1) a

Bachelor's degree in EE, CompE or ME, and (2) at least one year of experience with USB and other computer interface protocols. Ex. 1005, ¶¶ 43-48.

IX. PRIOR ART OVERVIEW

A. Effective Filing Date

Although the '243 claims priority to the Provisionals, claims 1-18 are not entitled to the filing date of either Provisional because neither provides written description support under 35 U.S.C. § 112 for at least the limitation "a plurality of connection fingers embedded to be exposed upon the cover of the contact bar," a requirement of every claim. *See* Appendix A, claims 1[f], 12[f] and 18[f]; Ex. 1005, ¶¶ 97-100.

The '139 and '379 Provisionals describe USB sticks with contact bars added to provide a USB 3.0 interface, but only show the connection fingers (USB 2.0 contacts) formed on the substrate's (*e.g.,* PCB) surface. Ex. 1002 at 7-13; Ex. 1003 at 4-12. The '139 Provisional explicitly states "USB 2 contacts on Board." Ex. 1002 at 12. The Provisionals nowhere describe connection fingers "embedded to be exposed" upon the contact bar cover. Accordingly, the effective filing date for the '243 claims can be no earlier than the '431 Application's filing date—January 31, 2012. *See* Ex. 1005, ¶¶ 98-101.

This is not an issue for this Petition, however, because Petitioners' cited prior art is also prior art to the Provisionals, whose earliest filing date is January 31, 2011.

B. Prior Art Bases

The following are prior art under at least 35 U.S.C. § 102(b) because each was published over one year before January 31, 2011:

- USB 2.0 Specification, published April 27, 2000 (Ex. 1007). *See* Ex. 1019, ¶¶ 1-7;
- USB 3.0 Specification, published November 12, 2008 (Ex. 1008). *See* Ex. 1019, ¶¶ 1-4, 8-10;
- U.S. Patent 7,625,243 ("Chen"), published December 1, 2009 (Ex. 1010);
- U.S. Patent Application Publication 2009/0098773 ("Cheng"), published April 16, 2009 (Ex. 1012);
- U.S. Patent Application Publication 2008/0150111 ("Hiller"), published June 26, 2008 (Ex. 1013);
- U.S. Patent 7,563,140 ("Wan"), published July 21, 2009 (Ex. 1011);

U.S. Patent 8,480,435 ("Hsiao"), filed November 23, 2010 (Ex. 1009) is prior art under 35 U.S.C. § 102(e).

Sun (Ex. 1014) is a World Intellectual Property Organization publication of a Patent Cooperation Treaty application ("PCT") under 35 U.S.C. § 351(a). The PCT was filed July 30, 2010 in English, designated the U.S., and was published in English as WO 2011/160321. Ex. 1014, face page. Accordingly, Sun is prior art under 35 U.S.C. § 102(e) as of its PCT filing date, July 30, 2010. *See also* MPEP § 2136.

Prior art references cited herein or in Dr. Baker's Declaration (Ex. 1005) but not applied to the claims are supplied to provide information regarding the state of the art as of January 31, 2011.

C. Hsiao (Ex. 1009)

Hsiao, entitled "USB Connector," teaches COB flash memory devices having both USB 2.0 and 3.0 interfaces. Ex. 1009, 1:36-39, 6:51-55, 7:30-38. Hsiao discloses the same two-tier contact arrangement that was later claimed in the '243. In Figures 9 and 10 (reproduced below), Hsiao discloses an external storage device wherein: (1) a contact bar having a cover (connector main body **320**) and springs (terminals **323** for the USB 3.0 interface) is mounted on COB substrate **310**'s connection surface; and (2) connection fingers (terminals **322** for the USB 2.0 interface) are embedded to be exposed upon the contact bar cover. Ex. 1009, 6:38-55, 7:4-29, 7:39-51, Figs. 9-10; Ex. 1005, ¶¶ 115-118.

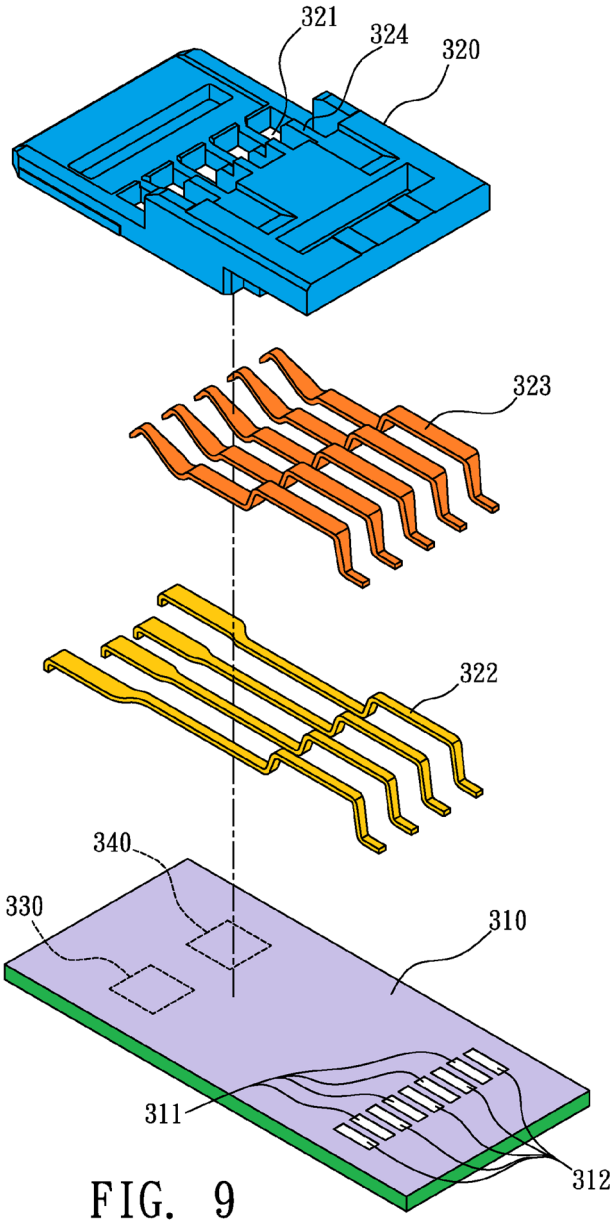


FIG. 9

Contact bar cover (connector main body 320)

Springs (terminals 323)

Connection fingers (terminals 322)

Substrate 310 connection surface

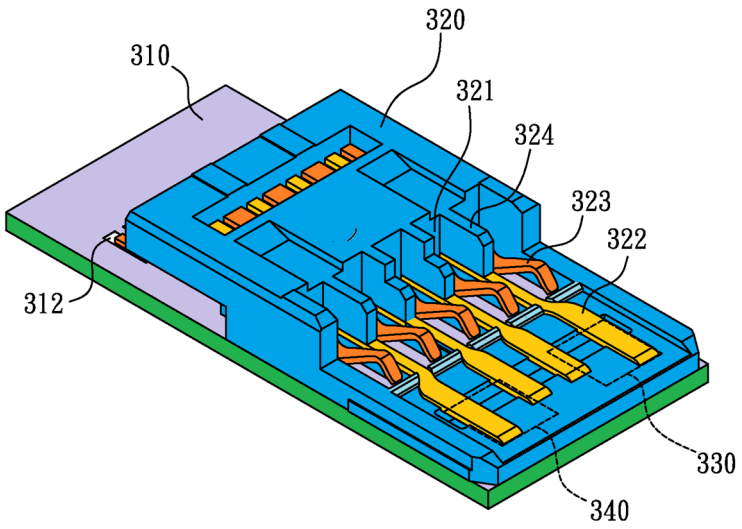


FIG. 10

Substrate **310**'s "connection surface" includes contact pads **311** (for USB 2.0 connections) and **312** (for USB 3.0 connections). Ex. 1009, Fig. 9, 6:47-50, 6:59-7:3 (contact pads **311** can transmit "signals of USB2.0 specification" and contact pads **312** can transmit "signals of USB3.0 specification"); Ex. 1005, ¶ 118.

Terminals **322** and **323** are "integrally formed" with connector main body **320**, which "is made of insulation material" such as "plastic." Ex. 1009, 7:4-5, 7:39-42. USB 2.0 terminals **322** are "installed below the plural slot columns **324"** of connector main body **320** and "forwardly extended" as shown in Fig. 10 so that they are exposed upon connector main body **320**. *Id.*, 7:10-13. USB 3.0 terminals **323** are installed in slot openings **321** with one end that is "upwardly bended then downwardly bended after being exposed outside the opening slots **321**." *Id.*, 7:18-29. Thus, the springs include a portion that is a greater height above the substrate

surface than the connection fingers. The terminals' tails ends are welded to contact pads **311** and **312**. *Id.*, 7:42-47. *See* Ex. 1005, ¶¶ 119-120.

"USB controller **330** and the flash memory **340** are installed on the substrate **310** through a means of [COB] package," which Hsiao describes as "conventional art." *Id.*, 7:30-36. In Figures 9 and 10, Hsiao depicts the memory and controller with dotted lines, indicating that they are mounted on the opposite substrate surface from the connector. Hsiao teaches the disclosed USB connector "has a smaller volume and lower production cost compared to conventional USB connectors." Ex. 1009, 7:52-54. *See* Ex. 1005, ¶ 121.

D. Chen (Ex. 1010)

Chen, entitled "Extension to Version 2.0 Universal Serial Bus Connector With Improved Contact Arrangement," discloses a connector plug having a USB 2.0 interface and a "non-USB 2.0" interface. Ex. 1010, Abstract. The plug has the same two-tier contact arrangement as later claimed in the '243 installed in insulative housing **10**. Ex. 1005, ¶¶ 123-124.

"[P]lug contacts **13** include four plug conductive contacts" (**131-134)** "and a plurality of additional plug contacts **137**" "located behind the conductive contacts." Ex. 1010, 6:31-34, 6:46-49. "[P]lug contacts **13** are all formed of a metal sheet and separated from each other." *Id.*, 8:26-27. The housing **10** includes passageways **123** for receiving the contacts (*id.*, 6:28-41) to make a contact bar.

Contacts **131-134** carry USB 2.0 signals. *Id.*, 7:59-64. "[E]ach comprises a plug contact portion **16**" (*id.*, 6:50-52), that "is flat and nonelastic." *Id.*, 6:57-58. When contacts **131-134** "are inserted into corresponding passageways **123**," this flat, non-elastic contact portion **16**, "is substantially coplanar with the supporting surface **121** as shown in FIGS. **3-4**." *Id.*, 6:58-62, Figs. 3-4.

"[P]lug contacts **137** include two pairs of differential plug contacts **138**" "for transferring/receiving high-speed signals" and "grounding plug contact **139**." *Id.*, 7:15-21, Fig. 2. These contacts are springs—each has "an elastic contact portion" designated **1381** and **1391**, respectively. *Id.*, 7:21-30. "[E]ach contact portion **1381**, **1391** is cantileveredly received in the passageways **123** and protruding upwardly beyond the supporting surface **121** so that the contact portion **1381**, **1391** is elastic and deformable when engaging with corresponding contacts of the extension to USB receptacle **200**." *Id.*, 7:43-48, Figs. 2-3.

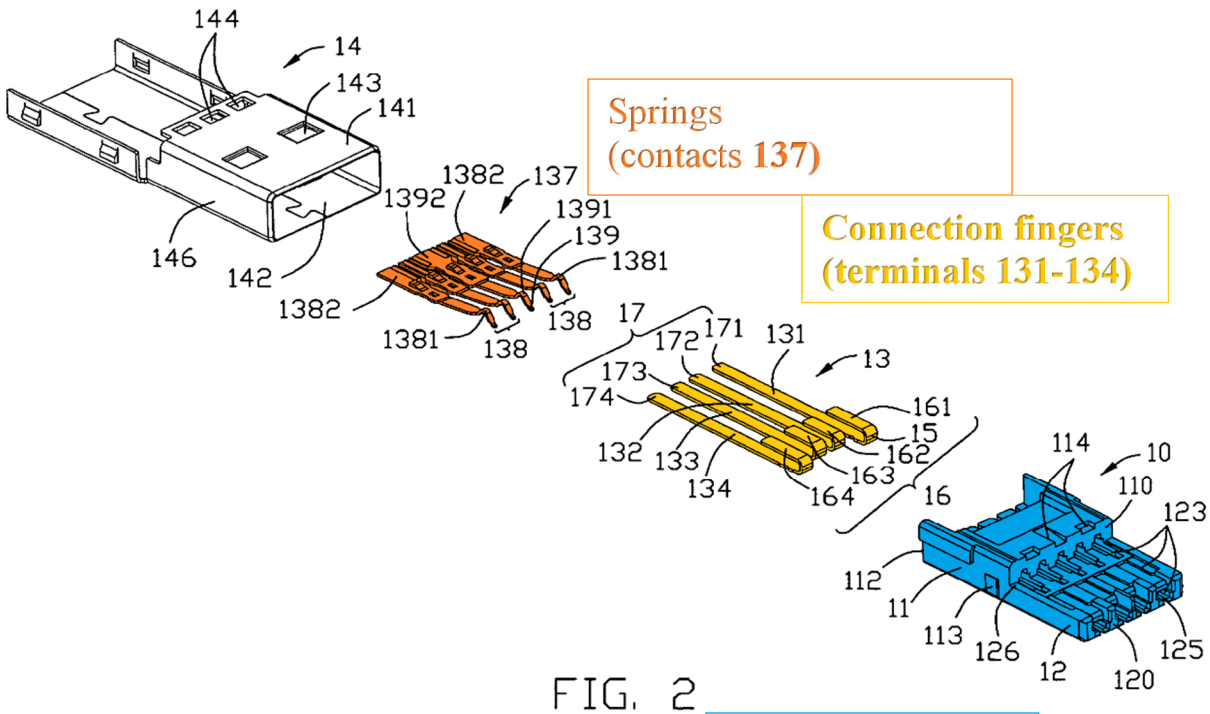

144
14
143
141
146
142
1382
137
1392
1391
139
1381
1382
1381
138
138
17
172
171
131
13
173
174
161
15
132
133
162
134
163
164
16
114
10
110
123
112
11
113
126
125
12
120
Springs
(contacts 137)
Connection fingers
(terminals 131-134)
Contact bar cover
(housing 10)

FIG. 2

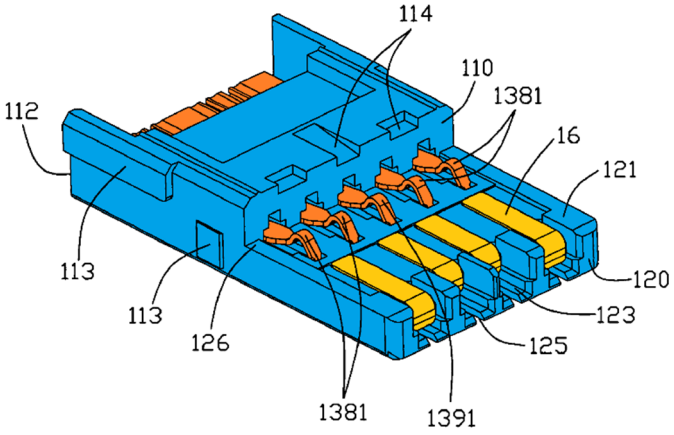

114
110
1381
112
16
121
113
120
113
123
126
125
1381
1391

FIG. 3

See Ex. 1005, ¶¶ 125-134.

Housing **10** has insulative base and tongue portions **11, 12** that are "integrally injecting [sic: injected] molded" as one piece. Ex. 1010, 5:49-52, 6:12-14. The plug tongue portion **12** has substantially the same dimensions as a standard USB 2.0 plug, and the springs have portions **1381/1391** that are a greater height above the substrate surface than the fingers. *Id.*, 7:43-48, 7:53-57, Fig. 4 (annotated) (black and red arrows show spring and fingers height, respectively):

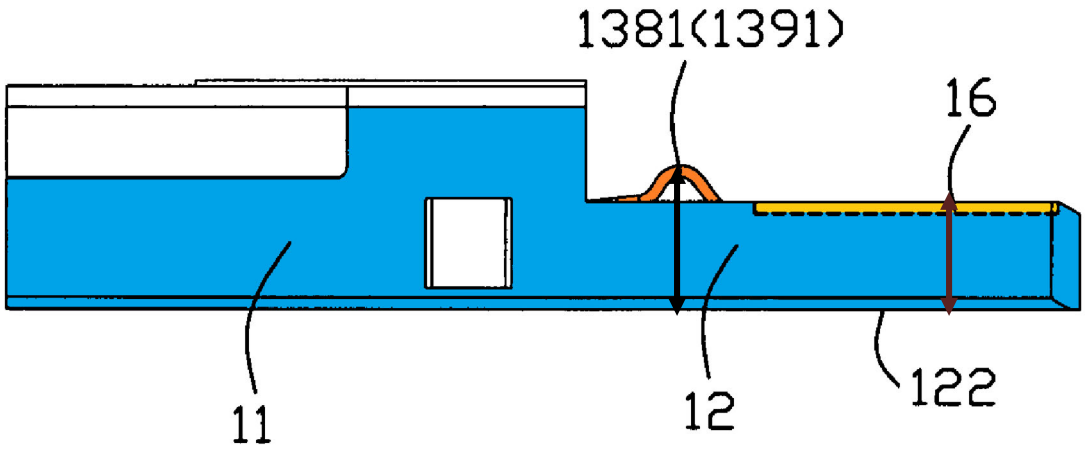


FIG. 4

Chen discloses an embodiment in which "the extension to USB is a memory device," that includes a PCB with a memory unit. Ex. 1010, 11:43-65, Fig 13. The USB plug has the configuration described above and the terminals' "tail portions" are "physically and electrically connected" to the PCB. *Id; see also id.* 11:66-12:22, claim 3. *See* Ex. 1005, ¶¶ 126-127, 134-136, 241.

E. Cheng (Ex. 1012)

Cheng, entitled "Space Minimized Flash Drive," discloses USB flash drives with memory mounted on both surfaces of the flash drive's PCB. *See* Ex. 1012, [**0029-30**], [**0035-36**], Figs. 2, 6.

Cheng teaches that mounting flash memory on both PCB surfaces permits miniaturization of a flash memory device by reducing its length while providing greater memory capacity. Ex. 1012, [**0030**]; Ex. 1005, ¶¶ 142-145.

F. Hiller (Ex. 1013)

Hiller, entitled "Memory Device," discloses that a "conventional approach" to memory die stacking includes stacking "same-sized dies with overhanging designs." Ex. 1013, [**0003**]. Hiller discloses "a memory device comprising at least one memory stack of stacked memory dies which are staggered with respect to each other." *Id.*, [**0004**]; Figs. 8-9, 18:

FIG 8

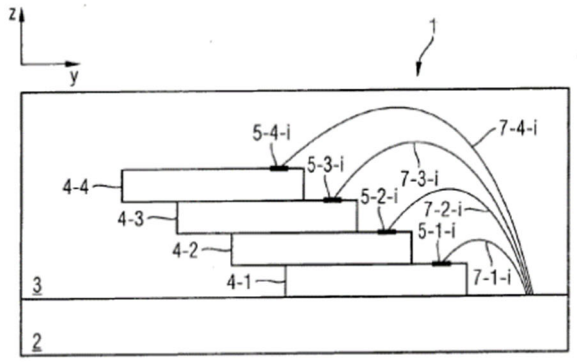


FIG 9

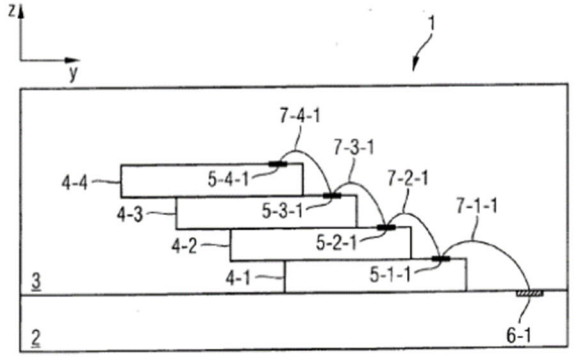
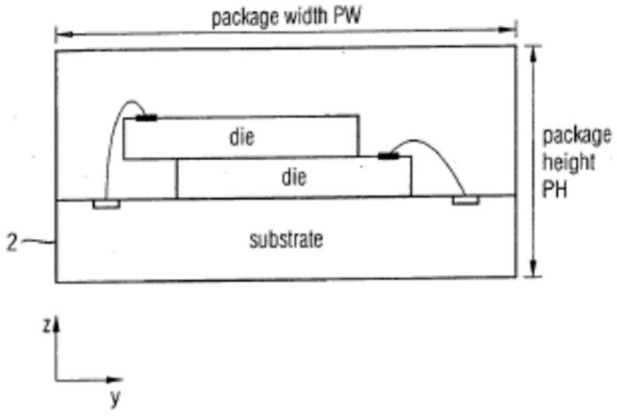


FIG 18



See Ex. 1005, ¶¶ 146-148.

G. Sun (Ex. 1014)

Sun, entitled "Data Storage Device," discloses USB "data storage device[s]" in which flash memory assemblies comprise "4 stacked flash memory dies." Ex. 1014, Abstract. Sun discloses that these memory assemblies can be mounted on either surface of the storage device's substrate or on both surfaces. *Id.* at 12-14, Figs. 10-11. Sun teaches that an advantage of multichannel stacked flash memory is "provid[ing] high data storage capability at high data transfer rates while maintaining a compact construction due to the high-rise stacked architecture." *Id.* at 2. *See* Ex. 1005, ¶¶ 149-151.

X. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Hsiao Anticipates Claims 1-4, 9-13 and 18

As shown below, Hsiao discloses every element of claims 1-4, 9-13 and 18, and thus anticipates these claims. *Id.*, ¶ 153.

1. Claim 1

a) An external storage device comprising:

Hsiao discloses an external storage device—*i.e.,* a USB COB flash memory device. Ex. 1009, 7:30-36 ("[S]ubstrate **310** of the USB connector" is "installed with a USB controller **330** and at least one flash memory **340** respectively coupled to the plural first contact pads **311** and the plural second contact pads **312**; the USB controller **330** and the flash memory **340** are installed on the substrate **310** through

a means of Chip-On-Board package, said means is a conventional art . . .”); Figs. 9-10:

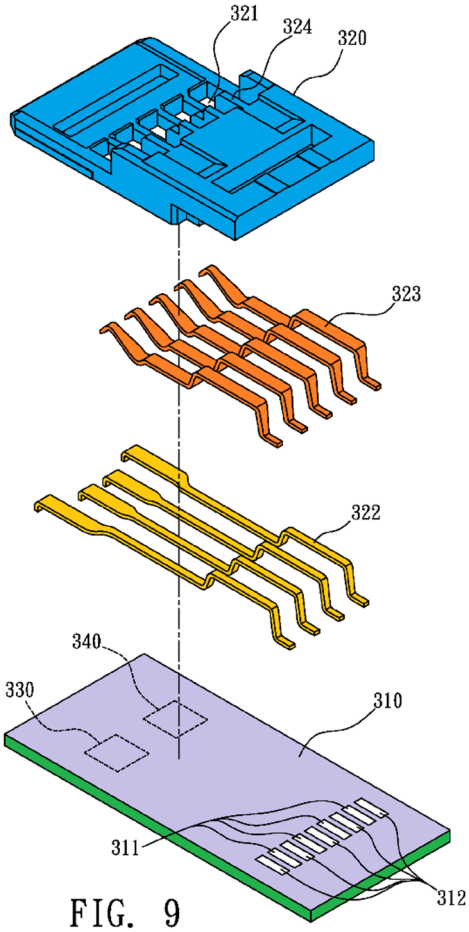


FIG. 9

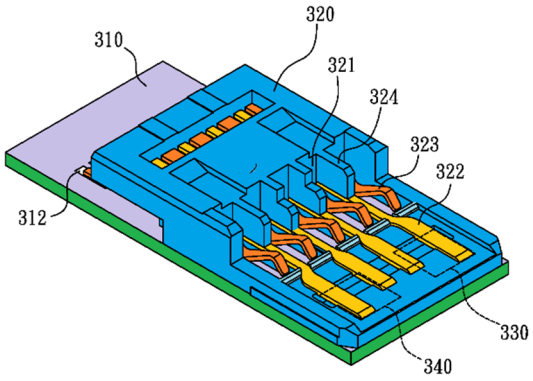


FIG. 10

See Ex. 1005, ¶¶ 154-155.

b) a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

The substrate is “Chip on Board (COB) substrate” **310**. Ex. 1009, 6:51-55. The **“**connection” surface is the surface where contact pads **311** and **312** are installed, and the component” surface is the opposite surface. *Id.*, 6:47-7:3:

> [S]ubstrate **310** is installed with a plurality of first contact pads **311** and a plurality of second contact pads **312** exposed outside the substrate **310** . . ..
>
> [C]ontact pads **311** . . . transmit V_{BUS}, D-, D+ and GND signals of USB2.0 specification. .
>
> [C]ontact pads **312** . . . transmit StdA_SSRX−, StdA_SSRX+, GND_DRAIN, StdA_SSTX− and StdA_SSTX+ signals of USB3.0 specification.

The dotted lines for memory **340** and controller **330** (*see id.*, Figs. 9-10) indicate they are mounted on the opposite substrate surface from the contact pads—the "component" surface. Ex. 1005, ¶¶ 156-158.

c) at least one memory die stack mounted on one of the connection surface and the component surface;

Hsiao teaches at least one memory die stack mounted on the substrate, stating: "***[S]ubstrate 310 of the USB connector of the present invention is further installed with*** a USB controller **330** and ***at least one flash memory 340*** respectively coupled to the plural first contact pads **311** and the plural second contact pads **312** . . .." Ex. 1009, 7:30-33 (emphasis added). POSITA would have known that flash memory **340** necessarily has at least one memory die. Ex. 1005,

¶¶ 159-160. As explained, the memory is mounted on substrate **310**'s "component" surface.

d) a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

The claimed controller is "USB controller **330**." The controller is configured to access the memory. As explained above, both the controller and memory are connected to contact pads **311** and **312.** Moreover, POSITA would have known that the purpose of a USB controller is to provide a USB standard compatible interface between the USB bus and the flash memory. The USB controller manages read and write operations between the flash memory and the USB bus to ensure that communications between the flash memory and USB bus follow the USB standard. Ex. 1005, ¶¶ 161-162.

e) a contact bar mounted on the connection surface of the substrate, the contact bar comprising a cover and a plurality of springs, each of the plurality of springs including a portion that is located at a first distance relative to the connection surface of the substrate;

Hsiao discloses a contact bar comprising a cover (connector main body **320**) and a plurality of springs (terminals **323**). Ex. 1009, 7:39-42. The springs (terminals **323**) are first "integrally formed" with the contact bar cover (connector main body **320**) along with terminals **322**; connector main body **320** is then

mounted on the substrate's connection surface. *Id.*, 7:39-47 ("As shown in FIG. **10**, when being manufactured, firstly the plural first terminals **322** and the plural second terminals **323** are arranged with a staggering means, then is integrally formed with the connector main body **320**; then the connector main body **320** is disposed on the substrate **310**, and the other ends of the plural first terminals **322** and the plural second terminals **323** are respectively welded on the plural first contact pads **311** and the plural second contact pads **312** with a means of surface mount technology (SMT).")

One end of the springs (terminals **323**) is "upwardly bended then downwardly bended after being exposed outside the opening slots **321**." *Id.*, 7:27-29. The first distance is the height of the "upwardly bended" portion of springs (terminals **323**) above substrate **310.**

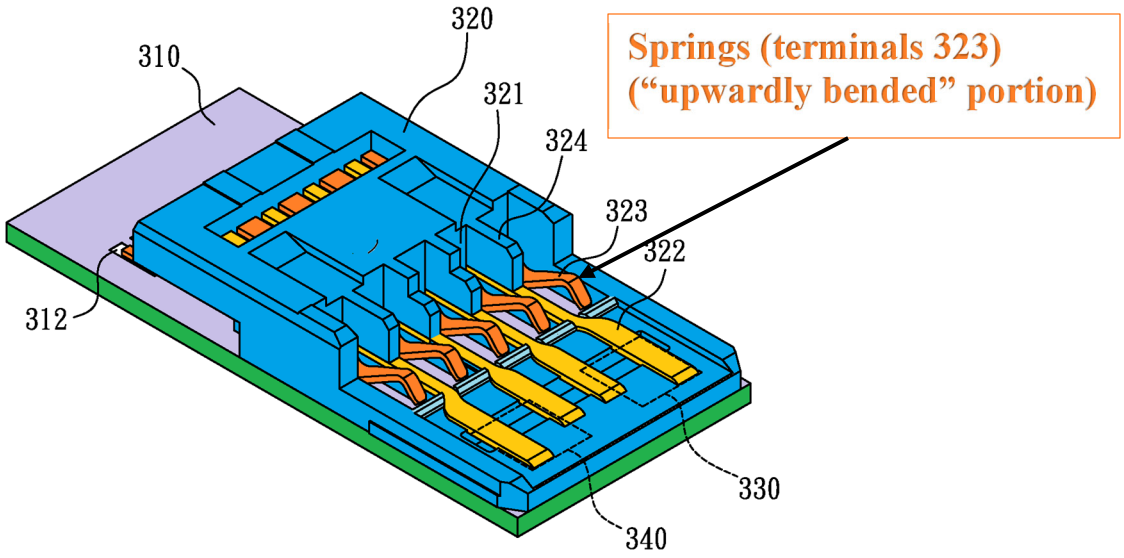


FIG. 10

Id., Fig. 10 (annotated); Ex. 1005, ¶¶ 163-165.

f) a plurality of connection fingers embedded to be exposed upon the cover of the contact bar, wherein the plurality of connection fingers are located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

Hsiao discloses a "plurality of connection fingers" (first terminals **322**) that are "embedded to be exposed upon the cover of the contact bar" (connector main body **320**). Ex. 1005, ¶ 167. One end of each of terminals **322** is "installed below the plural slot columns **324**" of connector main body **320**, "and exposed outside the slot columns **324** then forwardly extended." Ex. 1009 7:10-13, Fig. 10. These contacts are "integrally formed" with connector main body **320** before it is

mounted on the substrate's connection surface and are thus embedded. *Id.*, 7:39-47; Ex. 1005, ¶ 167.

This "embedding" occurs in two places. First, the terminals are embedded in the contact bar cover when they are installed below the slot columns **324** of connector main body **320**, and held in the openings in the horizontal lip shown in Ex. 1009, Fig. 10; Ex. 1005, ¶ 168.

Second, POSITA would have understood that the "forwardly extended" contact portion of terminals **322** would necessarily be fixed firmly in the front section of connector main body **320** to facilitate proper mating with and ensure compatibility with the USB 2.0 standard receptacle into which this connector is inserted. POSITA would have understood the front portion of terminals **322** (which bend downward) would be embedded in the connector main body as shown in figure 10 to secure the contacts and prevent them from bending upward or moving laterally. Ex. 1005, ¶ 168; Ex. 1009, Fig. 10 (annotated):

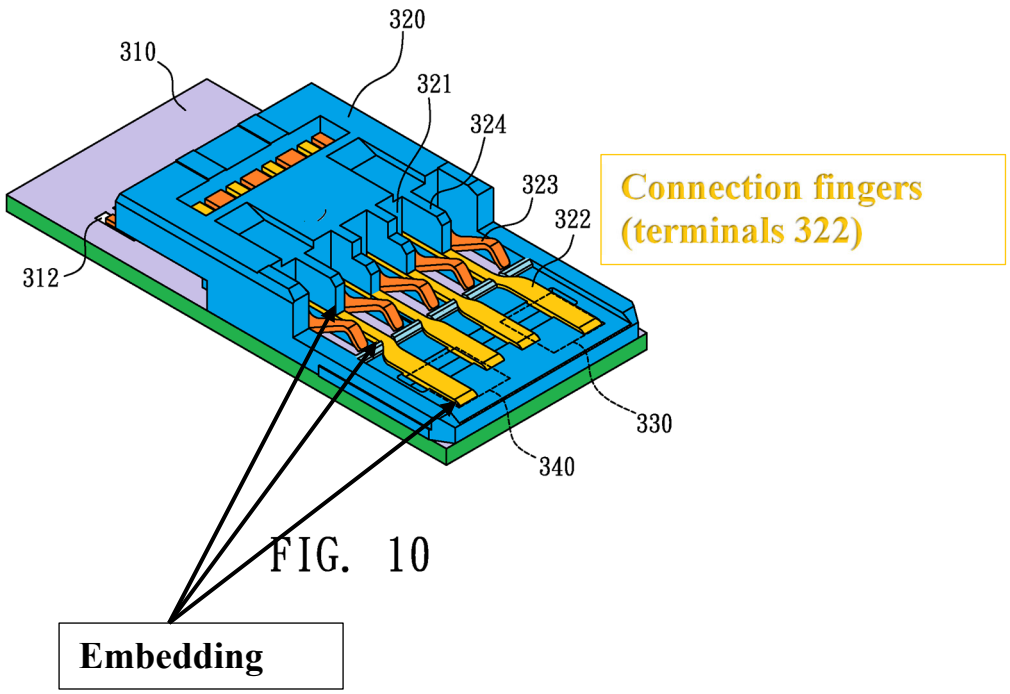


FIG. 10

The second distance is the height of the "forwardly extended" portions of terminals **322** above substrate **310's** connection surface. As Figure 10 shows, this second distance is less than the first distance. Ex. 1005, ¶ 169.

Notably, Hsiao's flash drive is configured to support the USB 2.0 and 3.0 protocols (*id.*, 7:47-50) and is a USB 3.0 Standard-A connector. *Id.*, 6:67-7:3 (explaining contact pads **312** transmit "StdA" signals). Thus, it must include the USB 3.0 Specification's two-tier contact arrangement for Standard-A connectors in which USB 3.0 SuperSpeed contacts (terminals **323** in Hsiao) are arranged in a row behind the USB 2.0 contacts (terminals **322** in Hsiao) and a portion of the

USB 3.0 SuperSpeed terminals sit above (in the vertical direction) the USB 2.0 contacts. *See* Section IV.B; Ex. 1005, ¶ 169.

g) wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of springs.

Hsiao teaches this element. *See, e.g.,* Ex. 1001, 7:47-50 ("the four first terminals **322** [connection fingers] of the USB connector are assembled as a USB2.0 connector, the five second terminals **323** [springs] of the USB connector are assembled as a USB3.0 connector"). *See* Ex. 1005, ¶¶ 170-171.

2. Claim 2

Claim 2 depends from claim 1 and requires that the each spring "further comprises a projection configured to be located at the first distance in an uncompressed position." *See* Appendix A. Hsiao teaches this limitation. The claimed projection is the high point of the springs' (terminals **323**) "upwardly bended" end, and the first distance is the projections' height above the substrate. When the springs are not mated with a corresponding connector's contacts (*i.e.,* uncompressed), the projections are located the first distance above substrate **310**. *See* Section X.A.1(e); Ex. 1005 ¶¶ 172-173; Ex. 1009, Fig. 10 (annotated):

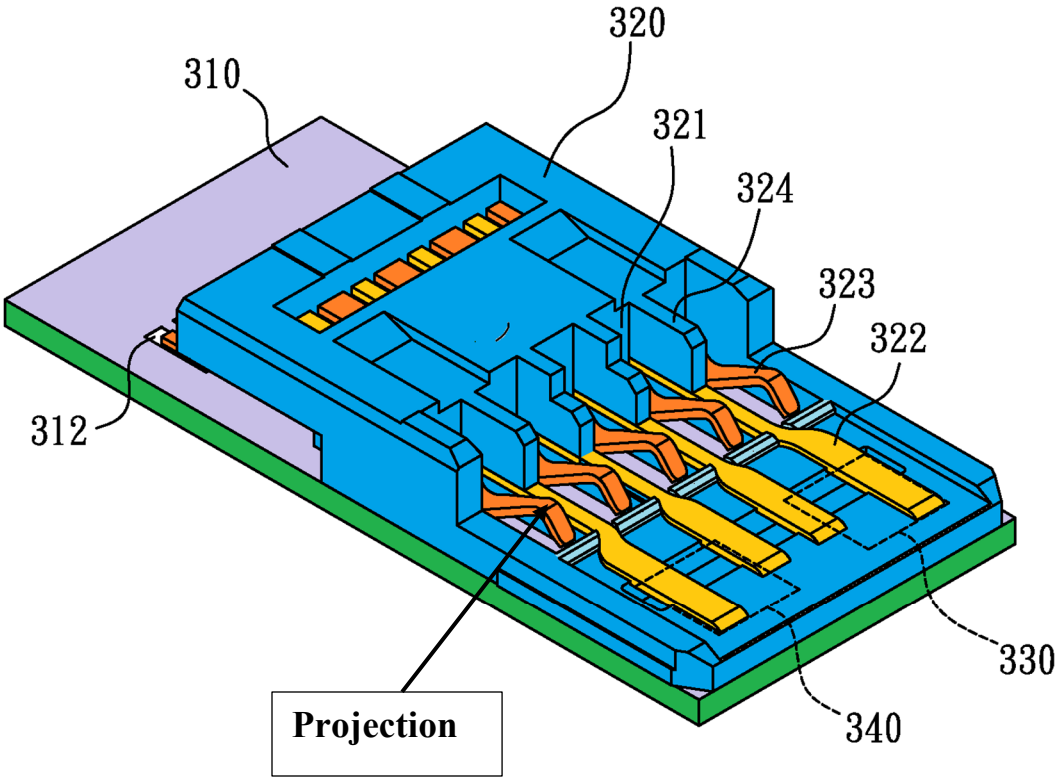


FIG. 10

3. Claim 3

Claim 3 depends from claim 2 and requires that "the projections are configured to extend through a plurality of apertures in the cover in the uncompressed position." *See* Appendix A. Hsiao teaches this limitation. As Figures 9-10 show, the projections extend through a plurality of apertures (slots **321**) in the cover (connector main body **320)** when uncompressed. Ex. 1009, 7:27-29 ("Moreover, one end of each of the second terminals **323** is further upwardly bended then downwardly bended after being exposed outside the opening slots **321**"); Ex. 1005 ¶¶ 174-175; Fig. 9-10 (annotated):

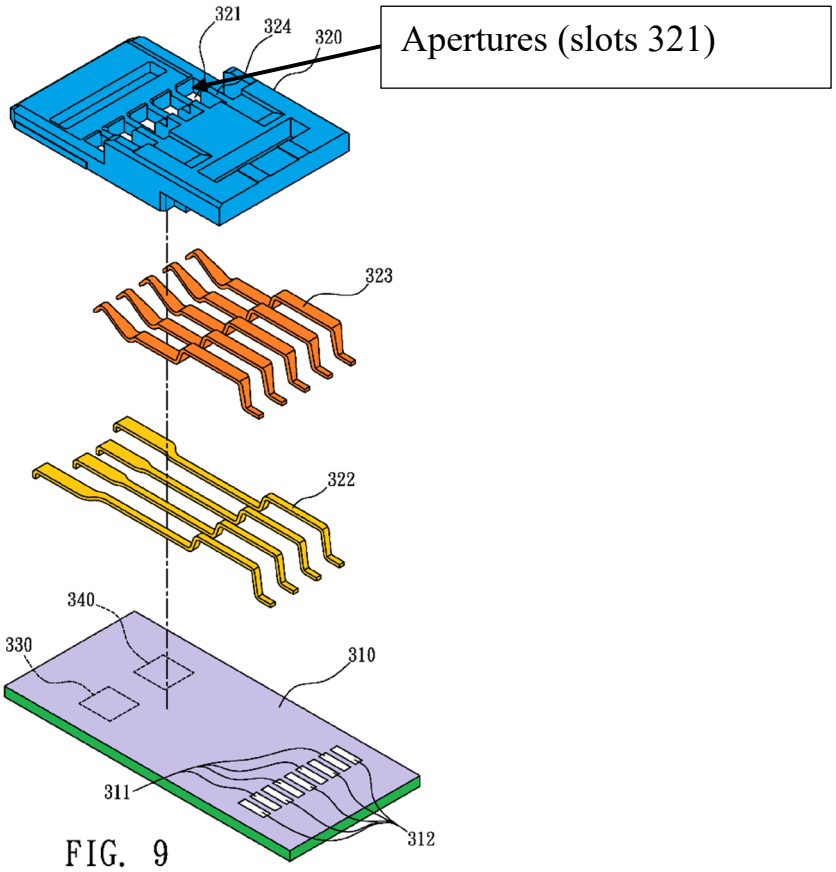


FIG. 9

4. Claim 4

Claim 4 depends from claim 1 and requires "the at least one memory die stack is mounted on the component surface of the substrate." *See* Appendix A. Hsiao teaches this limitation. Ex. 1009, 7:30-36 (disclosing substrate **310** has "at least one flash memory **340**" that is coupled to contact pads **311** and **312**.) Figures 9-10 disclose to POSITA that the memory **340** is mounted on the opposite surface of substrate **310** from the connection surface, *i.e.,* the component surface, through the use of dotted lines. Ex. 1005, ¶¶ 176-177.

5. Claim 9

Claim 9 depends from claim 1 and requires that the first and second distances each comprise heights above the substrate's connection surface, and the second height is less than the first. *See* Appendix A. *See* Appendix A. As Sections X.A.1(e) and X.A.1(f) explain, Hsiao teaches this limitation. *See* Ex. 1005, ¶¶ 178-179.

6. Claims 10 and 11

Claim 10 depends from claim 1 and requires that "each of the springs includes a connection pad," and claim 11 depends from claim 10 and requires that "each of the springs is integrally formed with the corresponding connection pad." *See* Appendix A. Hsiao teaches these limitations.

Hsiao explains that the springs (terminals **323)** and connection fingers (terminals **322**) are "integrally formed" with the contact bar cover (connector main body **320**), which is then mounted on substrate **310**'s connection surface by *inter alia* welding the springs' (terminals **323)** tail ends to substrate **310**'s contact pads **312** using surface mount technology. Ex. 1009, 7:39-47, Figs. 9-10.

These tails (shown in figure 9) are the springs' "connection pad[s]." Ex. 1005, ¶¶ 180-182.

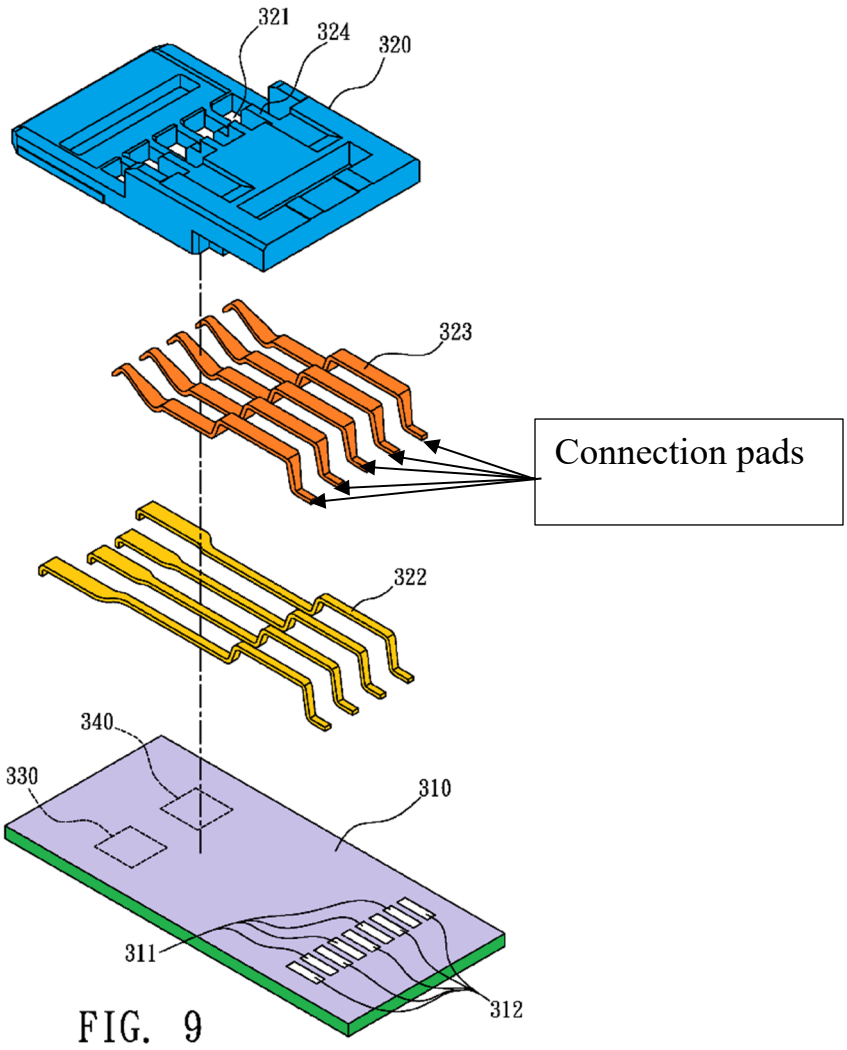


FIG. 9

As Ex. 1009, Fig. 9 shows, each spring is integrally formed with the corresponding connection pad as required by claim 11. Ex. 1005, ¶¶ 183-184.

7. Claim 12

a) Claim 12 Duplicates Elements (a)-(g) of Claim 1

Claim 12 – claiming "an external storage device" – duplicates elements [a]-[g] of claim 1. *Compare* Appendix A, claim 1 *with* claim 12. As discussed in Section X.A.1, Hsiao teaches these elements. *See* Ex. 1005, ¶¶ 154-171.

b) Hsiao Teaches the Additional Element of Claim 12

Hsiao teaches the additional limitation of claim 12 which requires "a plurality of coupling points mounted on the connection surface of the substrate for electrically coupling with the contact bar." *See* Appendix A, 12[h]. Contact pads **311** and **312** mounted on the connection surface of substrate **310** are the claimed coupling points. As discussed in Section X.A.1.b, contact pads **311** and **312** transmit USB 2.0 and 3.0 signals, respectively. When connector main body **320** is mounted on substrate **310**, the tail ends of the connection fingers (terminals **322**) and springs (terminals **323**) are welded onto first and second contact pads **311** and **312**, respectively. Ex. 1009, 7:39-54, Figs. 9-10. The contact bar is thereby electrically coupled with these coupling points. *See* Ex. 1005, ¶¶ 186-187.

8. Claim 13

Claim 13 depends from claim 12 and requires "the at least one memory die stack is mounted on the component surface of the substrate." *See* Appendix A. As explained in Section X.A.4, Hsiao discloses at least one memory die stack mounted on the substrate's component surface.

9. Claim 18

a) Claim 18 Duplicates Elements (a)-(g) of Claim 1

Claim 18 – claiming "an external storage device" –duplicates elements (a)-(g) of claim 1. *Compare* Appendix A, claim 1 *with* claim 18. As discussed in Section X.A.1, Hsiao teaches these elements.

b) Hsiao Teaches the Additional Element of Claim 18:

Claim 18 adds the limitation: "wherein the external storage device is configured to support Universal Serial Bus "USB") 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011." *See* Appendix A, claim 18[h]. The USB 2.0 and 3.0 standards published in April 2000 (Ex. 1007) and November 2008 (Ex. 1008), respectively were "in effect" as of January 31, 2011. Ex. 1019, ¶¶ 1-10; *see also* Ex. 1001, 1:37-45 (citing publication dates of USB 2.0 and 3.0 standards).

Hsiao teaches this limitation, and thus anticipates claim 18. *See, e.g.,* Ex. 1009, 7:47-54 ("the four first terminals **322** of the USB connector are assembled as a USB2.0 connector, the five second terminals **323** of the USB connector are assembled as a USB3.0 connector"); Ex. 1005 ¶¶ 191-192.

B. Ground 2: Claims 1-4, 9-13 and 18 are Obvious Over Hsiao

As Section X.A explains, claims 1-4, 9-13 and 18 are anticipated by Hsiao. Should the Board conclude, however, that: (1) the claim limitation "a plurality of connection fingers embedded to be exposed upon the cover of the contact bar"

(Appendix A, claims 1[f], 12[f], 18[f]) requires the *entire* "forwardly extended" portion of Hsiao's connection fingers (terminals **322**) to be embedded in the front portion of the contact bar cover (connector main body **320**), and (2) Hsiao does not explicitly disclose this, Hsiao renders claims 1-4, 9-13 and 18 obvious.

It would have been obvious to POSITA that the entire "forwardly extended" contact portion of terminals **322** could be embedded in the front portion of connector main body **320**. Ex. 1005, ¶ 193. POSITA would have been motivated to do so to increase the USB 2.0 interface's mechanical strength, inhibit lateral movement and upward bending of the contacts, and facilitate mating with a USB 2.0 standard receptacle. *Id*. POSITA would have had a reasonable expectation of success as embedding USB 2.0 contacts in insulative material in a USB 2.0 plug was commonplace and routine. *Id.*

C. Ground 3: Claims 1-18 Are Obvious Over Hsiao and Sun

1. Claims 1-4, 9-13, 18

As Sections X.A and X.B explain, Hsiao anticipates and/or renders obvious claims 1-4, 9-13 and 18.

Should the Board determine that Hsiao does not expressly disclose that Hsiao's "controller" is "configured to access memory," Sun discloses this, and Hsia and Sun combined render claims 1-4, 9-13 and 18 obvious. Sun discloses a USB 2.0/3.0 compatible "data storage device" that "comprises a multi-channel

flash memory assembly (100, 200, 300) which is constructed by stacking of flash memory members." Ex. 1014, Abstract.

Sun's USB 2.0/3.0 Compatible Flash Drive

Sun discloses a USB 2.0/3.0 compatible flash drive having a "USB 3.0 Controller" (**582**) that includes "NAND controller **510**" which "cooperate[s] with the flash memory assembly" to effectuate data transfer to and from the memory, and a "Main Controller **530**" connected between the NAND Controller and USB 2.0 and 3.0 physical layer interfaces ("PHY"). Ex. 1014 at 11-12, Fig. 9:

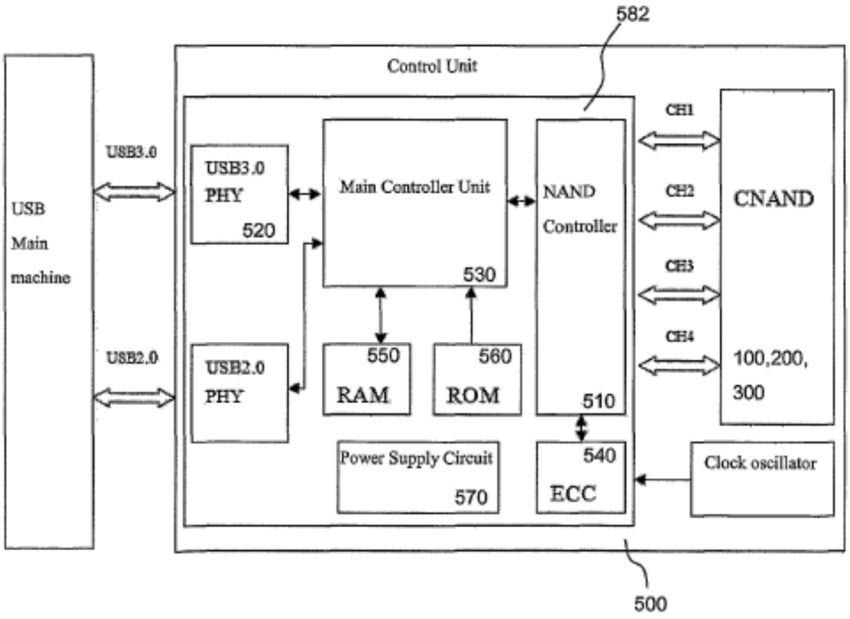


FIG. 9

It would have been obvious to POSITA to configure Hsiao's USB controller **330** to access Hsiao's flash memory **340** in order to effect data transfer to and from

memory in compliance with the USB specifications as taught by Sun. Ex. 1005, ¶¶ 194-197.

2. Claims 4-8 and 13-17

Claims 4-8 and 13-17 depend from claims 1 and 12 respectively and claim various placements of memory die stacks in the claimed "external storage devices" and/or the number of memory dies in a stack. *See* Appendix A. Sun discloses USB 2.0/3.0-compatible "USB memory sticks," having the memory arrangements of claims 4-8 and 13-17.

Sun discloses three flash memory assemblies, 100, 200 and 300, each of which has four stacked dies. *See* Ex. 1014 at 6 ("flash memory assembly 100 of Figures 2, and 2A" includes "a stack of 4 flash memory dies 102, 104, 106, & 108"), *id.* at 9 ("stack assembly 200 of Figures 3 and 3A has a structure substantially identical to that of Figures 2 and 2A"); *id.* at 9-10 ("structure and connection of the flash memory dies and PCB" for stack assembly 300 of Figs. 8, 8A "are identical to that of Figure 2"), *id.* at 10-11 ("the exemplary stack comprises 4 dies"); Figs. 2-2A, 3-3A, 8-8A:

Flash Memory Assembly (100)

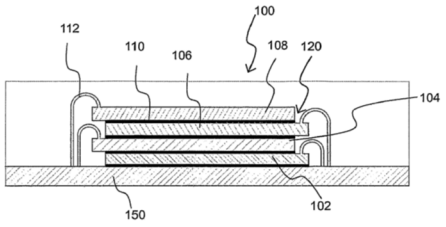


FIG. 2

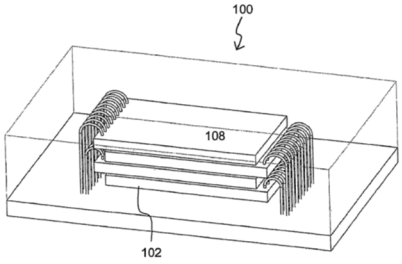


FIG. 2A

Flash Memory Assembly (200)

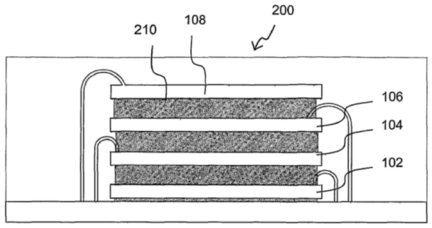


FIG. 3

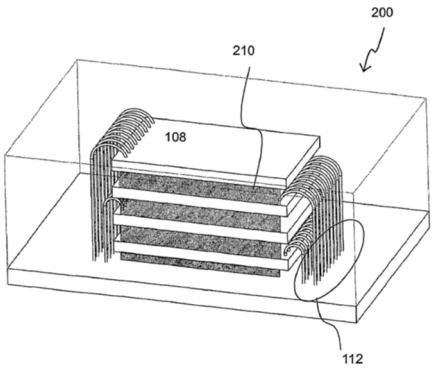


FIG. 3A

Flash Memory Assembly (300)

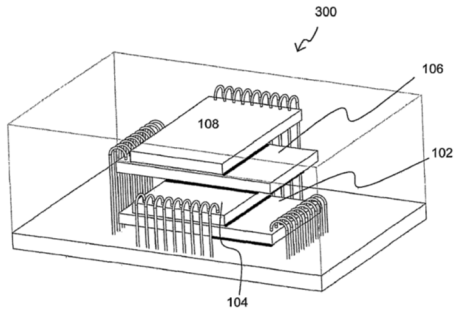


FIG. 8A

See Ex. 1005, ¶¶ 198-199.

a) Claims 4 and 13

Claims 4 and 13 require that the "external storage device" have at least one memory die stack mounted on the substrate's "component surface." Appendix A. Sun teaches this limitation in two places. First, Sun discloses an embodiment (Figs. 11-11C) in which the multi-channel memory die stack is placed on the surface opposite that on which the connector is mounted. *See, e.g.,* Ex. 1014, Figs. 11-11A.

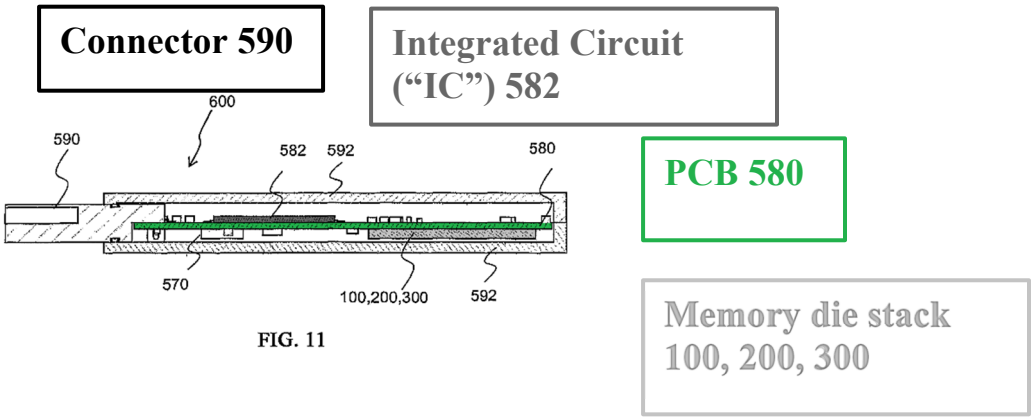


FIG. 11

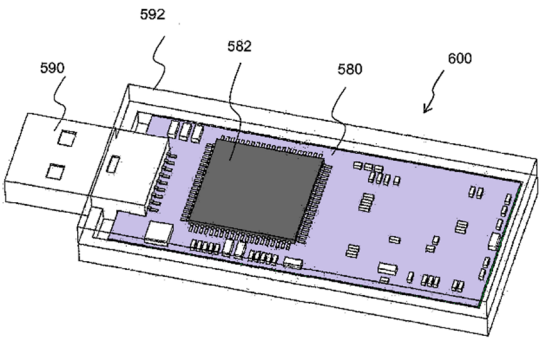


FIG. 11A

The memory die stack is 100, 200, or 300 and the connector is 590. Ex. 1014 at 12-13. As shown, connector **590** and IC **582** are mounted on the same side of PCB **580**, and Sun states that "flash memory assembly of the flash drive **600** is mounted on the side of the PCB **580** opposite to that on which the IC **582** is mounted . . .." *Id.* at 14, Figs. 11-11C.

Second, Sun discloses USB 3.0 flash drives having memory die stacks are mounted on ***both*** PCB surfaces (and thus at least one memory die stack mounted on the component surface):

> [M]ore than one flash memory stack could be included in each flash drive. ***For example, stacked flash memory assemblies could be mounted on both sides of the PCB***, and more than one stacked memory assembly could be mounted on the same side of the PCB, thereby substantially enhancing the storage capacity of the flash drive while maintaining a high speed performance due to the application of this multichannel stacked flash memory arrangement.

Id. at 14-15 (emphasis added). *See* Ex. 1005, ¶¶ 200-202.

b) Claims 5 and 14

Claims 5 and 14 require that the external storage devices of claims 1 and 12 have a memory die stack mounted on the substrate's "connection" surface. *See* Appendix A. Sun discloses this configuration. Ex. 1014 at 12, Fig. 10-10A:

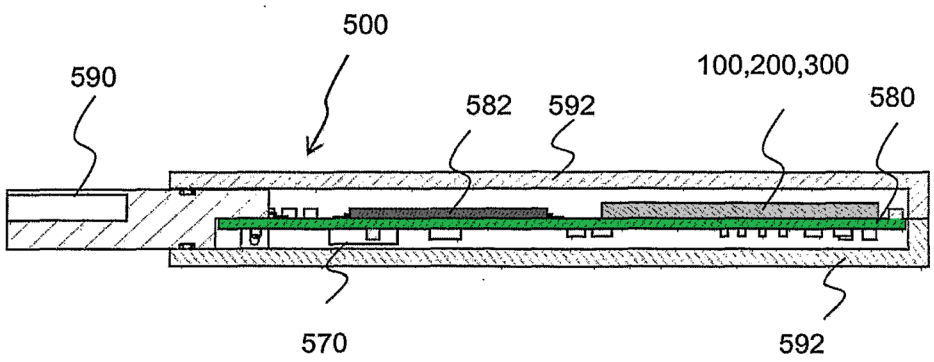
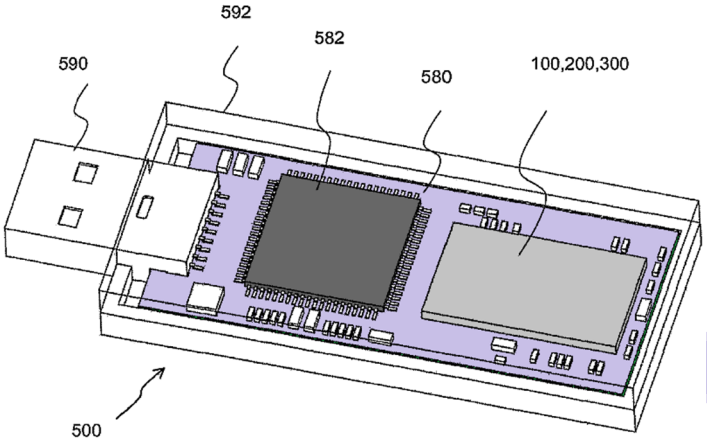


FIG. 10



Connection surface

FIG. 10A

Connector 590

IC 582

Memory die stack 100, 200, 300

As discussed, Sun also discloses that "more than one flash memory stack could be included in each flash drive," and "stacked flash memory assemblies could be mounted on both sides of the PCB" (Ex. 1014 at 14) thus meeting the requirement for at least one memory die stack mounted on the PCB's connection surface. *See* Ex. 1005, ¶¶ 203-204.

c) Claims 6 and 15

Claims 6 and 15 require that the "external storage devices" of claims 1 and 12 have a "plurality" of memory die stacks with at least one stack mounted on both the substrate's connection and component surfaces. *See* Appendix A. As discussed in Section X.C.2.a, Sun discloses this configuration. Ex. 1005, ¶ 205.

d) Claims 7 and 16

Claims 7 and 16 require that the plurality of memory die stacks of claims 6 and 15 each has a plurality of memory dies. *See* Appendix A. As Section X.C.2 explains, Sun discloses that the memory die stacks of claims 6 and 15 (flash memory assemblies **100**, **200** or **300**) each include 4 dies. Ex. 1005, ¶ 206.

e) Claims 8 and 17

Claims 8 and 17 require that the plurality of memory dies of claims 7 and 16 are arranged in an overlapping arrangement. *See* Appendix A. Sun discloses this arrangement:

> As shown more particularly in Figures 2 and 2A, the dies are organized such that the contact portion of one die is on one lateral end, while that of an adjacent die is on the direct opposite lateral end. This zigzag stacking facilitates a more balanced and symmetrical stacking to facilitate a more stable structure and enables more dies to be stackable in a stack to further increase storage capacity. In addition, this stacking arrangement also provides a more space efficient arrangement for the bonding wire to negotiate when extending from the die to the PCB.

Ex. 1014 at 9, Fig. 2, Fig. 8A:

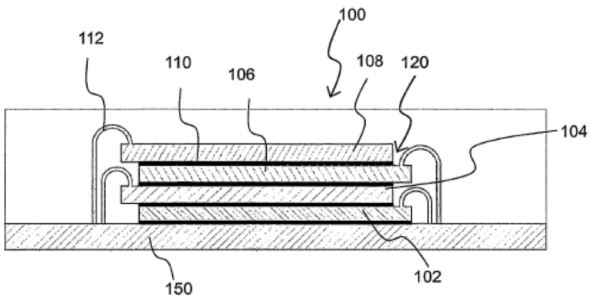


FIG. 2

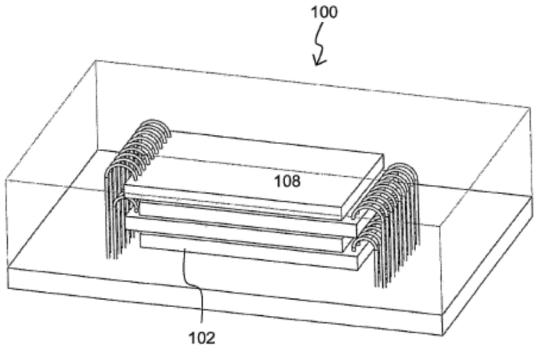


FIG. 2A

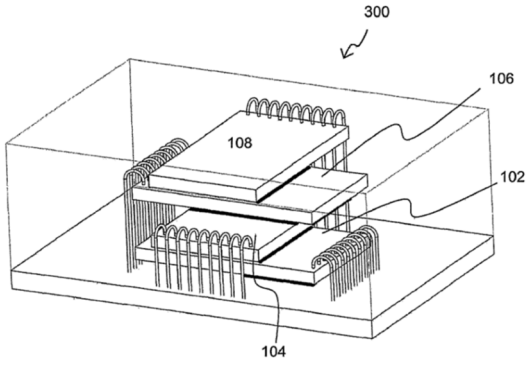


FIG. 8A

See Ex. 1005, ¶ 207.

It would have been obvious to POSITA to combine Hsiao with Sun to create external storage devices having the memory die stack arrangements claimed in claims 4-8 and 13-17. POSITA would be motivated to do so for the reasons set forth below. Ex. 1005, ¶ 208.

3. Motivation to Combine Hsiao With Sun

For external storage devices, POSITA had (and has) finite choices regarding which substrate surface(s) to mount a memory die stack on. Memory could be mounted on (1) the same surface as the USB connector, (2) the opposite surface, or (3) both surfaces. The decision of which surface(s) to use is a function of design requirements—*i.e.,* the desired dimensions and memory capacity of the storage device. Where a designer requires a slimmer device, the designer may choose to mount the memory on the same surface as the other components and the USB connector. Where keeping the device's length small is a consideration, the designer may choose to mount the memory on the surface opposite that on which the USB connector is mounted. Where the designer needs to increase memory capacity without substantially increasing the device's length, the designer may choose to mount a memory die stack on both surfaces, rather than placing memory die stacks side-by-side on the same surface. *See* Ex. 1005, ¶ 209.

POSITA would have been motivated to mount memory on the "component surface" of Hsiao's flash memory device as required by claims 4 and 13, and disclosed in Sun, Figs. 11-11C, where a design goal was to keep the overall device length shorter. *Id.*, ¶ 210.

POSITA would have been motivated to mount memory on the "connection surface" of Hsiao's flash memory device as required by claims 5 and 14, and

disclosed in Sun, Figs. 10-10C, where POSITA desired to minimize device thickness. *Id.*, ¶ 211.

POSITA would have been motivated to mount memory on both surfaces of Hsiao's flash memory device as required by claims 6 and 15 and disclosed in Sun (Ex. 1014 at 14) where POSITA desired to increase memory capacity without substantially increasing the overall length of Hsiao's device. Ex. 1005, ¶ 212.

The number of dies to include in a memory die stack, and the arrangement of those dies, is a function of the desired size and memory capacity of the device. Where greater memory capacity is required, a designer could include more dies in the stack, stacking them in a way that best meets the desired size requirements for the device. Ex. 1005, ¶ 213.

POSITA would have been motivated to include a plurality of memory dies in the memory die stacks of Hsiao's flash memory device as required by claims 7 and 16, and disclosed in Sun, in order to increase memory capacity without substantially increasing the length of Hsiao's device. As Sun teaches, "the footprint of the flash memory assembly" having multiple dies "is about the same as that of a single flash memory die **102**, **104**, **106**, and **108**." Ex. 1014 at 13; Ex. 1005, ¶ 214.

POSITA would have been motivated to stack the dies in an "overlapping arrangement" as required by claims 8 and 17 and taught by Sun in order to

facilitate wire bonding of the dies to the substrate and aid in miniaturization of the device. Ex. 1005, ¶ 215.

D. Ground 4: Claims 1-6 and 9-15 Are Obvious Over Chen and Cheng

As shown below Chen (Ex. 1010) and Cheng (Ex. 1012) combined teach the alleged inventions of claims 1-6 and 9-15, and render these claims obvious. Ex. 1005, ¶ 216, 256.

1. Claim 1

a) An external storage device comprising

Chen discloses an "external storage device," *i.e.,* memory device **300**. Ex. 1010, FIG. 13, 11:43-48 ("A second embodiment of the present invention is disclosed in FIG. 13. In this embodiment, the extension to USB is a memory device **300**. The memory device **300** includes an outer case **36** enclosing a printed circuited board with a memory unit (not shown) and an interface **31** electrically connecting with the printed circuit board.")

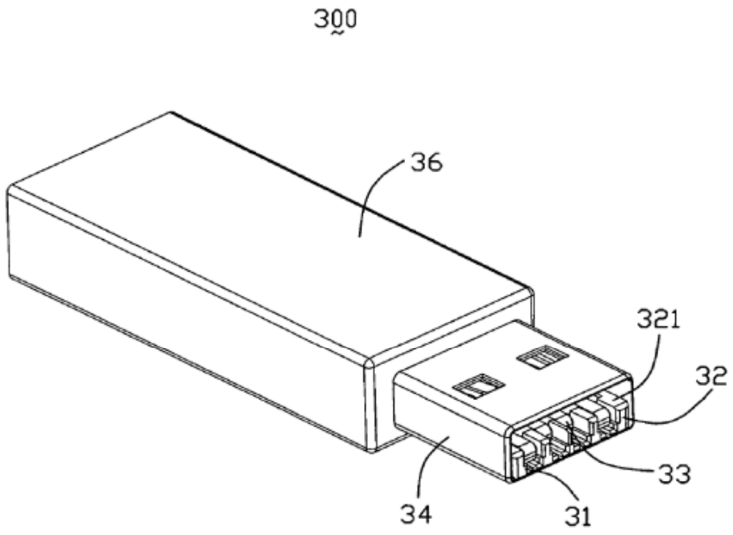


FIG. 13

POSITA would have understood Figure 13 to depict a USB memory device which is an external storage device. Ex. 1005, ¶ 217-219.

b) a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

The substrate is the PCB described above which necessarily has two opposite surfaces. In memory device **300** "tail portions" of the connector plug contacts **33** are "physically and electrically connected to the printed circuit board." Ex. 1010, 11:55-58. The PCB's "connection surface" is the surface to which these "tail portions" are physically and electrically connected. The "component surface" is the opposite PCB surface. Ex. 1005, ¶¶ 220-221.

Moreover, Cheng discloses "a space-minimized flash drive to effectively reduce" the flash drive's length "to miniaturize the flash drive without greatly increasing the manufacturing costs during mass production." Ex. 1012, **[0006].** Cheng's flash drive includes a PCB with two opposite surfaces in which memory is mounted on both surfaces to increase the device's memory capacity without increasing its length. *Id.*, **[0030]**, **[0035]**. It would have been obvious to POSITA to combine Chen and Cheng to create a storage device wherein the PCB has two opposite surfaces on which components could be mounted in order to keep the device's overall length smaller. Ex. 1005, ¶ 222.

c) at least one memory die stack mounted on one of the connection surface and the component surface;

Chen discloses that memory device **300** includes "a printed circuit board with a memory unit (not shown)." Ex. 1010, 11:45-47. POSITA would have known that this "memory unit" necessarily includes at least one memory die, and Chen's "memory unit" is necessarily mounted on one of the PCB's surfaces. Ex. 1005, ¶ 224.

d) a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

Chen does not expressly disclose that the "memory unit" of memory device **300** includes a controller. Chen, however, teaches that portable USB memory

devices require controllers. *See* Ex. 1010, 2:12-18, 2:27-29 (Explaining that prior art "***peripheral[s], like a portable memory device***," with "type-A USB connector" **500** include "four conductive contacts **53**" that "carry the USB signals generated or received ***by a controller chip in the peripherals.***") (emphasis added).

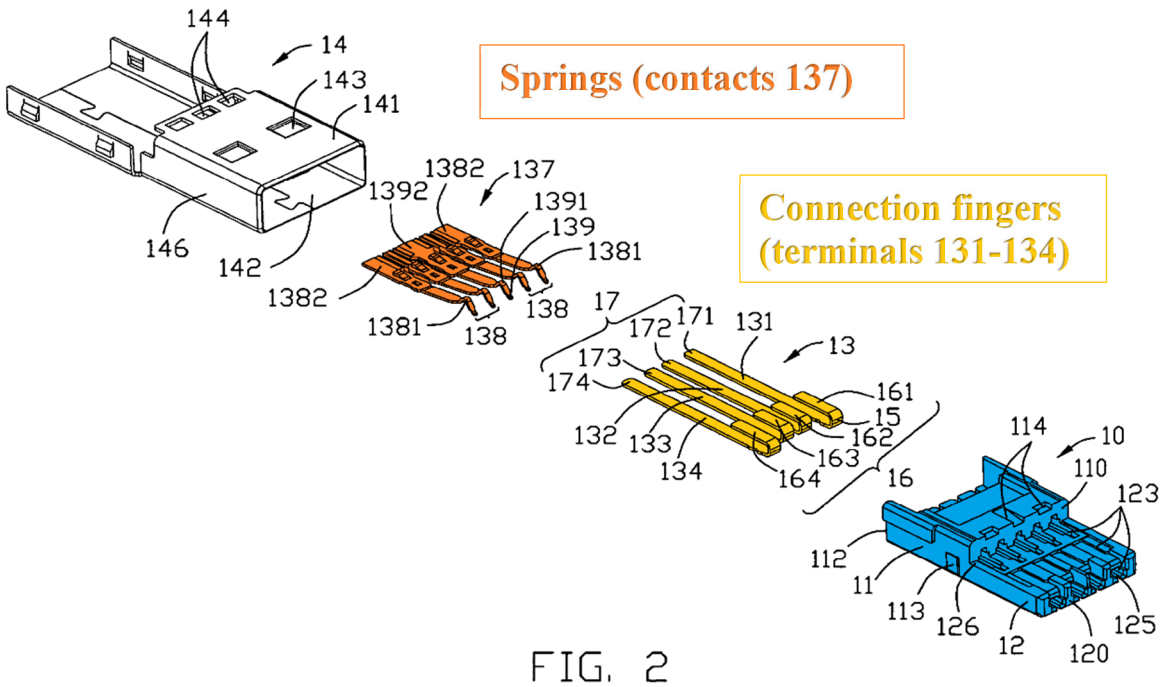
POSITA would have known that a memory controller is necessarily present in the memory device **300**, that it would be mounted on a PCB, and the controller's purpose is to provide a compatible interface between the USB 2.0/non-USB 2.0 buses and memory, and manage read/write operations between the memory and the buses to ensure communications follow the protocols. Ex. 1005, ¶¶ 225-227.

Moreover, Cheng discloses that "[a] conventional flash drive not only has a USB connector" but also "controllers." Ex. 1012, **[0004]**. Cheng discloses a USB flash drive wherein a controller is mounted on PCB **110**, and "electrically connected" to memory and the USB connector, and thus configured to access memory. *Id.*, **[0023], [0027]-[0029]**. It would have been obvious to POSITA to include a controller in Chen's memory device **300** mounted on the PCB as taught by Cheng. POSITA would have been motivated to do so to provide a standard compatible interface between the USB 2.0 bus/non-USB 2.0 bus and the memory, and provide a way to manage read/write operations to and from memory. *See* Ex. 1005, ¶¶ 228-229.

e) a contact bar mounted on the connection surface of the substrate, the contact bar comprising a cover and a plurality of springs, each of the plurality of springs including a portion that is located at a first distance relative to the connection surface of the substrate

Chen discloses "an extension to USB plug **100**," depicted in Figs. 1-5. Ex. 1010, 5:47-49. In Chen's second embodiment – memory device **300** – the plug is the same as extension to USB plug **100**. Chen states "interface **31** includes a tongue portion **32**, a plurality of contacts **33** supported on a supporting surface **321** of the tongue portion **32**. The tongue portion **32** and the contacts **33** are both with an arrangement same to [that] of the extension to USB plug **100** shown in FIG. 1, which is compatible to [that] of the standard USB connector." *Id.*, 11:43-54; *see also id.,* 11:65-12:22 (describing contacts), claim 3 (claiming memory device). Memory device **300** can mate with either a standard USB receptacle "or the extension to USB receptacle **200** shown in Figure 6" (*id.*, 11:62-65), which requires memory device **300**'s plug to have the same configuration as USB plug **100** extension. Ex. 1005, ¶¶ 230-231.

Chen discloses the claimed contact bar and describes it with reference to figures 2 and 3 (annotated):



Springs (contacts 137)

Connection fingers (terminals 131-134)

FIG. 2

Contact bar cover (housing 10)

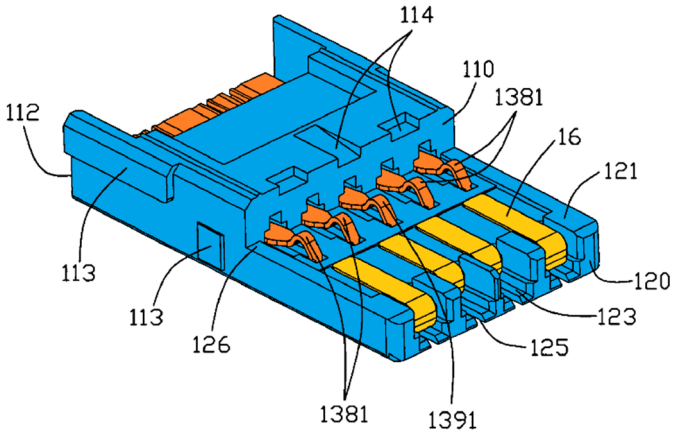


FIG. 3

See Ex. 1005, ¶ 232

The contact bar comprising a cover and springs is housing **10** (contact bar cover), with additional contacts **137** (springs) installed in passageways **123**. *Id.*, ¶¶ 233-234.

"[T]he plug contacts **13** include four plug conductive contacts designated [**131-134**] and a plurality of additional plug contacts **137**." Ex. 1010, 6:31-34; *see also id.*, 11:66-12:22 (discussing contacts in disclosed embodiments), claim 3. "[C]ontacts **137** include two pairs of differential plug contacts **138** and a grounding plug contact **139**." *Id.*, 7:15-17; *see also id.*, 12:18-22, Fig. 2, claim 3. These contacts have "elastic contact portion[s]" designated **1381** and **1391** (*id.*, 7:21-22, 7:27-30, Fig. 3), and thus are "springs." Ex. 1005, ¶ 234.

The housing **10** has "passageways **123** for receiving the additional plug contacts **137**" that "are located behind the passageways **123** for receiving the four plug conductive contacts [**131-134]** along the front-to-rear direction." Ex. 1010, 6:37-41. "[E]ach contact portion **1381**, **1391** is cantileveredly received in the passageways **123** and ***protruding upwardly beyond the supporting surface 121*** so that the ***contact portion 1381, 1391 is elastic and deformable*** when engaging with corresponding contacts of the extension to USB receptacle **200**." *Id.*, 7:43-48 (emphasis added); *see also id.* Figs. 3-4.

In memory device **300** the contact bar is mounted on the PCB by "physically and electrically" connecting the contacts' "tail portions" to the PCB. *Id.*, 11:55-58.

The first distance is the height of contact portions **1381**, **1391** above the PCB surface on which the contact bar is mounted. Ex. 1005, ¶¶ 235-237.

f) a plurality of connection fingers embedded to be exposed upon the cover of the contact bar, wherein the plurality of connection fingers are located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

Chen discloses the claimed plurality of connection fingers as conductive contacts **131-134** which Chen explains "are substantially of the same configuration" and include "a plug contact portion **16**" that "is flat and non-elastic." Ex. 1010, 6:50-58, Figs. 2-3.

These connection fingers are embedded to be exposed upon the cover of the contact bar (housing **10**). "A plurality of plug contact receiving passageways **123** are recessed in the supporting surface **121** of the plug tongue portion **12**." *Id.*, 6:28-30. The passageways are for receiving "the four conductive contacts [**131-134**]." *Id.*, 6:34-37. When these contacts "are inserted into corresponding passageways **123**, each plug contact portion **16** thereof is substantially coplanar with the supporting surface **121** as shown in FIGS. **3-4**." *Id.*, 6:58-62, Figs 3-4. As Fig. 3 shows, the connection fingers plug contact portion **16** is embedded in the contact bar cover (housing 10).

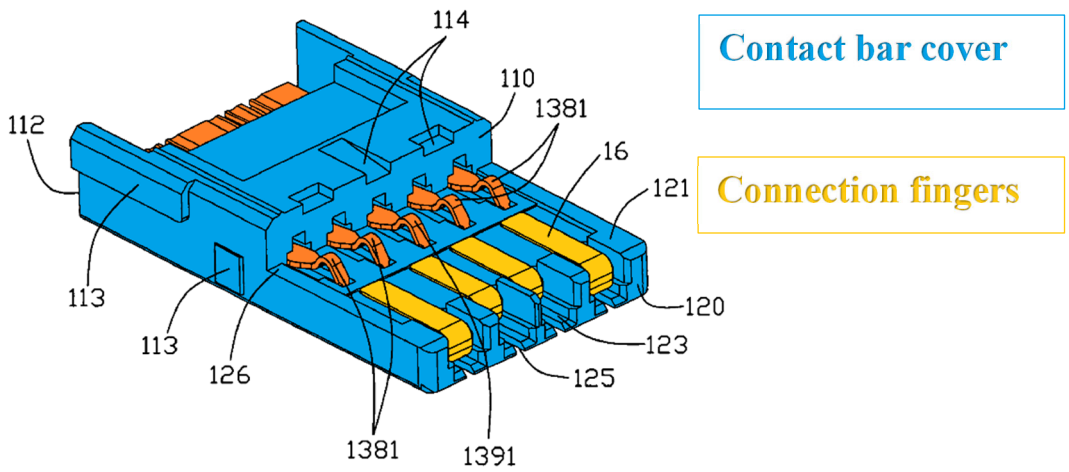


FIG. 3

Ex. 1010, Fig. 3 (annotated).

The second distance is the height of plug contact portion **16** above the PCB surface. Since plug contact portion **16** "is substantially coplanar with the supporting surface **121**" (*id.*, 6:60-62) and portions **1381/1391** of the springs "protrud[e] upwardly beyond the supporting surface **121**" (*id.*, 7:45-46), the second distance is necessarily less than the first distance. Figure 4 (annotated) illustrates this (black arrow shows first distance, red arrow shows second distance):

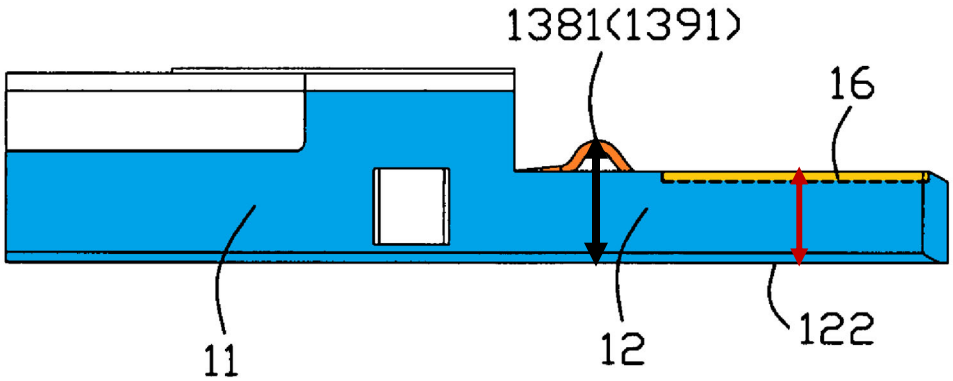


FIG. 4

See Ex. 1005, ¶¶ 238-241.

g) wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of springs

Chen discloses the plurality of connection fingers (contacts **131-134**), are "for USB protocol to transmit USB signals. In detail, the four conductive contacts [**131-134**] are for power (VBUS) signal, -data signal, +data signal and grounding, respectively." Ex. 1010, 7:59-64, 12:5-11. In contrast, the plurality of springs (contacts **137**) are "for a non-USB protocol." *Id.*, 12:14-19; Ex. 1005, ¶¶ 242-243.

2. Claims 2-3 and 9-11

Claims 2-3 and 9-11 depend from claim 1, either directly or indirectly. As shown, Chen and Cheng combined disclose the elements of claim 1 and render it obvious. Chen also teaches the additional elements of claims 2-3 and 9-11, and Chen and Cheng combined render these claims obvious. .

a) Claim 2

Claim 2 requires that the spring's projections be located at the first distance when uncompressed. *See* Appendix A. Chen discloses this limitation. The "projection" is elastic portions **1381/1391** that "protrud[e] upwardly beyond the supporting surface **121**." Ex. 1010, 7:43-48. When the springs are uncompressed, (*i.e.,* not mated with a receptacle) the projection is located at the first distance, *i.e.,*

the height of the projection above the PCB surface, as shown in Fig 4 above. *See* Ex. 1005, ¶¶ 244-245.

b) Claim 3

Claim 3 requires that the spring's projections of claim 2 extend through apertures in the cover when the springs are uncompressed. *See* Appendix A, claim 3. As Figure 3 shows, Chen discloses this limitation. The apertures include rear passageways **123** into which the terminals **137** are inserted, and the slots depicted below the elastic portions **1381/1391** of terminals **137**. *See* Section X.D.1; Ex. 1005, ¶¶ 246-248.

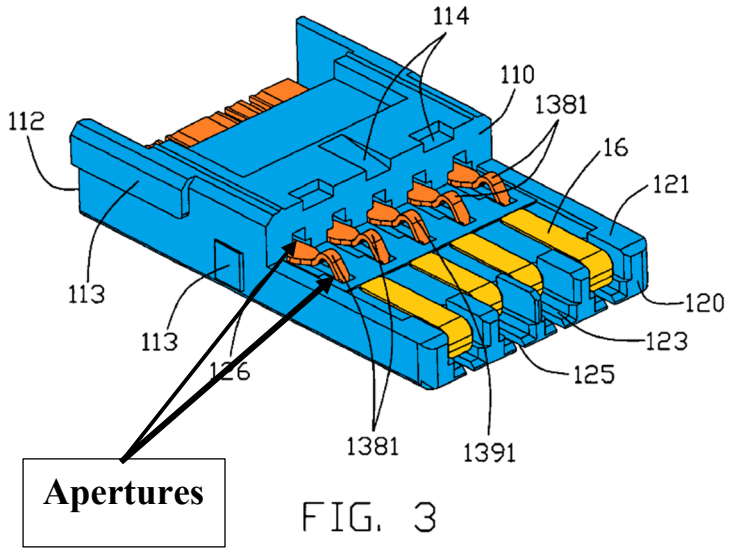


FIG. 3

Ex. 1010, Fig. 3 (annotated)

c) Claim 9

Claim 9 requires the first and second distances each comprise heights above the PCB's connection surface, and the second height is less than the first. *See* Appendix A. As explained in Sections X.D.1(e) and X.D.1(f), Chen discloses this limitation. *See* Ex. 1005, ¶¶ 249-250.

d) Claims 10 and 11

Claim 10 requires that each spring include a connection pad, and claim 11 requires that each spring "is integrally formed with the corresponding connection pad." Appendix A.

Chen also teaches these limitations. Chen discloses that the springs (contacts **137**) each includes a "tail portion" designated **1382** (for differential contacts **138**) and **1392** (for grounding contact **139**). Ex. 1010, 7:21-31. Figure 2 shows these "tail portions" (**1382** and **1392):**

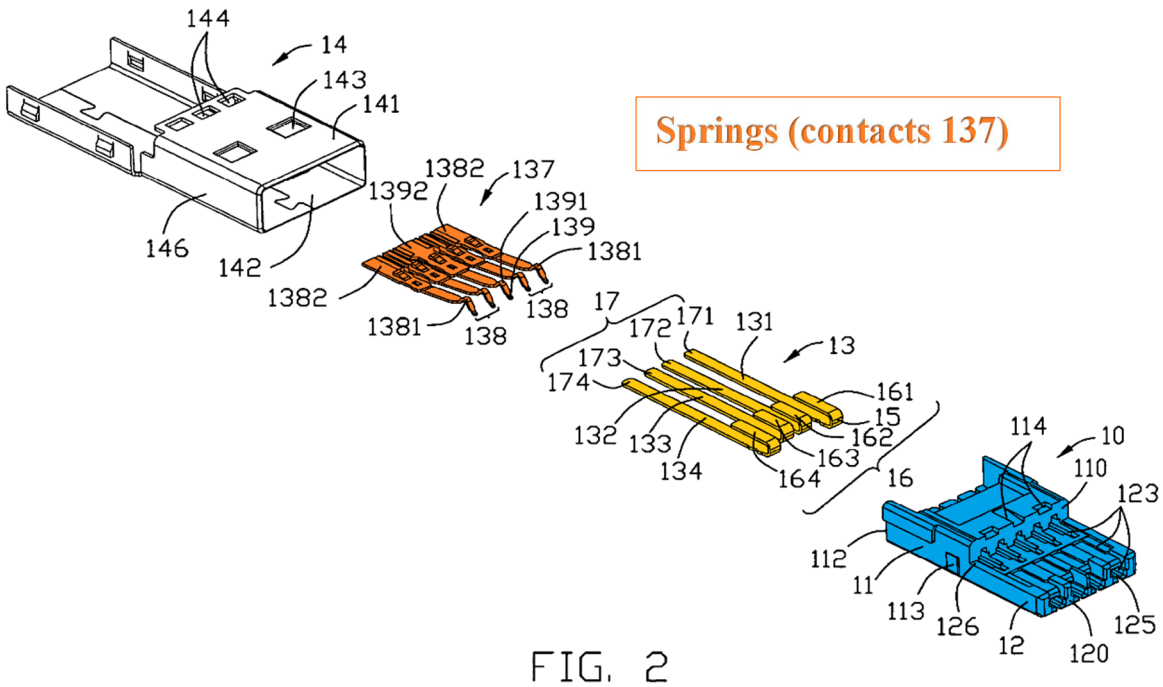


FIG. 2

Chen explains that in memory device **300**, the contacts' "tail portions" are "physically and electrically connected" to the device's PCB. *Id.*, 11:55-58. The springs' (contacts **137**) tail portions (**1382, 1392)** constitute claim 10's "connection pads." As Figure 2 shows, the tail portions are "integrally formed" with the springs (contacts **137**) as required by claim 11. Ex. 1005, ¶¶ 251-253.

3. Claim 12

Section X.A.7 explains that claim 12 contains the limitations of claim 1 and further requires "a plurality of coupling points" mounted on the substrate's connection surface "for electrically coupling with the contact bar." As discussed, Chen and Cheng combined disclose the elements of claim 1. Chen discloses claim 12's additional limitation.

Section X.D.1(e) explains that in Chen's memory device **300** the contacts' "tail portions" are "physically and electrically connected" to the PCB. In Chen's device, the "tail portions" are flat and located at the rear of the contacts. *See* Ex. 1010, Fig. 2.

POSITA would have known that to physically connect them to the PCB would require that they be soldered to the PCB. Thus, the PCB necessarily must have a plurality of coupling points to accommodate these physical connections of the tail portions. Moreover, it would have been obvious to POSITA that in order to make these physical and electrical connections, the PCB would require a plurality of coupling points on which to solder the contacts' "tail portions." Ex. 1005, ¶¶ 254-255.

4. Claims 4-6 and 13-15

Chen and Cheng combined render claims 4-6 and 13-15 obvious. Claims 4-6 depend from claim 1 and claims 13-15 depend from claim 12. *See* Appendix A. Sections X.D.1 and X.D.3 explain that Chen and Cheng combined teach the elements of claims 1 and 12 and render these claims obvious.

Dependent claims 4-6 and 13-15 are directed to the placement of memory die stacks on the external storage device's substrate. *See* Appendix A. Chen discloses that memory device **300** has a "memory unit" mounted on the device's substrate (a PCB), but does not explicitly state which PCB surface the memory unit

is mounted on. *See* Section X.D.1(c). Cheng discloses a USB device with memory mounted on both substrate surfaces, and thus teaches the limitations of claims 4-6 and 13-15. Ex. 1005, ¶¶ 256-257.

a) Claims 4 and 13

Claims 4 and 13 require at least one memory die stack mounted on the substrate's component surface. *See* Appendix A. POSITA would have been motivated to mount memory on the component surface of Chen's device where POSITA desired to minimize the device's length. Ex. 1005, ¶¶ 256-258.

Additionally, Cheng discloses a USB flash drive in which a plurality of memory die stacks, flash memories **150** and **130**, are mounted on opposite surfaces (**111A** and **111B)** of the substrate PCB **110**. Ex. 1012, **[0030]**, Fig. 2 (annotated):

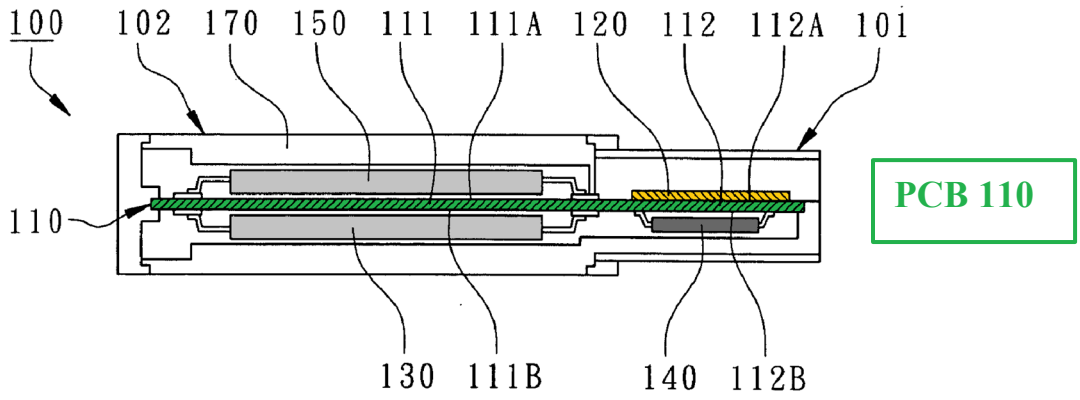


FIG. 2

Memory die stack
150, 130

In another embodiment, flash memories **250**, **230**, are mounted on opposite surfaces (**211A** and **211B)** of the substrate (PCB **210)** using "COB processes and are electrically connected to the printed circuit board through wire bonding." Ex. 1012, [0035-36], Fig. 6:

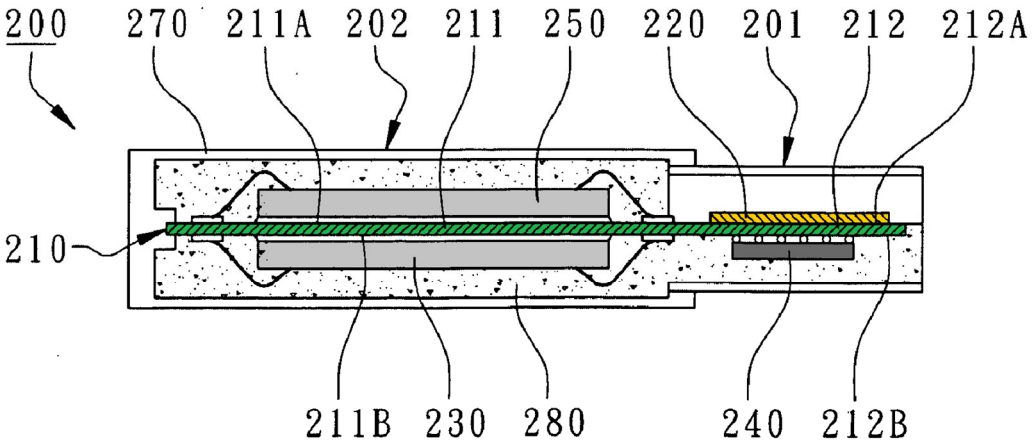


FIG. 6

Cheng's disclosure of mounting memory on both surfaces requires at least one memory die stack mounted on the substrate's component surface. Cheng explains that mounting flash memory on both PCB surfaces permits miniaturization of a flash memory device by keeping device length smaller while providing for "higher memory capacities." Ex. 1012, [**0010**], [**0030**]. POSITA would have been motivated to utilize the memory layout of Cheng, which includes at least one memory die stack mounted on the PCB's component surface in Chen's

memory device **300** device, in order to increase memory capacity without substantially increasing the device's length. Ex. 1005, ¶¶ 259-263.

b) Claims 5 and 14

Claims 5 and 14 require at least one memory die stack mounted on the substrate's connection surface. *See* Appendix A. POSITA would have been motivated to mount memory on the connection surface where POSITA desired to create a slimmer device. Ex. 1005, ¶ 264.

Additionally, as discussed, Cheng discloses mounting memory on both substrate surfaces and thus discloses this limitation. POSITA would have been motivated to mount memory on both PCB surfaces of Chen's memory device **300**, as disclosed in Cheng, to further increase the memory capacity of Chen's device without substantially increasing its length. *Id*., ¶ 265.

c) Claims 6 and 15

Claims 6 and 15 require a memory die stack mounted on both of the substrate's surfaces. *See* Appendix A. As discussed, Cheng discloses placing memory die stacks on both substrate surfaces. POSITA would have been motivated to do so in Chen's memory device **300** to increase the memory capacity of Chen's device without substantially increasing its length. Ex. 1005, ¶ 266.

E. Ground 5: Claims 7-8 and 16-17 are Obvious Over Chen and Cheng and Further in View of Hiller

Chen, Cheng, and Hiller combined render claims 7-8 and 16-17 obvious. Claims 7-8 depend from claim 6, either directly or indirectly, and claims 16-17 depend from claim 15, either directly or indirectly. Claims 7 and 16 require that the memory die stacks of claims 6 and 15 comprise "a plurality of dies," and claims 8 and 17 require that the dies "of at least two of the plurality of memory die stacks are stacked in an overlapping arrangement." Appendix A.

Section X.D.4 explains that (1) claims 6 and 15 require at least one memory die stack mounted on each of the substrate's surfaces, (2) POSITA would have been motivated to mount memory on both substrate surfaces to increase memory capacity without substantially increasing the device's length, (3) Cheng discloses a USB memory device with memory die stacks mounted on both substrate surfaces, and (3) Chen and Cheng combined disclose the elements of claims 6 and 15 and render those claims obvious.

Hiller (Ex. 1013) discloses the additional elements of claims 7-8 and 16-17. Hiller describes a "conventional approach" to memory die stacking that includes stacking "same-sized dies with overhanging designs." Ex. 1013, **[0003]**. Hiller also discloses "a memory device comprising at least one memory stack of stacked

memory dies which are staggered with respect to each other." Ex. 1013, **[0004]**; Figs. 8-9 and 18:

FIG 8

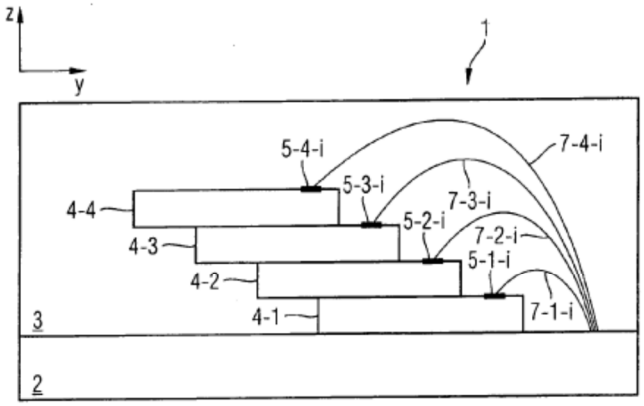


FIG 9

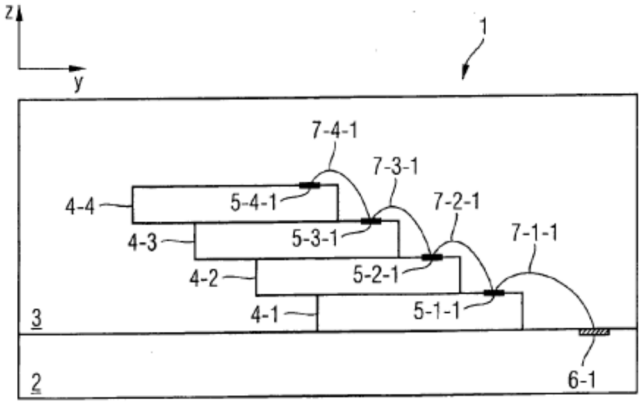
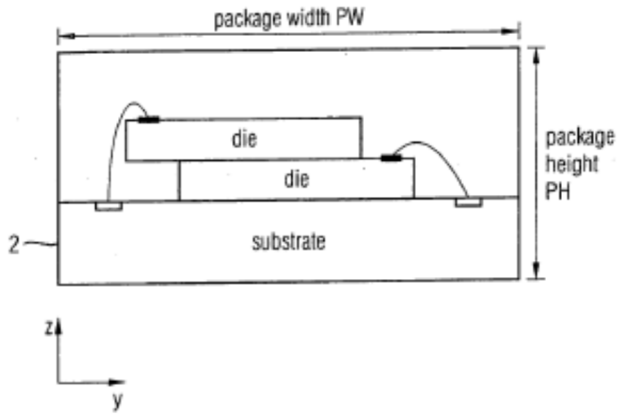


FIG 18



Ex. 1005, ¶¶ 267-269. It would have been obvious to POSITA to utilize the conventional approach of memory die stacking in Chen's device, and POSITA would have been motivated to do so because using stacks having multiple dies allows for a memory device with greater storage capacity contained in a smaller space. *Id.* at 270. Moreover, the overlapping arrangement facilitates wire bonding of the dies to the PCB while, as Hiller discloses, meeting constraints in the "y" direction, *i.e.,* PCB length. Ex. 1014, [0126]; Ex. 1005, ¶ 270.

F. Ground 6: Claims 1-18 are Obvious Over Chen and Sun

1. Claims 1-3 and 9-11

Sections X.D.1 and X.D.2 explain that Chen teaches elements [a]-[c] and [e]-[g] of claim 1 and the additional elements of claims 2-3 and 9-11 which depend from claim 1, but Chen does not expressly disclose element 1[d] "a controller

configured to access the at least one memory die stack" mounted on the PCB. *See* Appendix A, claim 1[d].

Sun discloses USB 3.0-compatible external storage devices having a controller configured to access memory—*i.e.,* "USB 3.0 controller" comprising *inter alia* NAND controller **510** and main controller unit **530.** Ex. 1014 at 11-12; Section X.C.1. The "USB 3.0 controller" (**582**) is "mounted on the PCB." Ex. 1014 at 12-13, Figs. 9, 10-10B. It would have been obvious to POSITA to include a controller as disclosed in Sun in Chen's memory device **300** to have a way to manage read/write operations and implement Chen's USB 2.0/non-USB 2.0 protocols. Ex. 1005, ¶¶ 271-274.

Sun also discloses that these storage devices have a PCB with two opposing surfaces and components mounted on both PCB surfaces. *See* Sections X.C.1 and X.C.2. It would have been obvious to POSITA to mount components on both PCB surfaces in Chen's memory device **300** to aid in shortening the device. Ex. 1005, ¶¶ 275.

Chen and Sun combined thus teach the elements of claim 1-3 and 9-11 and render them obvious. *Id.*, ¶¶ 276-277.

2. Claim 12

Section X.D.3 explains that Chen teaches elements [a]-[g] of claim 12 with the exception of element [d]—the claimed controller. As discussed in the

preceding section, it would have been obvious to POSITA to include the claimed controller, as disclosed in Sun, in Chen's memory device **300**.

Additionally, claim 12 requires that the substrate include "a plurality of coupling points mounted on the connection surface of the substrate for electrically coupling with the contact bar." Appendix A, claim 12[h]. Chen teaches that in memory device **300**, the contact bar is mounted on the PCB by "physically and electrically" connecting the contacts' tail ends to the PCB. Ex. 1010, 11:55-58. As discussed, POSITA would have known that the PCB in Chen's device would necessarily require a plurality of coupling points on which to physically connect these tail portions. *See* Section X.D.3. Chen, however, does not depict the connection of the contact tail portions to the PCB.

Sun depicts a USB 3.0-compliant flash drive in which the contact tail portions (for all 9 contacts of plug **590**) are mounted on PCB **580.** PCB **580** thus requires a plurality of coupling points. Ex. 1014 at 12-13 ("A USB connector **590** is also mounted on the PCB and in electrical communication with the USB 3.0 and USB 2.0 PHY interfaces"), Fig. 10A (annotated):

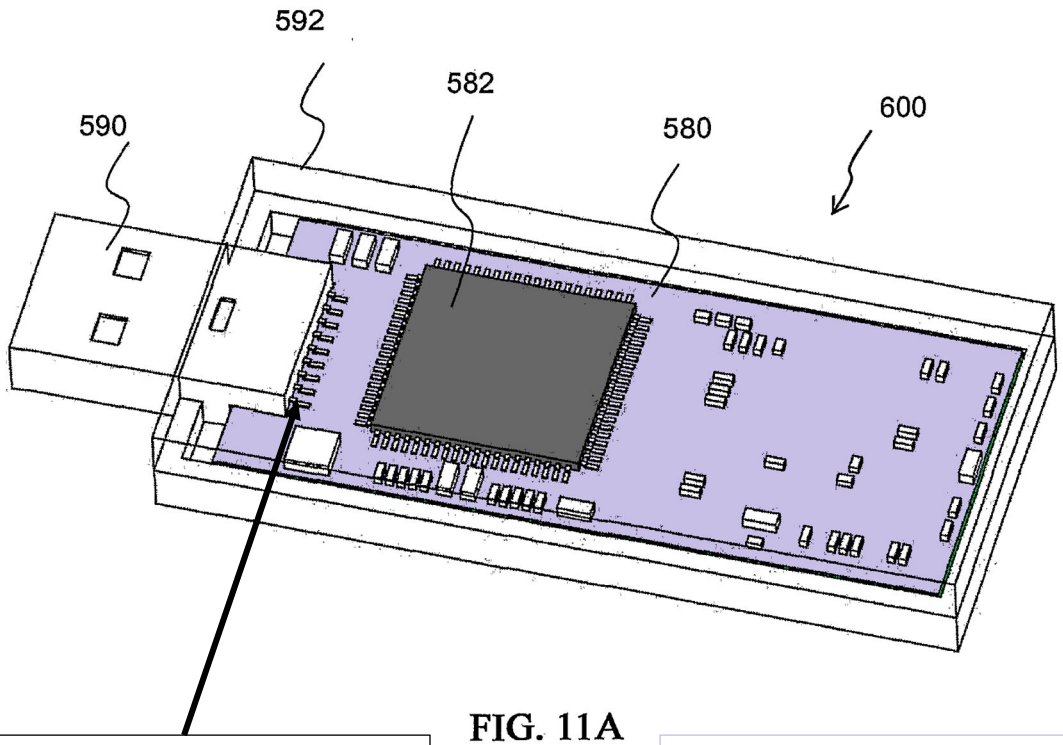


FIG. 11A

It would have been obvious to POSITA that mounting the contact tail portions on the PCB in this manner requires a plurality of coupling points on the PCB. Ex. 1005, ¶¶ 278-282.

3. Claims 4-8 and 13-17

Sections X.C.2 explains that claims 4-8 all depend from claim 1, either directly or indirectly, and claims 13-17 all depend from claim 12, either directly or indirectly. As explained, Chen and Sun combined teach the elements of claims 1 and 12 and render these claims obvious. Claims 4-8 and 13-17 are all directed to

the placement of memory die stacks on the substrate surfaces and the number of memory dies per stack. *See* Appendix A.

Section X.C.2 explains how Sun discloses the memory arrangements of claims 4-8 and 13-17. For the reasons discussed in Section X.C.3 with respect to Hsiao's external storage device, POSITA would have been motivated to combine Chen with Sun to create external storage devices having the memory die stacks arranged as required in claims 4-8 and 14-17.

Claims 4-8 and 14-17 are thus obvious over Chen in view of Sun. *See* Ex. 1005, ¶¶ 283-284.

4. Claim 18

As discussed in Section X.A.9, claim 18 – claiming "an external storage device" –duplicates elements (a)-(g) of claim 1 and adds a clause requiring the is device to be configured to support USB 2.0 and 3.0 standards "in effect as of Jan. 31, 2011." *See* Appendix A, claim 18[h].

Section X.F.1 explains that Chen and Sun combined teach elements (a)-(g) of claim 1. Moreover, Sun teaches an external storage device configured to support USB 2.0 and 3.0 standards. *See* Section X.C.1. It would have been obvious to POSITA to combine Chen and Sun to create external storage devices supporting USB 2.0/3.0 standards. POSITA would have been motivated to do so to meet market demand for a faster device (one that implements USB 3.0's

SuperSpeed protocol) but that retains the USB 2.0 plug's smaller form factor, and POSITA would have had a reasonable expectation of success in doing so.

Chen's memory device **300** has a plug with two sets of contacts supporting two interfaces, one of which (conductive contacts **131-134**) is for USB 2.0 signals. *See* Section X.D.1; Ex. 1010, 5:37-41 ("standard USB" refers to USB 2.0), *id*., 12:5-9 (contacts **131-134** compatible with "standard USB" receptacle).

Contacts **137** include "two pairs of differential plug contacts **138**" for "transferring/receiving high speed signals" (*id.*, 7:17-21), and support a second "non-USB protocol." *Id.*, 12:14-17. POSITA would have understood "non-USB protocol" to refer to a "non-USB **2.0**" protocol because (1) as of Chen's filing date, June 13, 2007, the USB 3.0 Specification had not issued (*see* Ex. 1019, ¶¶ 1-10), (2) Chen discloses that "standard USB" refers to USB 2.0 (Ex. 1010, 5:37-41), and (3) Chen's Abstract states that the "differential contacts are adapted for non-USB 2.0 protocol." *Id.*, Abstract.

Chen teaches that the purpose of his two-tier contact arrangement is to support the USB 2.0 protocol while providing contacts necessary to support another higher speed bus architecture and states "[t]o provide a kind of connector with a small size and a high transmission rate for portability and high data transmitting efficiency is much desirable." Ex. 1010, 3:10-12. POSITA would have been familiar with the USB 3.0 Specification and understood that it provides

a dual-bus architecture operating in parallel—one to support USB 2.0 and one to support USB 3.0 SuperSpeed which is significantly faster than USB 2.0. *See* Section IV.B. POSITA would have also understood Chen's second contacts **137** are exactly those required to support SuperSpeed in Standard-A plugs and Chen's arrangement of contact sets **131-134** and **137** is identical to that specified in the USB 3.0 Specification for supporting the dual-bus architecture.

See Ex. 1005, ¶¶ 285-290.

Accordingly, claim 18 is obvious over Chen in view of Sun.

G. Ground 7: Claim 18 Is Obvious Over Chen and Cheng and Further in View of Wan

Chen in view of Cheng and further in view of Wan teaches the elements of claim 18 and render it obvious. Chen and Cheng combined disclose elements [a]-[g] of claim 18. *See* Section X.D.1. Wan "provide[s] a plug connector that complies with USB 2.0 and 3.0 specifications." Ex. 1011, 1:47-49. Wan's plug connector has the same two-tier contact arrangement disclosed in Chen, and explains that the first contacts **12** "comply with a USB 2.0 specification" and the second contacts **22** "comply with a USB 3.0 specification." Ex. 1011, 2:40-41, 3:38-39, Figs. 2, 4:

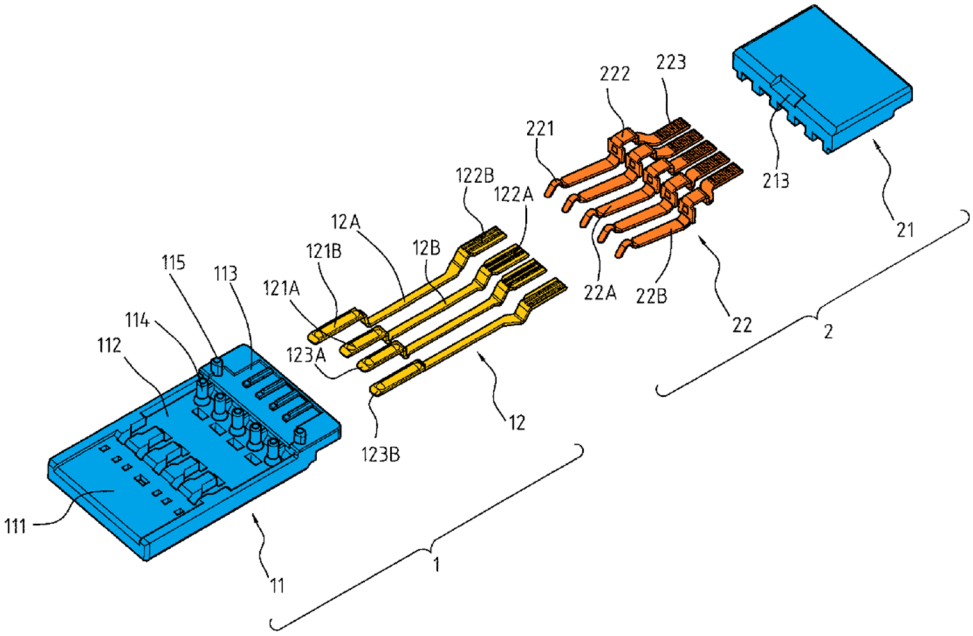

222
223
221
213
21
122B
122A
12A
121B
12B
121A
22A
22B
22
115
113
114
112
123A
2
12
123B
111
11
1

Fig. 2

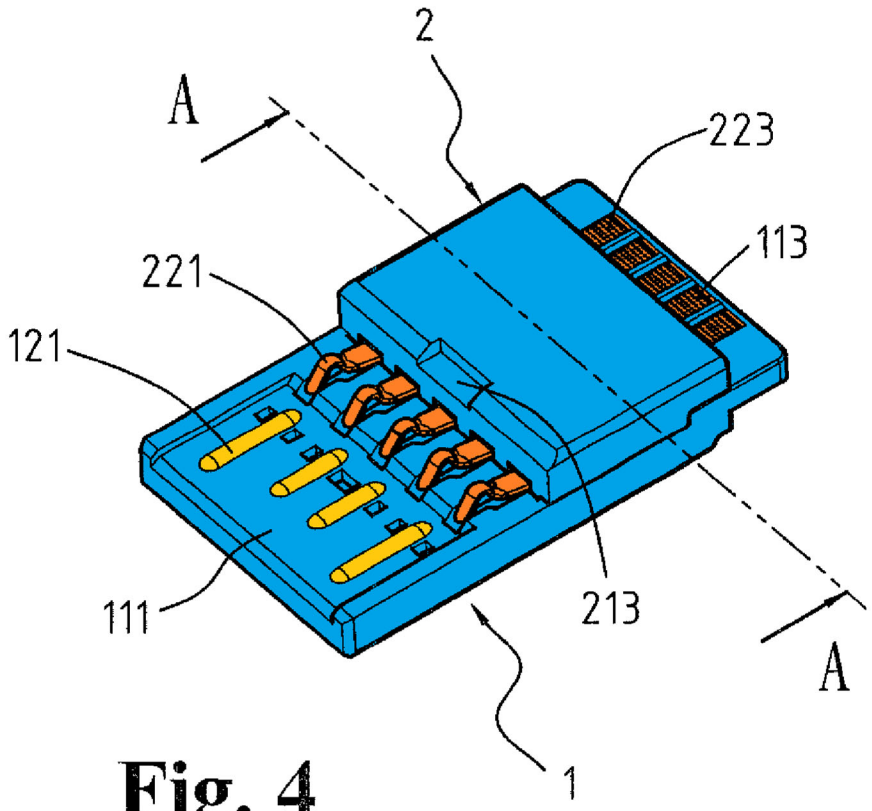

2
A
223
113
221
121
111
213
A
1

Fig. 4

Chen, Chang and Wan combined teach the elements of claim 18 and render it obvious. It would have been obvious to POSITA in view of Wan's disclosure to configure the USB plug of Chen's memory device **300** to support USB 2.0 and 3.0 standards. POSITA would have been motivated to do this and would have a reasonable expectation of success in doing so for the reason discussed in the preceding section X.F.4. Moreover, Wan teaches that a plug configured to support USB 2.0 and 3.0 Specifications "could be used simultaneously to meet consumers' current and emerging demands." Ex. 1011, 1:39-43.

See Ex. 1005, ¶¶ 137-141, 291-293.

XI. CONCLUSION

Petitioners request *Inter Partes* Review of these Challenged Claims pursuant to Grounds 1-7.

XII. PAYMENT OF FEES – 37 C.F.R. § 42.15(a)

The director is authorized to charge the fee specified by 37 C.F.R. § 42.15(a) to Deposit Account No. 502587 for this Petition and further authorizes payment for any additional fees to be charged to this Deposit Account.

DATED this 4th day of August, 2020.

Respectfully submitted,

/s/*Erica D. Wilson*

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Appendix A

U.S. Patent No. 8,705,243 Claim Listing

1. [a] An external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a cover and a plurality of springs, each of the plurality of springs including a portion that is located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers embedded to be exposed upon the cover of the contact bar, wherein the plurality of connection fingers are located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of springs.

2. The external storage device of claim 1, wherein each of the plurality of springs further comprises a projection configured to be located at the first distance in an uncompressed position.

3. The external storage device of claim 2, wherein the projections are configured to extend through a plurality of apertures in the cover in the uncompressed position.

4. The external storage device claim 1, wherein the at least one memory die stack is mounted on the component surface of the substrate.

5. The external storage device of claim 1, wherein the at least one memory die stack is mounted on the connection surface of the substrate.

6. The external storage device of claim 1, further comprising a plurality of memory die stacks, wherein at least one of the plurality of memory die stacks is mounted on the connection surface of the substrate, and at least one of the plurality of memory die stacks is mounted on the component surface of the substrate.

7. The external storage device of claim 6, wherein each of the plurality of memory die stacks comprises a plurality of dies.

8. The external storage device of claim 7, wherein the plurality of dies of at least two of the plurality of memory die stacks are stacked in an overlapping arrangement.

9. The external storage device of claim 1, wherein the first distance comprises a first height above the connection surface, and the second distance comprises a

second height above the connection surface, wherein the second height is less than the first height.

10. The external storage device of claim 1, wherein each of the springs includes a connection pad.

11. The external storage device of claim 10, wherein each of the springs is integrally formed with the corresponding connection pad.

12. [a] A external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of the substrate;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a cover and a plurality of springs, each of the plurality of springs including a portion that is located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers embedded to be exposed upon the cover of the contact bar, wherein the plurality of connection fingers are located at a

second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

[h] a plurality of coupling points mounted on the connection surface of the substrate for electrically coupling with the contact bar;

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of springs.

13. The external storage device of claim 12, wherein the at least one memory die stack is mounted on the component surface of the substrate.

14. The external storage device of claim 12, wherein the at least one memory die stack is mounted on the connection surface of the substrate.

15. The external storage device of claim 12, further comprising a plurality of memory die stacks, wherein at least one of the plurality of memory die stacks is mounted on the connection surface of the substrate, and at least one of the plurality of memory die stacks is mounted on the component surface of the substrate.

16. The external storage device of claim 15, wherein each of the plurality of memory die stacks comprises a plurality of dies.

17. The external storage device of claim 16, wherein the plurality of dies of at least two of the plurality of memory die stacks are stacked in an overlapping arrangement.

18. [a] An external storage device comprising:

[b] a substrate that includes a connection surface and a component surface, the connection surface opposite the component surface;

[c] at least one memory die stack mounted on one of the connection surface and the component surface of;

[d] a controller configured to access the at least one memory die stack, the controller mounted on one of the connection surface and the component surface of the substrate;

[e] a contact bar mounted on the connection surface of the substrate, the contact bar comprising a cover and a plurality of springs, each of the plurality of springs including a portion that is located at a first distance relative to the connection surface of the substrate;

[f] a plurality of connection fingers embedded to be exposed upon the cover of the contact bar, wherein the plurality of connection fingers are located at a second distance relative to the connection surface of the substrate, the second distance being less than the first distance; and

[g] wherein a first interface comprises the plurality of connection fingers, and a second interface comprises the plurality of springs; and

[h] wherein the external storage device is configured to support Universal Serial Bus “USB”) 2.0 and USB 3.0 standards in effect as of Jan. 31, 2011.

APPENDIX B

EXHIBIT LIST

Exhibit #	Reference Name
1001	U.S. Patent 8,705,243 (“the ’243”)
1002	Provisional Application No. 61/438,139
1003	Provisional Application No. 61/442,379
1004	’243 Prosecution History (as downloaded from USPTO Pair)
1005	Declaration of R. Jacob Baker, Ph.D., P.E.
1006	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
1007	USB 2.0 Specification
1008	USB 3.0 Specification
1009	U.S. Patent 8,480,435 (“Hsiao”)
1010	U.S. Patent 7,625,243 (“Chen”)
1011	U.S. Patent 7,563,140 (“Wan”)
1012	U.S. Patent Application Publication 2009/0098773 (“Cheng”)
1013	U.S. Patent Application Publication 2008/0150111 (“Hiller”)
1014	World Intellectual Property Organization Publication WO 2011/160321 (“Sun”) (also published as US Patent Application Publication 2012/0203954).

1015	Techspot Article
1016	Exhibits C and D to Patent Owner's Complaint filed in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA (W.D.Tex.)
1017	U.S. Patent Application Publication 2008/0093720 ("Hiew")
1018	U.S. Patent Application Publication 2005/0070138 ("Chiou")
1019	Declaration of Jeffrey L. Ravencraft
1020	Supp. Order re Court Operations During COVID-19 Pandemic (W.D.Tex. Jul. 2, 2020)
1021	USPTO update on in-person meetings available at https://www.uspto.gov/about-us/news-updates/uspto-update-person-meetings (last downloaded 7/25/2020)
1022	Patent Owner's Complaint (without Exhibits) filed in *Kuster v. Western Digital Technologies, Inc.*, Case No. 6:20-cv-00563 ADA (W.D.Tex.)

CERTIFICATION OF WORD COUNT UNDER 37 C.F.R. § 42.24(d

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition For *Inter Partes* Review Of U.S. Patent No. 8,705,243 totals 13,952 excluding the table of contents, table of authorities, mandatory notices under § 42.8, Appendix A (claim listing) and Appendix B (exhibit list), Certificate of Service and this word count certification.

This word count was made by using the built-in word count function tool in the Microsoft Word software used to prepare the document.

DATED this 4th day of August, 2020.

Respectfully submitted,

/s/ *Erica D. Wilson*

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. §§ 42.6 and 42.105, that a complete copy of the attached PETITION FOR INTER PARTES REVIEW OF U.S. PATENT NO. 8,705,243, including all Exhibits and related documents, was served on August 4, 2020 via overnight carrier upon the Patent Owner by serving the correspondence address of record with the USPTO as follows:

Kilpatrick Townsend & Stockton LLP
Mailstop: IP Docketing – 22
1100 Peachtree Street
Suite 2800
Atlanta, Georgia 30309

and is being served via overnight carrier and email on August 4, 2020 upon lead counsel of record for the Patent Owner in the litigation pending before the U.S. District Court for the Western District of Texas (Waco) entitled *Kuster v. Western Digital Technologies, Inc.,* 6:20-cv-00563 ADA as follows:

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DATED this 4th day of August, 2020.

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