UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TCT MOBILE (US), INC.; TCT MOBILE (US) HOLDINGS, INC.; HUIZHOU TCL MOBILE COMMUNICATION CO. LTD.; AND TCL COMMUNICATION, INC.,
Petitioners

v.

FUNDAMENTAL INNOVATION SYSTEMS INTERNATIONAL LLC,
Patent Owner

U.S. Patent No. 8,624,550
Issue Date: January 7, 2014
Title: MULTIFUNCTIONAL CHARGER SYSTEM AND METHOD

Case No. IPR2021-_____

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,624,550 CHALLENGING CLAIMS 1-18 UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104

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1002	U.S. Patent File History of the '550 Patent Excerpts (the "'550 File History")
1003	Declaration of Dr. Jacob Baker regarding U.S. Patent No. 8,624,550 ("Baker")
1004	*Curriculum Vitae* of Dr. Jacob Baker
1005	Amended Complaint, *Fundamental Innovation Systems Int'l LLC v. TCT Mobile (US) Inc. et al.*, No. 1:20-cv-00552-CFC (D. Del. Sep. 11, 2020) ("Complaint")
1006	U.S. Patent No. 7,360,004 ("Dougherty")
1007	Japanese Patent Application No. 2000-165513A ("Morita")
1008	U.S. Provisional Application No. 60/273,021
1009	U.S. Provisional Application No. 60/330,486
1010	Universal Serial Bus Specification, Revision 1.1, September 23, 1998 ("USB 1.1")
1011	Universal Serial Bus Specification, Revision 2.0, April 27, 2000 ("USB 2.0")
1012	U.S. Patent No. 6,531,845 ("Kerai")
1013	U.S. Patent No. 6,625,738 ("Shiga")
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1015	U.S. Patent No. 6,625,790 ("Casebolt")
1016	Cypress CY7C63722/23 CY7C63742/43 enCoRe™ USB Combination Low-Speed USB & PS/2 Peripheral Controller, by Cypress Semiconductor Corporation, published May 25, 2000 ("Cypress")
1017	U.S. Patent No. 5,923,146 ("Martensson")

I. INTRODUCTION

TCT Mobile (US), Inc.; TCT Mobile (US) Holdings, Inc.; Huizhou TCL Mobile Communication Co. Ltd.; and TCL Communication, Inc. ("Petitioners") petition for *inter partes* review of claims 1-18 (the "Challenged Claims") of U.S. Patent No. 8,624,550 (the "'550 Patent") on the grounds that they are unpatentable under 35 U.S.C. §103.

The Challenged Claims relate to an adapter that uses an industry standard Universal Serial Bus ("USB") port to charge a device. Providing power through USB ports was well understood and routine by the priority date of the '550 Patent, but the Challenged Claims purport to "invent" an adapter that provides current "without regard" to the power/current limits in the USB specification(s). In other words, the Challenged Claims cover little more than a charger/adapter that uses a USB interface but does not follow one or more of the requirements of the USB specification. Independent claims (1 & 10), for example, require an "adapter" that supplies current "without regard" to an associated "condition" or "limit" imposed by the USB Specification. Certain dependent claims (2, 9, 11, 18) clarify that the disregarded "condition" or "limit" is the USB Specification's requirement that no more than 500mA of current be supplied to any single device.

The USB specification itself, however, notes that certain devices will disregard this condition/limit in certain situations. Accordingly, this "invention"

would have been known and obvious to a POSITA as of the priority date of the '550 Patent. Specifically, the USB specification indicates that "high powered" ports will provide a *minimum* of 500 mA of current to downstream devices. Accordingly, those high powered ports—which were known and used in the art as of the priority date of the '550 Patent—are themselves invalidating prior art because they are configured to supply current without regard to the 500 mA limit when, for example, connected to a single downstream device (e.g., when used as a phone charger). Indeed, the provisional application to which the '550 Patent claims priority admits that such devices were known and available. Ex. 1008 ('021 Application) (discussing prior art "high powered" hubs configured to supply around 700mA-800mA of current).

The prior art cited in this petition has not been fully considered by the patent office. The Morita patent has not been considered by the examiner or the PTAB in any proceedings and it renders all 18 claims obvious. Specifically, Morita discloses a charging device that plugs directly into a power outlet, contains a high-powered port, and charges a single device (a phone) in a charging mode that does not involve communicating over the USB data lines. In that mode, a POSITA would have understood that the device provides more than 500mA of current to the phone and, accordingly, supplies current without regard to the corresponding USB limit.

The Dougherty reference discloses a docking station that supplies 2,500 mA of current—far exceeding the corresponding 500 mA limit—to a laptop device. The PTAB considered certain arguments related to Dougherty in prior proceedings, but found that the prior petitions pointed to an *external* "communication path" instead of an *internal* "communication path" (which the PTAB found to be required by the Challenged Claims). The PTAB noted, however, "[i]t is possible, if not highly probable," that the docking station of Dougherty includes the required "communication path" and, thus, essentially invited further arguments regarding Dougherty's internal "communication path." As explained herein, Dougherty in view of the USB 1.1 Specification discloses that the docking station of Dougherty does indeed have such an internal communication path

Because there is a reasonable likelihood that Petitioners will prevail with respect to these claims, Petitioners respectfully request that the Board institute *inter partes* review.

II. SUMMARY OF CHALLENGE 37 C.F.R. §42.104(B)

Petitioners requests that the Board review and cancel claims 1-18 of the '550 Patent based on the following grounds.

Ground	Claims	Basis	References
1	1-18	Pre-AIA 35 U.S.C. § 103(a)	Morita in view of the knowledge of a POSITA.

2	1-2, 10-11, 18	Pre-AIA 35 U.S.C. § 103(a)	Dougherty in view of the USB 1.1 Specification.

III. INSTITUTION SHOULD BE GRANTED; DISCRETIONARY DENIAL IS NOT APPROPRIATE

The Board should not exercise its discretion to deny institution under 35 U.S.C. §§ 314(a) or 325(d). If the Board considers exercising its discretion to deny institution, Petitioner respectfully requests leave to file a reply to address any discretionary denial arguments Patent Owner makes in its preliminary response.

A. The *Apple/Fintiv* Factors Support Institution.

There is a parallel district court proceeding involving the '550 Patent in the District of Delaware. Ex. 1005. The complaint was filed on April 23, 2020. However, the *Apple/Fintiv* factors support institution despite the existence of the Delaware litigation. *Apple Inc. v. Fintiv, Inc.,* IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020).

First, potential for a district court stay, is neutral or weighs in favor of institution. Neither party has requested a stay,[1] so at worst this factor is neutral because the Board "will not attempt to predict" how the district court will proceed. *Sand Revolution II, LLC v. Continental Intermodal Group5 Trucking LLC,* IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative). Congress, however,

[1] Petitioner does intend to move for a stay of the Delaware case.

intended for district courts to be liberal in granting stays pending PTAB proceedings, especially in cases where petitioners moved quickly after service of a complaint. 157 Cong. Rec. S1363 (Mar. 8, 2011) (Sen. Schumer) (Congress placed "a very heavy thumb on the scale in favor of a stay being granted"). Given that Petitioners have moved expeditiously (*see* factor 2 discussion below), this factor favors institution. Furthermore, Judge Connolly has consistently granted stays in similar patent litigation cases, especially those where the petitions are instituted. *See, e.g., Allergen USA, INC. v. Prollenium US Inc.,* 1-20-cv-00104, Dkt. No. 34 (July 16, 2020); *Uniloc 2017 LLC v. Vudu, Inc.*, 1-19-cv-00183, Dkt. No. 72 (March 26, 2020).

Second, the proximity of the trial date to the final written decision, weighs in favor of institution. The Court has scheduled a *Markman* hearing for June 23, 2021. PTAB will likely issue an institution decision before the Court issues a final *Markman* decision. Judge Connolly consistently grants stays when the PTAB institutes trial in such instances. *See id*. And, even in the unlikely case that Judge Connolly does not grant a stay, the trial date is scheduled for October 17, 2022. This is several months after the PTAB's expected final written decision based on this Petition's filing date of January 12, 2021, which would tentatively calendar an institution date of approximately July 12, 2021 and final written decision date of approximately early July, 2022 (depending on the accorded filing date).

Third, investment in the parallel proceeding, weighs in favor of institution. Discovery will still be in the early stages, with the deadline not until December 17, 2021. It is unlikely that any fact depositions will have taken place before the institution decision. Further, as stated above, it is unlikely that the district court will have issued a *Markman* ruling by the time of the institution decision, and little to no Court resources will have been devoted to analyzing prior art invalidity issues. Again, the parallel district court litigation is likely to be stayed once the present Petition is instituted.

Furthermore, as part of a holistic analysis, the Board considers the speed with which the petitioner acted. *Apple Inc. v. Seven Networks, LLC,* IPR2020-00156, Paper 10 at 11–12 (PTAB June 15, 2020). In cases where the petitioner acted diligently and without meaningful delay, as here, any investment of the parties in the parallel district court litigation is mitigated. *HP Inc. v. Neodron LTD,* IPR2020-00459, Paper 17 at 40 (PTAB Sept. 14, 2020). Here, Petitioners filed this Petition within about four months of the Answer date, and roughly two months after Patent Owner served preliminary infringement contentions. Such diligence favors institution.

Fourth, overlap of issues, weighs in favor of institution. The Petition challenges claims that are not asserted in the district court action. And while the petition also challenges the same claims as the parallel district court proceeding,

there is a high likelihood that Judge Connolly grants a stay upon institution. In the unlikely instance where a stay is not granted, a final written decision will still issue before the beginning of trial. The final written decision, once issued, will trigger estoppel for in the district court litigation for grounds that were raised or reasonably could have been raised. *See* 35 U.S.C. §315(e)(2).

Fifth, whether the parties are the same, weighs in favor of institution. The parties with respect to this Petition are the same as those engaged in the parallel district court case.

Finally, other circumstances strongly favor institution. Petitioners advance a targeted Petition with two grounds: the first ground has never been submitted to the Board, and the second ground is one which the Board considered and noted it is "highly probable" to have certain required elements (which it does, *see* Section III.C, *infra*). The strength of the present Petition strongly weighs in favor of institution. The '550 Patent has been asserted against several large electronics companies such as Coolpad, Lenovo, and Petitioners, which litigation remains pending. Patent Owners assert that USB adapters, which are ubiquitous, and the mobile devices they charge infringe the '550 Patent and related patents. Given the substantial impact that the '550 Patent and related patents could have on the mobile device industry, it is in the public interest to address invalidity, especially under new prior art never before submitted to the Board. And as the Supreme Court recently explained, there

is a significant public interest against "leaving bad patents enforceable." *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

B. The General Plastics Factors Support Institution

The *General Plastics* factors support institution despite earlier IPRs being filed by other, unrelated entities. *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (P.T.A.B. Sept. 6, 2017); *see also* Section X.B (Related Matters). First, the current Petitioner (and the real parties-in-interest) are different from the prior petitioners; and there is no relation between them. *Id.* Second, because the current Petitioner had not been sued or provided notice of alleged infringement when the earlier petitions were filed, the current Petitioner did not know of the prior art in this Petition when the earlier petitions were filed (nor did it have any reason to search for the prior art). *Id.* Third, while the preliminary responses and decisions from the earlier IPRs did issue before the filing of the current Petition, this timing is the result of Patent Owner not suing the current Petitioner until after said issuance and is thus not the result of current Petitioner's delay. *Id.*; *Microsoft Corp. v. Uniloc 2017, LLC*, IPR 2019-01252, Paper 7 at 8-9 (PTAB Dec. 20, 2019). Fourth, Petitioner was diligent in filing the current petition as well as promptly moving to file petitions on the other asserted patents after receiving Patent Owner's selection of claims. Section X.B; *LG Electronics, Inc. v.*

Bell Northern Research, LLC, IPR 2020-00319, Paper 15 at 13 (PTAB June 23, 2020).

C. The Factors Under 35 U.S.C. § 325(d) Support Institution

The factors under 35 U.S.C. § 325(d) also support institution.

The primary reference cited herein (Morita), which is the basis for Ground 1, is a USB mobile device charger that was not considered by the patent examiner or by the PTAB during any of the prior IPR proceedings. Accordingly, this petition presents and relies principally on evidence and argument not yet considered by the examiner or the Board.

In certain earlier proceedings, the PTAB did consider the Dougherty reference cited herein. The PTAB found, however, that the claims of the '550 Patent require a "communications path" that is internal to the claimed "adapter" and that petitioners cited only a communications path that was external to the "adapter" of Dougherty. *See ZTE (USA) Inc. et al. v. Fundamental Innovation System International LLC*, IPR2018-00110 at Paper 12 (Decision Denying Institution of *Inter Partes* Review) at 9-12. Because the petitioners presented no evidence or argument regarding the internal communications path of Dougherty, the PTAB denied institution. *Id.* at 11-12.

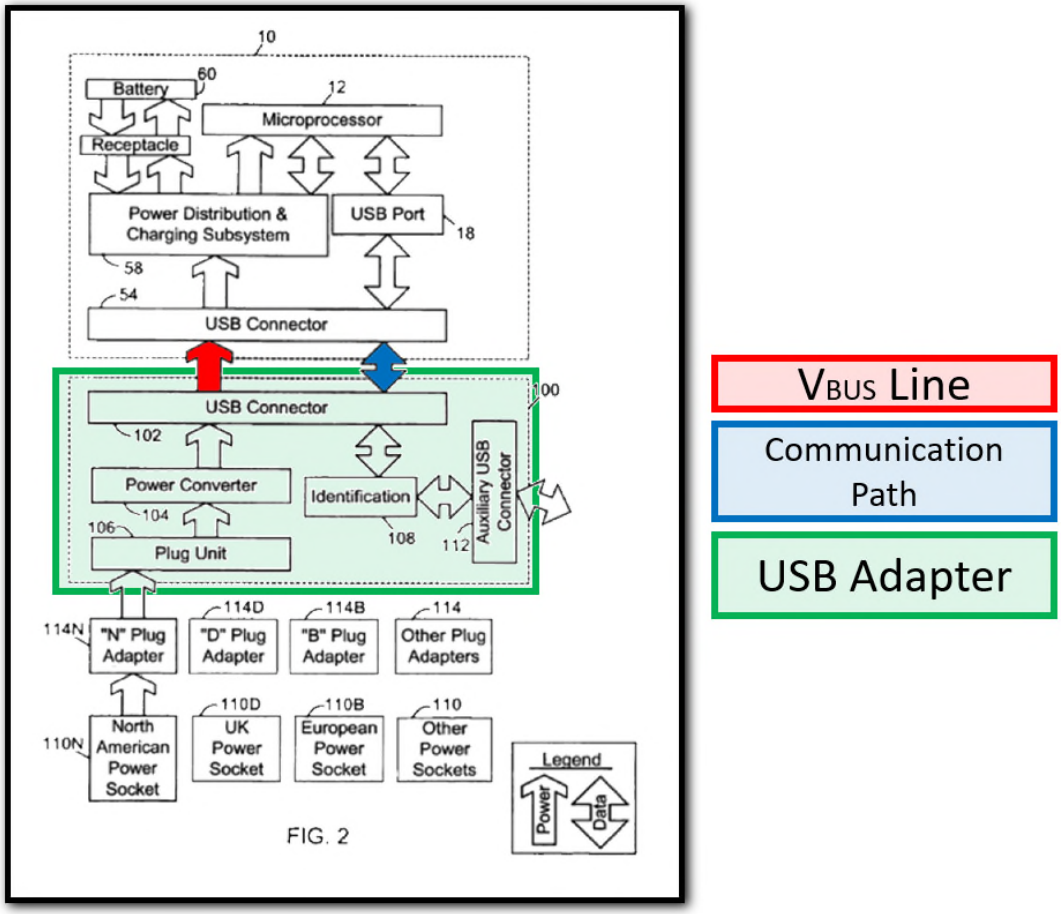
The PTAB noted, however, that it is likely the adapter of "Dougherty" comprises the necessary communication path. *Id.* at 12 ("It is possible, if not highly

probable, that docking station 200 contains an internal USB communication path that is utilized for these purposes.") Accordingly, the PTAB essentially invited an explanation as to how Dougherty satisfies the challenged claims as construed in that decision. *Id.* Petitioner provides the corresponding argument and evidence here.

IV. OVERVIEW OF THE '550 PATENT

A. Disclosure of the '550 Patent

The '550 Patent discloses "a USB adapter" that provides power to a connected device "through a USB port." Ex. 1001 ('550 Patent) at 2:34-36. The USB adapter comprises a "USB V_{BUS} line" and a "USB Communication Path." *Id.* at Claims 1 and 10. Figure 2, reproduced below, is a schematic diagram of the disclosed USB adapted coupled to an exemplary mobile device. *Id.*, 3:23-24.



Both the "V_{BUS} line" and the "communication path" were well known and understood components of USB devices. They are expressly accounted for in USB specifications which a POSITA would have been familiar with:

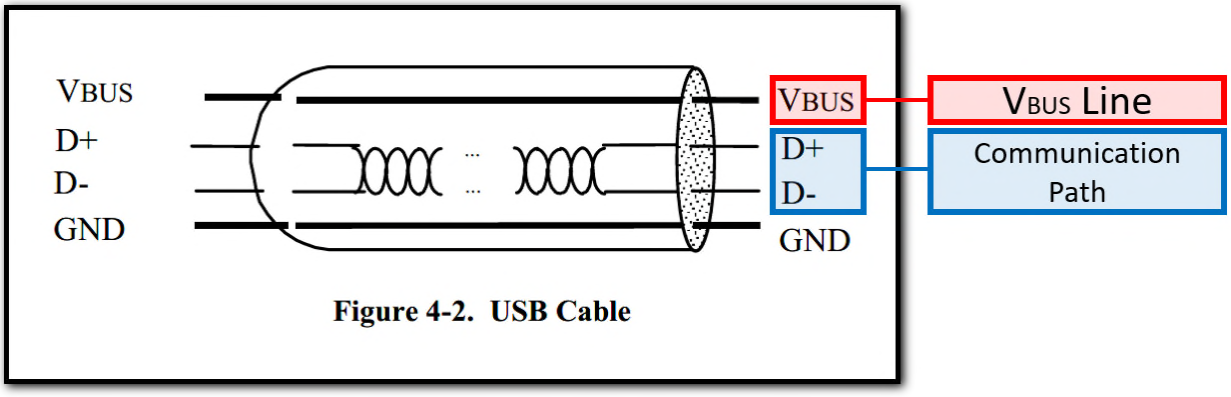


Figure 4-2. USB Cable

See e.g., Ex. 1010 (USB 1.1) at 17 and Figure 4-2 (annotated).

The challenged claims also require that the "adapter" be "configured to" supply current on the V_{BUS} line "without regard" to a "condition" or "limit" stated in a USB Specification. Ex. 1001 ('550 Patent) at Claims 1, 10. As discussed in more detail herein, this may involve, for example, being configured to supply current in excess of an amount specified by a USB specification (e.g., the 500mA that may be supplied to a particular device) (Claims 2, 9, 11, 18). *See* Section VII (Claim Construction).

Certain of the challenged claims also require that the adapter be configured to supply current "without USB enumeration" (Claims 3 and 12) or in response to an "abnormal data condition" (Claims 4 and 13) such as a logic high signal on the D+ and D- lines of the communication path (Claims 6-7 and 15-16). As discussed in more detail herein, USB "enumeration" is the communication engaged in by USB devices when connected in order to configure them. *See* USB 1.1 at 179; Baker, ¶ 74. The '550 Patent discloses that an adapter can supply current without engaging in the enumeration process using "an abnormal data line condition at the USB port 18." *Id.* at 9:21-24. Specifically, the '550 patent discloses that a device that detects "voltages on both the D+ and D- lines of the USB connector [that] are greater than 2 Volts (step 220), [will] determine[] that the device connected to the USB connector 54 is not a typical USB host or hub and that a USB adapter 100 has been detected."

Id., 9:39-44. In such a scenario, the mobile device can charge the battery or otherwise use the power from the USB connector, without waiting for enumeration. *Id.* at 9:44-47.

B. Priority Applications of the '550 Patent

The '550 patent claims priority through a series of continuations to two provisional applications: (1) U.S. Provisional Application 60/273,021 (the "'021 Application") (Ex. 1008), filed March 1, 2001; and (2) U.S. Provisional Application No. 60/330,486 (the "'486 Application") (Ex. 1009), filed October 23, 2001.

1. The '021 Application

The '021 Application was filed on March 1, 2001. Ex. 1008. The application does not disclose, describe, or purport to invent any novel adapter or charger. To the contrary, the specification discloses "a charging circuit" that is part of a mobile device and that can use current *received from* the mobile device's USB connection to charge the device's battery. *Id.* at 18 (". . . this invention relates to adapting power from the USB for use as a power source by the charging system of the mobile device . . . ."); *id.* at 20 ("It is an object of the invention . . . to use the power traditionally available on the USB as an alternate power source for recharging the portable power supply of the mobile device.") (emphasis added); *id.* at 20 (describing embodiments of "charging circuit" in mobile device).

The ’021 Application also noticeably omits any discussion of using an “abnormal data condition” on the USB communication path (claims 4 and 13), that comprises a “logic high signal on each of said D+ and D- lines” (claims 7 and 16), wherein “each said logic high signal is greater than 2V” (claims 8 and 17). *Id.* at 20-30 (discussing various embodiments).

Although the ’021 Specification does not purport to invent a USB device that supplies current “without regard” to the USB Specifications, it does make clear that such devices existed at the time. Specifically, the application discloses that the patentee tested *existing* USB hubs to see how much current they would supply. *Id.* at 22-33 (“It was determined experimentally that current can be drawn from several USB ports at a high rate”). The patentee noted that the tested “high powered” hubs were configured to provide up to 700mA-800mA of current before automatically shutting off the power. *Id.* at 22 (“Furthermore, it seems that certain high-power USB ports, such as a self-powered hub, appear to implement only an over-current protection, i.e., they turn off the voltage on the VBUS line for current valued exceeding 700mA-800mA.”).

2. The ’486 Application

The ’486 Application was filed on October 23, 2001. Ex. 1009 (’486 Application). The application, for the first time, discussed “a USB power adapter that can provide power to charge a USB chargeable device via the device USB

interface." *Id.* at 14. The application also discusses, again for the first time, the use of "abnormal data line conditions" including a signal in which D+ and D- are held high. *Id.* at 24-25.

3. Priority Date

Because the '021 Application does not describe various elements of the Challenge Claims, those claims are entitled to the October 23, 2001 priority date of the '486 Application at the earliest. The priority date, however, will not affect the arguments herein as each of the references cited constitutes prior art under either priority date.

C. Prosecution History of the '550 Patent

The '550 Patent issued from U.S. Patent Application No. 13/536,767, which was filed on June 28, 2012. On the filing date, the Applicant cancelled all pending claims and added 18 new claims. Ex. 1002 ('550 Patent File History Excerpts) at 1-65. On May 28, 2013, the Examiner rejected all pending claims based upon obviousness-type double patenting over claims 1-12 of U.S. Patent No. 7,986,127. *Id.* at 147-150. The original Patent Owner subsequently filed a terminal disclaimer (*id.* at 162), and the Examiner issued a notice of allowance without further rejections. *Id.* at 169.

V. PERSON OF ORDINARY SKILL IN THE ART

The PTAB held in the context of the '550 Patent that a POSITA "would have had a bachelor's degree in electrical engineering and 3-5 years of experience in circuit or device design, or equivalents thereof." *ZTE (USA) Inc. et al. v. Fundamental Innovation System International LLC*, IPR2018-00111 at Paper 62 at 14. At a minimum, such a person would have been aware of and familiar with the USB Specifications that existed as of the priority date of the '550 Patent, including the USB 1.1 and USB 2.0 Specifications discussed herein. Baker, ¶¶ 68. For purposes of this petition, petitioner adopts this description of the hypothetical person of ordinary skill in the art ("POSITA") of the subject matter of the '550 Patent.

VI. SUMMARY OF THE PRIOR ART

A. USB 1.1 Specification

The Universal Serial Bus Specification, Revision 1.1, ("USB 1.1") was published by the USB Implementers Forum, Inc. on September 23, 1998. Ex. 1010. It is prior art to the '550 Patent under at least 35 U.S.C. § 102(a) and (b). Moreover, the USB 2.0 Specification would have been part of the knowledge of a POSITA as of the priority date of the '550 Patent. Baker, ¶ 69.

Figure 4-1, below, shows the bus topology for a USB system. Generally, each such system requires a "host" with a "root hub" for purposes of communication. USB 1.1 at 16; Baker, ¶ 70. Without such a hub, there will be no communication

among the devices. For example, connecting, Hub 1 to a node (a node is a connected device, also called a "function") or Hub 2 without connecting Hub 1 to the Host via the Root Hub will not result in a functioning/communicating, USB system. *Id.*

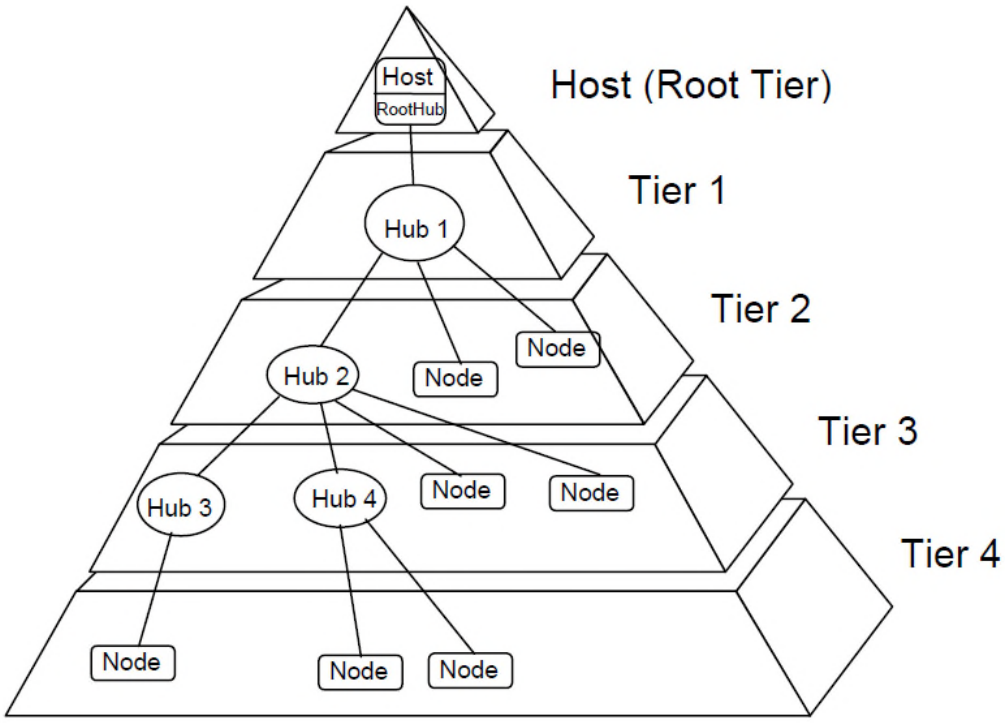


Figure 4-1. Bus Topology

USB 1.1 at 16 (annotated).

Generally, USB 1.1 instructs that a USB device (*i.e.*, node or function) is plugged into a port on a hub using a cable. USB 1.1 at 23. The cable is connected between a USB connector on a USB device and a USB connector on a host or hub. Baker, ¶ 71.

Figure 4-4 illustrates how hubs provide connectivity in a typical computer environment.

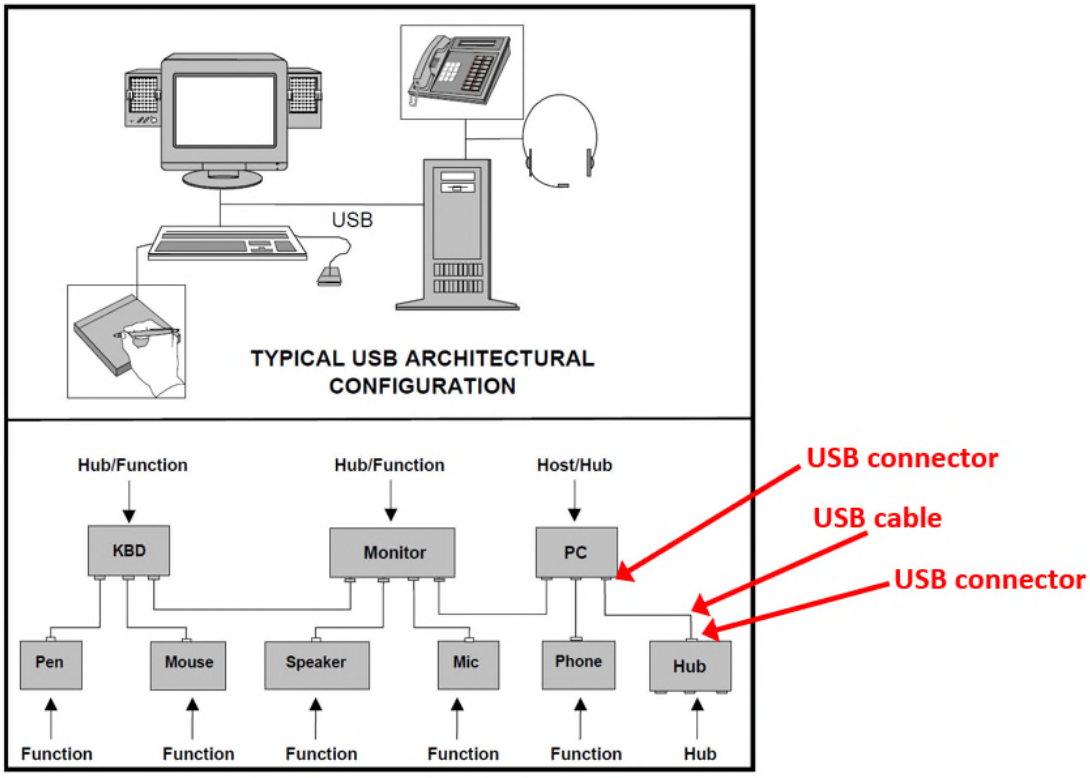


Figure 4-4. Hubs in a Desktop Computer Environment

USB 1.1 at 23 (annotated).

USB 1.1 teaches a POSITA how to implement a USB plug and that a USB connector includes four contacts: V_{BUS}, D+, D-, and GND:

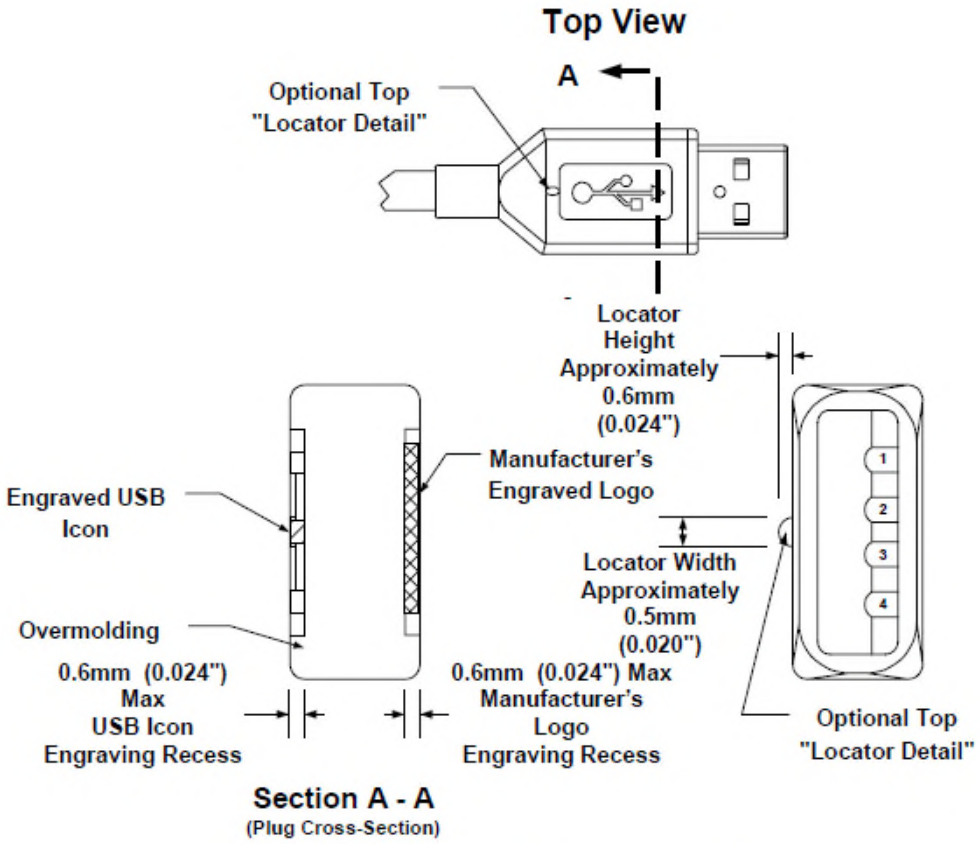


Figure 6-6. Typical USB Plug Orientation

Table 6-1. USB Connector Termination Assignment

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
Shell	Shield	Drain Wire

USB 1.1 at 81 and 82; Baker, ¶¶ 72-73.

The USB 1.1 Specification indicates that that the host is responsible for providing power to an attached USB device. USB 1.1 at 24 ("The host is responsible for . . . [p]roviding power to the attached USB devices.") The USB Specification also sets forth conditions and limits for the supply of power on the V_{BUS} line. Baker, ¶¶ 73-74. The Specification does so in terms of milliamps (mA) of current and in terms of "unit loads." USB 1.1 at 134. "A unit load is defined to be 100mA" of current. *Id.* Notably, the USB Specification includes the following current conditions/limitations:

- A "high-power" hub port supplies a minimum of 500mA
- A "low-power" device is supplied with a maximum of 100mA of current
- A "high-power" device is supplied with a maximum of 500 mA of current

These conditions/limitations, as well as others, are listed in table 7-5 of the USB 1.1 Specification:

Table 7-5. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage:					
High-power Port	VBUS	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	VBUS	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current:					
High-power Hub Port (out)	ICCPRT	Section 7.2.1	500		mA
Low-power Hub Port (out)	ICCUPT	Section 7.2.1	100		mA
High-power Function (in)	ICCHPF	Section 7.2.1		500	mA
Low-power Function (in)	ICCLPF	Section 7.2.1		100	mA
Unconfigured Function/Hub (in)	ICCINIT	Section 7.2.1.4		100	mA
Suspended High-power Device	ICCSH	Section 7.2.3 ; Note 15		2.5	mA
Suspended Low-power Device	ICCSL	Section 7.2.3		500	µA

USB 1.1 at 142 (annotated).

The USB Specification defines a "high power" port as one that obtains its power externally (e.g., from an outlet). *Id.* at 134 ("Systems that obtain operating power externally, either AC or DC must supply at least five unit loads to each port. Such ports are called high-power ports.") In other words, the USB specification, on its own, acknowledges that certain USB ports (high-powered ports) will supply current in excess of the 500mA limit supplied to a particular USB device (e.g., when the high-power hub port is (1) connected to its own external power sources and (2) connected to a single USB device). *Id.*; Baker, ¶ 74.

USB 1.1 discloses that an attached device can operate at "full-speed" or "low-speed." USB 1.1 discloses "The speed of an attached device is determined by the placement of a pull-up resistor on the device (see Section 7.1.5)." USB 1.1 at 251.

The specific nature of how D+ and D- are connected is discussed in detail below and in USB 1.1. *See* Baker, ¶¶ 77-83. "Hubs, and the devices to which they connect, use a combination of pull-up and pull-down resistors to control D+ and D- in the absence of their being actively driven. These resistors establish voltage levels used to signal connect and disconnect and maintain the data lines at their idle values when not being actively driven." USB 1.1 at 256.

USB 1.1 discloses "Full-speed devices are terminated as shown in Figure 7-10 with the pull-up resistor on the D+ line." and "Low-speed devices are terminated as shown in Figure 7-11 with the pull-up resistor on the D- line." USB 1.1 at 113. These figures are annotated below to show that a pull-up resistor, labeled R_{pu}, on the D+ line indicates a "full-speed device" while a pull-up resistor, also labeled R_{pu}, on the D- line indicates a "low-speed device." Baker, ¶ 78.

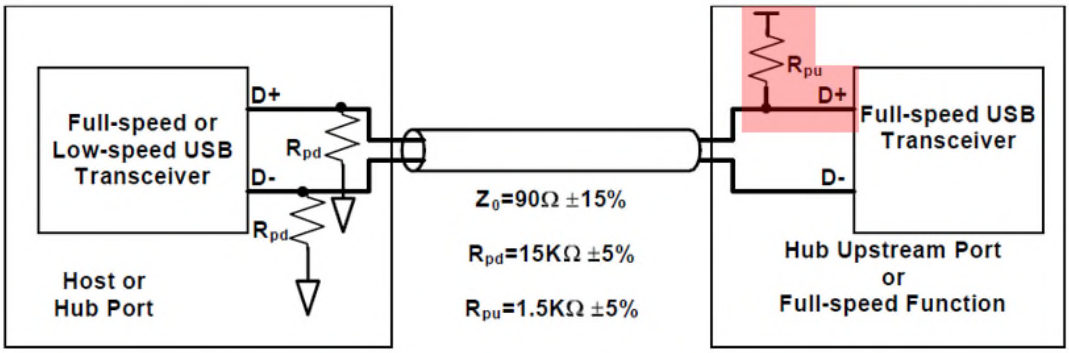


Figure 7-10. Full-speed Device Cable and Resistor Connections

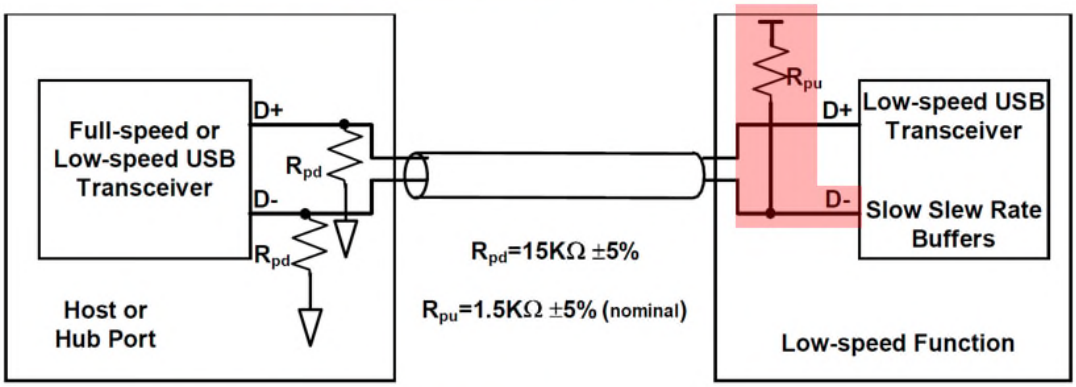


Figure 7-11. Low-speed Device Cable and Resistor Connections

USB 1.1 at 113 and 114 (annotated).

USB 1.1 also discloses that in the host or hub port "The pull-down terminators on downstream ports are resistors of 15kΩ+/-5% connected to ground." USB 1.1 at 113. These resistors are annotated below and labeled R_{pd}.

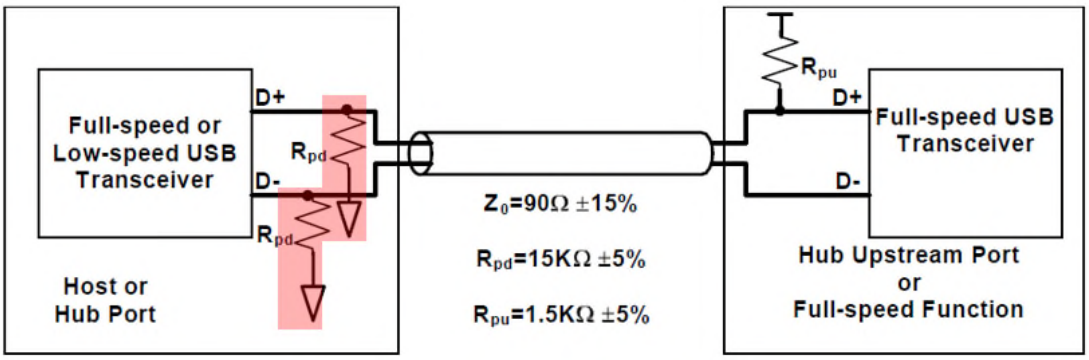


Figure 7-10. Full-speed Device Cable and Resistor Connections

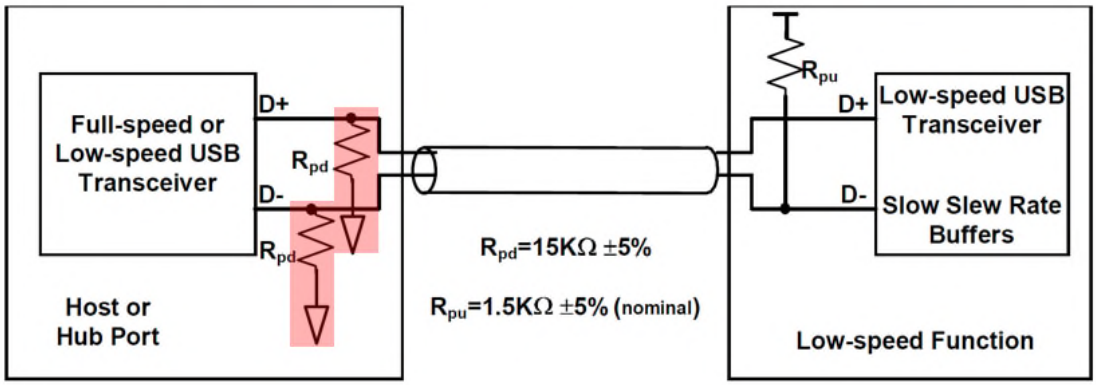


Figure 7-11. Low-speed Device Cable and Resistor Connections

USB 1.1 at 113 and 114 (annotated); Baker, ¶ 79.

When no pull-up resistor, R_{pu}, is present on D+ and/or D- the corresponding line is pulled to ground through R_{pd}. Baker, ¶ 80. If both D+ and D- are at ground then no device is connected to the USB host or hub port. If D+ is pulled high and D- is at ground the connected device operates in full-speed. *Id.* If D+ is at ground and D- is pulled high the connected device operates in low-speed. If D+ and D- are to be used for communications by either full- or low-speed devices then their voltages should never intentionally be pulled high (above 0.8V) at the same time. *Id.* A

summary of the relationship between the D+ and D- levels on a USB connector and the port configurations discussed in this section is shown below:

D+	D-	Port configuration
Low	Low	No device connected
High	Low	Full-speed
Low	High	Low-speed
High	High	Abnormal condition

Baker, ¶ 83. As discussed in more detail below, the High/High signal on the data lines is also referred to in the art as an "SE1" signal. *See* Section VI.C; Baker, ¶ 80. A POSITA would have been aware of the effects of the SE1 signal on the data lines as disclosed by the USB 1.1 Specification. Baker, ¶¶ 80-84. Specifically, a POSITA would have understood that a device receiving this signal would terminate data communications and standby while receiving power across the V_{BUS} line. *Id.*

For example, USB 1.1 states "Note: if both D+ and D- are high at this time, the hub may stay in the Disabled state and set the C_PORT_ENABLE bit to indicate that the hub could not determine the speed of the device." USB 1.1 at 252. Accordingly, a POSITA would have understood that this signal indicates that the speed of a connected device cannot be determined and thus communications between the host or hub and the connected device are not possible. Baker, ¶ 81.

Moreover, The USB 1.1 further states "After the device has been powered, it must not respond to any bus transactions until it has received a reset from the bus. After receiving a reset, the device is then addressable at the default address." USB

1.1 at 178. In other words, the connected device, after being powered-up through the connection to the USB port though a USB cable, won't process commands until it receives a reset. Baker, ¶ 82. However, if the connected device can't communicate (e.g., because communication has been disable by a High/High signal on the data lines) then the connected device can't receive a reset command and thus can't receive or process commands (to, for example, clear the set C_PORT_ENABLE bit which indicates the port speed can't be determined or to power-down). *Id.* Accordingly, the device simply continues to receive power via V_{BUS} and GND and wait for the reset command (which will not occur with both D+ and D- pulled high). *Id*.

B. Use of SE1 State in Various Contexts

Persons of ordinary skill in art quickly realized that USB devices could use a High/High signal on the D+ and D- lines for a number of purposes. *See e.g.*, Baker, ¶¶ 80-90. This is particularly the case because the signal is an "abnormal" condition that is outside the normal condition signals used by the Specification and thus will not be misread as being used for a specified purpose in the specification. Baker, ¶ 84. Indeed, of the four states available on a D+ and D- line (low/low, high/low, low/high, and high/high), the SE1 signal was the only state not already accounted for in the specification. Baker, ¶¶ 83-84. Accordingly, as noted below, a number of prior art references disclose using the signal for other purposes.

1. US Patent 6,531,845 ("Kerai") (Ex. 1012)

U.S. Patent 6,531,845 was filed as Application No. 09/864,273 on May 25, 2001, claimed a priority date of May 26, 2000, and issued on March 11, 2003. Thus, Kerai is prior art under at least pre-AIA §102(e).

Kerai used a high state on USB D+ and D- for purpose of charging a system while disabling communications. Kerai, Fig 3, 5:43-51. Specifically, Kerai disclosed "A battery charging circuit . . . in which power is derived from a communications port such as a USB interface (22) and is supplied to a rechargeable battery of a communications device." Ex. 1012, Abstract. In its disclosure, Kerai notes that it was "well known" to pull both D+ and D- high when communications were inactive and that this was helpful for purposes of charging a device. *Id.* at 5:45-48 ("*As is well known*, the data lines of a serial connection (D+ and D- in the USB interface) are held high when the connection is inactive and will vary between a high and low state whilst communication over the ports takes place.") (emphasis added); Baker, ¶ 85.

2. US Patent 6,625,738 ("Shiga") (Ex. 1013)

U.S. Patent 6,625,738 was filed as Application No. 09/454,621 on December 6, 1999, claimed a priority date of December 15, 1998, and issued on September 23, 2003. Thus, Shiga is prior art to the '550 patent under at least pre-AIA §102(e).

Shiga recognizes that, the existing USB standards accounted for three (D+, D-) signal line states representing three modes: (1) low-speed mode (D+ signal line is set to a low level ("L") and D- line is set to a high level ("H")); (2) full-speed mode (D+ is high and D- is low); and (3) unconnected mode (both D+ and D- are low). These three states are shown in Shiga's Table 1 seen below. Shiga, 5:38-60; Baker, ¶¶ 86-87.

TABLE 1

	Low Speed	Full Speed	Unconnected
D+	L (Hi-Z)	H	L (Hi-Z)
D–	H (Hi-Z)	L (Hi-Z)	L (Hi-Z)

In contrast to these three USB standard modes, Shiga also explains that the "fourth mode" signal, which is when both D+ and D- are in the H level state (an SE1 condition), is "not a USB standard state" and can therefore "be easily distinguished from USB standard data signals." Shiga, 5:60-62, 6:48-58; Baker, ¶ 87. Shiga discloses transmitting this fourth mode signal from a USB apparatus (*e.g.*, keyboard) to a host computer to wake up the computer. Shiga, Abstract, 6:35-47; Baker, ¶ 87. Accordingly, in 1999, using a signal state that is not a USB standard mode (*i.e.*, in which both D+ and D- are in the H state) was well-known. Shiga, 5:60-62; 6:48-50; Baker, ¶¶ 87.

3. US Patent Application Publication US20030135766 ("Zyskowski") (Ex. 1014)

U.S. Patent App. Publication No. 2003/0135766 was filed as Application No. 09/453,656 on December 3, 1999 and issued on July 17, 2003. Thus, Zyskowski is prior art to the '550 patent under at least pre-AIA §102(e).

Zyskowski is another example of prior art that discloses an SE1 condition (with D+ and D- being set at 5 V) being used by a host device (*e.g.*, computer) to signal its full power state to a connected device (*e.g.*, mass storage device, consumer electronic device). Ex. 1014, ¶ 19; Baker, ¶ 88.

4. US Patent 6,625,790 ("Casebolt") (Ex. 1015)

U.S. Patent 6,625,790 was filed as Application No. 09/409,683 on October 1, 1999, claimed a priority date of July 8, 1998, and issued on September 23, 2003 to Mark W. Casebolt and Lord Nigel Featherston. Thus, Casebolt is prior art to the '550 patent under at least pre-AIA §102(e).

Casebolt discloses that an SE1 condition could be used as a special signaling mode in which the D+ and D- data lines would be connected to Vcc (+5V) to signal the presence of a PS/2 adapter (a 6-pin connector used in older computer keyboards and mice). Ex. 1015 (Casebolt) at 7:40-54; Baker, ¶ 89. Indeed, the SE1 state for USB is shown in Casebolt's Table 1 below. *Id.*

TABLE 1

I/O State	D+/CLK	D−/DAT	USB	PS/2
0	L	L	SEO (Single Ended O) or Reset	Host Inhibit
1	L	H	J, Idle	Host Inhibit
2	H	L	K, Xmit Resume	Host Xmit
3	H	H	SE1 (Single Ended 1)	Idle, Confirm Connect

Ex. 1015, Table 1, *see also* 6:55-7:8.

5. Cypress Semiconductor enCoReUSB Datasheet (Ex. 1016)

Knowledge regarding the use of a state in which D+ and D- are both high was so common that Cypress Semiconductor integrated it into its enCoReUSB product in 2000. Ex. 1016 (Cypress enCoReUSB), 24-25; Baker, ¶ 90.

C. USB 2.0 Specification

The USB 2.0 Specification (USB 2.0) was published on April 27, 2000. Ex. 1011 (USB 2.0). It is prior art to the '550 Patent under at least 35 U.S.C. § 102(a). Moreover, the USB 2.0 Specification would have been part of the knowledge of a POSITA as of the priority date of the '550 Patent. Baker, ¶ 76.

As the USB 2.0 Specification notes, it is fully backwards compatible with devices built with previous versions of the specification, such as USB 1.1. USB 2.0

at 11. The majority of the disclosures of USB 1.1 are also contained in the USB 2.0 Specification. Baker, ¶ 76.

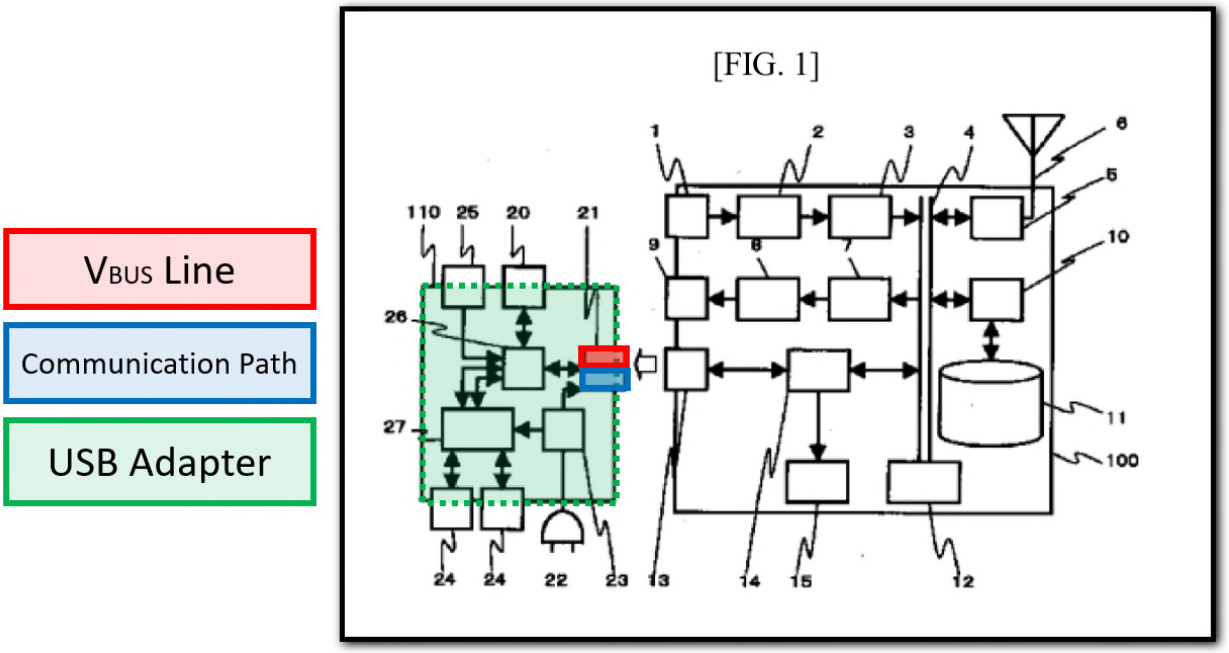
Given the prevalence of the use of the SE1 signal discussed above, the USB 2.0 Specification specifically addresses the SE1 signal. *See e.g.*, USB 2.0 at 123 ("SE1 is a state in which both the D+ and D- lines are at a voltage above V_{OSE1} (min), which is 0.8 V.") Among other things, the USB 2.0 Specification discloses that the signal should not be used for devices seeking to utilize data communications over the USB connection (either low-speed or full-speed). *Id.* ("Low-speed and full-speed USB drivers must never "intentionally" generate an SE1 on the bus."). As noted above, however, persons of ordinary skill in the art understood that the signal could be used for various purposes, including to disable communications for purposes of charging. Baker, ¶¶ 80-84.

D. Overview of Morita

Japanese Patent Application No. 2000-165513A ("Morita"), titled "Charger," was filed on November 30, 1998. Morita is prior art under at least §102(b). A certified translation of Morita is attached here to as Exhibit 1007. Morita was not considered during prosecution.

Morita discloses a charger with the ability to charge a mobile phone and connect the mobile phone to a computer. The charger comprises a "first coupling means for coupling to a mobile phone" and a "second coupling means for coupling

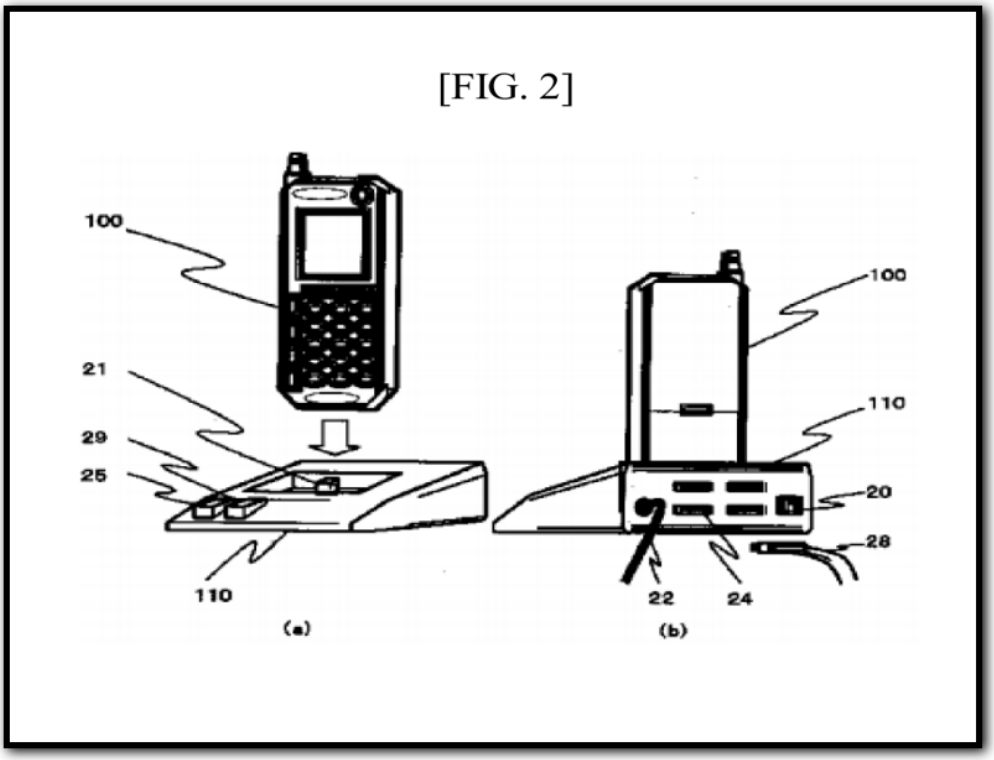
to an external device." Ex. 1007 (Morita) at Abstract. Morita discloses that the provided "coupling means" may be USB connections. *Id.* at [Claim 2]. Figure 1 of Morita discloses several of the key components:



Morita at Figure 1 (annotated); Baker, ¶¶ 102-105. As evidenced in Figure 1, the charger of Morita draws power from an outlet (22) to provide to the mobile device through the USB connection (21). *Id.* at column 3 (Embodiment of Invention) (disclosing a "power supply connection unit such as an outlet"); *id.* at [0014] ("A power supply voltage supplied from a power supply source is supplied from the charging control unit 23 to the USB hub control unit 27 and the second USB port 21"). Accordingly, as a POSITA would understand from the USB Specifications, the "first coupling" (21) provided by Morita is a "high powered" USB port that provides a *minimum* of 500mA to the mobile device. Baker, ¶¶ 117-118. Moreover,

unlike the existing high-power hubs discussed by the patentee in the '021 Application, Morita does not disclose any means for automatically terminating charging when the current supplied to the mobile device exceeds "700mA-800mA." Ex. 1008 ('021 Application) at 22; Baker, ¶ 120.

A POSITA would have understood that, although the charger of Morita can be simultaneously connected to an external computer, there will be situations in which no such active device is connected. In such situations the device acts merely as a charger for the phone. Baker, ¶ 122.

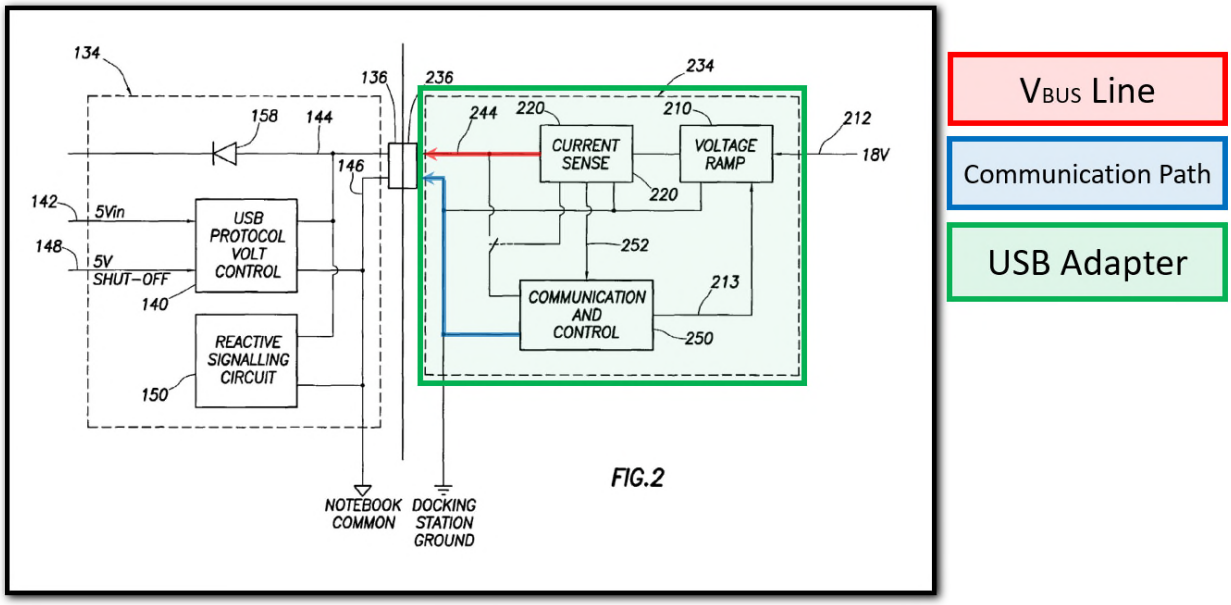


Morita at Figure 2.

E. Overview of Dougherty

U.S. Patent No. 7,360,004 ("Dougherty") is titled "Powering a Notebook Across a USB interface." Dougherty's effective filing date is June 30, 2000, which predates even the '550 Patent's earliest claimed priority date of March 1, 2001. Accordingly, Dougherty constitutes prior art to each of the challenged claims under at least pre-AIA 35 U.S.C. § 102(e).

Dougherty discloses a docking station that powers a laptop using a USB connection. Ex. 1006 (Dougherty) at 2:55-58 (disclosing "a laptop computer and related docking station adapted to supply power from the docking station to the laptop computer across the USB connection."); *see id.* at Figure 2. Dougherty refers to the lines in the connection as "USB power rails" and "serial communication conductors." *See e.g.*, *id.* at Abstract ("A laptop computer and mating docking station where the docking station provides power to the laptop computer over the power rails of the Universal Serial Bus (USB) interface.") and 5:26-37; Baker, ¶¶ 109-110. As a POSITA would have recognized by reference to a USB connection, the dock of Daugherty includes a USB V_{BUS} line and a USB communication path. Baker, ¶ 108.



Ex. 1006 (Dougherty) at Figure 2 (annotated).

In order to power the laptop, the system of Dougherty disregards a number of the conditions associated with the USB Specification. *See e.g.*, *id.* at 2:55-3:10; *id.* at 6:1 (disclosing that the system "breaks with standard USB protocol"); Baker, ¶¶ 109-110. Among other things, the 5V typically supplied by the output USB connection of the laptop is disengaged and, instead, the port receives power at 18.5 volts from the docking station on that connection. *Id.* at 2:58-64 ("To accomplish this, the laptop computer is modified to have circuitry which is capable of being detected across USB power rails by the docking station and also capable of turning off the five volts typical supplied by the laptop onto the USB port, and instead, receiving power at 18.5 volts, from the docking station across the USB connections."). Baker, ¶¶ 109-110. This means that the dock is supplying power at

its upstream port, which is inconsistent with the USB 1.1 Specification. *See e.g.*, USB 1.1 at 135 ("No device shall supply (source) current on the VBUS at its upstream port at any time."); Baker, ¶ 109.

As a result of this connection, the dock supplies current to the laptop over the USB connection that exceeds the maximum amounts permitted by the USB Specification. Baker, ¶ 110. Specifically, Dougherty discloses that dock may supply 2.5 amps of current to the laptop. *Id.* at 7:47-51 ("When the dock station 200 provides power for full operation of the laptop computer 100, as many as 2.5 amps of current may flow from the dock station 200 to the laptop computer 100 across the USB connectors 136,236."). As noted above, this is more than five times the maximum amount that a device is to consume/draw under the USB Specification. *See e.g.*, USB 1.1 at 134-134; Baker, ¶ 110.

Because the dock supplies all the power required by the laptop, no other power adapter is required. Dougherty at 3:4-6 ("Thus, a laptop user need only plug the laptop into the docking station via the USB port, even if the battery for the laptop computer is drained."); Baker, ¶ 110.

VII. CLAIM CONSTRUCTION

Claim construction is only necessary to the extent it is required to resolve disputes presented in the Petition. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Petitioners submit that, other

than the terms addressed below, no terms need to be construed to resolve the issues presented by this Petition and the claims should be afforded their plain and ordinary meaning in view of the '550 Patent's specification and prosecution history, as would have been understood by a POSITA. If Patent Owner attempts to create a claim construction dispute in its preliminary response, Petitioners reserve the right to address the issue in a reply to that preliminary response. If the Patent Owner attempts to create a claim construction issue in its post-institution response, Petitioners will address such issues in their reply.

The Board construes claims in an IPR in accordance with *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (*en banc*). 83 Fed. Reg. 51340, 51340-44 (Oct. 11, 2018). Under the *Phillips* standard, "words of a claim are generally given their ordinary and customary meaning." *Phillips*, 415 F.3d at 1312-13 (internal quotations omitted).

A. "at least one associated condition specified in a USB specification" (claim 1) and "at least one USB Specification imposed limit" (claim10)

The PTAB has already construed each of these phrases. *See ZTE (USA) Inc. et al. v. Fundamental Innovation System International LLC*, IPR2018-00111 at Paper 62 (Final Written Decision) at 7-13. Specifically, the PTAB held that the "at least one associated condition specified in a USB specification" (Claim1) and the

"at least one USB Specification imposed limit" must be conditions/limits that affect the supply of current on the V_{BUS} line. *Id.*

In adopting this construction, the PTAB adopted patent owner's argument that there were a number of current-related conditions/limits set forth in the USB Specification, including, for example, the amount of the current, the direction of the current flow, and the time limit for providing current. *Id.* at 10 ("Patent Owner persuasively demonstrates, however, that the USB specification specifies multiple conditions that are associated with the supply of current on the V_{BUS} line, including 'a current limit,' a condition on the 'current flow direction,' and a time limit for providing current."); *see* IPR2018-00111, Exhibit 2011 (Fernald Declaration) at ¶¶ 48-51. Patent owner explained, for example, that engaging in the "enumeration" process prior to supplying more than the 100 mA minimum amount of current over the interface was a condition that could satisfy this limitation. IPR2018-00111, Exhibit 2011 (Fernald Declaration) at ¶ 50 ("A POSA would understand that the condition that a USB device must participate in enumeration before drawing '5 unit loads' is an 'associated condition' to supplying current on the V_{BUS} line . . . .").

Accordingly, for purposes of this IPR Proceeding, Petitioner adopts the Board's prior construction which encompasses conditions/limitations related the supply of current, including at least: the amount of current supplied, the amount of current supplied prior to enumeration, and the direction in which current is supplied.

B. "abnormal data condition" (claims 4, 6, 7, 13, 15, and 16)

In previous litigations, Patent Owner has contended that the phrase "abnormal data condition" in claims 4, 6, 7, 13, 15 and 16 should be construed as "condition detected at the USB communication path that is not defined as a valid (or legal) data condition by the USB specification." Ex. 1023. For the limited and sole purpose of this IPR proceeding only, Petitioner adopts Patent Owner's proposal for the construction of this claim phrase. *Id.; Toyota Motor Corp.*, IPR2016-00422, *26.

VIII. ANALYSIS

A. Morita In View Of Knowledge of a POSITA Renders The Subject Matter Of Claims 1-18 Obvious.

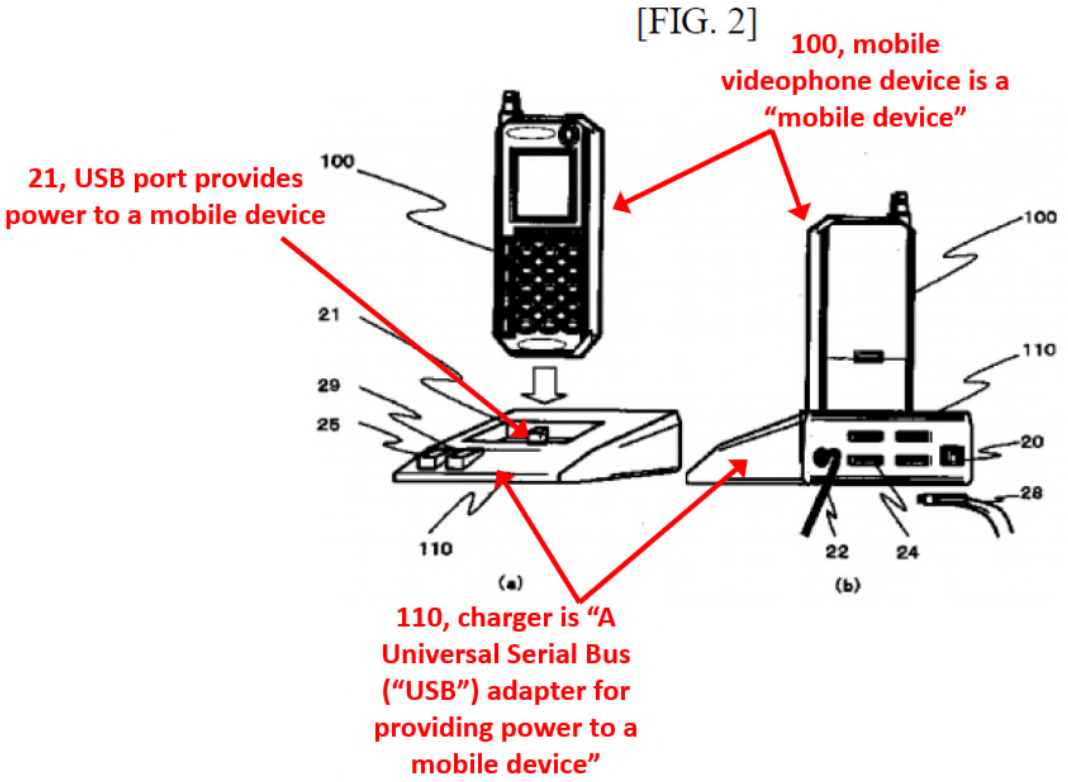
As noted above and herein, Morita expressly discloses a mobile device charger that provides a USB port for charging the mobile device. *See e.g.*, Ex. 1007 (Morita) at [Claim 1], [Claim 2], [0010]-[0011], and [0016]. As also discussed above, a POSITA would have been aware of the USB Specifications that existed as of the priority date of the '550 Patent. This includes the USB 1.1 and USB 2.0 Specifications. *See* Section IV.C; Baker, ¶ 68.

1. Claim 1

a. 1[a]. An adapter comprising

To the extent the preamble of claim 1 is limiting, it is disclosed by Morita. Baker, ¶¶ 111-112. Morita discloses a charger with a USB port for charging a mobile phone. *E.g.*, Morita at Claim 1 ("A charger capable of charging a mobile phone . . .

comprising: first coupling means for coupling to a mobile phone") and Claim 2 ("The charger according to claim 1, wherein the first coupling means . . . are configured from a USB format."); *id.* at [0016] ("In FIG. 2, the mobile videophone device 100 is connected to the USB port 21 of the charger 110. . ."); *see also id.*at [0010]-[0011]. A POSITA would have understood Morita's charger 110 to be a "an adapter." Baker, ¶¶ 111-112.



Morita, Figure 2 (annotated).

b. 1[b] a USB V_{BUS} line and a USB communication path

Morita discloses or renders obvious "a USB V_{BUS} line and a USB communication path." Baker, ¶¶ 113-115. As noted above with respect to claim element 1[a], Morita discloses a charger (adapter) that can be coupled to a mobile

phone through a "USB" connection. *See e.g.,* Morita at [Claim 1], [Claim 2], [0010]-[0011], and [0016]. And, as noted above in the summary of the prior art, as of the priority date of the '550 Patent, a POSITA would have knowledge of USB specifications, including USB 1.1 and USB 2.0. Baker, ¶ 68.

The USB Specifications disclose, and a POSITA would have understood, that the "USB" connection disclosed by Morita comprises a USB V_{BUS} line and a USB communication path. Indeed, the USB Specifications disclose that the USB coupling of Morita would have four wires or contacts: V_{BUS} and GND (ground) lines that provide power and D+ and D- lines that carry signals for communication. *See e.g.*, Ex. 1010 (USB 1.1) at 15-18, 80-82; Ex. 1011 (USB 2.0) at 15-18, 93-94, and 173-175; Baker, ¶¶ 113-115.

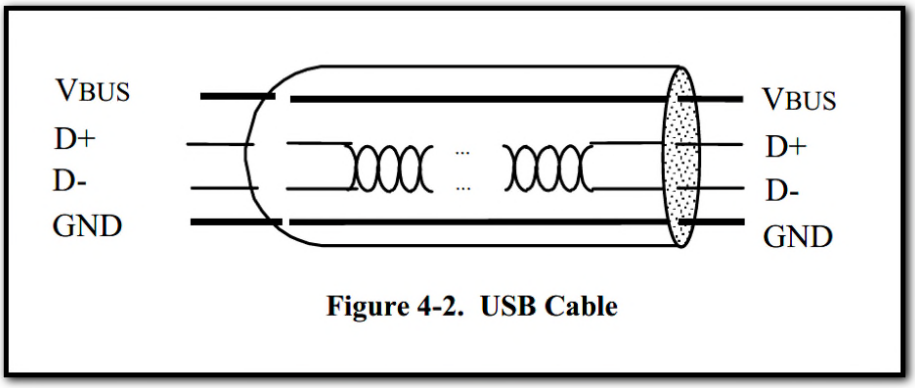


Figure 4-2. USB Cable

USB 1.1 at Figure 4-2.

Table 6-1. USB Connector Termination Assignment

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
Shell	Shield	Drain Wire

USB 1.1 at Table 6-1.

The "V_{BUS}" line disclosed in the specification constitutes the claimed V_{BUS} line. Baker, ¶ 113. Moreover, a POSITA would understand that the data connections, including at least the data lines (D+ and D-), provide a "USB communication path" as required by Claim 1 of the '550 Patent. *See e.g.* USB 1.1 at 25 ("The USB provides communication services between a host and attached USB devices."). Indeed, dependent claims of the '550 Patent identify the D+ and D- lines as the primary example of the claimed "USB communication path." *See e.g.*, Ex. 1001 ('550 Patent) at claim 5 ("The adapter of claim 4, wherein said USB communication path includes a D+ and D- line.").

Accordingly, a POSITA would understand that the charger (adapter) of Morita includes "a USB V_{BUS} line and a USB communication path" as required by Claim 1 of the '550 Patent.

c. 1[c] said adapter configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification

Morita discloses or renders obvious "said adapter configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification." Baker, ¶¶ 116-122. Specifically, a POSITA would have understood that the charger supplies current on the V_{BUS} line as this line is used for providing power to devices using power from a USB connection. *See e.g.*, USB. 1.1 at 142; Baker, ¶ 130. Moreover, Morita renders obvious a charger that (1) supplies more than 500 mA to a device and (2) provides more than 100 mA to a device without performing USB enumeration.

(1) Supplying More than 100 mA or 500mA of Current.

First, a POSITA would have understood or found obvious that the charger of Morita is configured to provide more that 500mA of current to the mobile device. Baker, ¶¶ 117-122. Specifically, as noted above, Morita discloses that the charger draws power from an outlet. *See e.g.,* Morita at Figure 2 (component 22, outlet connection) and [0014] ("A power supply voltage supplied from a power supply source is supplied from the charging control unit 23 to the USB hub control unit 27 and the second USB port 21"). Accordingly, a POSITA would understand from the USB 2.0 Specification that the "first coupling" provided by Morita is a "high powered" port, and would thus configure the charger to provide a ***minimum*** of five

"unit loads" of current (500mA) through that port to the charging mobile device. USB 2.0 at 171 ("Systems that obtain operating power externally, either AC or DC, must supply at least five unit loads [500mA] to each port. Such ports are called high-power ports.") (emphasis added); *see also* USB 1.1 at 134 (same); Baker, ¶ 120.

Table 7-7. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage:					
High-power Port	VBUS	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	VBUS	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current:					
High-power Hub Port (out)	ICCPRT	Section 7.2.1	500		mA
Low-power Hub Port (out)	ICCUPT	Section 7.2.1	100		mA
High-power Function (in)	ICCHPF	Section 7.2.1		500	mA
Low-power Function (in)	ICCLPF	Section 7.2.1		100	mA
Unconfigured Function/Hub (in)	ICCINIT	Section 7.2.1.4		100	mA
Suspended High-power Device	ICCSH	Section 7.2.3; Note 15		2.5	mA
Suspended Low-power Device	ICCSL	Section 7.2.3		500	A

USB 2.0 at 178 (Table 7-7) (annotated); *see also* USB 1.1 at 142 (Table 7-5) (same).

Given this configuration as a high-powered hub connected to a single downstream device, a POSITA would have understood or found obvious that the charger of Morita supplies more than 500mA through the port in at least some circumstances (e.g., when the phone is not already fully charged) and, thus, is configured to supply such current. Baker, ¶ 119. Indeed, the 500mA is only a ***minimum*** for the charger, and the patentee admitted in the '021 Application (to which the '550 Patent claims priority) that such high power hubs typically provided up to "700mA-800mA" to a single connected device before automatically

terminating the voltage. Ex. 1008 ('021 Application) at 23. Although it is not required to disclose this element, the Charger of Morita is likely to provide even more than 700mA-800mA of current because, unlike the existing devices cited by the patentee in the '021 Application, Morita does not disclose any means for automatically limiting the amount of current that it provides. Baker, ¶ 120. Moreover, a POSITA would have been motivated to charge the phone at a higher current because he or she would have known that it would improve the time for charging. *See e.g., id.*; Ex. 1019 (U.S. Pat. No 5,923,146, "Martensson"), 1:5-8 (invention relates to charging "cellular radio telephone"), 1:30-34 ("fast-charged" technique using "600-1000 mA").

Thus, a POSITA would have understood the charger is "configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification." Indeed, the USB Specification discloses as a condition/limit that a USB device should not be supplied with more than 100mA to a "low-power" power or 500 mA to a "high-power" device:

Table 7-7. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage:					
High-power Port	V_{BUS}	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	V_{BUS}	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current:					
High-power Hub Port (out)	I_{CCPRT}	Section 7.2.1	500		mA
Low-power Hub Port (out)	I_{CCUPT}	Section 7.2.1	100		mA
High-power Function (in)	I_{CCHPF}	Section 7.2.1		500	mA
Low-power Function (in)	I_{CCLPF}	Section 7.2.1		100	mA
Unconfigured Function/Hub (in)	I_{CCINIT}	Section 7.2.1.4		100	mA
Suspended High-power Device	I_{CCSH}	Section 7.2.3; Note 15		2.5	mA
Suspended Low-power Device	I_{CCSL}	Section 7.2.3		500	A

USB 2.0 at 178 (Table 7-7) (annotated); *see also* USB 1.1 at 142 (Table 7-5) (same). Accordingly, regardless of whether the mobile device is a high-powered or low-powered device a POSITA would understand that the charger of Morita would supply current without regard to these current limits. At a minimum, a POSITA would understand the charger is capable of supplying current in his manner, which is sufficient. *See ParkerVision, Inc. v. Qualcomm Inc.*, 903 F.3d 1354, 1361 (Fed. Cir. 2018); Baker, ¶¶ 120-121.

(2) Supplying More than 100mA of Current without Enumeration.

Second, a POSITA would have found obvious that the charger of Morita can be configured to provide current in excess of 100mA without enumeration. Baker, ¶¶ 122, 124; *see also id.* at ¶¶ 125-131. Specifically, as noted above, a POSITA would have understood that, in some circumstances, the charger of Morita would not

be connected to a computer and thus, would act only as a charging device. *See e.g.*, Morita at Figure 2; Baker, ¶ 122. In those situations, the two devices have no reason or ability to communicate over the data lines (D+ and D-) and thus enumeration is not possible. *Id.* Accordingly, as noted above, the charging device would provide a *minimum* of 500 mA of current on the V_{BUS} without enumeration. This disregards the USB Specification's condition/limit on the amount of current that may be supplied without enumeration, which is one unit load (100 mA). USB 2.0 at 171 ("Devices must also ensure that the maximum operating current drawn by a device is one unit load, until configured."); Baker, ¶ 122.

For each of these reasons, a POSITA would have understood that the charger of Morita discloses or renders obvious a charger "configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification"

2. Claim 2: The adapter of claim 1 wherein said associated condition is a current limit.

As explained above, Morita discloses or renders obvious the adapter of claim 1. A POSITA would have understood that said Morita also renders obvious that "said associated condition is a current limit." Indeed, as explained above with respect to claim element 1[c], Morita discloses a phone charger (adapter) that is connected directly to external power and supplies a *minimum* of 500 mA to a single mobile phone device without enumeration. *See* Section VIII.A.1.c; Baker, ¶¶ 116-

122. As such, the charger disregards two current limits of the USB Specifications: (1) that no more than 500 mA of current be supplied to a device and (2) that no more than 100 mA of current be supplied to a device without enumeration. *Id.*

3. Claim 3: The adapter of claim 1 wherein said current is supplied without USB enumeration

As explained above, Morita discloses the adapter of claim 1. Morita also renders obvious that "said current is supplied without USB enumeration." Baker, ¶¶ 116-124. Indeed, as explained above with respect to claim element 1[c], Morita discloses a phone charger (adapter) that is connected directly to external power and supplies a minimum of 500 mA to a mobile phone device without communication over the USB communication path. *See* Section *See* Section VIII.A.1.c. As such, the current is supplied without enumeration.

4. Claim 4: The adapter of claim 1 wherein said current is supplied in response to an abnormal data condition on said USB communication path

As explained above, Morita discloses the adapter of claim 1. Morita further renders obvious that "said current is supplied in response to an abnormal data condition on said USB communication path." Baker, ¶¶ 125-131.

As explained above with respect to claim element 1[c], a POSITA would have understood that, in at least some cases, the charger of Morita will be used with a mobile device but not an external computer and, in such cases, cannot engage in typical USB communication. Baker, ¶ 122. In such cases, the device will have to

signal that it can be used for charging but cannot engage in typical communication or enumeration processes. Baker, ¶¶ 122, 126. As of the priority date of the relevant claims, it was well known in the art that driving both of the data lines (D+ and D-) high (which, as noted above, was known as an "SE1" signal) would serve this purpose, i.e., it would disable communications and allow for charging. Baker, ¶¶ 126-131. Accordingly, a POSITA would have been motivated with a high expectation of success, to supply the current in response to an SE1 signal on the USB data lines.

As discussed in Section VI.B, above, other prior art expressly disclosed that it was known to use this state for a variety of reasons. Kerai, for example, is a patent that issued from an application filed on May 26, 2001. Ex. 1012 (Kerai). It discloses a "charging circuit" within a mobile device that can be charged via a USB connection with a laptop. *See e.g. id.* at Abstract ("A battery charging circuit is described in which power is derived from a communications port such as a USB interface (22) and is supplied to a rechargeable battery of a communications device. The communications device, which may be a mobile radio telephone, can be charged from the power supply or internal battery of a laptop computer equipped with a USB port and connected thereto with a suitable cable"). The specification of Kerai notes that it was "well known" in the art that data lines are held high when they are inactive, i.e., when no communication is taking place and, so, the state can be used

during charging. *Id.* at 5:43-51 "As is well known, the data lines of a serial connection (D+ and D- in the USB interface) are held high when the connection is inactive and will vary between a high and low state whilst communication over the ports takes place.") (emphasis added); *see also* Baker, ¶¶ 84-90, 128-131.

Moreover, use of the SE1 signal is also taught by the USB 2.0 Specification, which refers to this state as "single ended one" or "SE1." Indeed, while the SE1 signal was not disclosed or referenced in the USB 1.1 specification (1998), it had become so widely used by 2000 that it was added to the USB 2.0 specification in April 2000 (six months prior to the '486 Application in which the patentee first disclosed using this signal):

Table 7-2. Low-/full-speed Signaling Levels

Bus State	Signaling Levels		
	At originating source connector (at end of bit time)	At final target connector	
		Required	Acceptable
Differential "1"	D+ > V_{OH} (min) and D- < V_{OL} (max)	(D+) - (D-) 200 mV and D+ V_{IH} (min)	(D+) - (D-) 200 mV
Differential "0"	D- > V_{OH} (min) and D+ < V_{OL} (max)	(D-) - (D+) > 200 mV and D- V_{IH} (min)	(D-) - (D+) > 200 mV
Single-ended 0 (SE0)	D+ and D- < V_{OL} (max)	D+ and D- < V_{IL} (max)	D+ and D- < V_{IH} (min)
Single-ended 1 (SE1)	D+ and D- > V_{OSE1}(min)	D+ and D- > V_{IL} (max)	

USB 2.0 at 145 (excerpted and annotated); Baker, ¶ 80.

Table 11-8. Upstream Facing Port Receiver Signal/Event Definitions

Signal/Event Name	Event/Signal Source	Description
HS	Internal	Port is operating in high-speed
Tx_active	Transmitter	Transmitter in the Active state
J	Internal	Receiving a 'J' (IDLE) or an 'SE1' on the upstream facing port
HJ	Internal	Receiving an HJ on the upstream facing port
EOI	Internal	End of timed interval
EOITR	Internal	Generated 24 full-speed bit times after the K->SE0 transition at the end of resume
HK, K	Internal	Receiving an HK, 'K' on the upstream facing port
Tx_resume	Transmitter	Transmitter is in the Sresume state
HS_Idle	Internal	Receiving an Idle state on the high-speed upstream facing port
SE0	Internal	Receiving an SE0 on the full-speed upstream facing port
EOR	Internal	End of Reset signaling from upstream
POR	Implementation-dependent	Power_On_Reset

USB 2.0 at 320 (annotated).

Given his or her knowledge of the USB specification, a POSITA would know that the charger of Morita could not use the data lines to indicate "low-speed" or "high-speed" communications (by pulling D+ low and D- high or D+ high and D- low, respectively) because, without a connected computer (i., a USB Host or Hub), no such communications would be made. Baker, ¶ 126. And a POSITA would not have drawn both D+ and D- low because this would have indicated that no device was attached (which is not true because the mobile device is connected). *Id.* Accordingly, ***the only other possible state of the data lines*** is pulling both D+ and D- high, which, as noted above and as was well known in the art, would indicate to

the mobile device that it cannot communicate via the data lines. Baker, ¶¶ 126-131. Moreover, using this signal would have been a simple modification based on the teachings in the USB specifications. *Id.*. At a minimum, it would have been obvious to try using the SE1 state for a "charging only mode," which would have skipped enumeration, because there are only four possible states and three of them were used for states that did not apply. Baker, ¶ 126.

A POSITA would have understood that the SE1 signal is an "abnormal data condition" because it ceases normal USB communications. Baker, ¶¶ 80, 129. The SE1 signal is not mentioned in the USB 1.1 Specification. *See* USB 1.1; Baker, ¶ 129. Moreover, although it is noted and discussed in the USB 2.0 Specification, the USB 2.0 specification indicates that it is not a part of normal communications and thus, devices seeking to communicate should not intentionally use the signal. USB 2.0 at 123 ("Low-speed and full-speed USB drivers must never 'intentionally' generate an SE1 signal on the bus. SE1 is a state in which both the D+ and D- lines are at a voltage above V_{OSE1} (min), which is 0.8V.")[2]; Baker, ¶ 80. And, as mentioned above, other references related to USB connections explain that it is an

[2] Because the charger of Morita is neither a "low-speed" or "full-speed" USB driver, a POSITA would have understood that it may use this abnormal signal. Baker, ¶ 126.

abnormal state. *See e.g.*, Ex. 1013 (Shiga) at 5:60-62 ("The state in which both of these first and second signal data lines D+ and D- are in the H state is not a USB standard state.").

Accordingly, a POSITA would have understood or found obvious that the charger supplies current "in response to an abnormal data condition on said USB communication path."

5. Claim 5: The adapter of claim 4 wherein said USB communication path includes a D+ line and a D− line

As explained above, Morita renders the adapter of claim 4 obvious. A POSITA would have understood that "said USB communication path [of Morita] includes a D+ line and a D− line." Indeed, as explained above with respect to claim element 1, Morita discloses a phone charger (adapter) that is connected to a mobile phone via a "USB" coupling, which a POSITA would have understood comprises a D+ and a D- line. *See* Section VIII.A.1.a-b.

6. Claim 6: The adapter of claim 5 wherein said abnormal data condition is an abnormal data line condition on said D+ line and said D− line.

As explained above, Morita renders the adapter of claim 5 obvious. Morita further renders obvious that "said abnormal data condition is an abnormal data line condition on said D+ line and said D− line." Baker, ¶¶ 80, 129. Indeed, as explained above with respect to claim elements 1[c] and claim 4, a POSITA would have been

motivated to use an SE1 signal as the "abnormal data condition" by pulling the D+ and D- lines high. *See* Sections VIII.A.1 and VIII.A.4.

7. Claim 7: The adapter of claim 6 wherein said abnormal data line condition is a logic high signal on each of said D+ and D− lines.

As explained above, Morita renders the adapter of claim 6 obvious. Morita further renders obvious that "said abnormal data line condition is a logic high signal on each of said D+ and D− lines." Baker, ¶¶ 125-131. Indeed, as noted above, with respect to claim elements 1[c] and claims 4 and 6, the "abnormal data condition" is an SE1 signal provided by the D+ and D- lines. *See* Sections VIII.A.1, 4, 6. As explained by the USB 2.0 specification, and as would be known to persons of skill in the art, this signal is a logic high on each of said D+ and D- lines (at least 0.8V). *See e.g.*, USB 2.0 ("SE1 is a state in which both the D+ and D- lines are at a voltage above V_{OSE1} (min), which is 0.8V.").

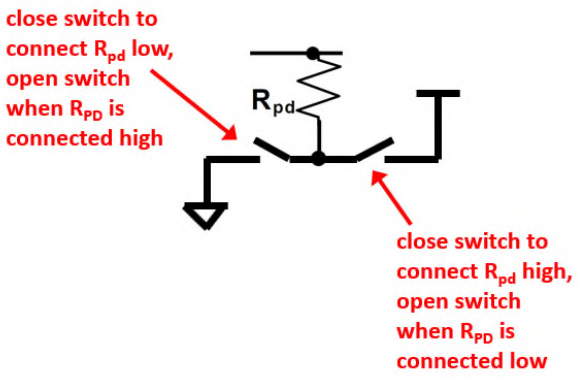
Table 7-2. Low-/full-speed Signaling Levels

Bus State	Signaling Levels		
	At originating source connector (at end of bit time)	At final target connector	
		Required	Acceptable
Differential "1"	D+ > V_{OH} (min) and D- < V_{OL} (max)	(D+) - (D-) 200 mV and D+ V_{IH} (min)	(D+) - (D-) 200 mV
Differential "0"	D- > V_{OH} (min) and D+ < V_{OL} (max)	(D-) - (D+) > 200 mV and D- V_{IH} (min)	(D-) - (D+) > 200 mV
Single-ended 0 (SE0)	D+ and D- < V_{OL} (max)	D+ and D- < V_{IL} (max)	D+ and D- < V_{IH} (min)
Single-ended 1 (SE1)	D+ and D- > V_{OSE1}(min)	D+ and D- > V_{IL} (max)	

USB 2.0 at 145 (excerpted and annotated).

8. Claim 8: The adapter of claim 7, wherein each said logic high signal is greater than 2V.

As explained above, Morita renders the adapter of claim 7 obvious. Morita further renders obvious that "each said logic high signal is greater than 2V." Specifically, the USB Specifications—which were within the knowledge of a POSITA—teach that implementing a logic high signal on the D+ and D- lines would be accomplished by connecting the lines through a pull-up resistor to V_{TERM}. Baker, ¶ 135.



USB 1.1 at 113 (annotated portion of Figure 7-10). Moreover, a person of ordinary skill in the art would have understood that V_{TERM} is typically 3.0 to 3.6 V, which is greater than 2.0V. Baker, ¶ 135.

9. Claim 9: The adapter of claim 2 wherein said current limit is 500 mA.

As explained above, Morita discloses the adapter of claim 2. A POSITA would have understood that said Morita also discloses said adapter in wherein "said current limit is 500 mA." Baker, ¶¶ 116-122. Indeed, as explained above with respect to claim element 1[c], Morita discloses a phone charger (adapter) that is

connected directly to external power and supplies a *minimum* of 500 mA to a mobile phone device without any limiting circuitry. *See* Section VIII.A.1.c. As such, the charger supplies current without regard to the condition of the USB Specification that no more than 500 mA of current be supplied to a device. *Id.*

10. Claim 10:

a. 10[a]. An adapter comprising

As explained above with respect to claim element 1[a], Morita an adapter. *See* Section VIII.A.1.a.

b. 10[b]. a USB V_{BUS} line and a USB communication path

As explained above with respect to claim element 1[b], Morita discloses an adapter comprising a USB V_{BUS} line and a USB communication path. *See* Section *See* Section VIII.A.1.b.

c. 10[c]. said adapter configured to supply current on the V_{BUS} line without regard to at least one USB Specification imposed limit.

Morita discloses or renders obvious an adapter "configured to supply current on the V_{BUS} line without regard to at least one USB Specification imposed limit." Indeed, as explained above with respect to claim element 1[c], Morita discloses a phone charger (adapter) that is connected directly to external power and supplies a minimum of 500 mA to a mobile phone device without enumeration. *See* Section VIII.A.1.c. As such, the charger (adapter) disregards two "USB Specification

imposed limits": (1) that no more than 500 mA of current be supplied to a single device; and (2) that no more than 100 mA of current be supplied to a single device without enumeration. *Id.*

11. Claim 11: The adapter of claim 10, wherein said USB Specification imposed limit is a current limit.

As explained above with respect to claim 10, Morita discloses the adapter of claim 10. Moreover, as explained above with respect to claim 2, Morita discloses or renders this additional limitation. *See* Section VIII.A.2.

12. Claim 12: The adapter of claim 10, wherein said current is supplied without USB enumeration.

As explained above with respect to claim 10, Morita discloses the adapter of claim 10. Moreover, as explained above with respect to claim 3, Morita discloses or renders obvious this additional limitation. *See* Section VIII.A.3.

13. Claim 13: The adapter of claim 10, wherein said current is supplied in response to an abnormal data condition on said USB communication path.

As explained above with respect to claim 10, Morita discloses the adapter of claim 10. Moreover, as explained above with respect to claim 4, Morita renders this additional limitation obvious. *See* Section VIII.A.4.

14. Claim 14: The adapter of claim 13, wherein said USB communication path includes a D+ line and a D− line.

As explained above with respect to claim 13, Morita renders the adapter of claim 13 obvious. Moreover, as explained above with respect to claim 5, Morita discloses this additional limitation. *See* Section VIII.A.5.

15. Claim 15: The adapter of claim 14, wherein said abnormal data condition is an abnormal data line condition on said D+ line and said D− line.

As explained above with respect to claim 14, Morita renders the adapter of claim 14 obvious. Moreover, as explained above with respect to claim 6, Morita renders obvious this additional limitation. *See* Section VIII.A.6.

16. Claim 16: The adapter of claim 15, wherein said abnormal data line condition is a logic high signal on each of said D+ and D- lines.

As explained above with respect to claim 15, Morita renders the adapter of claim 15 obvious. Moreover, as explained above with respect to claim 7, Morita renders obvious this additional limitation. *See* Section VIII.A.7.

17. Claim 17: The adapter of claim 16, wherein each said logic high signal is greater than 2V.

As explained above with respect to claim 16, Morita renders the adapter of claim 16 obvious. Moreover, as explained above with respect to claim 8, Morita renders obvious this additional limitation. *See* Section VIII.A.8.

18. Claim 18: The adapter of claim 11, wherein said current limit is 500 mA.

As explained above with respect to claim 11, Morita i discloses the adapter of claim 11. Moreover, as explained above with respect to claim 9, Morita discloses or renders obvious this additional limitation. *See* Section VIII.A.9.

B. Dougherty In View Of the USB 1.1 Renders The Subject Matter Of Claims 1-2, 9, 10-11, And 18 Obvious.

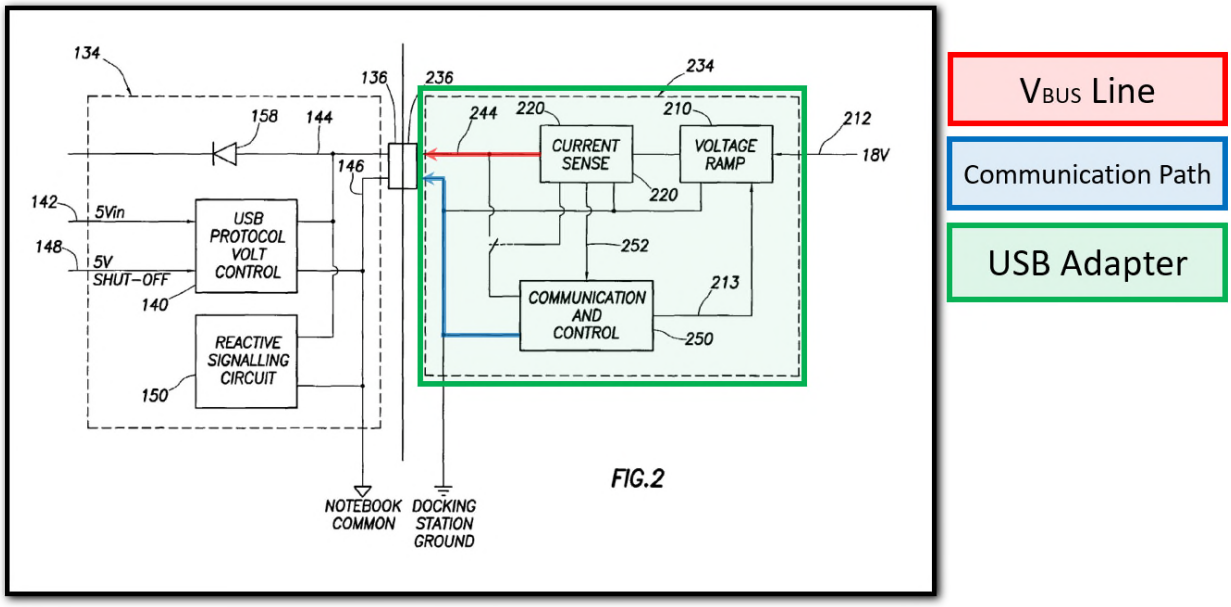
A POSITA would have been motivated to combine the teachings of Dougherty with the teachings of the USB Specification, including USB 1.1. Baker, ¶ 148. As noted above and herein, Dougherty expressly discloses a docking station with a USB port for providing power to a laptop. *See e.g.*, Ex. 1006 (Dougherty) at Abstract, Figure 2, 2:55-58, 5:26-37. Accordingly, to the extent the relevant components of that that port were not disclosed by Dougherty, a POSITA would have looked to the USB Specification to implement them as discussed herein. Baker, ¶ 148.

1. Claim 1

a. 1[a]. An adapter comprising

Dougherty in view of USB 1.1 discloses an adapter. Baker, ¶ 149. Specifically, Dougherty discloses "a laptop computer and related docking station adapted to supply power from the docking station to the laptop computer across the USB connection." Dougherty at 2:52-55 (emphasis added). A POSITA would have understood that the docking station is an "adapter" as that term is used by the '550

Patent because the dock adapts power from a voltage supply into a form that can supplied to the laptop. Baker, ¶ 149. Specifically, as shown in Figure 2 of Dougherty, the docking logic 234 (part of the docking station 200), "[v]oltage ramp logic 210 couples to an 18 volt supply which preferably comes from a power supply (not specifically shown)." Dougherty at 7:7-9.



Dougherty at Figure 2 (annotated).

The specification of the '550 Patent provides the following examples of adapters: (a) a wall adapter; (b) a pass-through device that creates a communication path between a USB hub or host and a mobile device; and (c) something that "may be embodied in a USB host or hub." *See e.g.*, '550 Patent at 2:19-33 and 8:60-62. In each case, the '550 identifies devices adapted to provide power, just as the dock

of Dougherty is designed to do. Accordingly, a POSITA would have understood that the dock of Dougherty is an "adapter." Baker, ¶ 149.

b. 1[b] a USB V_{BUS} line and a USB communication path

Dougherty in view of USB 1.1 discloses or renders obvious a USB V_{BUS} line and a USB Communication path. Baker, ¶¶ 150-151. Specifically, Dougherty discloses that the dock comprises "a mating USB connector 236" for connecting to the laptop computer. Dougherty at 5:11-14 ("Docking of these two logic circuits is preferably through USB connector 136 of the laptop computer and a mating USB connector 236 of the docking station.") (emphasis added)

USB 1.1 discloses, and a POSITA would have understood, that the USB connector 236 of the docking station of Dougherty includes at least four connections: (a) a V_{BUS} line, (b) a Ground (GND) line, (c) a D+ line, and (d) a D- line. *See e.g.*, USB 1.1 at 17; Baker, ¶ 150.

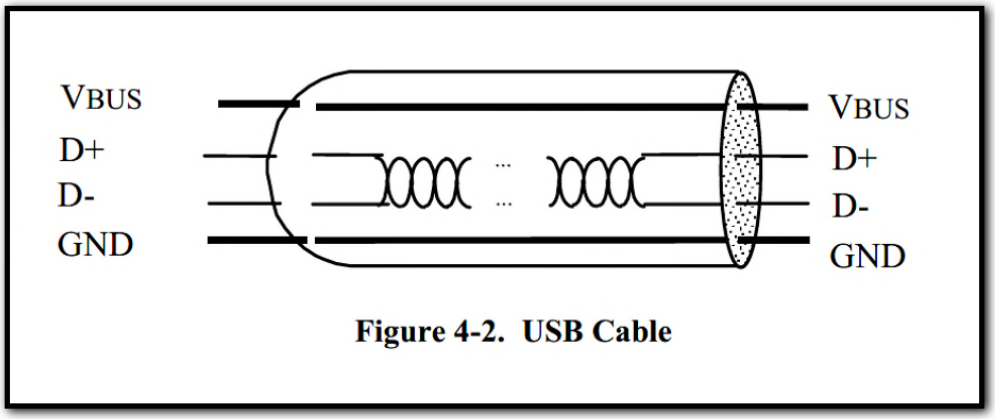


Figure 4-2. USB Cable

USB 1.1 at Figure 4-2.

Table 6-1. USB Connector Termination Assignment

Contact Number	Signal Name	Typical Wiring Assignment
1	VBUS	Red
2	D-	White
3	D+	Green
4	GND	Black
Shell	Shield	Drain Wire

Id. at Table 6-1.

A POSITA would understand that the V_{BUS} line disclosed by Dougherty in view of USB 1.1 constitutes the claimed USB V_{BUS} Line. Baker, ¶ 150. A POSITA would have further understood the D+ and D- lines to constitute the claimed "USB communication path." Indeed, the '550 specifically identifies the D+ and D- lines of a USB connection as a "communication path" in both the specification and later dependent claims. Ex. 1001 ('550 Patent) at 7:13-16 ("The USB adapter 100 also optionally provides a communication path for data across the D+ and D- data pins in the USB connectors 54 and 102."); *id.* at Claim 5 ("said USB communication path includes a D+ and a D- line).

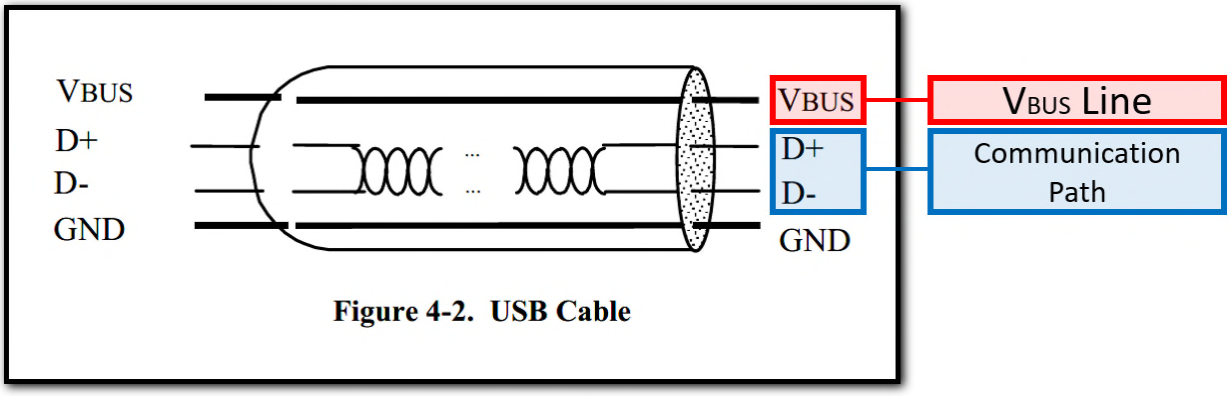


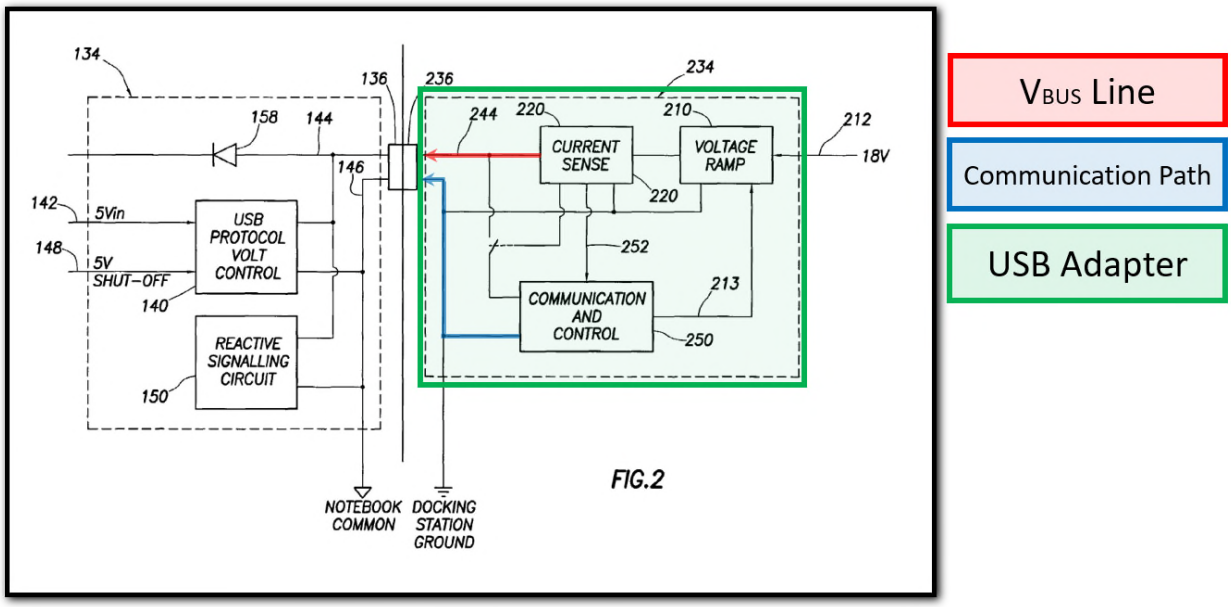
Figure 4-2. USB Cable

See e.g., Ex. 1010 (USB 1.1) at 17 and Figure 4-2.

Moreover, although it does not use the same terminology, Dougherty specifically discloses the required V_{BUS} line and Communication path. *See* Dougherty at 3:24-40 (discussing "Notation and Nomenclature" and noting that "[t]his document does not intend to distinguish between components that differ in name but not in function.") Specifically, Dougherty refers to the V_{BUS} line as the "USB Power rails"[3] and the communication path as the "serial communication conductors." *See e.g.*, *id.* at Abstract ("A laptop computer and mating docking station where the docking station provides power to the laptop computer over the power rails of the Universal Serial Bus (USB) interface.") and 5:39-52 ("Under normal USB protocol, coupling of USB devices requires a series of USB handshaking protocols to identify both the host or master devices . . . . It will be

[3] The '021 Application to which the '550 Patent claims priority also refers to the VBUS line as "power lines" or "rails." *See e.g.*, Ex. 1008 ('021 Application) at 20.

understood that this handshaking protocol between the laptop computer 100 and the docking station 200 occurs over the serial communication lines 126, and these lines are not shown in Figure 2."); Baker, ¶ 151.



Dougherty at Figure 2 (annotated).

Accordingly, a POSITA would have understood that Dougherty in view of the USB 1.1 Specification discloses an adapter comprising "a USB V_{BUS} line and a USB communication path" as required by Claim 1.

c. 1[c] said adapter configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification

Dougherty in view of USB 1.1 discloses that the dock (an adapter) "is configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification." Baker, ¶¶ 152-155. Indeed, Dougherty expressly discloses that the system "breaks the standard USB protocol." Dougherty

at 6:1. It does so by, for example, supplying more than 500 mA of current to the connected laptop and supplying current at its upstream port.

As noted above, supplying no more than 500 mA to a single device is a "condition"/"limitation" specified in the USB 1.1. Specification. *See* Section V.A:

Table 7-5. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage:					
High-power Port	VBUS	Note 2, Section 7.2.1	4.75	5.25	V
Low-power Port	VBUS	Note 2, Section 7.2.1	4.40	5.25	V
Supply Current:					
High-power Hub Port (out)	ICCPRT	Section 7.2.1	500		mA
Low-power Hub Port (out)	ICCUPT	Section 7.2.1	100		mA
High-power Function (in)	ICCHPF	Section 7.2.1		500	mA
Low-power Function (in)	ICCLPF	Section 7.2.1		100	mA
Unconfigured Function/Hub (in)	ICCINIT	Section 7.2.1.4		100	mA
Suspended High-power Device	ICCSH	Section 7.2.3 ; Note 15		2.5	mA
Suspended Low-power Device	ICCSL	Section 7.2.3		500	µA

See e.g. USB 1.1 Table 7-5 (annotated) and 34 (noting that "[a] unit load is defined to be 100mA" and that "[a] device may be either low-power at one unit load or high-power, consuming up to five unit loads."); Baker, ¶ 153. Indeed, the '550 Patent specifically discloses in dependent claims that "a current limit" can be a "condition" and that a "current limit of 500 mA" is one such limit in the USB Specification. Ex. 1001 ('550 Patent) at Claim 2 ("The adapter of claim 1, wherein said associated condition is a current limit"); *id.* at Claim 9 ("The adapter of claim 2, wherein said current limit is 500 mA.").

Dougherty discloses supplying current to the laptop without regard to this 500 mA current limit of the USB 1.1 Specification. Specifically, Dougherty discloses

supplying as much as 2.5 amps (five times the current limit) to the laptop in order to charge the laptop. Dougherty at 7:15-18 ("Laptop computer 100 preferably operates using the 18 volt power supplied by the docking station 200 across the USB interface. Also, the laptop computer may charge its battery, if needed, with this same supply."); *id.* at 7:47 ("When the dock station 200 provides full power for full operation of the laptop computer 100, as many as 2.5 amps of current may flow from the dock station 200 to the laptop computer 100 across the USB connectors 136, 236.") Because Dougherty supplies current to a device in excess of the 500 mA limit of the USB 1.1 Specification, a POSITA would have understood that it discloses "said adapter configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification." Baker, ¶ 154.

The USB 1.1 Specification also provides that a device shall not supply current at its upstream port. *See e.g.*, USB 1.1 at 135 ("No device shall supply (source) current on the V_{BUS} at its upstream port at any time."). A POSITA would understand that this constitutes a "condition specified in a USB specification" as claimed in Claim 1. Baker, ¶ 155.

Dougherty, however, discloses that the laptop 100 and the docking station 200 are connected in a configuration in which the laptop is a host and the docking station is a hub. Dougherty at 2:55-3:3 and 5:39-43 ("Under normal USB protocol, coupling of USB devices requires a series of USB handshaking protocols to identify both the

host or master device, which would be the laptop computer 100, and any downstream device, which in this exemplary case is the docking station 200.") (emphasis added); *see also* USB 1.1 Specification at 6 (defining "Host" as the "host computer system where the USB Host Controller is installed. This includes the host hardware platform (CPU, bus, etc.) and the operating system in use.") Accordingly, the docking station is supplying power at its "upstream" port. *See e.g.*, USB 1.1 at 10 (defining "upstream" as "[t]he direction of data that flows towards the host. An upstream port is the port on a device electrically closest to the host that generates upstream traffic from the hub. Upstream ports receive downstream data traffic."); Baker, ¶ 155. As noted above, this is inconsistent with the USB Specification.

For each of these reasons, a POSITA would have understood that Dougherty in view of the USB 1.1 Specification discloses that the dock of Dougherty (the adapter) is "configured to supply current on the V_{BUS} line without regard to at least one associated condition specified in a USB specification."

2. Claim 2: The adapter of claim 1, wherein said associated condition is a current limit

Dougherty in view of the USB 1.1 Specification discloses this limitation. Baker, ¶¶ 153-156. Indeed, as explained above with respect to claim element 1[c], Dougherty discloses a dock (adapter) that supplies current to a laptop device at up to 2.5 amps, which is five times the amount of current that may be drawn by such a device under the USB 1.1 Specification. Accordingly, Dougherty in view of the

USB 1.1 Specification renders obvious that the "associated condition" of Claim 1 is a current limit.

3. Claim 9: The adapter of claim 2 wherein said current limit is 500 mA.

As explained above, Dougherty in view of the USB 1.1 Specification discloses the adapter of claim 1. Dougherty in view of the USB 1.1 Specification also renders obvious that "said current limit is 500 mA." Baker, ¶¶ 153-157. Indeed, as explained above with respect to claim element 1[c], Dougherty discloses a dock (adapter) that supplies current to a laptop device at up to 2.5 amps, which is five times the amount of current that may be drawn by such a device under the USB 1.1 Specification (i.e., 500 mA). Accordingly, Dougherty in view of the USB 1.1 Specification renders obvious that the "associated condition" of Claim 1 is a current limit of 500 mA as required by Claim 9.

4. Claim 10:

a. 10[a] An adapter comprising

As explained with respect to claim element 1[a], Dougherty in view of the USB 1.1 Specification discloses an adapter. *See* Section VIII.B.1.a.

b. 10[b] a USB V_{BUS} line and a USB communication path

As explained with respect to claim element 1[b], Dougherty in view of the USB 1.1 Specification discloses an adapter comprising "V_{BUS} line and a USB communication path." *See* Section VIII.B.1.b.

c. 10[c] said adapter configured to supply current on the V_{BUS} line without regard to at least one USB Specification imposed limit.

Dougherty in view of USB 1.1 discloses that "said adapter configured to supply current on the V_{BUS} line without regard to at least one USB Specification imposed limit." As explained with respect to claim element 1[c], Dougherty in view of the USB 1.1 Specification discloses an adapter configured to supply up to 2.5 amps of current on the V_{BUS} line to a to a laptop device, which is in excess of the amount of current that may be supplied to such a device under the USB 1.1 Specification (500 mA). *See* Section VIII.B.1.c. Similarly, Dougherty discloses that the dock supplies current at its upstream facing port, which is contrary to portions of the USB 1.1 specification limiting the direction in which current may flow. *Id.*

Accordingly, a POSITA would have understood that the dock of Dougherty (adapter) is "configured to supply current on the V_{BUS} line without regard to at least one USB Specification imposed limit."

5. Claim 11: The adapter of claim 10 wherein said USB Specification imposed limit is a current limit

As explained above, Dougherty in view of the USB 1.1 Specification discloses the adapter of claim 10.

Moreover, As explained with respect to claim element 1[c] and claim 2, Dougherty in view of USB 1.1 discloses an adapter configured to supply up to 2.5 amps of current on the V_{BUS} line to a to a laptop device, which is in excess of the

amount of current that may be supplied to or drawn by such device under the USB 1.1 Specification (500 mA). *See* Sections VIII.B.1-2. Accordingly, a POSITA would have understood that the "USB Specification imposed limit" of Claim 10 is a current limit.

6. Claim 18: The adapter of claim 11 wherein said current limit is 500 mA.

As explained above, Dougherty in view of the USB 1.1 Specification discloses the adapter of claim 11.

Moreover, as explained with respect to claim element 1[c] and claim 9, Dougherty in view of the USB 1.1 Specification discloses an adapter configured to supply up to 2.5 amps of current on the V_{BUS} line to a to a laptop device, which is in excess of the amount of current that may be supplied to or drawn by such device under the USB 1.1 Specification (500 mA). *See* Sections VIII.B.1-3. Accordingly, a POSITA would have understood that the "USB Specification Imposed Limit" of Claim 10 is a current limit of 500 mA.

IX. CONCLUSION

For the foregoing reasons, there is a reasonable likelihood that Petitioners will prevail as to the Challenged Claims of the '550 Patent. Accordingly, *inter partes* review of claims 1-18 is requested.

Dated: January 13, 2021

Respectfully submitted,

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X. MANDATORY NOTICES – 37 C.F.R. §42.8

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The real parties-in-interest in this Petition are TCT Mobile (US), Inc.; TCT Mobile (US) Holdings, Inc.; Huizhou TCL Mobile Communication Co. Ltd.; and TCL Communication, Inc. Petitioners certify that no other party exercised control or could exercise control over Petitioners' participation in this proceeding, the filing of this Petition, or the conduct of any ensuing trial.

B. Related Matters (37 C.F.R. §42.8(b)(2))

To the best knowledge of the Petitioner, the '550 Patent is involved in the following litigation as of the filing date of this Petition:

- *Fundamental Innovation Systems International LLC v. Coolpad Group Limited et al.,* Case No. 2-20-cv-00117, Eastern District of Texas.
- *Fundamental Innovation Systems International LLC v. Belkin, Inc. et al.,* Case No. 1-20-cv-00550, District of Delaware.
- *Fundamental Innovation Systems International LLC v. Lenovo (United States) Inc. et al.,* Case No. 1-20-cv-00551, District of Delaware.
- *Fundamental Innovation Systems International LLC v. TCT Mobile (US) Inc. et al,* Case No. 1-20-cv-00552, District of Delaware. Petitioner is the named Defendant in this pending case. Petitioners

were served with the complaint in this action on April 23, 2020, and thus this Petition is timely under 35 U.S.C. §315(b).

C. Lead/Back-up Counsel (37 C.F.R. §42.8(b)(3))

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Petitioners consent to service by electronic mail at the following addresses: 3J6PTABDocket@orrick.com, R75PTABDocket@orrick.com, and TCL-FISI_OHS@orrick.com. Petitioners' Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioners to the deposit account of Orrick, Herrington & Sutcliffe LLP: 15-0665.

D. Service Information (37 C.F.R. §42.8(b)(4))

Please direct all correspondence to lead and backup counsel at the above address. Petitioners consent to electronic service at the email addresses above.

XI. GROUNDS FOR STANDING – 37 C.F.R. §42.104(A)

Petitioner certifies that: (i) the '550 Patent is available for IPR and (ii) Petitioner is not barred or estopped from requesting an IPR challenging the '550 patent's claims. Specifically, Petitioner certifies that: (1) no Petitioner entity or real party-in-interest has filed a civil action challenging the validity of any claim of the '550 patent; (2) Petitioner filed this petition within one year of the date they were served with a complaint asserting infringement of the '550 patent; and (3) the estoppel provisions of 35 U.S.C. § 315(e)(1) do not prohibit this IPR.

XII. FEES – 37 C.F.R. §42.15(A)

The Office is authorized to charge the filing fee and any other necessary fees that might be due in connection with this Petition to Deposit Account No. 15-0665 for the fees set forth in 37 C.F.R. §42.15(a).

CERTIFICATE OF COMPLIANCE – 37 CFR § 42.24

Pursuant to 37 C.F.R. §42.24 *et seq*., the undersigned certifies that this document complies with the type-volume limitations. The substance of this document (*i.e.,* excluding table of contents, table of authorities, mandatory notices, listing of exhibits, and certificates of service and word count) contains 13,469 words as calculated by the "Word Count" feature of Microsoft Word Office 365, the word processing program used to create it.

Dated: January 13, 2021

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CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§42.6(e), 42.8(b)(4) and 42.105, the undersigned certifies that on January 13, 2021, a complete and entire copy of this Petition for *Inter Partes* Review of U.S. Patent 8,624,550 and all supporting documents and exhibits were served via Federal Express, postage prepaid, on the Patent Owner by serving the correspondence address of record for the '550 Patent:

BOTOS CHURCHILL IP LAW LLP
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A courtesy copy was provided on January 13, 2021 to Patent Owner's litigation counsel in the action *Fundamental Innovation Systems International LLC v. TCT Mobile (US), Inc.; TCT Mobile (US) Holdings, Inc.; Huizhou TCL Mobile Communication Co. Ltd.; and TCL Communication, Inc.*, District of Delaware Case No. 1:20-cv-00552, pending between Petitioners and Patent Owner and involving the '111 Patent:

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