UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

PICTOS TECHNOLOGIES, INC.
Patent Owner

Patent No. 6,838,651

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 6,838,651

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner" or "Samsung") requests *inter partes* review of claims 13-15 ("the challenged claims") of U.S. Patent No. 6,838,651 ("the '651 patent") (Ex. 1001), which, according to PTO records, is assigned to Pictos Technologies Inc. ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '651 patent is at issue in *In the Matter of Certain Digital Imaging Devices and Products Containing the Same and Components Thereof*, Inv. No. 337-TA-1231, International Trade Commission ("the ITC Investigation").

The '651 patent was previously at issue in:

- *Imperium (IP) Holdings, Inc.*[1] *v. Apple Inc., et al.*, No. 4:11-cv-00163 (E.D. Tex.) (terminated) ("*Imperium II*");

[1] Patent Owner was formerly known as Imperium IP Holdings (Cayman) Ltd. (Ex. 1017, 1.)

- *Imperium (IP) Holdings, Inc. v. Apple Inc., et al.*, No. 6:11-cv-00128 (E.D. Tex.) (terminated) ("*Imperium I*").

Petitioner has filed another IPR petition challenging claims 1-5 and 18-22 of the '651 patent (IPR2021-00437.)

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Phillip Citroën (Reg. No. 66,541). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-Pictos-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '651 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 13-15 should be canceled as unpatentable based on the following grounds:

Ground 1: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 102(b) as anticipated by Japanese Patent Publication 2000-12819 to Isogai *et al.* ("*Isogai*") (Ex. 1005)[2];

Ground 2: Claims 14-15 are unpatentable under § 103(a) as being obvious over *Isogai* and U.S. Patent No. 7,133,073 to Neter ("*Neter*") (Ex. 1007);

Ground 3: Claims 14-15 are unpatentable under § 103(a) as being obvious over *Isogai* and U.S. Patent No. 6,704,049 to Fossum *et al.* ("*Fossum*") (Ex. 1008);

Ground 4: Claim 13 is unpatentable under § 102(b) as being anticipated by U.S. Patent No. 5,982,984 to Inuiya *et al.* ("*Inuiya*") (Ex. 1006);

Ground 5: Claims 14-15 are unpatentable under § 103(a) as being obvious over *Inuiya* and *Neter*; and

Ground 6: Claims 14-15 are unpatentable under § 103(a) as being obvious over *Inuiya* and *Fossum*.

[2] Ex. 1005 is a compilation containing the English-language translation of *Isogai* (Ex. 1005, 1-17), followed by the Japanese language version (*id.*, 18-34) and an affidavit required by 37 C.F.R. § 42.63(b) (in the form of a declaration as permitted by 37 C.F.R. § 42.2) (*id.*, 35).

The '651 patent issued January 4, 2005, from U.S. App. No. 10/113,545, filed March 28, 2002. *Isogai* was published on January 14, 2000. *Inuiya* issued November 9, 1999, from U.S. App. No. 08/594,598, filed January 31, 1996. Thus, *Isogai* and *Inuiya* qualify as prior art to the '651 patent at least under pre-AIA 35 U.S.C. § 102(b). *Fossum* issued March 9, 2004, from U.S. App. No. 09/028,961, filed February 23, 1998. *Neter* issued November 7, 2006, from U.S. App. No. 09/496,607, filed February 2, 2000. Thus, *Fossum* and *Neter* qualify as prior art to the '651 patent at least under pre-AIA 35 U.S.C. § 102(e). None of these references were considered during prosecution. (*See generally* Ex. 1004.)

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '651 patent ("POSITA") would have had a bachelor's degree in electrical engineering, computer science, or the equivalent, and two or more years of experience with image processing. (Ex. 1002, ¶¶20-21)[3] More education can supplement practical experience and vice versa. (*Id.*)

[3] Petitioner submits the declaration of Dr. R. Jacob Baker, PH.D., P.E. (Ex. 1002), an expert in the field of the '651 patent. (Ex. 1002, ¶¶5-15; Ex. 1003.)

VII. THE '651 PATENT

The '651 patent "relates generally to solid-state imaging devices" "implementing multiple analog-to-digital ('A/D') converters to obtain high frame rates." (Ex. 1001, 1:6-11; Ex. 1002, ¶¶27-29.) The '651 patent states that the imaging device has "four color channels (one red, one blue and two greens) used to define a color image based upon the Bayer Pattern of color filters." (Ex. 1001, 3:1-4.) The '651 patent discloses that "two A/D converters may be employed, where one A/D converter is used for the red and blue channels and the second A/D converter is used for the green channels." (*Id*., 3:8-10.)

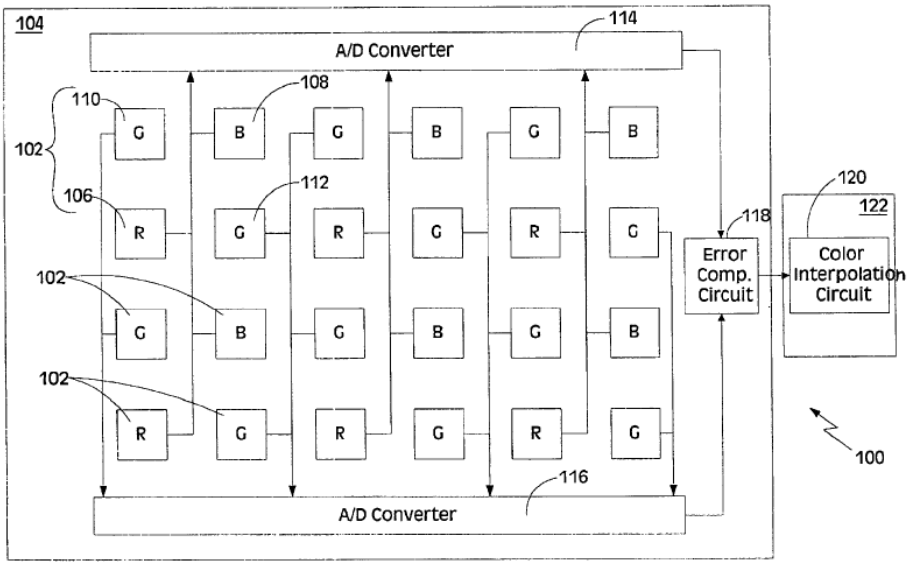


FIG. 1

(Ex. 1001, FIG. 1.)

An error compensation circuit 118 "provides an independent gain to correct the gain for each color channel" and "provides an independent offset to correct the fixed pattern noise offset for each color channel." (*Id*., 5:3-7.) "The color interpolation circuit 120 performs the interpolation for each pixel 102 to determine the color of the pixel," where "[t]he color interpolation circuit 120 may be located on a second chip 122, as shown in FIG 1" or "may be located on chip 104." (*Id*., 5: 23-27.)

VIII. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard," as set forth in *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). *See* 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶30.)

IX. DETAILED EXPLANATION OF GROUNDS[4]

A. Ground 1: Claim 13 Is Anticipated by *Isogai*

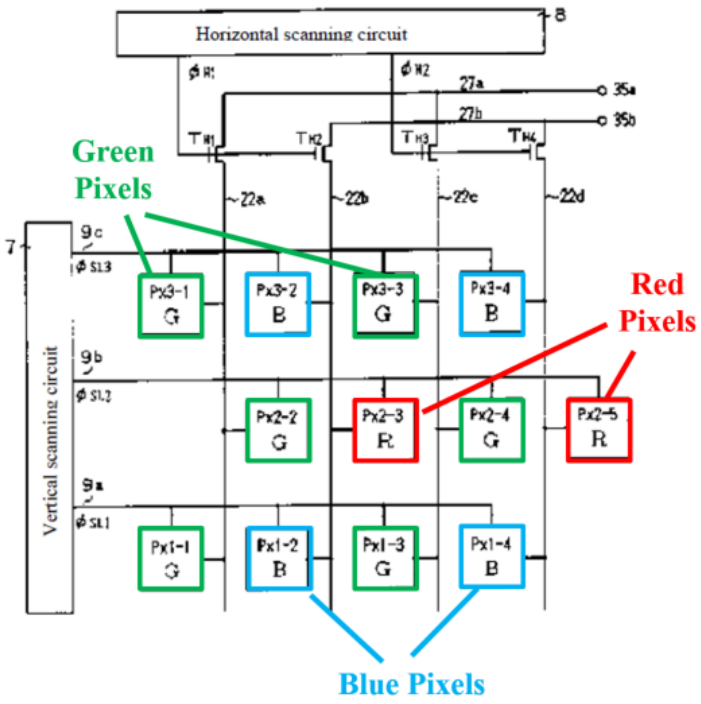
1. Claim 13

a) A solid state imaging device, comprising:

To the extent the preamble of claim 13 is limiting, *Isogai* discloses the limitations therein. (Ex. 1002, ¶¶42-46.) For instance, *Isogai* discloses a "solid-state image sensing element having a parallel output configuration," where "a signal of a specified pixel arranged in a checkered pattern is output to one of two horizontal signal lines." (Ex. 1005, Abstract; *see also id*., ¶[0001]; Ex. 1002, ¶42.) Annotated figure 1 of *Isogai* below shows a solid state image sensing element that includes an array of pixels. (Ex. 1005, ¶[0026], FIG. 1.)

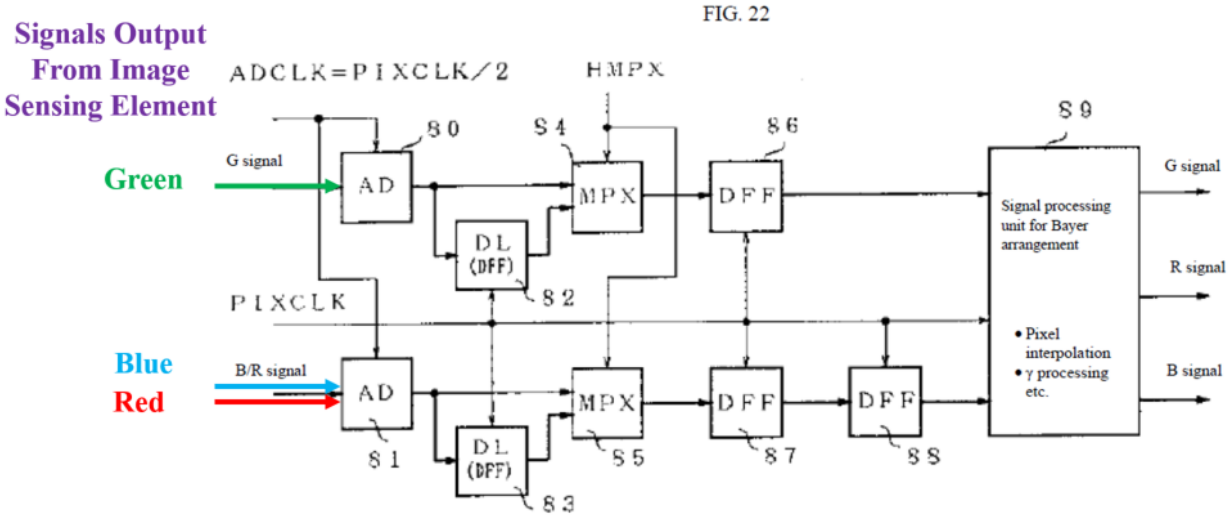
[4] Section IX below references exhibits other than the identified prior art for each ground. Such exhibits reflect the state of the art known to a POSITA at the time of the alleged invention consistent with the testimony of Dr. R. Jacob Baker, PH.D., P.E.

FIG. 1



(*Id*., FIG. 1 (annotated); Ex. 1002, ¶43.)

Isogai also discloses a system for processing the signal outputs from the solid-state imaging sensing elements. (Ex. 1005, ¶¶[0077]-[0078], FIG. 22.) The processing system, shown in annotated figure 22 below, receives inputs from the disclosed solid-state image sensing elements and performs color imaging. (*Id*., ¶[0078], FIG. 22; Ex. 1002, ¶45.)



(Ex. 1005, FIG. 22 (annotated); Ex. 1002, ¶45.)

The combination of the solid-stage image sensing element shown in figure 1 with the processing system shown in figure 22 constitutes a "solid state imaging device" as recited in claim 1. (Ex. 1002, ¶46.)

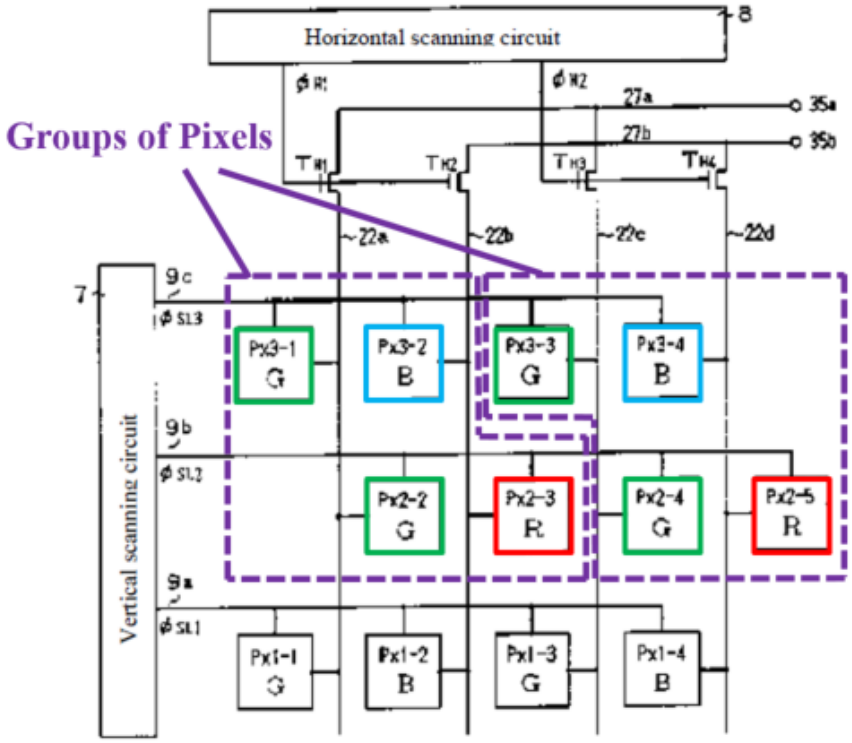
b) groups of pixels, wherein each said group of pixels include:

a red pixel having an output;
a blue pixel having an output;
a first green pixel having an output; and
a second green pixel having an output;

Isogai discloses these limitations. (Ex. 1002, ¶¶47-53.) Like the '651 patent, *Isogai's* "solid state imaging device" includes groups of pixels arranged in a Bayer pattern, where each group includes a red pixel, a blue pixel, a first green pixel, and

a second green pixel. (*Id*., ¶47.) For example, annotated figure 1 of *Isogai* below shows red, green, and blue pixels arranged in the checkered "Bayer" pattern where two green pixels are included for each red and blue pixel. (*Id*.; Ex. 1005, ¶[0009], ("In the arrangement shown in FIG. 28, the green (G) color filters are arranged in a checkered pattern, and the red (R) and blue (B) color filters are line-sequentially arranged corresponding to the remaining pixels (generally called a Bayer array)."), ¶[0028], ("Further, green (G) color filters are provided in a checkered pattern and arranged on the corresponding pixels (Px1-1, Px1-3, Px2-2, Px2-4, Px3-1, Px3-3). Red (R) and blue (B) color filters are arranged line-sequentially (Bayer arrangement) on the remaining pixels."), FIG. 1.)

FIG. 1



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶47.)

Isogai's groups of pixels, each of which includes a red pixel, a blue pixel, a first green pixel, and a second green pixel, are consistent with the disclosure of the '651 patent. (Ex. 1002, ¶¶48-49.) For example, annotated figure 1 of the '651 patent below shows groups of pixels with a red pixel, a blue pixel, and two green pixels arranged in the checkered "Bayer" pattern. (*Id.*; Ex. 1001, 3:1-4 ("There are four color channels (one red, one blue, and two greens) used to define a color image based on the Bayer Pattern of color filters."), 4:51-61 ("The solid state imaging device of the present invention defines a color image based upon the Bayer pattern of color

filters. In particular, the imager system comprises green pixels 110, 112 in checkerboard pattern. Thus, the green pixels 110, 112 exist in both odd rows (110) and even rows (112). The blue pixels 108 are shown alternating with the green pixels 110 in the odd rows, and the red pixels 106 are shown alternating with the green pixels 110 in the even rows. Alternatively, the blue pixels 108 may alternate with the green pixels 112 in the even rows and the red pixels 106 may alternate with the green pixels 110 in the odd rows."), FIG. 1.)

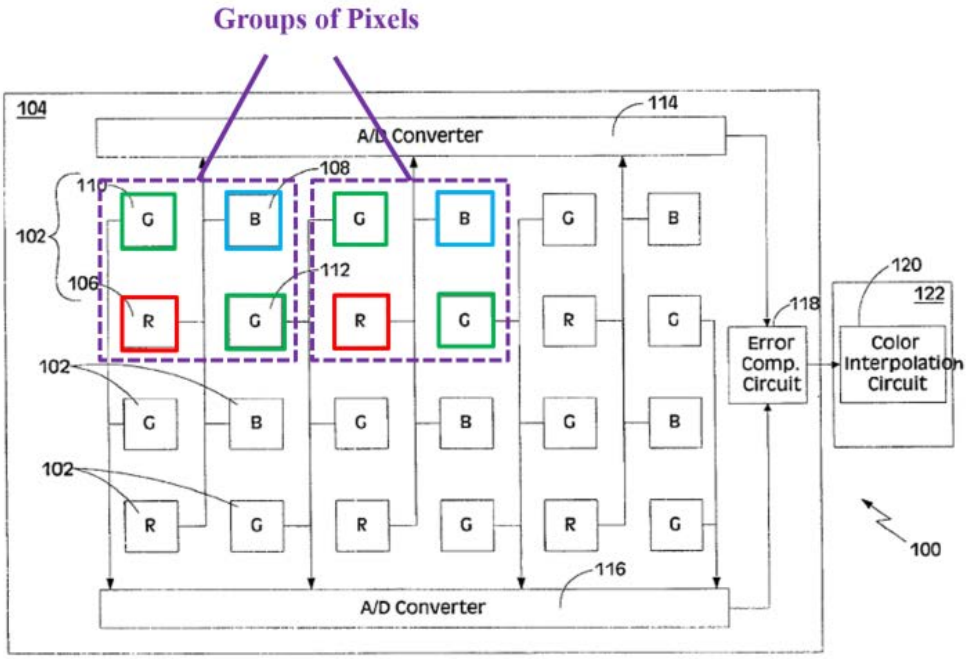
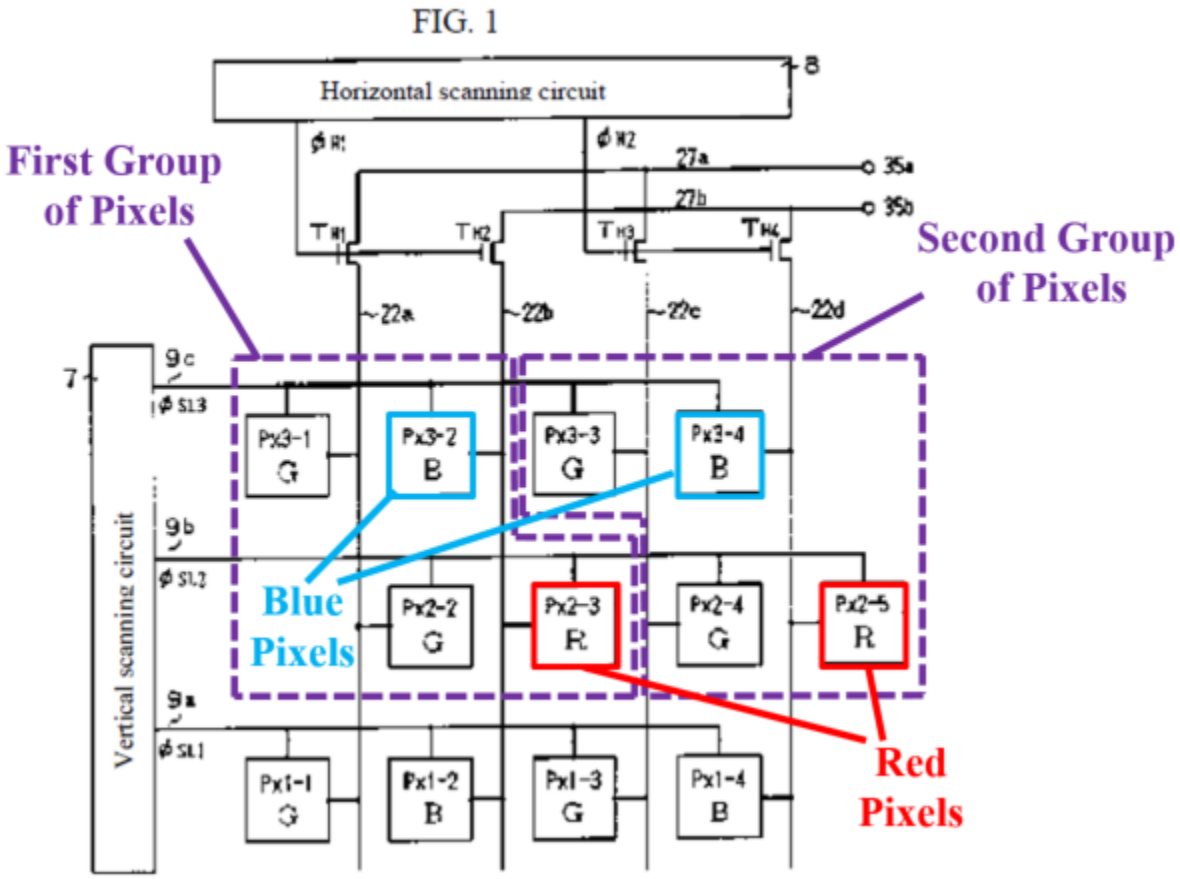


FIG. 1

(Ex. 1001, FIG. 1 (annotated); Ex. 1002, ¶48.)

Isogai further discloses that each of the red, blue, first green, and second green pixels in each group of pixels includes a respective output. (Ex. 1002, ¶¶50-53.) For

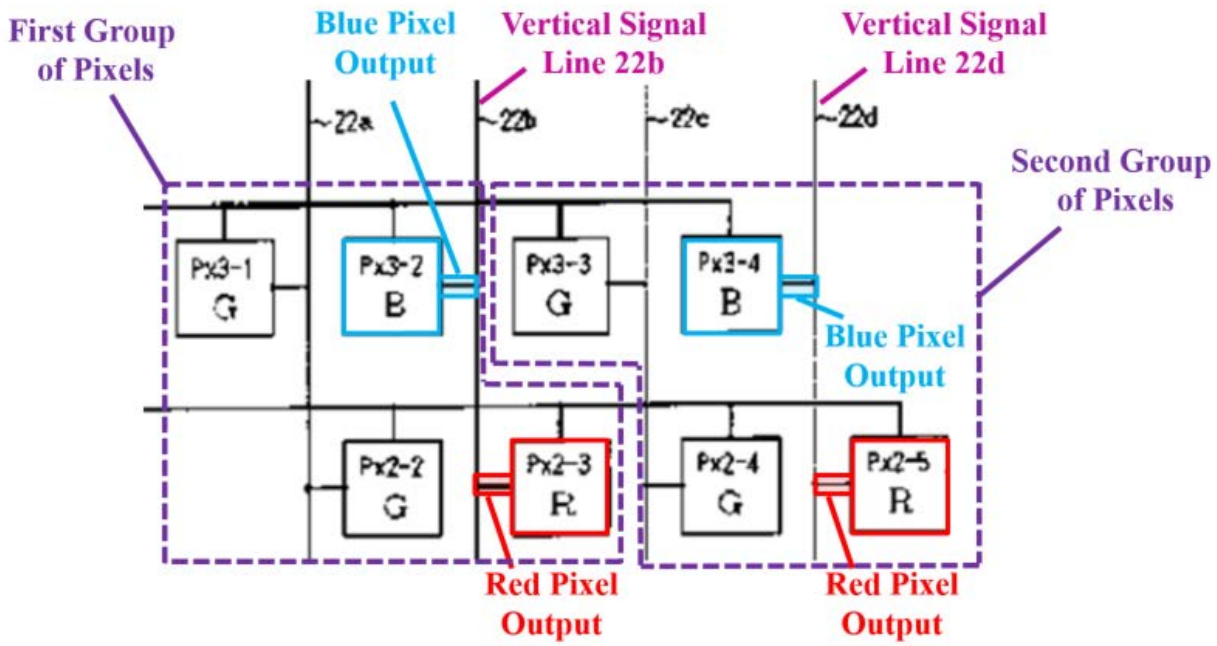
example, as shown in annotated figure 1 below, a first group of pixels includes red pixel Px2-3 and blue pixel Px3-2, whereas a second group of pixels includes red pixel Px2-5 and blue pixel Px3-4. (Ex. 1005, ¶[0028], FIG. 1; Ex. 1002, ¶50.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶50.)

Each of the red and blue pixels highlighted above has an output. (Ex. 1002, ¶51.) *Isogai* discloses that vertical signal lines 22a-22d are used to connect alternating columns of pixels to either the first horizontal signal line 27a or the second horizontal signal line 27b. (Ex. 1005, ¶¶[0025], [0027], FIG. 1.) The outputs

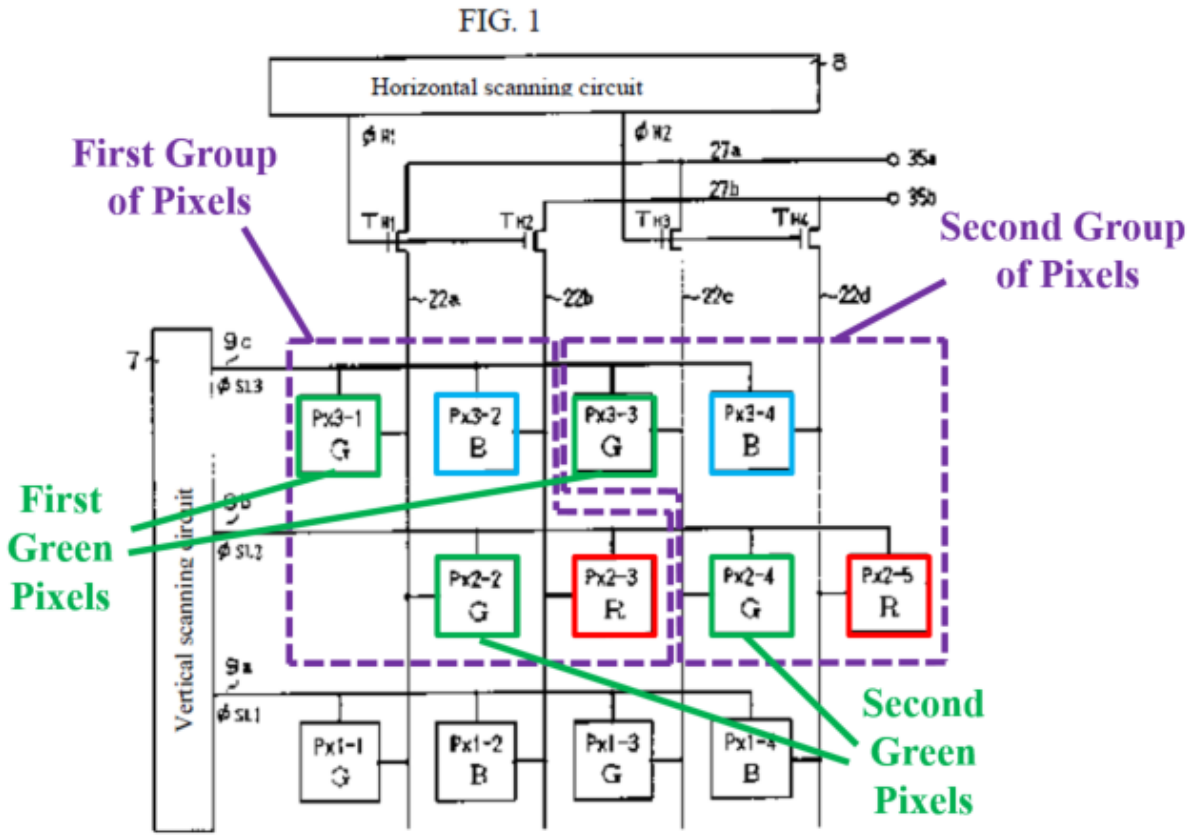
from the pixels are routed from the vertical signal lines to the horizontal signal lines and then output by the output terminals 35a and 35b. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1.) As shown in the annotated and enlarged excerpt of figure 1 below, each of the red pixel Px2-3 and the blue pixel Px3-2 has an output that connects to the vertical signal line 22b, whereas each of the red pixel Px2-5 and the blue pixel Px3-4 has an output that connects to the vertical signal line 22d. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1; Ex. 1002, ¶51.)



(Ex. 1005, FIG. 1 (excerpt, annotated); Ex. 1002, ¶51.)

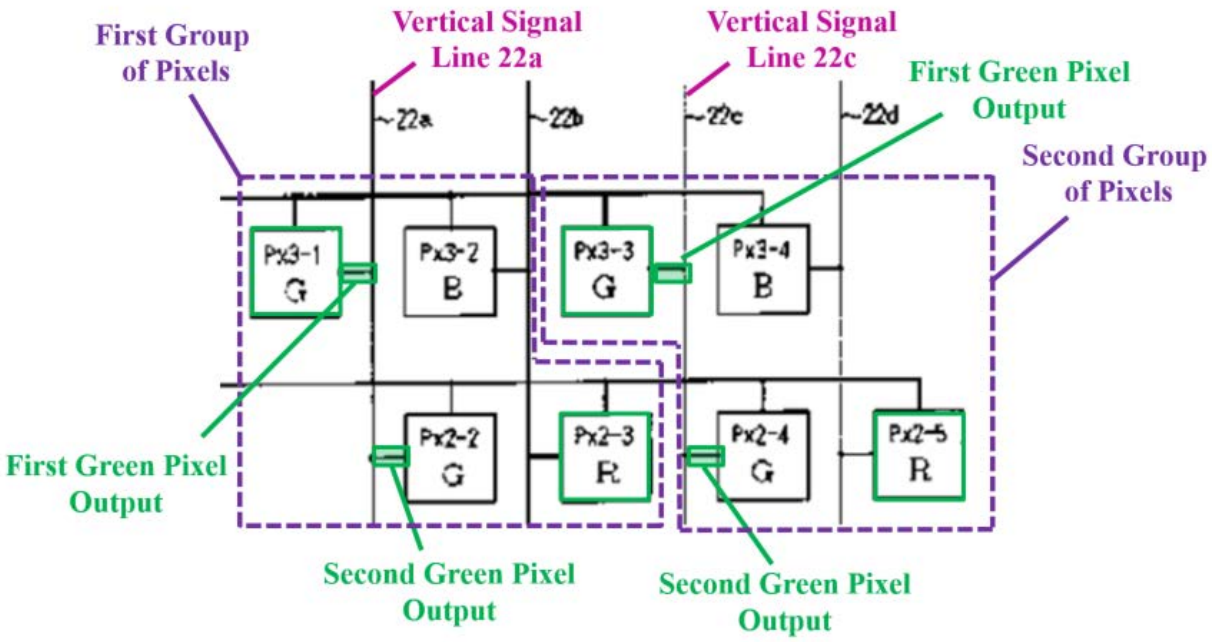
Similarly, each of the green pixels in each of the groups of pixels has an output. (Ex. 1002, ¶52.) As shown in annotated figure 1 below, the first group of pixels includes first green pixel Px3-1 and second green pixel Px2-2, whereas the

second group of pixels includes first green pixel Px3-3 and second green pixel Px2-4. (Ex. 1005, ¶[0028], FIG. 1; Ex. 1002, ¶52.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶52.)

As shown in the annotated and enlarged excerpt of figure 1 below, each of green pixels Px3-1 and Px2-2 has an output that connects to the vertical signal line 22a, whereas each of green pixels Px3-3 and Px2-4 has an output that connects to the vertical signal line 22c. (*Id.*, ¶¶[0025], [0027]-[0029], FIG. 1; Ex. 1002, ¶53.)



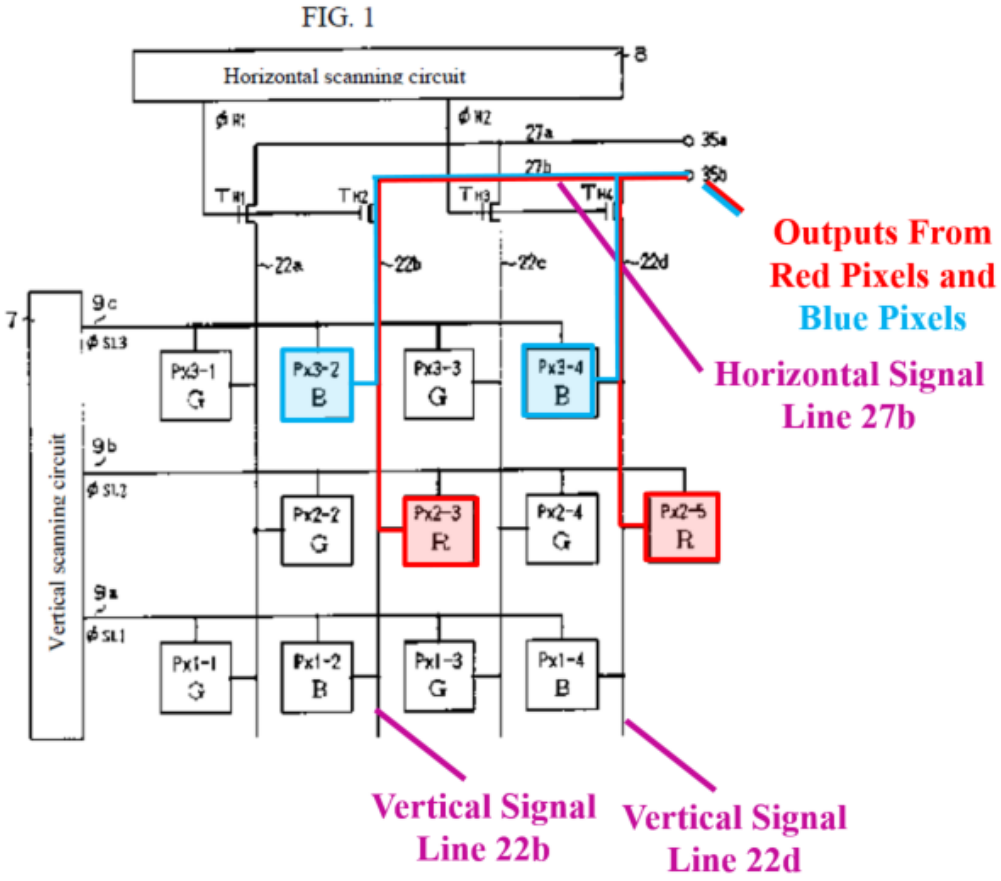
(Ex. 1005, FIG. 1 (excerpt, annotated); Ex. 1002, ¶53.)

c) a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixels into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixels into a second digital signal;

Isogai discloses these limitations. (Ex. 1002, ¶¶54-63.)[5] As discussed above in Section IX.A.1(b), the outputs of the red pixels and blue pixels are connected to the vertical signal lines 22b and 22d, whereas as the outputs of the green pixels are connected to the vertical signal lines 22a and 22c. (Ex. 1005, ¶[0027], FIG. 1; *supra*

[5] Petitioner reserves the right to challenge the claims-at-issue here under 35 U.S.C. § 112, as appropriate, in other proceedings.

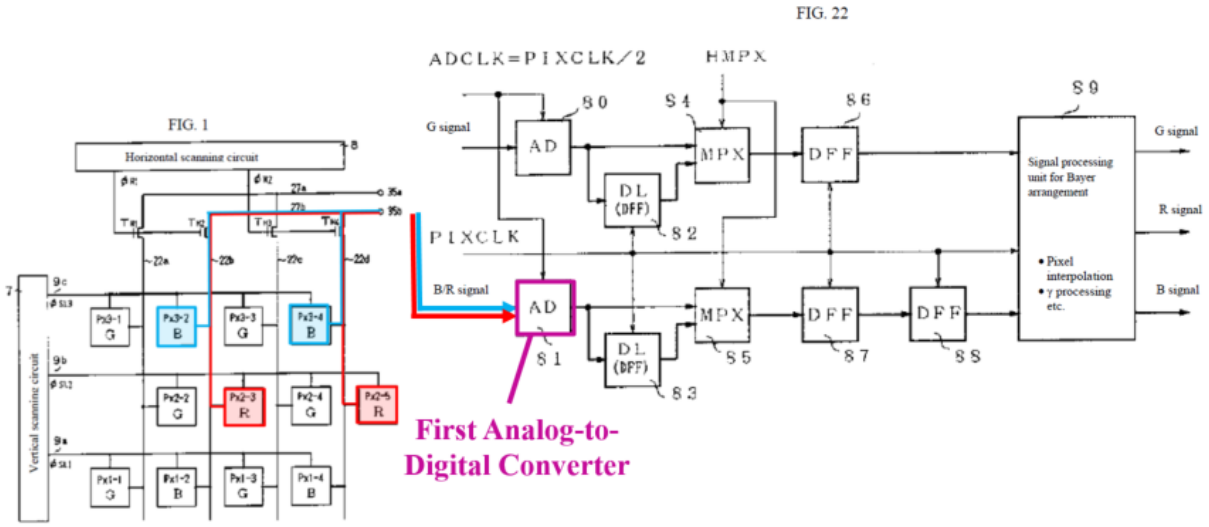
section IX.A.1(b).) As shown in annotated figure 1 below, the vertical signal lines 22b and 22d, which correspond to the red and blue pixels, are connected to horizontal signal line 27b. (*Id*., ¶¶[0027], [0029] ("Further the red (R) and blue (B) signals are output from the output terminal 35b via the other horizontal signal line 27b."), FIG. 1; Ex. 1002, ¶¶54-56.)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶54.)

As shown in the demonstrative below, the output signals corresponding to the horizontal signal lines 27a and 27b are provided as inputs to the processing system

that is included in *Isogai's* "solid state imaging device" and shown in figure 22. (Ex. 1002, ¶57.)



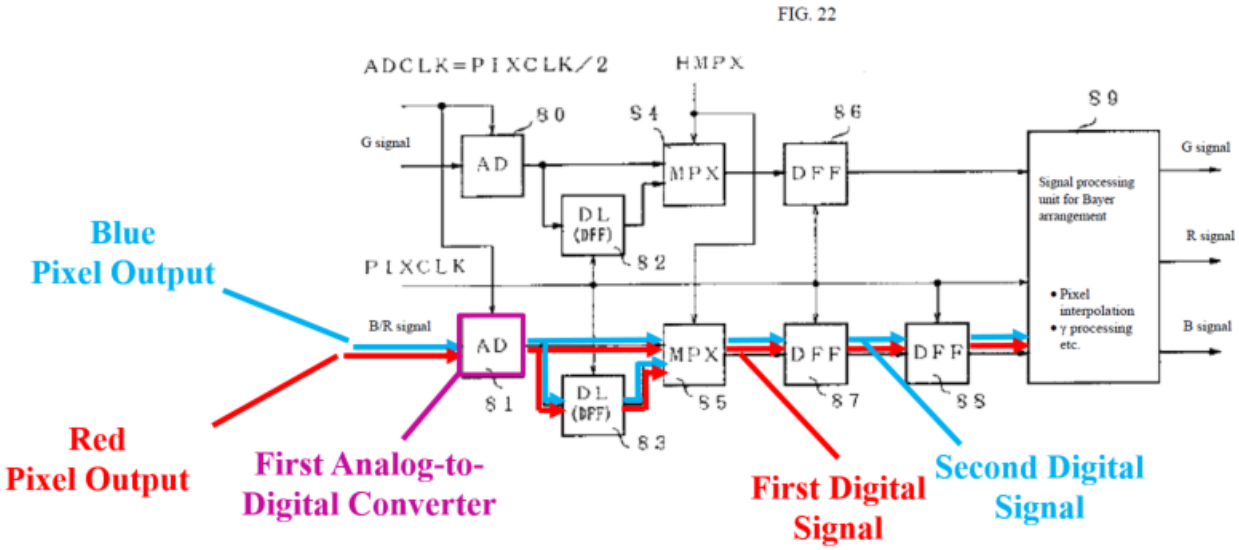
(*Id.*, FIGs. 1, 22 (annotated); Ex. 1002, ¶57.)

As shown above, the outputs of the red and blue pixels on the horizontal signal line 27b are provided as the "B/R signal" to the analog-to-digital converter (AD) 81. (Ex. 1005, ¶¶[0079], [0080]; Ex. 1002, ¶58.) A POSITA would have understood that AD blocks 80 and 81, which are further identified in the "Explanation of Reference Numerals" of *Isogai* as "80, 81 AD converter," are analog-to-digital (A/D) converters that are connected to the outputs of the pixels and convert those outputs into digital signals. (Ex. 1005, ¶[0079] ("The G signal . . . is AD-converted into the output signal" where the "A/D conversion frequency is 1/2 of PIXCLK."); Ex. 1002, ¶¶59-60.)

Isogai further discloses that the digital signals generated by the analog-to-digital converter 81 include a red digital signal (R signal) ("first digital signal") and a blue digital signal (B signal) ("second digital signal") that are "sequentially output" by AD 81. (*Id*., ¶[0079] ("This apparatus output the G signal as the first channel, and output the line sequential signals of R and B as the second channel."), ¶[0080] ("The second channel, in which the B signal and the R signal are output line sequentially."); Ex. 1002, ¶61.) A POSITA would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the horizontal scanning circuit 8 will control the column selection transistors TH2 and TH4 such that the blue pixel outputs for the first and second groups of pixels are sequentially provided from the vertical signal lines 22b and 22d to horizontal signal line 27b and then converted to the first digital signal by AD 81. (Ex. 1002, ¶61.) Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the red pixel outputs are sequentially provided from the vertical signal lines 22b and 22d to the horizontal signal line 27b and converted to the second digital signal by AD 81. (*Id*.) Thus, AD 81 will sequentially convert different red and blue pixel outputs into digital signals that are "sequentially output." (*Id*.; Ex. 1005, ¶¶[0079], [0080].)

Annotated figure 22 below shows that the signal path for the first (red) and second (blue) digital signals includes D-flip flops 83, 87, and 88, and multiplexer

85, where such elements control the timing of the presentation of the first and second digital signals to the signal processing unit 89. (Ex. 1005, ¶¶[0079], [0080], FIG. 22; Ex. 1002, ¶62.) The PIXCLK scanning clock controls the presentation of the red/blue digital pixel information to the processing block 89 by the D-flip flop (DFF) 88, whereas the HMPX signal selects which of the red/blue pixel digital signals that are sequentially output by AD 81 is forwarded to the DFF 87 using the multiplexer (MPX) 85. (Ex. 1005, ¶¶[0079], [0080], FIG. 22; Ex. 1002, ¶62.)



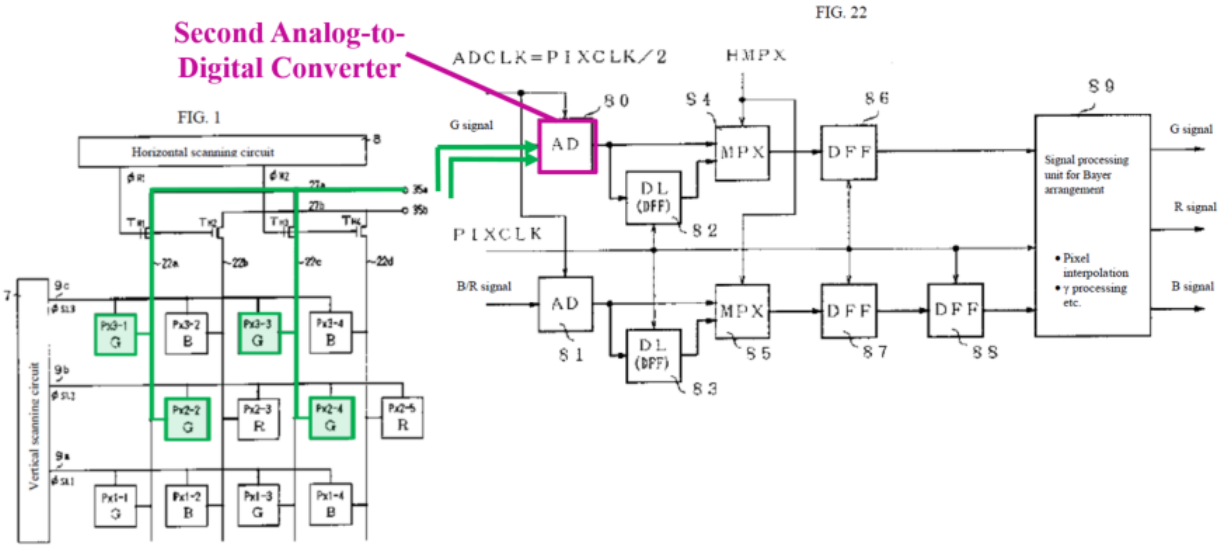
(*Id.*, FIG. 22 (annotated); Ex. 1002, ¶62.)

Analog-to-digital converter 81 constitutes "a first analog-to-digital converter" as recited in claim 13. (Ex. 1002, ¶63.)

d) a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixels into a third digital signal and connected to the output of the second green pixel for converting the output of the second green

pixels into a fourth digital signal; and

Isogai discloses these limitations. (Ex. 1002, ¶¶64-68.) Just as the analog-to-digital converter 81 converts the red and blue pixel outputs into digital signals, the analog-to-digital converter 80 is connected to and converts the outputs of the first and second green pixels on horizontal signal line 27a into digital signals. (*Supra* Section IX.A.1(c); *see also* Ex. 1005, ¶[0079], FIGs. 1, 22; Ex. 1002, ¶¶64-65.)

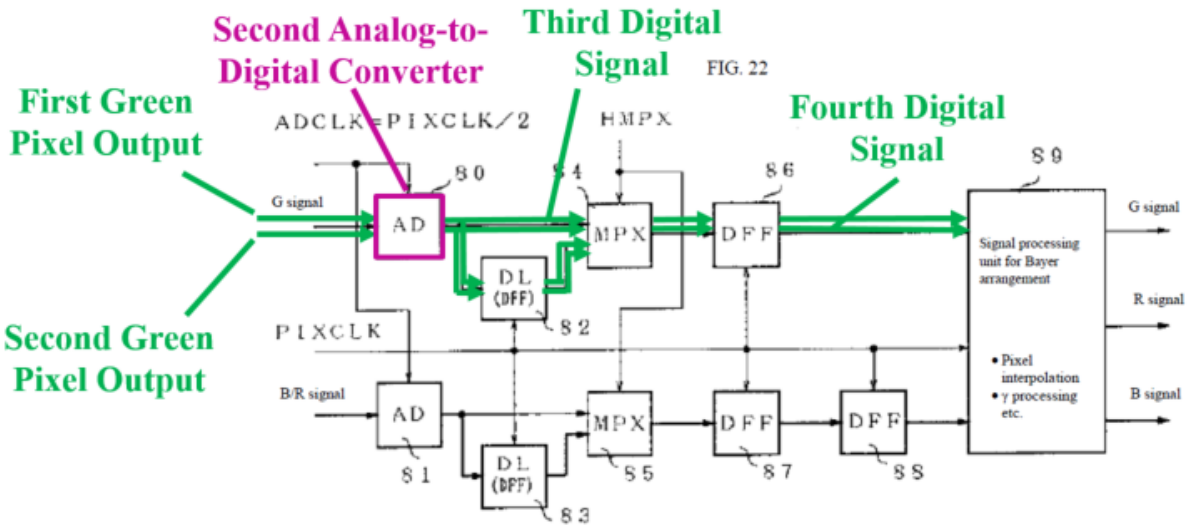


(Ex. 1005, FIGs. 1, 22 (annotated); Ex. 1002, ¶64.)

Isogai further discloses that the digital signals generated by the analog-to-digital converter 80 include first and second green digital signals (G signal) ("third digital signal" and "fourth digital signal"). (*Id.*, ¶[0079] ("The G signal . . . is AD-converted into the output signal" where the "A/D conversion frequency is 1/2 of PIXCLK."); Ex. 1002, ¶66.) A POSITA would have understood that when the row select signal 55c corresponding to the top row of pixels is asserted, the horizontal

scanning circuit 8 will control the column selection transistors TH1 and TH3 such that the first green pixel outputs for the first and second groups of pixels are sequentially provided from the vertical signal lines 22a and 22c to horizontal signal line 27a and then converted to the third digital signal by AD 80. (Ex. 1002, ¶66.) Similarly, when the row select signal 55b corresponding to the second row of pixels is asserted, the second green pixel outputs are sequentially provided from the vertical signal lines 22a and 22c to the horizontal signal line 27a and converted to the fourth digital signal by AD 80. (*Id*.) Thus, AD 80 will sequentially convert different green pixel outputs into two digital signals. (*Id*.; Ex.1005, ¶[0079].)

Annotated figure 22 below shows that the signal path for the third (first green) and fourth (second green) digital signals includes D-flip flops 82 and 86 as well as multiplexer 84, where such elements control the timing of the presentation of the third and fourth digital signals to the signal processing unit 89. (Ex. 1005, ¶[0079], FIG. 22; Ex. 1002, ¶67.) The PIXCLK scanning clock controls the presentation of the green digital pixel information to the processing block 89 by the D-flip flop (DFF) 86, whereas the HMPX signal selects which of the first/second green pixel digital signals that are sequentially output by AD 81 is forwarded to the DFF 86 using the multiplexer (MPX) 84.



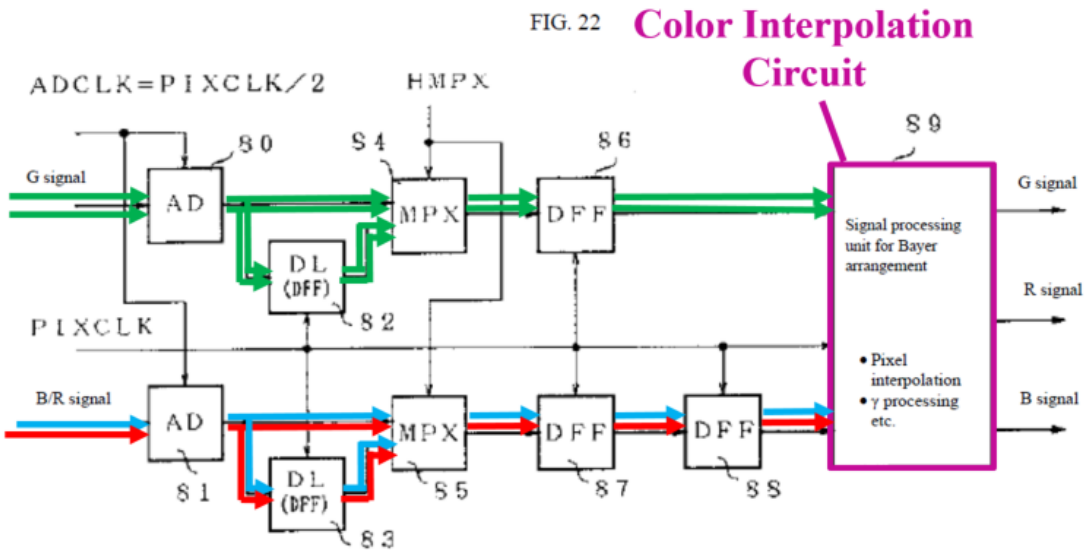
(*Id*., FIG. 22 (annotated); Ex. 1002, ¶67.)

Analog-to-digital converter 80 constitutes "a second analog-to-digital converter" as recited in claim 13. (Ex. 1002, ¶68.)

e) a color interpolation circuit for combining the first, second, third and fourth digital signals.

Isogai discloses this limitation. (Ex. 1002, ¶¶69-73.) For instance, *Isogai* discloses a signal processing unit 89 that combines the first, second, third, and fourth digital signals ("a color interpolation circuit for combining the first, second, third and fourth digital signals"). As discussed above in Sections IX.A.1(c)-(d), the analog-to-digital converters 80, 81 convert the outputs of red, blue, first green, and second green pixels into the first, second, third, and fourth digital signals, respectively. (*Supra* Sections IX.A.1(c)-(d).) *Isogai* further discloses that the first,

second, third, and fourth digital signals are provided to the signal processing unit 89. (Ex. 1005, ¶¶[0077]-[0080], FIG. 22; Ex. 1002, ¶69.)



(Ex. 1005, FIG. 22 (annotated); Ex. 1002, ¶69.)

Isogai discloses that the signal processing unit 89 performs signal processing on the digitized pixel outputs, including "**pixel interpolation** of empty grid points of each RGB color . . . to output RGB color signals with all pixels having RGB color signal." (Ex. 1005, ¶[0080] (emphasis added); Ex. 1002, ¶70.) Such pixel interpolation of empty grid points (unknown color data for a pixel) includes processing that combines the digital signals corresponding to the outputs of the pixels in a manner consistent with the disclosure of the '651 patent. (Ex. 1005, ¶[0078]; Ex. 1001, 5:13-16 ("Color interpolation is used to determine the amount of red, green and blue light incident on each pixel. This process averages the color

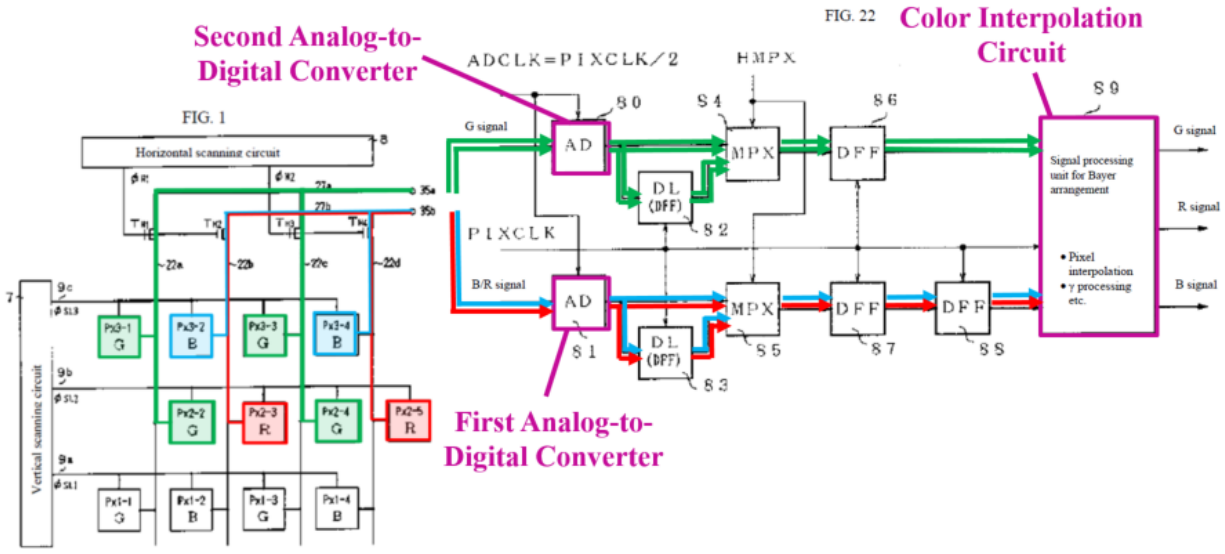
outputs of appropriate neighboring pixels to approximate each pixel's unknown color data."); Ex. 1002, ¶71.) For example, a POSITA would have understood that *Isogai's* disclosure of "pixel interpolation" would include combining color data corresponding to neighboring pixels in order to determine the pixel color data for the empty grid points as described by the '651 patent. (Ex. 1005, ¶[0080]; Ex. 1001, 5:13-25; Ex. 1002, ¶¶72-73.)

B. Ground 2: Claims 14-15 Are Obvious Over *Isogai* in View of *Neter*

1. Claim 14

a) The solid stage imaging device of claim 13 further comprising a first chip and a second chip, wherein the groups of pixels, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

The *Isogai-Neter* combination discloses or suggests these limitations. (Ex. 1002, ¶¶74-86.) As discussed above in Section IX.A.1(a), *Isogai* discloses a solid state imaging device that includes a solid state image sensing element as shown in figure 1 in combination with the processing system shown in figure 22. (*Supra* Section IX.A.1(a).)



(Ex. 1005, FIG. 1 (annotated); Ex. 1002, ¶74.)

Isogai does not explicitly disclose that the groups of red, blue, and green pixels are disposed on a first chip with the analog-to-digital converters, while the color interpolation circuit is disposed on a second chip as recited in claim 14. However, including groups of pixels and analog-to-digital converters on a first chip and the associated color interpolation circuitry on a second chip is disclosed by *Neter*, and a POSITA would have found it obvious in view of *Neter* to implement the recited components of *Isogai* on two separate chips as recited in claim 14. (Ex. 1002, ¶¶75-86.)

Neter, like *Isogai*, describes circuits for processing imaging pixel sensor elements. (Ex. 1007, 2:60-62, 3:4-16; Ex. 1002, ¶76.) Both *Neter* and *Isogai* describe image sensing devices that include red, blue, and green pixels arranged in

the Bayer pattern scheme. (Ex. 1007, 3:12-14, FIG. 3; Ex. 1004, ¶[0028], FIG. 1.) Therefore, a POSITA implementing an image sensing device like that described in *Isogai* would have had reason to look to *Neter*. (Ex. 1002, ¶76.)

Neter discloses that the disclosed imaging system, which includes groups of red, blue, and green pixels, analog-to-digital converters, and additional processing circuitry like a color interpolation circuit, can be implemented on one or more chips. (Ex. 1002, ¶77.) For example, *Neter* discloses an array of red, green, and blue pixels arranged in the Bayer color pattern (Ex. 1007, 7:33-37), where additional components of the imaging system, including analog-to-digital converters and color interpolation circuitry, may or may not be included on the same integrated circuit as the array of pixels. (*Id*., 5:47-52 ("The imaging system in accordance with the present invention may also include additional **on-chip or off chip** amplification stages, **analog-to-digital conversion units**, memory units and various other **signal processing blocks**.") (emphasis added), 7:48-53, 7:55-63, 3:1-3; Ex. 1002, ¶77.)

Given *Neter's* disclosure of various image processing system components being included either on the same chip as the pixel array that includes the groups of pixels or on another chip separate from the pixel array, a POSITA would have found it obvious to combine the teachings of *Neter* and *Isogai* such that *Isogai's* imaging device would include the analog-to-digital converters on the same chip as the groups of red, blue, and green pixels, whereas the color interpolation circuitry is on a

separate chip. (Ex. 1002, ¶78.) Such a skilled person would have been motivated to do so because, in some embodiments, while integration may have been desirable, the complexity of the color interpolation circuitry may require significant hardware and software that would be better implemented on a separate chip. (*Id*.; Ex. 1007, 1:32-49.) Indeed, *Isogai* recognizes that implementing components of its imaging device on on the same or different chips is a design choice. (Ex. 1005, ¶[0065] (disclosing, with respect to the embodiment shown in FIG. 17, that the output buffer amplifiers 28a-28d can be provided "inside the solid-state image sensing element in order to avoid the influence of external noise" whereas differential amplifiers 34a-b are provided "outside the solid-state image sensing element.", FIG. 17; Ex. 1002, ¶79.)

Neter discloses that in conventional image processing systems (like that disclosed by *Isogai*) the image processing **may require** significant resources that could increase the complexity, size and expense of the imaging device. (Ex. 1007, 1:32-49; Ex. 1002, ¶80.) A POSITA reading *Neter* would have understood that *Neter* discloses that the color interpolation circuitry, as well as the analog-to-digital conversion circuitry, can either be placed on the same chip as the pixel array or not, where the decision as to whether to use one chip or two is a design choice that is influenced by many factors, including the complexity of pixel interpolation and other image processing, the size of the pixel array, the complexity of the analog-to-digital

converters, as well as the presence or absence of additional intervening circuitry between the pixel array and the color interpolation circuitry. (Ex. 1002, ¶80.)

Indeed, a POSITA would have understood that while integration of circuitry onto a single chip can provide a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like, in some instances it is preferable to maintain the color interpolation circuitry on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. (*Id*., ¶81.) For instance, including the analog-to-digital conversion on the same chip as the pixel array while keeping the color interpolation circuitry on a separate chip provides flexibility to support different systems/applications with different levels of color processing. (*Id*.) In such a scenario, a pixel-array chip that includes analog-to-digital converters would provide digital outputs that can be provided as the inputs to different color interpolation/processing chips with different processing capabilities in order to satisfy the needs of different applications. (*Id*.)

Such an understanding is supported by contemporaneous references that disclose analog-to-digital converters included with the pixel array on the same chip while the color interpolation circuitry resides on a separate chip. (*Id*., ¶82.) For example, *Fossum* (Ex. 1008) discloses CMOS imagers with analog-to-digital conversion on the same chip as the pixel array "to provide a digital representation of

the image which can be retrieved from the imager 10 through a parallel port interface." (Ex. 1008, 1:7-26, FIG. 1; Ex. 1002, ¶82.)

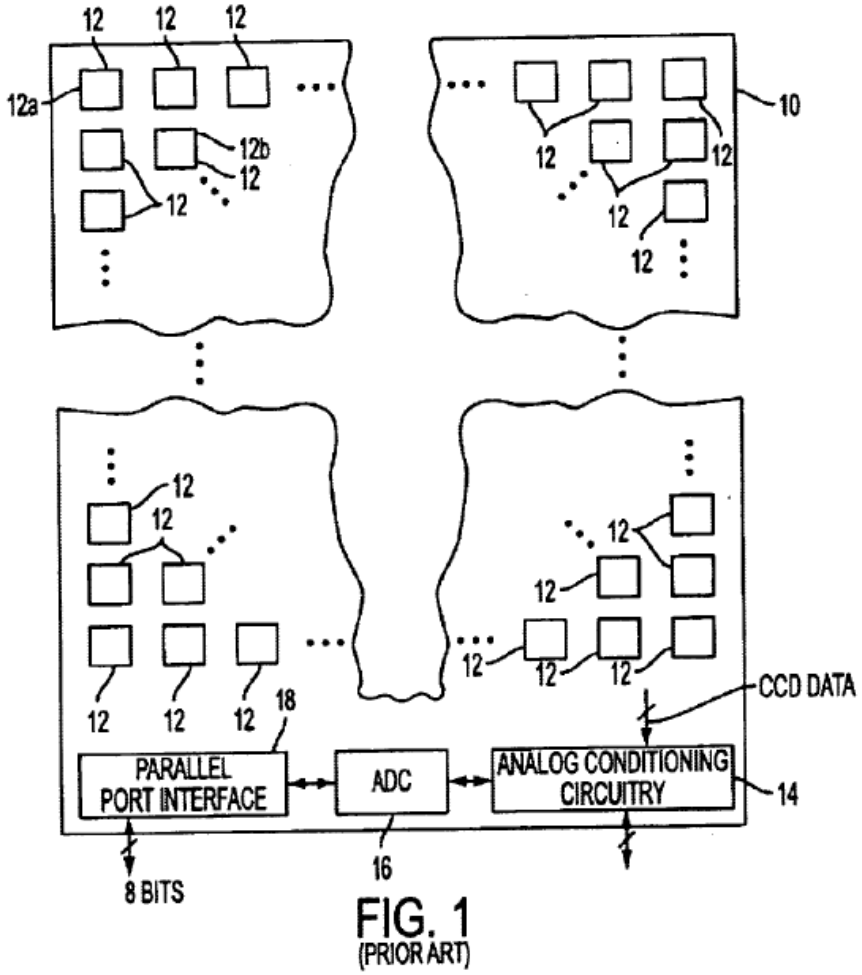


FIG. 1
(PRIOR ART)

(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 can be used with the imaging chip 10 above, where the DSP chip performs color interpolation. (*Id*., 2:5-7.)

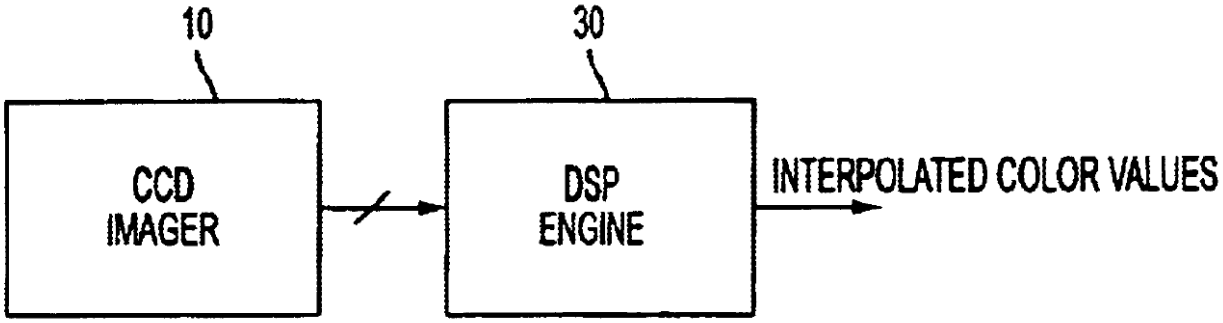


FIG. 4
(PRIOR ART)

(*Id*., FIG. 4.)

Therefore, in view of *Neter* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters on the same chip as the pixel array, while providing a second chip that includes the color processing circuitry. (Ex. 1002, ¶83.) Including the analog-to-digital converters on the same chip as the pixel array in the imaging device of *Isogai* and a second chip that includes the color processing circuitry would have merely involved the use of a known technique (performing analog-to-digital conversion of the pixel outputs on the same chip as the red, blue, and green pixels and color processing on a separate chip) to improve a similar device (the device described in *Isogai*) to achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels

of pixel interpolation. (*Id*., ¶84; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-417 (2007).) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation of success. (Ex. 1002, ¶84; *KSR*, 550 U.S. at 421.) Therefore, the *Isogai-Neter* combination discloses or suggests the features recited in claim 14 of the '651 patent. (Ex. 1002, ¶85.)

Including the analog-to-digital converters of *Isogai's* imaging device on the same chip as the pixel array and the color processing circuitry on another chip would have been straightforward for a POSITA to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*. (*Id*., ¶86.) For example, as demonstrated by *Neter*, *Fossum*, and *Loinaz*, a POSITA at the relevant time had the capability to include both the analog-to-digital conversion circuitry and the color processing (color interpolation) circuitry on the same chip as the pixel array. (Ex. 1007, 5:47-52; Ex. 1008, FIGs. 1, 5; Ex. 1010, FIG. 1; *infra* section IX.B.2; Ex. 1002, ¶86.) Therefore, such a POSITA would also have been able to include a subset of those components on the same chip while keeping the color processing circuitry on a second chip. (Ex. 1002, ¶86.) Moreover, a POSITA would have understood

how to make any needed modifications in order to ensure that such an implementation was succesful. (*Id*.)

2. Claim 15

a) The solid stage imaging device of claim 13 further comprising a chip, wherein the groups of pixels, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

The *Isogai-Neter* combination discloses or suggests these limitations. (Ex. 1002, ¶¶87-94.) *Isogai* does not explicitly disclose that the components recited in claim 15 are included on a single integrated circuit. *Neter*, however, discloses such a feature, and a POSITA would have found it obvious, in view of *Neter*, to implement the imaging device of *Isogai* such that all of the components recited in claim 15 are on the same chip. (*Id*., ¶¶87-88.)

As discussed above in Section IX.B.1, *Neter* discloses including the circuitry for color interpolation and the analog-to-digital conversion circuitry on the same chip as the pixel array that includes the red, blue, and green pixels. (Ex. 1007, 5:47-52, 7:33-37, 7:48-53, 7:55-59, 3:1-3; Ex. 1002, ¶88.) As also discussed above in Section IX.B.1, a POSITA would have understood, based on the disclosure of *Neter* and the understanding of the state of the art, that implementing the analog-to-digital converters and color processing circuitry ("color interpolation circuit") on the same chip as the pixel array in an image processing device is a design choice. (*Supra*

section IX.B.1.) Moreover, a POSITA would have been motivated to include all of these components of an imaging device, like that disclosed by *Isogai*, on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like. (*Id*.; Ex. 1002, ¶88.) Therefore, in view of *Neter* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters and the color processing circuitry on the same chip as the pixel array that includes the groups of pixels. (Ex. 1002, ¶88.)

Including the analog-to-digital converters and color processing circuitry on the same chip as the pixel array in the imaging device of *Isogai* would have merely involved the use of a known technique (performing analog-to-digital conversion and color processing on the same chip as the red, blue, and green pixels as disclosed in *Neter*) to improve a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. (*Id*., ¶89; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. (Ex. 1002, ¶89.) Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai*

on either one chip or more than one chip with a reasonable expectation of success. (*Id*.; *KSR*, 550 U.S. at 421.) Therefore, the *Isogai-Neter* combination discloses or suggests the features recited in claim 15 of the '651 patent. (Ex. 1002, ¶90.)

Including the analog-to-digital conversion and color processing circuitry on the same chip with *Isogai's* solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Neter*. (*Id*.) Indeed, the motivation and ability for a POSITA to perform such integration is supported by *Fossum*, which discloses CMOS imagers with analog-to-digital conversion and color interpolation circuitry on the same chip as the pixel array. (*Id*., ¶¶91-92; Ex. 1008, 4:4-6, 4:33-44, FIG. 5.)

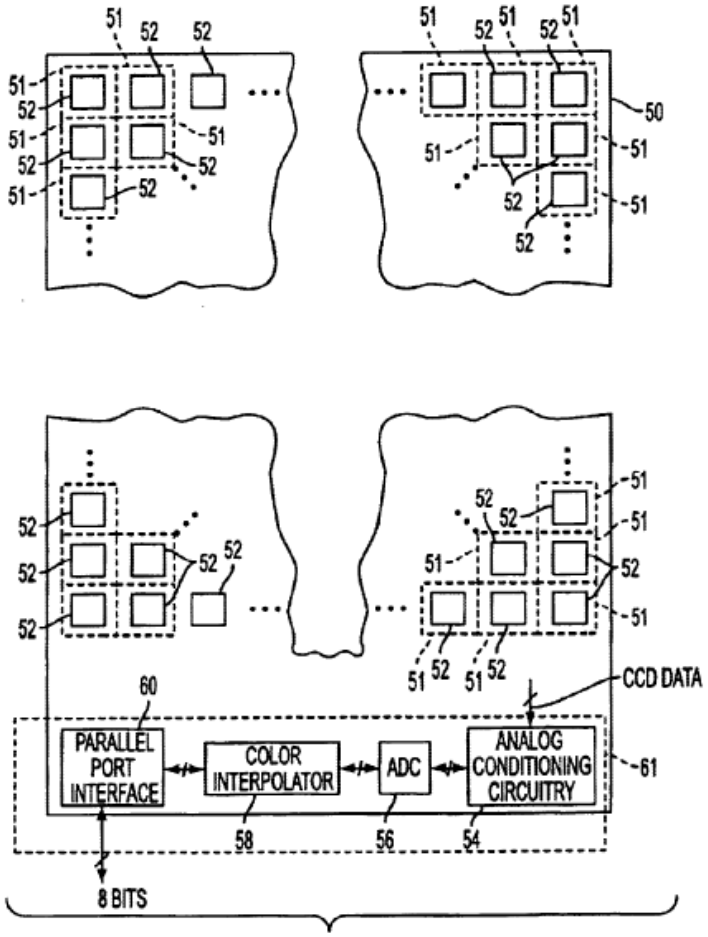
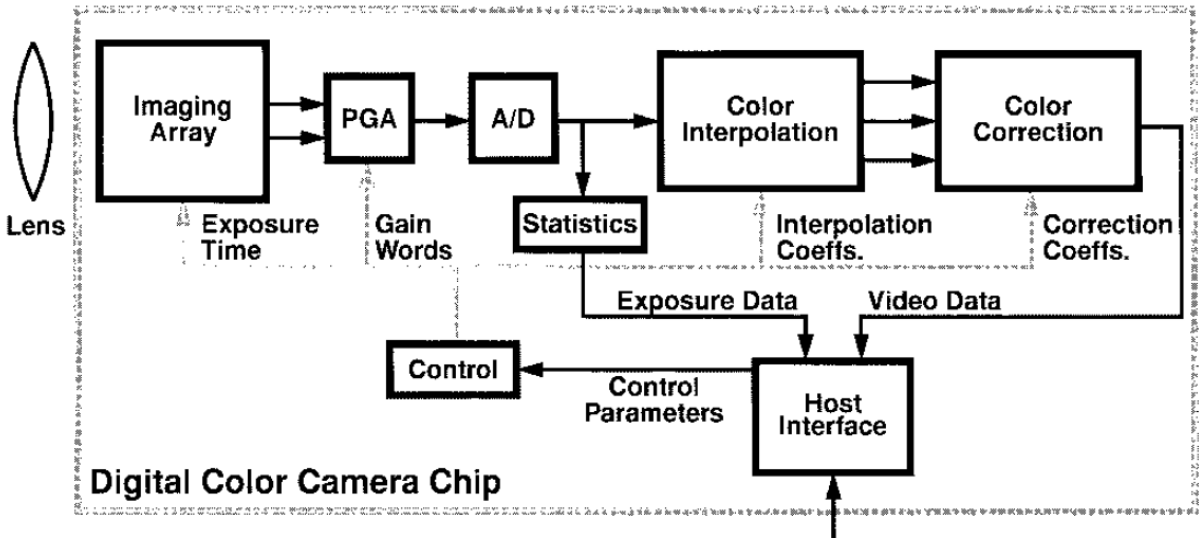


FIG. 5

(Ex. 1008, FIG. 5.)

Similarly, as shown in figure 1 below, *Loinaz* discloses a digital color camera chip that includes the imaging array, analog-to-digital conversion circuitry, and color interpolation circuitry on the same chip. (Ex. 1010, Abstract, FIG. 1; Ex. 1002, ¶¶93-94.)



(Ex. 1010, FIG. 1 (excerpt).

C. Ground 3: Claims 14-15 Are Obvious Over *Isogai* in View of *Fossum*

1. Claim 14

a) The solid stage imaging device of claim 13 further comprising a first chip and a second chip, wherein the groups of pixels, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

Isogai in combination with *Fossum* discloses or suggests the limitations of claim 14. (Ex. 1002, ¶¶95-107.) *Isogai* does not explicitly disclose that, for the solid state imaging device discussed in section IX.A.1 above, the groups of pixels and analog-to-digital converters are disposed on a first chip and the color interpolation circuit is disposed on a second chip as recited in claim 14. However, such a configuration is disclosed by *Fossum*, and a POSITA would have found it obvious

in view of *Fossum* to implement the recited components in *Isogai* on two separate chips as recited in claim 14. (Ex. 1002, ¶¶95-96.)

Fossum, like *Isogai*, describes circuits for processing red, blue, and green imaging pixel sensor elements that includes color interpolation. (Ex. 1008, 4:45-59, FIG. 5.) As shown in figure 5 below, *Fossum* discloses color interpolation done after analog-to-digital conversion, similar to as described in *Isogai*. (Ex. 1008, FIG. 5; *see also id*., 5:7-11; Ex. 1002, ¶97.) Therefore, a POSITA implementing the image sensing device of *Isogai* would have had reason to look to *Fossum*. (Ex. 1002, ¶98.)

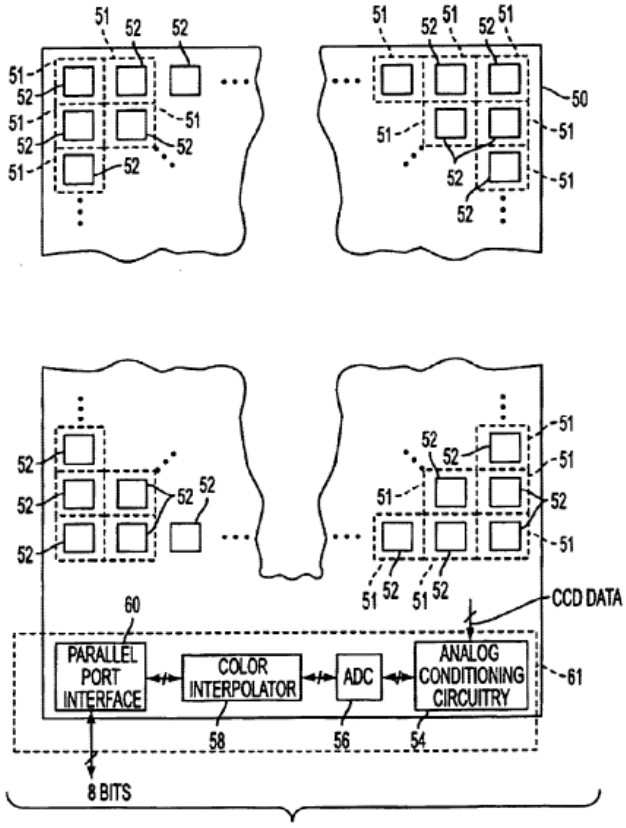


FIG. 5

(Ex. 1008, FIG. 5.)

Fossum also discloses CMOS imagers with analog-to-digital conversion on the same chip as a red, blue, and green pixel array "to provide a digital representation of the image which can be retrieved from the imager 10 through a parallel port interface." (Ex. 1008, 1:7-26, FIG. 1 (showing analog to digital converter (ADC) 16 on the same chip as pixel cells 12); Ex. 1002, ¶99.)

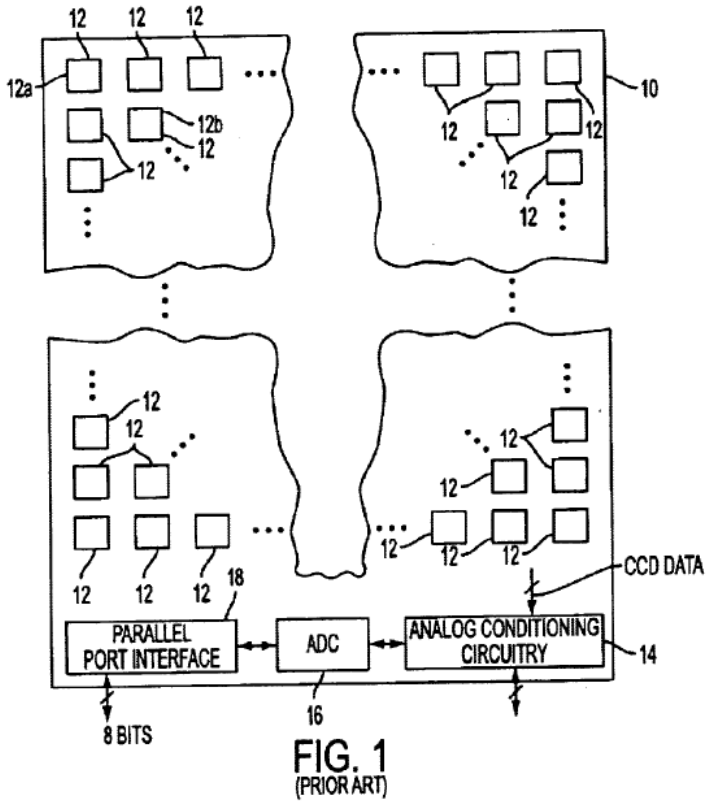


FIG. 1
(PRIOR ART)

(Ex. 1008, FIG. 1.) *Fossum* further discloses that a separate DSP chip 30 is used with the imaging chip 10 above, where the DSP chip 30 performs color interpolation. (*Id*., 2:5-7; Ex. 1002, ¶99.)

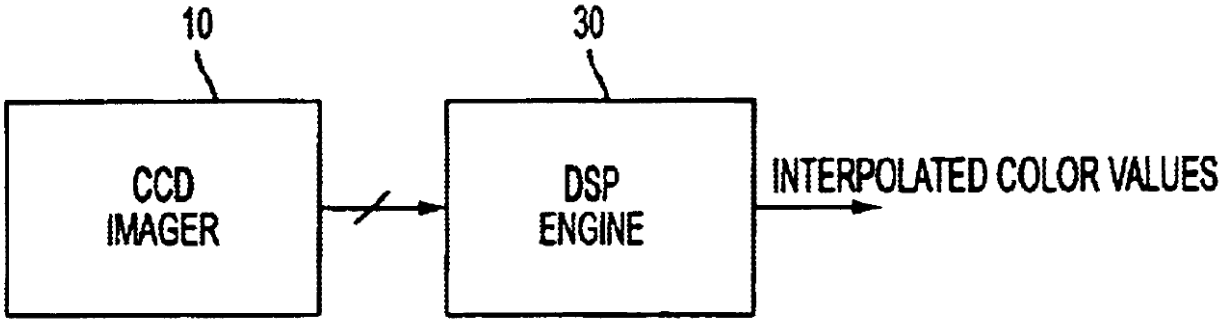


FIG. 4
(PRIOR ART)

(Ex. 1008, FIG. 4.)

Therefore, *Fossum* discloses the arrangement of components on two chips as recited in claim 14. (*Id*.; Ex. 1002, ¶100.) In view of *Fossum*, a POSITA implementing the imaging device of *Isogai* would have found it obvious to include *Isogai's* analog-to-digital conversion circuitry on the same chip with the groups of red, blue, first green and second green pixels while maintaining the color processing circuitry on a separate chip. (Ex. 1002, ¶100.)

As discussed above in Section IX.B.1, a POSITA would have understood that while integration of circuitry onto a single chip can provide a number of advantages, in some instances it may be preferable to maintain the color interpolation circuitry on a separate chip while integrating the analog-to-digital converters onto the same chip as the pixel array. (*Supra* section IX.B.1.) For example, such an arrangement

would provide flexibility to support different systems/applications with different levels of color processing. (*Id*.; Ex. 1008, 1:24-26; Ex. 1002, ¶101.)

Moreover, a POSITA would have understood that determining whether to put the analog-to-digital converters and/or color interpolation circuitry for an image processing system on the same chip with the pixel array is a design choice that is influenced by many factors. (*Supra* section IX.B.1; Ex. 1002, ¶¶102-103.) Indeed, *Isogai* recognizes that implementing components of its imaging device on the same or different chips is a design choice. (Ex. 1007, ¶[0065], FIG. 17; Ex. 1002, ¶102.)

Therefore, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters on the same chip as the pixel array that includes the groups of pixels, while providing the color processing circuitry on a second chip. (Ex. 1002, ¶104.) Such a configuration would have merely involved the use of a known technique (performing analog-to-digital conversion on the same chip as the pixels and color processing on a separate chip as disclosed in *Fossum*) to improve a similar device (the device of *Isogai*) to achieve the expected and desired result of increased integration while maintaining flexibility to support different systems/applications with different levels of color processing. (Ex. 1002, ¶105; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one

chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful. (Ex. 1002, ¶105; *KSR*, 550 U.S. at 421.)

Including the analog-to-digital conversion with the groups of pixels in *Isogai's* imaging device would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in *Fossum*. (Ex. 1002, ¶¶106-107; *supra* Section IX.B.1.)

2. Claim 15

a) The solid stage imaging device of claim 13 further comprising a chip, wherein the groups of pixels, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

The *Isogai-Fossum* combination discloses or suggests the limitations of claim 15. (Ex. 1002, ¶¶108-117.) *Isogai* does not explicitly disclose that the components recited in claim 15 are included on a single integrated circuit. *Fossum*, however, discloses such a feature, and a POSITA would have found it obvious, in view of *Fossum*, to implement the imaging device of *Isogai* such that all of the components recited in claim 15 are on the same chip. (Ex. 1002, ¶109.)

Fossum discloses including the circuitry for color interpolation and the analog-to-digital conversion circuitry on the same chip as the pixel array that includes red, blue, and green pixels. (Ex. 1008, 4:33-44, FIG. 5; Ex. 1002, ¶111.)

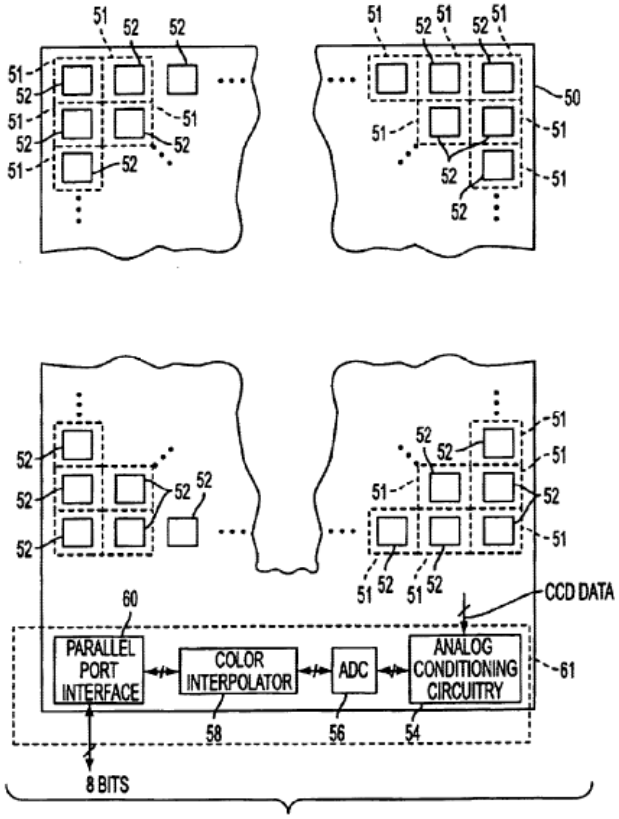


FIG. 5

(Ex. 1008, FIG. 5.)

Fossum discloses that "FIG. 5 shows a CMOS imager 50 located on a monolithic semiconductor substrate, or chip" (*id*., 4:33-34), without "requiring . . . off chip-color interpolation" (*id*., 4:40-44). According to *Fossum*, "[a]mong the advantages of the invention" is [t]rue color imaging occurs on a single semiconductor chip." (*Id*., 4:4-6; *see also id*., 4:45-58; Ex. 1002, ¶112.)

As discussed above in Section IX.B.1, a POSITA would have understood that implementing the analog-to-digital converters and color processing circuitry on the same chip as the pixel array is a design choice. (*Supra* section IX.B.1; Ex. 1002, ¶110.) Moreover, a POSITA would have been motivated to include all of these components of an imaging device, like that disclosed by *Isogai*, on the same chip in order to realize a number of advantages, including increased performance, reduced manufacturing costs, fewer chips required, and the like. (*Supra* section IX.B.1; Ex. 1002, ¶110.) Therefore, in view of *Fossum* and having knowledge of the state of the art at the relevant time, a POSITA looking to implement a solid state imaging device as disclosed in *Isogai* would have found it obvious to include the analog-to-digital converters and the color processing circuitry on the same chip as the pixel array. (Ex. 1002, ¶¶113-114.) Such integration would have merely been the use of a known technique (performing analog-to-digital conversion and color processing on the same chip as the pixels as disclosed in *Fossum*) for a similar device (the imaging device of *Isogai*) to achieve the expected and desired result of increased integration that can provide increased speed, reduced costs, and support for smaller devices. (*Id*.; *KSR*, 550 U.S. at 416-417.) Additionally, as discussed above, it was known and predictable that imaging circuitry like that described in *Isogai* could have been implemented on either one chip or more than one chip, depending on the needs of the system. Thus, a POSITA would have had reason to try implementing the

circuitry in *Isogai* on either one chip or more than one chip with a reasonable expectation that one would be successful. (Ex. 1002, ¶113; *KSR*, 550 U.S. at 421.)

Including the analog-to-digital converters and color processing circuitry in *Isogai's* solid-state image sensing element as shown in figure 1 would have been straightforward for a skilled person to implement given such a person's knowledge of the state of the art and the disclosure in Fossum. (*Supra* Section IX.B.2; Ex. 1010, Abstract, FIG. 1; Ex. 1002, *Id*., ¶¶114-117.)

D. Ground 4: Claim 13 Is Anticipated by *Inuiya*

1. Claim 13

a) A solid state imaging device, comprising:

To the extent the preamble of claim 13 is limiting, *Inuiya* discloses the limitations therein. (Ex. 1002, ¶¶118-120.) For instance, *Inuiya* discloses a "a solid-state electronic image sensing device and a method of reading a signal change out of the solid-state electronic image sensing device." (Ex. 1006, 1:15-18; *see also id*., 2:20-23; 4:56-67.) Figure 18 of *Inuiya* is a block diagram of a digital video tape recorder that includes an image sensing section with a charge-coupled device (CCD) 100 that includes a large number of pixels. (*Id*., 20:12-22; Ex. 1002, ¶120.)

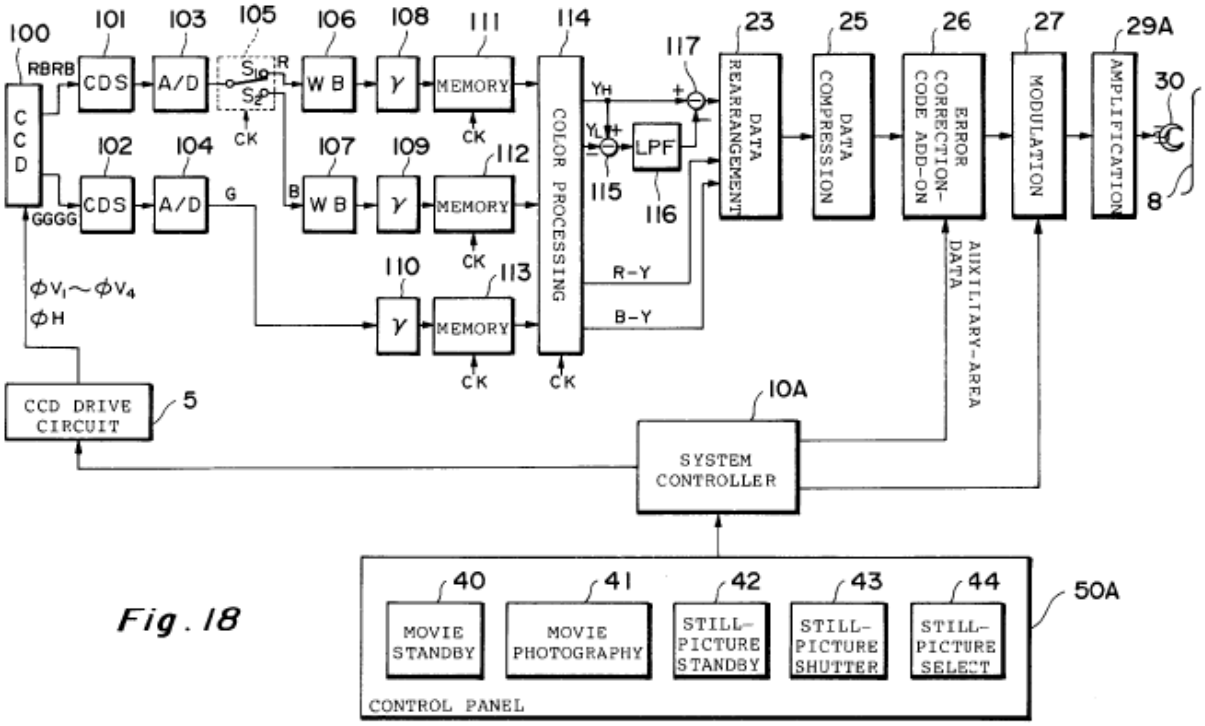


Fig. 18

(Ex. 1006, FIG. 18.) Image data from the CCD 100 is provided to color processing circuit 114, which combines the pixel data to generate luminance and color difference data. (*See infra* Section IX.D.1(e).) *Inuiya's* digital tape recorder constitutes a "solid-state image processing device" as recited in claim 1. (Ex. 1002, ¶120.)

b) groups of pixels, wherein each said group of pixels include:

a red pixel having an output;

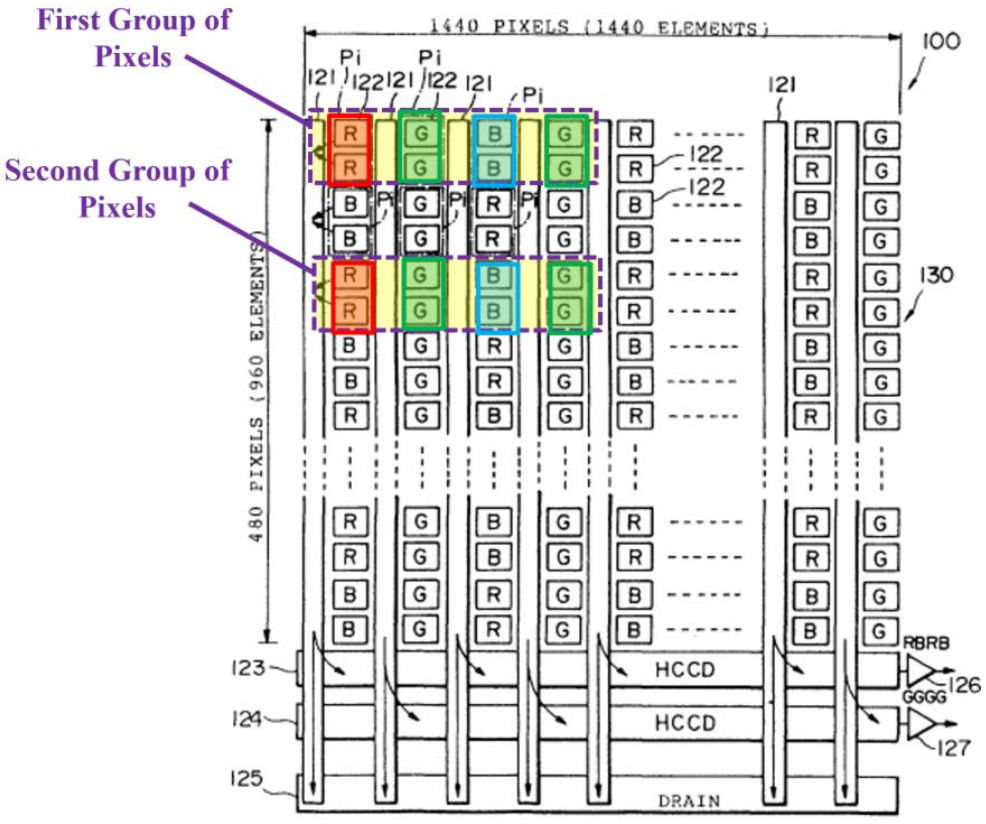
a blue pixel having an output;

a first green pixel having an output; and

a second green pixel having an output;

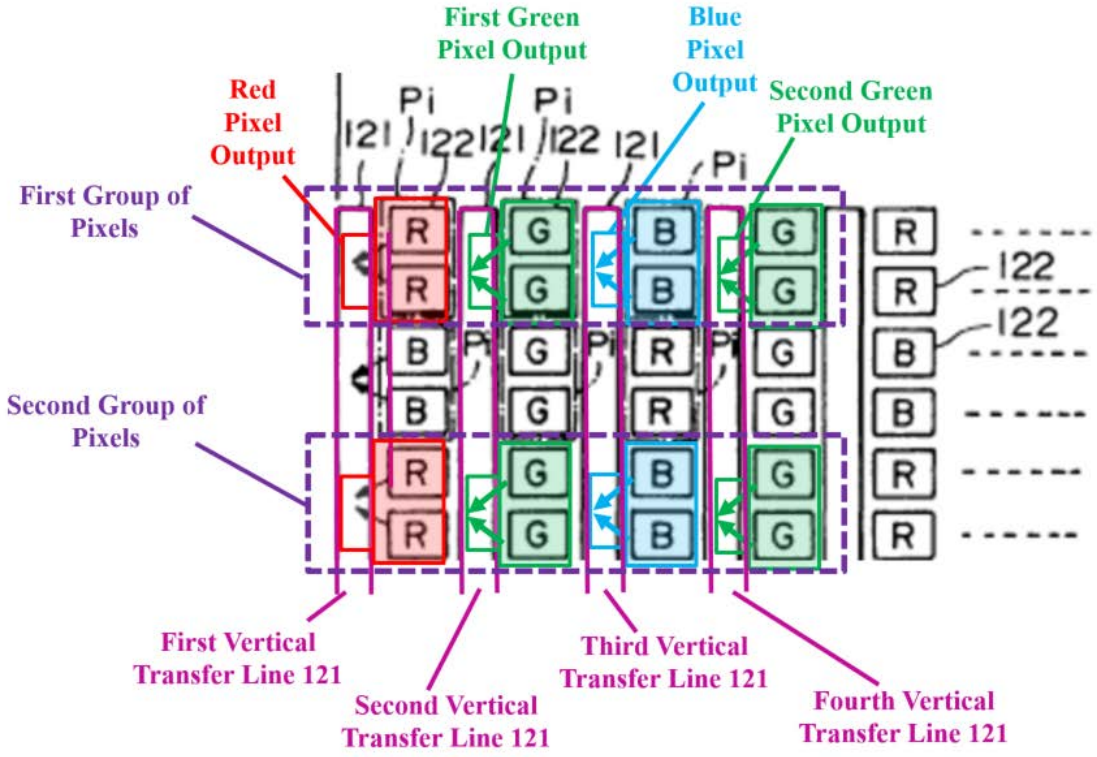
Inuiya discloses these limitations. (Ex. 1002, ¶¶121-124.) Figure 19 of *Inuiya* is a schematic view of the CCD 100 included in the solid-state image processing device shown in figure 18. (Ex. 1006, 20:23.) The CCD 100 includes a plurality of groups of pixels, where each group includes a red pixel, a blue pixel, a first green pixel, and a second green pixel. For example, two such groups of pixels are highlighted in annotated figure 19 below.

Fig. 19



(Ex. 1006, FIG. 19 (annotated); Ex. 1002, ¶121.)

Inuiya discloses that the signal charges that have accumulated in two photodiodes are mixed in the vertical transfer lines 121 of the CCD 100 such that the pixels, which are labeled "Pi" in figure 19, are each composed of two photodiodes 122. (*Id*., 20:33-62, FIG. 19; Ex. 1002, ¶122.) Therefore, each of the red, blue, first green, and second green pixels in each group of pixels has an output. (Ex. 1002, ¶123.) *Inuiya* discloses that a transfer gate is used to control when the charge for each pixel is applied to the vertical transfer line. (Ex. 1006, 21:7-12; Ex. 1002, ¶123.)



(Ex. 1006, FIG. 19 (excerpt, annotated); Ex. 1002, ¶123.)

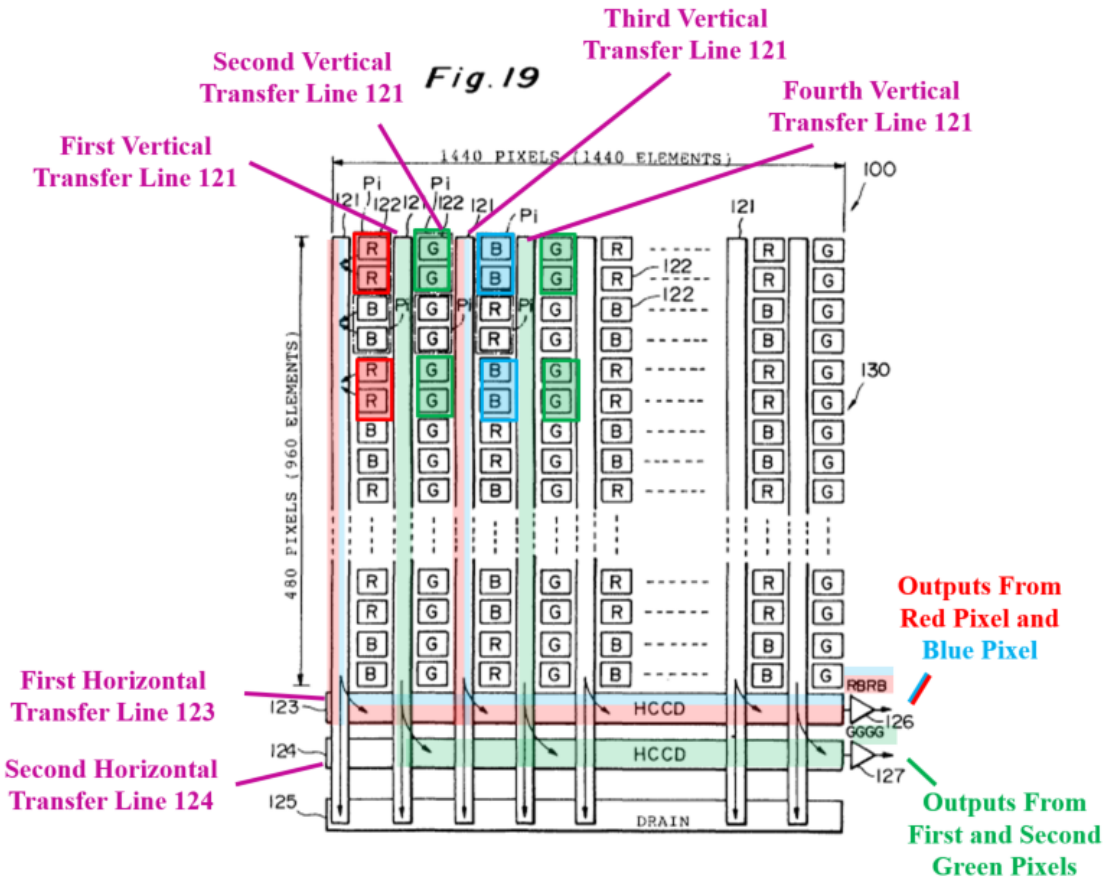
As shown in the enlarged and annotated excerpt of figure 19 above, the outputs of the highlighted red, blue, first green, and second green pixels are connected to the first, second, third, and fourth vertical transfer lines, respectively. (Ex. 1006, 20:47-62, 21:7-12, FIG. 19; Ex. 1002, ¶124.)

c) a first analog-to-digital converter connected to the output of the red pixel for converting the output of the red pixels into a first digital signal and connected to the output of the blue pixel for converting the output of the blue pixels into a second digital signal;

d) a second analog-to-digital converter connected to the output of the first green pixel for converting the output of the first green pixels into a third digital signal and connected to the output of the second green pixel for converting the output of the second green pixels into a fourth digital signal; and

Inuiya discloses these limitations. (Ex. 1002, ¶¶125-133.) As discussed above in Section IX.D.1(b), for each of the groups of pixels, the red pixel output is connected to the first vertical transfer line 121, and the blue pixel output is connected to the third vertical transfer line 121. Similarly, the first green pixel output is connected to the second vertical transfer line 121, and the second green pixel output is connected to the fourth vertical transfer line 121. (Ex. 1006, 20:44-53, 21:7-12, FIG. 19; *supra* Section IX.D.1(b).) As shown in annotated figure 19 below, the first and third vertical transfer lines 121 are connected to the horizontal transfer line 123, whereas the second and fourth vertical transfer lines are connected to the horizontal

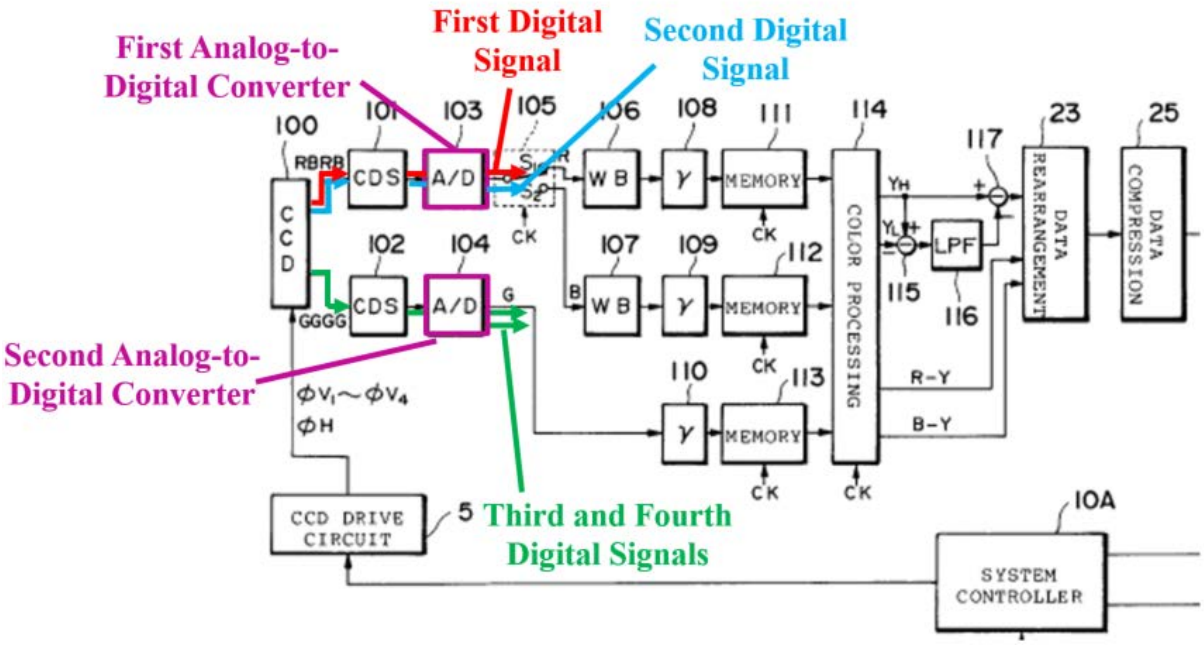
transfer line 124, such that the red/blue pixel outputs are sequentially output by amplifier 126 and the first/second green pixel outputs are sequentially output by amplifier 127. (Ex. 1006, 21:36-62, 22:63-23:25; Ex. 1002, ¶¶125-128.)[6]



(Ex. 1006, FIG. 19 (annotated); Ex. 1002, ¶125.)

[6] The even rows in the pixel array also have the outputs of the red and blue pixels connected to the odd vertical transfer lines (e.g. first, third, etc.) such that odd vertical transfer lines only carry red/blue pixel outputs and the even vertical transfer lines only carry green pixel outputs. (Ex. 1006, FIG. 19; Ex. 1002, ¶128.)

As shown in the annotated excerpt of figure 18 below, *Inuiya* discloses that the output signals from the CCD 100 are provided through correlated data sampling circuits 101, 102 to analog-to-digital converters 103, 104. (*Id*., 25:36-43; Ex. 1002, ¶129.)



(Ex. 1006, FIG. 18 (excerpt, annotated); Ex. 1002, ¶129.)

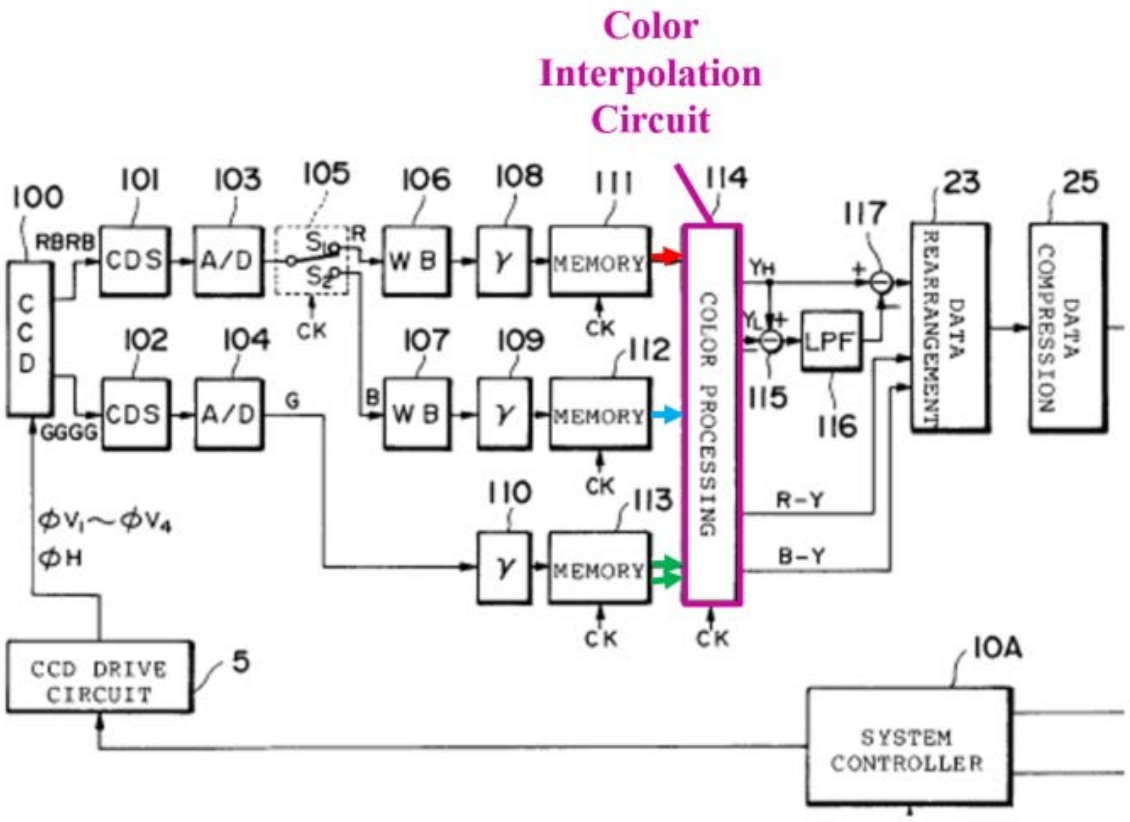
As shown in the annotated excerpt of figure 18 above, the outputs of the red and blue pixels for each pixel group (part of RBRB coming out of the CCD) are "outputted alternately by the first horizontal transfer line 123" and provided to the analog-to-digital converter (A/D) 103, whereas the outputs of the first and second green pixels for each pixel group (part of GGGG coming out of the CCD) are sequentially provided to the analog-to-digital converter (A/D) 104. (Ex. 1006, 25:36-43; Ex. 1002, ¶130.) A POSITA would have understood that the analog-to-digital

converters 103 and 104 are "connected to" the outputs of the pixels as they receive and convert the analog signals from those outputs into digital image data. (Ex. 1002, ¶130.) The digital image data generated by the analog-to-digital converter 103 includes a "first digital signal" corresponding to the red pixel output and a "second digital signal" corresponding to the blue pixel output. (*Id*., ¶131.) The red and blue pixel outputs are sequentially provided from the CCD 100 to A/D 103. The digital image data generated by the analog-to-digital converter 103 includes a "first digital signal" that is output when the red pixel is provided to A/D 103 and a "second digital signal" that is output when the blue pixel output is provided to the A/D 103. (*Id*.) Similarly, the first and second green pixel outputs are sequentially provided to A/D 103. (*Id*., ¶132.) *Inuiya* discloses the G signals are converted into a digital G data, including the "third digital signal" for the "first green pixel," the "fourth digital signal" for the "second green pixel," and other digital signals corresponding to other green pixels. (*Id*.; Ex. 1006, 25:55-59.) Therefore, the analog-to-digital converters 103 and 104 disclose first and second analog-to-digital converters, respectively, as recited in claim 13. (Ex. 1002, ¶133.)

e) a color interpolation circuit for combining the first, second, third and fourth digital signals.

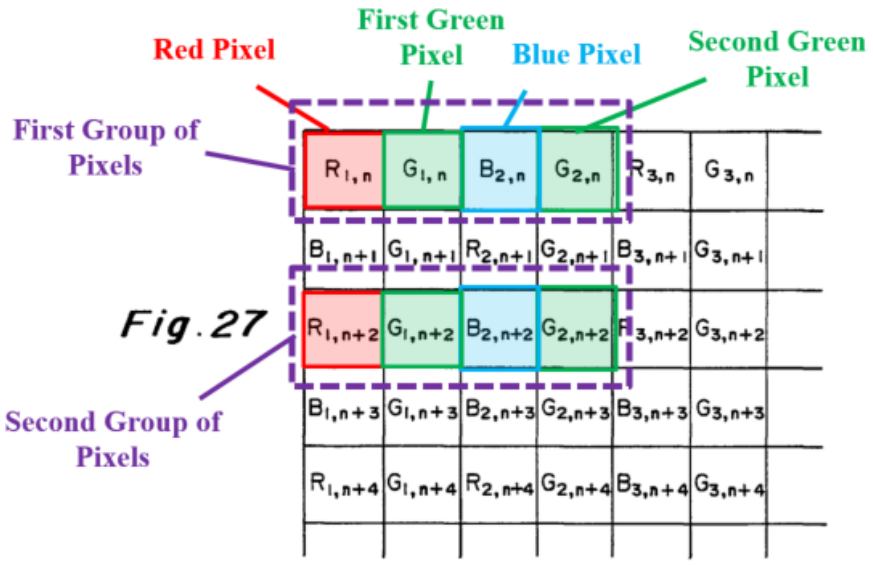
Inuiya discloses these limitations. (Ex. 1002, ¶¶134-141.) As discussed above in Sections IX.D.1(c)-(d), the analog-to-digital converters 103 and 104 convert the outputs of red, blue, first green, and second green pixels into the first,

second, third, and fourth digital signals, respectively. (*Supra* sections IX.D.1(c)-(d).) *Inuiya* further discloses that these digital signals are processed by white-balance adjustment circuits 106-107 and gamma-correction circuits 108-110 before being stored in memories 111-113. (Ex. 1006, 25:49-63, FIG. 18; Ex. 1002, ¶134.) The digital pixel data stored in the memories 111-113 is then processed by the color processing block ("color interpolation circuit"), which combines the first, second, third and fourth digital signals to produce luminance data and color difference data. (Ex. 1006, 26:5-19, 27:10-18; Ex. 1002, ¶135.)



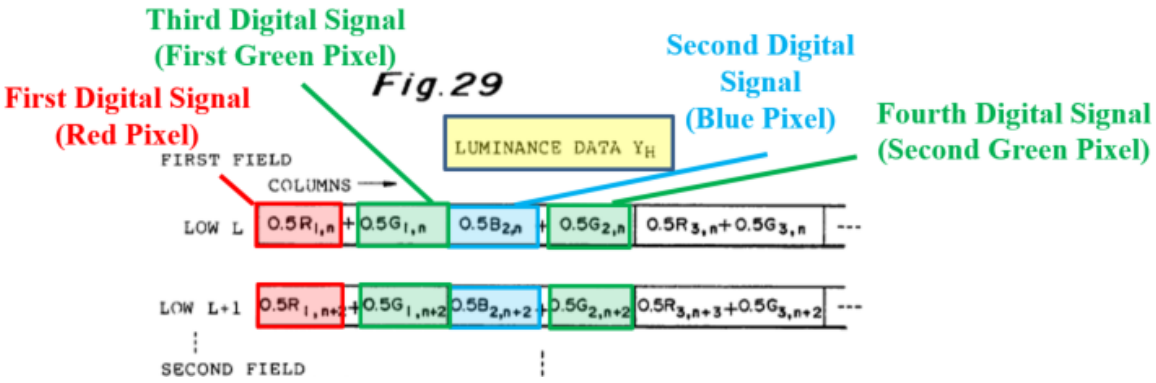
(Ex. 1006, FIG. 18 (excerpt, annotated); Ex. 1002, ¶135.)

Inuiya discloses that generation of the luminance data includes combining the digital signals corresponding to the red, blue, and first and second green pixels. (Ex. 1006, FIGs. 27, 29; Ex. 1002, ¶¶136-138.) The red, blue, and first/second green pixels of the first and second groups of pixels discussed above in Section IX.D.1(b) are highlighted in figure 27 below. (*Supra* Section IX.D.1(b); Ex. 1006, FIG. 27; Ex. 1002, ¶137.)



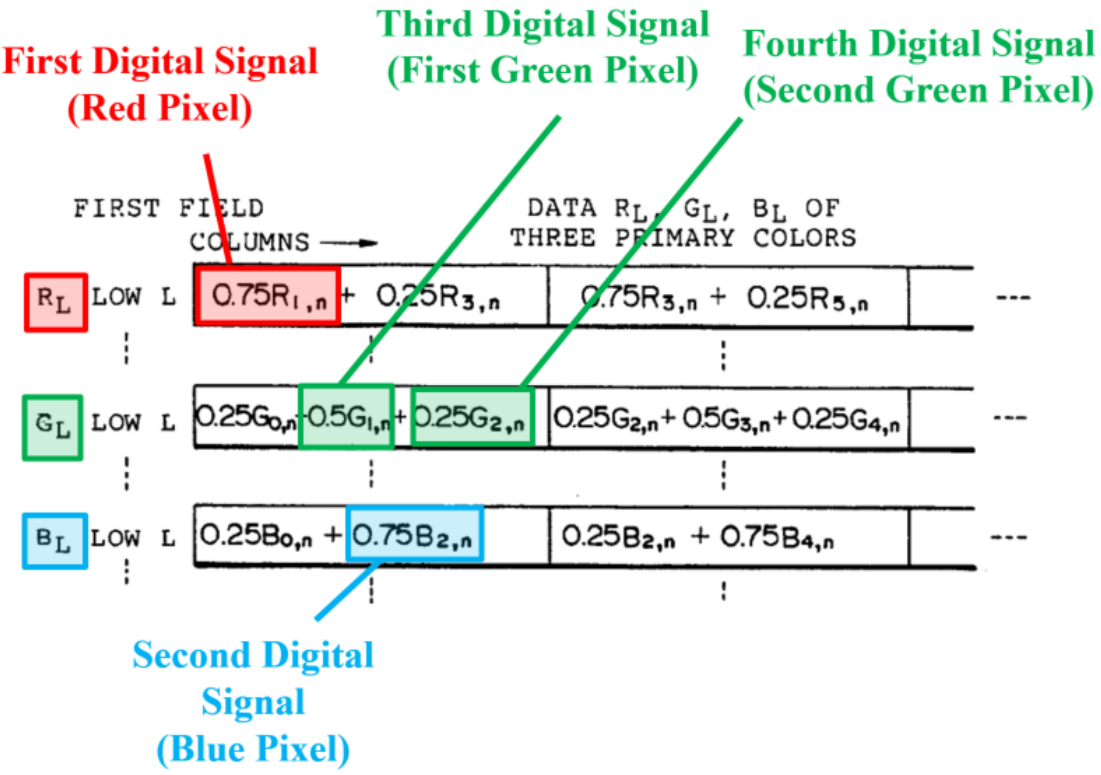
(Ex. 1006, FIG. 27 (annotated); Ex. 1002, ¶137.)

As shown in the annotated excerpt of figure 29 below, the first, second, third, and fourth digital signals are combined by the color processing circuit 114 to generate the luminance data Y_H. (Ex. 1006, FIG. 29; Ex. 1002, ¶138.)



(Ex. 1006, FIG. 29 (excerpt, annotated); Ex. 1002, ¶138.)

Inuiya further discloses that the pixel outputs for the red, blue, first green, and second green pixels are combined in calculating the luminance data Y_L of the low-frequency components. (Ex. Ex. 1002, ¶139.) For example, figure 30 of *Inuiya* shows that the outputs for the red, blue, first green, and second green pixels are included in calculating R_L, G_L, and B_L, where, as discussed below, those values are in turn used to calculate the luminance data Y_L:



(Ex. 1006, FIG. 30 (excerpt, annotated); Ex. 1002, ¶139.)

Inuiya discloses:

> When the R_L data, G_L data and B_L data is generated for each of the first, second, third and fourth fields, the luminance data Y_L of the low-frequency components is generated, for each of the first, second, third and fourth fields, from the R_L data, G_L data and B_L data in accordance with the following equation:
>
> $$Y_L = 0.3R_L + 0.59G_L + .11B_L \qquad \text{(Eq. (1)}$$

(Ex. 1006, 28:49-57 (equation annotated); Ex. 1002, ¶140.)

As demonstrated above, the digital signals corresponding to the red, blue, first green, and second green pixels are combined to produce both the luminance data Y_H and luminance data Y_L. (Ex. 1002, ¶141.) Therefore, the color processing block 114 constitutes a "color interpolation circuit for combining the first, second, third and fourth digital signal." (*Id*.)

E. Ground 5: Claims 14-15 Are Obvious Over *Inuiya* in View of *Neter*

1. Claim 14

a) The solid stage imaging device of claim 13 further comprising a first chip and a second chip, wherein the groups of pixels, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

As discussed above in Section IX.B.1, a POSITA would have understood that implementing the components of an imaging device on two chips would have been an obvious combination and/or design choice. (*Supra* section IX.B.1.) *Inuiya*, like *Isogai* and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Neter* in Section IX.B.1, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Neter* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip. (Ex. 1002, ¶142.)

2. Claim 15

a) The solid stage imaging device of claim 13 further comprising a chip, wherein the groups of pixels, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

As discussed above in Section IX.B.2, a POSITA would have understood that implementing the components of an imaging device on one chip would have been an obvious combination and/or design choice. (*Supra* section IX.B.2.) *Inuiya*, like *Isogai* and *Neter*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Neter* in Section IX.B.2, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Neter* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters and color processing circuitry are on the same chip as the pixel array. (Ex. 1002, ¶143.)

F. Ground 6: Claims 14-15 Are Obvious Over *Inuiya* in View of *Fossum*

1. Claim 14

a) The solid stage imaging device of claim 13 further comprising a first chip and a second chip, wherein the groups of pixels, the first analog-to-digital converter and the second analog-to-digital converter are disposed on the first chip and the color interpolation circuit is disposed on the second chip.

As discussed above in Section IX.B.1, a POSITA would have understood that implementing the components of an imaging device on two chips would have been

an obvious combination and/or design choice. (*Supra* section IX.B.1.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Fossum* in Section IX.C.1, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Fossum* with a reasonable expectation of success such that *Inuiya's* analog-to-digital converters are on the same chip as the pixel array, while maintaining the color processing circuitry on a second chip. (*Supra* Section IX.C.1; Ex. 1002, ¶144.)

2. Claim 15

a) The solid stage imaging device of claim 13 further comprising a chip, wherein the groups of pixels, the first analog-to-digital converter, the second analog-to-digital converter and the color interpolation circuit are disposed on the chip.

As discussed above in Section IX.B.2, a POSITA would have understood that implementing the components of an imaging device on one chip would have been an obvious combination and/or design choice. (*Supra* section IX.B.2.) *Inuiya*, like *Isogai* and *Fossum*, discloses an imaging device with a pixel array, analog-to-digital converters, and color processing circuitry. Therefore, for the same reasons discussed above with respect to *Isogai* in combination with *Fossum* in Section IX.C.2, a POSITA would have found it obvious to combine the teachings of *Inuiya* and *Fossum* with a reasonable expectation of success such that *Inuiya's* analog-to-digital

converters and color processing circuitry are on the same chip as the pixel array. (Ex. 1002, ¶145.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE HERE

The Board should not exercise its discretion to deny institution under *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha* IPR2016-01357, Paper 19 (P.T.A.B Sept. 6, 2017) (precedential) and *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. March 20, 2020) (precedential). A balanced assessment of the seven *General Plastic* factors and the six *Fintiv* factors favors institution. *General Plastic*, IPR2016-01357, Paper 19 at 9-10; *Fintiv*, IPR2020-0019, Paper 11 at 6.

A. Institution Is Appropriate Under *General Plastic*

Shortly after institution of the ITC investigation that includes the ’651 patent, Petitioner filed a Petition requesting *inter partes* review of claims 1-5 and 18-22 of the ’651 patent. *Samsung Electronics Co., LTD. v. Pictos Technologies, Inc.*, IPR20201-00437, Paper 1, (P.T.A.B Jan. 15, 2021.) At that time, the claims asserted in the ITC investigation did not include any of claims 13-15. (Ex. 1017, 12.) On February 1, 2021, claims 13 and 15 of the ’651 patent were added to Patent Owner’s infringement contentions. Upon learning of the assertion of claims 13 and 15, Petitioner promptly prepared and filed this Petition to cancel claims 13-15, which were not challenged in the previous IPR petition.

Because this Petition challenges new claims and was filed shortly after the petition in IPR20201-00437 (and within three weeks after Patent Owner added claims 13 and 15 to its infringement contentions on February 1, 2021), the Board should institute trial. The concerns regarding undue burden on Patent Owner and the Board, raised in *General Plastic*, are inapplicable here, where Petitioner's second petition—triggered by Patent Owner's infringement allegations—was filed early enough to permit the Board to manage these proceedings efficiently and address all challenged claims together (e.g., through consolidation or otherwise coordinating them).

The **first *General Plastic* factor**—whether the same petitioner previously filed a petition directed to the same claims of the same patent—weighs in favor of institution. Petitioner challenged claims 1-5 and 18-22 in IPR2021-00437 in the previous petition and challenges claims 13-15 in the present petition. Because the present Petition is directed to different claims, the first factor weighs in favor of institution.

The **second and fourth *General Plastic* factors**—whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it, and the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition—are related and weigh in favor of institution or, at worst, are neutral.

General Plastic, IPR2016-01357, Paper 19 at 9. While Petitioner was aware of the prior art relied upon in this petition, which is the same prior art asserted in IPR2021-00437, that should not "bear on [the Board's] determination as to whether to exercise [its] discretion in this matter" because "two different sets of claims are challenged in the two proceedings." *Signify Holding B.V. v. Lighting Sci. Grp. Corp.*, IPR2020-00753, Paper 16 at 13–14 (P.T.A.B. Sept. 16, 2020). Furthermore, barely a month has elapsed since Petitioner filed the first petition, and Petitioner's promptness weighs in favor of institution. *Id.* at 14.

The **third *General Plastic* factor**—whether Petitioner received Patent Owner's preliminary response or the Board's institution decision in IPR2021-00437 prior to the filing of this petition—also favors institution. *General Plastic*, IPR2016-01357, Paper 19 at 9. Patent Owner has not filed a preliminary response in IPR2021-00437. Nor has the Board decided whether to institute. Thus, Petitioner is not engaging in strategic serial petitioning or attempting to secure a "second bite[] at the apple"—the very concerns giving rise to the *General Plastic* framework. *Id.* at 17 & n.14; *see also Google LLC v. Hammond Dev. Int'l, Inc.*, IPR2020-00412, Paper 16 at 41 (P.T.A.B. July 16, 2020) (institution favored where petitioner filed two petitions within "a few weeks of each other, and thus did not obtain an unfair advantage").

The **fifth *General Plastic* factor**—whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent—has little relevance here, because the two petitions are directed to different sets of claims. Petitioner filed this petition promptly upon learning, on February 1, that Patent Owner was asserting claims 13 and 15 in the ITC proceeding. *See Volkswagen*, IPR2019-01573, Paper 7 at 7–8 (instituting second petition petitioner filed "a mere three weeks after being served with preliminary infringement contentions asserting the[] [challenged] claims").

The **sixth and seventh *General Plastic* factors**—preservation of the Board's resources and protecting the Board's statutory obligation to issue a final written decision no later than one year from the Board's institution decision—also favor institution. *General Plastic*, IPR2016-01357, Paper 19 at 9–10. Notably, the prior art relied upon in the present petition is the same as that presented with respect to claims 1-5 and 18-22 in IPR2021-00437, and only three additional claims are challenged. As such, the additional burden on the Board presented by the present petition is minimal

While the Board has denied institution where a delay in filing successive petitions prevents coordinating or consolidating related proceedings and adopting a common schedule, that is not an issue here. *E.g.*, *Club Champion LLC v. True Spec Golf LLC*, IPR2019-01569, Paper 9 at 10–11 (P.T.A.B. Mar. 17, 2020). Because

Petitioner promptly filed this Petition, the Board can manage this proceeding efficiently with IPR2021-00437, thereby preserving the Board's resources and ensuring the Board can meet its statutory deadlines. *See, e.g.*, 37 C.F.R. § 42.222(a) (the Board may consolidate related matters). Petitioner is also amenable to scheduling or other adjustments that would facilitate the efficient management of these two proceedings.

In sum, all the *General Plastic* factors either favor institution or are neutral. Because the concerns discussed in *General Plastic* are not present, the Board should institute a trial and coordinate this proceeding with IPR2021-00437.

Pursuant to the direction in the Board's Trial Practice Guide, if the Board nevertheless were to institute trial on just one of the two petitions, Petitioner asks that the Board institute IPR2021-00437, which addresses more claims, including independent claims 1 and 18. This petition, however, provides the Board an opportunity to address another independent claim and dependent claim that PO did not identify in its initial infringement contentions at the ITC, but later asserted.[7] By

[7] There is some question as to whether PO could have asserted new claims at this point in the ITC proceeding. Given PO's infringement allegations, however, the Board should still institute even if PO drops its infringement allegations in the ITC

coordinating and instituting trial on both petitions, the Board can address the '651 Patent more comprehensively and cancel its unpatentable claims.

B. Institution Is Appropriate Under *Fintiv*

The '651 patent will expire on March 28, 2022, which is before the April 1, 2022 target competition date of the co-pending ITC Investigation. (Ex. 1021, 2.) As a result, unless the ITC makes a determination ahead of the target conmpletion date, the ITC cannot issue a remedy as to the '651 patent. *See Certain Color Intraoral Scanners and Related Hardware and Software*, Inv. No. 337-TA-1091, Initial Determination (Mar. 1, 2019). Therefore, the Board's decision in *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 20 (Sept. 12, 2018) (precedential), has limited relevance.

Even if considered, institution is proper under *NHK*, because an evaluation of the six factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential), favors institution. As discussed below, while the '651 patent is currently involved in an ITC investigation, Petitioner diligently filed this Petition less than three months after after institution of the ITC investigation and less than *three weeks* after claims 13 and 15 were added to Patent Owner's infringement

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proceeding for the claims being challenged in this petition. This is because PO could assert such allegations in district court even if it drops them in the ITC proceeding.

contentions, one of the three challenged claims is not asserted in the ITC investigation, the ITC involves different evidentiary standards and burdens, and—most importantly—the ITC cannot invalidate a patent.[8] Accordingly, the Board should institute IPR based on the Petition, which presents strong arguments for unpatentability.

The **first *Fintiv* factor (stay)** is neutral, because the ITC favors suspension of remedial orders that conflict with an IPR decision (e.g., issued near the end of an ITC investigation) over staying investigations at the onset. *See In the Matter of Certain Unmanned Aerial Vehicles and Components Thereof*, ITC-337-TA-1133, 2020 WL 5407477, at *1, *20-*22 (ITC Sept. 8, 2020).

The **second *Fintiv* factor (proximity of trial)** is neutral, if not slightly for granting institution, because of Petitioner's diligence in filing the Petition. First, Petitioner filed its Petition ***less than three months*** after institution of the ITC

[8] Whether *NHK Spring* and *Fintiv* should apply to an ITC investigation was recently raised in a request for rehearing by the Board and the Precedential Opinion Panel in *Garmin Int'l, Inc. v. Koninklijke Philips N.V.*, IPR2020-00754, Paper 12 (Nov. 19, 2020).

investigation.[9] (Ex. 1018, 2.) Moreover, claims 13 and 15 of the '651 were not included in the original infringement contentions submitted by Patent Owner. Instead, they were recently added to the infringement contentions on February 1, 2021. Thus, this Petition was promptly filed less than three weeks after Patent Owner served its contentions adding those claims.

Second, the Board's institution decision will likely issue around August 2021, which is before the ITC's initial determination set for December 1, 2021 (Ex. 1023, 3). And, while the investigation hearing is set for August 16-20, 2021 (Ex. 1022, 1; Ex. 1023, 4) and the target completion date is set for April 1, 2022 (Ex. 1021, 2), those dates are "subject to change because of restrictions and uncertainty due to the COVID-19 pandemic" (*id.*, 2; Ex. 1022, 2). Indeed, the ITC has recently delayed a significant number of investigations in which a violation was found. (*See, e.g.*, Ex. 1024.)

Third, the hearing before the ALJ is merely the initial step in the ITC's decisional process. *See* 19 C.F.R. § 210.36(a). The ALJ's initial determination is subject to a review by the full Commission, which must issue a final determination. *Id.* §§ 210.43(d), 210.45-46. Additionally, if the Commission finds a violation, it

[9] PO amended its complaint on October 23, 2020, and further supplemented it in November 2020. (Ex. 1018.)

must "transmit" a copy of its final determination and recommended actions (together with the full record) to the President, *see* 19 U.S.C. § 1337(j)(1)(B), and only upon the President's approval or the expiration of the 60-day presidential review period would the ITC's final determination become final (and subject to appeal), *see id.* § 1337(j)(4). Thus, even though the target completion date in the ITC Investigation is set to predate the Board's final written decision, the ultimate completion of the investigation will occur closer to and possibly after the Board's final written decision (per typical Commission extensions).

The **third *Fintiv* factor (investment)** weighs in favor of institution. To date, the ITC investigation is in its infancy and thus the Commission and parties have not yet invested substantial resources. (Ex. 1023, 2; Ex. 1017.) While activity in the investigation will subsequently increase at a pace typical of ITC actions, Samsung's diligence in filing this Petition—***less than three months after investigation institution and less than three weeks after the addition of claims 13 and 15***—weighs against discretionary denial. (Ex. 1018, 2.) *See Philip Morris Prods., S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 at 10 (Nov. 16, 2020); *Fintiv*, Paper 11 at 11. Concluding otherwise would mean that this factor would always weigh against institution when there is a parallel ITC investigation because such investigations always require a rapid investment of resources at the outset.

The **fourth *Fintiv* factor (overlap)** weighs strongly in favor of institution. Claim 14 of the '651 patent is not at issue in the ITC investigation (Ex. 1017; Ex. 1018, 2), and resolution of the investigation will not resolve the parties' dispute concerning patentability of claim 14, which is challenged in the Petition. *See Samsung Elecs. Co. Ltd. v. Dynamics Inc.*, IPR2020-00505, Paper 11 at 13 (Aug. 12, 2020).

Moreover, the ITC investigation does "not render [this] proceeding duplicative or … a waste of the Board's resources," because the ITC involves "differen[t] … evidentiary standards and burdens" and "does not have the authority to invalidate a patent." *Samsung Elecs. Co., Ltd. v. BitMicro, LLC*, IPR2018-01410, Paper 14 at 18 (Jan. 23, 2019); *see also Bio-Tech. Gen. Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996) (The ITC cannot "set aside a patent as being invalid [and/or] render it unenforceable."). Indeed, even if the ITC finds any of the challenged claims invalid, PO can still assert those claims in district court. *See Renesas Elecs. Corp. v. Broadcom Corp.*, IPR2019-01040, Paper 9 at 7-8 (Nov. 13, 2019). That PO's predecessor unsuccessfully sued Samsung on invalid patents in the recent past strongly suggests it may do so again here. *See Imperium IP Holdings (Cayman) Ltd. v. Samsung Electronics Co., Ltd.*, 757 Fed. Appx. 974, 980 (Fed. Cir. 2019).

The **sixth *Fintiv* factor (other circumstances)** likewise weighs strongly in favor institution. As demonstrated above (*supra* Section IX), the Petition presents strong arguments for unpatentability of the challenged claims. *See Dynamics*, Paper 11 at 14 (finding the "merits of the case weigh in favor" of institution). Thus, institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). Indeed, this Petition is the ***sole*** challenge to claims 13-15 of the '651 patent before the Board—a "crucial fact" favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020). And there is currently no district court litigation to serve as an alternative forum that can issue a binding decision on the validity of the '651 patent.

Accordingly, based on a "holistic view of whether efficiency and integrity of the system are best served," the facts here weigh against exercising discretion under § 314(a) to deny institution. *Dynamics*, Paper No. 11 at 15. While factor 5 (parties) usually weighs against institution, the remaining factors are at least neutral (factors 1 and 2) or favor institution (factors 3, 4, and 6). Plus, the fact that this proceeding is not duplicative or a waste of the Board's resources (factor 4) and the strength of Petitioner's unpatentability positions (factor 6) outweigh other applicable factors, such as if the ITC investigation concludes before the final written decision is issued in this proceeding (factor 2) or if there were great investment in the ITC investigation

(factor 3)—which typically occur when there is a parallel ITC investigation. *See 3Shape A/S v. Align Tech., Inc.*, IPR2020-00223, Paper 12 at 33-34 (May 26, 2020). Thus, institution here is proper.

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 13-15 of the '651 patent based on each of the grounds specified in this petition.

Respectfully submitted,

Dated: February 18, 2021 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,838,651 contains, as measured by the word-processing system used to prepare this paper, 11,593 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: February 18, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on February 18, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,838,651 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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