IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Micron Technology, Inc.; Micron Semiconductor Products, Inc.;
and Micron Technology Texas LLC

Petitioners,

v.

Unification Technologies LLC,

Patent Owner.

Case No. IPR2021-00940

U.S. Patent No. 8,533,406

PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 15-21 AND 26 OF U.S. PATENT NO. 8,533,406

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PETITIONERS' EXHIBIT LIST

Ex. No.	Brief Description
1001	U.S. Pat. No. 8,533,406 B2, titled "APPARATUS, SYSTEM, AND METHOD FOR IDENTIFYING DATA THAT IS NO LONGER IN USE," to Flynn et al.
1002	U.S. Provisional Pat. App. No. 60/912,728, titled "REMOVE-ON-DELETE TECHNOLOGIES FOR SOLID STATE DRIVE OPTIMIZATION," to Frank Shu et al. ("Shu Provisional").
1003	U.S. Pat. No. 9,207,876, titled "Remove-On-Delete Technologies for Solid State Drive Optimization," to Frank Shu et al. ("Shu Patent").
1004	Expert Declaration of Jacob Baker, Ph.D., P.E., Regarding U.S. Patent No. 8,533,406 (June 4, 2021).
1005	American National Standard for Information Technology—ATA/ATAPI Command Set – 2 (ACS-2), ANSI INCITS 482-2012 (May 30, 2012) (excerpts filed with permission).
1006	Serial ATA: High Speed Serialized AT Attachment Revision 1.0, Serial ATA International Organization (Aug. 29, 2001).
1007	Serial ATA (SATA) ATA Revision 2.5, Serial ATA International Organization (Oct. 27, 2005).
1008	William D. Brown & Joe E. Brewer, *Nonvolatile Semiconductor Memory Technology* (IEEE 1998).
1009	Brian Dipert & Markus Levy, *Designing with FLASH MEMORY* (Annabooks 1994).
1010	April 2007 Plenary Minutes 2, e07156r0 (T13 and INCITS, Apr. 24, 2007).
1011	U.S. Pat. No. 8,762,658, titled "SYSTEMS AND METHODS FOR PERSISTENT DEALLOCATION," to Flynn et al.
1012	Original Complaint for Patent Infringement, *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020), ECF No. 1.
1013	Exhibit B to Plaintiff's First Amended Infringement Contentions: Unification Technologies' Allegations of Infringement with Respect to U.S. Patent No. 8,533,406, *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020).

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1015	U.S. Provisional Pat. No. 60/873,111, titled "Elemental Blade System," to Flynn et al. (Dec. 6, 2006) ("2006 Provisional").
1016	Docket Report for *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020) (accessed June 3, 2021).
1017	Frank Shu, *Notification of Deleted Data Proposal for ATA8-ACS2*, T13 (rev. 0, Apr. 21, 2007).
1018	Frank Shu & Nathan Obr, *Data Set Management Commands Proposal for ATA8-ACS2*, T13 (rev. 1, July 26, 2007).
1019	Excerpt of Plaintiff's Responses to Defendant's First Set of Interrogatories (No. 16) (April 26, 2021), *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020).
1020	Eran Gal et al., *Mapping Structures for Flash Memories: Techniques and Open Problems*, PROCEEDINGS OF THE IEEE INTERNATIONAL CONFERENCE ON SOFTWARE—SCIENCE, TECHNOLOGY & ENGINEERING ("SwSTE'05") (digital version), Herzlia, Israel, 2005, pp. 83-92, doi: 10.1109/SWSTE.2005.14.
1021	Public file history of U.S. Pat. No. 8,533,406, titled "APPARATUS, SYSTEM, AND METHOD FOR IDENTIFYING DATA THAT IS NO LONGER IN USE," to Flynn et al.
1022	Frank Shu, Solid-State Drives: Next-Generation Storage, Microsoft WinHEC 2007 (May 14-17, 2007).
1023	Wayback Machine Archive of Microsoft WinHEC 2007 Conference Presentations Website, captured Sept. 12, 2007, https://web.archive.org/web/20070214023104/http://www.microsoft.com/whdc/winhec.
1024	Frank Shu, Windows 7 Enhancements for Solid-State Drives, Microsoft WinHEC 2008 (Nov. 4-6, 2008).
1025	U.S. Pat. No. 5,404,485A, titled "FLASH FILE SYSTEM," to Ban.
1026	Curriculum vitae of Jacob Baker, Ph.D., P.E. (June 2021).
1027	H. Niijima, *Design of a Solid-State File Using Flash EEPROM*, IBM JOURNAL OF RESEARCH AND DEVELOPMENT,

Ex. No.	Brief Description
	vol. 39, no. 5, pp. 531-45, Sept. 1995.
1028	U.S. Pat. No. 7,057,942, titled "MEMORY MANAGEMENT DEVICE AND MEMORY DEVICE" to Suda et al.
1029	U.S. Pat. No. 7,624,239, titled "METHODS FOR THE MANAGEMENT OF ERASE OPERATIONS IN NON-VOLATILE MEMORIES" to Bennett et al.
1030	Plaintiff's Reply Claim Construction Brief, *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020), ECF No. 57.
1031	Computer generated redline comparison of changes from the Shu Provisional to the Shu Patent.
1032	SD Specifications Part 1 PHYSICAL LAYER Simplified Specification Version 1.10, SD Group and SD Card Association Technical Committee (Mar. 18, 2005).
1033	U.S. Pat. 6,014,724, titled "FLASH TRANSLATION LAYER BLOCK INDICATION MAP REVISION SYSTEM AND METHOD," to Jenett.
1034	U.S. Provisional Pat. App. 60/974,470 for "Apparatus, System, And Method for Object-Oriented Solid-State Storage," to Flynn et al. ("Sept. '07 provisional").
1035	Claim Construction Order, *Unification Techs. LLC v. Micron Tech. Inc.*, No. 6:20-cv-500 (W.D. Tex. 2020), ECF No. 67.
1036	U.S. Pat. No. 6,677,432 B2, titled "MEMORY MANAGEMENT SYSTEM SUPPORTING OBJECT DELETION IN NON-VOLATILE MEMORY," to Saltz et al.
1037	U.S. Pat. No. 9,632,727 B2, titled "SYSTEMS AND METHODS FOR IDENTIFYING STORAGE RESOURCES THAT ARE NOT IN USE," to Flynn et al.
1038	IDS submitted on September 25, 2013 during prosecution of U.S. Pat. No. 8,762,658.
1039	Declaration of Frank Shu Regarding Publication of Proposals (Ex. 1018 and 1019) dated June 2, 2021.
1040	American National Standard for Information Technology—AT Attachment with Packet Interface – 7 Volume 1 – Register Delivered Command Set, Logical Register Set (ATA/ATAPI-7 V1), ANSI INCITS 397-2005 (Feb. 7, 2005) (excerpts filed with permission).

I. Introduction

The challenged claims in the U.S. Patent No. 8,533,406 ("the '406 Patent") should never have issued. The fatal flaw for these claims arises from the classic scenario of an applicant filing claims in a manner unsupported by the broad, high-level disclosure of an earlier provisional application. When applying the proper priority date—here, the September 22, 2007 filing date of the second provisional application[1] (the "2007 Provisional," Ex. 1034)—intervening prior art invalidates the challenged claims.

The intervening prior art in this case is exceptionally strong. In co-pending litigation, Patent Owner alleges that challenged claims cover products that implement the "Trim" command. Here, the intervening prior art consists of Frank Shu's initial proposal of the accused Trim command (Ex. 1017) to the standards-setting Technical Committee 13 ("T13") and his U.S. Pat. No. 9,207,876 encompassing the same. Ex. 1003. Indeed, Frank Shu led Microsoft's efforts to announce that the popular Windows operating system would support Trim months

[1] Petitioners assume priority for the challenged claims is properly supported by the 2007 Provisional because the prior art included in the grounds herein predate September 22, 2007, but Petitioners reserve the right to challenge this assumption in the co-pending district court litigation.

before the assumed September 2007 priority date for the challenged claims. Ex. 1022 at 1, 2, 9; Ex. 1023 at 3; Ex. 1024 at 1, 2, 5.

Given these facts, the Board can easily resolve the present IPR challenge. If the Board finds that the earliest provisional application does not fully support the challenged claims, the claims are unquestionably invalid.

II. Petitioners Meet Standing and Eligibility Requirements for *Inter Partes* Review.

Petitioners certify under 37 C.F.R. § 42.104(a) that the '406 Patent "is available for *inter partes* review and that the petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition." The Patent Owner sued Petitioners for alleged infringement less than one year ago on June 5, 2020. Exs. 1012, 1016.

III. Prosecution History of the '406 Patent

On October 4, 2012, the applicant filed amendments to the claims and specification, stating, "The Applicants have inserted new paragraphs 226-231 to include subject matter disclosed in, and incorporated from … United States Provisional Patent Application No. 60/974,470, filed September 22, 2007." Ex. 1021 at 191.

During examination, the Examiner twice rejected representative claim 45 (issued as claim 15) and its dependent claims. Ex. 1021 at 962-63, 1032-33. In a non-final rejection, the Examiner cited Patent No. 6,014,724 to Jenett ("Jenett") for

sending a "file indication map" to anticipate the claimed "indication identifying data that can be erased." *Id.* at 967. To overcome Jenett, the applicant amended claim 45 to specify that the indication "comprises a logical identifier that is associated with the data structure by a storage client" and that "the logical identifier is mapped to a physical address of the data." *Id.* at 999. The applicant argued, as a result, that the claims "as amended herein are patentable over Jenett." *Id.* at 1003. As discussed in Section VI below, the earliest provisional application for the '406 Patent (the "2006 Provisional") provides no support for this amendment.

After the final rejection, the applicant again amended the claims to distinguish the publication 2007/0136555 to Sinclair. Ex. 1021 at 1032-33, 1036-37, 1245-48.

The applicant never informed the Examiner about Frank Shu's Trim Proposals during prosecution of the '406 Patent. Thus, the Examiner allowed the application, noting that "the art of record fails to teach or suggest receiving a message at a storage controller (or storage layer) comprising a logical identifier, where the message indicates that a client has deleted a blocks [sic] associated with the logical identifier." *Id.* at 1267. About two weeks after the '406 Patent issued, the applicant eventually submitted an IDS listing a later, sixth revision of the Trim Proposals during prosecution of the related '658 Patent. Ex. 1011 at 4; Ex. 1038 at 13 (IDS line D19); Ex. 1014.

IV. Technology Background

Flash memory is a form of solid-state nonvolatile computer memory. Flash memory is organized in erasable units called "blocks," which are made up of smaller "pages." Ex. 1004 (Expert Declaration of Jacob Baker, hereinafter "Baker") ¶ 107.

Since at least the early 1990s, the generic architecture of both flash (e.g., solid-state drive ("SSD")) and magnetic-platter (e.g. hard disk drive ("HDD")) mass-storage devices have included: 1) an interface, 2) a controller to manage data in the storage device, and 3) a storage medium in the form of flash memory or a magnetic platter. *E.g.*, Ex. 1009 at 66, Fig. 4.14 (reproduced below); Ex. 1025 at Fig. 1.

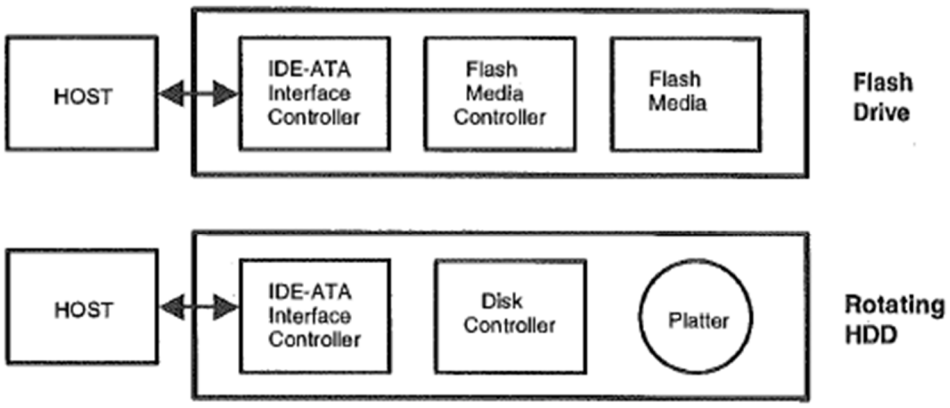


Figure 4.14: Mass Storage Architecture

Flash memory has long used a flash translation layer ("FTL") to map logical addresses to physical addresses. Baker ¶¶ 125-27; *see also, e.g.*, Ex. 1020 at 3, 9 (crediting Ban with patenting the FTL in 1995); Ex. 1025 (Ban's FTL patent); Ex. 1033, 5:21-26; Ex. 1015 at 77 (admitting that "[t]raditional" flash storage systems used FTL's like those patented by M-Systems, referring to Ex. 1025); Ex. 1027 Fig.

1 (showing direct and reverse Address Translation Tables between logical addresses ("LA") and physical addresses ("PA")). The FTL allows computer systems to operate and address data in a logical address space (e.g., logical address 0x0000 through 0xFFFF) without concern for where a solid-state storage device physically saves the data (e.g., in which particular block/page). Baker ¶ 128.

Unlike magnetic-platter hard drives, flash memory cannot be directly overwritten—a block must be erased before written to again. *Id.* ¶ 117. To improve an SSD's ability to identify and erase invalid data, Jenett invented sending file indication maps from an operating system to a flash memory controller so that the flash memory controller can track invalid blocks and erase them. Ex. 1033. Later, Frank Shu improved upon Jenett's idea and proposed that the operating system instead send the Trim command, which specifies the logical block addresses of invalid data, instead of sending an entire file indication map. Ex. 1007. Frank Shu then led Microsoft Windows to announce support for the Trim command. Ex. 1022 at 8; Ex. 1023; Ex. 1024 at 2, 4, 10. The industry would go on to adopt the Trim command as part of the ACS-2 standard. Ex. 1005 § 7.9.3.2.

V. Summary of the '406 Patent

Independent claim 15 recites an apparatus that includes a nonvolatile storage medium, a request receiver module, and a marking module. Ex. 1001, 54:13-27. The request receiver module receives "an indication that a data structure,

corresponding to data stored on the non-volatile storage medium, has been deleted." *Id.* The indication "comprises a logical identifier that is associated with the data structure." *Id.* The logical identifier "is mapped to a physical address of the data." *Id.* The marking module is configured to record that the data "can be erased … in response to receiving the indication." *Id.*

The Patent Owner contends that the "indication" in claim 15 covers Frank Shu's Trim command. Ex. 1013, *passim*.

VI. The '406 Patent's Priority Date Does Not Precede September 22, 2007

The 2006 Provisional cannot support the priority date for the challenged claims because it lacks support for two elements in claim 15: (1) "wherein the indication comprises a logical identifier that is associated with the data structure by a storage client," (2) the "marking module," configured as recited. The 2006 Provisional also fails to support the dependent claims. The Patent Owner contends that certain sections of the 2006 Provisional provide support (Ex. 1019 at 37-38), but each section lacks support for the reasons explained below. Thus the priority date for the challenged claims comes on or after September 22, 2007.

A. Priority Law Requires Every Element to Have Explicit, Implicit, or Inherent Support

To comply with the written description requirement of 35 U.S.C. § 112 and

receive an earlier priority date under 35 U.S.C. § 120,[2] each claim limitation must be expressly, implicitly, or inherently supported in the originally filed disclosure. MPEP § 2163(II)(A)(3)(b). That original disclosure "must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed." *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005). "In other words, the specification of the *provisional* must 'contain a written description of the invention and the manner and process of making and using it, in such full, clear, concise, and exact terms,' 35 U.S.C. § 112 ¶ 1, to enable an ordinary skilled artisan to practice the invention *claimed* in the *non-provisional* application." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). One skilled in the art, reading the original disclosure, "must immediately discern the limitation at issue in the claims." *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323 (Fed. Cir. 2000).

The written description requirement "guards against the inventor's overreaching by insisting that he recount his invention in such detail that his future claims can be determined to be encompassed within his original creation." *Vas-Cath*

[2] Nothing in 35 U.S.C. § 112 or § 120 allows the Patent Owner to provide support by arguing that the claims were obvious under § 103 in view of a provisional.

Inc. v. Mahurkar, 935 F.2d 1555, 1561 (Fed. Cir. 1991). If the originally filed disclosure does not provide support for each claim limitation, a priority or benefit claim under 35 U.S.C. § 120 must be denied. MPEP § 2163(II)(A)(3)(b).

Narrowing the claims by introducing elements or limitations that are not supported by the as-filed disclosure is a violation of the written description requirement of pre-AIA 35 U.S.C. § 112. MPEP § 2163.05(II); *see, e.g.*, *Rozbicki v. Chiang*, 590 F. App'x 990, 996 (Fed. Cir. 2014) (nonprecedential) (finding that patentee "cannot now improperly narrow its language by importing limitations not supported by the claim language or written description").

When an explicit limitation in a claim "is not present in the written description whose benefit is sought[,] it must be shown that a person of ordinary skill would have understood, at the time the patent application was filed, that the description *requires* that limitation." MPEP § 2163(II)(A)(3)(b) (citing cases) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted). A subgenus is not necessarily implicitly described by a genus encompassing it and a species upon which it reads. *Application of Smith*, 458 F.2d 1389, 1395, 173 USPQ 679, 683 (CCPA 1972). "[O]ne cannot disclose a forest in the original application, and then later pick a tree out of the forest and say

here is my invention. In order to satisfy the written description requirement, the blaze marks directing the skilled artisan to that tree must be in the originally filed disclosure." *Purdue Pharma*, 230 F.3d at 1326-27.

When filing an amendment to pending claims "an applicant should show support in the original disclosure for new or amended claims." MPEP § 2163(II)(A)(3)(b); *see also* MPEP §§ 714.02 and 2163.06 ("Applicant should ... specifically point out the support for any amendments made to the disclosure."). The applicant here never argued that the claim amendments at issue are supported by the 2006 Provisional. Ex. 1021 at 996-1003.

B. Summary of the 2006 Provisional

The 2006 Provisional contains a scattershot of separate ideas catalogued as "claims," none of which match the '406 Patent claims. *Compare* Ex. 1015, *with* Ex. 1001. Most of these "claims" in the 2006 Provisional have nothing to do with the challenged claims. *See, e.g.,* Ex. 1015, 10-22 (describing "identical card pairings" for pairing together cards in a blade server chassis), 24 (describing a business model of leasing storage to third parties).

The Patent Owner asserts in the co-pending litigation that the 2006 Provisional's "claim" 18 provides § 112 support for related patents asserted against the same products, and the Patent Owner appears to rely on the same provisional disclosure for the '406 Patent. Ex. 1030 at 10-11 (highlighting the "empty block"

directive of provisional "claim" 18).

"Claim" 18 of the 2006 Provisional presents a high level problem and solution. The problem: "Garbage collection based storage systems such as those commonly used with NAND flash get very poor performance when they do not have enough free space." Ex. 1015 at 40. The stated solution references an "empty-block directive" or "hint":

> ***Statement of Solution***
>
> **Most agents that use block storage do not need the contents of every block to be preserved. File systems, for example, are rarely filled to near the capacity of the block storage on which they are storing the data. If the file system were to supply a hint to the block storage regarding which specific blocks do not hold data that needs to be preserved, the efficiency of the garbage collection on the underlying block storage system can be greatly enhanced.**
>
> **The empty-block directive can be added to the block storage API and protocols. File systems and other clients of that API/protocol can be enhanced to issue these directives. For example, when a file is deleted, the file-system can issue an "empty-block" directive for the blocks that contained the data for that file, but no longer need to remember the contents. This directive could even serve a secondary security purpose by incorporating a flag to indicate that the data not only need not be preserved, but should be destroyed.**

Id. The applicant also provided an "alternative" solution. In the alternative solution, instead of sending the hint/command, the 2006 Provisional states that agents can write zeros to the storage medium, thereby overwriting the blocks whose contents are no longer needed:

> **An alternative to introducing this empty-block directive could be to have the agents simply write all zeros to the blocks whose contents are no longer needed. The underlying block storage system can recognize all-zero blocks and avoid having to actually store the contents. Subsequent reads can return the same all-zero data. Certain file systems such as XFS, for security purposes, have options for zeroing out the blocks that held data from deleted files. Simply enabling those options could be sufficient to allow garbage collection based block storage systems to achieve high efficiency by interpreting those zeroed blocks as "free". Or, those file systems could be enhanced to issue an "empty-block" directive in place of zeroing the blocks.**

Id.

C. The 2006 Provisional Has No Support for "wherein the indication comprises a logical identifier that is associated with the data structure by a storage client"

As explained in Section IV above, Jenett invented sending a file indication map to an SSD to indicate invalid data, and in April 2007, Frank Shu proposed that this type of command should identify the specific logical block address of invalid data (instead of sending a whole file indication map). Ex. 1033; Ex. 1017. The 2006 Provisional lacks any disclosure of this concept.

Indeed, the 2006 Provisional has no disclosure about the structure of the "hint" or "empty-block" directive other than it could incorporate "a flag" that indicates whether data should be destroyed. Baker ¶ 67. Nowhere does the 2006 Provisional state that the "empty-block" hint/directive should comprise "a logical identifier that is associated with the data structure by a storage client." *Id.*, ¶¶ 67-84. At best, the 2006 Provisional describes a hint "regarding which specific blocks do not hold data" and that "file-systems can issue an 'empty-block' directive for the blocks that contained data for that file." Ex. 1015 at 40. But this disclosure falls short of disclosing that the hint or directive uses or "comprises a logical identifier that is associated with the data structure by a storage client" for identifying such blocks, as opposed to identifying the blocks some other way. Baker ¶ 66-67. For these reasons, a POSITA would not have understood "claim" 18 of the 2006 Provisional to explicitly teach that the "indication comprises a logical identifier." *Id*. Thus, the

2006 Provisional contains no explicit support of "the indication comprises a logical identifier that is associated with the data structure by a storage client" as recited in the challenged claims. *Id.* ¶¶ 66-69.

Nor does the 2006 Provisional provide an inherent or implicit disclosure of the empty-block hint/directive comprising a logical identifier. Baker Baker ¶ 68-69. In a related patent, the applicant claimed the empty-block directive separately from logical block addresses. Ex. 1037, 54:55-56. The '406 Patent discloses that some commands use physical addresses, not logical addresses, to identify blocks. Ex. 1001, 14:55-57, 17:42-50, 21:1-11, 34:63-65. Based on this disclosure, a POSITA would have recognized that a hint or directive might have identified a physical address instead of the claimed logical identifier. Baker ¶ 69. Indeed, a POSITA would have recognized even more alternatives for the structure of the hint or directive. *Id.* For example, a different instruction, separate from the hint or directive, could include the logical identifier, which is similar to how erase commands worked in the SD Specification. *Id.*; Ex. 1032 § 4.3.5 (requiring, in sequence, a command CMD32 to identify the START block, a separate command CMD33 to identify the END block, and finally the command CMD38 to ERASE the previously indicated blocks). As yet another example, Jenett solved this same problem by sending an entire "file indication map." Ex. 1033, Fig. 5 block 600, *passim*; Ex. 1021 at 936-37; Baker ¶ 69.

For these reasons, "claim" 18 of the 2006 Provisional fails to expressly, implicitly, or inherently disclose any of these options, much less the specific option that the hint or directive comprises "a logical identifier that is associated with the data structure by a storage client."

Patent Owner cannot salvage support from other parts of the 2006 Provisional. The alternative solution of writing zeros also makes no reference to using a logical identifier. Ex. 1015 at 40. Aside from "claim" 18, the only other 2006 Provisional "claims" that mention an empty-block hint/directive include "claims" 14 and 29. Baker ¶¶ 72, 79; Ex. 1015 at 35, 103. But, these "claims" discuss entirely different problems and solutions, and neither discloses a hint/directive comprises a logical identifier. Baker ¶¶ 72, 79; Ex. 1015 at 35, 103. Moreover, provisional "claim" 14 operates under an incompatible assumption—"that every block contains contents that must always be remembered—in other words, no block can be considered free space". Ex. 1015 at 35; Baker ¶ 70. If anything, provisional "claim" 14, titled "object based storage with garbage collection," shows that the inventors had not solved how to integrating object storage and garbage collection. Ex. 1015 at 35 (reciting incomplete sentences as the "solution"); Baker ¶ 72.

Furthermore, other passages in the 2006 Provisional mention a "logical block" in other contexts, but these parts also fail to describe an empty-block hint/directive involving a logical identifier. For example, "claims" 22 and 24 of the 2006

Provisional mention logical blocks *in a map* but say nothing about receiving logical identifiers with the empty-block hint/directive. Baker ¶¶ 71, 75; Ex. 1015 at 68, 72-74.

Additionally, to the extent that the Patent Owner refers to the 2006 Provisional's "claim" 30, this description involves object-based commands—a type of command different from block commands such as the empty-block hint/directive. Baker 80; Ex. 1015 at 104. Also, this provisional "claim" directs the POSITA away from block-based commands entirely because it purportedly gives the POSITA "a killer reason to change from block access to object access." Ex. 1015 at 104.; Baker ¶ 80. Provisional "claims" 31 and 32 also discuss an incompatible object-based system and provide no further detail about the empty-block hint/directive. Ex. 1015 at 105-06; Baker ¶ 80.

Provisional "claims" 22 and 23 mentions "messages," but these "messages" refer to "units on NAND flash," or encapsulated data on a media. Ex. 1015 at 69-70. "A message is written by placing commands on the command queues." *Id.* at 69. Thus, the disclosures about the structure of a "message" written in NAND in provisional "claims" 22 and 23 do not support the structure of a command like the empty-block hint/directive. Baker ¶¶ 74-75.

Provisional "claim" 27(E) relates to a "NAND controller" and a "NAND Write Agent." Ex. 1015 at 92. This "claim" relates to a controller command for

writing new data to pages of flash memory and has nothing to do with the empty-block hint/directive. Baker 77.

The Patent Owner also relies on provisional "claims" 2, 9, and 28, but likely only to support claimed hardware elements instead of the challenged element. Ex. 1015 at 23, 31. The remaining provisional "claims" 2, 9, and 28 cited by Patent Owner say nothing about the empty-block hint/directive. *Id.*; Baker ¶¶ 78, 83. The Patent Owner also relies on provisional "claims" 13, 25, and 33 which relate to garbage collection, but likely only to support the next challenged element, thus Section VI.D addresses these in more detail. Ex. 1015 at 35, 74-75, 113. Provisional "claims" 13, 25, and 33 say nothing about the empty-block hint/directive. *Id.*; Baker ¶¶ 73, 76, 81.

For these reasons, the 2006 Provisional fails to describe "a message comprising a logical identifier" in sufficient detail so that one skilled in the art could reasonably conclude that the applicant had possession of the claimed invention and thus fails to provide written description support for the challenged claims. Baker ¶ 84.

D. The 2006 Provisional Has No Support for the "Marking Module" Described in Claim 15

The 2006 Provisional makes no mention of a marking module configured to record "that the data … can be erased" in response to receiving the indication, as claimed in the '406 Patent. Ex. 1001, 54:24-27.

"Claim" 18 in the 2006 Provisional only discloses what the empty-block hint/directive signifies, not what to do afterward—especially not what a *marking module* is, or does, in response to the empty-block hint/directive. Ex. 1015 at 40; Baker ¶ 88. Assuming that the empty-block directive indicates that data "need not be preserved," or "should be destroyed," a POSITA would have either not preserved the data or would have destroyed the data. Ex. 1015 at 40; Baker ¶ 88. But nothing instructs the POSITA to make the claimed marking that data can be erased in response.

At best, the 2006 Provisional only mentions that because of the hint/directive, "the efficiency of the garbage collection on the underlying block storage system can be greatly enhanced." Ex. 1015 at 40. But the 2006 Provisional never explains how. Baker ¶ 89. The lack of this teaching leaves the implementation to the imagination of a POSITA, including whether to preserve the data or whether to destroy it, as signified by the empty-block hint/directive. Baker ¶ 88. In any event, the 2006 Provisional's disclosure fails to suggest the possibility of doing any marking in response to the empty-block hint/directive.

One alternative to performing any "marking" in response to the hint/directive, would be the flash memory immediately erasing the blocks and marking the blocks as already erased instead of "can be erased." Baker ¶ 90. Another alternative includes scheduling the blocks for mandatory erasure later, at a more convenient

time, instead of marking the blocks with the option of "can be erased." *Id*. Another alternative includes marking the logical or physical identifiers of the blocks, or both, as invalid without physically erasing the blocks. *Id*. Another alternative includes preserving the blocks because the disclosed hint permits preservation. *Id*. Another alternative includes removing the logical or physical identifier of the block from a mapping or index in the FTL. *Id*. Another alternative includes having storage module recover the physical storage location, instead of marking the location with a marking module. Ex. 1001, claim 26; Baker ¶ 90. Indeed the '406 Patent claims performing different actions in response to receiving an indication. Ex. 1001, claims 16-26. The 2006 Provisional fails to expressly, implicitly, or inherently disclose any of these options, much less the specific option to respond by having a marking module "record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium in response to receiving the indication." For these reasons, the provisional "claim" 18 fails to expressly, implicitly, or inherently disclose a marking module configured to record "that the data … can be erased" In response to the indication, as claimed. Baker ¶¶ 86-90.

Patent Owner cannot salvage support from other parts of the 2006 Provisional. For example, provisional "claim" 25 describes garbage collection that operates under the opposite, incompatible assumption: "Blocks are always considered valid,

their contents needing to be preserved, even if the client (say a file system) doesn't have anything useful stored in a given block." Ex. 1015 at 74; Baker ¶ 93. This incompatible assumption would have prevented a POSITA from combining provisional "claim" 18's "hint ... regarding which specific blocks do not hold data that needs to be preserved" with the garbage collection system of provisional "claim" 25. Ex. 1015 at 40, 74; Baker ¶ 93. This provisional "claim" also describes a different solution that occurs in response to a different condition: "Whenever data is appended to the medium, we identify the old data that is becoming garbage." Ex. 1015 at 75. This disclosure of identifying different data (old data) in response to a different condition (when new data is appended) cannot support the '406 Patent's claimed marking module that operates in response to the "indication that a data structure ... has been deleted." Baker ¶ 93.

Neither provisional "claims" 13 nor 33, which also relate to garbage collection, disclose performing any actions in response to the empty-block hint/directive. Ex. 1015 at 35, 113; Baker ¶¶ 95-96. Provisional "claim" 13 discusses a garbage collection snapshot system and, at best, vaguely references a "clear-block" directive on nonexistent page "xxx." Ex. 1015 at 35. Provisional "claim" 33 teaches eliminating revision numbers used during garbage collection. *Id.* at 113. These provisional "claims" 13 and 33 show no possession of a marking module configured to record "that the data … can be erased" in response to receiving

the empty-block hint/directive. Baker ¶¶ 95-96.

Provisional "claim" 29 relates to "Object Storage," and only briefly mentions "providing an 'empty-block' directive can additionally improve the efficiency of emulating a block device on top of object based storage that uses garbage collection underneath" without the further detail needed to support the claims. Baker ¶ 94; Ex. 1015 at 103. Provisional "claim" 29 says nothing about what happens during garbage collection in response to receiving the empty-block hint/directive. Baker ¶ 94.

Aside from provisional "claim" 18, only provisional "claims" 14 and 29 mention the same empty-block hint/directive, and neither provisional "claim" 14 nor claim 29 discloses a marking module recording anything in response to the empty-block hint/directive. Baker ¶ 94; Ex. 1015 at 35, 103. Provisional "claim" 14 provides an incomprehensible solution.

Provisional "claim" 24 relates to identifying "bad" blocks that are "no longer useable" due to defects, but this has nothing to do with the empty-block hint/directive. Ex. 1015 at 72; Baker ¶ 97.

None of the other parts of the 2006 Provisional support the challenged claim element. They are all directed to different ideas or incompatible for the reasons discussed in Section VI.C above.

For these reasons, the 2006 Provisional fails to describe a marking module

configured to record "that the data … can be erased" in response to receiving the indication in sufficient detail so that one skilled in the art could reasonably conclude that the applicants had possession of the claimed invention and thus fails to provide written description support for the challenged claims. Baker ¶¶ 85-98.

E. The Dependent Claims Similarly Lack Priority

Claims 16-21 and 26 depend from claim 15 and thus lack priority support to the 2006 Provisional because of dependency. Claims 16-21 and 26 independently lack priority support to the 2006 Provisional because the 2006 Provisional fails to describe any further details about the specific configuration of the claimed marking module as recited in claims 16-19 and 21, what removal of a mapping indicates as recited in claim 20, or what a storage module does as recited in claim 26. Baker ¶¶ 99-104.

Thus, the 2006 Provisional disclosure would not have conveyed possession of these dependent claims to a POSITA, and the priority claim to the 2006 Provisional "must be denied" for the dependent claims. *Id.*; MPEP § 2163(II)(A)(3)(b).

VII. Level of Ordinary Skill in the Art

A POSITA in September 2007 would have a Bachelor of Science degree in computer science or electrical engineering and at least two years of experience in the design, development, implementation, or management of solid-state memory devices. Baker, ¶ 57. The references cited in this Petition, the state of the art, and

the experience of Dr. Jacob Baker as described in his expert declaration (Ex. 1004) reflect this level of skill in the art. In this Petition, reference to a POSITA refers to a person with these or similar qualifications.

The POSITA in September 2007 would have also known about Frank Shu's Trim proposals to T13 and Microsoft's announcement to support Trim at WinHEC 2007. Baker, ¶ 59. The POSITA would also have known, as background information: how flash memory erases data, how flash memory programs or writes data, how memory is used in a cache hierarchy, relative speeds of flash memory compared to other memory, how garbage collection is used with flash memory, how to use wear leveling to combat endurance limits of flash memory, how the FTL works, and industry standards affecting flash memory, including the ATA standard. Baker, ¶ 58.

VIII. Claim Construction

The Board construes claims under the same claim construction standard as civil actions in federal district court. The district court for the co-pending litigation has construed certain terms. Ex. 1035. Although the parties have disputed the claim constructions, the construction disputes do not affect the outcome of this Petition.[3] The district court's constructions for the claims at issue in this Petition are as follows:

[3] Petitioners reserve all rights to appeal the district court's claim constructions.

Claim Term	Court's Final Construction
"logical identifier"	An identifier that can be associated with a physical address on a storage device for identifying data stored at the physical address.
"marking module"	Not indefinite; not subject to § 112(f); plain and ordinary meaning.

IX. Precise Relief Requested

A. Proposed Ground 1

Claims 15, 21, and 26 are rendered obvious by U.S. Pat. No. 9,207,876 to Frank Shu et al., (the "Shu Patent," Ex. 1003) in view of Frank Shu's Trim Proposals revisions 0-1 (Exs. 1017-1018), and U.S. Pat. No. 5,404,485 to Ban ("Ban," Ex. 1025).

B. Proposed Ground 2

Claims 16-20 are rendered obvious by the Shu Patent (Ex. 1003) in view of the Shu Trim Proposal revisions 0-1 (Exs. 1017-18), Ban (Ex. 1025), and U.S. Pat. No. 6,014,724 to Jenett ("Jenett," Ex. 1033).

C. Qualifying Prior Art

For the reasons discussed in Section VI, above, the challenged claims of the '406 Patent have an effective filing date no earlier than September 22, 2007.

The Shu Patent has priority to provisional application 60/912,728 ("Shu

Provisional"), filed on April 19, 2007, and is § 102(a) and (e) prior art. Ex. 1003; Ex. 1002. The Shu Patent contains minor edits in comparison to its provisional. Ex. 1031 (showing computer-generated comparison). As shown in the table, the Shu Provisional provides full support for the claims under 35 U.S.C. §§ 112, 120. Thus, the Shu Patent has priority to its provisional filing date.

Shu Patent Element	**Shu Provisional Support (Ex. 1002)**
1. A system comprising:	Fig. 3 (showing system).
[1a] a computing device that includes at least one processor and memory;	Fig. 3 (showing computing device 301, processing unit 307, memory 309), [0028].
[1b] a file system; and	Fig. 1 (showing file system 112b), [0014], [0016]-[0017].
[1c] a solid state drive ("SSD") driver that, based on execution by the at least one processor, is configured to:	Fig. 1 (showing SSD driver 114b), [0012]-[0014], [0016]-[0019], [0021], [0023], [0025]-[0027]. "Processor 307 typically processes or executes various computer-executable instructions to control the operation of computing device 301," which includes the operating system shown in Fig. 3, which includes the SSD driver shown in Fig. 1. [0026].
[1d1] receive, from a file system, a remove-on-delete command that includes invalid data information	Fig. 1 (showing SSD driver 114b, receiving the remove-on-delete command via interface 140, from the file system 112b), [0017] ("File system 112b uses new interface 140 to communicate invalid data information to SSD driver 114b."), [0023] ("Block 230 indicates a remove-on-delete command. This command typically includes the invalid data information and instructs the SSD device and/or its driver to mark the indicated data as invalid.")
[1d2] that indicates that, based on a deletion of at least a portion of a file in the file system, particular data that is stored on an SSD and	[0015] ("For example, when a file is deleted, the data associated with the file is invalid."); [0017] ("File system 112b utilizes new interface 140 to communicate invalid data information to SSD driver 114b. . . . Interface 140 enables file system 112b to indicate to SSD driver 114b via the invalid data

corresponds to the at least the portion of the file is, as indicated by the deletion, considered invalid by the file system; and	information exactly which data stored on SSD 130 are invalid."); [0014] (generally); Fig. 2 at 210-230; [0021] ("Block 210 indicates a delete event impacting data stored on the SSD device. One example of such a delete event is a file delete operation performed by a file system wherein the file is stored on an SSD device."); [0023] ("such a command is issued by the system performing the delete operation and an SSD driver.")
[1e] instruct, based on the received invalid data information, the SSD to mark the particular data invalid on the SSD.	Fig. 2 block 240, [0014], [0017], [0019] ("SSD driver 114b typically interacts with SSD 130 via interface 120b to mark appropriate data, blocks, pages, or the like as invalid."); [0020] ("Such a method may be used to mark deleted SSD data as invalid, otherwise known as 'remove-on-delete'."); [0023] ("Block 230 indicates a remove-on-delete command. This command typically . . . instructs the SSD device and/or its driver to mark the indicated data as invalid."); [0024] ("Block 240 indicates marking the deleted data as invalid.").

A pre-AIA 35 U.S.C. § 102(e) prior art reference "'shall have the same effect,' including a patent-defeating effect, . . . as though it was filed on the date of the . . . provisional" to which it claims priority, as long as certain requirements are met. *In re Giacomini*, 612 F.3d 1380, 1383-84 (Fed. Cir. 2010) (quoting 35 U.S.C. § 119(e)). In particular, the Board has held that a § 102(e) reference is available as prior art as of its provisional application's filing date when the provisional provides support for: (1) at least one claim of the § 102(e) reference and (2) the subject matter on which the petitioner relies. *Cisco Sys., Inc. v. Capella Photonics, Inc.*, IPR2014- 01276, Paper No. 40 at 21-22 (P.T.A.B. Feb. 17, 2016). With respect to the first prong, the provisional application must disclose an invention claimed in the § 102(e) reference

"in the manner provided by the first paragraph of section 112." 35 U.S.C. § 119(e)(1); *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). Only one claim from the later issued patent must be supported by the provisional. *See id*. at 22 n.9; *Polaris Indus., Inc. v. Arctic Cat Inc*., IPR2016-01713, Paper 9, at 13 (P.T.A.B. Feb. 27, 2017).

The Shu Trim Proposals published in April 2007 (rev. 0) and August 2007 (rev. 1) and qualify as prior art under § 102(a). Ex. 1010 § 8.1.2; Ex. 1017; Ex. 1018; Ex. 1039. T13 published the proposal on its freely accessible website T13.org, and industry representatives met to discuss Frank Shu's original Trim Proposal. Ex. 1010 § 8.1.2 (referencing the document number of Ex. 1017); Ex. 1039. Grounds 1 and 2 below include citations to the Shu Provisional to show that the provisional discloses the same technology described in the Shu Patent.

Ban issued in 1995 and qualifies as prior art under § 102(a), (b), and (e). Ex. 1025. Jenett issued in 2000 and qualifies as prior art under § 102(a), (b), and (e). Ex. 1033.

D. The Proposed Grounds Are Not Cumulative or Redundant

The grounds for trial presented in this Petition are not cumulative to issues already examined during prosecution. The applicant never informed the Patent Office about any of Frank Shu's Trim Proposals before the '406 Patent issued. The Patent Office did not know that the Patent Owner contends that the claims cover the

Trim command. So although the Examiner considered U.S. Publication 2008/0263305 to Shu et al., the Examiner lacked the supplemental, clarifying information that Frank Shu disclosed in the Trim Proposals as proposed herein.

The grounds for trial presented in this Petition are not cumulative to issues already examined in parallel IPR proceeding IPR2021-00343. The parallel IPR proceeding assumed, without conceding, the December 2006 priority date and thus did not raise Frank Shu's Trim proposals or the Shu Patent as prior art. The PTAB "recognizes that there may be circumstances in which more than one petition may be necessary, including, for example, ... when there is a dispute about priority date requiring arguments under multiple prior art references." PTAB Consolidated Trial Practice Guide at 59, available at www.uspto.gov/sites/default/files/documents/tpgnov.pdf (Nov. 2019).

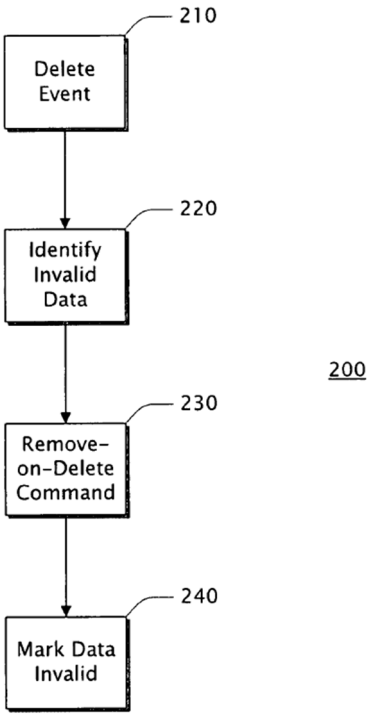
The *General Plastic* factors do not warrant denying this Petition. *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (P.T.A.B. Sept. 6, 2017). IPR2021-00343 relates to overlapping claims of the '406 Patent and was filed on December 22, 2020. At that time, investigation into the Shu Trim Proposals remained ongoing, and Petitioners did not have possession of relevant materials, such as Frank Shu's presentations (Ex. 1022, Ex. 1024) until recently. Patent Owner also delayed providing its priority contentions until late April, 2021. Ex. 1019. Discovery remains ongoing. The earlier IPR petition dealt with different prior art

and assumed a different priority date; thus, the Patent Owner's Preliminary Response to the earlier petition confers no unfair advantage here. The limited resources of the Board will be put to efficient use because the Board is already familiar with the technology and mainly needs to decide a priority date challenge to prevent the Patent Owner from unfairly using hindsight to capture Frank Shu's invention.

X. The Prior Art

A. Summary of the Shu Patent

The Shu Patent relates to managing SSDs with flash memory. Ex. 1003, 1:12-15. The Shu Patent teaches that SSDs might unnecessarily preserve invalid data during "wear leveling" and "merge" operations because SSDs "are generally unaware of what data ... is invalid." *Id.*, 1:20-43. Thus, the Shu Patent proposes that an operating system or file system send a "remove-on-delete" command to identify the invalid data to the SSD. *Id.*, 4:4-7, 4:51-5:4. The SSD can then mark the deleted data as invalid using "any form sufficient to identify the invalid data." *Id.*, 5:5-11. These invalid marks allow the SSD to avoid unnecessarily preserving the invalid data during wear leveling operations. *Id.*, abstract, 5:11-13. Shu Patent figure 2 shows the process:



B. Summary of Shu's Trim Proposals

In these Trim Proposals, Frank Shu proposes the "Trim" command, which corresponds to the "remove-on-delete" command described in the Shu Patent. Baker ¶¶ 155-56; Exs. 1017-1018. These Trim Proposals describe the Trim command that the Patent Owner now accuses of infringement. Exs. 1017-1018. The exact format of the Trim command varied across revisions, but all formats reserve bits for a logical block address ("LBA") and a "Count" field to indicate the starting address of data and a length of the data.

Word	Name	Description
00h	Feature	XXh
01h	Count	Number of 256 word-blocks of LBA Range Entry to be transferred. 0000h specifies that 65,536 blocks are to be transferred
02-04h	LBA	Reserved
05h	Command	XXh

Ex. 1017 § 3. Later revisions bundled the Trim command as part of the Data Set Management (DSM) command. Ex. 1018 § 6.1.1.

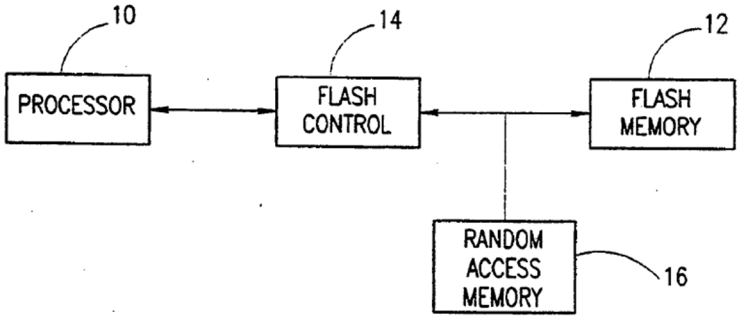
C. Summary of Ban

The industry widely credits Ban's 1995 patent as the invention of the modern flash translation layer, or "FTL." Ex. 1027 § 2.2 (citing "Ban [5]"); Ex. 1033, 1:50-53. The 2006 Provisional admits that M-System's patented FTL (referring to Ban, Ex. 1025), had become one of the "[t]raditional flash storage systems." Ex. 1015 at 77; Ex. 1025, cover (showing assignment to M-Systems).

In Ban's flash memory system, "[a] table, called a virtual map, converts virtual addresses to physical addresses." Ex. 1025, 2:6-8. The "virtual" address refers to the "computer generated address." *Id.*, 31-32. POSITAs also call this a "logical" address. Baker ¶ 162. Ban's map also tracks which data are "deleted and not writable." Ex. 1025, 4:47-50, 5:45-46, 5:64-66, 8:7-9.

This petition relies on Ban for showing the general components of a generic flash memory device that manages logical-to-physical mappings. Ban figure 1 shows that components include a flash memory controller and flash memory:

FIG.1



D. Summary of Jenett

The year after Ban issued, Jenett realized that Ban's system could be improved if the FTL avoided preserving deleted files. Ex. 1033, cover, abstract, background. Jenett identifies Ban's system with an FTL as the relevant background art to improve on. *Id.*, 1:50-53. Jenett teaches that an operating system sends a file indication map to the FTL, and the FTL compares the file indication map to an earlier version of the file indication map to identify which blocks are invalid, permitting erasure of those blocks. *Id.*, abstract, Fig. 4.

Jenett's figure 4 shows the "FTL structures," including the BAM (a block allocation map) stored in the flash memory card. Jenett's BAM "is a physical to virtual map which associates particular physical sectors of the flash medium with a related virtual address, provided that a relationship exists," just like Ban's FTL. Ex. 1033, 6:16-18. Jenett also teaches marking deleted data as "invalid." *Id.*, 3:11-13, 5:16-21, Fig. 3 block 404.

Jenett teaches various techniques for marking data invalid. One marking

technique includes making "the blocks associated with each deleted file invalid in the block allocation map." *Id.*, 4:56-57. As another marking technique, "block allocation map 501a(1) is updated to delete the association between the physical location at which the identified deleted file was stored and the virtual address formerly connected with the particular physical location." *Id.*, 6:12-16.

E. Motivation to Combine

The Shu Patent provides an explicit teaching to modify existing flash devices, such as Jenett's flash memory card or Ban's flash memory system, to use Shu's newly proposed remove-on-delete (Trim) command. The Shu Patent teaches to implement "new functionality" by sending the new remove-on-delete (Trim) command to identify invalid data to solid-state devices. Ex. 1003, 3:62-4:9, 4:35-41, 4:65-5:4. The Shu Patent teaches that the command could be sent to any type of SSD or flash memory device, especially those that perform wear leveling or merge operations. *Id.*, 1:20-32, 2:35-40, 2:52-67, 4:25-34.

Jenett and Ban provide examples of solid-state, flash memory devices that would benefit from receiving the new remove-on-delete command taught in the Shu Patent. Thus, a POSITA would have used a flash memory device, like the flash memory device from Jenett or Ban, to receive the remove-on-delete command. Baker ¶¶ 168-69. Jenett incorporated Ban by reference and instructs POSITAs to improve on Ban's system by sending a command used to identify invalid data. Ex.

1033, 1:46-56, 5:20-26. So like Shu, Jenett already had the same idea of identifying invalid data, albeit by sending a file indication map instead of a remove-on-delete/Trim command. Baker 1004 ¶¶ 169-70. Identifying invalid data would improve the performance by allowing the flash memory device to avoid "unnecessarily operating on invalid data," such as during merge operations. Ex. 1003, 3:8-17, 4:29-34. Ban shows an example where valid data is merged or transferred from an old block into a new block before erasing an old block. Ex. 1025, 2:61-3:2. Both the Shu Patent and Jenett address this same problem. Ex. 1003, 3:8-15; Ex. 1033, 1:12-21. Shu's remove-on-delete/Trim command identified the invalid data more efficiently, by specifying the starting logical block address and length of invalid data rather than sending an entire file indication map. Ex. 1003, 3:17-22; Ex. 1017 § 3; Baker ¶ 170. Once identified, invalid data will not be preserved during merge operations. Ex. 1003, 4:29-31.

Indeed, the PTAB need not speculate about a hypothetical POSITA's motivations because actual POSITAs in the solid-state industry applied the teachings of the Shu Patent to flash devices that used Ban's FTL. Frank Shu proposed his new Trim command to representatives of major companies in the flash storage industry. Ex. 1010 §§ 3.3, 8.1.2. Microsoft announced that the Windows operating system would support the command for SSDs. Ex. 1022 at 8. T13 considered and adopted the command. Ex. 1005 § 7.9.3.2.

A POSITA would have further turned to the Shu Trim Proposals (Exs. 1017-1018) for supplemental details about the operation of the remove-on-delete/Trim command, because Frank Shu submitted his Trim Proposals to T13, the organization responsible for the ATA standard. A POSITA would have looked to T13 submissions and wanted to comply with the ATA industry standards because the Shu Patent specified that the remove-on-delete/Trim command would use the ATA interface. Ex 1003, 2:49-51, 4:18-20, claims 7, 12, and 18; Ex. 1002 [0012], [0018].

Thus, a POSITA would have been motivated—and POSITAs were, in fact, motivated—to add support for Shu's new command to flash memory devices like those described in Jenett and Ban. Baker ¶¶ 168-70. When doing so, POSITAs would have looked to the Shu Trim Proposals for details about how the command would be implemented in the industry standard. *Id.* ¶¶ 171-72.

XI. Ground 1: Obvious Over the Shu Patent, the Shu Trim Proposal, Ban, and POSITA Knowledge

The Patent Owner accuses the Trim command, as used by generic SSDs, of infringing the claims. Ex. 1013, *passim*. But as explained in Section VI above, Frank Shu disclosed the Trim command to the public months before the applicant ever attempted to provide written description support for the asserted claims. Thus, Frank Shu's Trim Proposals, combined with details of a generic flash memory device (e.g., as shown in Ban), invalidate the claims under the Patent Owner's interpretation of the claims.

Petitioners allege in co-pending litigation that accused products that implement the TRIM command do not infringe, but for purposes of this IPR petition, use Patent Owner's interpretations. The Board and Federal Circuit has approved of this procedure in several matters. *See, e.g., Spherix Inc. v. Matal*, 703 F. App'x 982, 983 (Fed. Cir. 2017) (approving petitioner's proposal of patent owner's claim interpretations); *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (P.T.A.B. Nov. 10, 2020) ("Petitioner's alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review.").

A. Claim 15

a) Element 15[a]. An apparatus, comprising:

The Shu Patent discloses an apparatus in the form of a computer system with a solid-state storage device ("SSD"). Ex. 1003, Figs. 1 (cropped, reproduced below), 3 (reproduced below); Ex. 1002,[4] Figs. 1, 3; Baker ¶¶ 174-75.

[4] Citations to Exhibit 1002 show the Shu Patent's priority to its provisional.

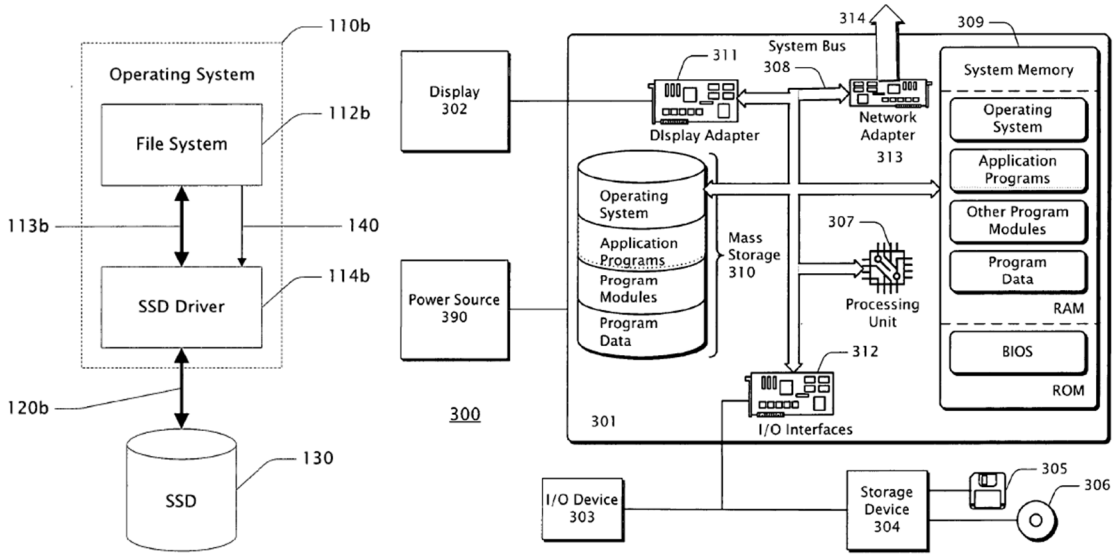


FIG. 3

b) Element 15[b]. a non-volatile storage medium;

The Shu Patent shows an SSD in figure 1 (reproduced above) and discloses, "SSDs are commonly fabricated to include flash memory devices, such as nonvolatile flash memory devices including Not AND ('NAND') type devices." Ex. 1003, 1:13-16; *see also id.* at 2:52-57; Ex. 1002, [0001], [0013]. Thus, a POSITA would have understood Shu's SSD in figure 1 and Shu's storage device in figure 3 to have included a nonvolatile storage medium in the form of nonvolatile NAND flash memory. Baker ¶ 177.

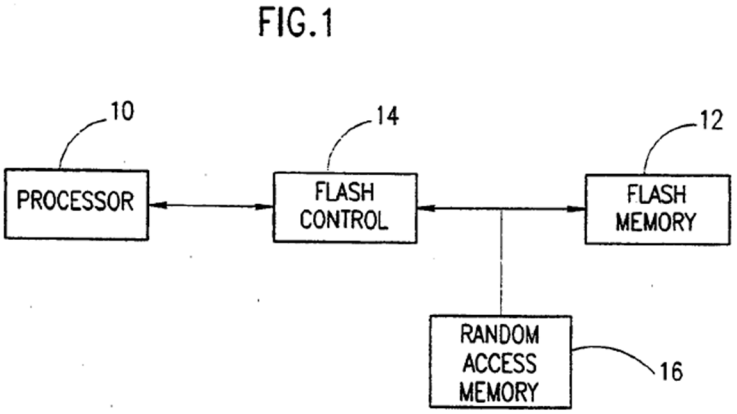
c) Element 15[c]. a request receiver module of a storage layer for the non-volatile storage medium …

The Patent Owner accuses the serial ATA ("SATA") interface of infringing this element and contends that the storage layer refers to "the part of the Accused [] Product that implements storage operations[] that includes circuitry, software, and/or firmware for receiving information over a SATA bus." Ex. 1013 at 2.

The Shu Patent teaches the same thing. Figures 1 and 3 of the Shu Patent show an SSD interfacing with a host to receive commands, including receiving a "remove-on-delete" (Trim) command. Ex. 1003, abstract, 1:60-63, 3:20-22, 4:35-38, 4:65-5:4; Ex. 1002 at 23, [0003], [0014], [0020], [0023]. The Shu Patent further teaches that interfaces for receiving commands "include the advanced technology attachment ('ATA') interface." Ex. 1003, 2:49-51; Ex. 1002, [0012]. A POSITA would have understood this mention of the ATA interface refers to both the same SATA interface accused by the Patent Owner and the parallel ATA (PATA) interface. Baker ¶ 180. Moreover, Frank Shu presented his Trim Proposal to T13, which sets the ATA standard used by SATA. Ex. 1017-1018 (proposing the command for inclusion in the ATA8-ACS2 standard, used by SATA). Thus, POSITAs in the industry knew about Frank Shu's proposal to include the Trim command in the ATA standard used by SATA. Baker ¶¶ 180-81. For these reasons, a POSITA would have found it obvious that the SSD in the Shu Patent has a SATA interface as the claimed "request receiver module of a storage layer for the non-volatile storage medium." Baker ¶ 181.

To the extent the Patent Owner argues the claimed "module" requires "circuitry, software, and/or firmware," this would have been obvious to a POSITA. Ex. 1013 at 2 (interpreting the "request receiver module" as "circuitry, software, and/or firmware"). A SATA interface is a type of circuitry. Additionally, although

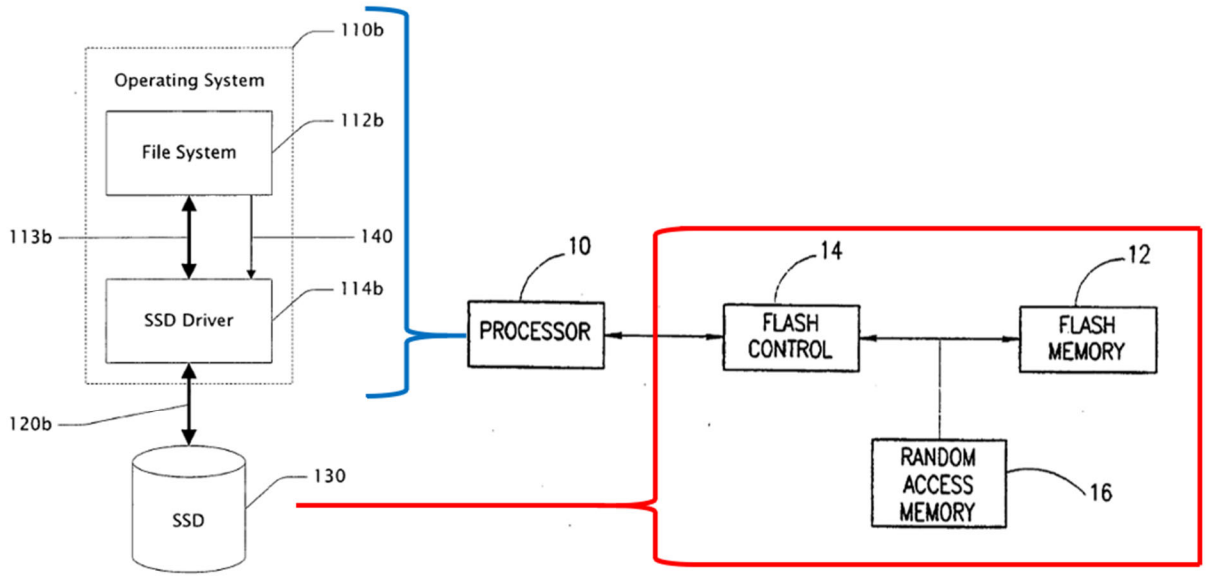
the Shu Patent does not detail the inner components of the SSD, a POSITA would have known that SSDs at the time generally included a memory controller and flash memory as shown in figure 1 of Ban. Ex. 1025, Fig. 1 (reproduced below); *see also supra* Section VI, (explaining the basic components).



These components form a circuit that "writes data to, and read data from, a flash memory," and the functions "may be carried out in software, firmware, or hardware." Ex. 1025, 3:60-61, 4:7-10. Thus, by applying the Patent Owner's interpretation, a POSITA would have understood the part of the Shu Patent's SSD with a SATA interface that receives the remove-on-delete (Trim) command (a storage operation) to include "circuitry, software, and/or firmware for receiving information over a SATA bus," as pictured below. Baker ¶ 182..

From Shu Patent, Fig. 1

From Ban, Fig. 1

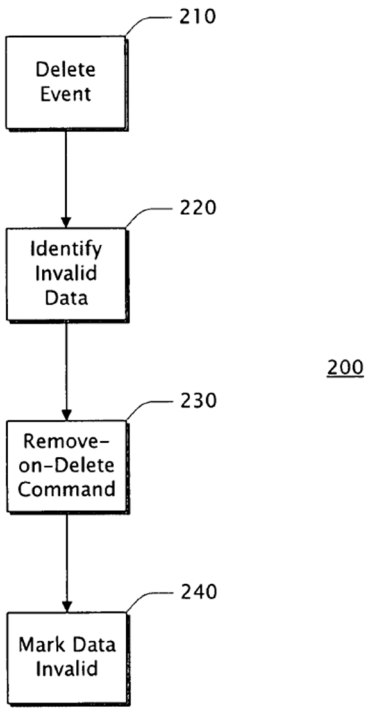


Ban shows the generic components in Shu's SSD

d) Element 15[d]. a request receiver module … configured to receive an indication that a data structure, corresponding to data stored on the non-volatile storage medium, has been deleted,

The Patent Owner accuses the remove-on-delete (Trim) command of infringing the '406 Patent. Ex. 1013 at 2. But because the '406 Patent lacks priority to the 2006 Provisional as explained in Section VI above, the accused command is prior art against this element under the Patent Owner's own theory, regardless of how the Patent Owner construes this element.

The Shu Patent teaches that the SSD is configured to receive a "remove-on-delete" command. Ex. 1003, abstract, 1:60-63, 3:20-22, 4:35-38, 4:65-5:4, Fig. 2 block 230 (reproduced below); Ex. 1002 at 23, [0013], [0014], [0020], [0023], Fig. 2.



An SSD receives this command when:

> A user, such as a person or system, may indicate via any suitable interface that some data, such as a file, should be deleted. The file system typically modifies a persistent data structure indicating the file has been deleted, such as by removing a reference to the deleted file from a directory or the like. Further, the file system may mark the data representing the file on the SSD as invalid. In one example, this includes sending file location information indicating the beginning of the file via logical block addressing ("LBA") typically followed by the length of the file to the SSD. The LBA or data location information describing the data to be deleted is typically sent by command via an interface to the SSD device. Upon receiving the command

> and associated data location information, the SSD and/or its driver can mark as invalid data stored on the SSD that corresponds to the deleted file.
>
> As used herein, invalid data may be data stored in memory locations, such as SSD memory locations, that have been deleted by a higher-level system, such as a file system, driver, application, or the like, or that are unused, or the like. For example, when a file is deleted, the data associated with the file may be considered invalid.

Ex. 1003, 3:8-25, 3:48-53; *see also id.*, 1:32-34, 1:55-63, 4:35-38, 5:3-11; Ex. 1002, [0014]-[0015]; *see also id.*, [0001], [0003], [0020], [0023]-[0024].

A POSITA would have recognized this "remove-on-delete" in the Shu Patent as the same "Trim" command proposed by Frank Shu to T13. Baker ¶¶ 155-56; Exs. 1017-1018. Both the "remove-on-delete" command and the Trim command have the same format (specifying an LBA), originated from the same person (Frank Shu), published around the same time (in April 2007), and do the same thing (identify invalid data stored on an SSD). Ex. 1003, 3:17-20; Ex. 1002, [0014]; Ex. 1017 § 3; Ex. 1018 § 6.1.1.

Thus, by applying the Patent Owner's interpretations, a POSITA would have found this element obvious. Baker ¶¶ 187-88.

e) Element 15[e]. wherein the indication comprises a logical identifier that is associated with the data structure by a storage client,

As best understood, the Patent Owner accuses the Trim command of infringing this element by specifying a logical block address ("LBA") associated with a document that has been deleted in a computer. Ex. 1013 at 2. But because the '406 Patent lacks priority to the 2006 Provisional as explained in Section VI above, the accused command is prior art against this element under the Patent Owner's own theory, regardless of how the Patent Owner construes this element.

First, a POSITA would have understood that found it explicit or obvious that the indication comprises a logical identifier. Ex. 1003, 3:17-22 ("In one example, this includes sending file location information indicating the beginning of the file via logical block addressing ('LBA') typically followed by the length of the file to the SSD"); Ex. 1002, [0014]; Baker ¶ 190. Although this sentence of the Shu Patent does not explicitly mention the "remove-on-delete" or "Trim" command, to the extent the Shu Patent is unclear about what contains the LBA, a POSITA would have seen that Frank Shu clarified in his proposal that the Trim command is what contains the LBA. Ex. 1017 §§ 2-3 (describing same format using LBAs); Ex. 1018 § 6; Baker ¶ 190.

Second, the Patent Owner contends that an example of the claimed "storage client" includes "a computer." Ex. 1013 at 2. The Shu Patent also discloses "a

personal computer" with an operating system or file system that sends the remove-on-delete/Trim command to the SSD. Ex. 1003, 5:23-32, Figs. 1, 3; Ex. 1002, [0025], Figs. 1, 3. This computer operating system sets the LBA in the remove-on-delete/Trim command. Ex. 1003, 3:15-20, Fig. 1; Ex. 1002, [0014], Fig. 1.

Finally, as best understood, the Patent Owner interprets the claimed "data structure" to include a file, such as a "document." Ex. 1013 at 2 (asserting, "From the user's perspective, this data has been deleted from a document."). The Shu Patent discloses that an operating system's file system "typically manages the abstraction of data as files, folders, properties, and the like," and the remove-on-delete (Trim) command is sent when "[a] user, such as a person or system, may indicate via any suitable interface that some data, such as a file, should be deleted." Ex. 1003, 2:42-44, 3:9-11, 3:22-25; Ex. 1002, [0012], [0014]. The computer system associates these files with the LBA and a length specified in the remove-on-delete command, so the logical identifier "is associated with the data structure by a storage client" as claimed. Ex. 1003, 3:17-20; Ex. 1002, [0014].

Thus, by applying the Patent Owner's interpretations, a POSITA would have found this element obvious. Baker ¶¶ 190-93.

f) Element 15[f]. and wherein the logical identifier is mapped to a physical address of the data on the non-volatile storage medium; and

The Shu Patent discloses "mapping the data of the file being deleted to the

corresponding data stored on an SSD." Ex. 1003, 4:51-54; Ex. 1002, [0022]. A POSITA would have understood this "mapping" to refer to the correspondence of the logical block address specified in the remove-on-delete command to the physical "blocks, pages" in the SSD where data are stored. Baker ¶ 194; Ex. 1003, 3:17-22, 4:51-61; Ex. 1002, [0014], [0022]. Frank Shu further clarified this concept in his Trim Proposal. Ex. 1017 at 3 ("A[] device will further remap LBA to its internal page and block for SSD"). Thus, a POSITA would have found this element obvious. Baker ¶¶ 194-95.

g) Element 15[g]. a marking module configured to record that the data stored at the physical address mapped to the logical identifier can be erased from the non-volatile storage medium in response to receiving the indication.

As best understood, the Patent Owner alleges this element is infringed if data is marked invalid. Ex. 1013 at 5 (providing further detail in dependent claim 5). But because the '406 Patent lacks priority to the 2006 Provisional as explained in Section VI above, the alleged infringement is prior art against this element under the Patent Owner's own theory, regardless of how the Patent Owner construes this element.

The Shu Patent discloses "marking the deleted data stored on the SSD as invalid such that the SSD can avoid unnecessary operations on the invalid data." Ex. 1003, 1:55-59; Ex. 1002, [0003]; *see* '406 Patent Claim 16 (marking is performed "by invalidating an association"); *see also* Ex. 1003, 1:60-63 ("identify the corresponding SSD data to be marked as invalid"), 3:22-25 ("Upon receiving the

command and associated data location information, the SSD and/or its driver can mark as invalid data stored on the SSD that corresponds to the deleted file."), 5:5-17 (explaining how marking invalid can take any form); Ex. 1002, [0003], [0014], [0024].

The Shu Patent does not require data marked "invalid" to be immediately removed or erased. Ex. 1003, 3:53-55; Ex. 1002, [0015]. Data marked "invalid" may remain stored in the storage device and will not be moved and preserved during future "merge" operations but, alternatively, may be "garbage collected,"[5] removed, overwritten, or the like. Ex. 1003, 3:35-44, 3:55-58, 4:38-39; Ex. 1002, [0014], [0020]. Thus, by applying the Patent Owner's interpretations, the prior art renders obvious to record "that the data … can be erased from the non-volatile storage medium," as claimed. Baker ¶ 198.

The Shu Patent further discloses, "Given the invalid data information, SSD drive 114b typically interacts with SSD 130 via interface 1220b to mark appropriate data, blocks, pages, or the like as invalid." Ex. 1003, 4:26-28; Ex. 1002, [0019]. The invalid data information takes the form of a logical block address ("LBA"),

[5] A POSITA would have understood the Shu Provisional's reference to the "merge" operation to refer to the "collection" part of "garbage collection," despite the lack of explicitly mentioning "garbage collection." Baker ¶ 198.

which is the claimed "logical identifier." Ex. 1003, 3:17-22; Ex. 1002, [0014]. This LBA maps to the physical "blocks, pages" being invalidated. Ex. 1003, 4:51-56; Ex. 1002, [0019]; Ex. 1017 at 3 ("A[] device will further remap LBA to its internal page and block for SSD"). Thus, a POSITA would have understood that the Shu Patent teaches that the data is "stored at the physical address mapped to the logical identifier," as claimed. Baker ¶ 199; *see also* § XI.A.f, *supra* (explaining mapping of the logical identifier).

As discussed above in Section XI.A.c (element 15[c]), a POSITA would have known the SSD in the Shu Patent would have included a processor, memory controller, and flash memory as shown in figure 1 of Ban. Ex. 1025, Fig. 1; *see also supra* Section VI (explaining the basic components). These components form a circuit that marks blocks as "deleted" (invalid), and the functions "may be carried out in software, firmware, or hardware." Ex. 1025, 3:21, 4:7-10, 5:44-47, 5:64-67, 7:20-30, 8:1-9. Thus, by applying the Patent Owner's interpretations, a POSITA would have found it obvious for the SSD in the Shu Patent to include a "marking module" that includes "circuitry, software, and/or firmware" configured as claimed. Baker ¶ 200; Ex. 1013 at 3 (interpreting the "marking module" as "circuitry, software, and/or firmware").

B. Claim 21: The apparatus of claim 15, wherein the marking module is configured to mark a data packet at the physical address invalid.

The Shu Patent teaches this claim. The Patent Owner interprets "data packet" as "the area of the [memory] that contains the data." Ex. 1013 at 6. The Shu Patent teaches, "Block 240 indicates marking the deleted data as invalid." Ex. 1003, 5:5; Ex. 1002, [0024]. "Such marking may involve marking pages and/or blocks or the like as invalid." Ex. 1003, 5:7-8; Ex. 1002, [0024].

Thus, by applying the Patent Owner's interpretations, a POSITA would have found this element obvious. Baker ¶¶ 202-03.

C. Claim 26

a) Element 26[a]. The apparatus of claim 15, wherein the non-volatile storage medium comprises a flash storage medium, the apparatus further comprising:

The Shu Patent shows an SSD in figure 1 (reproduced above) and discloses, "SSDs are commonly fabricated to include flash memory devices, such as nonvolatile flash memory devices including Not AND ('NAND') type devices." Ex. 1003, 1:13-16; *see also id.*, 2:52-57; Ex. 1002, [0001], [0013]. Thus, a POSITA would have understood Shu's SSD in figure 1 and Shu's storage device in figure 3 to have included a nonvolatile storage medium in the form of nonvolatile NAND flash memory. Baker ¶¶ 205-06.

b) Element 26[b]. a storage recovery module configured to recover the physical storage location at the physical address; and

The Patent Owner accuses generic "garbage collection" of infringing this claim element. Ex. 1013 at 5. The garbage collection technique generally includes (1) "collecting" valid data by copying and merging the valid data into a new block and (2) erasing or removing garbage data left in the old block. Baker ¶ 207. The Patent Owner appears to interpret the second, erasing step of garbage collection as "recover the physical storage location at the physical address" so that data can be written in the block again.

The 2006 Provisional admits that "garbage collection" was "commonly used with NAND flash" in the background statement of the existing problem. Ex. 1015 at 40. The SSD illustrated in figure 1 of the Shu Patent uses NAND flash as explained in Section XI.H.a (element 26a) above. Thus, a POSITA would have found it obvious that the SSD in the Shu Patent would have used the admittedly "common" technique of garbage collection. Baker ¶ 208. The POSITA would have known to do this to free up blocks in the flash memory. *Id.*. Thus, by applying the Patent Owner's interpretations, a POSITA would have found this claim obvious. *Id.*

Moreover, Frank Shu proposed that the Trim command was to be used to "make pre-erased area for next write," again referring to erasing or "recovering" the block so that data can be written. Ex. 1017 § 1. Thus, a POSITA would have

understood that garbage collection takes place after marking data invalid. Baker ¶ 209; Ex. 1003, 4:39-41 ("This frees the SSD device from performing any operations to preserve or maintain such data."); Ex. 1002, [0020]. The Shu Patent discloses the use of a new remove-on-delete/Trim command to "avoid unnecessary operations on the invalid data." Ex. 1003, 1:59; Ex. 1002, [0003]. Specifically, the SSD avoids performing an unnecessary "merge" operation on the invalid data. Ex. 1003, 1:23-25, 3:28-40, 4:29-31; Ex. 1002, [0001], [0014], [0019]. A POSITA would have understood that this "merge" operation refers to the "collection" part of "garbage collection," where data are merged or collected and preserved by copying the data from old blocks into a new block, before erasing garbage left behind in the old blocks. Ex. 1003, 1:20-23; Ex. 1002, [0001]; Baker ¶ 210. Thus, by applying the Patent Owner's interpretation of the claim to refer to "garbage collection," a POSITA would have found this claim obvious. Baker ¶¶ 208-10.

In its name, the "remove-on-delete" command inherently signifies that the physically stored, invalid data is to be "removed" or erased. Ex. 1003, 4:39-41; Ex. 1002, [0020]; Baker ¶ 210. Thus, the data identified as "invalid" or "garbage" will be removed or erased from the block. Baker ¶ 210. This again matches the "recover" process accused by the Patent Owner. Thus, by applying the Patent Owner's interpretation of the claim to refer to "garbage collection," a POSITA would have found this claim obvious. Baker ¶ 210.

As discussed above in Section XI.A.c (element 15[c]), a POSITA would have known the SSD in the Shu Patent would have included a processor, memory controller, and flash memory as shown in figure 1 of Ban. Ex. 1025, Fig. 1; *see also supra* Section VI (explaining the basic components). These components form a circuit that erases data, and the functions "may be carried out in software, firmware, or hardware." Ex. 1025, 1:16-27, 4:7-10. Thus, by applying the Patent Owner's interpretation, a POSITA would have found it obvious that the Shu Patent's SSD would include a "storage recovery module" in the form of "circuitry, software, and/or firmware." Baker ¶ 212; Ex. 1013 at 5 (interpreting the "storage recovery module" as "circuitry, software, and/or firmware").

c) Element 26[c]. a storage module configured to store data associated with another logical identifier on the physical storage location in response to recovering the physical storage location.

The Patent Owner accuses an SSD with an FTL of infringing this element. Ban patented the FTL in 1995, and Ban's FTL had admittedly become one of the "[t]raditional flash storage systems."[6] Ex. 1025; Ex. 1015 at 77 (referring to Ban's patents assigned to M-systems).

The Shu Patent teaches that SSDs typically performed "wear leveling"

[6] *See also*, Ex. 1020 § 2.2 ("The *Flash Translation Layer* (FTL) is a technique …. This technique was originally patented by Ban [5]").

operations, which involves the use of Ban's FTL (or "mappings"). Ex. 1003, 1:25-27, 3:41-42, 4:51-58; Ex. 1002, [0001], [0014], [0022]. Wear-leveling operations "move data from one block or page to another block or page," while using Ban's FTL to keep the same logical address despite the move to a new physical location. Ex. 1003, 1:27-29; Ex. 1002, [0001]; Ex. 1025, 3:64-4:5, 4:40-44. Thus, the garbage collection process described in Section XI.C.b (element 26[b]) above frees up the physical storage location so that other data will be moved in as part of wear-leveling operations. Baker ¶ 215. Any new data moving in to the now-empty block would have mapped to another, different logical address, because different data maps to different logical addresses. *Id.*; *see* Ex. 1003, 1:38-39 ("the data is physically stored on the device, as one or more logical block addresses"), 4:53-55 (referencing the mapping); Ex. 1002, [0001], [0022]. Thus, by applying the Patent Owner's interpretation of the claim to refer to the use of the FTL, a POSITA would have found this claim obvious. Baker ¶ 215.

As discussed above in Section XI.A.c (element 15[c]), a POSITA would have known the SSD in the Shu Patent would have included a processor, memory controller, and flash memory as shown in figure 1 of Ban. Ex. 1025, Fig. 1; *see also supra* Section VI (explaining the basic components). These components form a circuit that "writes data to, and read data from, a flash memory," and the functions "may be carried out in software, firmware, or hardware." Ex. 1025, 3:60-61, 4:7-

10. Thus, by applying the Patent Owner's interpretation, a POSITA would have found it obvious for the SSD in the Shu Patent to include a "storage module" that includes "circuitry, software, and/or firmware." Baker ¶ 216; Ex. 1013 at 5 (interpreting the "storage module" as "circuitry, software, and/or firmware").

XII. Ground 2: Obvious Over the Shu Patent, the Shu Trim Proposal, Ban, Jenett, and POSITA Knowledge

A POSITA would have found independent claim 15 obvious for the reasons discussed in Section XI.A above because Frank Shu's Trim disclosures precede the priority date of the asserted claims. Claims 16-21 recite various language for marking data invalid in response. An additional reference, Jenett, shows that the dependent claims on marking data invalid would have been obvious to a POSITA.

A. Claim 16: The apparatus of claim 15, wherein the marking module is configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium by invalidating an association between the logical identifier and the physical address.

As discussed in Section XI.A.g (element 15[g]) above, the Shu Patent teaches to mark that data "invalid," meaning that the data can be erased. *E.g.*, Ex. 1003, 5:5-17 ("Block 240 indicates marking the deleted data as invalid. Such a mark may take any form sufficient to identify the invalid data to the SSD device. Such marking may involve marking pages and/or blocks or the like as invalid, depending on how the SSD structures its data …. the corresponding data is now marked as invalid on the SSD in such a manner that the SSD can recognize the corresponding data as

invalid."); Ex. 1002, [0024].

Jenett discloses a common technique used by SSDs to indicate invalid data: to "delete the association between the physical location at which the identified deleted file was stored and the virtual[7] address formerly connected with the particular physical location." Ex. 1033, 6:13-16; *see also id.* 6:20-33 (providing additional detail), 4:56-57, Fig. 3 block 404. A POSITA would have understood that a deleted mapping is invalid. *Id.*, 4:40-42, 4:57-61, 5:16-17, 6:11-23 (a deleted relationship indicates something "other than valid"); Baker ¶ 220. This deletion occurs in a "block allocation map" ("BAM"), which "is a physical to virtual map which associates particular physical sectors of the flash medium with a related virtual address, provided that a relationship exists." Ex. 1033, 6:16-19, Fig. 4 (showing "BAM"). The Examiner cited Jenett for teaching the element, and the applicant did not dispute it. Ex. 1021 at 967, 1003.

A POSITA would have known that Jenett's SSD with a block allocation map (or physical-to-virtual map) in flash memory exemplifies an SSD system with the "mapping" of logical addresses to "pages, blocks" envisioned in the Shu Patent. Baker, ¶ 221; Ex. 1003, 4:51-61; Ex. 1002, [0022]. Jenett teaches to delete the association between the physical and logical address when "the deletion of the file

[7] A "virtual" address is a form of a logical address. Baker ¶ 162.

is evidenced" by a discrepancy in a file mapping; Shu teaches to similarly note the same invalidation in response to a remove-on-delete (Trim) command.

Thus, a POSITA would have found it obvious for an SSD to delete an association between a logical address and a physical address to invalidate that association, as disclosed in Jenett, in response to Frank Shu's remove-on-delete/Trim command. Baker ¶ 221. The Shu Patent expressly taught that marking data as invalid "may take any form sufficient to identify the invalid data to the SSD device," and Jenett merely discloses a well-known way to do so. Ex. 1003, 5:5-7; Ex. 1002, [0024]. Jenett's well-known technique of deleting the association between the logical address and the physical address would have worked predictably in Shu's system. Baker ¶ 221. Shu's system could have predictably incorporated Jenett's technique because both systems operated similarly. *Id*. Both Shu's system and Jenett's system involved SSDs that have logical-to-physical maps and need to identify invalid data addressable by logical addresses and physical addresses.

Thus, it would have been obvious to a POSITA for the SSD in the Shu Patent to have a marking module that "is configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium by invalidating an association between the logical identifier and the physical address," as claimed. Baker ¶ 222.

B. Claim 17: The apparatus of claim 15, wherein the marking module is configured to record that data stored at a physical

address on the non-volatile storage medium can be erased from the non-volatile storage medium by deleting a mapping between the logical identifier and the physical address.

For the reasons explained in Section XI.A.g (element 15[g]) above, it was obvious for a marking module to record that data stored at a physical address on the non-volatile storage medium can be erased. As explained in Section XII.A (claim 16) above, Jenett discloses a common technique used by SSDs to indicate invalid data: to "delete the association between the physical location at which the identified deleted file was stored and the virtual address formerly connected with the particular physical location." Ex. 1033, 6:13-16.

A POSITA would have found it obvious for the SSD in the Shu Patent to use this technique for the same reasons discussed in XII.A above. Baker ¶ 224-26. Thus, a POSITA would have found it obvious for the marking module to be "configured to record that data stored at a physical address on the non-volatile storage medium can be erased from the non-volatile storage medium by deleting a mapping between the logical identifier and the physical address." Baker ¶ 226.

C. Claim 18: The apparatus of claim 15, further comprising an index comprising mappings between logical identifiers and physical addresses on the non-volatile storage medium, wherein the marking module is configured to remove a mapping between the logical identifier and the physical addresses of the data from the index.

As explained in Section XI.A.f (element 15[f]) above, the Shu Patent teaches that the logical identifier is mapped to a physical address. A POSITA would have

understood this as the claimed "index comprising mappings between logical identifiers and physical addresses on the non-volatile storage medium." Baker ¶ 228.

As explained in Section XII.A (claim 16) above, Jenett teaches that the BAM "is a physical to virtual map which associates particular physical sectors of the flash medium with a related virtual address," stored on the nonvolatile flash memory card. Ex. 1033, 6:16-18, Fig. 4. As explained in Section XII.A (claim 16) above, Jenett discloses to "delete the association between the physical location at which the identified deleted file was stored and the virtual address formerly connected with the particular physical location." Ex. 1033, 6:13-16. A POSITA would have found it obvious for the SSD in the Shu Patent to use Jenett's deletion technique on the flash memory for the same reasons discussed in XII.A (claim 16) above, such that "the marking module is configured to remove a mapping between the logical identifier and the physical addresses of the data from the index." Baker ¶¶ 228-29.

D. Claim 19: The apparatus of claim 18, wherein the marking module is configured to delete a reference to the physical address from an index entry of the logical identifier.

As explained in Section XI.A.f (element 15[f]) above, the Shu Patent teaches that the logical identifier is mapped to a physical address. As explained in Section XII.A (claim 16) above, Jenett discloses to "delete the association between the physical location at which the identified deleted file was stored and the virtual

address formerly connected with the particular physical location." Ex. 1033, 6:13-16. A POSITA would have found it obvious for the SSD in the Shu Patent to use Jenett's deletion technique in a BAM on the flash memory for the same reasons discussed in XII.A (claim 16) above, such that "the marking module is configured to remove a mapping between the logical identifier and the physical addresses of the data from the index." Baker ¶ 231.

E. Claim 20: The apparatus of claim 18, wherein removal of the mapping indicates that data stored at the physical address can be erased from the non-volatile storage medium.

For the reasons explained in Section XII.D (claim 19) above, it would have been obvious for the SSD in the Shu Patent to "delete the association between the physical location … and the virtual address," as taught by Jenett. Further, Section XII.D (claim 19) refers to the reasoning in Section XII.A (claim 16), which explains how a POSITA would have used Jenett's technique for marking data invalid because the Shu patent discloses, "Block 240 indicates marking the deleted data as invalid. Such a mark may take any form sufficient to identify the invalid data to the SSD device." Ex. 1003, 5:5-7; Ex. 1002, [0024]. Thus, the resulting removal indicates that data are "invalid." Baker ¶ 233.

The Patent Owner appears to accuse marking data as "invalid" to mean marking data to indicate that the data can be erased. Ex. 1013 at 3, 5 (accusing claims 16 and 21). Jenett discloses that an "invalid" marking means that blocks can

be erased during garbage collection. Ex. 1033, 4:57-64 ("This making invalid … means that … the blocks containing deleted files will not be moved. Instead, they are left behind to face erasure."). Thus, a POSITA would have found this element obvious for the reasons explained in Sections XII.D (claim 19) and XII.A (claim 16) above. Baker ¶¶ 223-24.

XIII. Secondary Considerations

Simultaneous invention by others shows that the claims fall within the level of the ordinary skill in the art. "Independently made, simultaneous inventions, made 'within a comparatively short space of time,' are persuasive evidence that the claimed apparatus 'was the product only of ordinary mechanical or engineering skill.'" *Geo M. Martin Co. v. All. Mach. Sys. Int'l LLC*, 618 F.3d 1294, 1305 (Fed. Cir. 2010). The Board has held that exhibits of a standard-setting group on a related standard "are evidence of simultaneous invention by others," support finding challenged claims obvious, and "are persuasive evidence that the claimed apparatus 'was the product only of ordinary mechanical or engineering skill.'" *ZTE (USA) Inc. v. Evolved Wireless LLC*, No. IPR2016-00757, Paper 42, at 29 (P.T.A.B. Nov. 30, 2017).

Here, Exhibits 1017-1018 show that standard-setting group T13 began work on the Trim command proposal at least by April 21, 2007, months before September 2007. Baker ¶ 236. The Patent Owner accuses this Trim command of infringing the

claims. Ex. 1013, *passim*. Like the *ZTE* case, here a standard-setting group worked on the same technology around the same time. Exs. 1017-1018. Also, other prior art taught similar commands. Ex. 1029, 17:52-56 (an erase command "specifies the (logical) sectors to be erased"); Ex. 1028, 9:2-3 ("logical block address … designated in the erase command"). Furthermore, many claim elements were already well known in the art. *See, e.g.*, Ex. 1027 §§ 2.2 (Ban patented the FTL in 1995, and the FTL became part of an industry standard), 2.3 (explaining the garbage collection process). Thus, Exhibits 1002-1003, 1017-1018, 1029, and 1028 all serve as evidence of simultaneous invention by others, and the Board should find the challenged claims obvious for being only the product of ordinary mechanical or engineering skill.

XIV. Mandatory Notices

A. Real Parties-in-Interest

The named Petitioners are the only entities who are funding and controlling this Petition and are therefore all named as real parties-in-interest. No other entity is funding, controlling, or otherwise has an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

Out of an abundance of caution, Petitioners also identify Dell Technologies Inc., Dell Inc., Denali Intermediate Inc. (which is a corporate parent entity of Dell Inc.), and HP Inc. as real parties-in-interest. The Patent Owner sued Dell

Technologies Inc., Dell Inc., and HP Inc., alleging infringement of the challenged patent but those cases were dismissed before the filing of this Petition.

Petitioners also identify that there are many entities such as suppliers, resellers, part providers, contractors, etc., who may have financial liabilities with respect to the hundreds of accused products in the related litigations. Petitioners do not believe that any of these entities, however, are real parties-in-interest. None of these other entities participated in the preparation or funding of this Petition or otherwise had an opportunity to control or direct this Petition. To Petitioners' best knowledge, no entity, other than Petitioners and the entities named in this Section XIV, has been served with a complaint alleging infringement of the patent at issue herein.

B. Related Proceedings

The Patent Owner asserted the '406 Patent against Petitioners in the Western District of Texas, Case No. 6:20-cv-500. In the same Court, the Patent Owner also asserted the '658 Patent against Dell Technologies Inc. and Dell Inc. in Case No. 6:20-cv-499 and against HP Inc. in Case No. 6:20-cv-501. The Patent Owner filed each lawsuit on June 5, 2020.

Three IPR proceedings relate to the same patent family: IPR2021-00343 ('406 Patent), IPR2021-00344 (Pat. 8,762,658), and IPR2021-00345 (Pat. 9,632,727). Petitioners are also filing contemporaneously two additional IPR proceedings that

challenge the priority date of the same patent family: IPR2021-00941 (Pat. 8,762,658), and IPR2021-00942 (Pat. 9,632,727).

C. Lead and Backup Counsel

The following lead and backup counsel represent Petitioners:

Lead Counsel for Petitioner	Backup Counsel for Petitioner
Katherine A. Vidal Winston & Strawn LLP 275 Middlefield Rd., Suite 205 Menlo Park, CA 94025 kvidal@winston.com T: 650.858.6500, F: 650.858.6550 USPTO Reg. No. 46,333	Michael Rueckheim Winston & Strawn LLP 275 Middlefield Rd., Suite 205 Menlo Park, CA 94025 mrueckheim@winston.com T: 650.858.6500, F: 650.858.6550 (to seek *pro hac vice* admission) Qi (Peter) Tong Winston & Strawn LLP 2121 N Pearl St. Dallas, TX 75201 ptong@winston.com T: 214.453.6473, F: 214.453.6400 USPTO Reg. No. 74,292

D. Electronic Service

Petitioners consent to electronic service at:

Winston-IPR-Unification@winston.com

XV. Fees

Petitioners have paid the required fee electronically through P.T.A.B. E2E.

XVI. Conclusion

Petitioners respectfully request that the Board institute IPR and enter a final

written decision finding the challenged claims unpatentable.

Dated: June 4, 2021

Respectfully submitted,

/s/ *Katherine A. Vidal*
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CERTIFICATE OF COMPLIANCE

This Petition complies with the word-count limits set forth in 37 C.F.R. § 42.24(a)(1)(i), because this Petition contains 12,698 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1) and determined using the word count provided by Microsoft Word, which counsel used to prepare this Petition.

Dated: June 4, 2021

Respectfully submitted,
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CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105(a), this is to certify that on June 4, 2021, I caused to be served a true and correct copy of the foregoing "**PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 15-21 AND 26 OF U.S. PATENT NO. 8,533,406**" and Exhibits 1001-1040 by FedEx on the Patent Owner at the correspondence address of record for U.S. Patent No. 8,533,406:

Western Digital, c/o Longitude Licensing Stoel Rives LLP
201 South Main Street, Suite 1100
One Utah Center
Salt Lake City UT 84111

A courtesy copy of this Petition and supporting material was also served on litigation counsel for Patent Owner via email:

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