UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

LED WAFER SOLUTIONS LLC,
Patent Owner

Patent No. 9,786,822

PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,786,822

TABLE OF CONTENTS

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 9,786,822
Ex. 1002	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003	Curriculum Vitae of R. Jacob Baker, Ph.D., P.E.
Ex. 1004	Prosecution History of U.S. Patent No. 9,786,822
Ex. 1005	U.S. Patent No. 9,634,191 to Keller et al.
Ex. 1006	U.S. Patent No. 7,419,839 to Camras et al.
Ex. 1007	U.S. Patent No. 8,835,937 to Wirth et al.
Ex. 1008	U.S. Patent No. 9,837,583
Ex. 1009	U.S. Patent No. 6,020,602 to Sugawara et al.
Ex. 1010	Prosecution History of U.S. Patent 8,941,137
Ex. 1011	RESERVED
Ex. 1012	U.S. Patent No. 6,562,709 to Lin
Ex. 1013	U.S. Provisional Patent Application No. 61/449,685 filed March 6, 2011
Ex. 1014	U.S. Provisional Patent Application No. 61/449,686 filed March 6, 2011
Ex. 1015	RESERVED
Ex. 1016	RESERVED
Ex. 1017	RESERVED
Ex. 10181	RESERVED
Ex. 1019	RESERVED
Ex. 1020	RESERVED

Ex. 1021	Complaint (Dkt. #1) in *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd. et al.,* 6-21-cv-00292 (W.D. Tex. Mar. 25, 2021)
Ex. 1022	Judge Albright's (W.D. Tex.) "Order Governing Proceedings - Patent Cases 062421.pdf" available at https://www.txwd.uscourts.gov/judges-information/standing-orders/
Ex. 1023	Schubert, Light Emitting Diodes, Second Edition, 2006 ("Schubert")

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1, 2, and 5-10 ("the challenged claims") of U.S. Patent No. 9,786,822 ("the '822 patent") (Ex. 1001) assigned to LED Wafer Solutions LLC ("Patent Owner" or "PO"). For the reasons below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '822 patent is asserted in the following civil action *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd. et al.*, 6-21-cv-00292 (W.D. Tex). The '822 patent is also related to U.S. Patent No. 8,941,137 ("the '137 patent"). Petitioner previously filed a petition challenging the '137 patent. (IPR2021-01506)

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224). Backup counsel: (1) Joseph E. Palys (Reg. No. 46,508), (2) Chetan R. Bansal (Limited Recognition No. L0667), (3) Paul M. Anderson (Reg. No. 39,896), and (4) Jason Heidemann (Reg. No. 77,880).

Service information is Paul Hastings LLP, 2050 M Street NW, Washington, DC 20036, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-LEDWafer-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '822 patent is available for review, and Petitioner is not barred/estopped from requesting review on the grounds herein.

V. PRECISE RELIEF REQUESTED

A. Claims for Which Review Is Requested

Petitioner requests review and cancellation of claims 1, 2, and 5-10 as unpatentable based on the following grounds.

B. Statutory Grounds of Challenge

Ground 1: Claims 1, 2, and 5-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) based on U.S. Patent No. 8,835,937 to Wirth et al. ("Wirth") (Ex. 1007);

Ground 2: Claim 10 is unpatentable under pre-AIA 35 U.S.C. § 103(a) based on Wirth in combination with U.S. Patent No. 6,562,709 to Lin ("Lin") (Ex. 1012);

Ground 3: Claims 1, 2, and 5-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) based on Wirth in combination with the Applicant Admitted Prior Art ("AAPA");

Ground 4: Claim 10 is unpatentable under pre-AIA 35 U.S.C. § 103(a) based on Wirth in view of the AAPA and Lin;

Ground 5: Claims 1, 2, and 5-9 are unpatentable under pre-AIA 35 U.S.C. § 103(a) based on Wirth in combination with U.S. Patent No. 7,419,839 to Camras *et al.* ("Camras") (Ex. 1006); and

Ground 6: Claim 10 is unpatentable under pre-AIA 35 U.S.C. § 103(a) based on Wirth in view of Camras and Lin.

The '822 claims priority to two provisional applications, U.S. Provisional Patent Application Nos. 61/449,685 (Ex. 1013) and 61/449,686 (Ex. 1014), each dating back to March 6, 2011. Wirth is an issued patent with a §371(c)(1), (2), (4) date of December 2, 2008. Thus, Wirth qualifies as prior art at least under pre-AIA 35 U.S.C. § 102(e).

AAPA qualifies as prior art at least under pre-AIA 35 U.S.C. §§ 102(a) and 311(b) with respect to the '822 patent. *See, e.g., One World Techs., Inc. v. Chamberlain Group, Inc.*, IPR2017-00126, slip op. at 9-10 (May 4, 2017) (Paper 8); *see also Apple Inc., v. Qualcomm Inc.,* IPR2018-01316, slip op. at 22 (January 18,

2019) (Paper 7). Camras issued September 2, 2008, and Lin published on May 13, 2003. Therefore, both Camras and Lin are prior art under pre-AIA 35 U.S.C. § 102(b).

Wirth, Camras, and Lin were not considered during prosecution of the '822 patent (Ex. 1001, Cover ("References Cited"); *see also generally* Ex. 1004).

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of the claimed priority date of the '822 patent ("POSITA") would have had a bachelor's degree in electrical engineering, material science, or the equivalent, and two or more years of experience with light emitting diodes (LEDs). (Ex. 1002 ¶¶20-21.)[1] More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE '822 PATENT AND THE PRIOR ART

A. The '822 patent

The '822 patent relates to "a light emitting diode (LED) device." (Ex. 1001, 1:16-19; *see also id.*, Abstract, 2:6-30; Ex. 1002 ¶¶30-36.) The '822 patent admits

[1] Petitioner submits the declaration of Dr. R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '822 patent. (Ex. 1002 ¶¶5-15; Ex. 1003.)

that light emitting diode (LED) devices were well-known and depicts a prior art LED device in figure 3 below. (Ex. 1001, 2:54-59, 4:16-18, FIGs. 1-3.)

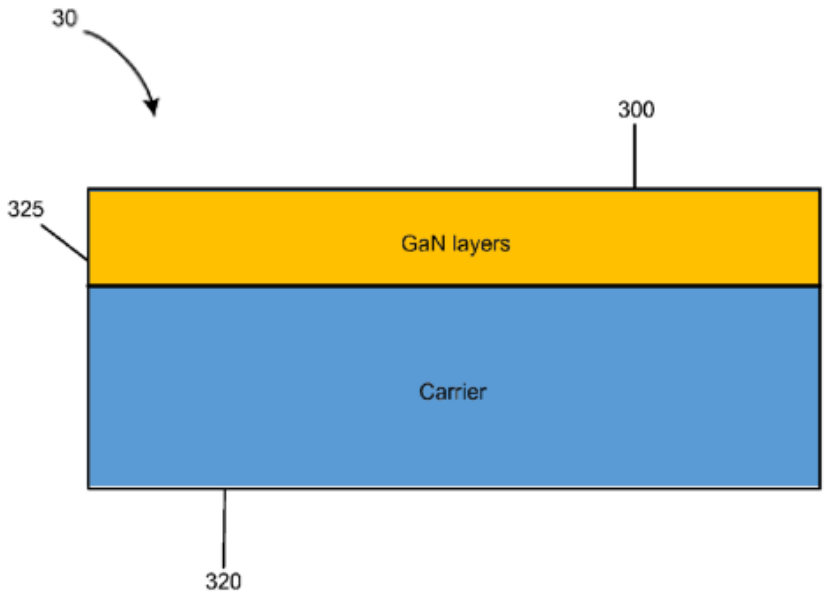


Fig. 3
(Prior Art)

(Ex. 1001, FIG. 3 (annotated); Ex. 1002 ¶30.)

The prior art light emitting device 30 of figure 3 includes a semiconductor LED layer 300 (highlighted in orange), a metallic interface 325, and a carrier layer 320 (highlighted in blue). (Ex. 1001, 3:64-4:2, 4:16-18.) The semiconductor LED layer 300 includes a GaN layer. (*Id.*, FIG. 3.) GaN refers to a gallium nitride "which is a type of bandgap semiconductor suited for use in high power LEDs." (*Id.*, 3:28-30.) The '822 patent states that GaN LEDs "comprise a P-I-N junction device having

an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer." (*Id.*, 3:32-34; Ex. 1002 ¶31.) In other words, the '822 patent admits that prior art GaN LEDs have an intrinsic region disposed between an n-type doped layer and a p-type doped layer. (Ex. 1002 ¶31.)

The disclosed embodiments of the '822 patent build on the prior art device of figure 3. For instance, the disclosed embodiments describe an LED device comprised of additional layers that "act to promote mechanical, electrical, thermal, or optical characteristics of the device" (Ex. 1001, 2:2-4, 19-23; *see also id.,* Abstract), as seen in figures 6 and 14, reproduced below. (*Id.*, 4:55-59, 7:16-23, FIGS. 6, 14; *see also id.*, 2:64-66, 3:13-14; Ex. 1002 ¶32.) Like the prior-art LED device in figure 3 above, each of the devices 60 and 1401 in figures 6 and 14, respectively, includes the GaN LED layer (highlighted in orange) separated from the carrier layer (highlighted in blue) by a metallic interface (e.g., element 625 in figure 6). (*Id.*, 4:55-59; *compare id.*, FIGS. 6, 14 *with* FIG.3.)

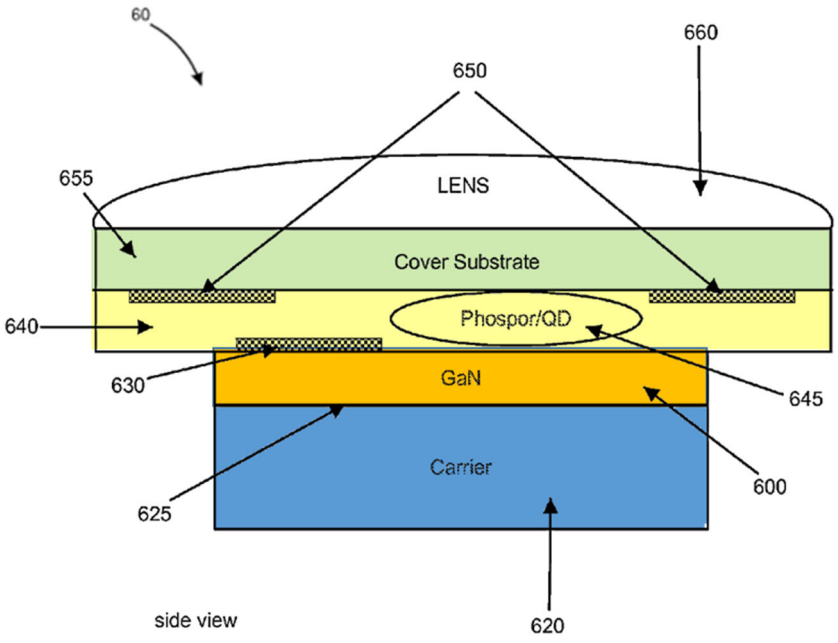


Fig. 6

(Ex. 1001, FIG. 6 (annotated); Ex. 1002 ¶33.)

The LED device 60, as shown by figure 6 above, further includes an optically transparent or transmissive adhesive layer 640 (*id.*, 4:60-65), a cover substrate 655 (*id.*, 5:17-24), and an optical lens 660 (*id.*, 5:25-30). The transparent or optically permissive adhesive layer 640 may contain "a region containing phosphor and/or quantum dot material (QD) 645." (*Id.*, 5:9-11.) The optical lens 660 "act[s] to spread, diffuse, collimate, or otherwise redirect and form the output of the LED." (*Id.*, 5:26-30.) Like device 60 in figure 6, the device 1401 in figure 14 below includes similar layers. (*Id.*, 7:16-23; Ex. 1002 ¶¶34-35.)

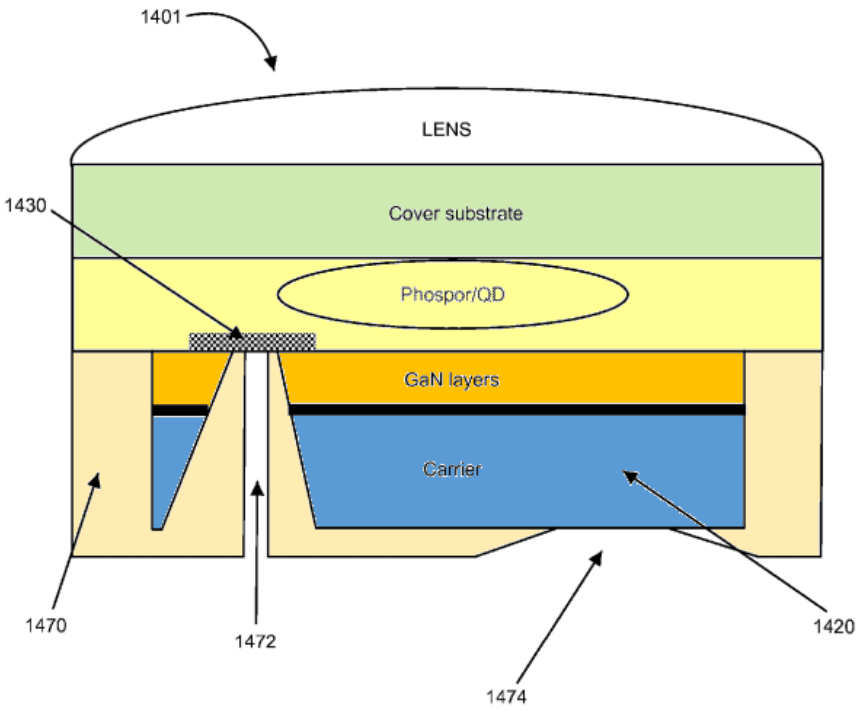


Fig. 14

(Ex. 1001, FIG. 14 (annotated); Ex. 1002 ¶35.)

Device 1401 further includes a passivation layer 1470. (Ex. 1001, 7:19-21; *see also id.*, 6:22-26 (the device in figure 11 "including a passivation layer 1170 that has been applied to surround certain portions of the device around LED semiconducting layer 1100, metallic interface 1125, and carrier layer 1120."), FIG. 11.) Device 1401 also includes contact holes 1472, 1474, which have been drilled or etched into passivation layer material 1470, along with the carrier and GaN layers. (*Id.*, 7:19-21; *see also id.*, 6:14-21, FIG. 10.) The '822 patent states that "this

exposes a first contact 1472 at metal pad 1430 and a second contact 1474 at carrier 1420." (*Id.*, 7:21-22; Ex. 1002 ¶¶35-36.)

As explained below and in the accompanying declaration of Dr. Baker, all the limitations in the challenged claims were known in the prior art. (*See infra* Section IX; Ex. 1002 ¶37; *see also* Ex. 1002 ¶¶16-19, 22-29 (technology background, citing Exhibit 1023), 39-56 (discussing the prior art at issue in this petition), 57-122 (discussing prior art disclosures in view of each claim's limitations).)

B. Prosecution History of the '822 patent

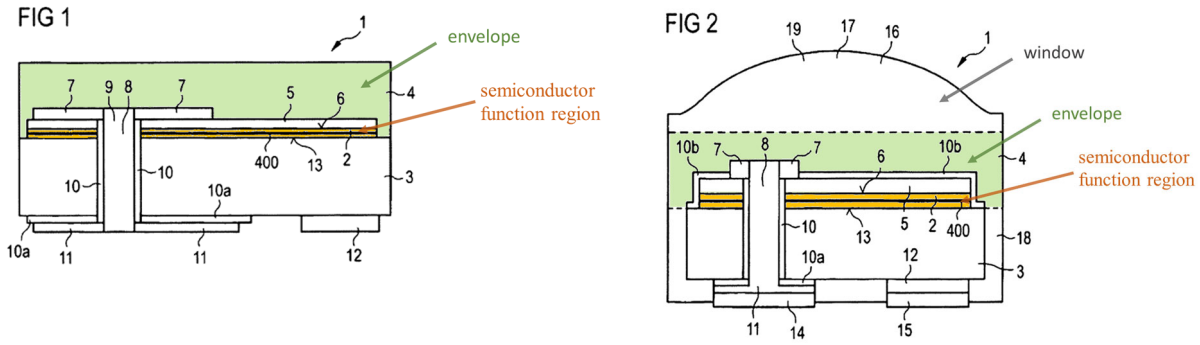
During prosecution, no prior art references were applied to the claims in any office action (Ex. 1004, 11-18 (Notice of Allowance), 69-73 (Non-Final Office Action), 119-123 (Restriction Requirement).) The claims, however, were amended in response to a written description rejection. (Ex. 1004, 61-64 (Applicant's Remarks), 69-73 (Non-Final Office Action).)

C. Wirth (Ex. 1007)

Wirth discloses a light-emitting device and methods for manufacturing such devices. (Ex. 1007, Abstract; *see also id.,* 1:20-24; Ex. 1002 ¶¶39-48.) In particular, Wirth discloses a "device comprising a plurality of optoelectronic components that can be produced in a simplified and low-cost manner." (Ex. 1007, 1:59-61; *see also*

id., 4:47-62 ("The optoelectronic component …. can for example be configured in the manner of an LED chip") (excerpted), 18:17-38 (describing that the optoelectronic component in figure 1 comprises a GaN LED), FIGS. 1, 2.)

With reference to figures 1 and 2, Wirth discloses an LED structure that includes a "semiconductor function region 2" that is based on GaN, and includes a plurality of semiconductor layers. (*Id.*, 18:15-38, FIG. 1.) Wirth discloses phosphor, either in the form of a phosphor layer (*id*., 21:44-49) or included in an envelope 4 (*id*., 21:31-43), over the semiconductor function region to alter the wavelength of the light emitted. Wirth further discloses an encapsulating element (such as the envelope 4 and a window 17) over the semiconductor to protect the semiconductor layers from harmful external influences. (*Id.*, 5:43-6:32, 20:36-39, 21:44-49, FIG. 1-2.)



(Ex. 1007, FIGS. 1, 2 (annotated); Ex. 1002 ¶42.)

VIII. CLAIM CONSTRUCTION

Under the applicable standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), claim terms are typically given their ordinary and customary meanings as understood by a POSITA at the time of the invention based on the claim language, specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the claims when necessary to resolve the controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citation omitted). Petitioner

believes no express constructions of any claim terms are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002 ¶38.)[2]

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Wirth Renders Obvious Claims 1, 2, and 5-9

1. Claim 1

a) A light emitting device, comprising:

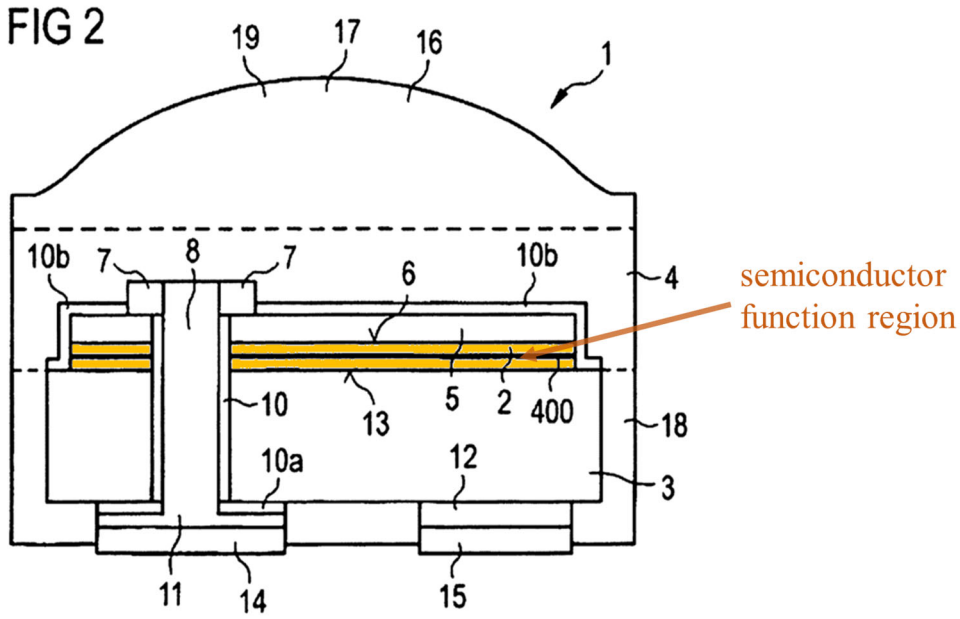
Wirth discloses the preamble of claim 1. (Ex. 1002 ¶58.) Wirth discloses an optoelectronic component 1 ("light emitting device") that includes a semiconductor function region 2 as illustrated in figure 2 below. (Ex. 1007, 18:17-21)[3] Wirth

---

[2] Petitioner reserves all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §§ 101 or 112, in district court as relevant to those proceedings. *See, e.g.*, *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11-13 (November 10, 2020). A comparison of the claims to any accused products in litigation may raise controversies that are not presented here given the similarities between the references and the patent.

[3] Wirth's description corresponding to components in figure 1 equally applies to the similar components in figure 2. (Ex. 1002 ¶58, n.4.) This is so because Wirth explains that "[t]he component shown here [in FIG. 2] is substantially the same as

explains that the semiconductor function region 2 includes an active zone 400 that emits light. (*Id.*, 18:25-33.)



(Ex. 1007, FIG. 2 (annotated); Ex. 1002 ¶58.)

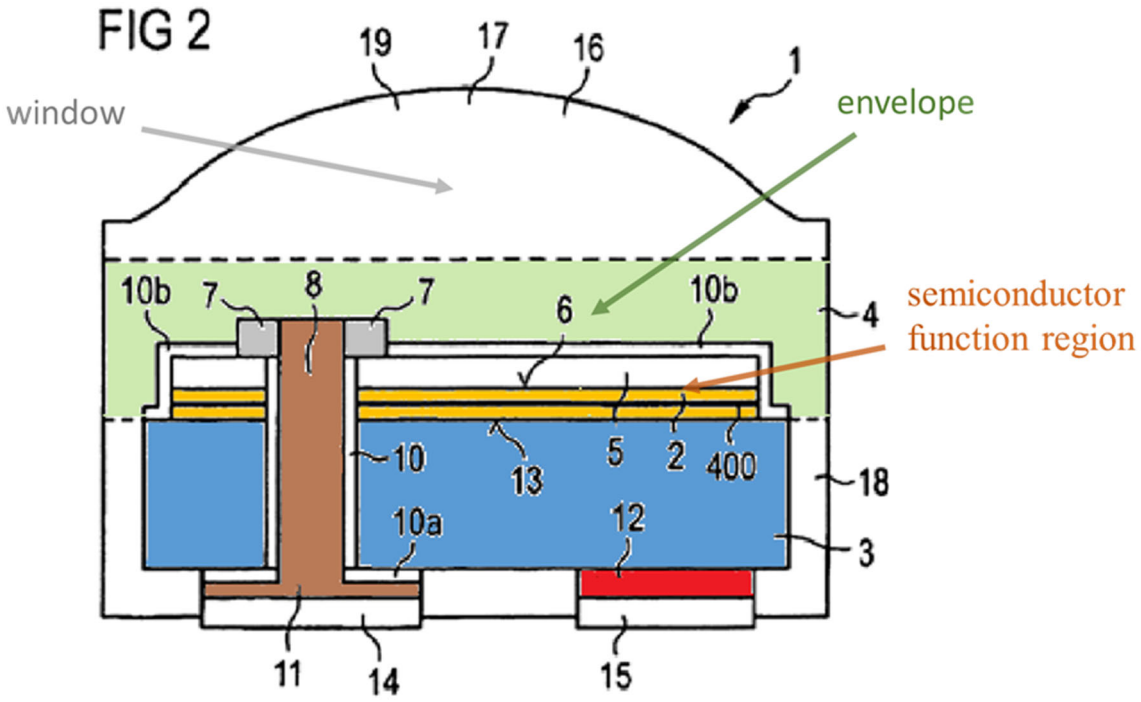
Wirth therefore discloses a "light emitting device." (Ex. 1002 ¶58; *see also infra* Sections IX.A.1.b-h.)

---

that depicted in FIG. 1" (Ex. 1007, 21:52-53) and figure 2 contains several common elements denoted by the same reference numbers to those in figure 1 (*compare id.*, FIG. 1 *with* FIG. 2). Nor does Wirth repeat the description of the functions of the common components shown in its figures. (Ex. 1002 ¶58, n.4; Ex. 1007, 21:50-24:53.)

b) an optically transparent cover substrate;

Wirth discloses this limitation. (Ex. 1002 ¶¶59-62.) For example, the optoelectronic component 1, as illustrated in figure 2 below, includes a window 17 ("optically transparent cover substrate"). (Ex. 1007, 22:29-35; *see also supra* Section IX.A.1.a.)



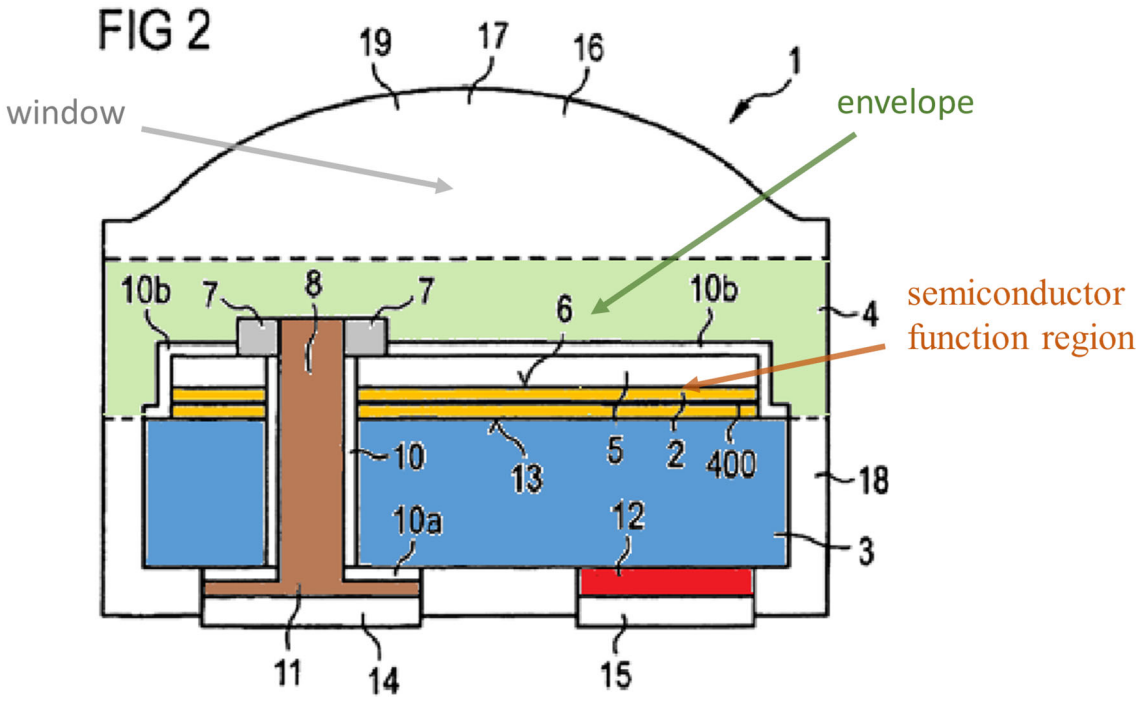
(Ex. 1007, FIG. 2 (annotated); Ex. 1002 ¶59.)

Window 17 is "preferably configured as radiation-transparent ["optically transparent"] with respect to this radiation in order to advantageously increase the efficiency of the component." (Ex. 1007, 22:58-61; Ex. 1002 ¶60.) Wirth also discloses that the window 17 can be a portion of a glass plate formed separately from

the envelope 4. (*Id.*, 22:62-65.) In some embodiments, the window 17 includes an optical element 19 that is "configured as convex in the manner of a lens and advantageously increases the efficiency of the optoelectronic component," whereas in other embodiments the optical element is a Fresnel lens. (*Id*., 23:5-24; Ex. 1002 ¶61.) Window 17, as illustrated in figure 2 above, provides cover to envelope 4 of the optoelectronic component 1. (*Id.*, 22:31-35 ("This encapsulation includes a window 17, which, viewed from the first main face of the semiconductor function region, is disposed after envelope 4, which at least partially envelops or is embedded in the semiconductor function region."); Ex. 1002 ¶62.) Accordingly, a POSITA would have understood that window 17 is "an optically transparent cover substrate," as claimed. (Ex. 1002 ¶62.)

c) an optically transparent layer attached to a bottom surface of said optically transparent cover substrate, said optically transparent layer including an optically definable material;

Wirth discloses this limitation. (Ex. 1002 ¶¶63-65.) For example, Wirth's optoelectronic component 1 includes a "radiation-transparent" envelope 4 ("an optically transparent layer"), which, as shown in annotated figure 2 below, is attached to the bottom surface of the window 17 ("optically transparent cover substrate"). (Ex. 1007, 18:55-58, FIG. 2; Ex. 1002 ¶63.)



(Ex. 1007, FIG. 2 (annotated); Ex. 1002 ¶63.)

Wirth discloses that the envelope 4 is attached to window 17 "by adhesive bonding." (*Id.*, 23:47-50; *see also id.*, 23:1-4 (explaining that "[i]f the window and the envelope are configured in two pieces, however, then the broken line denotes the boundary area between those elements."), 22:67-23:4; Ex. 1002 ¶64.)

Wirth further discloses that the envelope 4 "includ[es] an optically definable material," as claimed. (Ex. 1002 ¶65.) For example, Wirth discloses "phosphor, particularly for generating mixed color light, is preferably disposed in the envelope 4." (Ex. 1007, 23:51-53; *see also id.*, 23:53-59 ("In particular, the envelope material can serve as a carrier matrix for phosphor particles, which can subsequently be

applied to the semiconductor function region along with the material of the envelope.").)

Accordingly, Wirth discloses claim element 1.c. (Ex. 1002 ¶65.)

d) claim element 1(d)

(1) a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region,[]

Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶66-75.) For example, Wirth discloses that the "semiconductor function region 2 . . . comprises a plurality of semiconductor layers and/or is based for example on GaN or GaP." (Ex. 1007, 18:25-38.) Wirth explains that the semiconductor function region 2 includes an active zone 400 that emits light. (*Id.*; *see also id.*, 4:53-54 ("The semiconductor function region can for example be configured in the manner of an LED chip").) The "semiconductor function region 2" having the active zone 400 is further described with reference to figure 4, which describes the process to prepare "a component similar to that depicted in Figure 2." (*Id.*, 27:22-26.) In particular, the semiconductor function region includes a "semiconductor layer sequence 200," which includes "active zone 400." (*Id.*, 27:27-32.) The active zone 400 is between a p-conducting ("positively-doped") and n-conducting ("negatively-doped") layer in

the "semiconductor layer sequence 200". (*Id.*, 40:36-43.) Therefore, Wirth discloses that semiconductor function region includes an active zone 400 between a p-doped layer and an n-doped layer. (Ex. 1002 ¶¶67-70.)

Wirth also suggests (if not discloses to a POSITA) that the active zone 400 includes an "intrinsic region" for several reasons. (Ex. 1002 ¶¶70-71.) First, the lack of any indication of doping (n-type or p-type) of active zone 400 suggests that active zone 400 is "intrinsic" (i.e., not doped). (*Id.* ¶70.) In fact, it was well-understood in the LED art that "[f]requently the active layer is left undoped." (*Id.*; Ex. 1023, 117.)[4] Second, as confirmed by the Applicant during the prosecution of U.S. Patent No. 8,941,137, the parent patent to the '822 patent, an intrinsic region, when present, is "typically [provided] between p-n layers." (Ex. 1010, 227.) Here, Wirth's active zone 400, which is between p and n layers, is consistent with Applicant's assertions regarding the placement of an intrinsic layer. Third, Wirth discloses that in some embodiments, the LED device is a gallium nitride (GaN) LED. (Ex. 1007, 18:25-38.) The '822 patent admits that prior art GaN LEDs, like that described in Wirth, "*comprise* a P-I-N junction device *having an intrinsic (I) layer*

[4] Schubert is cited to demonstrate the knowledge of a POSITA at the time of the alleged invention of the '822 patent.

disposed between a N-type doped layer and a P-type doped layer." (Ex. 1001, 3:30-34 (emphasis added); *see also id.,* 4:21-24; Ex. 1002 ¶71.)

Wirth further discloses that a current spreading layer 5 is also disposed on semiconductor function region 2. (Ex. 1007, 18:59-62.) A POSITA would have known that current spreading layers are used to improve the light extraction efficiency in LEDs by distributing the current under the top electrode across the top surface. (Ex. 1002 ¶72; Ex. 1023, 127.)[5] Electrodes can be made of metal and opaque, whereas current spreading layers are transparent such that they were often referred to as "window layers." (Ex. 1023, ("The window layer is the top semiconductor layer located between the upper cladding layer and the top ohmic contact.") A POSITA would have understood that the claimed "semiconductor LED" would include current spreading layer 5, which can be formed of semiconductor material, in addition to semiconductor function region 2. (Ex. 1007, 25:33-37; Ex. 1002 ¶¶73-74.) The current spreading layer 5 is spread along the top surface of semiconductor function region 2, taking its shape, and the layer's function is "to facilitate uniform current inflow from the first main face 6 of the

[5] Schubert is cited to demonstrate the knowledge of a POSITA at the time of the alleged invention of the '822 patent.

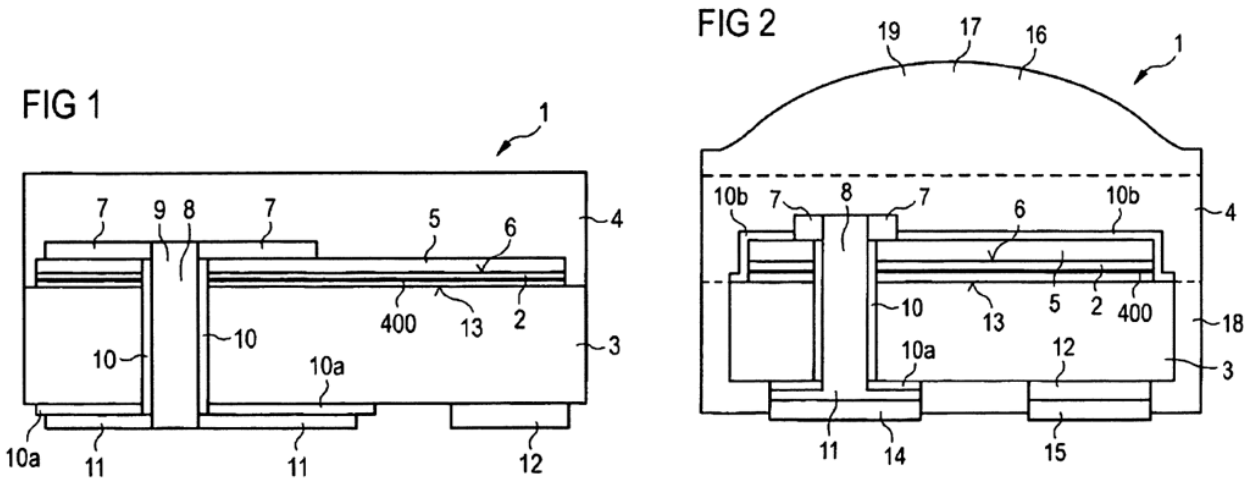
semiconductor function region . . . ." (Ex. 1007, 18:65-19:3, FIG. 2.)

Given that the claim language is open-ended ("a semiconductor LED including . . . ."), a POSITA would have understood that the claimed "semiconductor LED" is not limited to just the doped and intrinsic layers. (Ex. 1002 ¶74.) Indeed, such an understanding is supported by U.S. Patent No. 9,837,583 ("the '583 patent") (Ex. 1008), which is related to the '822 patent in that it claims priority to the same two provisional patent applications as the '822 patent. (*Compare* Ex. 1001, Cover *with* Ex. 1008, Cover.) Claim 1 of the '583 patent recites "a semiconductor LED including *a LED carrier layer*, a positively-doped region, an intrinsic region, and a negatively doped region" (Ex. 1008, 8:27-29), which supports the understanding that a "semiconductor LED including . . . ." as recited in the claims is not limited to just the doped and intrinsic layers. (Ex. 1002 ¶74.)

For the above reasons, Wirth discloses or suggests "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region." (*Id.* ¶75.)

(2) [] and a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer;

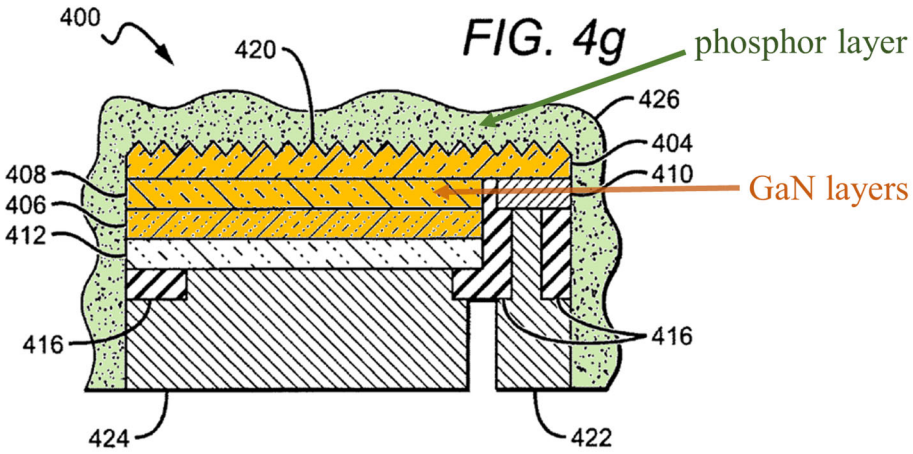
Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶66, 76-83.) While the optoelectronic component 1 shown in figure 2 of Wirth includes an isolation material 10b that separates the semiconductor LED (the combination of semiconductor function region 2 and the current spreading layer 5) and envelope 4 ("an optically transparent layer"), Wirth discloses that isolation material 10b is optional. (Ex. 1002 ¶76.) For example, the optoelectronic component 1 in figure 1 of Wirth does not include such isolation material, whereas the embodiment shown in figure 2 includes isolation material 10b. (*Compare* Ex. 1007, FIG. 1 *with* FIG. 2.) Therefore, a POSITA would have recognized that isolation material 10b is optional. (Ex. 1002 ¶76; Ex. 1007, 21:54-59 (describing that isolation material 10b is not present in figure 1).) Thus, Wirth discloses or suggests an implementation of Figure 2 without isolation material 10b. (Ex. 1002 ¶77.) In such an implementation, a first surface of said semiconductor LED (combination of semiconductor function region 2 and current spreading layer 5) contacts a first portion of a bottom surface of said optically transparent layer ("envelope 4"). (*Id.*)



(Ex. 1007, FIGs. 1, 2.)

To the extent Patent Owner argues that Wirth does not suggest such an implementation of Figure 2 in which isolation material 10b is not present, it would have been obvious to configure Wirth's optoelectronic component 1, as shown in figure 2, such that the device does not include the isolation material 10b. (Ex. 1002 ¶78.) As explained below, implementing figure 2 without layer 10b would have been a mere design choice. (*Id.*) Such an understanding is confirmed by Wirth's teachings (e.g., those relating to figure 1 in which no isolation material 10b is present) and the knowledge of a POSITA, as evidenced by contemporaneous prior

art such as Keller (Ex. 1005).[6] (Ex. 1002 ¶¶78-80.) For example, as shown in figure 4g below, Keller discloses an exemplary light emitting device 400 similar to the optoelectronic component described in Wirth. (Ex. 1005, 5:29-35, 7:30-32, 10:56-63, FIGS.4a-g.)



(*Id.*, FIG. 4g (annotated); Ex. 1002 ¶79.)

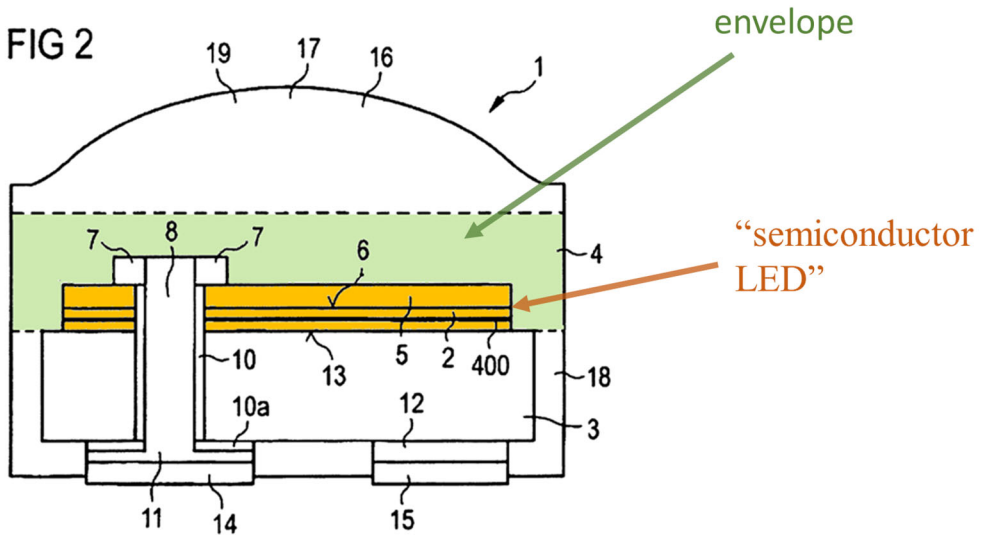
[6] Petitioner relies on the teachings of Wirth for the limitations of claim 1. Keller (Ex. 1005) demonstrates what a POSITA would have known at the time of the alleged invention of the '822 patent regarding the optionality of the isolation material like isolation material 10b in figure 2 of Wirth. *Int'l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016).

Like Wirth, Keller's exemplary light emitting device 400 includes a semiconductor LED containing a GaN layer comprised of n- and p-type layers 404, 406 and active region 408. (Ex. 1005, 7:44-63; Ex. 1002 ¶¶79-80.) The light emitting device 400 further includes a phosphor layer 426, similar to Wirth's envelope 4, with its bottom surface in contact with the top-surface of the LED semiconductor. (Ex. 1005, 10:38-39, FIG. 4g.) A POSITA would have thus understood that Keller's light emitting device 400 does not include an isolation material like the isolation material 10b in figure 2 of Wirth. (Ex. 1002 ¶80.) Accordingly, Keller confirms that a POSITA would have known at the time of the alleged invention of the '822 patent that the use of such an isolation material in an LED device was optional. (*Id.*)

Accordingly, at a minimum, an optoelectronic component 1 as illustrated in figure 2 without the isolation material 10b would have been obvious to a POSITA in view of the teachings of Wirth and the knowledge of POSITA. (*Id.* ¶81.) As discussed above, given that Wirth recognizes that the isolation material is optional, a POSITA would have recognized that, while Wirth provides illustrated embodiments where an isolation material is present, the inclusion of such material is a design choice. (*Id*.) That is, depending on the application or specification of the

optoelectronic component (e.g., its size, cost, or desired output), an isolation material may or may not be included in the optoelectronic component. (*Id.*)

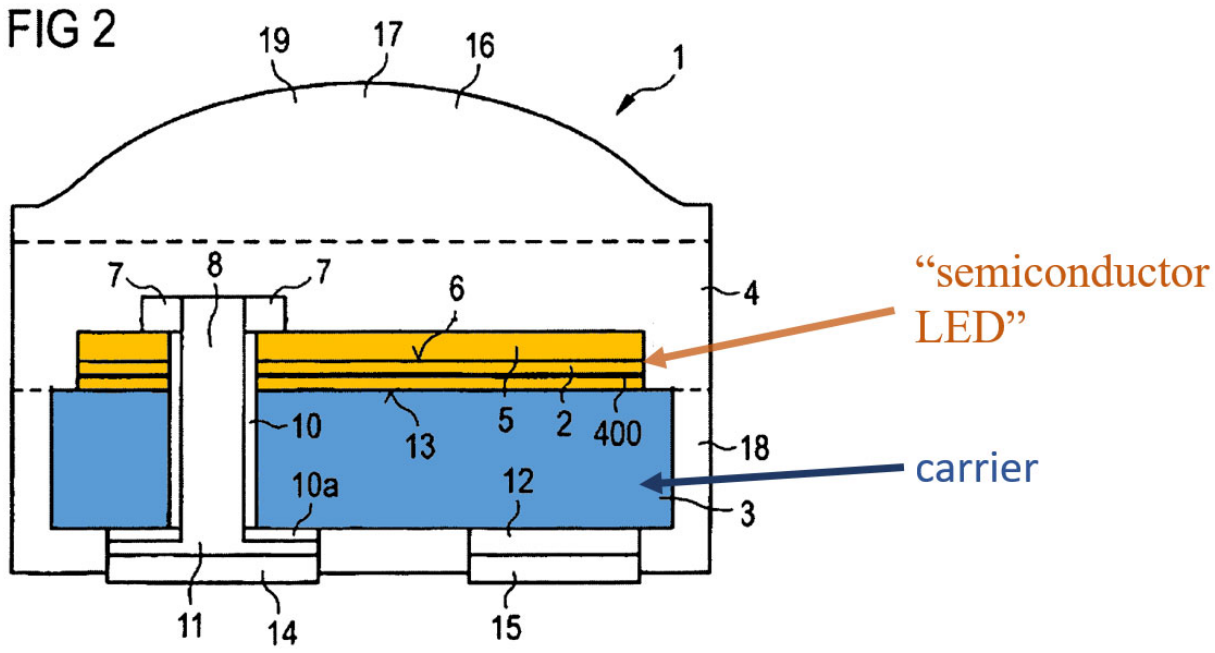
Accordingly, a POSITA also would have had a reasonable expectation of success in implementing such an optoelectronic component 1 as illustrated in figure 2 without the isolation material 10b. (*Id.* ¶82.) For example, a non-limiting example of such a configuration of Wirth's optoelectronic component 1 is illustrated below. (*Id.*) As shown in modified figure 2 below, a first surface of the semiconductor LED contacts a first portion of a bottom surface of the envelope ("optically transparent layer"). Therefore, Wirth discloses or suggests claim element 1.d(2). (*Id.* ¶83.)



(Ex. 1007, FIG. 2 (modified, annotated); Ex. 1002 ¶82.)

e) a carrier layer proximal to a second surface of said semiconductor LED, said first and second surfaces on opposing sides of said semiconductor LED;

Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶84-85.) As shown in the annotated figure below, optoelectronic component 1 includes a carrier 3 ("carrier layer") proximal to the bottom surface ("a second surface") of the semiconductor function region 2 portion of the "semiconductor LED" discussed above in claim element 1(d). (*Supra* Section IX.A.1(d); Ex. 1002 ¶84.) Indeed, Wirth discloses that carrier 3 is disposed underneath the semiconductor function region 2. (Ex. 1007, 18:39-43, FIGS. 1, 2; *see also id.*, 23:60-24:25; Ex. 1002 ¶84.)



(Ex. 1007, FIG. 2 (modified, annotated); Ex. 1002 ¶85.)

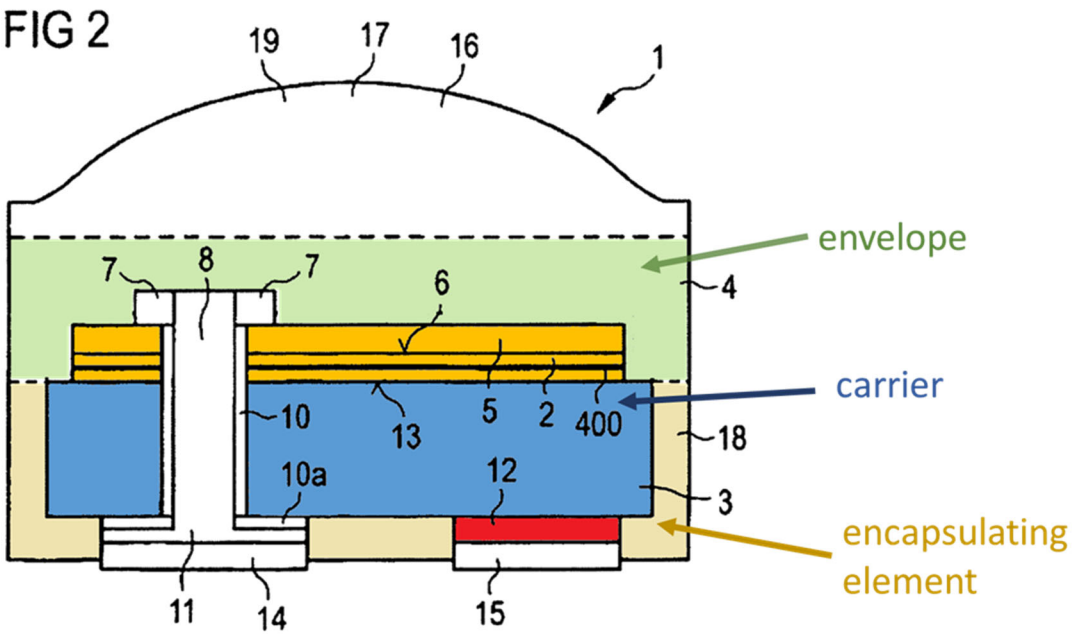
A POSITA would have further understood that Wirth discloses that the "first

and second surfaces [are] on opposing sides of said semiconductor LED," as claimed. (Ex. 1002 ¶85.) For example, as discussed above, the first surface corresponds to the top surface of the current spreading layer 5 overlying the semiconductor function region 2. (*See supra* Section IX.A.1.d.)

Accordingly, Wirth discloses or suggests claim element 1.e. (Ex. 1002 ¶85.)

f) a passivation layer disposed on said carrier layer and on an exposed portion of said bottom surface of said optically transparent layer;

Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶86-89.) The optoelectronic component 1 shown in modified figure 2 below includes encapsulating element 18 ("passivation layer") disposed on carrier 3 ("carrier layer") (Ex. 1007, 22:35-42) and on an exposed portion of the bottom surface of envelope 4 ("bottom surface of said optically transparent layer") (*id.*, 22:43-44). (*Id.*, 22:49-52; *see also id.*, 24:50; Ex. 1002 ¶¶86-88.) The encapsulating element 18 "embraces carrier 3, for example in a pincer-like manner, from the side thereof facing away from semiconductor function region 2." (Ex. 1007, 22:39-42; *see also id.*, 9:37-44.) Encapsulating element 18 is a "passivation" layer because it provides protection to the LED device from harmful external influences. (*Id.*, 21:54-66; Ex. 1002 ¶89.)

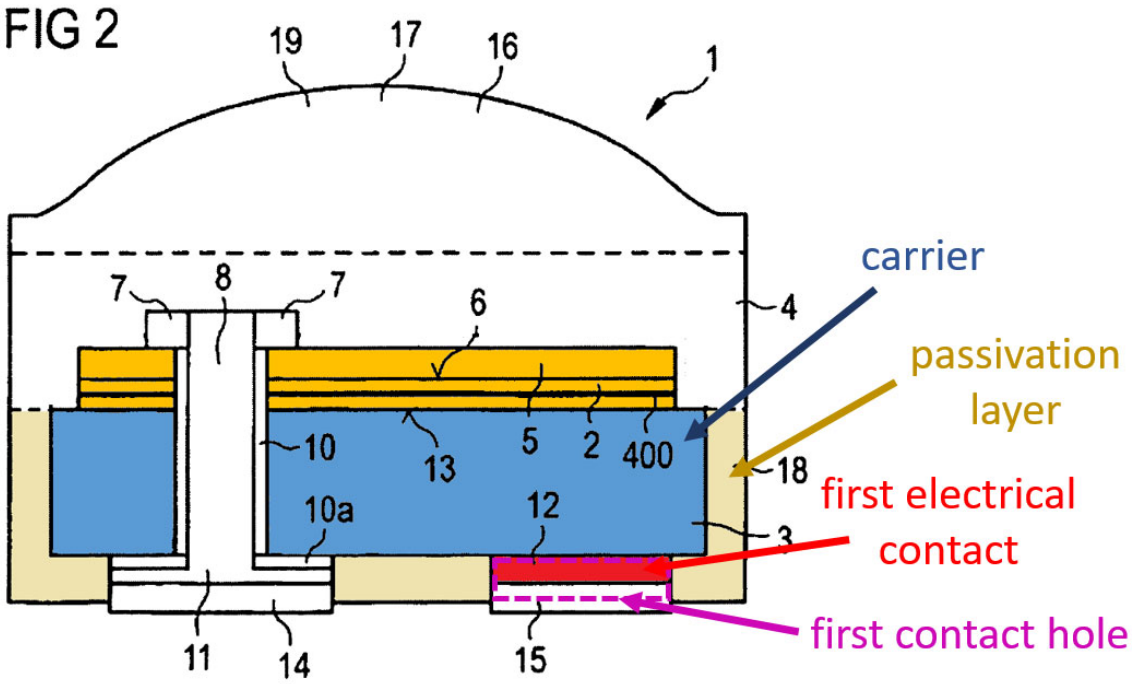


(Ex. 1007, FIG. 2 (modified, annotated); Ex. 1002 ¶86.)

Accordingly, Wirth discloses or suggests claim element 1.f. (Ex. 1002 ¶89.)

g) a first electrical contact disposed on said carrier layer in a first contact hole defined in said passivation layer; and

Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶90-91.) The optoelectronic component 1 includes an interconnect 12 ("first electrical contact") (Ex. 1007, 22:18-23) disposed on carrier 3 ("carrier layer") in a cavity ("first contact hole") defined in the encapsulating element 18 ("passivation layer") as shown in annotated modified figure 2 below. (*Id.*, 20:22-29 ("Interconnect 12 is conductively connected to the carrier, which is preferably implemented as electrically conductive, so that the semiconductor function region can be driven electrically via the first interconnect and the second interconnect."); Ex. 1002 ¶90.)



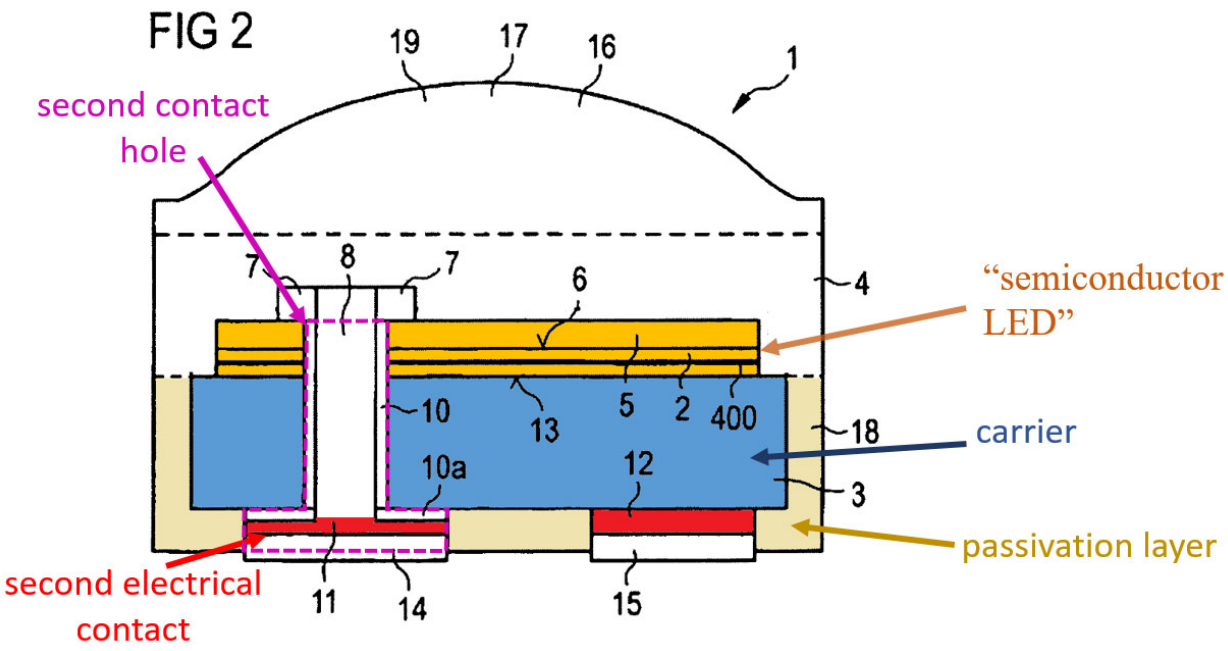
(Ex. 1007, FIG. 2 (modified, annotated); Ex. 1002 ¶90.)

Accordingly, Wirth discloses claim element 1.g. (Ex. 1002 ¶91.)

> **h) a second electrical contact disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED, said second electrical contact in electrical communication with said first surface of said semiconductor LED.**

Wirth discloses or suggests this limitation. (Ex. 1002 ¶¶92-93.) The optoelectronic component 1 includes an interconnect 11 ("second electrical contact") (Ex. 1007, 22:16-23) disposed in an opening/gap ("second contact hole") penetrating the encapsulating element 18 ("passivation layer"), carrier 3 ("carrier layer"), and the semiconductor function region ("semiconductor LED") as shown in

the figure below. (*Id.*, 22:16-20 ("Connecting conductor material 8 is electrically conductively coupled to first interconnect 11, which is electrically isolated by isolating material 10a from second interconnect 12 on the side comprising the main face of the carrier, located oppositely from the semiconductor function region."), 3:17-22 ("The opening preferably extends in the vertical direction, substantially perpendicularly to the lateral main direction of extension of the semiconductor function region, through the entire semiconductor function region."); *see also id.*, 18:48-54, 19:41-20:21; Ex. 1002 ¶92.)



(Ex. 1007, FIG. 2 (modified, annotated); Ex. 1002 ¶92.)

Accordingly, as explained above, Wirth discloses or suggests "a second electrical contact disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED," as claimed. (Ex. 1002 ¶93.)

A POSITA would have further understood that Wirth discloses or suggests that the "second electrical contact [is] in electrical communication with said first surface of said semiconductor LED," as recited in claim 1. (*Id*.) For example, Wirth explains that "connecting conductor material 8 is connected electrically conductively by a first interconnect 11 to the side of the carrier" (Ex. 1007, 20:10-21) and "contact layer 7 is electrically conductively connected to a connecting conductor material 8" (*id.*, 19:44-45), where the conductor material 8 is in electrical contact with the first surface of the semiconductor LED (*id.*, 21:5-11, 19:52-63 ("Connecting conductor material 8 extends in the vertical direction *through the opening in the active zone in semiconductor function region 2 from first contact layer 7 through the region of current spreading layer 5 and semiconductor function region 2 and through carrier 3 to the side of the carrier opposite from the semiconductor function region*.") (emphasis added).) (*Id.*, 22:16-28.)

Accordingly, Wirth discloses or suggests claim element 1.h. (Ex. 1002 ¶93.)

2. Claim 2

a) The light emitting device of claim 1 wherein said optically definable material is disposed in a portion of said optically transparent layer.

Wirth discloses or suggests claim 2. (Ex. 1002 ¶94.) Wirth discloses that "phosphor, particularly for generating mixed color light, is *preferably disposed in the envelope 4 as close as possible to the active zone*." (Ex. 1007, 23:51-53 (emphasis added); *see also id.*, 21:31-43.) Accordingly, a POSITA would have understood that the phosphor ("optically definable material") is disposed in a portion of the envelope 4 ("optically transparent layer"). (Ex. 1002 ¶94.)

3. Claim 5

a) The light emitting device of claim 2 wherein said optically definable material is embedded in said portion of said optically transparent layer.

Wirth discloses or suggests claim 5. (Ex. 1002 ¶¶95-96.) For example, Wirth discloses that "the envelope material can serve as a carrier matrix for phosphor particles, which can subsequently be applied to the semiconductor function region along with the material of the envelope." (Ex. 1007, 23:53-56; *see also id.*, 21:31-43.) Accordingly, a POSITA would have understood that the phosphor particles ("optically definable material") are embedded in a portion of the envelope 4 ("optically transparent layer"). (Ex. 1002 ¶96.)

4. Claim 6

a) The light emitting device of claim 1 wherein said optically transparent layer is comprised of silicone.

Wirth discloses or suggests claim 6. (Ex. 1002 ¶97.) For example, Wirth discloses that envelope 4 ("optically transparent layer") contains silicone. (Ex. 1007, 18:55-57 ("The semiconductor function region is surrounded by an envelope 4 that is preferably implemented as radiation-transparent and contains for example, a *silicone* ….") (emphasis added).)

5. Claim 7

a) The light emitting device of claim 6 wherein said optically definable material is comprised of phosphor.

Wirth discloses or suggests claim 7. (Ex. 1002 ¶98.) Wirth discloses that envelope 4 contains phosphor ("optically definable material"). (Ex. 1007, 23:51-53 ("A phosphor, particularly for generating mixed color light, is preferably disposed in the envelope 4 as close as possible to the active zone."); *see also id.*, 21:31-43.)

6. Claim 8

a) The light emitting device of claim 1 wherein said first and second electrical contacts are comprised of at least one of titanium, chrome, nickel, palladium, platinum, and copper.

Wirth discloses or suggests claim 8. (Ex. 1002 ¶99.) As discussed above, Wirth discloses an optoelectronic component 1 that includes a first and second

interconnects ("first and second electrical contacts"). (*See supra* Sections IX.A.1.g, h.) Wirth further discloses that "the first and/or the second interconnect *contain a metal, such as Ti, Pt, Al or Au*." (Ex. 1007, 20:26-29 (emphasis added).)

7. Claim 9

a) The light emitting device of claim 1 wherein said passivation layer is comprised of at least one of SiO_2, SiN, AlN, Al_2O_3, an epoxy, and an electrophoretic deposited paint.

Wirth discloses or suggests claim 9. (Ex. 1002 ¶100.) As discussed above, Wirth discloses an optoelectronic component 1 that includes an encapsulating element 18 ("passivation layer"). (*See supra* Section IX.A.1.f.) Wirth further discloses that "[t]he material of the encapsulating element can advantageously be selected arbitrarily within the framework of production capabilities." (Ex. 1007, 22:52-59.) That said, "[t]he elements of the encapsulation, particularly encapsulating element 18 and envelope 4, are preferably so constituted as to be substantially resistant to, preferably dimensionally stable against, the temperatures that occur during soldering for at least a period of time equal to that of the soldering process." (*Id.*, 23:33-38.) In particular, Wirth discloses that the encapsulating element "can be applied on-wafer, for example, by spin coating" (*id.*, 15:52-16:2) and notes that "materials particularly suitable for spin coating are, for example, . . .

Al_2O_3" (*id.*, 14:12-17). Accordingly, Wirth discloses or suggests claim 9. (Ex. 1002 ¶100.)

B. Ground 2: The Combination of Wirth and Lin Renders Obvious Claim 10

1. Claim 10

a) The light emitting device of claim 1 wherein said first and second electrical contacts comprise an electroplated material.[7]

Wirth in combination with Lin discloses or suggests claim 10. (Ex. 1002 ¶¶101-105.) As discussed above in Sections IX.A.1.g and IX.A.1.h, Wirth discloses a first and second interconnects 11 and 12 ("electrical contacts") that have been disposed onto the optoelectronic component 1. (*See supra* Sections IX.A.1.g, h.) Wirth further discloses that "the first and/or the second interconnect contain a metal, such as Ti, Pt, Al or Au." (Ex. 1007, 20:26-29.) However, Wirth is silent as to such interconnects containing "electroplated material."

[7] The specification of the '822 patent does not provide any disclosure describing the "first and second electrical contacts comprise an *electroplated* material" as recited in claim 10. (*See, e.g.*, Ex. 1001, generally.) While Petitioner addresses such features with the asserted prior art, Petitioner does not concede that the '822 patent provides adequate disclosure of the claimed feature.

(Ex. 1002 ¶102.) But it was well-known to use electroplating to deposit a material such as copper, onto aluminum and/or gold electrical contacts, like Wirth's interconnects, to improve the performance of the contacts. (*Id.*)

For example, Lin relates to "a semiconductor chip assembly in which a semiconductor chip is electrically connected to a support circuit by electroplated connection joints." (Ex. 1012, 1:15-19; *see also id*., 5:20-23 ("method of manufacturing the semiconductor chip assembly includes simultaneously electroplating the contact terminal and the connection joint").) That is, Lin discloses contacts that include electroplated metal. (Ex. 1012, 1:15-19, 5:20-23, Abstract.) For example, a pad or contact may contain an aluminum or gold base adapted to receive an electroplated metal, such as electroplated copper. (*Id.*, 6:23-30.) A POSITA would have known that copper (Cu) is a better conductor (and less expensive) than gold (Au). (Ex. 1002 ¶103.)

Lin explains that electroplating these contacts "provides an assembly that is reliable and inexpensive" (Ex. 1012, 14:24-26) because "[t]he connection joint is generally confined to the vicinity near the pad" (*id.*, 14:26-28) and "[t]he mode of the connection shifts from the initial mechanical coupling to metallurgical coupling to assure sufficient metallurgical bond strength" (*id.*, 14:28-31.) (*Id*, 3:25-26

("Electroplating is relatively easy to control and creates far less stress on the plated surface than electroless plating."), 14:31-33; Ex. 1002 ¶104.)

A POSITA would have recognized that using electroplating would have been a predictable way to deposit the material onto interconnects 11 and 12 ("electrical contacts") to improve reliability given how easy electroplating is to control. (Ex. 1002 ¶105.) Thus, using electroplating, as described in the above manner, for applying electroplated metal, such as copper, to the interconnects 11 and 12 would have been a mere combination of known components and technologies, according to known methods, to produce predictable results. (*Id.*); *KSR*, 550 U.S. at 416.

Therefore, Wirth in combination with Lin discloses or suggests "wherein said first and second electrical contacts comprise an electroplated material." (Ex. 1002 ¶105.)

C. Ground 3: The Combination of Wirth and AAPA Renders Obvious Claims 1, 2, and 5-9

As discussed above, Wirth discloses or suggests the features of claims 1, 2, and 5-9. (*Supra* Section IX.A.) As also discussed above, Wirth discloses or suggests "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region," as recited in claim element 1.d. In particular, Wirth would have disclosed or suggested to a POSITA that active zone

400 is an "intrinsic region." (*Supra* Section IX.A.1.d.) But to the extent PO argues or the Board finds that Wirth does not disclose or suggest such an intrinsic region, a POSITA would have found it obvious to use an "intrinsic" region for the active zone 400 in Wirth's GaN LED as the inclusion of such an intrinsic layer between p- and n-type layers was a well-known conventional structure, as admitted by the '822 patent. (Ex. 1002 ¶106-110; Ex. 1001, 3:32-34 ("These LEDs comprise a *P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer*.") (emphasis added); *see also id.,* 4:21-25.) Indeed, using an "intrinsic" region for the active zone 400 in Wirth's GaN LED would have been obvious because it would have constituted applying a known feature (an intrinsic region provided between n and p-doped layers in a GaN LED) to a particular device (the Wirth GaN LED) to achieve a predictable result (emission of light by radiative recombination of a hole and an electron in the intrinsic region). (Ex. 1002 ¶109); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). For the above reasons, Wirth in combination with the AAPA, discloses or suggests that the semiconductor function region 2 and current spreading layer 5 constitute "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region." (Ex. 1002 ¶110.)

The above modification of Wirth based on the AAPA does not affect the remainder of the analysis in Section IX.A, which applies equally to this ground. Thus, Wirth in combination with the AAPA discloses or suggests claims 1, 2, and 5-9 for the reasons discussed in Section IX.A and those discussed above. (*Id*.; *Supra* Section IX.A.)

D. Ground 4: The Combination of Wirth, AAPA, and Lin Renders Obvious Claim 10

As discussed above in Section IX.B, Wirth in combination with Lin renders obvious claim 10. (*Supra Section* IX.B.) As discussed above in Section IX.C, the analysis for claim 1 is modified to include reliance on the AAPA. (*Supra Section* IX.C.) The reliance on the AAPA does not, however, alter the analysis for claim 10 set forth in Section IX.B. Thus, claim 10 is rendered obvious by Wirth in combination with AAPA and Lin for reasons similar to those discussed above in Section IX.B. (*Supra Section* IX.B.) For example, the Wirth-AAPA combination would have been modified based on Lin for the same reasons discussed above in Section IX.B to arrive at claim 10. (Ex. 1002 ¶111.)

E. Ground 5: The Combination of Wirth and Camras Renders Obvious Claims 1, 2, and 5-9

As discussed above in Section IX.A, Wirth discloses or suggests the features of claims 1, 2, and 5-9. (*Supra* Section IX.A.) As also discussed above, Wirth

discloses or suggests "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region," as recited in claim element 1.d. In particular, Wirth would have disclosed or suggested to a POSITA that active zone 400 includes an "intrinsic region." (*Supra* Section IX.A.1.d.) But to the extent PO argues or the Board finds that Wirth does not disclose or suggest such an intrinsic region between positively and negatively doped regions, Camras discloses such an LED structure, and a POSITA would have found it obvious to use an "intrinsic" region in the active zone 400 of Wirth's GaN LED in view of Camras. (Ex. 1002 ¶¶112-115.)

Camras, like Wirth, is directed to LED structures that include an n-type layer, a p-type layer, and a light emitting active region. (Ex. 1006, 2:27-32, 2:44-61.) Camras discloses that the light emitting active region of the LED is between p-type layer 110 and n-type layer 108 and includes intrinsic (undoped) material. (Ex. 1006, 2:44-54 ("*active region 112 includes one or more semiconductor layers that are* doped n-type or p-type or are *undoped*") (emphasis added); Ex. 1002 ¶115.) Camras further discloses that "[a]ctive region 112 emits light upon application of a suitable voltage across contacts 114 and 116." (Ex. 1006, 2:62-63.) Figure 1B of Camras,

shown in annotated form below, illustrates the intrinsic layer 112 between p-type layer 110 and n-type layer 108.

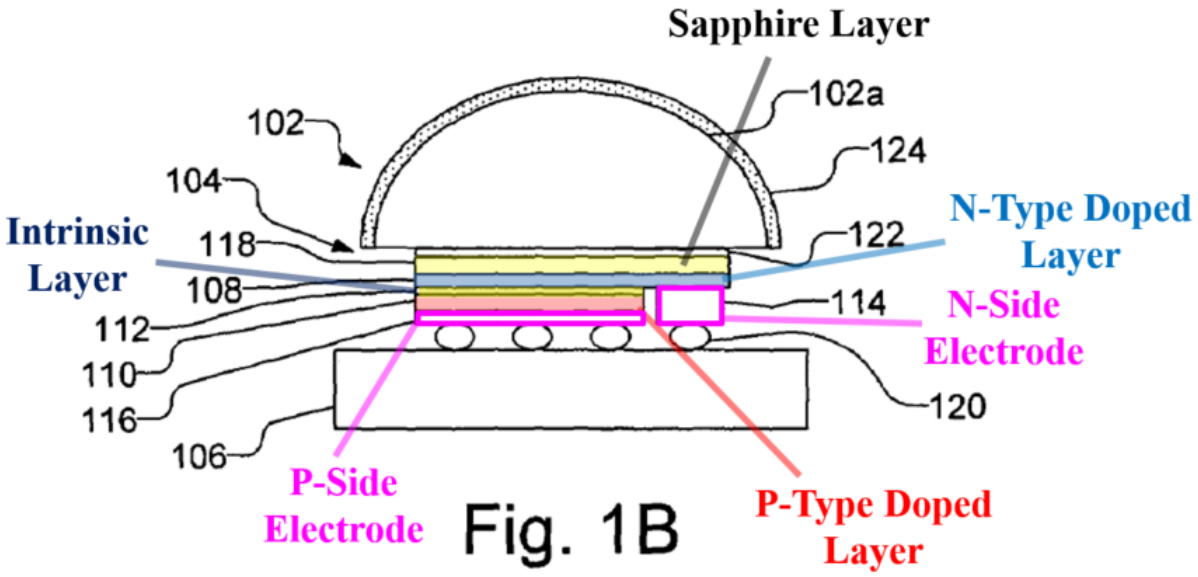


Fig. 1B

(Ex. 1006, FIG. 1B (annotated); Ex. 1002 ¶116.)

A POSITA would have looked to Camras for guidance regarding implementing LED devices as disclosed by Wirth, particularly because Camras and Wirth are references in the same field that disclose LED devices with many common features. (Ex. 1002 ¶117.) Having looked to Camras, such a POSITA would have found it obvious to implement the light-emitting active zone 400 in Wirth such that it includes an intrinsic layer between the p-type and n-type doped regions. (*Id.*)

The semiconductor LED disclosed by Wirth is specified to include a p-type layer, an n-type layer, and a light emitting active zone between those layers. (Ex.

1007, 40:36-43.) As discussed above, Camras discloses LED structures that include an intrinsic light-emitting layer sandwiched between p-type and n-type regions. (Ex. 1006, 2:44-52.) A POSITA would have found it obvious to use an intrinsic light-emitting layer between the p-type and n-type doped regions, as disclosed by Camras, in conjunction with an LED device as disclosed by Wirth. (Ex. 1002 ¶118.)

Such a POSITA would also have been motivated to use an intrinsic layer for the light emitting layer in an LED as disclosed by Wirth because using an intrinsic layer is one of a limited number of alternatives disclosed by Camras, where those alternatives include p-type, n-type, and intrinsic semiconductor material. (Ex. 1006, 2:50-52; Ex. 1002 ¶119.) Indeed, as discussed above in Section IX.C, the '822 patent discloses that LEDs with an intrinsic layer between p-type and n-type material were known and in use. (*See supra* Section VII; Ex. 1001, 3:27-34, 3:52-55, FIG. 1; Ex. 1002 ¶119.) Similarly, Sugawara also demonstrates that a POSITA would have been aware of the use of intrinsic layers between p- and n-type layers in LEDs. (Ex. 1009, 3:45-51.)[8]

[8] Sugawara is cited to demonstrate the knowledge of a POSITA at the time of the alleged invention.

A POSITA would have found it straightforward to use an intrinsic layer as disclosed by Camras in an LED device as disclosed by Wirth because Camras discloses such an intrinsic layer in a device very similar to that of Wirth. (Ex. 1002 ¶120.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. *KSR*, 550 U.S. at 416. Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Camras, as well as Sugawara and the '822 patent (*see supra* Section VII.A; Ex. 1001, 3:27-34, 3:52-55, FIG. 1), LEDs with intrinsic light-emitting layers were well known in the art. (Ex. 1002, ¶120.) *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) ("only a reasonable expectation of success, not a guarantee, is needed" in an obviousness analysis).

For the above reasons, Wirth in combination with Camras discloses or suggests that the semiconductor function region 2 and current spreading layer 5 constitute "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region." (Ex. 1002 ¶121.)

The above modification of Wirth based on Camras does not affect the remainder of the analysis in Section IX.A, which applies equally to this ground. (*Id*.)

Thus, Wirth in combination with Camras discloses or suggests claims 1, 2, and 5-9 for the reasons discussed in Section IX.A and those discussed above. (*Id*.; *Supra* Section IX.A.)

F. Ground 6: The Combination of Wirth, Camras, and Lin Renders Obvious Claim 10

As discussed above in Section IX.B, Wirth in combination with Lin renders obvious claim 10. (*Supra Section* IX.B.) As discussed above in Section IX.E, the analysis for claim 1 is modified to include reliance on Camras. (*Supra Section* IX.E.) The reliance on the Camras does not, however, alter the analysis for claim 10 set forth in Section IX.B. Thus, claim 10 is rendered obvious by Wirth in combination with Camras and Lin for reasons similar to those discussed above in Section IX.B. (*Supra* Section IX.B.) For example, the Wirth-Camras combination would have been modified based on Lin for the same reasons discussed above in Section IX.B to arrive at claim 10. (Ex. 1002 ¶122.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

The Board should decline any arguments for a discretionary denial under 35 U.S.C. §§ 314(a) or 325(d). The '822 patent is not at issue in any other proceeding before the Board. Therefore, the factors concerning discretionary denial under 35 U.S.C. § 314(a) set forth in *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 3, 8, 15-19 (Sept. 6, 2017), are not applicable here. Nor does Petitioner rely on any art or arguments that are the same or substantially the same as those previously presented to the Office. *See Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) (precedential).

Similarly, *NHK Spring Co., Ltd. v. Intri-Plex Techs, Inc.*, IPR2018-00752, Paper 8 (P.T.A.B. Sept. 12, 2018) does not apply here. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 3 (P.T.A.B. Mar. 20, 2020) (precedential) ("*NHK* applies … where the district court has set a trial date to occur earlier than the Board's deadline to issue a final written decision in an instituted proceeding."). The six-factor test addressed in *Fintiv* favors institution. *See id.*, 5-6.

For the *first factor* (stay), there is no stay, but courts routinely issue stays after institution. *Western Digital Corp. et al v. Kuster*, IPR2020-01391, Paper 10 at 8-9 (Mar. 11, 2021); *Samsung Elec. Am., Inc. v. Snik LLC*, IPR2020-01427, Paper 10 at

10 (Mar. 9, 2021). At a minimum, this factor deserves little weight given that factors two through four and six weigh in favor of institution. *See Fintiv*, 7.

The second (proximity of trial dates) and third (investment in parallel proceedings) factors weigh in favor of institution. The district court has not set a trial date, and, there has not been significant resource investment by the court and the parties, particularly compared to the resource expenditures leading up to a trial. *See Resideo Techs., Inc. v. Innovation Sciences, LLC*, IPR2019-01306, Paper 19 at 11 (Jan. 27, 2020). Furthermore, the court's order governing patent proceedings sets a default Markman hearing date as "23 weeks after [case management conference] (or as soon as practicable)" and a default trial date as "52 weeks after Markman hearing (or as soon as practicable)." (Ex. 1022, 9, 11); *see Precision Planting, LLC. v. Deere & Co.*, IPR2019-01044, Paper 17 at 14-15 (P.T.A.B. Dec. 2, 2019) (weighs against finding that case is at "an advanced stage"); *Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 30 (P.T.A.B. Oct. 7, 2019) (same). Additionally, WDTX civil trials "may possibly slip" due to "months of backlogged trials." *HP Inc. v. Slingshot Printing LLC*, IPR2020-01085, Paper 12 at 7 (Jan. 14, 2021). Nevertheless, even "an early trial date" is "non-dispositive" and simply means that "the decision whether to institute will likely implicate other factors," which, as explained, favor institution. *Fintiv*, 5, 9.

Furthermore, the Board has held "that it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding." *Id.* at 11. Here, Patent Owner has not served its infringement contentions.

The fourth factor (overlap) also weighs in favor of institution. PO's infringement contentions only assert claims 1, 2, 5, 7, and 9 of the '822 patent while the present Petition challenges claims 1, 2 and 5-10 of the '822 patent. (Section IX.) Moreover, Petitioner hereby stipulates that, if the IPR is instituted, Petitioner will not pursue the IPR grounds in the district court litigation. Thus, "[i]nstituting trial here serves overall system efficiency and integrity goals by not duplicating efforts and by resolving materially different patentability issues." *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 at 19 (P.T.A.B. June 15, 2020) (finding the fourth factor "strongly favored" institution even though there was no stipulation and a significant dispute about the extent of overlap); *see also Sand Revolution II, LLC v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 12 (P.T.A.B. June 16, 2020) (finding the fourth factor weighs in favor of institution due, in part, to petitioner's stipulation that it will not pursue the same grounds in district court).

For the fifth factor (parties), the Petitioner and PO are the same parties as in district court.

The sixth factor (other circumstances) weighs in favor of institution given the undeniable similarity between Petitioner's primary reference and the '822 patent and that Petitioner diligently filed this Petition within six months of PO's complaint. (Ex. 1021.) Institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020). This Petition is the ***sole*** challenge to the '822 patent before the Board—a "crucial fact" favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020).

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for the challenged claims based on each of the specified grounds.

Respectfully submitted,

Dated: September 10, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,786,822 contains, as measured by the word-processing system used to prepare this paper, 8,160 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: September 10, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on September 10, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,786,822 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

Intrinsic Law Corp.
221 Moody Street
Waltham MA 02453

A courtesy copy was also sent via electronic mail to the Patent Owner's litigation counsel at the following addresses:

E. Leon Carter
lcarter@carterarnett.com
Scott W. Breedlove
sbreedlove@carterarnett.com
Joshua J. Bennett
jbennett@carterarnett.com
Bradley D. Liddle
bliddle@carterarnett.com
Nathan Cox
ncox@carterarnett.com
CARTER ARNETT PLLC
8150 N. Central Expy, 5th Floor
Dallas, Texas 75206

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)