UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

LED WAFER SOLUTIONS LLC,
Patent Owner

Patent No. 9,502,612

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,502,612

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I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") requests *inter partes* review ("IPR") of claims 1-9 ("the challenged claims") of U.S. Patent No. 9,502,612 ("the '612 patent") (Ex. 1001) assigned to LED Wafer Solutions LLC ("Patent Owner" or "PO"). For the reasons below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES

Real Parties-in-Interest: Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters: The '612 patent is asserted in the following civil action *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd. et al.*, 6-21-cv-00292 (W.D. Tex). Petitioner previously filed petitions challenging U.S. Patent Nos. 8,952,405, 8,941,137, and 9,786,822, which are also at issue in the same Western District of Texas litigation. The '612 patent is also challenged by Seoul Semiconductor Co., Ltd. ("SSC") in IPR No. 2021-01504 ("SSC IPR").

Counsel and Service Information: Lead counsel: Naveen Modi (Reg. No. 46,224). Backup counsel: (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Quadeer A. Ahmed (Reg. No. 60,835).

Service information is Paul Hastings LLP, 2050 M Street NW, Washington, DC 20036, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-Samsung-LEDWafer-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '612 patent is available for review, and Petitioner is not barred/estopped from requesting review on the grounds herein.

V. PRECISE RELIEF REQUESTED

A. Claims for Which Review Is Requested

Petitioner requests review and cancellation of claims 1-9 as unpatentable based on the following grounds.

B. Statutory Grounds of Challenge

Ground 1: Claims 1, 2, 8, and 9 are unpatentable under 35 U.S.C. § 103 based on U.S. Patent Publication No. 2003/0232455 to Tanaka ("Tanaka") (Ex. 1005);

Ground 2: Claim 3 is unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with U.S. Patent No. 7,233,028 to Weeks et al. ("Weeks") (Ex. 1006);

Ground 3: Claims 4-7 are unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with U.S. Patent Publication No. 2007/0284602A1 to Chitnis et al. ("Chitnis") (Ex. 1007);

Ground 4: Claims 1, 2, 8, and 9 are unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with the Applicant Admitted Prior Art (AAPA);

Ground 5: Claim 3 is unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with the AAPA and Weeks;

Ground 6: Claims 4-7 are unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with the AAPA and Chitnis;

Ground 7: Claims 1, 2, 8, and 9 are unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with U.S. Patent No. 7,419,839 to Camras et al ("Camras") (Ex. 1008);

Ground 8: Claim 3 is unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with Camras and Weeks; and

Ground 9: Claims 4-7 are unpatentable under 35 U.S.C. § 103 based on Tanaka in combination with Camras and Chitnis.[1]

[1] For the Grounds presented, Petitioner does not rely on any prior art reference other than those listed here. Any other references discussed herein are provided to show

The '612 patent issued from an application filed October 7, 2013, which was a continuation-in-part of an earlier application. Thus, the effective filing date of the '612 patent is no earlier than October 7, 2013. However, the references relied upon in the above Grounds would qualify as prior art with respect to the '612 patent even if the '612 patent is entitled to an earlier priority date including the earliest priority date of September 20, 2009.

Tanaka published on December 18, 2003. Weeks issued on June 19, 2007. Chitnis published on December 13, 2007. Camras issued on September 2, 2008. Thus, Tanaka, Weeks, Chitnis, and Camras qualify as prior art at least under 35 U.S.C. § 102(a)(1).

AAPA qualifies as prior art at least under pre-AIA 35 U.S.C. § 311(b) with respect to the '612 patent. *See, e.g., One World Techs., Inc. v. Chamberlain Group, Inc.*, IPR2017-00126, slip op. at 9-10 (May 4, 2017) (Paper 8); *see also Apple Inc., v. Qualcomm Inc.,* IPR2018-01316, slip op. at 22 (January 18, 2019) (Paper 7).

Tanaka, Weeks, Chitnis, and Camras were not considered during prosecution of the '612 patent (Ex. 1001, Cover ("References Cited"); *see also generally* Ex. 1004).

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the state of the art at the time of the alleged invention. *Int'l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016).

VI. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art as of (i) the October 7, 2013 filing date of the application from which the '612 patent issued and (ii) the September 20, 2009 filing date of the earliest priority application to which the '612 patent claims priority ("POSITA") would have had a bachelor's degree in electrical engineering, material science, or the equivalent, and two or more years of experience with light emitting diodes (LEDs). (Ex. 1002 ¶¶20-21.)[2] More education can supplement practical experience and vice versa. (*Id.* ¶20.)

VII. OVERVIEW OF THE '612 PATENT

The '612 patent relates to "a light emitting diode (LED) device." (Ex. 1001, 1:21-25; Ex. 1002 ¶¶30-34.) The '612 patent admits that light emitting diode (LED) devices were conventional and well-known and, with reference to Figure 1 below, describes a known prior art Gallium Nitride (GaN) LED device. (Ex. 1001, 1:29-39, 2:1-3:6, 4:18, 5:4-17, 5:29-45; FIG. 1.)

[2] Petitioner submits the declaration of Dr. R. Jacob Baker, Ph.D., P.E. (Ex. 1002), an expert in the field of the '612 patent. (Ex. 1002 ¶¶5-15; Ex. 1003.)

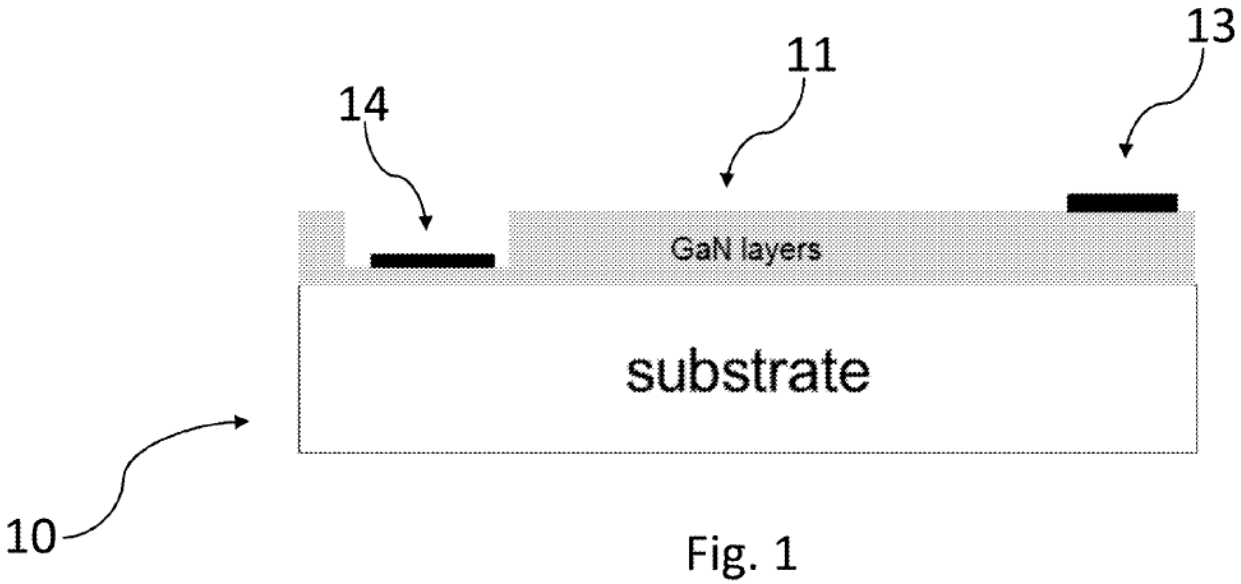

Fig. 1
(Prior Art)

(Ex. 1001, FIG. 1.)

As disclosed by the ’612 patent:

> Modern LED devices are based on semiconducting materials and their properties. For example, some LEDs are made using Gallium Nitride (GaN) . . . Ga LEDs are typically epitaxially grown on a sapphire substrate. These LEDs comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer.

(Ex. 1001, 5:4-17.)

The prior art GaN LED chip 10 of Figure 1 includes GaN layers 11 grown on a substrate 12. (Ex. 1001, 5:29-32.) The GaN layers 11 include an n-type doped region disposed directly adjacent to substrate 12 and electrically connected to pad

14 and a p-type doped region electrically connected to pad 13. (*Id.*, 5:34-37.) As noted above, the '612 patent states that GaN LEDs "comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer." (*Id.*, 5:9-11.) In other words, the '612 patent admits that prior art GaN LEDs have an intrinsic region disposed between an n-type doped layer and a p-type doped layer. (Ex. 1002 ¶31.)

The disclosed embodiments of the '612 patent build on the prior art device of Figure 1. For example, the '612 patent discloses "methods and apparatus for LED packaging to efficiently remove excess heat during active operation." (Ex. 1001, 4:44-46; *see also id.*, 3:37-48, 4:46-52, 4:63-5:3.) Like the prior-art LED device in Figure 1 above, the device of Figure 5 includes a substrate, GaN layers constituting the semiconductor LED, and n-type/p-type pads 55, 56. (*Id.*, 8:60-9:28, FIG. 5; *see also id.*, 5:29-45, FIG. 1.)

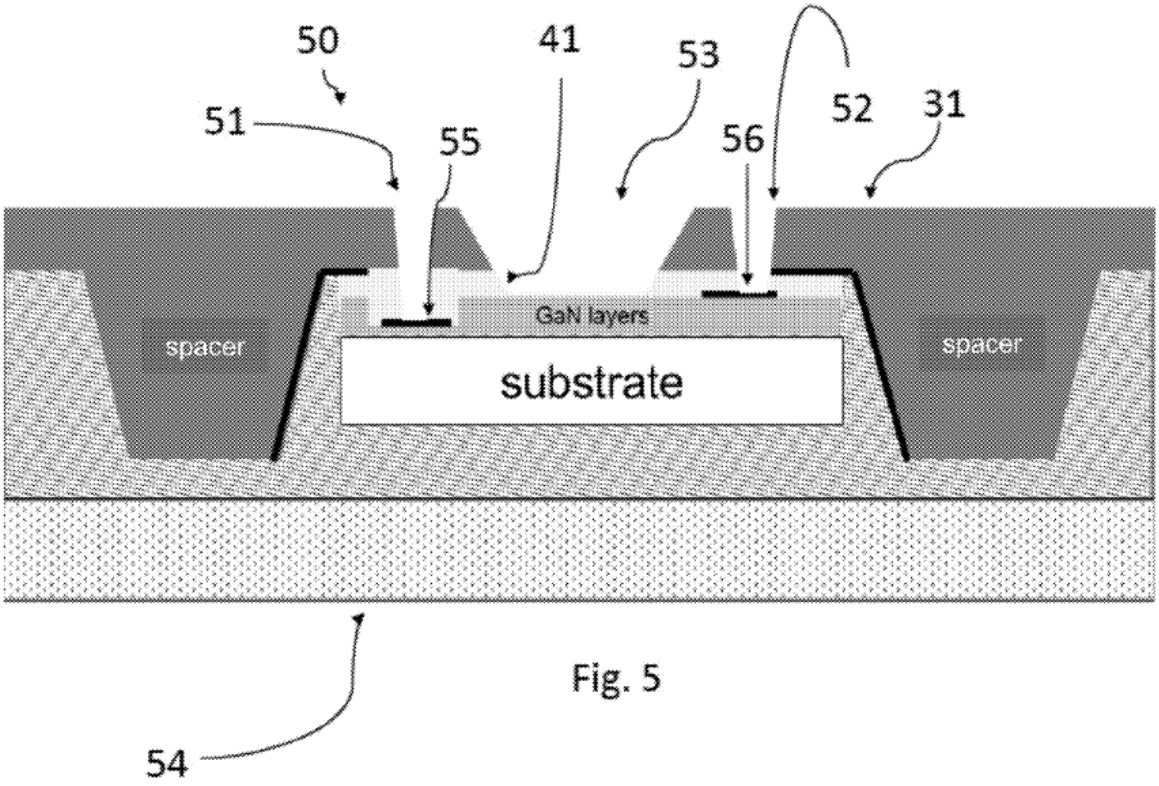

Fig. 5

(*Id.*, FIG.5; Ex. 1002 ¶32.)

The Figure 5 device further includes an adhesive layer 41, silicon wafer 31, peripheral reflectors 34, 35 (labeled in Figure 4), a silicone encapsulation 42 that is an optically transmissive layer, and a relief defined by the silicon wafer 31 and adhesive layer 41. (*Id.*, 6:45-64 (describing silicon wafer 31 and peripheral reflectors 34, 35), 7:22-29 (describing adhesive layer 41), 7:54-58 (describing silicone encapsulation 42), 9:1-28 (describing the relief).) The '612 patent discloses that "[t]here are two types of geometrical reliefs which are evident in [] FIG. 5,"

namely (i) a "via (hole)" such as vias 51, 52 and (ii) a thermally conducting hole 53. (*Id.*, 9:1-28; Ex. 1002 ¶33.)

As explained below and in the accompanying declaration of Dr. Baker, all the limitations in the challenged claims were known in the prior art. (*See infra* Section IX; Ex. 1002 ¶¶34, 84, 16-19, 22-29 (technology background), 36-52 (discussing the prior art at issue in this petition), 53-183 (discussing prior art disclosures in view of each claim's limitations).)

VIII. CLAIM CONSTRUCTION

Under the applicable standard in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), claim terms are typically given their ordinary and customary meanings as understood by a POSITA at the time of the invention based on the claim language, specification, and the prosecution history of record. *Phillips*, 415 F.3d at 1313; *see also id.* at 1312-16. The Board, however, only construes the claims when necessary to resolve the controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citation omitted). Petitioner believes no express constructions of any claim terms are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002 ¶35.)[3]

[3] Petitioner reserves all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §§ 101 or 112, in district court as relevant to

IX. DETAILED EXPLANATION OF GROUNDS

A. Ground 1: Tanaka Renders Obvious Claims 1, 2, 8, and 9

1. Claim 1

a) A light emitting device, comprising:

To the extent that the preamble is limiting, Tanaka discloses the limitations therein. (Ex. 1002 ¶¶53-54.) For example, Tanaka discloses a light emitting element 10 ("light emitting device") including a blue-color light-emitting diode chip 70 in its Figure 7 embodiment. (Ex. 1005 ¶[0072], FIG. 7; *see also id.*, Abstract, ¶¶[0004], [0067], [0072], FIG. 6.)[4]

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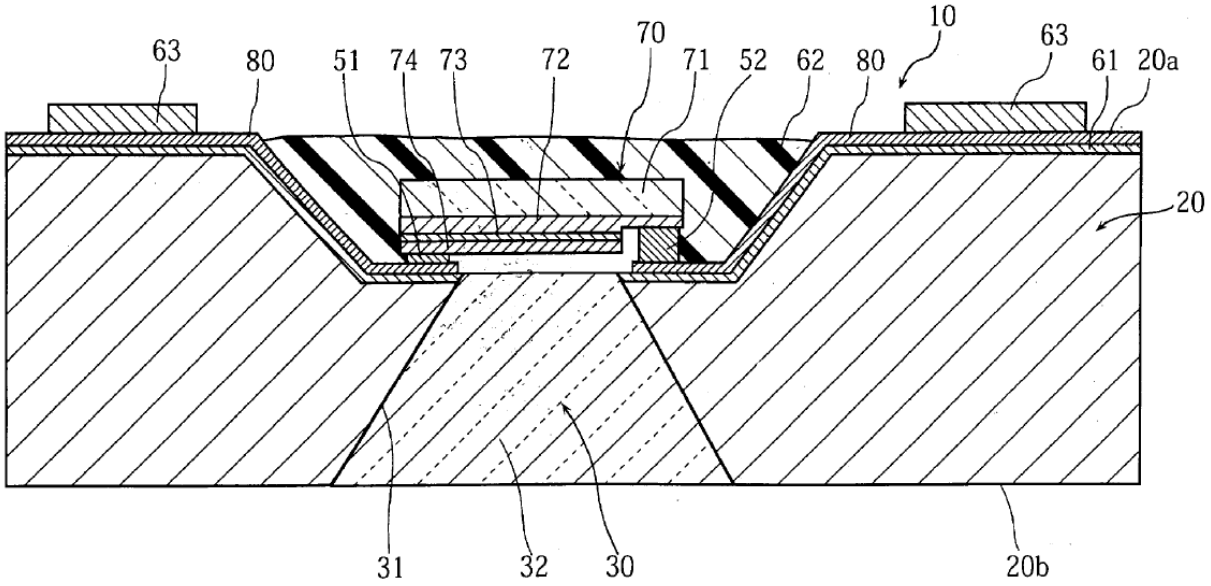
those proceedings. *See, e.g.*, *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11-13 (November 10, 2020). A comparison of the claims to any accused products in litigation may raise controversies that are not presented here given the similarities between the references and the patent.

[4] Tanaka's description of Figure 7 builds on Figure 6, and thus the description of components in Figure 6 applies to similar components in Figure 7. (Ex. 1002 n.4.) Indeed, Tanaka specifically states that, aside from the differences specifically described for Figure 7, "[t]he structure is otherwise the same as in the embodiment shown in FIG. 6." (Ex. 1005 ¶[0072], FIGS. 6-7.) Thus, Tanaka does not repeat the

FIG.7



(Ex. 1005, FIG. 7; Ex. 1002 ¶54; *see also* Ex. 1002 ¶¶36-43.)

b) a substrate having opposing first and second substrate surfaces;

Tanaka discloses this limitation. (Ex. 1002 ¶¶55-57.) For example, Tanaka discloses that its light emitting element 10 ("light emitting device") includes a sapphire substrate 71 ("substrate") having opposing first and second surfaces, as shown in annotated Figure 7 below. (Ex. 1005 ¶¶[0068], [0072] ("[T]he [blue-color

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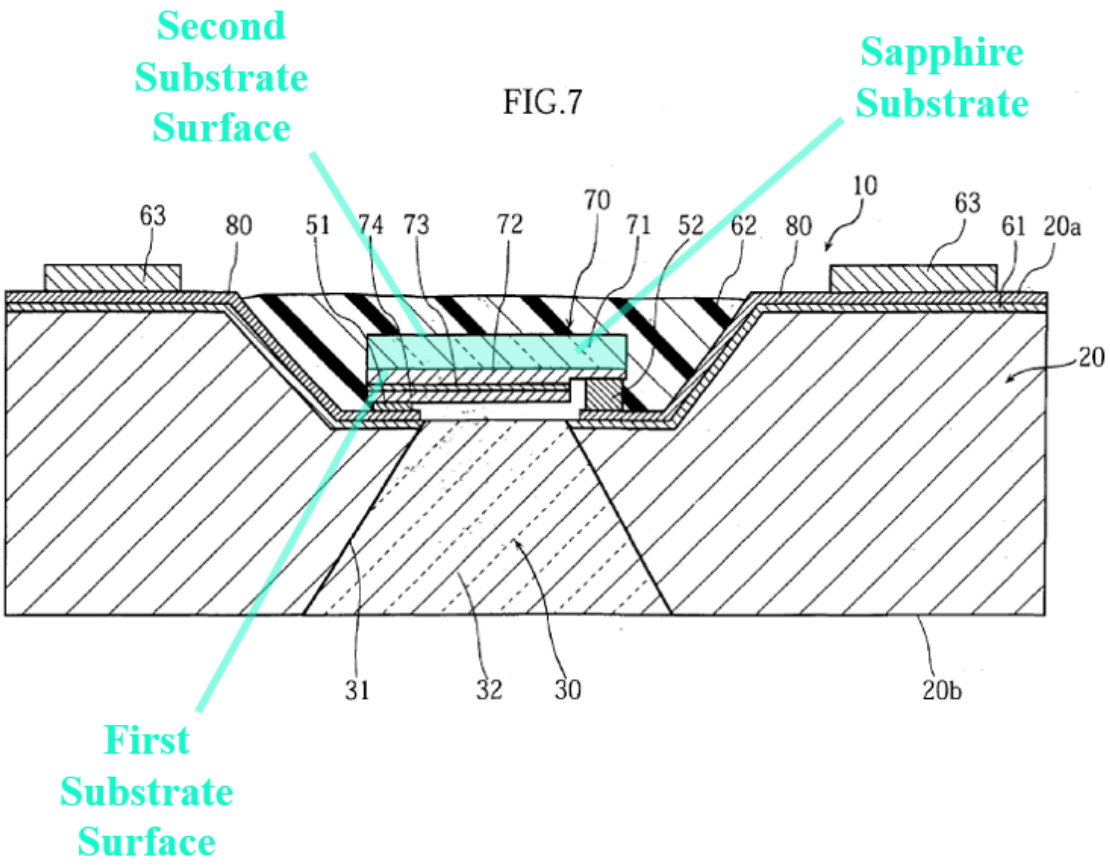
description of the functions of the common components shown in its Figures. (Ex. 1002 n.4.)

light-emitting diode] chip [70] is mounted on a sapphire substrate 71.").)[5] The '612 patent similarly discloses that its wafer 200 may be made of sapphire. (Ex. 1001, 5:58-60 ("*sapphire* substrate 22")[6]; *see also id.*, 2:1-4, 5:29-30; Ex. 1002 ¶56.)



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶55.)

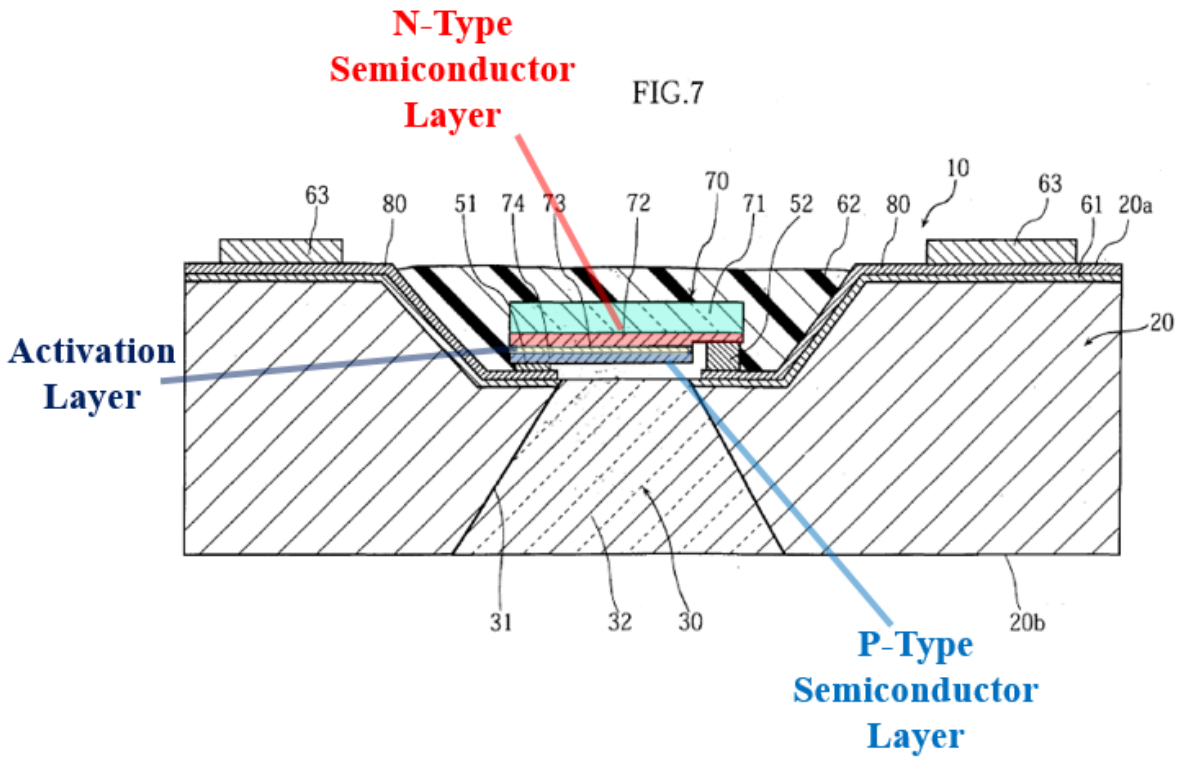
[5] *See* n.4.

[6] Emphasis added unless otherwise noted.

c) a semiconductor LED including doped and intrinsic regions thereof, said semiconductor LED having opposing first and second LED surfaces, said first LED surface disposed on the first substrate surface;

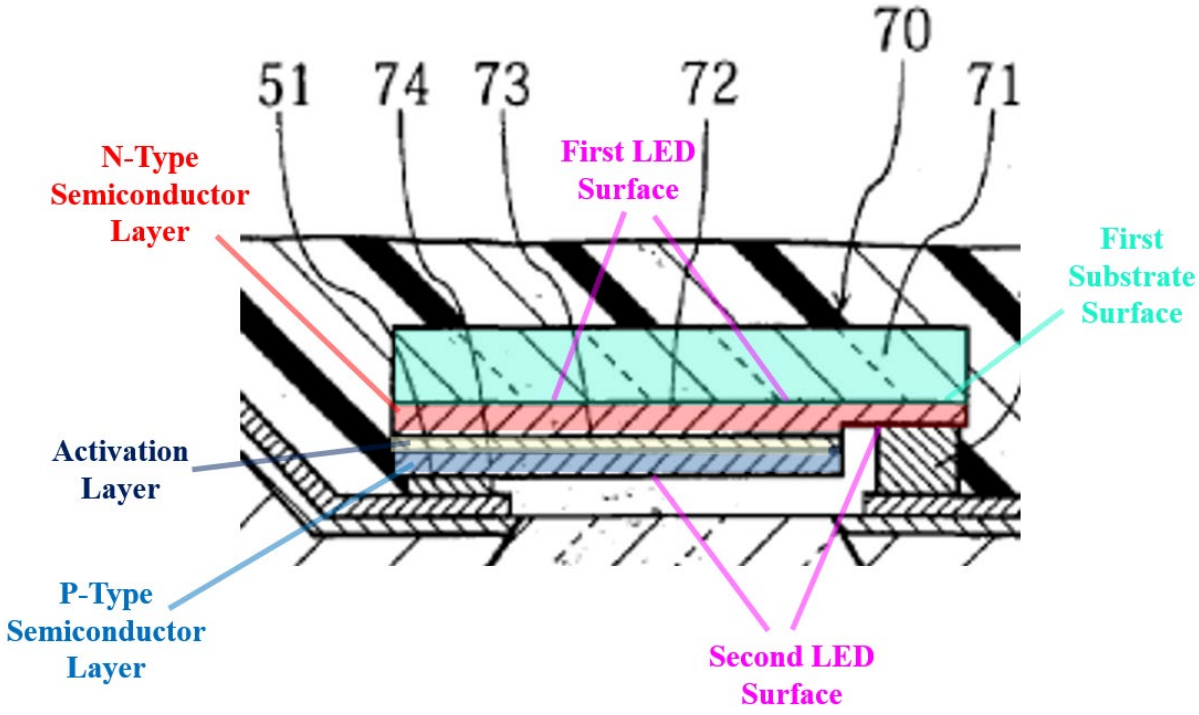
Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶58-63.) For example, Tanaka discloses that its light emitting element 10 ("light emitting device") includes blue-color light-emitting diode chip 70 with an N-type semiconductor layer 72, a P-type semiconductor layer 74, and an activation layer 73 between the N- and P-type layers (collectively, the claimed "semiconductor LED"). (Ex. 1005 ¶¶[0068] ("The blue-color light-emitting diode chip 70 fabricated in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer)."), [0072], FIG. 7.)[7]

[7] *See* n.4.



(*Id.*, FIG. 7 (annotated); Ex. 1002 ¶58.)

As shown in the enlarged annotated excerpt of Figure 7 below, Tanaka's semiconductor LED has opposing first and second LED surfaces, and the first LED surface is disposed on the first substrate surface of the sapphire substrate 71 ("substrate").



(Ex. 1005, FIG. 7 (excerpt, annotated); Ex. 1002 ¶59.)

Tanaka also suggests (if not discloses to a POSITA) that the activation layer 73 includes an "intrinsic region." (Ex. 1002 ¶60.) First, the lack of any indication of doping (n-type or p-type) of activation layer 73 suggests that activation layer 73 is "intrinsic" (i.e., not doped). (*Id.*) In fact, it was well-understood in the LED art that "[f]requently the active layer is left undoped." (*Id.*; Ex. 1017, 117.)[8] Second, Tanaka discloses that in some embodiments, the LED device is a gallium nitride (GaN) LED. (Ex. 1005 ¶¶[0002], [0014], [0030], [0068]; Ex. 1002 ¶61.) The '612

[8] *See* n.1.

patent admits that prior art GaN LEDs, like that described in Tanaka, "*comprise* a P-I-N junction device *having an intrinsic (I) layer* disposed between a N-type doped layer and a P-type doped layer." (Ex. 1001, 5:9-11; *see also id.,* 5:38-39 ("An active region makes up the interface of the GaN layers between the p-type and n-type regions.").) And this is the same configuration illustrated in Figure 7 of Tanaka where the activation layer 73 is interposed between the N-type semiconductor layer 72 and P-type semiconductor layer 74. (Ex. 1002 ¶62; Ex. 1005 ¶¶[0068], [0072], FIG. 7; *see also* Ex. 1010, 29:15-23 (describing a p-i-n semiconductor device including "p-doped and n-doped regions separated by an optically *active intrinsic region*."); Ex. 1011, 3:29-58, FIG. 1.)[9]

Therefore, Tanaka discloses or suggests a semiconductor LED including doped and intrinsic regions thereof, said semiconductor LED having opposing first and second LED surfaces, said first LED surface disposed on the first substrate surface, as claimed. (Ex. 1002 ¶63.)

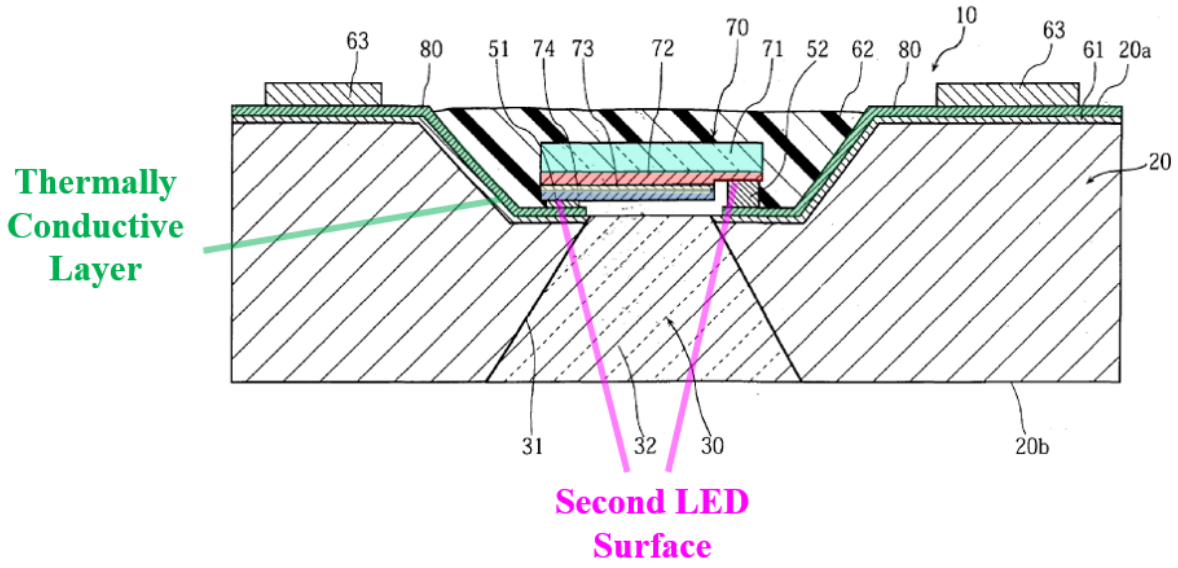
d) a thermally conductive layer disposed on the second LED surface of the semiconductor LED;

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶64-72.) For example, Tanaka discloses a wiring pattern 80 ("thermally conductive layer") disposed on the second LED surface of its semiconductor LED (which includes the

[9] *See* n.1.

N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74). (Ex. 1005 ¶[0072] ("[A]n N-side electrode 52 and a P-side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective *wiring pattern 80* via an anisotropic conductive layer or a conductive adhesive."), FIG. 7.)

FIG.7



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶64.)

A POSITA would have understood that the wiring pattern 80 is "disposed on" the second LED surface (the lower surface of P-type semiconductor layer 74) at least because it overlaps with the second LED surface in the vertical direction of Tanaka's Figure 7 embodiment (e.g., in the regions where the P-side electrode 51 and N-side electrode 51 are disposed). (Ex. 1005 ¶[0072] ("[A]n N-side electrode 52 and a P-

side electrode 51 are adjusted in height, and each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive."), FIG. 7; Ex. 1002 ¶65.) This is consistent with the teachings of the '612 patent, which describes an adhesive layer 41 (an example of the claimed thermally conductive layer) overlapping with the second LED surface of the GaN layers (an example of the claimed semiconductor LED) in the vertical direction of the Figure 5 embodiment (e.g., in the regions where the n-type pad 55 and p-type pad 56 are disposed). (Ex. 1002 ¶66.)

It would have been apparent to a POSITA that the wiring pattern 80 is a "thermally conductive" layer. (*Id.* ¶67.) A POSITA would have readily understood that such wiring is thermally conductive because it would conduct heat. (*Id.*) Indeed, the '612 patent confirms that a material is considered "thermally conductive" even at lower levels of thermal conductivity. (*See, e.g.*, Ex. 1001, 7:26-41 (generally describing the adhesive layer 41 as including "material optimized to provide [] heat conduction" and "[a]s a metric for suitable performance, heat conductions of 3 W/mK or more is sufficient"), 10:43-46 (describing the passivation layer 81 as another example of a thermally conductive layer "used to minimize the thermal

conductance of the package").)[10] Thus, the wiring pattern 80 is a thermally conductive layer, as claimed. (Ex. 1002 ¶67.)

Moreover, if Patent Owner argues or the Board finds that Tanaka does not necessarily disclose that its wiring pattern 80 is thermally conductive, it would have been obvious to configure Tanaka's wiring pattern 80 such that it is made of metal, which is thermally conductive. (*Id.* ¶68.) As explained below, using metal for the wiring pattern 80 would have been a mere design choice. (*Id*. ¶69.) For example, a POSITA would have understood that metal was a common material used for conductive wires and traces in semiconductor devices. (*Id*.) Indeed, such an understanding is supported by Tanaka's disclosure that electrodes 51, 52 are made of metal. (*See infra* Section IX.A.1.f.) Such a skilled person would have known that a wiring pattern like wiring pattern 80 in Tanaka can be made from a limited

[10] A POSITA would have known that a wire is typically used to determine thermal conductivity of a sample, by measuring the wire temperature over time after inserting the wire into the sample. (Ex. 1002 ¶67; Ex. 1013, 1:43-52 (describing the hot wire technique to measure thermal conductivity); *see also id.* generally, 1:6-20 (describing thermal conductivity measurement techniques), 2:1-20 (describing modified hot wire techniques for measuring thermal conductivity).) *See* n.1.

number of materials, where metals and metal alloys are the most common materials chosen for such conductive patterns. (Ex. 1002 ¶69; Ex. 1012, 5:60-6:5 (describing that conventional wire material used in semiconductor packaging includes metals and alloys).)[11] Metals are known to be thermally conductive. (Ex. 1002 ¶69; Ex. 1014, 44 ("Thus, like every other solid material, metals possess a component of heat conduction associated with the vibrations of the lattice called lattice (or phonon) thermal conductivity, κ_p.").)[12] As discussed above, the '612 patent confirms that a material may be "thermally conductive" regardless of the degree of its thermal conductivity. (*See, e.g.*, Ex. 1001, 7:26-41, 10:43-46.)

Accordingly, at a minimum, using metal for the wiring pattern 80 in Tanka would have been obvious to a POSITA in view of the teachings of Tanaka and the knowledge of POSITA. (Ex. 1002 ¶70.) For instance, as discussed above, given that Tanaka discloses that the wiring pattern 80 is connected to electrodes 51, 52 (Ex. 1005 ¶[0072]), a POSITA would have recognized that the wiring pattern is intended to provide an electrical connection to those electrodes and using metal for the wiring pattern 80 would have been a design choice that would accomplish that objective. (Ex. 1002 ¶70.)

[11] *See* n.1.

[12] *See* n.1.

Because metals and metal alloys were well-known materials for formation of conductive wires and traces in semiconductor devices, a POSITA would have understood how to implement the wiring pattern 80 using metal and would had a reasonable expectation of success. (*Id.* ¶71); *see Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) ("only a reasonable expectation of success, not a guarantee, is needed" in an obviousness analysis). Therefore, it would have been obvious to implement the wiring pattern 80 in Tanaka using metal such that it would have been a thermally conductive layer, as claimed. (Ex. 1002 ¶71.)

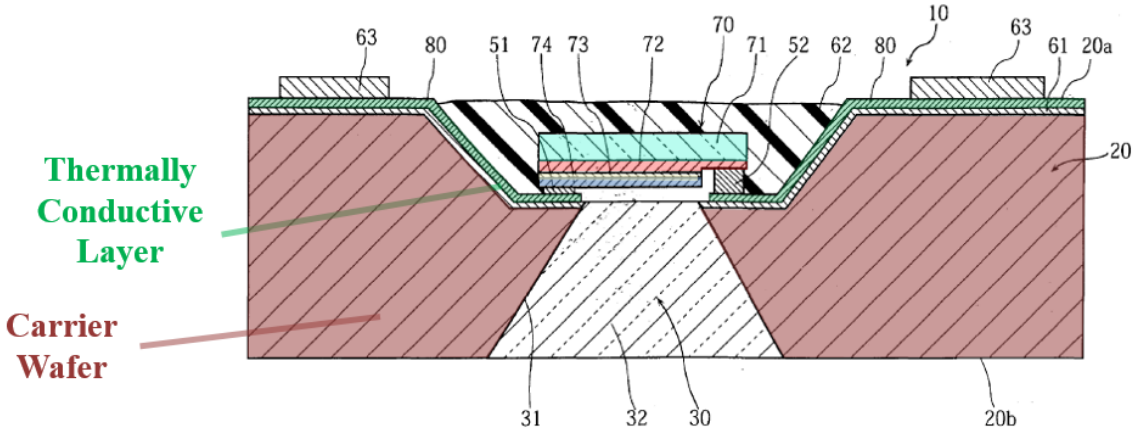
Therefore, Tanaka discloses or suggests a thermally conductive layer disposed on the second LED surface of the semiconductor LED, as claimed. (*Id.* ¶72.)

e) a carrier wafer disposed on the thermally conductive layer;

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶73-76.) For example, Tanaka discloses a monocrystal silicon substrate 20 ("carrier wafer") disposed on the wiring pattern 80 ("thermally conductive layer"). (Ex. 1005 ¶¶[0068]-[0072], FIG. 7.)[13]

[13] *See* n.4.

FIG.7



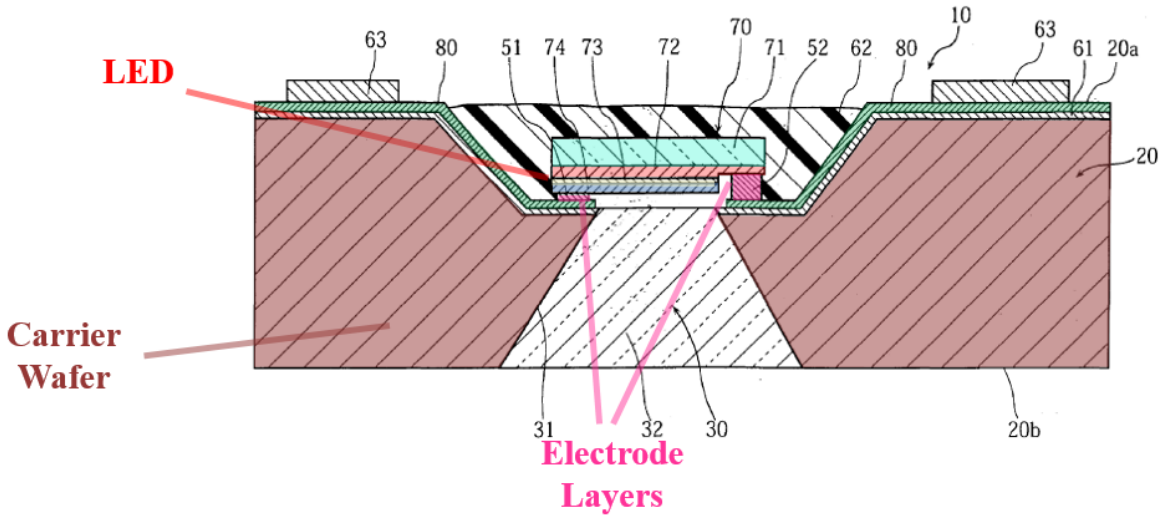
(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶73.)

A POSITA would have understood that the monocrystal *silicon* substrate 20 is "disposed on" the wiring pattern 80 at least because it overlaps with the wiring pattern 80 in the vertical direction of Tanaka's Figure 7 embodiment (e.g., in the regions where the insulating layer 61 are disposed). (Ex. 1005 ¶[0068] ("Each wiring pattern 80 has a lower surface formed with an insulating layer 61 made of e.g. silicon oxide film for insulation from the monocrystal *silicon* substrate 20."), FIG. 7; Ex. 1002 ¶74.) Similarly, the '612 patent describes a *silicon* wafer 31 (an example of the claimed carrier wafer) overlapping with an adhesive layer 41 (an example of the claimed thermally conductive layer) in the vertical direction of the Figure 5 embodiment (e.g., including the regions where the peripheral reflectors 34, 35 are disposed). (Ex. 1001, 6:45-65, 7:22-29, 8:60-63, FIGS. 3-5; Ex. 1002 ¶¶75-76.)

f) at least one optically reflective surface disposed between said carrier wafer and said semiconductor LED; and

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶77-81.) For example, Tanaka discloses electrode layers 51, 52 ("at least one optically reflective surface") disposed between the monocrystal silicon substrate 20 ("carrier wafer") and the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, the claimed "semiconductor LED"). While the embodiment shown in Figure 6 of Tanaka uses bonding wires to connect the N- and P-type semiconductor layers to the wiring pattern 80, the Figure 7 embodiment includes electrodes 51, 52 that are connected directly to the wiring pattern. (Ex. 1005 ¶¶[0068], [0072] ("[E]ach of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive layer or a conductive adhesive."); Ex. 1002 ¶78.)

FIG.7



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶77.)

Tanaka further discloses that its electrode layers 51 and 52 are made of metal, where such metal electrodes function as reflectors. (Ex. 1005 ¶¶[0061] ("The electrode layers 51, 52 are made of an Au- or Ag-based metal material for example."), [0054] ("Further, in the illustrated embodiment, the exposed portion of the GaN-based semiconductor laminate 40 at the first surface 20a side is completely covered with a metal electrode layer (the first electrode layer 51). *Consequently, the metal electrode layer serves as a reflector for efficiently reflecting light*, traveling from the activation layer 42 upward in FIG. 1A, toward the light guide 30."); *see also id.* ¶[0051] ("The first electrode layer 51 is formed . . . of an Au- or Ag-based

conductive metal optionally combined with etching.").)[14] Thus, a POSITA would have understood that Tanaka's electrode layers 51, 52 provide "at least one optically reflective surface," as claimed. (Ex. 1005 ¶¶[0051], [0054], [0061], [0072], Ex. 1002 ¶79.)

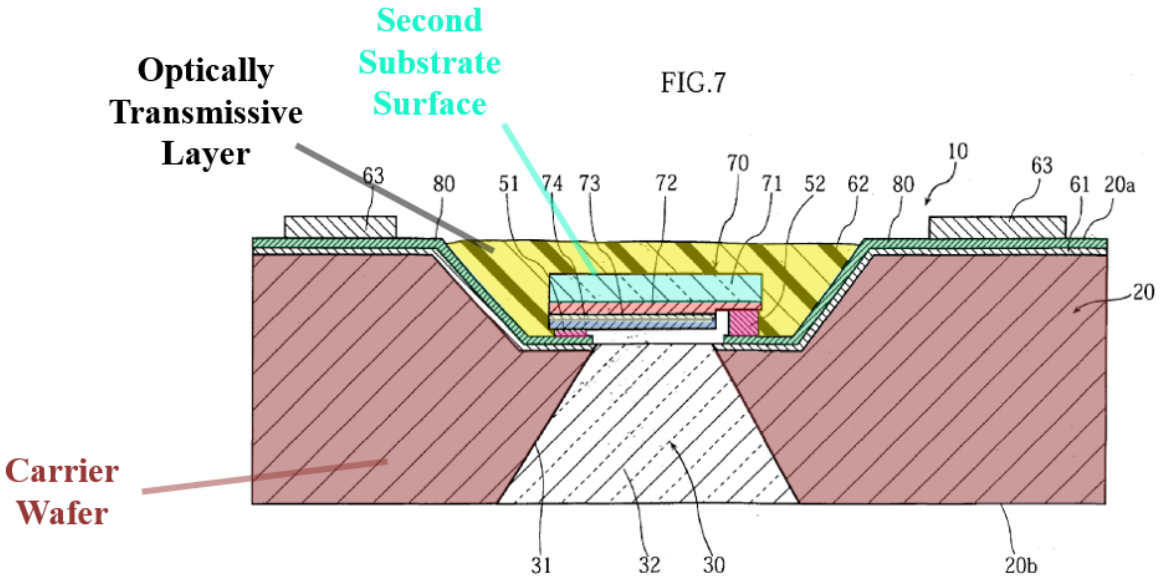
A POSITA would have recognized that, irrespective of the LED configuration in Tanaka's embodiments, a metal electrode would reflect light based on Tanaka's description of such electrodes and the knowledge of a POSITA. (Ex. 1002 ¶80.) Indeed, Tanaka's electrode layers 51, 52 are similar to the '612 patent's p-type pad 23, which, as the '612 patent describes, "can be fabricated to provide optical reflections." (Ex. 1001, 5:66-6:2.)

Accordingly, Tanaka discloses or suggests at least one optically reflective surface disposed between said carrier wafer and said semiconductor LED, as claimed. (Ex. 1002 ¶81.)

[14] While Tanaka provides details regarding its electrode layers 51, 52 with respect to some of its other figures, a POSITA would have understood that Tanaka's descriptions regarding the same component with common reference numbers in its figures are equally applicable to the Figure 7 embodiment. (Ex. 1002 n.18.)

g) a substantially optically transmissive layer disposed proximal to the second substrate surface,

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶82-86.) For example, Tanaka discloses a protective member 62 ("substantially optically transmissive layer") disposed proximal to the second substrate surface of sapphire substrate 71 ("substrate"). (*See also supra* Section IX.A.1.b.)



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶82.)

Tanaka's protective member 62 is a "substantially optically transmissive layer" at least because it is made of epoxy resin that allows for light transmission there through. (Ex. 1005 ¶[0069] ("The depression 21 on the first surface 20a is also filled with a *protective member 62 such as epoxy resin* to protect the chip 70 and the bonding wires 75."); Ex. 1002 ¶83.) Tanaka confirms that epoxy resin is a material

that allows for light transmission as it discloses that the light from the LED chip is emitted through the hole 31, which can be filled with epoxy resin 32 which serves as a protective member, i.e., the same material constituting protective member 62 providing the same protective function.

> The hole 31 is preferably filled with *a translucent resin 32 such as epoxy resin. The epoxy resin serves as a light guide 30 for guiding light emitted from the GaN-based semiconductor laminate 40 toward from the second surface 20b side while also serving as a protective member for the semiconductor laminate 40*. The epoxy resin may be contain a light scattering material such as fluorescent or metalic particles.

(Ex. 1005 ¶[0053]; *see also id.* ¶¶[0054], [0063], [0069].)

Thus, a POSITA would have understood that the epoxy resin in protective member 62 would have been "substantially optically transmissive," as claimed. (Ex. 1002 ¶¶84-86.) As shown above in annotated Figure 7, the protective member 62 is proximal to the second substrate surface of the sapphire substrate 71. (*Id.*)

> **h) wherein the carrier wafer and the thermally conductive layer define a relief to expose at least a portion of the second LED surface.**

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶¶87-99.) For example, Tanaka discloses that the monocrystal silicon substrate 20 ("carrier wafer") and the wiring pattern 80 ("thermally conductive layer") define an area ("relief") that includes the hole 31 and exposes at least a portion of the second LED surface of

the semiconductor LED (e.g., the bottom surface of the P-type semiconductor layer 74). (Ex. 1005 ¶¶[0049]-[0050], [0053], [0062]-[0064], [0069], [0072]; *see also supra* Sections IX.A.1.c, IX.A.1.e.)

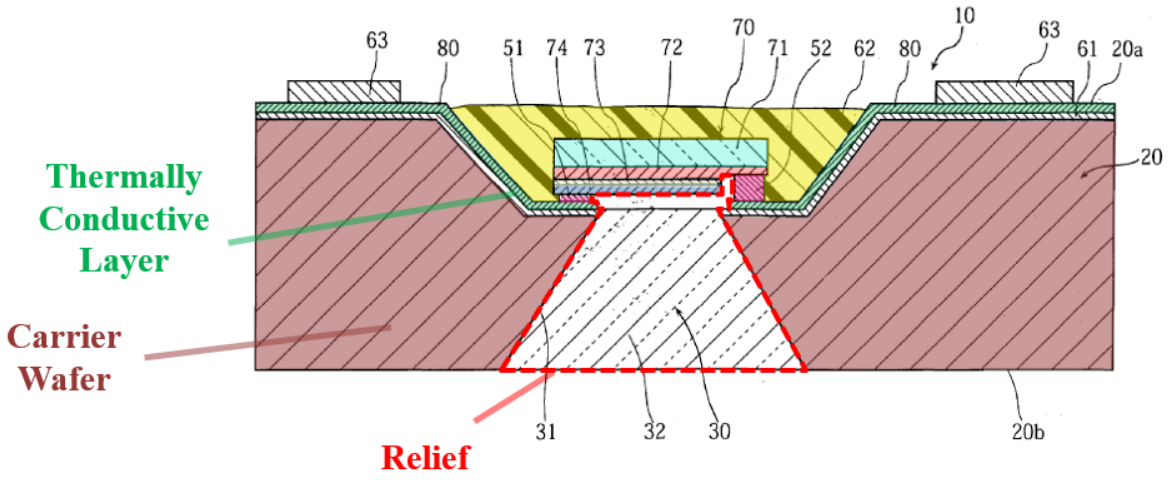
In particular, Tanaka discloses or suggests this limitation in at least two ways. (Ex. 1002 ¶87.) **First**, Tanaka discloses this limitation under Patent Owner's apparent understanding of this limitation to mean that the claimed relief may be filled with material such that a portion of the second LED surface is covered and not exposed to the environment. (*See* Ex. 1018, 18-20 (alleging that a filled region that does not expose the second LED surface to the environment meets the limitation), Ex. 1019, 18-19 (same), Ex. 1020, 17-19 (same).)

Tanaka similarly discloses an area that includes hole 31 that can be filled with epoxy resin 32. (Ex. 1005 ¶[0053] ("The hole 31 is preferably filled with a translucent resin 32 such as epoxy resin.").) Specifically, Tanaka discloses that "as shown in FIG. 3E, the monocrystal silicon substrate 20 is formed *with a hole 31 extending from the second surface 20 b to partially expose the bottom surface of the GaN-based semiconductor laminate 40*." (Ex. 1005 ¶[0062]; *see also id.* ¶¶[0049] ("The monocrystal silicon substrate 20 is formed with a thorough-hole 31 extending thicknesswise from the bottom of the depression 21 to the second surface 20 b."),

[0050], [0069], [0072]; Ex. 1002 ¶88.)[15] Similar to the semiconductor LED of the Figure 7 embodiment which includes the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (*see supra* Section IX.A.1.c), the semiconductor laminate 40 in Tanaka's Figure 3E embodiment includes an N-type semiconductor layer 41, an activation layer 42, and a P-type semiconductor layer 43 (Ex. 1005 ¶¶[0040], [0059]). Thus, at least under Patent Owner's apparent understanding of this claim term, when Tanaka describes forming a hole 31 to partially expose the bottom surface of its semiconductor laminate 40 with respect to Figure 3E (Ex. 1005 ¶[0062]), a POSITA would have understood that similarly, as shown in annotated Figure 7 below, the hole 31 partially exposes the bottom surface of the second LED surface of the semiconductor LED (e.g., the bottom surface of the P-type semiconductor layer 74). (Ex. 1002 ¶89.)

[15] *See* n.14; *see also* n.4.

FIG.7



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶89.)

Moreover, as shown in annotated Figure 7 above, the monocrystal silicon substrate 20 and the wiring pattern 80 define the area corresponding to the claimed "relief" because, for example, the area including the hole is formed by etching through the monocrystal silicon substrate 20 (Ex. 1005 ¶[0062]) and the width of the hole near the P-type semiconductor layer 74 is approximate to the gap between the wiring pattern 80. (Ex. 1002 ¶90.) Indeed, Tanaka's area that includes hole 31 and exposes the LED surface is similar to the '612 patent's description of its relief which it describes as a "via (hole)" or a "thermally conducting hole" in the Figure 5 embodiment, which are formed by etching through the silicon wafer 31 (example of the claimed carrier wafer). (Ex. 1001, 8:60-9:28, FIG. 5; Ex. 1002 ¶91.)

Therefore, Tanaka discloses this limitation under Patent Owner's apparent understanding of this limitation where the claimed "relief" may be filled with

material such that a portion of the second LED surface is covered and not exposed to the environment. (Ex. 1018, 18-20, Ex. 1019, 18-19, Ex. 1020, 17-19.)

Second, Tanaka also discloses or suggests this limitation where the relief is free of material such that a portion of the second LED surface is left uncovered and exposed to the environment, as shown in Figure 5 of the '612 patent. (Ex. 1001, 9:1-28, FIG. 5 (showing a thermally conducting hole 53 exposing a surface of the GaN LED layer to the environment); Ex. 1002 ¶¶92-93.) For instance, Tanaka discloses that "[a]ccording to a preferred embodiment the light guide comprises a hole penetrating the monocrystal silicon substrate thicknesswise, and the GaN-based semiconductor laminate includes a lowermost layer whose surface includes a portion substantially exposed to the second surface." (Ex. 1005 ¶[0015].) Tanaka further discloses that "the hole *may be preferably filled* with translucent resin." (*Id.* ¶[0016]; *see also id*. ¶[0053] (disclosing that the "hole 31 is *preferably* filled with a translucent resin.").) Because Tanaka discloses that the hole 31 *may be* filled, Tanaka discloses, or at least suggests, that in some embodiments, the hole 31 is left unfilled. (Ex. 1002 ¶94.) Such an understanding is supported by claims 2 and 3 of Tanaka. Claim 2 recites such a hole where the surface of the lowermost layer of the semiconductor laminate is exposed, whereas claim 3, which depends from claim 2, states that "the hole is filled with translucent resin." (Ex. 1005, claims 2, 3.) Indeed, a POSITA would have understood that in some applications, the extra protection or

possible light scattering feature of the resin 32 is unnecessary. (Ex. 1002 ¶95.) In such applications, such a POSITA would have known not to include resin 32 in the hole 31 in order to simplify the manufacturing of the LED device and reduce costs. (*Id*.)

The understanding of a POSITA that unfilled hole on the backside of such a light emitting device can be used to allow efficient light emission is further supported by Weeks (Ex. 1006).[16] (Ex. 1002 ¶96.) Weeks explicitly discloses forming a via (hole) that exposes the surface of an LED, where the via "is free of any material formed therein." (Ex. 1006, 8:57-58.) Weeks, like Tanaka, discloses GaN LED structures with a light emitting active region and a hole or via is provided on the other side in order to allow the generated light to be emitted from the LED structure. (Ex. 1006, 8:47-67, 12:50-56, 13:35-58, 14:60-66, 15:50-60, FIGs. 14, 17.) For example, as shown in annotated Figure 14 of Weeks below, light generated in the active region 97 exits the device through the via 24.

[16] *See* n.1.

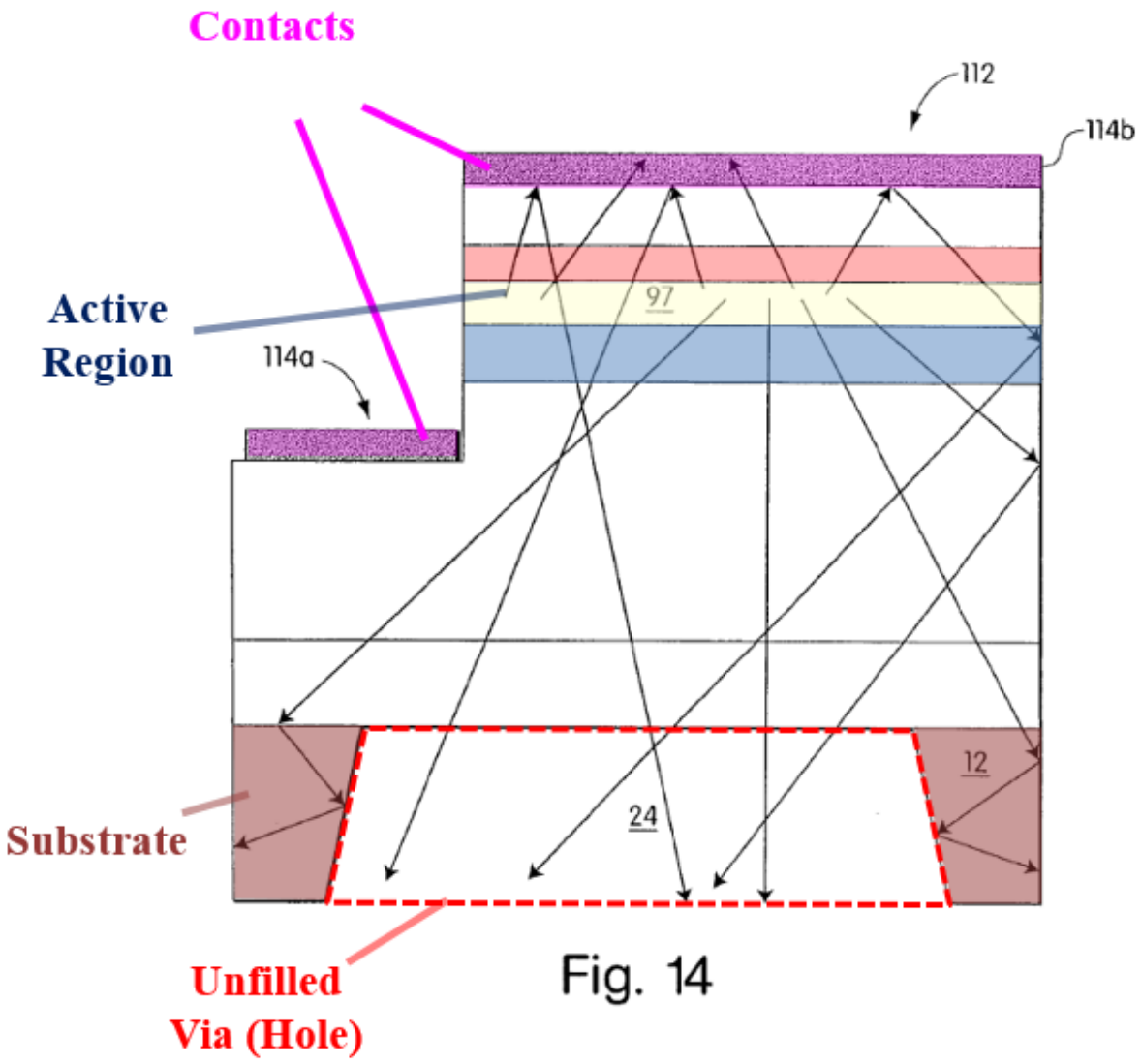


Fig. 14

(Ex. 1006, FIG. 14 (annotated); *see also id.*, FIG. 1; Ex. 1002 ¶96.)

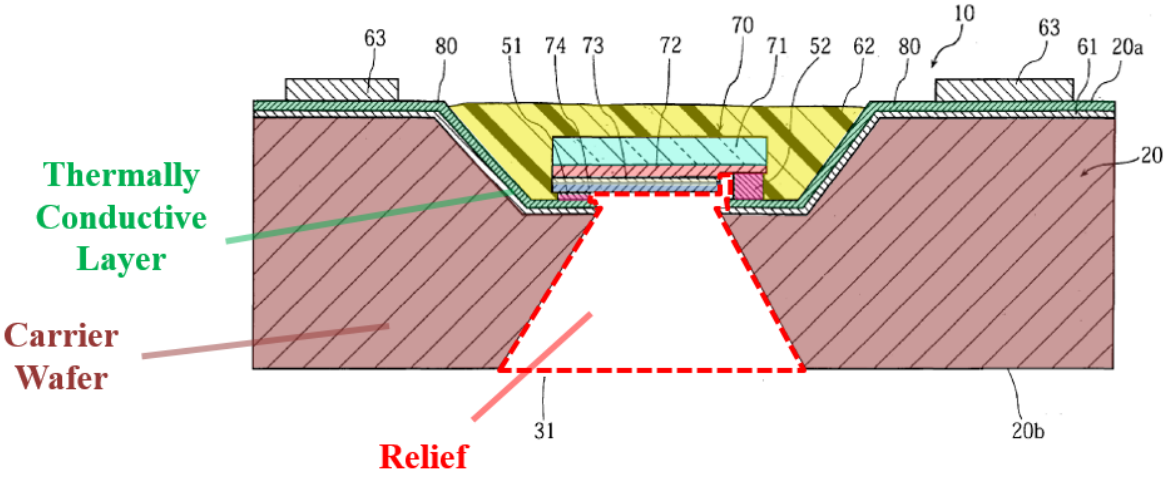
Weeks discloses that in LED embodiments like that shown in Figure 14 above, the via or hole can be left unfilled and free of material in order to expose the gallium nitride material device to the outside, which can enhance the extraction of light from the device:

> In certain embodiments, and as described further below in connection with FIGS. 9-11, 13-14, and 16-18, it may be preferable for via 24 to be free of a contact. That is, a contact is not formed within the via. In some cases, the via may be free of a contact but may have one or more other regions(s) or layer(s) formed therein (e.g., a reflective layer), as described further below. In some cases, the *via may be free of any material formed therein. When free of material, the via may function as a window that exposes internal layers of the device* (e.g. a transition layer 15 or gallium nitride material device region 14) *to the outside. This exposure may enhance the extraction of light from the device which can be particularly useful in light-emitting devices such as LEDs* or lasers. In embodiments in which via 24 is free of an electrical contact, it should be understood that contacts are formed on other parts of the device including other (non-via) areas of backside 22 or areas of topside 18.

(Ex. 1006, 8:51-67; Ex. 1002 ¶97.)

Therefore, Weeks confirms the understanding of a POSITA with respect to Tanaka disclosing that the hole 31 can either be filled or left unfilled. A non-limiting example of Tanaka's light emitting element is illustrated in modified Figure 7 below, where the hole 31 is left unfilled. The unfilled hole constitutes a "relief" defined by the carrier wafer and thermally conductive layer that exposes portions of the n- and p-doped layers to the outside.

FIG.7



(Ex. 1005, FIG. 7 (modified, annotated); Ex. 1002 ¶98.)

Therefore, Tanaka discloses or suggests this limitation where the relief is free of material such that a portion of the second LED surface is left uncovered and exposed to the environment, as shown in Figure 5 of the '612 patent. (Ex. 1002 ¶98.)

Accordingly, Tanaka discloses or suggests that the carrier wafer and the thermally conductive layer define a relief to expose at least a portion of the second LED surface, as claimed. (Ex. 1002 ¶99.)

2. Claim 2

a) The light emitting device of claim 1, said at least one optically reflective surface comprising metal.

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶100.) For example, as noted above with respect to claim limitation 1(f), Tanaka discloses that its

electrode layers 51, 52 ("at least one optically reflective surface") include metal. (*See supra* Section IX.A.1.f; Ex. 1005 ¶¶[0061] ("The electrode layers 51, 52 are made of an Au- or Ag-based *metal* material for example."), [0054]; *see also id.* ¶[0051] ("The first electrode layer 51 is formed by vacuum spattering [*sic*, sputtering] or vapor deposition of an Au- or Ag-based conductive *metal* optionally combined with etching.").) Thus, Tanaka discloses or suggests that the at least one optically reflective surface includes metal. (Ex. 1002 ¶100.)

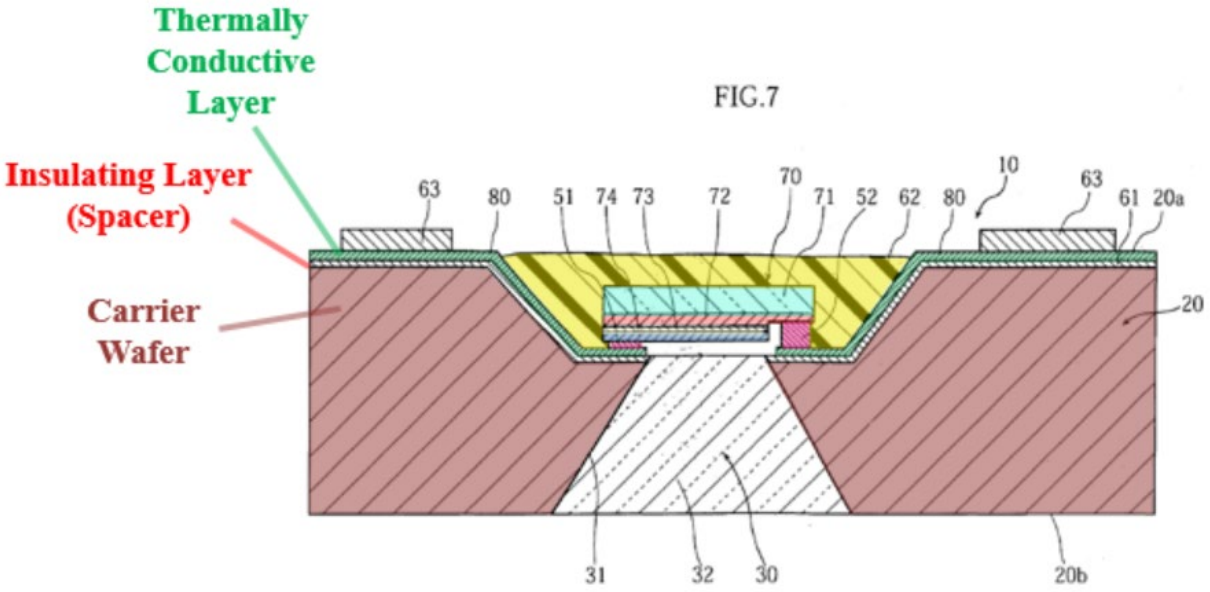
3. Claim 8

a) The light emitting device of claim 1, further comprising at least one spacer attached to said carrier wafer; whereby, said at least one optically reflective surface is affixed thereto.[17]

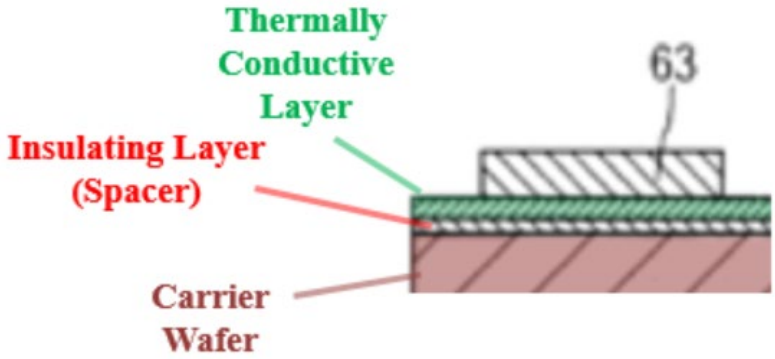
Tanaka discloses or suggests claim 8. (Ex. 1002 ¶¶101-108.) For example, Tanaka discloses an insulating layer 61 ("at least one spacer") attached to the monocrystal silicon substrate 20 ("carrier wafer"), whereby, at least one of the electrodes 51, 52 ("said at least one optically reflective surface") is affixed thereto, as discussed below. (Ex. 1005 ¶[0072]; *see supra* Sections IX.A.1.e-f.) The insulating layer 61 ("spacer") is highlighted in annotated Figure 7 and an enlarged

[17] While Petitioner addresses the "at least one spacer" feature recited in claim 8, Petitioner does not concede that the '612 patent provides adequate disclosure of the claimed feature in compliance with 35 U.S.C. § 112.

excerpt of Figure 7 of Tanaka below.



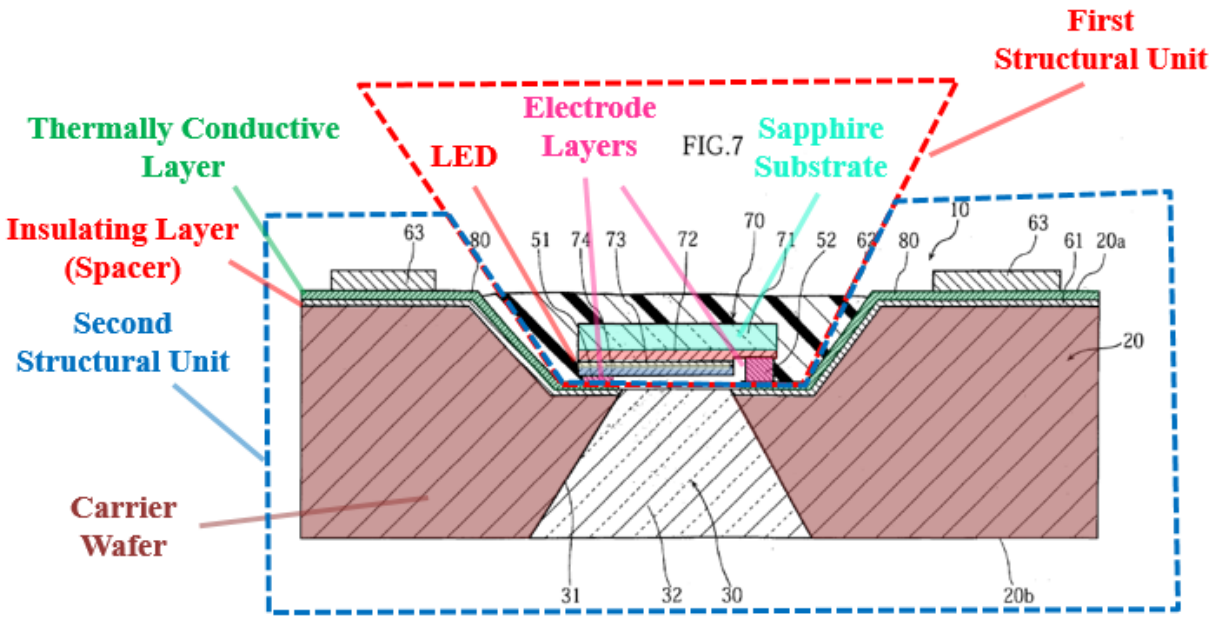
(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶101.)



(Ex. 1005, FIG. 7 (excerpt, annotated); Ex. 1002 ¶101.)

In particular, Tanaka discloses with respect to its Figure 7 embodiment discussed above with respect to claim 1 that "each of the electrodes 51, 52 is connected directly to a respective wiring pattern 80 via an anisotropic conductive

layer or a conductive adhesive." (Ex. 1005 ¶[0072], FIG. 7.) A POSITA would have understood that in Tanaka's LED device, at least the sapphire substrate 71, semiconductor LED (N-type semiconductor layer 72, activation layer 73, P-type semiconductor layer 74), and electrodes 51, 52 constitute a first structural unit (the blue-color light-emitting diode chip 70) while at least the wiring pattern 80, monocrystal silicon substrate 20, and insulating layer 61 constitute a second structural unit. (*Id.*; Ex. 1002 ¶102.) The first and second structural units are shown in annotated Figure 7 below.



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶102.)

With respect to the first structural unit, Tanaka discloses:

> The blue-color light-emitting diode chip 70 *fabricated* in the conventional manner has a sapphire substrate 71 including an upper surface successively formed with an N-type semiconductor layer 72 (GaN layer or AlGaN layer), an activation layer 73 (InGaN layer), and a P-type semiconductor layer 74 (GaN layer or AlGaN layer). *The N-type semiconductor layer 72 has an exposed portion formed with an N-side electrode 52, whereas the P-type semiconductor layer 74 includes a surface formed with a P-side electrode 51.*

(Ex. 1005 ¶[0068].) Thus, a POSITA would have understood that the *fabricated* blue-color light-emitting diode chip 70 includes each of the sapphire substrate 71, N-type semiconductor layer 72, activation layer 73, P-type semiconductor layer 74, and electrodes 51, 52 such that they constitute a first structural unit in Tanaka's LED device. (Ex. 1002 ¶103.)

Similarly, with respect to the second structural unit, Tanaka discloses:

> Each of the N-side electrode 52 and the P-side electrode 51 is connected, by wire bonding, to a corresponding *wiring pattern 80 arranged on the first surface 20 a* [of monocrystal silicon substrate 20]. *Wiring patterns 80* corresponding to the N-side electrode 52 and the P-side electrode 54 *extend to suitable portions on the first surface 20 a* where bumps 63 are formed. *Each wiring pattern 80 has a lower surface formed with an insulating layer 61 made of e.g. silicon oxide film for insulation from the monocrystal silicon substrate 20.*

(Ex. 1005 ¶[0068]; *see also id.* ¶[0067].) A POSITA would have understood that because wiring pattern 80 is "arranged on" the surface 20a of the silicon substrate 20 ("carrier wafer") and "extends to suitable portions on the first surface 20a," and the wiring pattern is further "formed with" an insulating layer 61, the wiring pattern 80, silicon substrate 20, and insulating layer 61 constitute a second structural unit in Tanaka's LED device. (Ex. 1002 ¶104.) This understanding is further corroborated by Tanaka's disclosure that given the substrate 20 is made of monocrystal silicon, a "wafer process maybe performed on the first surface 20a of the substrate 20 to form another element or a set of elements 90" such that the substrate 20 can include elements such as "a current regulating drive circuit or a logic circuit as a part of an IC-built-in semiconductor light-emitting element, or [] a discrete element such as a diode, or sensor or the like." (Ex. 1005 ¶[0055], FIG. 1B; *see also id.* ¶[0067] (describing with respect to the Figure 6 embodiment that "similarly to the first embodiment [including FIG. 1B], the monocrystal silicon substrate 20 *may be formed integrally* with a current regulating drive circuit or a logic circuit by wafer process.").)[18] A POSITA would have understood that if discrete elements are formed on the first surface 20a of the substrate 20, then a wiring pattern such as

[18] *See* n.4.

wiring pattern 80 connecting such discrete elements would have been included on the first surface 20 of the substrate 20. (Ex. 1002 ¶105.)

Tanaka's insulating layer 61 ("at least one spacer") is attached to the monocrystal silicon substrate 20 ("carrier wafer"), because Tanaka describes that the "wiring pattern 80 has a lower surface formed with an insulating layer 61 . . . for insulation from the monocrystal silicon substrate 20." (Ex. 1005 ¶[0068].) A POSITA would have understood that the insulating layer 61 is a "spacer" as it provides spacing between the monocrystal silicon substrate 20 and the electrodes 51, 52. (Ex. 1002 ¶106.)

Moreover, a POSITA would have understood that when Tanaka discloses that an anisotropic conductive layer or a conductive adhesive is used to bond electrodes 51, 52 to the wiring pattern 80 (Ex. 1005 ¶[0072]), then the electrodes 51, 52 ("said at least one optically reflective surface"), which are part of the first structural unit, are "affixed to" the insulating layer 61 ("at least one spacer"), which is part of the second structural unit (and is formed at the lower surface of wiring pattern 80). (Ex. 1002 ¶107.)

Therefore, Tanaka discloses at least one spacer attached to said carrier wafer; whereby, said at least one optically reflective surface is affixed thereto, as claimed. (Ex. 1002 ¶108.)

4. Claim 9

a) The light emitting device of claim 1, said thermally conductive layer comprises metal.

Tanaka discloses or suggests this limitation. (Ex. 1002 ¶109.) For example, as noted above, it would have been obvious to configure Tanaka's wiring pattern 80 ("thermally conductive layer") such that it is made of metal, as claimed. (*See supra* Section IX.A.1.d.) Thus, Tanaka suggests that the thermally conductive layer comprises metal. (Ex. 1002 ¶109.)

B. Ground 2: The Combination of Tanaka and Weeks Renders Obvious Claim 3

1. Claim 3

a) The light emitting device of claim 1, said at least one optically reflective surface comprising a dielectric stack.

Tanaka in combination with Weeks discloses or suggests claim 3. (Ex. 1002 ¶¶110-120.) For example, Tanaka discloses that its electrode layers 51, 52 ("at least one optically reflective surface") may be made of metal. (*See supra* Sections IX.A.1.f, IX.A.2; Ex. 1005 ¶[0061] ("The electrode layers 51, 52 are made of an Au- or Ag-based *metal* material *for example*.").)

Tanaka is silent regarding its electrode layers 51, 52 including a dielectric stack. (Ex. 1002 ¶112.) However, Weeks discloses a Distributed Bragg Reflector (DBR) with dielectric layers, and as discussed below, it would have been obvious to include such a Distributed Bragg Reflector in an LED device like that depicted in

Figure 7 of Tanaka in order to further improve reflection of light in a desired direction. (*Id.*)

Weeks, like Tanaka, relates to fabrication of LED devices. (Ex. 1006, Abstract, 1:15-49, 8:51-67; Ex. 1002 ¶113, 44-45.) For example, as noted above, Weeks discloses GaN LED structures with a light emitting active region and a hole or via is provided on the other side in order to allow the generated light to emitted from the LED structure. (Ex. 1006, 8:47-67, 12:50-56, 13:35-58, 14:60-66, 15:50-60, FIGs. 14, 17, 20.) Both Tanaka and Weeks are also concerned with improving the reflection of light in LED devices to improve light efficiency. (Ex. 1005 ¶¶[0054] ("[T]he metal electrode layer serves as a reflector for efficiently reflecting light, traveling from the activation layer 42 upward in FIG. 1A, toward the light guide 30, which also results in significant improvement in light-emitting efficiency."), [0070], [0072]; Ex. 1006, 7:23-41, 8:33-67, 10:8-46, 16:42-17:11.) Thus, a POSITA would have been motivated to consider Weeks' teachings when implementing reflective surfaces like those disclosed with respect to Tanaka's Figure 7 embodiment. (Ex. 1002 ¶113; Ex. 1005 ¶[0072].)

In this regard, Weeks discloses with respect to its Figure 20 embodiment an LED 136 that includes a reflector with two reflection regions: a topside contact 114b (first reflector region) and a Distributed Bragg Reflector (DBR) 120b (second reflector region).

FIG. 20 illustrates a light emitting device 136 that has been flipped during use so that backside 22 faces upward and topside 18 faces downward. *Topside contact 114b also functions as a reflector region* that can upwardly reflect light generated in region 97. The device also includes *a second reflector region 120b which may be a Distributed Bragg Reflector (DBR) that includes a number of semiconductor or dielectric layers*.

(Ex. 1006, 16:62-17:2.)

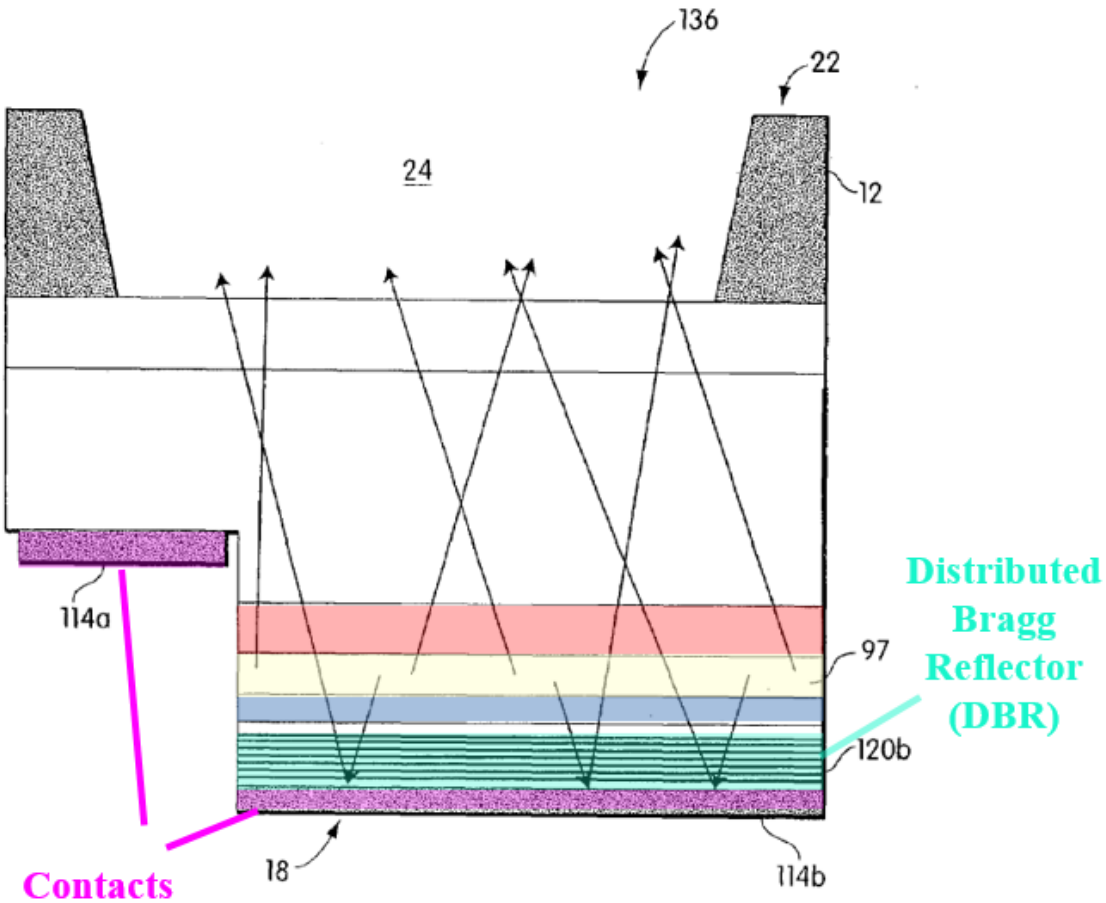
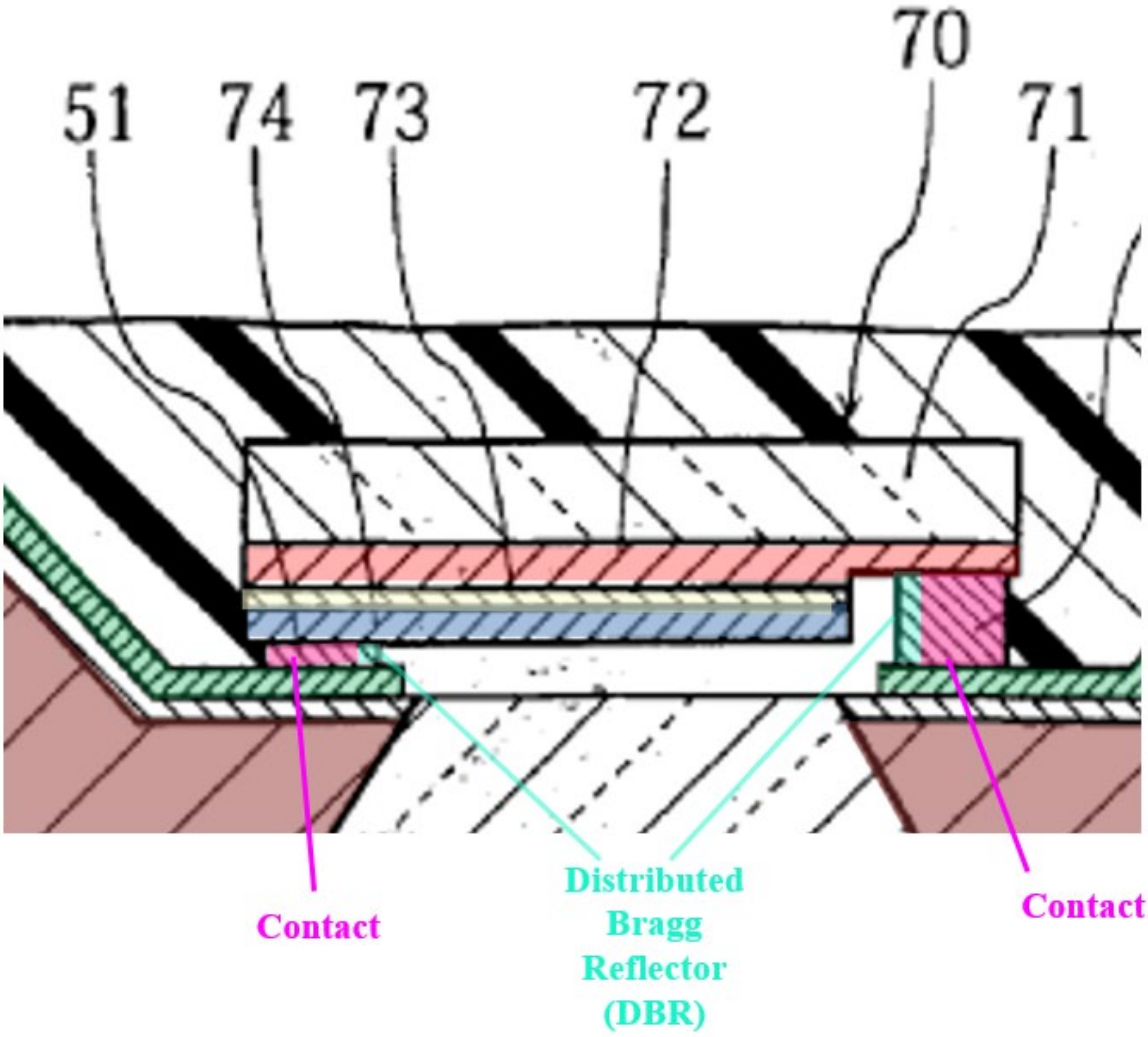


Fig. 20

(Ex. 1006, FIG. 20 (annotated); Ex. 1002 ¶114.)

Since the DBR 120b includes a number of dielectric layers (Ex. 1005 ¶[0072]), a POSITA would have understood that the DBR 120b discloses an optically reflective surface including a dielectric stack, as claimed. (Ex. 1002 ¶115.)

As discussed below, it would have been obvious to include a reflective surface like Weeks' DBR 120b with the electrodes 51, 52 in Tanaka's LED device to improve light reflection in the desired direction, and thereby improve device performance. (*Id.* ¶116.) A POSITA would have been motivated to include such a reflective surface to provide additional layers of protection from light leaking into undesired portions of the device. (*Id.*) For example, a POSITA would have been motivated to include a DBR like the one disclosed in Weeks on the inner sides of electrodes 51 as shown in the enlarged annotated excerpt of Figure 7 below, so that the DBR could reflect light towards the desired direction. (*Id.*.)



(Ex. 1005, FIG. 7 (excerpt, annotated); Ex. 1002 ¶116.)

Moreover, any light not reflected by the DBR could then be reflected by the surface of the electrodes 51, 52, thus providing a device with improved light reflection capability. (Ex. 1002 ¶117.) That is, the surfaces of electrodes 51, 52 and the surfaces of the DBRs on the inner sides of these electrodes would serve as the claimed at least one optically reflective surface. (*Id.*) Indeed, such a configuration would be similar to the configuration disclosed by Weeks' Figure 20 embodiment,

where the DBR 120b provides a first layer for light reflection and the contact 114b provides a second layer of light reflection such that any light that is not reflected by DBR 120b is reflected by the contact 114b. (Ex. 1006, 16:62-17:11, FIG. 20.) Weeks specifically recognizes the advantage of such a configuration: "Device 136 includes two reflector regions to increase the ability of the device to reflect generated light in the desired direction." (*Id.*, 17:2-4, FIG. 20.) Moreover, a POSITA would have understood that the inclusion of a DBR would provide additional advantages as DBRs can be designed to provide custom reflectances at particular wavelengths, which can be beneficial in certain LED applications. (Ex. 1002 ¶117 (citing Ex. 1017, 170-181.).)

Therefore, a POSITA would have been motivated in light of Weeks' teachings to use a DBR like DBR 120b with multiple dielectric layers as an optically reflective surface in Tanaka's semiconductor LED device (as discussed above) to enhance light-emission efficiency and improve device performance. (Ex. 1002 ¶118; Ex. 1005 ¶¶[0054], [0070], [0072]; Ex. 1006, 7:23-41, 8:33-67, 10:8-46, 16:42-17:11.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007).

A POSITA facing the wide range of needs created by developments in the technical field of Tanaka and Weeks would have appreciated the benefits of using a

DBR like Weeks' DBR 120b with Tanaka's LED device such as, e.g., minimizing the amount of light leaking into undesired portions of the LED device by providing multiple reflective surfaces to direct the generated light in the desired direction. (Ex. 1002 ¶119.) A POSITA would have been skilled and knowledgeable about configuring Tanaka's LED device to include a DBR like DBR 120b, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. (*Id*.) Thus, a POSITA would have had a reasonable expectation of success in the above modification. (*Id*.); *see Pfizer, Inc.*, 480 F.3d at 1364.

Accordingly, the combination of Tanaka with Weeks discloses or suggests claim 3. (Ex. 1002 ¶120.)

C. Ground 3: The Combination of Tanaka and Chitnis Renders Obvious Claims 4-7

1. Claim 4

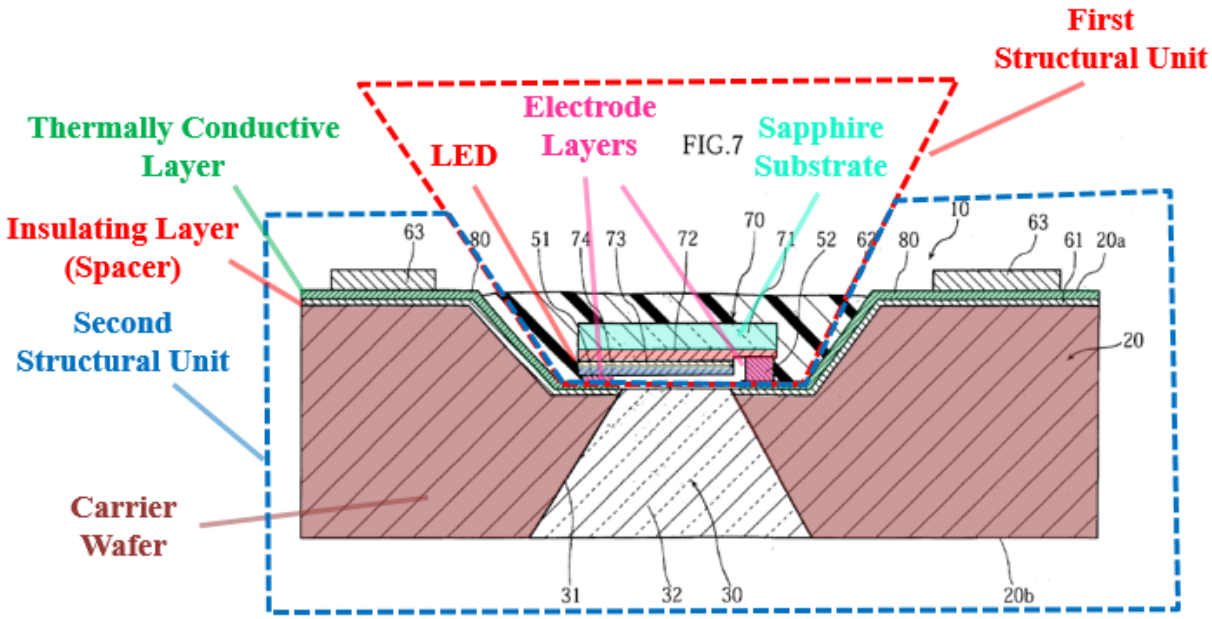
a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of high thermal conductivity.[19]

Tanaka in combination with Chitnis discloses or suggests claim 4. (Ex. 1002 ¶¶121-139.) For example, Tanaka discloses that the blue-color light-emitting diode chip 70 with N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, the claimed "semiconductor LED") is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with an adhesive ("adhesive material"). (*Id.* ¶122; *see also supra* Sections IX.A.1.c, IX.A.1.e.) As discussed below, it would have been obvious for a POSITA to use an adhesive with the property of high thermal conductivity. (Ex. 1002 ¶122.)

For example, as discussed above with respect to claim 8, a POSITA would have understood that in Tanaka's LED device, at least the sapphire substrate 71, semiconductor LED (N-type semiconductor layer 72, activation layer 73, P-type

[19] While Petitioner addresses the "high thermal conductivity" feature recited in claim 4, Petitioner does not concede that the '612 patent provides adequate disclosure of the claimed feature in compliance with 35 U.S.C. § 112.

semiconductor layer 74), and electrodes 51, 52 constitute a first structural unit (the blue-color light-emitting diode chip 70) while at least the wiring pattern 80, monocrystal silicon substrate 20, and insulating layer 61 constitute a second structural unit. (*See supra* Section IX.A.3.) The first and second structural units are shown in annotated Figure 7 below.



(Ex. 1005, FIG. 7 (annotated); Ex. 1002 ¶123.)

As such, a POSITA would have understood that when Tanaka discloses that a conductive adhesive is used to bond electrodes 51, 52 to the wiring pattern 80, then the N-type semiconductor layer 72, activation layer 73, and P-type semiconductor layer 74 (collectively, "semiconductor LED"), which are part of the first structural

unit, would have been affixed by the conductive adhesive to monocrystal silicon substrate 20 ("carrier wafer"), which is part of the second structural unit. (Ex. 1002 ¶124.) Therefore, Tanaka discloses that the semiconductor LED is affixed to the carrier wafer with an adhesive material, as claimed. (*Id.* ¶125.)

Tanaka is silent regarding its conductive adhesive having the property of high thermal conductivity, as claimed. However, as discussed below, it would have been obvious to use a conductive adhesive having the property of high thermal conductivity like that described by Chitnis with an LED device like that depicted in Figure 7 of Tanaka, in order to bond an LED chip to a wafer like the aforementioned bonding of Tanaka's blue-color light-emitting diode chip 70 (including the claimed "semiconductor LED") with the monocrystal silicon substrate 20 ("carrier wafer"). (*Id.*¶126.)

Chitnis, like Tanaka, relates to fabrication of LED devices. (Ex. 1007 ¶[0004].) By way of its background, Chitnis discloses well-known wafer-level bonding techniques used during LED device fabrication:

> Recent developments in wafer-bonding technology have provided the means to integrate different materials into semiconductor devices. Wafer bonding is a semiconductor manufacturing process in which two semiconductor wafers are bonded to form a single substrate having specific properties. A variety of bonding methods can be used to create integrated

> electronics, and to combine multifunctional components onto a single die.

(Ex. 1007 ¶[0010]; *see also id.* ¶[0008]; Ex. 1002 ¶127.)

A POSITA would have understood that the wafer-level bonding techniques described by Chitnis are directed to bonding similar structural units as those discussed above with respect to Tanaka. (Ex. 1002 ¶128.) For example, as noted above, Tanaka teaches bonding a first structural unit, which includes the LED and sapphire substrate, with a second structural unit, which includes the wiring pattern and silicon substrate. (*See supra* Section IX.A.3.) Similarly, Chitnis is directed to bonding an LED wafer 10 shown in Figures 1A-1C (including LED grown substrate 12, n- and p-type layers 16, 18, and active region 14) with a submount 40 shown in Figure 2 (including a submount wafer 42 and a dielectric material 44). (Ex. 1007 ¶[0037], [0040], [0045].) Thus, a POSITA would have been motivated to consider Chitnis' teachings when implementing the bonding process disclosed with respect to Tanaka's Figure 7 embodiment. (Ex. 1002 ¶129; Ex. 1005 ¶[0072].)

Chitnis further describes that "[t]he choice of wafer bonding process used to fabricate a device is dependent upon the type of device, particularly the components and materials used to build the device." (Ex. 1007 ¶[0011].) In this regard, Chitnis discloses that "eutectic wafer bonding is based on the use of bonding materials that form a eutectic alloy at specific temperature conditions, and *eutectic bonding media*

such as Au-Si, Au-Sn or Pd-Si are widely used." (*Id.*; *see also id.* ("For chip scale packages (e.g. flip chips), it would be advantageous to create devices at the wafer level with both electrical contacts on the bottom of the chip," and that "this would require *electrically and thermally conducting bond medium* selectively deposited to avoid electrical shorting."); Ex. 1002 ¶130.)

A POSITA would have understood that the type of bonding media disclosed by Chitnis like Au-Si (gold-silicon) or Au-Sn (gold-tin) have the property of high thermal conductivity. (Ex. 1002 ¶131.) This is because gold, silicon, and tin are all known to have high thermal conductivity. (Ex. 1014, 23 ("*High-thermal-conductivity materials like . . . silicon have been extensively studied* in part because of their potential applications in thermal management of electronics."), 50 (Table 1 showing thermal conductivity of gold is 318 Watts/meter-Kelvin and tin is 64 W/m-K), 129 (Table 1 showing thermal conductivity of silicon is 124 W/m-K).)[20] A POSITA would have understood that the thermal conductivity of Au-Si or Au-Sn would be similarly high. (Ex. 1002 ¶132.)

While the '612 patent does not provide adequate disclosure regarding the term "high thermal conductivity," it discloses with reference to its adhesive layer 41 that it can include "material optimized to provide [] heat conduction" and that "[a]s a

[20] *See* n.1.

metric for suitable performance, heat conductions of 3 W/mK or more is sufficient." (Ex. 1001, 7:26-41.) Thus, a POSITA would have understood that conductive adhesives such as Au-Si or Au-Sn as disclosed by Chitnis would have had the property of high thermal conductivity, as claimed. And as discussed below, it would have been obvious to use such a conductive adhesive to bond Tanaka's semiconductor LED with the monocrystal silicon substrate 20. (Ex. 1002 ¶133.)

A POSITA would have been motivated in light of Chitnis to use a conductive adhesive with the property of high thermal conductivity in Tanaka's semiconductor device (as discussed above for claim 1) so that the bond between the first structural unit (including the semiconductor LED) and the second structural unit (including the monocrystal silicon substrate 20) could withstand heat and improve device performance. (*Id.* ¶134.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*); *KSR*, 550 U.S. at 416-18.

A POSITA would have recognized that Tanaka and Chitnis disclose features in a similar technological field. (Ex. 1002 ¶135.) For example, as discussed above, both Tanaka and Chitnis relate to techniques for fabricating semiconductor LED devices. (*Compare* Ex. 1005, Abstract, ¶¶[0002], [0004], [0014], [0047] *with* Ex. 1007, Abstract, ¶¶[0004]-[0006], [0008], [0010]-[0011]; Ex. 1002 ¶135, 46-48.) Accordingly, a POSITA would have had reason to consider the teachings of Chitnis

when fabricating an LED device as described in Tanaka given Chitnis discloses the details regarding bonding media for affixing various structures in an LED device like the structures to be bonded in Tanaka. (Ex. 1002 ¶135.)

A POSITA would have further recognized that implementing Chitnis' teachings regarding an adhesive such as Au-Si or Au-Sn with the property of high thermal conductivity in Tanaka would have improved device performance by, e.g., allowing for heat generated by the LED to conduct through the adhesive and dissipate in the wiring pattern and attached carrier substrate. (*Id.* ¶136.) Such heat dissipation is desirable to avoid damage to the LED device and to promote proper functionality. (*Id*.) A POSITA facing the wide range of needs created by developments in the technical field of Tanaka and Chitnis would have appreciated the benefits of using a conductive adhesive such as Au-Si or Au-Sn as described in Chitnis with Tanaka's LED device such as, e.g., ensuring electrical connection between the wiring pattern 80 and electrodes 51, 52. (*Id*.) Indeed, as noted above, Chitnis discloses that "[f]or chip scale packages (e.g. flip chips), it would be advantageous to create devices at the wafer level with both electrical contacts on the bottom of the chip," and that "[t]his would require *electrically and thermally conducting bond medium* selectively deposited to avoid electrical shorting." (Ex. 1007 ¶[0011].) A POSITA would have similarly deposited such a bond medium in

Tanaka's device selectively on wiring pattern 80. (Ex. 1002 ¶137; Ex. 1005 ¶[0072].)

A POSITA would have been skilled and knowledgeable about configuring Tanaka's LED device to include a conductive adhesive such as Au-Si or Au-Sn, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. (Ex. 1002 ¶138.) Thus, a POSITA would have had a reasonable expectation of success in using such a thermally conductive adhesive in an LED device like that disclosed by Tanaka. (*Id*.); *see Pfizer, Inc.*, 480 F.3d at 1364.

Accordingly, the combination of Tanaka with Chitnis discloses or suggests claim 4. (Ex. 1002 ¶139.)

2. Claim 5

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical diffusion.[21]

Tanaka in combination with Chitnis discloses or suggests claim 5. (Ex. 1002 ¶¶140-151.) For example, as discussed above with respect to claim 4,

[21] While Petitioner addresses the "optical diffusion" feature recited in claim 5, Petitioner does not concede that the '612 patent provides adequate disclosure of the claimed feature in compliance with 35 U.S.C. § 112.

Tanaka discloses that its semiconductor LED is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with an adhesive ("adhesive material"). (*See supra* Section IX.C.1.)

Tanaka discloses bonding its electrodes 51, 52 (part of the first structural unit including the semiconductor LED) to the wiring pattern 80 (part of the second structural unit including monocrystal silicon substrate 20) "via an anisotropic conductive layer or a conductive adhesive" (Ex. 1005 ¶[0072]), but Tanaka is silent regarding the adhesive having the property of optical diffusion, as claimed. However, as discussed below, it would have been obvious to use an adhesive having the property of optical diffusion like that described by Chitnis with an LED device like that depicted in Figure 7 of Tanaka, in order to bond an LED chip to a wafer like the aforementioned bonding of Tanaka's blue-color light-emitting diode chip 70 (including the claimed "semiconductor LED") with the monocrystal silicon substrate 20 ("carrier wafer"). (*See supra* Section IX.C.1; Ex. 1002 ¶141.)

For example, as discussed above in Section IX.C.1, Chitnis, like Tanaka, relates to fabrication of LED devices (Ex. 1007 ¶[0004]) and further discloses well-known wafer-level bonding techniques during LED device fabrication (*id.* ¶[0010]). (*See supra* Section IX.C.1; Ex. 1002 ¶142.) While Chitnis discloses using conductive adhesives like Au-Si or Au-Sn as discussed above with respect to claim 4, Chitnis also discloses using insulating adhesives (e.g., electrically insulating,

dielectric bonding media) to bond the LED chip to the submount wafer. (Ex. 1007 ¶¶[0013], [0025], [0047].) Chitnis discloses such insulating adhesives include benzocyclobutene (BCB). (*Id.* ¶[0047].) A POSITA would have understood that BCB has the property of optical diffusion as it is used as an optical waveguide. (Ex. 1002 ¶¶143-144; Ex. 1015, 1; Ex. 1016, 1.)[22] Thus, a POSITA would have understood that an adhesive such as BCB, as disclosed by Chitnis, would have had the property of optical diffusion, as claimed. (Ex. 1002 ¶143.)

As discussed below, it would have been obvious to use such an optically diffusive adhesive to bond Tanaka's semiconductor LED with the monocrystal silicon substrate 20. (*Id.* ¶145.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*); *KSR*, 550 U.S. at 416-18.

As discussed above with respect to claim 4, a POSITA would have recognized that Tanaka and Chitnis disclose features in a similar technological field. (*See supra* Section IX.C.1.) Accordingly, a POSITA would have had reason to consider the teachings of Chitnis when fabricating an LED device as described in Tanaka given Chitnis discloses the details regarding bonding media for affixing various structures in an LED device like the structures to be bonded in Tanaka. (*Id.*; Ex. 1002 ¶146.)

[22] *See* n.1.

A POSITA would have further recognized that while Tanaka discloses the use of an anisotropic conductive layer or a conductive adhesive between the wiring pattern 80 and electrodes 51, 52 (Ex. 1005 ¶[0072]), a non-conductive adhesive material like BCB could be used in Tanaka's LED device without impeding the functionality of the device. (Ex. 1002 ¶147.) For instance, Chitnis discloses that when an insulating adhesive is used, "vias can be fabricated into the submount wafer and bonding medium after the wafer bonding process (post bond)" and "[t]he vias may subsequently be filled . . . with conductive material to provide electrical contacts to the device." (Ex. 1007 ¶[0025]; *see also id.* ¶¶[0035], [0048] ("After wafer bonding, one or more vias 52 can be fabricated into the submount 40 and bonding medium layer 50 as needed for a particular device or application.").)

In such a scenario, the wiring pattern 80 would have served as an alignment guide for forming the vias in Tanaka's LED device, where the vias provide for an electrical connection between the wiring pattern 80 to the electrodes 51, 52. (Ex. 1002 ¶148.) A POSITA would have understood that this would have been similar to how a bond pad 20 on the LED wafer side of Chitnis' LED device serves as an alignment guide for forming the vias 52. (*Id.*; Ex. 1007 ¶[0048] ("In the embodiment shown, the vias 52 is formed in alignment with the bond pad 20. The vias 52 can be aligned with the bond pad 20 without using difficult and costly alignment processes.").)

Moreover, Tanaka discloses using an adhesive to bond electrodes 51, 52 to the wiring pattern 80 in an LED device, but does not disclose the details of bonding techniques. (Ex. 1005 ¶[0072], FIG. 7.) Chitnis, as described above, discloses well-known bonding techniques in LED devices which include bonding LED structures using conductive and insulating adhesives. (Ex. 1007 ¶¶[0011]-[0012].) Thus, a POSITA would have been motivated to draw from the teachings of Chitnis to implement the bonding in Tanaka's LED device. (Ex. 1002 ¶149.) Based on Chitnis' disclosure, a POSITA would have known that there were from a finite number of identified, predictable solutions for bonding structures during LED device fabrication. (*Id.*; Ex. 1007 ¶¶[0011]-[0013], [0025], [0047].) Therefore, a POSITA would have found it obvious to try using an insulating adhesive (including BCB) to bond electrodes 51, 52 to wiring pattern 80 in Tanaka, given the limited types of adhesives for bonding structures during LED device fabrication. (Ex. 1002 ¶149.); *KSR*, 550 U.S. at 421.

A POSITA would have been skilled and knowledgeable about configuring Tanaka's LED device to include an adhesive such as BCB, while considering any known design, and other related concepts, limitations, benefits, and the like to ensure the resulting combination operated properly and as intended. (Ex. 1002 ¶150.) Thus, a POSITA would have had a reasonable expectation of success in the above modification. (*Id.*); *see Pfizer, Inc.*, 480 F.3d at 1364.

Accordingly, the combination of Tanaka with Chitnis discloses or suggests claim 5. (Ex. 1002 ¶151.)

3. Claim 6

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical reflection.[23]

Tanaka in combination with Chitnis discloses or suggests claim 6. (Ex. 1002 ¶¶152-154.) For example, as discussed above with respect to claim 4, the Tanaka-Chitnis combination discloses that Tanaka's semiconductor LED is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with a conductive adhesive ("adhesive material") such as Au-Si (gold-silicon) or Au-Sn (gold-tin). (*See supra* Section IX.C.1.) As confirmed by the '612 patent, gold-tin can be used to form a reflective surface and would have the property of optical reflection. (Ex. 1001, 6:3-5.) Indeed, both gold and tin are metals which have reflecting properties, and a POSITA would have understood that an adhesive such as Au-Sn would have the property of optical reflection. (Ex. 1002 ¶153; *see also* Ex. 1001, 6:47-50 (disclosing "a reflective material, such as, gold (Au)").) Accordingly, the Tanaka-

[23] While Petitioner addresses the "optical reflection" feature recited in claim 6, Petitioner does not concede that the '612 patent provides adequate disclosure of the claimed feature in compliance with 35 U.S.C. § 112.

Chitnis combination discussed above with respect to claim 4 discloses or suggests claim 6. (Ex. 1002 ¶154.)

4. Claim 7

a) The light emitting device of claim 1, wherein said semiconductor LED is affixed to said carrier wafer with an adhesive material which has the property of optical transmissivity.[24]

Tanaka in combination with Chitnis discloses or suggests claim 7. (Ex. 1002 ¶¶155-156.) For example, as discussed above with respect to claim 5, the Tanaka-Chitnis combination discloses that Tanaka's semiconductor LED is affixed to the monocrystal silicon substrate 20 ("carrier wafer") with a dielectric adhesive ("adhesive material") such as BCB. (*See supra* Section IX.C.2.) Chitnis discloses that such a dielectric adhesive would have the property of optical transmissivity. (Ex. 1007 ¶[0048] ("In the preferred embodiment, the submount wafer 42, dielectric layer 44 and *bonding medium layer 50 are substantially transparent* in the infrared (IR) or visible wavelength spectrum."); *see also id.* ¶[0047] (disclosing examples of bond media 50 including BCB).) Accordingly, the Tanaka-Chitnis combination discussed above with respect to claim 5 discloses or suggests claim 7.

[24] While Petitioner addresses the "optical transmissivity" feature recited in claim 7, Petitioner does not concede that the '612 patent provides adequate disclosure of the claimed feature in compliance with 35 U.S.C. § 112.

(Ex. 1002 ¶156.)

D. Ground 4: The Combination of Tanaka and the AAPA Renders Obvious Claims 1, 2, 8, and 9

As discussed above, Tanaka discloses or suggests the features of claims 1, 2, 8, and 9, including "a semiconductor LED including doped and intrinsic regions thereof," as recited in claim element 1.c. (Ex. 1002 ¶¶157-158.) In particular, as discussed above in Section IX.A.1.c, Tanaka would have disclosed or suggested to a POSITA that activation layer 73 includes an "intrinsic region." (*Supra* Section IX.A.1.c.) But to the extent PO argues or the Board finds that Tanaka does not disclose or suggest such an intrinsic region, a POSITA would have found it obvious to use an "intrinsic" region in the activation layer 73 of Tanaka's GaN LED as the inclusion of such an intrinsic layer between p- and n-type layers was a well-known conventional structure, as admitted by the '612 patent. (Ex. 1002 ¶¶159-162; Ex. 1001, 5:9-11, ("These LEDs comprise a *P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer*."); *see also id.,* 5:30-31 ("*FIG. 1* represents a characteristic horizontal-type Ga LED chip 10. *As described*, GaN layers 11 are grown upon a substrate 12."), 5:38-39.) Indeed, using an "intrinsic" region in the activation layer 73 in Tanaka's GaN LED would have been obvious because it would have constituted applying a known feature (an intrinsic region provided between n and p-doped layers in a GaN LED) to a particular device (the Tanaka GaN LED) to achieve a predictable result

(emission of light by radiative recombination of a hole and an electron in the intrinsic region). (Ex. 1002 ¶161); *KSR*, 550 U.S. at 416-18. For the above reasons, Tanaka in combination with the AAPA, discloses or suggests that the light-emitting diode chip 70 with an N-type semiconductor layer 72, a P-type semiconductor layer 74, and an intrinsic activation layer 73 constitutes "a semiconductor LED including doped and intrinsic regions thereof." (Ex. 1002 ¶161.)

The above modification of Tanaka based on the AAPA does not affect the remainder of the analysis in Section IX.A, which applies equally to this ground. (*Id*. ¶162.) Thus, Tanaka in combination with the AAPA discloses or suggests claims 1, 2, 8, and 9 for the reasons discussed in Section IX.A and those discussed above. (*Id*.; *Supra* Section IX.A.)

E. Ground 5: The Combination of Tanaka, the AAPA, and Weeks Renders Obvious Claim 3

As discussed above in Section IX.B, Tanaka in combination with Weeks renders obvious claim 3. (*Supra* Section IX.B; Ex. 1002 ¶¶163-164.) As discussed above in Section IX.D, the analysis for claim 1 is modified to include reliance on the AAPA. (*Supra* Section IX.D.) The reliance on the AAPA does not, however, alter the analysis for claim 3 set forth in Section IX.B. Thus, claim 3 is rendered obvious by Tanaka in combination with the AAPA and Weeks for reasons similar to those discussed above in Section IX.B. (*Supra* Section IX.B.) For example, the Tanaka-

AAPA combination would have been modified based on Weeks for the same reasons discussed above in Section IX.B to arrive at claim 3. (Ex. 1002 ¶164.)

F. Ground 6: The Combination of Tanaka, the AAPA, and Chitnis Renders Obvious Claims 4-7

As discussed above in Section IX.C, Tanaka in combination with Chitnis renders obvious claims 4-7. (*Supra* Section IX.C; Ex. 1002 ¶¶165-168.) As discussed above in Section IX.D, the analysis for claim 1 is modified to include reliance on the AAPA. (*Supra* Section IX.D.) The reliance on the AAPA does not, however, alter the analysis for claims 4-7 set forth in Section IX.C. (Ex. 1002 ¶167.) Thus, claims 4-7 are rendered obvious by Tanaka in combination with the AAPA and Chitnis for reasons similar to those discussed above in Section IX.C. (*Supra* Section IX.C.) For example, the Tanaka-AAPA combination would have been modified based on Chitnis for the same reasons discussed above in Section IX.C to arrive at claims 4-7. (Ex. 1002 ¶168.)

G. Ground 7: The Combination of Tanaka and Camras Renders Obvious Claims 1, 2, 8, and 9

As discussed above in Section IX.A, Tanaka discloses or suggests the features of claims 1, 2, 8, and 9. (*Supra* Section IX.A; Ex. 1002 ¶¶169-178.) As also discussed above, Tanaka discloses or suggests "a semiconductor LED including doped and intrinsic regions thereof," as recited in claim element 1.c. In particular, Tanaka would have disclosed or suggested to a POSITA that activation layer 73

includes an "intrinsic region." (*Supra* Section IX.A.1.c; Ex. 1002 ¶170.) But to the extent PO argues or the Board finds that Tanaka does not disclose or suggest such an intrinsic region between positively and negatively doped regions, Camras discloses such an LED structure, and a POSITA would have found it obvious to use an "intrinsic" region in the activation layer 73 of Tanaka's GaN LED in view of Camras. (Ex. 1002 ¶171.)

Camras, like Tanaka, is directed to LED structures that include an n-type layer, a p-type layer, and a light emitting active region. (Ex. 1008, 2:27-32, 2:44-61; Ex. 1002 ¶¶171-172, 49-52.) Camras discloses that the light emitting active region of the LED is between p-type layer 110 and n-type layer 108 and includes intrinsic (undoped) material. (Ex. 1008, 2:44-54 ("*active region 112 includes one or more semiconductor layers that are* doped n-type or p-type or are *undoped*").) Camras further discloses that "[a]ctive region 112 emits light upon application of a suitable voltage across contacts 114 and 116." (Ex. 1008, 2:62-63.) Figure 1B of Camras, shown in annotated form below, illustrates the intrinsic layer 112 between p-type layer 110 and n-type layer 108.

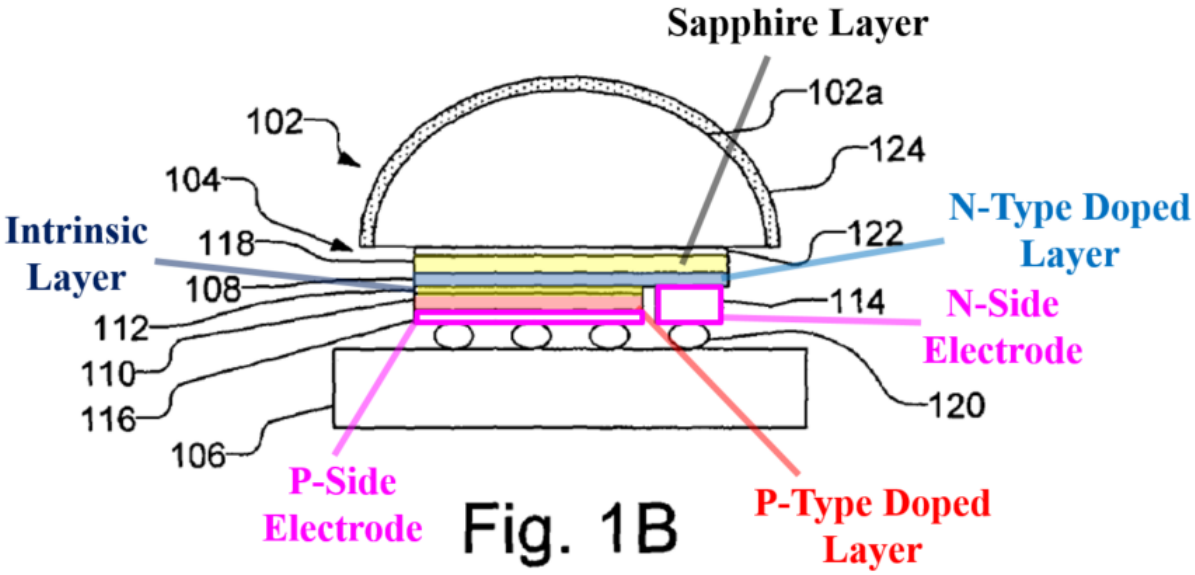


Fig. 1B

(Ex. 1008, FIG. 1B (annotated); Ex. 1002 ¶172.)

A POSITA would have looked to Camras for guidance regarding implementing LED devices as disclosed by Tanaka, particularly because Camras and Tanaka are references in the same field that disclose LED devices with many common features. (Ex. 1002 ¶173.) Having looked to Camras, such a POSITA would have found it obvious to implement the light-emitting activation region 73 in Tanaka such that it includes an intrinsic layer between the p-type and n-type doped regions. (*Id.*)

The semiconductor LED disclosed by Tanaka is specified to include a p-type layer, an n-type layer, and a light-emitting activation region between those layers. (Ex. 1005 ¶¶[0068], [0070] ("light emitted from the activation layer").) As discussed above, Camras discloses LED structures that include an intrinsic light-

emitting layer sandwiched between p-type and n-type regions. (Ex. 1008, 2:44-52.) A POSITA would have found it obvious to use an intrinsic light-emitting layer between the p-type and n-type doped regions, as disclosed by Camras, in conjunction with an LED device as disclosed by Tanaka. (Ex. 1002 ¶174.)

Such a POSITA would also have been motivated to use an intrinsic layer for the light-emitting layer in an LED as disclosed by Tanaka because using an intrinsic layer is one of a limited number of alternatives disclosed by Camras, where those alternatives include p-type, n-type, and intrinsic semiconductor material. (Ex. 1008, 2:50-52; Ex. 1002 ¶175.) Indeed, as discussed above in Section VII.A, the '612 patent discloses that LEDs with an intrinsic layer between p-type and n-type material were known and in use. (*See supra* Section VII; Ex. 1001, 5:9-11, 5:38-39; Ex. 1002 ¶175.) Similarly, Sugawara, Atanackovic, and Herner also demonstrate that a POSITA would have been aware of the use of intrinsic layers between p- and n-type layers in LEDs. (Ex. 1009, 3:45-51; Ex. 1010, 29:15-23; Ex. 1011, 3:29-58, FIG. 1; Ex. 1002 ¶175.)[25]

A POSITA would have found it straightforward to use an intrinsic layer as disclosed by Camras in an LED device as disclosed by Tanaka because Camras discloses such an intrinsic layer in a device very similar to that of Tanaka. (Ex. 1002

[25] *See* n.1.

¶176.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. *KSR*, 550 U.S. at 416. Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Camras, as well as Sugawara, Atanackovic, Herner, and the '612 patent (*see supra* Section VII.A; Ex. 1001, 5:9-11, 5:38-39), LEDs with intrinsic light-emitting layers were well known in the art. (Ex. 1002 ¶176); *see Pfizer, Inc.*, 480 F.3d at 1364.

For the above reasons, Tanaka in combination with Camras discloses or suggests that the light-emitting diode chip 70 with an N-type semiconductor layer 72, a P-type semiconductor layer 74, and an intrinsic activation layer 73 between the N- and P-type layers constitutes "a semiconductor LED including doped and intrinsic regions thereof." (Ex. 1002 ¶177.)

The above modification of Tanaka based on Camras does not affect the remainder of the analysis in Section IX.A, which applies equally to this ground. (*Id*. ¶178.) Thus, Tanaka in combination with Camras discloses or suggests claims 1, 2, 8, and 9 for the reasons discussed in Section IX.A and those discussed above. (*Id*.; *Supra* Section IX.A.)

H. Ground 8: The Combination of Tanaka, Camras, and Weeks Renders Obvious Claim 3

As discussed above in Section IX.B, Tanaka in combination with Weeks renders obvious claim 3. (*Supra* Section IX.B.) As discussed above in Section IX.G,

the analysis for claim 1 is modified to include reliance on Camras. (*Supra* Section IX.G.) The reliance on the AAPA does not, however, alter the analysis for claim 3 set forth in Section IX.B. Thus, claim 3 is rendered obvious by Tanaka in combination with Camras and Weeks for reasons similar to those discussed above in Section IX.B. (*Supra* Section IX.B.) For example, the Tanaka-Camras combination would have been modified based on Weeks for the same reasons discussed above in Section IX.B to arrive at claim 3. (Ex. 1002 ¶¶179-180.)

I. Ground 9: The Combination of Tanaka, Camras, and Chitnis Renders Obvious Claims 4-7

As discussed above in Section IX.C, Tanaka in combination with Chitnis renders obvious claims 4-7. (*Supra* Section IX.C.) As discussed above in Section IX.G, the analysis for claim 1 is modified to include reliance on Camras. (*Supra* Section IX.G.) The reliance on Camras does not, however, alter the analysis for claims 4-7 set forth in Section IX.C. Thus, claims 4-7 are rendered obvious by Tanaka in combination with Camras and Chitnis for reasons similar to those discussed above in Section IX.C. (*Supra* Section IX.C.) For example, the Tanaka-Camras combination would have been modified based on Chitnis for the same reasons discussed above in Section IX.C to arrive at claims 4-7. (Ex. 1002 ¶¶181-183.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. The Other IPR Petition Provides No Basis For Discretionary Denial

This petition is not a "follow-on" petition that the Board should deny under *General Plastics*. *General Plastic Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19, 16–17 (Sept. 6, 2017) (precedential) ("*GP*"). None of the non-exclusive factors that the Board considers in exercising discretion on instituting review as to "follow-on" petitions weigh in favor of a denial here in light of the SSC IPR (*see supra* Section II).

Under the first *General Plastic* factor, the Board considers "whether the *same* petitioner previously filed a petition directed to the *same* claims of the same patent." *GP* at 16. Petitioner has not previously done so. Indeed, this is Petitioner's first IPR petition directed to any claims of the '612 patent. Petitioner has not coordinated in any way with SSC in relation to challenging claims of the '612 patent. Moreover, the SSC IPR does not challenge the "same claims" of the '612 patent as the instant IPR. While the SSC IPR challenges claims 1-4, 6, 7, and 9, Petitioner is challenging claims 1-9 of the '612 patent. SSC IPR, Paper 1 at 10-11. That is, the SSC IPR does not cover all the challenged claims in the instant IPR, including claim 5, which is asserted against Petitioner in the related district court litigation. Thus, the first factor favors institution.

The second through fifth *General Plastic* factors have little to no bearing here

given factor one favors institution. *Amneal Pharmaceuticals LLC et al. v. Almirall, LLC*, IPR2019-00207, Paper 13 ("*Amneal*") at 12–13 (May 10, 2019) (finding factor one dispositive); *Western Digital Corp. v. Spex Technologies, Inc.*, IPR2018-00084, Paper 14 at 17 (April 25, 2018) ("Because Petitioner has not previously filed a petition against the same patent, factors 2–5 bear little relevance in this case."). In any event, with respect to the second factor (*GP* at 16), the prior art asserted in the instant Petition is different than the prior art asserted in the SSC IPR. (*See supra* Section V.B.); SSC IPR, Paper 1 at 10-11. Further, with respect to the third factor (*GP* at 16), this Petition is being filed shortly after the SSC IPR was filed and before any preliminary response or institution decision in the SSC IPR and thus, Petitioner could not have leveraged any perceived flaws in the SSC IPR. *See, e.g.*, *Unified Patents Inc. v. Speakware, Inc.*, IPR2019-00495, Paper 9 at 14-15 (July 1, 2019) (instituting IPR filed after two other IPRs because petitioner did not receive any preliminary response or institution decision from the prior IPRs and thus "there is no indication that Petitioner strategically staged its prior art and arguments in order to use PO's preliminary response or the Board's decision on institution as a roadmap"); *Livanova, Inc. et al. v. Neuro and Cardiac Tech., LLC*, IPR2019-00264, Paper 7 at 30-31 (May 20, 2019) (similar). The fourth and fifth factors (*GP* at 16) are inapplicable since this is Petitioner's first petition challenging any claims of the '612 patent and because there is no overlap between the grounds of this petition and

the grounds in the SSC IPR. (*See supra* Section V.B.); SSC IPR, Paper 1 at 10-11. Thus, if anything, the second through fifth *General Plastic* factors favor institution.

The sixth and seventh *General Plastic* factors (*GP* at 16) also favor institution because there is no indication that the instant IPR would unduly burden Board resources or impact the Board's duty to render a FWD in this IPR, particularly given the undeniable similarity between Petitioner's primary reference and the '612 patent. *SK Hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00364, Paper 7 at 35 (August 6, 2018); *Cooler Master Co. Ltd. v. Aavid Thermalloy LLC*, IPR2019-00337, Paper 7 at 44-45 (June 12, 2019) (instituting review and noting that "considerations of patent quality and merits of the challenges outweigh concerns about duplication of resources and potential for harassment").

Accordingly, the Board should consider and institute review of the challenged claims of the '612 patent.

B. The Related Litigation Provides No Basis For Discretionary Denial

NHK Spring Co., Ltd. v. Intri-Plex Techs, Inc., IPR2018-00752, Paper 8 (P.T.A.B. Sept. 12, 2018) does not apply here. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 3 (P.T.A.B. Mar. 20, 2020) (precedential) ("*NHK* applies . . . where the district court has set a trial date to occur earlier than the Board's deadline to issue a final written decision in an instituted proceeding."). The six-factor test addressed in *Fintiv* favors institution. *See id.*, 5-6.

For the *first factor* (stay), there is no stay, but courts routinely issue stays after institution. *Western Digital Corp. et al v. Kuster*, IPR2020-01391, Paper 10 at 8-9 (Mar. 11, 2021); *Samsung Elec. Am., Inc. v. Snik LLC*, IPR2020-01427, Paper 10 at 10 (Mar. 9, 2021). At a minimum, this factor deserves little weight given that factors two through four and six weigh in favor of institution. *See Fintiv*, 7.

The second (proximity of trial dates) and third (investment in parallel proceedings) factors weigh in favor of institution. The district court has not set a trial date, and, there has not been significant resource investment by the court and the parties, particularly compared to the resource expenditures leading up to a trial. *See Resideo Techs., Inc. v. Innovation Sciences, LLC*, IPR2019-01306, Paper 19 at 11 (Jan. 27, 2020). Furthermore, the court's order governing patent proceedings sets a default Markman hearing date as "23 weeks after [case management conference] (or as soon as practicable)" and a default trial date as "52 weeks after Markman hearing (or as soon as practicable)." (Ex. 1022, 9, 11); *see Precision Planting, LLC. v. Deere & Co.*, IPR2019-01044, Paper 17 at 14-15 (P.T.A.B. Dec. 2, 2019) (weighs against finding that case is at "an advanced stage"); *Abbott Vascular, Inc. v. FlexStent, LLC*, IPR2019-00882, Paper 11 at 30 (P.T.A.B. Oct. 7, 2019) (same). Additionally, WDTX civil trials "may possibly slip" due to "months of backlogged trials." *HP Inc. v. Slingshot Printing LLC*, IPR2020-01085, Paper 12 at 7 (Jan. 14, 2021). Nevertheless, even "an early trial date" is "non-dispositive" and simply

means that "the decision whether to institute will likely implicate other factors," which, as explained, favor institution. *Fintiv*, 5, 9.

Furthermore, the Board has held "that it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding." *Id.* at 11. Here, Patent Owner served its infringement contentions just five weeks before this petition is being filed.

The fourth factor (overlap) also weighs in favor of institution. PO's infringement contentions assert claims 1-7 and 9 of the '612 patent while the present Petition challenges claims 1-9 of the '612 patent. (Section IX.) Moreover, Petitioner hereby stipulates that, if the IPR is instituted, Petitioner will not pursue the IPR grounds in the district court litigation. Thus, "[i]nstituting trial here serves overall system efficiency and integrity goals by not duplicating efforts and by resolving materially different patentability issues." *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 at 19 (P.T.A.B. June 15, 2020) (finding the fourth factor "strongly favored" institution even though there was no stipulation and a significant dispute about the extent of overlap); *see also Sand Revolution II, LLC v. Continental Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 12 (P.T.A.B. June 16, 2020) (finding the fourth factor weighs in favor of institution due, in part, to petitioner's stipulation that it will not pursue the same grounds in district court).

For the fifth factor (parties), the Petitioner and PO are the same parties as in district court.

The sixth factor (other circumstances) weighs in favor of institution given the undeniable similarity between Petitioner's primary reference and the '612 patent (as noted earlier) and Petitioner diligently filed this Petition within six months of PO's complaint. (Ex. 1021.) Institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc. v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).[26]

[26] The Board should also decline any arguments for a discretionary denial under 35 U.S.C. § 325(d). Petitioner does not rely on any art or arguments that are the same or substantially the same as those previously presented to the Office, including the art relied upon in the SSC IPR. *See Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) (precedential).

XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for the challenged claims based on each of the specified ground(s).

Respectfully submitted,

Dated: September 20, 2021 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,502,612 contains, as measured by the word-processing system used to prepare this paper, 13,986 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: September 20, 2021

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on September 20, 2021, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,502,612 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

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A courtesy copy was also sent via electronic mail to the Patent Owner's litigation counsel at the following addresses:

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