IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re *Ex Parte* Reexamination of:	)	
	)	
U. S. Patent No. 9,786,822	)	Control No.: *To be assigned*
	)	
Issue Date: Oct. 10, 2017	)	Group Art Unit: *To be assigned*
	)	
Inventor: Mordehai Margalit	)	Examiner: *To be assigned*
	)	
Appl. No. 14/570,449	)	Confirmation No.: *To be assigned*
	)	
Filing Date: Dec. 15, 2014	)	
	)	
For: LIGHT EMITTING DIODE PACKAGE AND METHOD OF MANUFACTURE	)	

Mail Stop *Ex Parte* Reexam
Attn: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

REQUEST FOR *EX PARTE* REEXAMINATION OF U.S. PATENT NO. 9,786,822

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Ex. LIT-4	Transfer of *LED Wafer Sols. LLC v. Samsung Elecs. Co.*, No 6:21-CV-00292 (W.D. Tex.) to *LED Wafer Sols. LLC v. Samsung Elecs. Co.*, No 3:22-CV-04809 (N.D. Cal.)

I. Introduction

An *ex parte* reexamination is requested on claims 1, 2, and 5-10 ("the challenged claims") of U.S. Patent No. 9,786,822, which issued on October 10, 2017 to Margalit ("the '822 patent," Ex. PAT-A), for which the U.S. Patent and Trademark Office ("Office") files identify LED Wafer Solutions LLC ("LED Wafer" or "Patent Owner") as the assignee. In accordance with 37 C.F.R. § 1.510(b)(6), Requester Samsung Electronics Co., Ltd. ("Requester") hereby certifies that the statutory estoppel provisions of 35 U.S.C. § 315(e)(1) and 35 U.S.C. § 325(e)(1) do not prohibit it from filing this *ex parte* reexamination request.

This request raises substantial new questions of patentability based on prior art that the Office did not have before it or did not fully consider during the prosecution of the '822 patent, and which discloses or suggests the features recited in the challenged claims. Requester respectfully urges that this request be granted and that reexamination be conducted with "special dispatch" pursuant to 35 U.S.C. § 305. The Office should find the claims unpatentable over this art.

In accordance with 37 C.F.R. § 1.20(c), the fee for *ex parte* reexamination (non-streamlined) is submitted herewith. If this fee is missing or defective, please charge the fee as well as any additional fees that may be required to Deposit Account No. 50-2613.

II. Related Proceedings

On March 25, 2021, Patent Owner filed suit against Requester asserting, *inter alia*, infringement of the '822 patent in *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd.*, No 6-21-CV-00292 (W.D. Tex.). (Ex. LIT-1.) Thereafter, on August 22, 2022, the case was transferred to *LED Wafer Solutions LLC v. Samsung Electronics Co., Ltd.*, No 3-22-CV-04809 (N.D. Cal.). (Ex. LIT-4.)

Requester filed an *inter partes* review petition against the '822 patent on September 10, 2021. IPR2021-01526, Paper 1. The Patent Trial and Appeal Board ("the PTAB") denied that petition on March 22, 2022. IPR2021-01526, Paper 9. Petitioner's motion for rehearing of the decision was denied on June 8, 2022. IPR2021-01526, Papers 10 and 11.

This request, however, does not raise "the same or substantially the same prior art or arguments" previously presented, including in IPR2021-01526. 35 U.S.C. § 325(d). This request is based on prior art that the Office did not have before it or did not fully consider during the prosecution of the '822 patent, that the PTAB did not have before it in IPR2021-01526, and which

discloses or suggests the features recited in the challenged claims, especially under the broadest reasonable interpretation standard applicable to this request. This request also presents new combinations of references that were not before the Office or the PTAB. In fact, no prior art references were applied to the claims in any office action during prosecution. (Ex. PAT-B, 11-18 (Notice of Allowance), 69-73 (Non-Final Office Action), 119-123 (Restriction Requirement).) And the references used in this request are substantially different than those used in IPR2021-01526. In IPR2021-01526, the PTAB denied institution, because it determined that Petitioner had not demonstrated sufficiently that Wirth (U.S. Patent No. 8,835,937) teaches or suggests "a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer," as recited in claim 1. IPR2021-01526, Paper 9 at 8-14 (P.T.A.B. Mar. 22, 2022). The Board reached this determination based on its finding that "Petitioner has not explained adequately why a person of ordinary skill in the art would have considered Wirth's current spreading layer to be part of the claimed 'semiconductor LED' in view of Wirth's teachings." IPR2021-01526, Paper 9 at 8-14 (P.T.A.B. Mar. 22, 2022). This request neither cites Wirth nor maps to a current spreading layer as a part of any semiconductor LED. As discussed below in Section VI, the primary references in this request (*Epler* and *Shimokawa*) provide substantially different disclosure regarding this limitation. Regardless, the Office erred in a manner material to patentability by not considering the teachings, arguments, obviousness combinations, and evidence presented in this request (Section VI).

III. Identification of Claims and Citation of Prior Art Presented

Requester respectfully requests reexamination of claims 1, 2, and 5-10 of the '822 patent in view of the following prior art references, which are also listed on the attached PTO Form SB/08.

Ex. PA-1	U.S. Patent Application Publication No. 2010/0019260 to Epler *et al.* ("*Epler*")
Ex. PA-9	U.S. Patent Application Publication No. 2004/0000672 to Fan *et al.* ("*Fan*")
Ex. PA-11	U.S. Patent Application Publication No. 2010/0308367 to Aldaz *et al.* ("*Aldaz*")

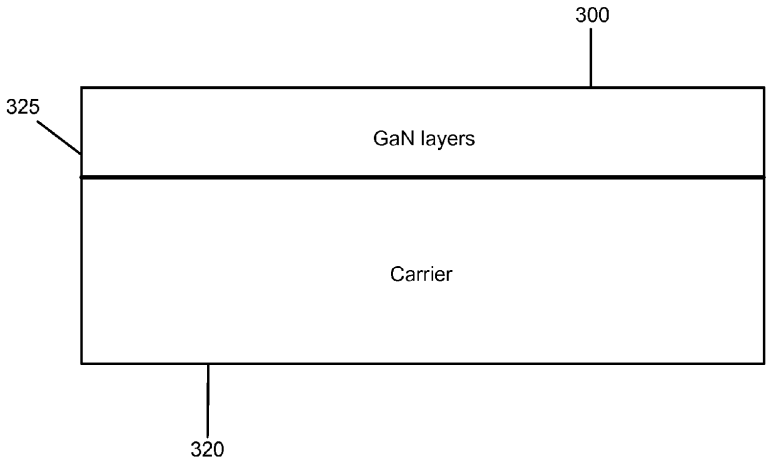
Ex. PA-34	U.S. Patent No. 7,791,090 to Lester *et al.* ("*Lester*")
Ex. PA-3	U.S. Patent No. 8,581,291 to Shimokawa *et al.* ("*Shimokawa*")
Ex. PA-20	U.S. Patent Application Publication No. 2008/0251781 to Han *et al.* ("*Han*")
Ex. PA-36	U.S. Patent No. 7,105,857 to Nagahama *et al.* ("*Nagahama*")
Ex. PA-37	U.S. Patent Application Publication No. 2009/0121241 to Keller et al. ("*Keller*")

A copy of each of the above-listed references is attached to this request pursuant to 37 C.F.R. § 1.510(b)(3). A copy of the '822 patent is also attached to this request as Exhibit PAT-A pursuant to 37 C.F.R. § 1.510(b)(4).

IV. Overview of the '822 Patent

A. Specification and Drawings of the '822 Patent

The '822 patent relates to "a light emitting diode (LED) device." (Ex. PAT-A, 1:16-19; *see also id.*, Abstract, 2:6-30; Ex. PA-DEC, ¶31.) The '822 patent admits that light emitting diode (LED) devices were well known and depicts a prior art LED device in Figure 3 below. (Ex. PAT-A, 2:54-59, 4:16-18, FIGs. 1-3.)

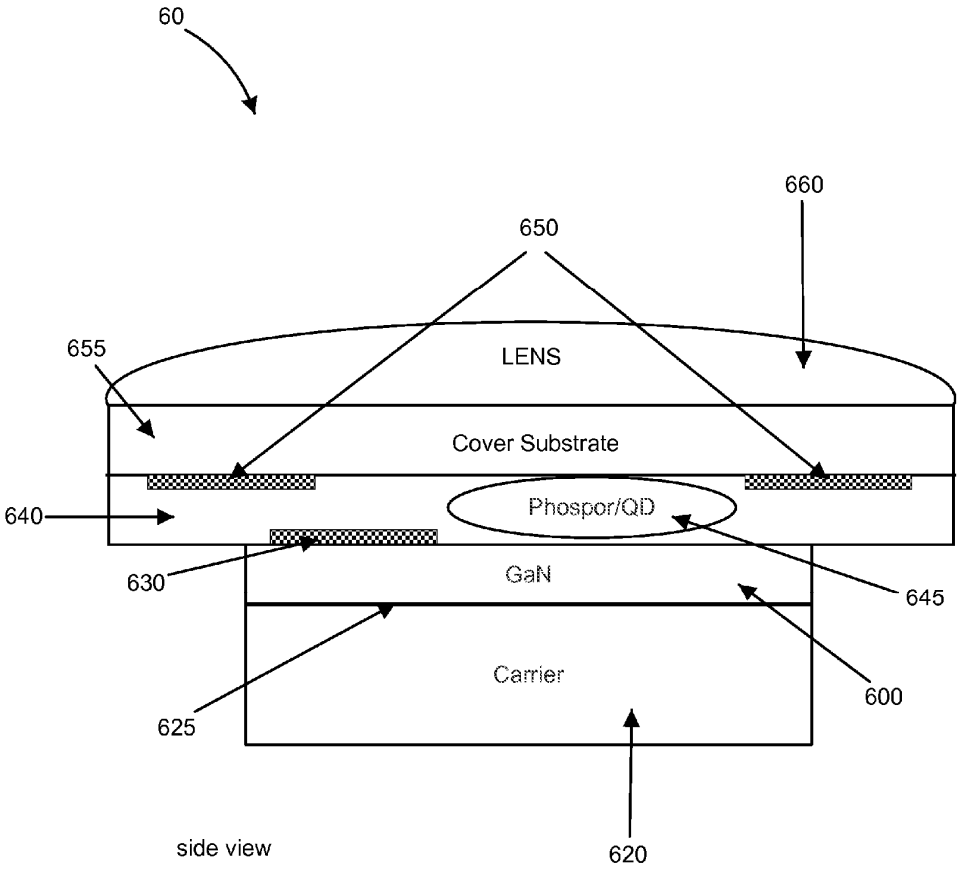


(Ex. PAT-A, FIG. 3; Ex. PA-DEC, ¶31.)

The prior art light emitting device 30 of Figure 3 includes a semiconductor LED layer 300, a metallic interface 325,[1] and a carrier layer 320. (Ex. PAT-A, 3:64-4:2, 4:16-18.) The semiconductor LED layer 300 includes a GaN layer. (*Id.*, FIG. 3.) GaN refers to a gallium nitride "which is a type of bandgap semiconductor suited for use in high power LEDs." (*Id.*, 3:28-30.) The '822 patent states that GaN LEDs "comprise a P-I-N junction device having an intrinsic (I) layer disposed between a N-type doped layer and a P-type doped layer." (*Id.*, 3:32-34; Ex. PA-DEC, ¶32.)

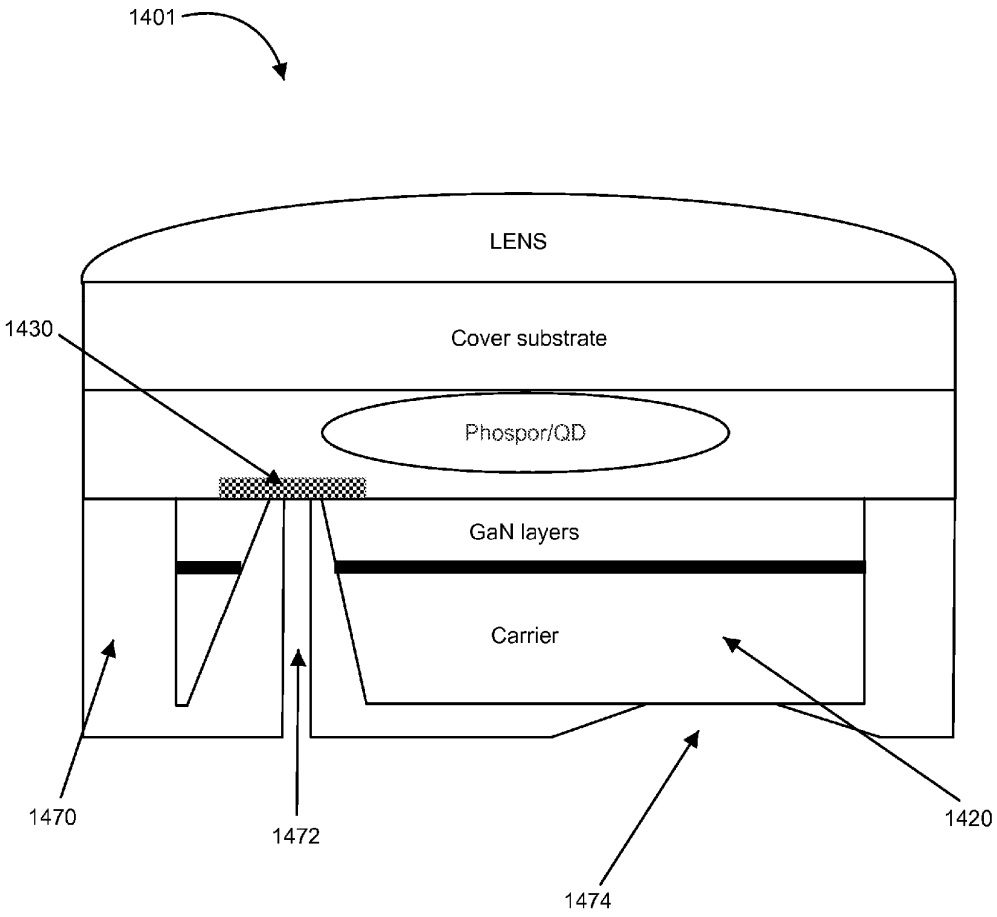
The disclosed embodiments of the '822 patent build on the prior art device of Figure 3. For instance, the disclosed embodiments describe an LED device comprised of additional layers that "act to promote mechanical, electrical, thermal, or optical characteristics of the device" (Ex. PAT-A, 2:2-4, 19-23; *see also id.,* Abstract), as seen in Figures 6 and 14, reproduced below. (*Id.*, 4:55-59, 7:16-23, FIGS. 6, 14; *see also id.*, 2:64-66, 3:13-14; Ex. PA-DEC, ¶33.) Like the prior-art LED device in Figure 3 above, each of the devices 60 and 1401 in Figures 6 and 14, respectively, includes the GaN LED layer separated from the carrier layer by a metallic interface (e.g., element 625 in Figure 6 and the dark black line between "GaN layers" and "Carrier" in Figure 14). (*Id.*, 4:55-59; *compare id.*, FIGs. 6, 14 *with* FIG. 3.)

[1] Element 325 points to GaN layers in Figure 3, but element 325 is described as a metallic interface in the '822 patent. (Ex. PAT-A, FIG. 3, 3:64-4:2, 4:16-18.)



(*Id.*, FIG. 6; Ex. PA-DEC, ¶33.)

The LED device 60, as shown by Figure 6 above, further includes an optically transparent or transmissive adhesive layer 640 (*id.*, 4:60-65), a cover substrate 655 (*id.*, 5:17-24), and an optical lens 660 (*id.*, 5:25-30). The transparent or optically permissive adhesive layer 640 may contain "a region containing phosphor and/or quantum dot material (QD) 645." (*Id.*, 5:9-11.) The optical lens 660 "act[s] to spread, diffuse, collimate, or otherwise redirect and form the output of the LED." (*Id.*, 5:26-30.) Like device 60 in Figure 6, the device 1401 in Figure 14 below includes similar layers. (*Id.*, 7:16-23; Ex. PA-DEC, ¶34.)



(Ex. PAT-A, FIG. 14; Ex. PA-DEC, ¶34.)

Device 1401 further includes a passivation layer 1470. (Ex. PAT-A, 7:19-21; *see also id.*, 6:22-26 (the device in Figure 11 "including a passivation layer 1170 that has been applied to surround certain portions of the device around LED semiconducting layer 1100, metallic interface 1125, and carrier layer 1120"), FIG. 11.) Device 1401 also includes contact holes 1472, 1474, which have been drilled or etched into passivation layer material 1470, along with the carrier and GaN layers. (*Id.*, 7:19-21; *see also id.*, 6:14-21, FIG. 10.) The '822 patent states that "this exposes a first contact 1472 at metal pad 1430 and a second contact 1474 at carrier 1420." (*Id.*, 7:21-22; Ex. PA-DEC, ¶35.)

As explained below and in the accompanying declaration of Dr. Baker, all the limitations in the challenged claims were known in the prior art. (*See infra* Section VI; Ex. PA-DEC, ¶36.)

B. Prosecution History of the '822 patent

During prosecution, no prior art references were applied to the claims in any office action. (Ex. PAT-B, 11-18 (Notice of Allowance), 69-73 (Non-Final Office Action), 119-123 (Restriction

Requirement).) The claims, however, were amended in response to a written description rejection. (*Id.*, 61-64 (Applicant's Remarks), 69-73 (Non-Final Office Action).) Neither *Epler*, *Fan*, *Aldaz*, *Lester*, *Nagahama*, *Shimokawa*, *Han*, nor *Keller* were considered during prosecution of the '822 patent. (*See generally* Ex. PAT-B.)

C. The Effective Priority Date of the '822 Patent

For purposes of this reexamination only, Requester assumes that claims 1, 2, and 5-10 are entitled to the filing date of related provisional application Nos. 60/449,685 and 61/449,686, which is March 6, 2011. (Ex. PAT-A, 2.) *Epler*, *Fan*, *Nagahama*, *Han*, and *Keller* each issued more than one year prior to March 6, 2011, and thus qualify as prior art at least under pre-AIA 35 U.S.C. § 102(b); *Shimokawa*, which was filed on September 9, 2009, *Aldaz*, which was filed on April 23, 2010, and *Lester*, which was filed on June 11, 2007, qualify as prior art at least under pre-AIA 35 U.S.C. § 102(e).

V. Claim Construction

"During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" MPEP § 2111; *see also* MPEP § 2258. Limitations in the specification are not read into the claims. MPEP § 2258. The standard of claim interpretation in reexamination is different than that used by the courts in patent litigation and the Board in *inter partes* review proceedings.[2] Therefore, any claim interpretations submitted or implied herein for the purpose of this reexamination do not necessarily correspond to the appropriate construction under the legal standards mandated in litigation. MPEP § 2686.04.11; *see also In re Zletz*, 893 F.2d 319, 322, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). For purposes of this request, Requester believes that no constructions of the challenged claims are needed.

In the Western District of Texas litigation involving the '822 patent (*see generally* Ex. LIT-1), Seoul Semiconductor proposed that an "electrical contact in electrical communication with said first surface of said semiconductor LED," as recited in claim 1 of the '822 patent, should be

[2] Requester reserves all rights and defenses available including, without limitation, defenses as to invalidity, unenforceability, and non-infringement regarding the '822 patent. Further, because the claim interpretation standard used by courts in patent litigation is different from the appropriate standard for this reexamination, any claim constructions submitted or implied herein for the purpose of this reexamination are not binding upon Requester in any litigation related to the '822 patent. Specifically, any interpretation or construction of the claims presented herein or in Dr. Baker's declaration for reexamination, either implicitly or explicitly, should not be viewed as constituting, in whole or in part, the Requester's own interpretation or construction of such claims.

construed to mean an "electrical contact that is in a conduction path with the first surface of the semiconductor LED." (Ex. LIT-2, 5.) Patent Owner asserted that the limitation should be given its plain and ordinary meaning. (*Id.*) In addition, the Patent Owner and Requester also agreed that a "carrier layer," as recited in claim 1 of the '822 patent, should be given its plain and ordinary meaning. (*Id.*, 1.) No other other claim construction positions were offered for the '822 patent. (*Id.*, 1-5.)

While Requester believes no constructions are needed, the prior art mappings found in Section VI of this Request include analysis explaining how the claims of the '822 patent are unpatentable under the constructions advanced in the Western District of Texas litigation. Nonetheless, the claims would be unpatentable under any reasonable construction of the terms given how closely the prior art maps to the claims. This is particularly true given that the broadest reasonable interpretation standard governs this request.

VI. Statement of Substantial New Questions of Patentability

As mentioned above, *Epler*, *Fan*, *Aldaz*, *Lester*, *Nagahama*, *Shimokawa*, *Han*, and *Keller* were never made of record or considered by the Office during original prosecution of the '822 patent. However, the references (in various combinations for respective claims) disclose or suggest all of the features of claims 1, 2, and 5-10 of the '822 patent.

SNQ1: *Epler* raises a substantial new question of patentability (SNQ1) with respect to claims 1, 2, 5-7, and 9 of the '822 patent.

SNQ2: *Epler* and *Fan* raise a substantial new question of patentability (SNQ2) with respect to claim 8 of the '822 patent.

SNQ3: *Epler* and *Aldaz* raise a substantial new question of patentability (SNQ3) with respect to claim 10 of the '822 patent.

SNQ4: *Epler* and *Lester* raise a substantial new question of patentability (SNQ4) with respect to claims 1, 2, 5-7, and 9 of the '822 patent.

SNQ5: *Epler*, *Lester*, and *Fan* raise a substantial new question of patentability (SNQ5) with respect to claim 8 of the '822 patent.

SNQ6: *Epler*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ6) with respect to claim 10 of the '822 patent.

SNQ7: *Epler* and *Han* raise a substantial new question of patentability (SNQ7) with respect to claims 1, 2, 5-7, and 9 of the '822 patent.

SNQ8: *Epler*, *Han*, and *Fan* raise a substantial new question of patentability (SNQ8) with respect to claim 8 of the ’822 patent.

SNQ9: *Epler*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ9) with respect to claim 10 of the ’822 patent.

SNQ10: *Epler*, *Han*, and *Lester* raise a substantial new question of patentability (SNQ10) with respect to claims 1, 2, 5-7, and 9 of the ’822 patent.

SNQ11: *Epler*, *Han*, *Lester*, and *Fan* raise a substantial new question of patentability (SNQ11) with respect to claim 8 of the ’822 patent.

SNQ12: *Epler*, *Han*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ12) with respect to claim 10 of the ’822 patent.

SNQ13: *Epler* and *Nagahama* raise a substantial new question of patentability (SNQ13) with respect to claims 1, 2, 5-7, and 9 of the ’822 patent.

SNQ14: *Epler*, *Nagahama*, and *Fan* raise a substantial new question of patentability (SNQ14) with respect to claim 8 of the ’822 patent.

SNQ15: *Epler*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ15) with respect to claim 10 of the ’822 patent.

SNQ16: *Epler*, *Nagahama*, and *Lester* raise a substantial new question of patentability (SNQ16) with respect to claims 1, 2, 5-7, and 9 of the ’822 patent.

SNQ17: *Epler*, *Nagahama*, *Lester*, and *Fan* raise a substantial new question of patentability (SNQ17) with respect to claim 8 of the ’822 patent.

SNQ18: *Epler*, *Nagahama*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ18) with respect to claim 10 of the ’822 patent.

SNQ19: *Shimokawa* raises a substantial new question of patentability (SNQ19) with respect to claims 1, 2, and 5-10 of the ’822 patent.

SNQ20: *Shimokawa* and *Aldaz* raise a substantial new question of patentability (SNQ20) with respect to claim 10 of the ’822 patent.

SNQ21: *Shimokawa* and *Han* raise a substantial new question of patentability (SNQ21) with respect to claims 1, 2, and 5-10 of the ’822 patent.

SNQ22: *Shimokawa*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ22) with respect to claim 10 of the ’822 patent.

SNQ23: *Shimokawa* and *Nagahama* raise a substantial new question of patentability (SNQ23) with respect to claims 1, 2, and 5-10 of the '822 patent.

SNQ24: *Shimokawa*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ24) with respect to claim 10 of the '822 patent.

SNQ25: *Shimokawa* and *Keller* raise a substantial new question of patentability (SNQ25) with respect to claims 1, 2, and 5-10 of the '822 patent.

SNQ26: *Shimokawa*, *Keller*, and *Aldaz* raise a substantial new question of patentability (SNQ26) with respect to claim 10 of the '822 patent.

SNQ27: *Shimokawa*, *Keller*, and *Han* raise a substantial new question of patentability (SNQ27) with respect to claims 1, 2, and 5-10 of the '822 patent.

SNQ28: *Shimokawa*, *Keller*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ28) with respect to claim 10 of the '822 patent.

SNQ29: *Shimokawa*, *Keller*, and *Nagahama* raise a substantial new question of patentability (SNQ29) with respect to claims 1, 2, and 5-10 of the '822 patent.

SNQ30: *Shimokawa*, *Keller*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ30) with respect to claim 10 of the '822 patent.

Thus, for these reasons and the reasons discussed below and in the accompanying declaration of Dr. Baker (Ex. PA-DEC), *Epler* raises a substantial new question of patentability (SNQ1) with respect to claims 1, 2, 5-7, and 9 of the '822 patent; *Epler* and *Fan* raise a substantial new question of patentability (SNQ2) with respect to claim 8 of the '822 patent; *Epler* and *Aldaz* raise a substantial new question of patentability (SNQ3) with respect to claim 10 of the '822 patent; *Epler* and *Lester* raise a substantial new question of patentability (SNQ4) with respect to claims 1, 2, 5-7, and 9 of the '822 patent; *Epler*, *Lester*, and *Fan* raise a substantial new question of patentability (SNQ5) with respect to claim 8 of the '822 patent; *Epler*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ6) with respect to claim 10 of the '822 patent; *Epler* and *Han* raise a substantial new question of patentability (SNQ7) with respect to claims 1, 2, 5-7, and 9 of the '822 patent; *Epler*, *Han*, and *Fan* raise a substantial new question of patentability (SNQ8) with respect to claim 8 of the '822 patent; *Epler*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ9) with respect to claim 10 of the '822 patent; *Epler*, *Han*, and *Lester* raise a substantial new question of patentability (SNQ10) with respect to claims 1, 2, 5-7, and 9 of the '822 patent; *Epler*, *Han*, *Lester*, and *Fan* raise a substantial new question of

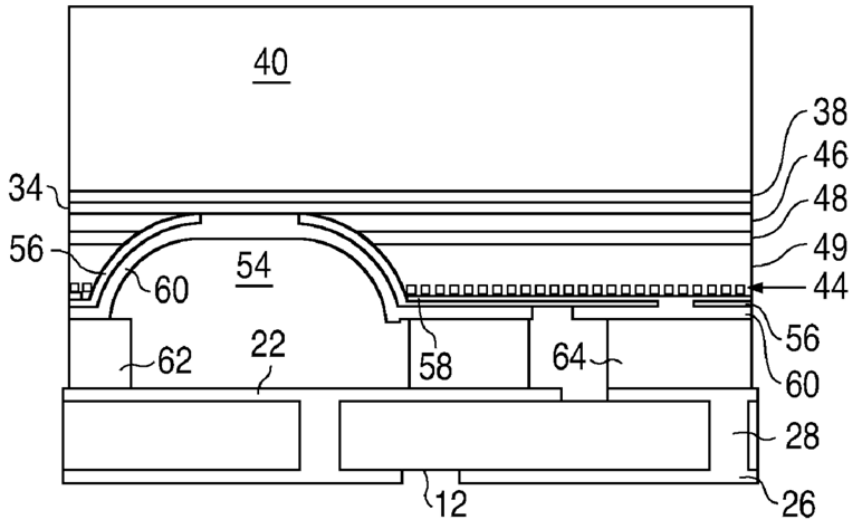
patentability (SNQ11) with respect to claim 8 of the ’822 patent; *Epler*, *Han*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ12) with respect to claim 10 of the ’822 patent; *Epler* and *Nagahama* raise a substantial new question of patentability (SNQ13) with respect to claims 1, 2, 5-7, and 9 of the ’822 patent; *Epler*, *Nagahama*, and *Fan* raise a substantial new question of patentability (SNQ14) with respect to claim 8 of the ’822 patent; *Epler*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ15) with respect to claim 10 of the ’822 patent; *Epler*, *Nagahama*, and *Lester* raise a substantial new question of patentability (SNQ16) with respect to claims 1, 2, 5-7, and 9 of the ’822 patent; *Epler*, *Nagahama*, *Lester*, and *Fan* raise a substantial new question of patentability (SNQ17) with respect to claim 8 of the ’822 patent; *Epler*, *Nagahama*, *Lester*, and *Aldaz* raise a substantial new question of patentability (SNQ18) with respect to claim 10 of the ’822 patent; *Shimokawa* raises a substantial new question of patentability (SNQ19) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa* and *Aldaz* raise a substantial new question of patentability (SNQ20) with respect to claim 10 of the ’822 patent; *Shimokawa* and *Han* raise a substantial new question of patentability (SNQ21) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ22) with respect to claim 10 of the ’822 patent; *Shimokawa* and *Nagahama* raise a substantial new question of patentability (SNQ23) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ24) with respect to claim 10 of the ’822 patent; *Shimokawa* and *Keller* raise a substantial new question of patentability (SNQ25) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa*, *Keller*, and *Aldaz* raise a substantial new question of patentability (SNQ26) with respect to claim 10 of the ’822 patent; *Shimokawa*, *Keller*, and *Han* raise a substantial new question of patentability (SNQ27) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa*, *Keller*, *Han*, and *Aldaz* raise a substantial new question of patentability (SNQ28) with respect to claim 10 of the ’822 patent; *Shimokawa*, *Keller*, and *Nagahama* raise a substantial new question of patentability (SNQ29) with respect to claims 1, 2, and 5-10 of the ’822 patent; *Shimokawa*, *Keller*, *Nagahama*, and *Aldaz* raise a substantial new question of patentability (SNQ30) with respect to claim 10 of the ’822 patent.

A. SNQ1: *Epler* Discloses or Suggests Claims 1, 2, 5-7, and 9

As explained below and in the attached declaration of Dr. Baker (Ex. PA-DEC), *Epler* discloses or suggests the limitations of claims 1, 2, 5-7, and 9 of the '822 patent. (Ex. PA-DEC, ¶41.)

1. Overview of *Epler*

Epler relates to LED technologies and discloses a "semiconductor light emitting device." (Ex. PA-1, Abstract, ¶¶[[0001]-[0002], [0034]-[0035], FIGs. 6-7.) The device includes a light emitting region and emits "rays of light." (*Id.*, ¶¶[0030], [0034].) An example semiconductor light emitting device is illustrated in Figure 6. (*Id.*, ¶[0017].)



(*Id.*, FIG. 6.)

The top layers of the *Epler* semiconductor light emitting device affect light output. For instance, one or more phosphors may be disposed in semiconductor bonding material to shape the color of the emitted light. (*Id.*, ¶[0027], FIG. 6.) When the *Epler* semiconductor light emitting device includes bonding layers 34 and 38, bonding layer 38 may be formed on a window layer 40. (*Id.*, ¶[0027].) When the *Epler* semiconductor light emitting device does not include bonding layer 38, bonding layer 34 is attached to the bottom of the window layer as described with respect to layer 38. (*Id.*, ¶¶[0016], [0020], [0027], FIGs. 4-6.)

Beneath the top optical layers, *Epler* discloses an "n-type region 49," which includes a "porous region 44," a light emitting region 48" (an active region), and a "p-type region 46," which together comprise a semiconductor LED. (*Id.*, ¶¶[0001]-[0002], [0034], [0020], [0030], FIG. 6.) An n-contact metal 58 is formed on porous layer 44 of the n-type region 49 (porous layer 44 is a

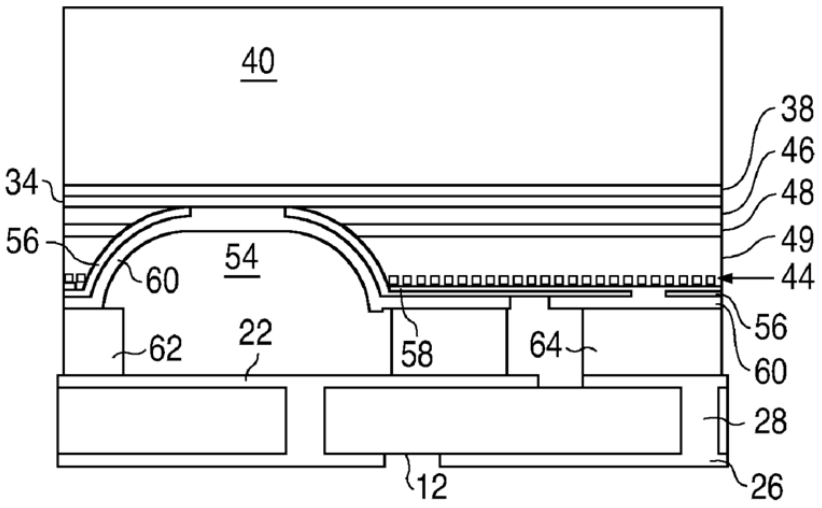
pitted section of n-type region 49). (*Id.*, ¶¶[0032], [0034]-[0035], FIG. 6.) And a p-contact metal 60 is formed on an exposed portion of conductive bonding layer 34. (*Id.*, ¶¶[0032], [0034]-[0035], FIG. 6.) A dielectric layer 56 insulates portions of the n-contact metal 58 and p-contact metal 60. (*Id.*, ¶[0034], FIG. 6.)

Epler discloses that one or more openings are etched through layers of the *Epler* semiconductor light emitting device as a part of a contact formation process. (Ex. PA-1, ¶[0034], FIG. 6.) A first opening/hole through dielectric layer 56 allows p-contact metal 60 to make electrical contact with bonding layer 34 and form a p-type conductive path of the semiconductor device. (*Id.*, ¶¶[0034]-[0035], FIG. 6.) In a similar fashion, a second opening/hole through dielectric layer 56 allows n-contact metal 58 to make electrical contact and form an n-type conductive path of the semiconductor light emitting device. (*Id.*, ¶¶[0034]-[0035], FIG. 6.)

2. Claim 1

a. A light emitting device, comprising:

To the extent the preamble is limiting, *Epler* discloses this limitation. (Ex. PA-DEC, ¶46.) For example, *Epler*, which relates to LED technologies (*e.g.*, Ex. PA-1, Abstract, FIGs. 1, 6, ¶¶[0001]-[0002]), discloses a "semiconductor light emitting device." (*Id.*, ¶¶[0034]-[0035], FIGs. 6-7.) The device includes a light emitting region and emits "rays of light." (*Id.*, ¶¶[0030], [0034].) An example semiconductor light emitting device is illustrated in Figure 6. (*Id.*, ¶[0017].)

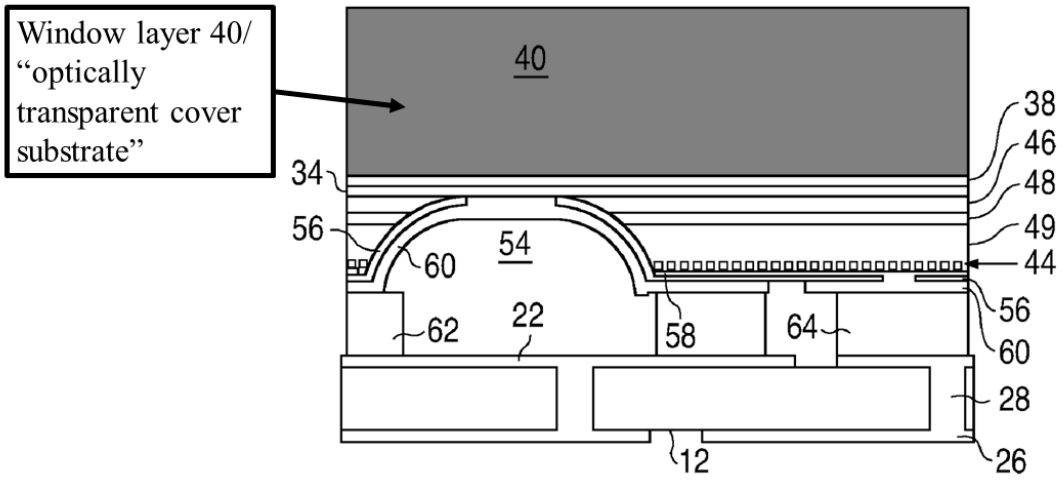


(*Id.*, FIG. 6.) A similar device with a different mounting configuration is illustrated in Figure 7. (*Id.*, FIG. 7, ¶¶[0017]-[0018].)

b. an optically transparent cover substrate;

Epler discloses this limitation. (Ex. PA-DEC, ¶¶47-49.) For example, *Epler* discloses a "window layer 40" ("optically transparent cover substrate") that may be a "**transparent substrate**." (Ex. PA-1, ¶[0026] (emphasis added), FIG. 6.) Light is configured to pass through window layer 40 as an "optically transparent" material. (*Id.*, ¶[0027] ("For example, a red-emitting phosphor may be disposed in bonding layer 38, and a yellow- or green-emitting phosphor such as cerium-doped yttrium aluminum garnet may be disposed in or on window layer 40, such that the composite light emitted from the device appears warm white. Alternatively, a mixture of phosphors may be disposed in a silicone bonding layer 38, to provide the desired spectrum. In such devices, window layer 40 may be transparent."); Ex. PA-DEC, ¶47.)

Window layer 40 is bonded to the semiconductor light emitting device during manufacturing and is a cover that overlays the remaining components of the semiconductor light emitting device. (Ex. PA-1, FIGs. 4, 6, ¶¶[0017], [0026], [0034]; Ex. PA-DEC, ¶48.)



(Ex. PA-1, FIG. 6 (annotated); Ex. PA-DEC, ¶48.)

The transparent window layer 40 also provides mechanical support to the semiconductor light emitting device (Ex. PA-1, ¶¶[0026]-[0027], [0039] ("Since window layer 40 provides mechanical support to the semiconductor structure during and after removal of the growth substrate, a package substrate or other mount is not required.")), which is consistent with how the transparent cover substrate is described in the '822 patent (Ex. PAT-A, 5:20-25 ("The cover substrate 655 provides structural presence and mechanical coupling for elements of the LED

device 60. The cover substrate 655 is also transparent or optically permissive to light in the wavelength emitted by LED layer 600 and Phosphor layer.")).

c. an optically transparent layer attached to a bottom surface of said optically transparent cover substrate, said optically transparent layer including an optically definable material;

Epler discloses or suggests this limitation. (Ex. PA-DEC, ¶¶50-56.)

Bonding layer 34 alone and in combination with bonding layer 38 each discloses "an optically transparent layer," as claimed. (Ex. PA-DEC, ¶51.) For example, *Epler* discloses a "bonding layer 34" ("optically transparent layer"). (Ex. PA-1, ¶[0024], FIG. 6.) Bonding layer 34 is formed of "transparent" material such that it has a "minimal[]" impact on the wavelength of the light that is emitted from the semiconductor light emitting device. (*Id.*) *Epler* discloses that "[s]uitable materials" for bonding layer 34 "include, for example, transparent conductive oxides such as indium tin oxide (ITO), zinc oxide, and ruthenium oxide." (*Id.*)

In addition, the material consisting of bonding layer 34 and 38 also comprise an "optically transparent layer," as claimed. (Ex. PA-DEC, ¶52.) For instance, *Epler* discloses that the bonding layer 38 "may be the same material as bonding layer 34" (Ex. PA-1, ¶[0027], FIG. 6), and is therefore optically transparent for the previously discussed reasons (*id.*, ¶[0024]). Furthermore, *Epler* discloses that a variety of suitable "transparent" materials can be used for bonding layer 38 and refers to 38 as a "transparent bonding layer 38." (*Id.*, ¶¶[0024], [0027].) *Epler* also discloses that bonding layers 34 and 38 are "bonded" together "for example by anodic bonding, direct bonding via plasma preparation of hydrophilic surfaces, or bonding via use of an intermediate bonding layer" and, accordingly, form a transparent layer of the semiconductor light emitting device. (*Id.*, ¶[0027-28], FIG. 6; Ex. PA-DEC, ¶52.) The material comprising 34 and 38 is a "layer" under the broadest reasonable interpretation. (Ex. PA-DEC, ¶52.) For example, a layer may include a thickness of material, and material that constitutes a "layer" does not become multiple layers simply because a manufacturer decided to deposit it in multiple steps rather than in a single step. (*Id.*)

Epler discloses that bonding layers 34 and 38 may be "attached to a bottom surface of said optically transparent cover substrate," as claimed. (Ex. PA-DEC, ¶53.) Bonding layer 38 is an optional material that can be included in the semiconductor light emitting device "[i]f conductive bonding layer 34 and window layer 40 are not suitable for bonding." (Ex. PA-1, ¶[0027]; Ex. PA-DEC, ¶53.) Indeed, *Epler* discloses that bonding layer 38 "may be the same material as bonding

layer 34," which also denotes that bonding layer 38 is an optional layer. (Ex. PA-1, ¶[0027]; Ex. PA-DEC, ¶53.) When the *Epler* semiconductor light emitting device includes bonding layers 34 and 38, bonding layer 38 may be "formed on window layer 40" ("optically transparent cover substrate") such that it is attached to a bottom surface of said optically transparent cover substrate. (Ex. PA-1, ¶[0027].) Figures 4-6 illustrate the fabrication of a "bonded structure," wherein bonding layer 38 of the semiconductor light emitting device attaches to the bottom of window layer 40 ("optically transparent cover substrate"). (Ex. PA-1, ¶¶[0016], [0020], FIGs. 4-6; Ex. PA-DEC, ¶53.)

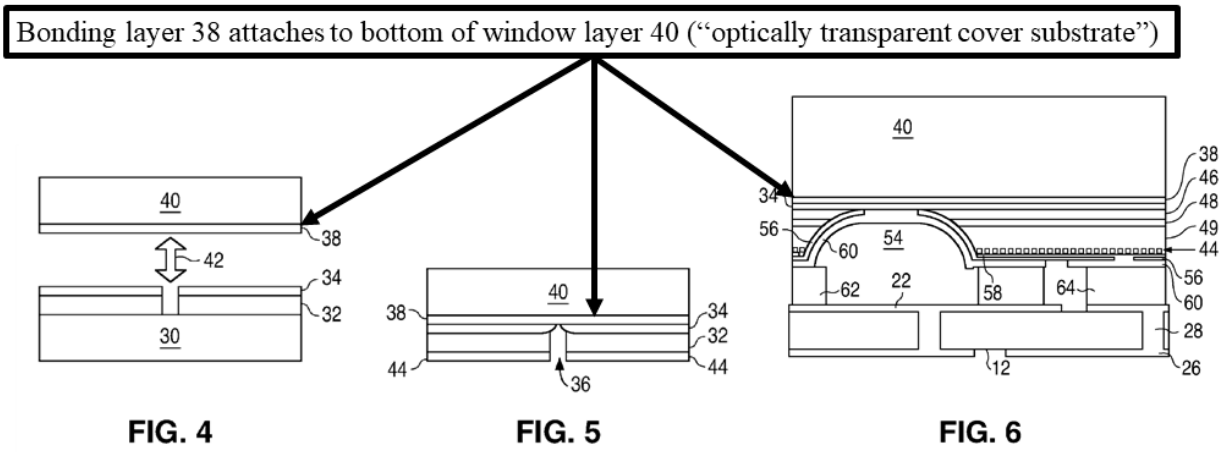


FIG. 4 FIG. 5 FIG. 6

(Ex. PA-1, FIGs. 4-6 (annotated); Ex. PA-DEC, ¶53.)

When the *Epler* semiconductor light emitting device does not include bonding layer 38, bonding layer 34, which may be the same material as bonding layer 38, would be attached to the bottom of the window layer 40 as described with respect to layer 38. (Ex. PA-1, ¶¶[0016], [0020], [0027], FIGs. 4-6; Ex. PA-DEC, ¶54.)

Epler discloses that the bonding layer 38 material may "includ[e] an optically definable material," as claimed, at least because the bonding material may include one or more phosphors to help shape the color of emitted light. (Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶55.) "For example, a red-emitting phosphor may be disposed in bonding layer 38" to allow the light emitted from the device to appear warm white. (Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶55.) "Alternatively, a mixture of phosphors may be disposed in a silicone bonding layer 38, to provide [a] desired spectrum." (Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶55.) This disclosure is

consistent with the '822 patent, which also discloses a similar phosphor-based configuration. (Ex. PAT-A, 5:9-16.)

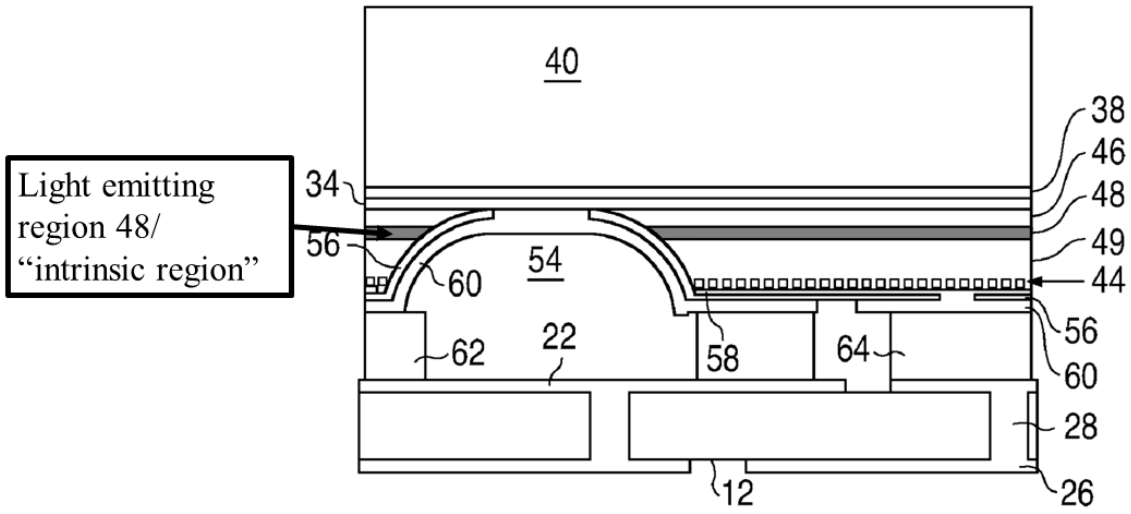
Additionally, because *Epler* discloses that bonding layer 34 and bonding layer 38 can be the same material, *Epler* discloses that layer 34 may also include one or more phosphors ("optically definable material"). (Ex. PA-1, ¶[0027].) To the extent *Epler* does not explicitly disclose that bonding layer 34 may include such a phosphor, the configuration would have been obvious. (Ex. PA-DEC, ¶56.) Adding a phosphor to bonding layer 34 would have yielded similar lighting benefits to those described with respect to bonding layer 38 and could have easily been manufactured by a POSITA in a similar way. (*Id.*, ¶[0027]; Ex. PA-DEC, ¶56.) *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007).

d. a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region, and a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer;

Epler discloses this limitation. (Ex. PA-DEC, ¶¶57-60.) *Epler* discloses "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region," as claimed. (Ex. PA-DEC, ¶57.) For instance, *Epler* discloses an "n-type region 49," which includes a "porous region 44," a "light emitting region 48" (an active region), and a "p-type region 46," which together comprise a semiconductor LED. (Ex. PA-1, ¶¶[0034], [0020], [0030]; Ex. PA-DEC, ¶57; *see generally* Ex. PA-1, ¶¶[0001]-[0002] (describing a semiconductor LED as including an n-type layer, an active layer, a p-type layer).) A person of ordinary skill in the art ("POSITA") would have understood that p-type region 46 refers to a positively doped semiconductor material ("positively-doped region") and that n-type region refers to a negatively doped semiconductor material ("negatively-doped region"). (Ex. PA-1, ¶¶[0021]-[0023], [0032]; Ex. PA-4, 1:61-65 ("electron 'holes' become the charge carriers and the doped silicon is referred to as positive or P-type silicon . . . additional electrons become the charge carriers and the doped silicon is referred to as negative or N-type silicon"); Ex. PA-5, ¶¶[0003]-[0005]; Ex. PA-DEC, ¶57.) *Epler* discloses that light emitting/active region 48 "may be doped . . . [or] **not intentionally doped**" and so does not include the n-type or p-type doping of layers 46 and 49. (Ex. PA-1, ¶¶[0022] (emphasis added), [0034]; Ex. PA-DEC, ¶57.) Indeed, *Epler* explains that a "not intentionally doped" region refers to region with a "dopant concentration [of] zero" (i.e., the region is not doped at all). (Ex. PA-1,

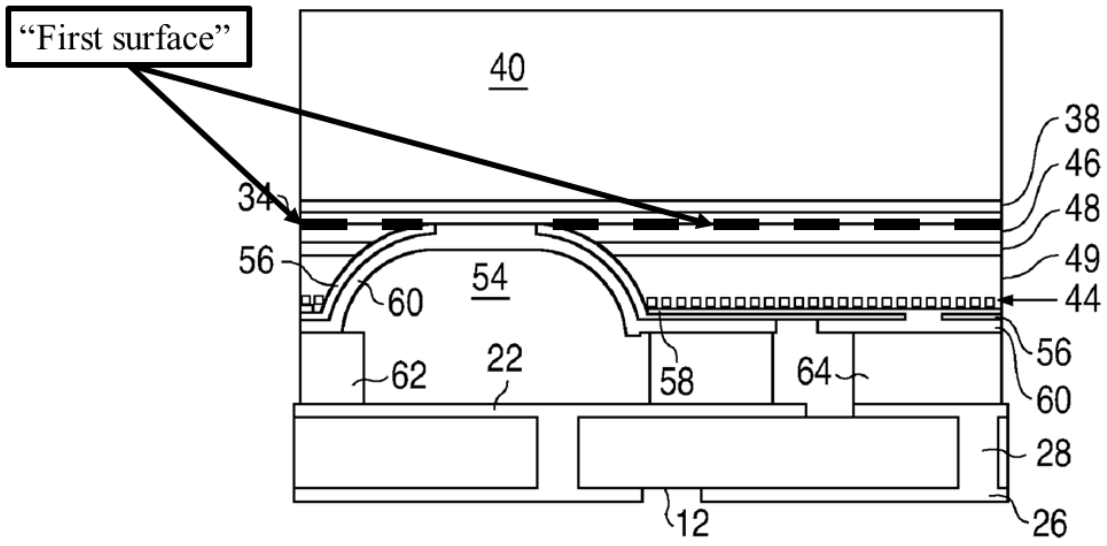
¶[0032].) Because *Epler* discloses that light emitting/active region 48 may not be doped, such that it has a dopant concentration of zero, light emitting/active region 48 discloses an "intrinsic region" under the broadest reasonable interpretation. (Ex. PA-DEC, ¶57.)

Epler discloses that "wherein said intrinsic region is between said positively-doped region and said negatively-doped region," as claimed. (Ex. PA-DEC, ¶58.) For instance, *Epler* discloses that "[t]he light emitting region is grown over the n-type region" and that "the p-type region is grown over the light emitting region." (Ex. PA-1, ¶¶[0023], [0034]; Ex. PA-DEC, ¶58.) Figure 6 illustrates this configuration, wherein the light emitting region 48 is sandwiched between the p-type region 46 and n-type region 49:



(Ex. PA-1, FIG. 6 (annotated); Ex. PA-DEC, ¶58).

Epler discloses that "a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer," as claimed. (Ex. PA-DEC, ¶59.) For instance, referring to the fabrication process depicted in Figures 2-5, *Epler* discloses that "bonding layer 34 is formed over the top layer of semiconductor structure 32, generally the p-type region, using a conventional thin-film deposition technique such as vacuum evaporation, sputtering, and electron beam deposition." (Ex. PA-1, ¶[0024].) Additionally, the bottom of 34 and top of p-type region 46 (which is part of semiconductor structure 32 in Figures 2-5) are in contact such that "[c]onductive bonding layer 34 serves as the electrical contact to the p-type region." (*Id.*, ¶[0034].) Figure 6 also illustrates how a first surface of p-type region 46 of the semiconductor LED contacts the bottom of 34:



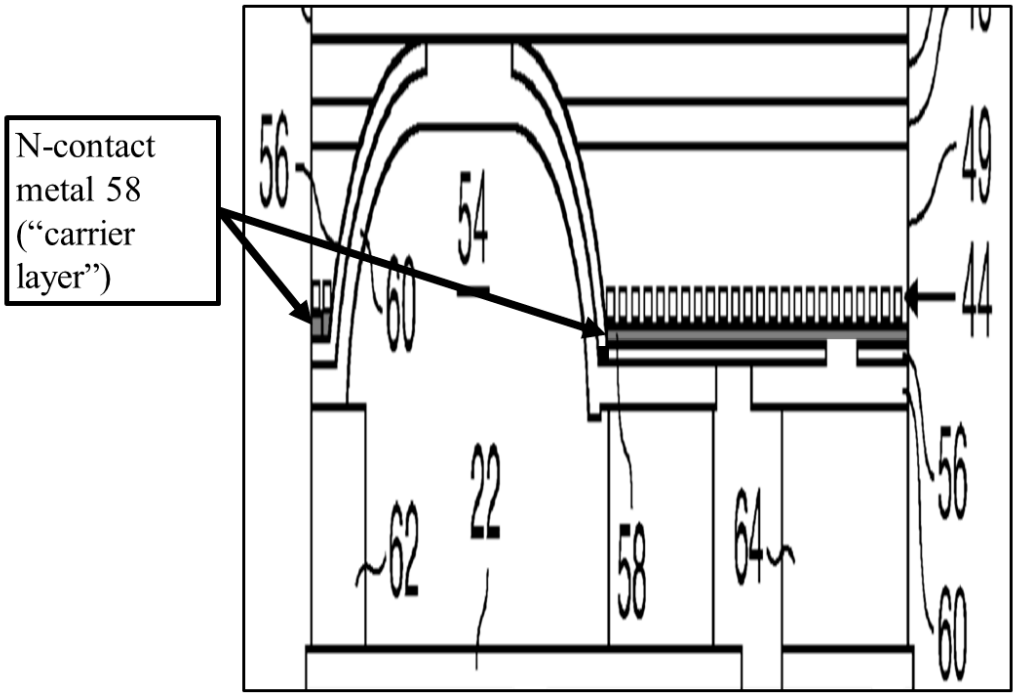
(Ex. PA-1, FIG. 6 (annotated); Ex. PA-DEC, ¶59).

Bonding layer 34 would similarly contact the first surface of p-type region 46 in the embodiment wherein the semiconductor light emitting device does not include optional bonding layer 38. (Ex. PA-1, ¶¶[0024], [0027], [0034], FIG. 6; Ex. PA-DEC, ¶60.)

e. a carrier layer proximal to a second surface of said semiconductor LED, said first and second surfaces on opposing sides of said semiconductor LED;

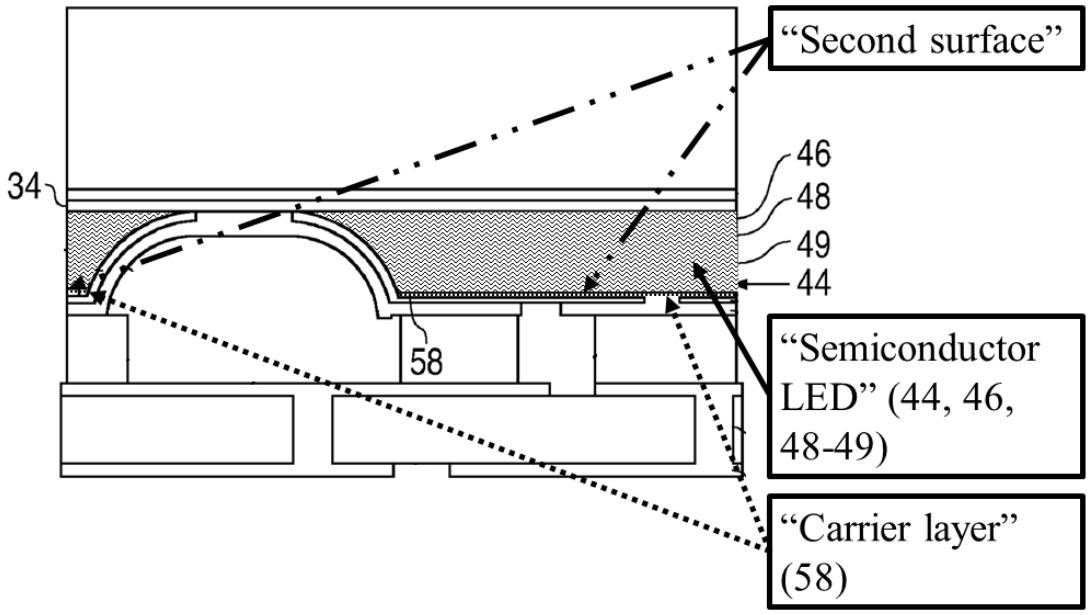
Epler discloses this limitation, based at least on the broadest reasonable interpretation of the term "carrier layer." (Ex. PA-DEC, ¶¶61-63.) For example, *Epler* describes an "[n]-contact metal 58" formed on a porous layer 44 of the n-type region 49 (porous layer 44 is a pitted section of n-type region 49). (Ex. PA-1, ¶¶[0034]-[0035], [0032], FIG. 6; Ex. PA-DEC, ¶61.) N-contact metal 58 is configured to conduct electricity. (Ex. PA-1, ¶¶[0011], [0034]-[0035], FIGs. 6-7; Ex. PA-DEC, ¶61.) The N-contact metal 58 meets the term "carrier layer" under the broadest reasonable interpretation, at least because it supports the base of the semiconductor LED (i.e., layers 44, 46, 48, and 49). (Ex. PA-1, ¶¶[0011], [0034]-[0035], FIGs. 6-7; Ex. PA-DEC, ¶61.) In fact, Patent Owner has applied the "carrier layer" term broadly in district court, as evidenced by Patent Owner's infringement allegations, which allege that even a thin metal interconnect layer corresponds to the claimed "carrier layer." (Ex. LIT-3, 11-12 (asserting that a copper interconnect layer is a carrier layer); Ex. PA-DEC, ¶61.) *See Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (citation omitted) ("A patent may not, like a 'nose of wax,' be twisted one way to avoid anticipation and another to find infringement."). Thus, the annotated

portion of Figure 6 below, which corresponds to n-contact metal 58, discloses the claimed "carrier layer," based on Patent Owner's infringement allegations. (Ex. PA-DEC, ¶61.)



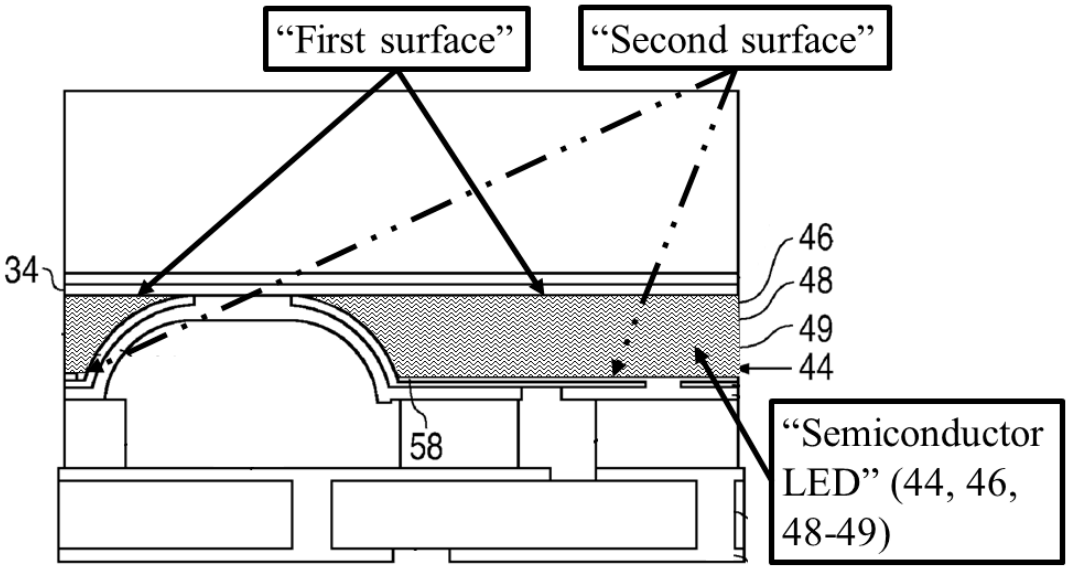
(Ex. PA-1, ¶[0034], FIG. 6 (excerpted, enlarged, and annotated); Ex. PA-DEC, ¶61.)

As illustrated below, the n-contact metal 58 illustrated above ("carrier layer") is "proximal to a second surface of said semiconductor LED," as claimed. (Ex. PA-DEC, ¶62.) For instance, *Epler* discloses that "[n]-contact metal 58 is **formed on the remaining part of porous region 44**" of the semiconductor LED after an opening is etched through layers 44, 46, 48, and 49 to expose bonding layer 34. (Ex. PA-1, ¶[0034] (emphasis added), FIGs. 6-7; Ex. PA-DEC, ¶62.) Layering 58 on the remaining part of 44 (which includes the bottom of the "semiconductor LED" (*see supra* §VI.A.2.d)) layers 58 "proximal to a second surface of said semiconductor LED," as claimed:



(Ex. PA-1, FIG. 6 (annotated), ¶[0034]; Ex. PA-DEC, ¶62).

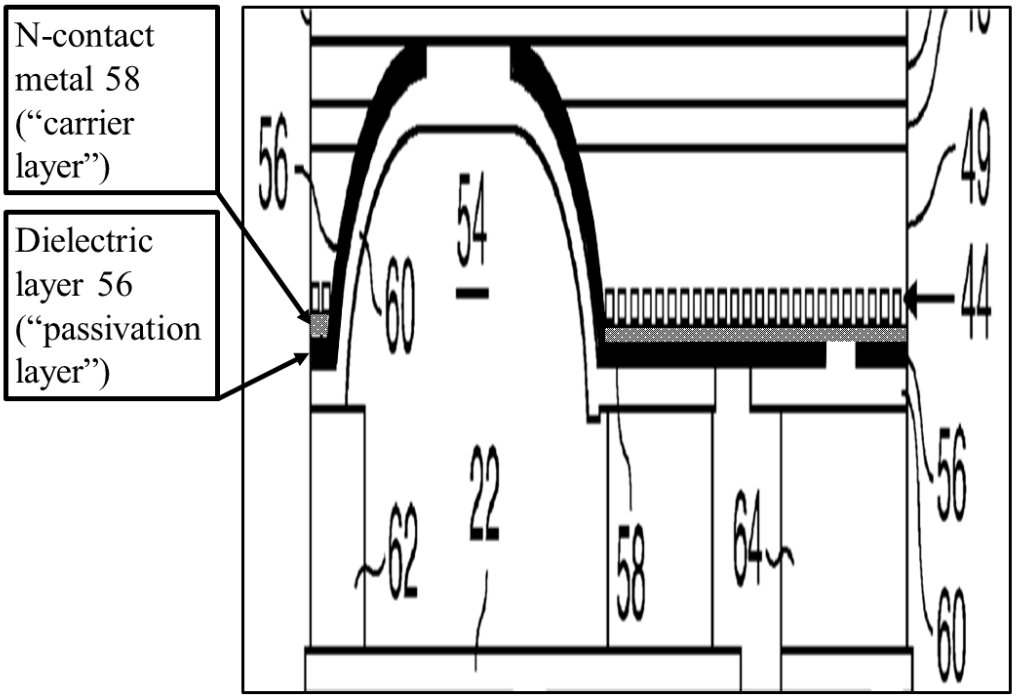
As illustrated in Figure 6 and described, the top of the p-type region 46 ("first surface") of the semiconductor LED and the bottom of the porous region 44 ("second surface") of the semiconductor LED are on "opposing sides," as claimed:



(Ex. PA-1, ¶[0034], FIG. 6 (annotated); Ex. PA-DEC, ¶63).

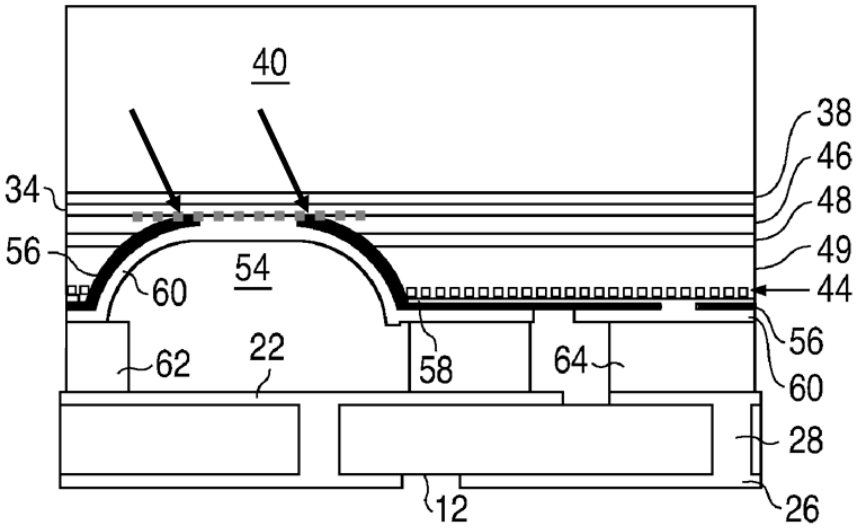
f. a passivation layer disposed on said carrier layer and on an exposed portion of said bottom surface of said optically transparent layer;

Epler discloses this limitation. (Ex. PA-DEC, ¶¶64-65.) For instance, *Epler* discloses "dielectric layer 56" ("passivation layer"). (Ex. PA-1, ¶[0034]; Ex. PA-DEC, ¶64.) Dielectric layer 56 "electrically isolate[s]" n-contact metal 58 ("carrier layer") to ensure that the recombination of electrical carriers occurs in the radiative region, and, as shown in Figure 6, is "disposed on" the portion of n-contact metal 58 discussed above in Section VI.A.2.e ("said carrier layer"):



(Ex. PA-1, ¶[0034], FIG. 6 (excerpted, enlarged, and annotated); Ex. PA-DEC, ¶64.) Indeed, *Epler* explains that the dielectric layer 56 may be composed of a "SiN_x" material, consistent with the '822 patent. (Ex. PA-1, ¶¶[0034], [0039]; Ex. PAT-A, ("The passivation layer 1170 can comprise a non conductive layer and can be composed of . . . SiN.").) Additionally, given *Epler*'s explanation that n-contact metal 58 "is formed on" porous region 44, and the fact that dielectric layer 56 is illustrated proximate to n-contact metal 58 in Figure 6, a POSITA would have understood that dielectric layer 56 is formed on ("disposed on") the portion of n-contact metal 58 discussed above in Section VI.A.2.e ("carrier layer") after that portion of n-contact metal 58 is formed on region 44. (Ex. PA-1, ¶[0034], FIG. 6; Ex. PA-DEC, ¶64.)

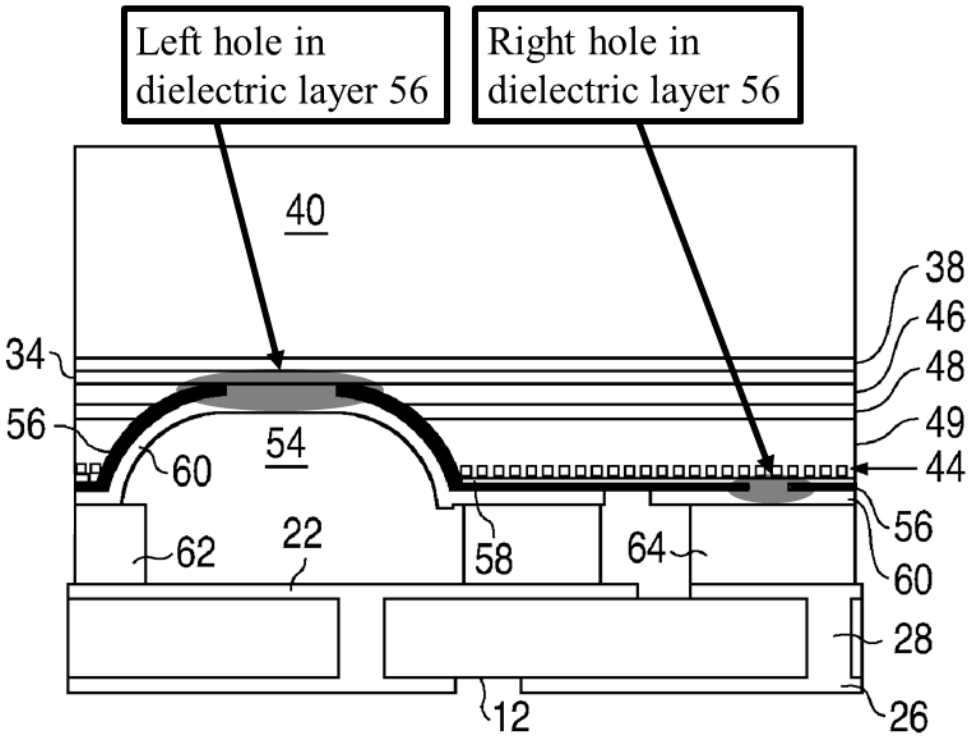
Epler further discloses that the dielectric layer 56 ("passivation layer") is "on an exposed portion of said bottom surface of said optically transparent layer," as claimed. (Ex. PA-DEC, ¶65.) For instance, *Epler* discloses that "one or more openings which expose bonding layer 34 are etched through the semiconductor structure." (Ex. PA-1, ¶¶[0034].) After the bottom of bonding layer 34 is exposed, "contacts are formed." (*Id.*) As a part of the contact formation process and illustrated by the below dotted line, dielectric layer 56 is layered on a portion of the exposed bottom of bonding layer 34:



(Ex. PA-1, ¶[0034], FIG. 6 (annotated); Ex. PA-DEC, ¶65). Thus, dielectric layer 56 ("passivation layer") is "on an exposed portion of said bottom surface of" bonding layer 34 and accordingly on the bottom of the "optically transparent layer." (Ex. PA-1, ¶[0034], FIGs. 6-7; Ex. PA-DEC, ¶65.)

g. a first electrical contact disposed on said carrier layer in a first contact hole defined in said passivation layer; and

Epler discloses this limitation. (Ex. PA-DEC, ¶¶66-70.) For instance, *Epler* discloses "a first contact hole defined in said passivation layer," as claimed. (*Id.*, ¶66.) As shown in annotated Figure 6 below, dielectric layer 56 ("passivation layer") does not cover the entire length of the semiconductor light emitting device. (Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶66.) Rather, dielectric layer 56 includes two openings, a left opening and a right opening ("hole defined in said passivation layer"):

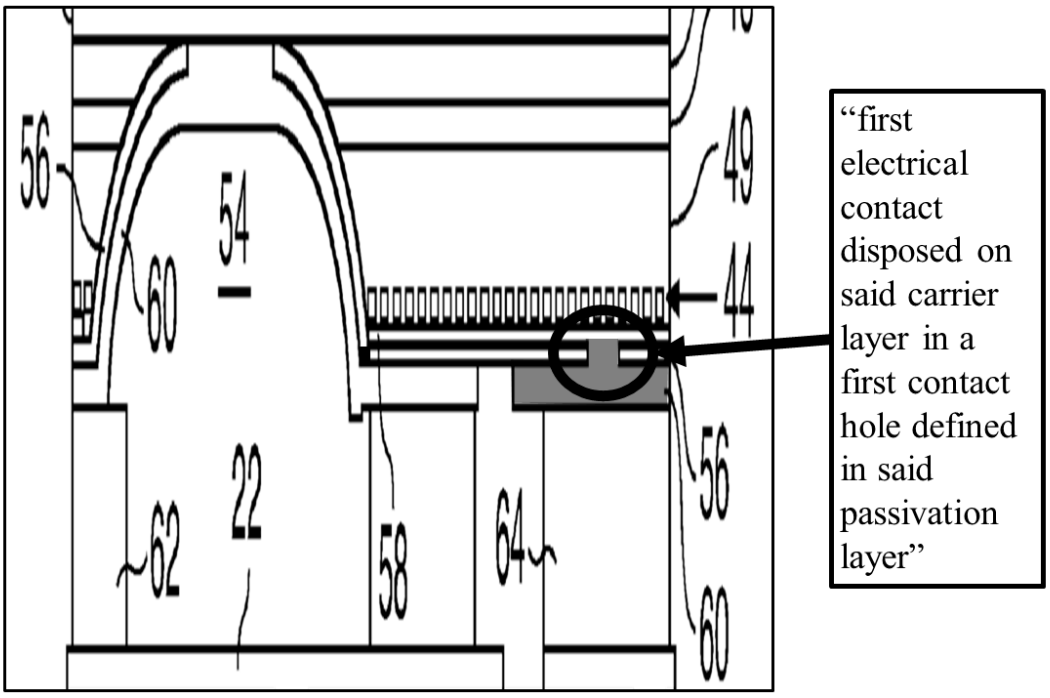


(Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶66.)

A "first electrical contact," as claimed, is formed in the right hole in dielectric layer 56 ("passivation layer"). (Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶67.) As disclosed by *Epler* and further explained in the following paragraphs, after creation of the hole on the right-hand side of the dielectric layer 56, an additional portion of n-contact metal 58 illustrated in annotated Figure 6 below is formed such that an electrical contact ("first electrical contact") is formed in the hole with the portion of n-contact metal 58 discussed above in Section VI.A.2.e ("carrier layer").[3] (Ex. PA-1, ¶¶[0030], [0034]-[0035], FIG. 6; Ex. PA-DEC, ¶67.) Thus, a

[3] In addition to label 58, Figure 6 includes a label 60 for the same n-contact metal region. Based on *Epler*'s disclosure, a POSITA would have understood that this inclusion of label 60 is a typographical error. (Ex. PA-DEC, ¶67.) For example, in the specification, 60 refers to a "p-contact metal," which a POSITA would have understood corresponds to the p-contact region on the left side of the device illustrated in Figure 6, not the n-contact region on the right side of the device illustrated in Figure 6. (Ex. PA-1, ¶¶[0034]-[0035], [0020]-[0023], FIG. 6; Ex. PA-DEC, ¶67.) In fact, Figure 6 already includes a separate label 60 for the p-contact metal on the left side of the device illustrated in Figure 6. (Ex. PA-1, FIG. 6.) Additionally, Figure 7, which illustrates a device that is similar to the device in Figure 6 except without a package substrate, does not include label 60 for the n-contact metal region that is also identified by label 58. (Ex. PA-1,

conductive path to the n-type region 49 is formed via an n-path top-side contact 22 (which is not labeled in the below figure), bottom-side contact 26, conductive pillar 28, and n-interconnect 64. (Ex. PA-1, ¶¶[0030], [0034]-[0035], FIG. 6; Ex. PA-DEC, ¶67.)



(Ex. PA-1, ¶¶[0034]-[0035], FIG. 6 (excerpted, enlarged, and annotated) (illustrating a "first electrical contact" formed in the right hole in dielectric layer 56 ("passivation layer")); Ex. PA-DEC, ¶67.)

A POSITA would have understood that the two portions of n-contact metal 58 are formed by first forming the portion of n-contact metal 58 discussed above in Section VI.A.2.e (the claimed "carrier layer"), then forming passivation layer 56 and the contact holes in passivation layer 56, and finally forming the portion of n-contact metal 58 discussed above in this Section. (Ex. PA-DEC, ¶68.) This is the case because each portion of n-contact metal 58 and dielectric layer 56 must be formed in sequence, consistent with known semiconductor fabrication techniques available at the time. (*Id.*; *see generally* Ex. PA-27, FIG. 3, ¶[0047] (explaining that after an n-electrode is formed "a transparent, nonconductive passivation layer 47 is formed . . . to protect the light emitting diode chip" and that thereafter "portions of the passivation layer are punched so as

¶[0039], FIG. 7; Ex. PA-DEC, ¶67.) Thus, a POSITA would have understood that label 58 also refers to the right n-contact metal region erroneously marked as 60 on the right side of the device illustrated in Figure 6. (Ex. PA-DEC, ¶67.)

to expose" the n-electrode in operation 305); Ex. PA-28, ¶[0037] (explaining that LED manufacturing "includes depositing a dielectric layer 32 in which vias 34 are formed to provide access to the . . . the n-type electrode 14, followed by metallization processing that fills the vias 34 with an electrically conductive material 36 and that forms intermediate connecting pads, specifically . . . an intermediate n-type connecting pad 44"); Ex. PA-29, ¶[0056] ("forming an insulation layer on the substrate having the n-type electrodes 64 and the p-type electrode pads 66 as shown in FIG. 7. Thereafter, the insulation layer is patterned through a photolithography and etching process to form openings exposing the n-type electrodes 64 and the p-type electrode pads 66. Subsequently, through an e-beam evaporation technology, the openings are filled and the metal layer covering the top surface of the insulation layer is formed.").

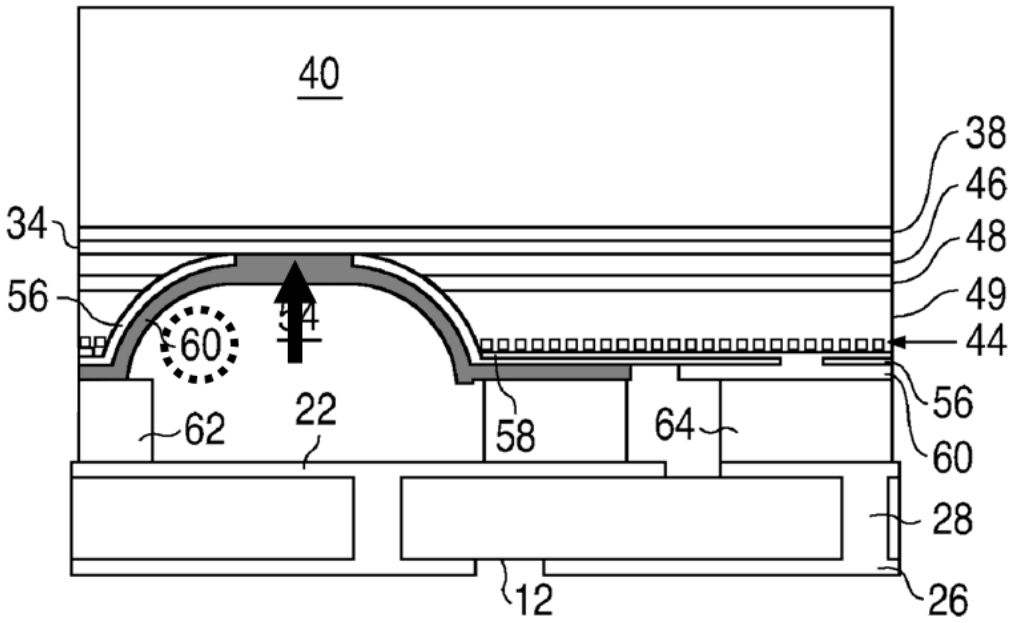
Alternatively, this limitation would have been obvious, because a POSITA would have had good reason to form two portions of n-contact metal 58 by, first, forming the portion of n-contact metal 58 discussed above in Section VI.A.2.e (the claimed "carrier layer"), second, forming passivation layer 56, third, forming contact holes in passivation layer 56, and, finally, forming the portion of n-contact metal 58, including within the right hole in the passivation layer 56, to form the claimed "first electrical contact." (Ex. PA-DEC, ¶69.) N- and p-region connections were routinely formed by first depositing metals on n- and p-type materials, and thereafter layering additional metal on the deposited metal through an insulation, via/etching, etc., process. (*Id.*; *see generally* Ex. PA-27, FIG. 3, ¶[0047] (explaining that after an n-electrode is formed "a transparent, nonconductive passivation layer 47 is formed . . . to protect the light emitting diode chip" and that thereafter "portions of the passivation layer are punched so as to expose" the n-electrode in operation 305); Ex. PA-28, ¶[0037] (explaining that LED manufacturing "includes depositing a dielectric layer 32 in which vias 34 are formed to provide access to the . . . the n-type electrode 14, followed by metallization processing that fills the vias 34 with an electrically conductive material 36 and that forms intermediate connecting pads, specifically . . . an intermediate n-type connecting pad 44"); Ex. PA-29, ¶[0056] ("forming an insulation layer on the substrate having the n-type electrodes 64 and the p-type electrode pads 66 as shown in FIG. 7. Thereafter, the insulation layer is patterned through a photolithography and etching process to form openings exposing the n-type electrodes 64 and the p-type electrode pads 66. Subsequently, through an e-beam evaporation technology, the openings are filled and the metal layer covering the top surface of the insulation layer is formed."); Ex. PA-11, ¶[0036]; Ex. PA-37, ¶¶[0049]-[0050].). A POSITA would have

had good reason to manufacture the n-contact metal 58 in this fashion, including to reduce costs by using established and widely-available methods to manufacture such devices; to simply manufacturing by using established and reliable methods to manufacture such devices; to electrically isolate the p- and n-contacts; and to improve the thermal performance of the device and yield. (Ex. PA-DEC, ¶69; Ex. Pa-11, ¶¶[0011], [0037]; Ex. PA-27, ¶[0020] Ex. PA-28, ¶[0037]; Ex. PA-29, ¶[0056].)

Because *Epler* teaches or suggests that the disclosed "first electrical contact" is formed on the portion of n-contact metal 58 discussed above in Section VI.A.2.e ("carrier layer") inside the hole in dielectric layer 56 ("passivation layer") *Epler* discloses or renders obvious that the "first electrical contact" is "disposed on said carrier layer in a first contact hole defined in said passivation layer," as claimed. (Ex. PA-DEC, ¶70.) Indeed, *Epler* discloses that the left opening/hole allows the left p-contact metal 60 to make electrical contact with bonding layer 34 and form a p-type conductive path of the semiconductor device. (Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶70.) In a similar fashion, *Epler* discloses that the right hole allows the n-contact metal 58 to form the n-type conductive path of the semiconductor light emitting device. (Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶70.) This disclosure is consistent with the '822 patent, which describes a similar contact 1472 in Figure 14. (Ex. PAT-A, 7:16-22, FIG. 14; Ex. PA-DEC, ¶70.)

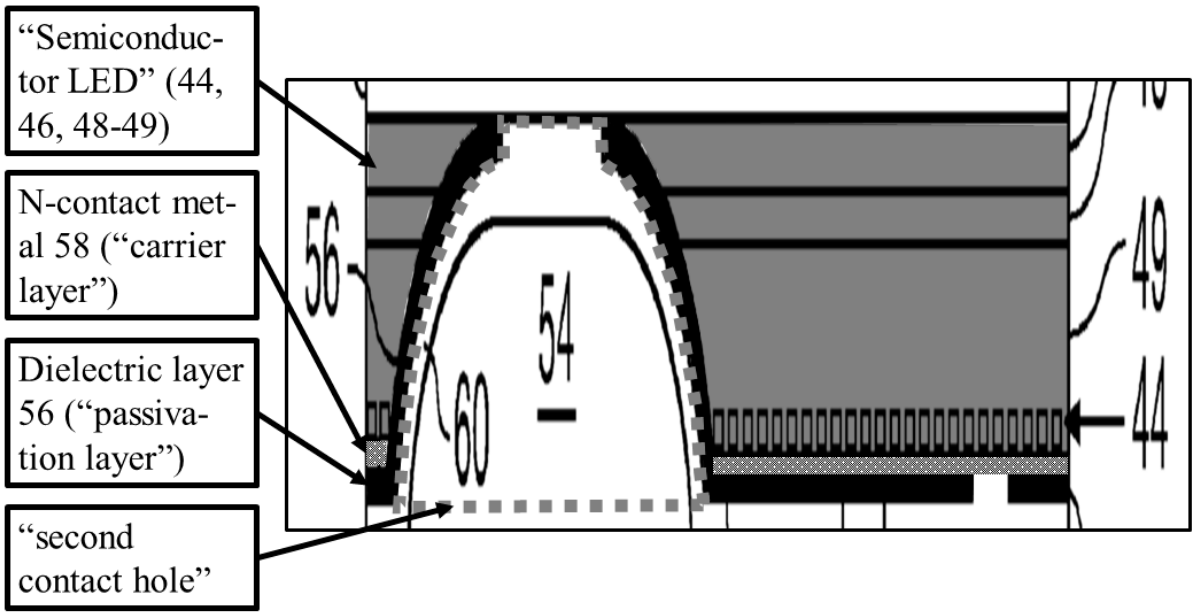
h. a second electrical contact disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED, said second electrical contact in electrical communication with said first surface of said semiconductor LED.

Epler discloses this limitation. (Ex. PA-DEC, ¶¶71-73.) For instance, *Epler* discloses "p-contact metal 60" forming a contact with bonding layer 34 ("second electrical contact") in opening 54 ("second contact hole"). (Ex. PA-1, ¶¶[0034]-[0035], FIG. 6; Ex. PA-DEC, ¶71.) P-contact metal 60 makes electrical contact with p-interconnects 62 and bonding layer 34 to form a conductive path to the p-type region 46 via top-side contact 22, a p-path bottom-side contact 26 (which is not labeled in the below figure), and a p-path conductive pillar 28 (which is not labeled in the below figure). (Ex. PA-1, ¶¶[0024], [0030], [0034]-[0035], FIG. 6; Ex. PA-DEC, ¶71.)



(Ex. PA-1, ¶¶[0034]-[0035], FIG. 6 (annotated) (illustrating a p-type electrical contact); Ex. PA-DEC, ¶71.)

Epler's p-contact metal 60 is "disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED," as claimed. (Ex. PA-DEC, ¶72.) For instance, *Epler* discloses that "[a]n opening 54 is etched through porous region 44, non-porous n-type region 49, light emitting region 48, and p-type region 46" (which together comprise the semiconductor LED (*see supra* §VI.A.2.d)) "to expose conductive bonding layer 34." (Ex. PA-1, ¶[0034]; Ex. PA-DEC, ¶72.) Furthermore, *Epler* discloses that n-contact metal 58 "is formed on the remaining part of porous region 44" such that the opening extends through the carrier layer and the semiconductor LED. (Ex. PA-1, ¶[0034]; Ex. PA-DEC, ¶72; *see supra* §VI.A.2.e.) Figure 6 also illustrates that an etching through porous region 44, non-porous n-type region 49, light emitting region 48, and p-type region 46 (the semiconductor LED) is partially lined with dielectric layer 56. (Ex. PA-1, FIG. 6, dielectric layer 56); Ex. PA-DEC, ¶72.) As illustrated in Figure 6, the dielectric layer 56 ("passivation layer") includes a second contact hole, wherein p-contact metal 60 is layered on dielectric layer 56 and makes contact with bonding layer 34 such that p-contact metal 60, forming "a second electrical contact" that is "disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED," as claimed. (Ex. PA-1, ¶[0034]; Ex. PA-DEC, ¶72.)



(Ex. PA-1, ¶¶[0034]-[0035], FIG. 6 (excerpted, enlarged, and annotated) (illustrating a second contact hole that p-contact metal 60 ("second electrical contact") is disposed in); Ex. PA-DEC, ¶72.)

The disclosed "second electrical contact" is also "in electrical communication with said first surface of said semiconductor LED," as claimed. (Ex. PA-DEC, ¶73.) The first surface of the semiconductor LED refers to a surface of p-type region 46. (*See supra* §§VI.A.2.c-d; Ex. PA-1, ¶[0034], FIG. 6.) *Epler* further discloses that "[c]onductive bonding layer 34 serves as the electrical contact to the p-type region" 46. (Ex. PA-1, ¶¶[0034], [0024], FIG. 6.) Because the first surface of p-type region 46 is in physical and electrical contact with conductive bonding layer 34 and p-contact metal 60 is "formed on the exposed portion of conductive bonding layer 34," the p-contact metal 60 ("second electrical contact") is "in electrical communication with said first surface of said semiconductor LED," as claimed. (Ex. PA-1, ¶[0034], FIG. 6; Ex. PA-DEC, ¶73.) Indeed, a POSITA would have understood that this configuration allows the semiconductor light emitting device to comprise a p-type electrical region (as illustrated above) for lighting purposes. (Ex. PA-1, ¶[0034], FIG. 6; Ex. PA-DEC, ¶73.) For similar reasons, p-contact metal 60 is an "electrical contact that is in a conduction path with the first surface of the semiconductor LED" consistent with Seoul Semiconductor's proposed construction in district court. (*See supra* §IV; Ex. PA-1, ¶¶[0034], [0024], FIG. 6; Ex. PA-DEC, ¶73.) This disclosure is consistent with the '822

patent, which describes similar contact 1472 in Figure 14. (Ex. PAT-A, 7:16-22, FIG. 14; Ex. PA-DEC, ¶73.)

3. Claim 2

a. The light emitting device of claim 1 wherein said optically definable material is disposed in a portion of said optically transparent layer.

Epler discloses this limitation. (Ex. PA-DEC, ¶74.) As discussed previously, bonding layer 34 and the material consisting of bonding layer 34 and 38 each comprises an "optically transparent layer." (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶74.) Further, the "optically definable material" may be a phosphor, as disclosed by *Epler*. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], [0034], FIG. 6; Ex. PA-DEC, ¶74.) *Epler* further discloses that the "wavelength converting material"/"phosphor may be disposed in bonding layer 38" ("disposed in a portion of said optically transparent layer"). (Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶74.) As explained previously, layer 34 may also include phosphor, because *Epler* discloses that layer 34 may comprise the same material as layer 38. (*See supra* §VI.A.2.c; Ex. PA-DEC, ¶74.) Disposing such a phosphor in the optically transparent layer shapes and defines the light spectrum that is emitted from the semiconductor light emitting device. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶74.)

4. Claim 5

a. The light emitting device of claim 2 wherein said optically definable material is embedded in said portion of said optically transparent layer.

Epler discloses this limitation. (Ex. PA-DEC, ¶75.) As discussed previously, bonding layer 34 and the material consisting of bonding layer 34 and 38 each comprises an "optically transparent layer." (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶75.) Further, the "optically definable material" may be a phosphor, as disclosed by *Epler*. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶75.) *Epler* further discloses that the "wavelength converting material"/"phosphor may be disposed in bonding layer 38" ("embedded in said portion of said optically transparent layer"). (Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶75.) As explained previously, layer 34 may also include phosphor, because *Epler* discloses that layer 34 may comprise the same material as layer 38. (*See supra* §VI.A.2.c; Ex. PA-DEC, ¶75.) Disposing such a phosphor in the optically transparent layer shapes and defines the light spectrum that is emitted

from the semiconductor light emitting device. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶75.)

5. Claim 6

a. The light emitting device of claim 1 wherein said optically transparent layer is comprised of silicone.

Epler discloses or suggests this limitation. (Ex. PA-DEC, ¶76.) As discussed previously, bonding layer 34 and the material consisting of bonding layer 34 and 38 each comprises an "optically transparent layer." (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶76.) *Epler* further discloses that "bonding layer 38 may be . . . silicone" and that boding layer 34 is a "conductive" layer. (Ex. PA-1, ¶¶[0024] ("An electrically conductive bonding layer 34 is formed over the top layer of semiconductor structure 32 . . . . Suitable materials for conductive bonding layer 34 are minimally optically absorbing at the wavelength emitted by the light emitting layers of the semiconductor structure, are conductive enough to not significantly add to the series resistance of the device, and form an ohmic contact with the top layer of semiconductor structure 32. . . . In some embodiments, bonding layer 34 is a thick, transparent, conductive layer, such as a spin-on or sol-gel material."), [0027], FIG. 6; Ex. PA-DEC, ¶76.) Because "[b]onding layer 38 may be the same material as bonding layer 34," *Epler* discloses that conductive bonding layer 34 may also comprise silicone, which was used for conductive bonding. (Ex. PA-1, ¶¶[0024], [0027], FIG. 6; *see generally* Ex. PA-41, ¶[0003] ("Conductive silicone and conductive epoxies have been used as conductive adhesives."); Ex. PA-42, ¶[0011] ("[A]n electrically conductive thermosetting silicone adhesive or a solder may be used as the electrically conductive adhesive."); Ex. PA-43, 1:28-37; Ex. PA-DEC, ¶76.) To the extent *Epler* does not explicitly disclose that bonding layer 34 may comprise silicone, the configuration would have been obvious. (Ex. PA-DEC, ¶76.) The use of silicone in layer 34 would have yielded similar lighting benefits to those described with respect to bonding layer 38 and could have easily been manufactured by a POSITA in a similar way. (Ex. PA-1, ¶[0027]; Ex. PA-DEC, ¶76.) *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007).

6. Claim 7

a. The light emitting device of claim 6 wherein said optically definable material is comprised of phosphor.

Epler discloses this limitation. (Ex. PA-DEC, ¶77.) The "optically definable material" may be a phosphor, as disclosed by *Epler*. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex.

PA-DEC, ¶77.) *Epler* further discloses that the "wavelength converting material"/"phosphor may be disposed in bonding layer 38," which may be a silicone material:

> A wavelength converting material such as a **phosphor may be disposed in bonding layer 38**. For example, a red-emitting phosphor may be disposed in bonding layer 38, and a yellow- or green-emitting phosphor such as cerium-doped yttrium aluminum garnet may be disposed in or on window layer 40, such that the composite light emitted from the device appears warm white. **Alternatively, a mixture of phosphors may be disposed in a silicone bonding layer 38**, to provide the desired spectrum.

(Ex. PA-1, ¶[0027] (emphasis added), FIG. 6; Ex. PA-DEC, ¶77.) As explained previously, layer 34 may also include phosphor, because *Epler* discloses that layer 34 may comprise the same material as layer 38. (*See supra* §VI.A.2.c; Ex. PA-DEC, ¶77.) Disposing such a phosphor in the optically transparent layer would have shaped and defined the light spectrum that is emitted from the semiconductor light emitting device. (*See supra* §VI.A.2.c; Ex. PA-1, ¶[0027], FIG. 6; Ex. PA-DEC, ¶77.)

7. Claim 9

a. The light emitting device of claim 1 wherein said passivation layer is comprised of at least one of SiO_2, SiN, AlN, Al_2O_3, an epoxy, and an electrophoretic deposited paint.

Epler discloses this limitation. (Ex. PA-DEC, ¶78.) As discussed previously, *Epler* discloses a "dielectric layer 56" ("passivation layer"). (*See supra* §VI.A.2.f.) *Epler* further discloses that "[d]ielectric layer[] 56 . . . may be, for example, SiN_x" ("SiN"). (Ex. PA-1, ¶[0039], FIG. 6; Ex. PA-DEC, ¶78.)

B. SNQ2: *Epler* in View of *Fan* Discloses or Suggests Claim 8

As explained below and in the attached declaration of Dr. Baker (Ex. PA-DEC), *Epler* in view of *Fan* discloses or suggests the limitations of claim 8 of the '822 patent. (Ex. PA-DEC, ¶79.)

1. Claim 8

a. The light emitting device of claim 1 wherein said first and second electrical contacts are comprised of at least one of titanium, chrome, nickel, palladium, platinum, and copper.

Epler in view of *Fan* discloses or suggests this limitation. (Ex. PA-DEC, ¶80.) As discussed previously, *Epler* discloses the limitations of claim 1. (*See supra* §§VI.A.2.)

Specifically, *Epler* discloses or suggests that p-contact metal 60 is in contact with conductive bonding layer 34 and n-contact metal 58 includes two portions that are in contact, which correspond to the "first and second electrical contacts," as claimed. (*See supra* §§VI.A.2.g-h.) Although *Epler* discloses that the contacts are conductive and comprised of metal (Ex. PA-1, ¶¶[0034]-[0035]), *Epler* does not explicitly disclose that the metal contacts may be made of "titanium, chrome, nickel, palladium, platinum, [or] copper," as claimed. However, it was well-understood and conventional to use "titanium, chrome, nickel, palladium, platinum, [or] copper" to form LED semiconductor contact metals before the alleged time of invention. (*See, e.g.*, Ex. PA-DEC, ¶80; Ex. PA-6, ¶[0063] ("For example, contacts 16, 20 may contact n-type material or p-type material. Suitable metals for n-type contacts include titanium, nickel, . . . copper, and alloys thereof. Suitable metals for p-type contacts include nickel, . . . and titanium, and alloys thereof"); Ex. PA-7, ¶[0018] ("Typically, high-work function metals (as used herein, defined to be metals with a work-function exceeding 4.55 eV such as nickel, chrome, . . . and some rare earth metals and composites are used to make good ohmic p-doped semiconductor contacts."); Ex. PA-8, ¶[0050] ("The n-contact 201 and the p-contact 207 are metal and may be . . . platinum . . . or the like.").) As one specific example, *Fan* discloses forming n- and p-type contacts with "nickel," "platinum," "titanium," "palladium" or combinations thereof and combinations with other metals. (Ex. PA-9, ¶[0024]-[0027], FIG. 1; Ex. PA-DEC, ¶80.) Thus, if not disclosed, it would have been obvious for the *Epler* contact metals to comprise "titanium, chrome, nickel, palladium, platinum, [or] copper" for the various understood benefits associated therewith, including low resistivity and high conductivity. (Ex. PA-DEC, ¶80; *see, e.g.*, Ex. PA-24, ¶[0046]; Ex. PA-25, 25:61-26:6.) *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416-17 (2007).

C. SNQ3: *Epler* in View of *Aldaz* Discloses or Suggests Claim 10

As explained below and in the attached declaration of Dr. Baker (Ex. PA-DEC), *Epler* and *Aldaz* disclose or suggest the limitations of claim 10 of the '822 patent. (Ex. PA-DEC, ¶81.)

1. Claim 10

a. The light emitting device of claim 1 wherein said first and second electrical contacts comprise an electroplated material.

Epler in view of *Aldaz* discloses or suggests this limitation. (Ex. PA-DEC, ¶¶82-87.) *Epler* does not explicitly disclose that its first and second electrical contacts discussed in Sections VI.A.2.g-h may be formed via an electroplating process (wherein the first and second contacts

would comprise electroplated material). However, based on the teachings of *Aldaz* and the state of the art, this feature would have been obvious. (Ex. PA-DEC, ¶82.)

For more context regarding this limitation, manufacturing techniques for electroplating one or more semiconductor LED layers were well established before the alleged time of invention. (Ex. PA-DEC, ¶83.) "Electrodeposition" (also known as electroplating) "ha[d] been used for decades" in the semiconductor industry before the alleged time of invention. (Ex. PA-30, 1818.) Indeed, electroplating processes were "widely recognized" as being "considerably simpler and more cost-effective than dry processes" to form semiconductor metals and could be used to create "either uniform films or complex-shaped objects." (*Id.*) Such "electrochemical technology ha[d] played a decisive role in the phenomenal advancement and growth of storage, interconnection, packaging and other aspects of the microelectronics industry." (Ex. PA-31, 1) The '822 patent does not claim or describe anything more than an application of such well-known and conventional electroplating manufacturing techniques. (*See* Ex. PAT-A, 7:40-54 (expressing that a metal layer may be "plated" in defined patterns), 9:19-21 (claim 10).).

Aldaz, as one example, discloses electroplating openings in an LED dielectric to form n and p contacts. (Ex. PA-DEC, ¶84.) For instance, *Aldaz* discloses a "semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region." (Ex. PA-11, abstract.) More specifically, *Aldaz*, like *Epler*, discloses depositing a "dielectric layer" on an LED structure. (*Id.*, ¶[0030]; *see supra* §§VI.A.2.g-h.) Thereafter, "[o]penings for the n- and p-contacts are patterned into the dielectric, then the n- and p-contacts are formed in the openings, for example by electroplating, evaporation, or any other suitable technique." (Ex. PA-11, ¶[0030]; *see also id.*, ¶[0036].) Thus, *Aldaz* discloses forming first and second electrical contacts in dielectric openings via an electroplating process as claimed. (Ex. PA-DEC, ¶84.)

More generally, a POSITA would have understood that *Aldaz* is representative, as a variety of LED electroplating processes were understood during the relevant time period. (Ex. PA-DEC, ¶85; *see, e.g.*, Ex. PA-28, ¶[0040] ("The electrically conductive material 36 can be deposited by vacuum evaporation, sputtering, electroplating, or the like. . . . For electroplating, a thin seed layer (not shown) is deposited inside the vias 34 and the electrically conductive material 36 is electroplated to fill the vias 34 and to extend outside the vias 34. Extension or overflowing of the electroplated material outside of the vias is known as 'mushrooming' in the art. The electrically conductive material 36 lying outside of the vias 34 defines the connecting pads 42, 44."); Ex. PA-

32, ("Current spreading layer 44, p-electrode 46, and n-electrode 48 may be deposited by electroplating."); Ex. PA-10, ¶[0025] ("After etching, the structure has openings 24 and 26, as shown in FIG. 4, over the n-contact and p-contact metal, respectively. The photoresist 28 remaining from the photolithography step is left in place for the electroplating process. As mentioned previously, in current approaches to electroplating, a further masking and etching process, typically with photolithography, occurs to ensure connection between the ground plane and the electroplating seed layers of the n-contact and p-contact metals."); Ex. PA-33, Abstract.)

Thus, it would have been obvious to form *Epler*'s first and second electrical contacts discussed above (contacts formed by connection of metal 58 and connection of metal 60 to layer 34) via well-established electroplating processes, like taught by *Aldaz* and understood in the art. (Ex. PA-DEC, ¶86.) In combination, *Epler*'s first and second contacts (*see supra* §§VI.A.2.g-h) would be formed through dielectric layer 56 as disclosed by *Aldaz*. (Ex. PA-DEC, ¶86.) A POSITA would have had good reason for manufacturing the contacts with such electroplating processes. (Ex. PA-DEC, ¶86.) For instance, a POSITA would have been motivated to use an electroplating technique to form the contacts at least because it was a "suitable technique" to manufacture the *Epler* device. (Ex. PA-11, ¶[0030]; Ex. PA-DEC, ¶86.) Further, electroplated contacts provided "a more robust electrical connection" over other conventionally formed semiconductor contacts. (Ex. PA-2, 9:43-46; *see also, e.g.*, 1:20-4:49; Ex. PA-1, ¶[0035]; Ex. PA-DEC, ¶86.) Indeed, as with any semiconductor device, a POSITA would have recognized that *Epler*'s lighting device would have benefited from increases in reliability, cost savings, manufacturability, etc., by electroplating its semiconductor metals. (Ex. PA-2, 14:24-43; Ex. PA-30, 1826 ("Many investigations have highlighted the advantages of electrodeposition, the main one being less costly fabrication."); Ex. PA-DEC, ¶86.)

A POSITA would have had a reasonable expectation of success in modifying *Epler* based on the teachings of *Aldaz*, at least because conventional electroplating was "relatively easy to control." (Ex. PA-2, 3:26-27; Ex. PA-DEC, ¶87.) Additionally, electroplating processes for LED contacts were well known. (*See, e.g.*, Ex. PA-10, ¶¶[0020]-[0021], [0026]-[0028], FIGs. 5-6 (disclosing techniques to electroplate n-contact metal 18 and p-contact metal 14 of an LED); Ex. PA-11, ¶[0030] ("Openings for the n- and p-contacts are patterned into the dielectric, then the n- and p-contacts are formed in the openings, for example by electroplating, evaporation, or any other suitable technique.").) Modifying *Epler* based on the teachings of *Aldaz*, as discussed above,

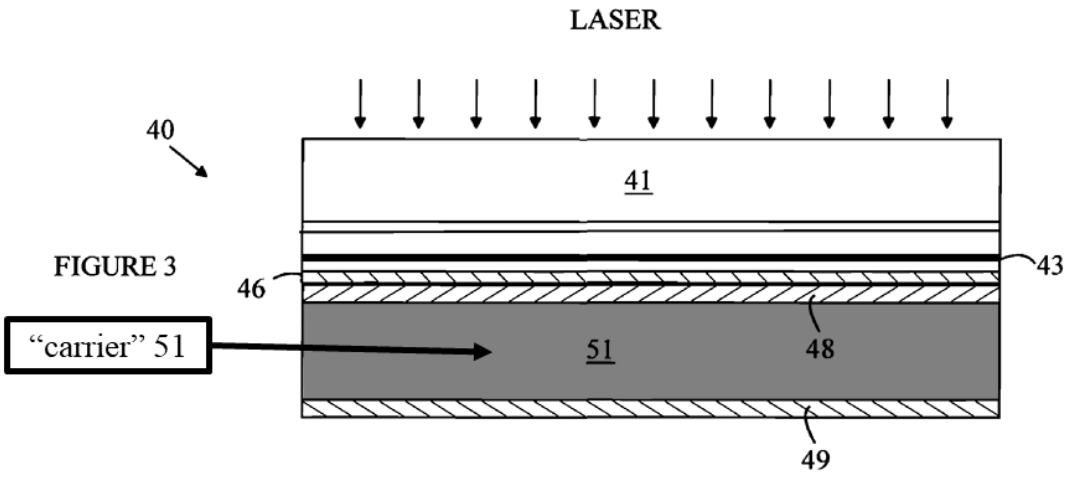
would have involved no more than an application of known technologies (e.g., semiconductor metals and connections) according to known methods (e.g., electroplating techniques as disclosed by *Aldaz* and others) to yield the predictable result of electroplated metal contacts. (Ex. PA-DEC, ¶87.) *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

D. SNQ4: *Epler* in View of *Lester* Discloses or Suggests Claims 1, 2, 5-7, and 9

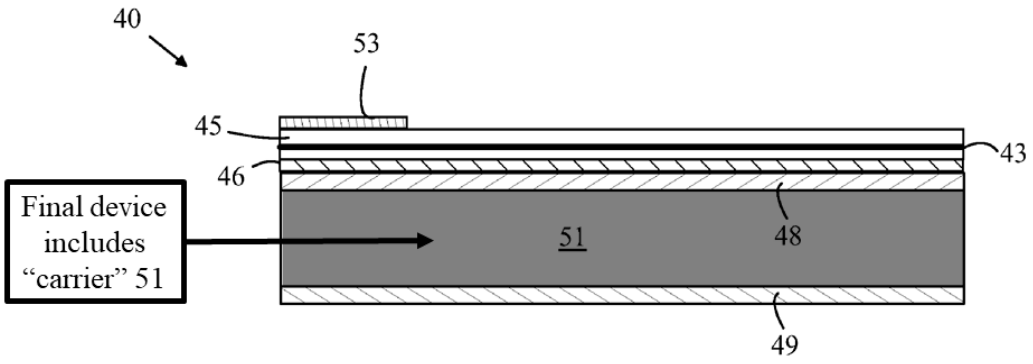
1. Claim 1

As discussed above in Section VI.A.2.e, based on Patent Owner's infringement allegations in district court, the portion of n-contact metal 58 of *Epler*'s device discussed in in Section VI.A.2.e discloses "a carrier layer proximal to a second surface of said semiconductor LED, said first and second surfaces on opposing sides of said semiconductor LED," as recited in claim 1. To the extent Patent Owner argues that limitation is not disclosed by *Epler*, however, that limitation would have been obvious based on *Epler* in view of *Lester*. (Ex. PA-DEC, ¶¶88-97.)

Similar to *Epler*, *Lester* describes fabricating a GaN LED device. (Ex. PA-34, 3:24-46, FIGS. 2-5.) According to *Lester*, once the GaN LED layers are deposited, "the wafer is turned upside down and bonded to a carrier 51 as shown in FIG. 3." (*Id.*, 3:47-49, FIG. 3.)



(*Id.*, FIG. 3 (annotated).) *Lester* explains that "carrier 51 is constructed from a conducting material such as silicon or a metal," and as shown in Figure 4 below, remains in the final device. (*Id.*, 3:52-54, FIG. 4.)



(*Id.*, FIG. 4 (annotated).)

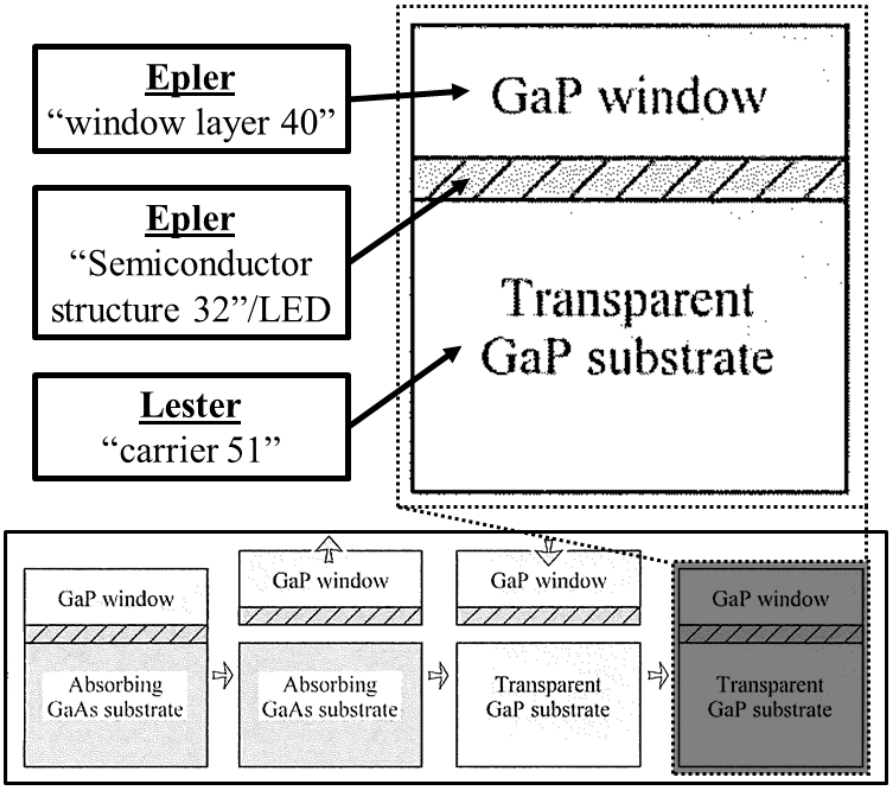
Based on the teachings of *Lester*, a POSITA would have had good reason to fabricate the LED device described in *Epler* using a carrier like that described in *Lester*. (Ex. PA-DEC, ¶91.) As *Lester* explains, fabricating a GaN LED using a carrier such as carrier 51 allows for LED thinning to improve conversion efficiency and light extraction. (Ex. PA-34, 1:26-2:21, 3:5-21, 3:22-24, 4:8-12; Ex. PA-DEC, ¶91.) For example, *Lester* explains that "conversion efficiency of individual LEDs is an important factor in addressing the cost of high power LED light sources" (Ex. PA-34, 1:26-28), and that "a significant fraction of the light generated in the active layer is lost" (*id.*, 1:57-59). To address these issues, *Lester* describes using a "LED structure with reduced thickness to reduce the amount of light that is absorbed in the GaN layers," as illustrated in Figures 2-4. (*Id.*, 3:22-26, FIGS. 2-4.) In order to reduce the LED structure thickness, *Lester* explains that the structure is "bonded to carrier 51" so that the GaN layers of the structure can be "thinned to a thickness of less than 1.25 μm and preferably a thickness between 1 μm and 1.25 μm." (*Id.*, 3:55-4:1.) In other words, carrier 51 allows for GaN layer thinning and therefore improved conversion efficiency / light extraction. (Ex. PA-DEC, ¶91.) The extra support of carrier 51 would have been particularly helpful given the reduced thickness of lighting region. (*Id.*) Indeed, as explained in more detail below with respect to Ex. PA-26, supporting a lighting region via both a window layer support and a carrier support was common in the art. (Ex. PA-DEC, ¶91; Ex. PA-26, 156-157.)

Lester further explains that its techniques involving carrier 51 "can be performed at the wafer scale," such that "wafer-scale economies of scale can be achieved." (Ex. PA-34, 4:8-12.) Additionally, as a POSITA would have recognized, carrier 51 would have allowed LED manufacturers to supply LED wafers to customers that can then perform additional fabrication

steps depending on the customer's desired application, including adding various color filters or lenses over the LEDs. (Ex. PA-DEC, ¶92.)

A POSITA would have also had a reasonable expectation of success fabricating LED devices like those described in *Epler* to include a carrier layer like that described in *Lester*. (*Id.*, ¶93.) For example, in order to achieve the advantages described in *Lester*, a POSITA would have recognized that the fabrication process described in *Epler* would have been modified so that the LED structure 32 in *Epler* is bonded to a carrier layer, similar to the carrier layer described in *Lester*, after the LED structure is bonded to window layer 40 and substrate 30 is removed. (*Id.*, ¶93; Ex. PA-1, FIGs. 4-5, ¶[0029].) A POSITA would have recognized that the *Epler* LED structure 32 could have been thinned before the carrier layer is added as suggested by *Lester* (Ex. PA-34, 3:22-26, 3:55-4:1, FIGS. 2-4), and that adding the carrier layer after thinning would have provided additional structural support to the thinned layers, such that the same objectives described in *Lester* are achieved. (Ex. PA-DEC, ¶93.) This is because, as a POSITA would have recognized, the *Epler* window layer 40 would have provided the necessary structural support during the thinning process, until the carrier is added for additional support. (*Id.*, ¶93; Ex. PA-1, ¶[0026] ("Window layer 40 is prefer ably thick enough to permit wafer level handling of the window layer/semiconductor structure combination after the growth substrate is removed.").)

Indeed, the process described above would have been consistent with well-known LED processing technologies available at the time. (*Id.*, ¶94.) For example, it was well known at the time to first create LED layers (e.g., like LED layer 32 in *Epler*) on a growth substrate (e.g., like growth substrate 30 in *Epler*), then attach the LED layers to a window layer (e.g., like window layer 40 in *Epler*), then remove the growth substrate and attach the LED layers to another substrate (e.g., like carrier layer 51 described in *Lester*). (Ex. PA-26, 156-157 (describing and illustrating this process flow); Ex. PA-1, FIGs. 2-5.) The window layer serves as "temporary mechanical support" for the LED layers until additional support is provided by the carrier layer. (Ex. PA-26, 156-157; Ex. PA-1, ¶[0026].)

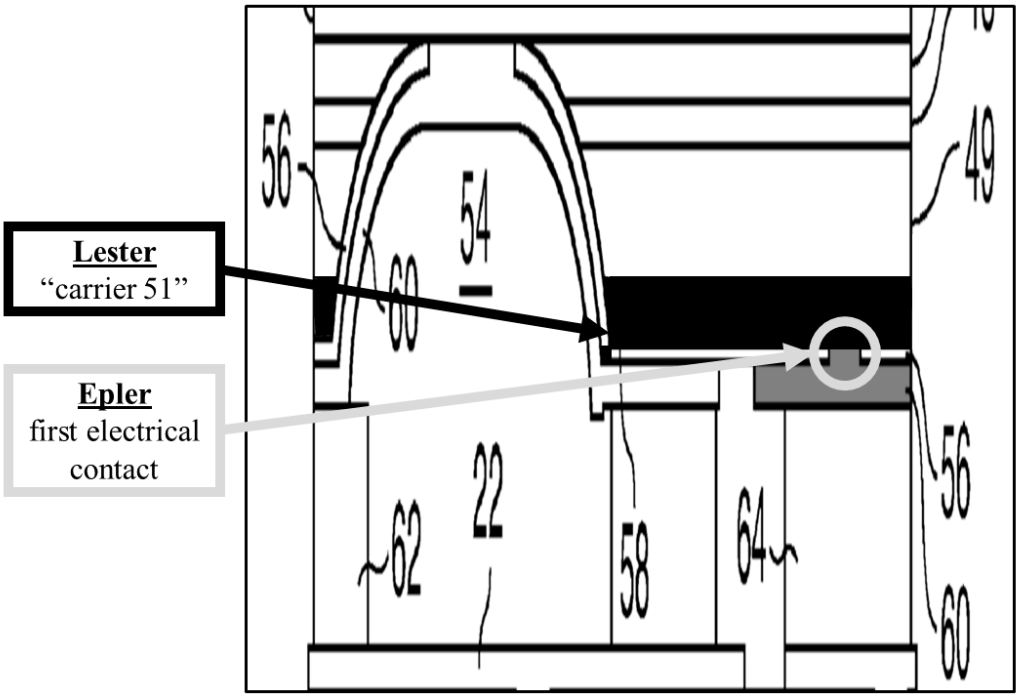


(Ex. PA-26, 156-157 (annotated) (describing and illustrating how the LEDs in the combination could have been manufactured consistent with a conventional window layer, lighting region, and carrier).)

The resulting structure would have achieved an improved version of the device shown in *Epler*'s Figure 6, where the carrier layer would obviate the need for porous region 44 (intended to improve light extraction) and the portion of n-contact metal 58 (an interconnect material) discussed above in Section VI.A.2.e, given the incorporated carrier layer is itself conductive and supports the thinned GaN layers. (PA-34, 3:52-54 ("In one embodiment, carrier 51 is constructed from a conducting material such as silicon or a metal."), 3:65-4:1 (describing the thinning process used in order to improve conversion efficiency / light extraction); Ex. PA-DEC, ¶95.)

The remaining steps described in *Epler* would have remained largely the same. (Ex. PA-DEC, ¶96.) For example, after adding the carrier layer, passivation layer 56 would have been deposited on the carrier layer, a hole similarly would have been created in the passivation layer, and n-contact metal 58 would have been deposited in order to create a first contact in the hole in the passivation layer. (*Id.*) Similarly, another hole would have been created in the carrier, LED layers, and the passivation layer to create a second contact. (*Id.*) As needed, a POSITA would

have adjusted other aspects of the process in order to achieve the combination described above, including depositing the GaN layers in the reverse order or swapping the locations of the p- and n-metals. (*Id.*) These were well known and straightforward semiconductor processes at the time, and therefore a POSITA would have been capable of making any adjustments necessary to achieve such a combination. (*Id.*) An example illustration of the resulting combination is provided below. (*Id.*)



(Ex. PA-DEC, ¶96.)

Accordingly, the inclusion of a carrier like that described in *Lester* in the device like that described in *Epler* would have been nothing more than a combination of known elements (*Epler*'s LED device that includes a carrier like that in *Lester* that supports thinned LED layers) according to known methods (attaching the LED layers to a carrier, similar to as described in *Lester*) yielding the predictable result of a LED device that includes a carrier and therefore improved conversion efficiency / light extraction and wafer-scale economies. (*Id.*, ¶97.) *KSR*, 550 U.S. 398, 416.

2. Claims 2, 5-7, and 9

Epler in view of *Lester* discloses or suggests the limitations of claims 2, 5-7, and 9 for substantially the same reasons discussed *supra* in Section VI.A, as the inclusion of *Lester* does not detract from the relied upon disclosures in Section VI.A. (*See supra* §VI.A.)

E. SNQ5: *Epler* in View of *Lester* and *Fan* Discloses or Suggests Claim 8

Epler in view of *Lester* and *Fan* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.B, as the inclusion of *Lester* does not detract from the relied upon disclosures in Section VI.B. (*See supra* §VI.B.)

F. SNQ6: *Epler* in View of *Lester* and *Aldaz* Discloses or Suggests Claim 10

Epler in view of *Lester* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.C, as the inclusion of *Lester* does not detract from the relied upon disclosures in Section VI.C. (*See supra* §VI.C.)

G. SNQ7: *Epler* in View of *Han* Discloses or Suggests Claims 1, 2, 5-7, and 9

Relevant to SNQ7, the claim 1 analysis set forth above explains how *Epler* discloses an "n-type region 49," which includes a "porous region 44," a light emitting region 48" (an active region), and a "p-type region 46," which together comprise a semiconductor LED. (*See supra* §VI.A.2.d.) *Epler* discloses that light emitting/active region 48 may not be doped, which discloses an "intrinsic region," as claimed. (*Id.*) *Epler* does not, however, explicitly refer to light emitting region 48 as an "intrinsic" region. Thus, to the extent it is argued that *Epler* does not disclose "an intrinsic region," as claimed, it would have been obvious for *Epler*'s LED to include an undoped intrinsic region, similar to as taught by *Han*. (Ex. PA-DEC, ¶¶101-107.)

Conventional LEDs of the time comprised an undoped active layer. (Ex. PA-DEC, ¶102.) For example, gallium nitride (GaN) LEDs were well understood and "predominantly expected to replace existing light sources such as incandescent lamps, fluorescent lamps and mercury lamps." (Ex. PA-21, ¶[0002].) The typical GaN LED included an "undoped InGaN (an active layer . . .)" that was sandwiched between an n-type and a p-type layer. (*Id.*, ¶[0002], FIGs. 1-2.)

Han discloses one such conventional LED comprising an undoped active layer ("intrinsic region"). (Ex. PA-DEC, ¶103.) For instance, *Han* discloses a "conventional . . . nitride semiconductor LED." (Ex. PA-20, ¶[0007].) The conventional LED "includes . . . an n-type GaN layer-based clad layer 14, an active layer 16, and a p-type GaN layer-based clad layer" that are sequentially deposited on a substrate. (*Id.*, ¶[0007], FIG. 1.) To enhance light emitting efficiency, *Han* discloses that the active layer may be "formed of a multiple quantum well structure including an undoped GaN layer barrier layer and an undoped InGaN layer well layer." (*Id.*, ¶[0007].) Such an undoped active layer, often referred to as an "intrinsic" region (Ex. PA-DEC, ¶103; *see, e.g.*, PA-19, ¶[0004]), was well understood in the art. (Ex. PA-DEC, ¶103; *see*, e.g., Ex. PA-16,

¶[0004], ¶[0007] ("an undoped active layer . . . . The active layer 5 may have a multiple quantum well structure in which a plurality of GaN quantum barrier layers and a plurality of InGaN quantum well layers are alternately laminated"); Ex. PA-17, 1:14-45; Ex. PA-22, Abstract, ¶[0054]; Ex. PA-23, ¶[0028]; Ex. PA-35, ¶[0033] ("As illustrated in FIG. 9, the active layer 105 has a multiple quantum well structure in which an undoped $In_{0.1}5Ga_{0.8}5N$ well layer (thickness: 4 nm) and an undoped $In_{0.2}Ga_{0.9}8N$ barrier layer (thickness: 8 nm) are formed in the order of a barrier layer, a well layer, a barrier layer, a well layer, a barrier layer, a well layer, and a barrier layer on then-type GaN light guide layer 104.").)

It would have been obvious for the active layer in *Epler*'s LED structure to be an undoped active ("intrinsic") region, like taught by *Han* and understood in the art. (Ex. PA-DEC, ¶104.) For example, both *Epler* and *Han* disclose the use of InGaN for the LED region (Ex. PA-1, [0022]; Ex. PA-20, ¶[0007]), and *Han* explains that the active region may be undoped (Ex. PA-20, ¶[0007]). Based on *Han*'s teachings, a POSITA would have had good reason to modify *Epler*'s LED structure such that light emitting region 48 is an undoped active region, similar to as taught by *Han*, because, for example, such a configuration would have improved the efficiency of the *Epler* lighting system. (Ex. PA-20, ¶[0007] (describing efficiency benefits associated with an LED that comprises an undoped, multiple quantum well structure); Ex. PA-17, 1:14-33 (same); Ex. PA-DEC, ¶104.) Additionally, "if [an] active layer is doped with impurities, [a] light emitting element is likely to be deteriorated" more quickly over time as compared to a light emitting element with an undoped active layer. (Ex. PA-35, ¶[0034]; Ex. PA-DEC, ¶104.) Including the *Han* active layer comprising undoped barrier and well layers in the *Epler* LED structure would have "extend[ed] the life" and improved the reliability of the structure. (Ex. PA-35, ¶¶[0034], [0007], Abstract; Ex. PA-DEC, ¶104.)

As a POSITA would have appreciated, such a substitution of different types of active layers would have represented a simple substitution of one known element for another to obtain a predictable result, especially here, where *Epler* itself discloses that light emitting region 48 includes a doping concentration of zero (i.e., is not doped), as discussed above in Section VI.A.2.d. (Ex. PA-DEC, ¶105.) Indeed, "when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious." *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (citation and internal quotation marks omitted). Furthermore, the modification

would have been obvious to try. (Ex. PA-DEC, ¶105.) A POSITA would have appreciated that the active layer could have been doped or undoped. (*Id.*) Implementing the *Epler* active layer as an undoped, intrinsic layer, as taught by *Han* and others, would have been an obvious choice. (*Id.*)

A POSITA would have had a reasonable expectation of success in modifying *Epler* based on the teachings of *Han*, at least because the LED configuration was well understood in the art. (*See, e.g.*, Ex. PA-16, ¶[0004], ¶[0007]; Ex. PA-17, 1:14-33 (same); Ex. PA-20, ¶[0007]; Ex. PA-22, Abstract, ¶[0054]; Ex. PA-23, ¶[0028]; Ex. PA-DEC, ¶106.) And, as noted above, both *Epler* and *Han* disclose the use of InGaN for the LED region. (Ex. PA-1, [0022]; Ex. PA-20, ¶[0007].) Modifying *Epler* as discussed above would have involved no more than an application of known technologies (e.g., the LED structure described in *Epler* and the active region described in *Han*) according to known methods (e.g., conventional LED manufacturing techniques, like those described in *Epler* and *Han*) to yield the predictable result of an LED that includes an undoped active layer. (Ex. PA-DEC, ¶106.) *See KSR*, 550 U.S. at 416.

Epler discloses the remaining features of claims 1, 2, and 5-7, and 9 as set forth in the preceding sections. (*See supra* §VI.A.)

H. SNQ8: *Epler* in View of *Han* and *Fan* Discloses or Suggests Claim 8

Epler in view of *Han* and *Fan* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.B, as the inclusion of *Han* does not detract from the relied upon disclosures in Section VI.B. (*See supra* §VI.B.)

I. SNQ9: *Epler* in View of *Han* and *Aldaz* Discloses or Suggests Claim 10

Epler in view of *Han* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.C, as the inclusion of *Han* does not detract from the relied upon disclosures in Section VI.C. (*See supra* §VI.C.)

J. SNQ10: *Epler* in View of *Han* and *Lester* Discloses or Suggests Claims 1, 2, 5-7, and 9

Epler in view of *Han* and *Lester* discloses or suggests the limitations of claim 1, 2, 5-7, and 9 for substantially the same reasons discussed *supra* in Section VI.D, as the inclusion of *Han* does not detract from the relied upon disclosures in Section VI.D. (*See supra* §VI.D.)

K. SNQ11: *Epler* in View of *Han*, *Lester*, and *Fan* Discloses or Suggests Claim 8

Epler in view of *Han*, *Lester*, and *Fan* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.B, as the inclusion of *Han* and *Lester* does not detract from the relied upon disclosures in Section VI.B. (*See supra* §VI.B.)

L. SNQ12: *Epler* in View of *Han*, *Lester*, and *Aldaz* Discloses or Suggests Claim 10

Epler in view of *Han*, *Lester*, and *Aldaz* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.C, as the inclusion of *Han* and *Lester* does not detract from the relied upon disclosures in Section VI.C. (*See supra* §VI.C.)

M. SNQ13: *Epler* in View of *Nagahama* Discloses or Suggests Claims 1, 2, 5-7, and 9

Relevant to SNQ13, the claim 1 analysis set forth above explains how *Epler* discloses an "n-type region 49," which includes a "porous region 44," a light emitting region 48" (an active region), and a "p-type region 46," which together comprise a semiconductor LED. (*See supra* §VI.A.2.d.) *Epler* discloses that light emitting/active region 48 may not be doped and therefore discloses an "intrinsic region," as claimed. (*Id.*) *Epler* does not, however, explicitly refer to light emitting region 48 as an "intrinsic" region. Thus, to the extent it is argued that *Epler* does not disclose "an intrinsic region," as claimed, it would have been obvious for *Epler*'s LED to include an undoped intrinsic region, similar to as taught by *Nagahama*. (Ex. PA-DEC, ¶113-119.)

As discussed above, conventional LEDs of the time comprised an undoped active layer. (Ex. PA-DEC, ¶114.) For example, gallium nitride (GaN) LEDs were well understood and "predominantly expected to replace existing light sources such as incandescent lamps, fluorescent lamps and mercury lamps." (Ex. PA-21, ¶[0002].) The typical GaN LED included an "undoped InGaN (an active layer . . .)" that was sandwiched between an n-type and a p-type layer. (*Id.*, ¶[0002], FIGs. 1-2.)

Nagahama discloses one such conventional LED comprising an undoped active layer ("intrinsic region"). (Ex. PA-DEC, ¶115.) For instance, *Nagahama* discloses a "fabrication method of a nitride semiconductor device comprising a nitride semiconductor . . . , such as a light emitting diode (LED)." (Ex. PA-36, 1:7-13.) The active layer of the LED includes an "un-doped"

well layer that "increase[s] the light emitting efficiency of the light emitting device."[4] (*Id.*, 20:3-24, FIG. 1; *see also id.*, 20:35-43 ("in order to improve the crystallinity to the maximum extent, an un-doped well layer has to be grown"), 20:60-65 ("In the case of a high output device such as a high output LD and a high power LED, to be operated with a high quantity of electric current, if the well layer is undoped and practically contains no n-type impurity, the re-coupling of carriers in the well layer can be promoted and light emitting re-coupling can be carried out at a high efficiency.").)

It would have been obvious for the light emitting region 48 in *Epler*'s LED structure to be an undoped active ("intrinsic") region, like taught by *Nagahama* and understood in the art. (Ex. PA-DEC, ¶116.) For example, both *Epler* and *Nagahama* disclose the use of InGaN for the LED region (Ex. PA-1, ¶[0022]; Ex. PA-36, 20:4-15), and *Nagahama* explains that the active region may be undoped (Ex. PA-36, 20:4-21:9). Based on *Nagahama*'s teachings, a POSITA would have had good reason to modify *Epler*'s LED structure such that light emitting region 48 is an undoped active region, similar to as taught by *Nagahama*, because, for example, such a configuration would have improved the efficiency of the *Epler* lighting system and supported high output applications. (Ex. PA-36, 20:4-21:9; Ex. PA-DEC, ¶116.)

As a POSITA would have appreciated, such a substitution of different types of active layers would have represented a simple substitution of one known element for another to obtain a predictable result, especially here, where *Epler* itself discloses that light emitting region 48 includes a doping concentration of zero (i.e., is not doped), as discussed above in Section VI.A.2.d. (Ex. PA-DEC, ¶117.) Indeed, "when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious." *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (citation and internal quotation marks omitted). Furthermore, the modification would have been obvious to try. (Ex. PA-DEC, ¶117.) A POSITA would have appreciated that the active layer could have been doped or undoped. (*Id.*) Implementing the *Epler* active layer as an undoped, intrinsic layer, as taught by *Nagahama* would have been an obvious choice. (*Id.*)

[4] *Nagahama* explains that the active layer may also comprise a "barrier layer" that "is an n-impurity-doped layer," which does not alter the conclusion that *Nagahama*'s well layer discloses the claimed "intrinsic region," which is between n- and p-type layers, as required by claim 1. (Ex. PA-DEC, ¶115.)

A POSITA would have had a reasonable expectation of success in modifying *Epler* based on the teachings of *Nagahama*, at least because both *Epler* and *Nagahama* disclose the use of InGaN for the LED region. (Ex. PA-1, ¶[0022]; Ex. PA-36, 20:4-15.) Modifying *Epler* as discussed above would have involved no more than an application of known technologies (e.g., the LED structure described in *Epler* and the active region described in *Nagahama*) according to known methods (e.g., conventional LED manufacturing techniques, like those described in *Epler* and *Nagahama*) to yield the predictable result of an LED that includes an undoped active layer. (Ex. PA-DEC, ¶118.) *See KSR*, 550 U.S. at 416.

Epler discloses the remaining features of claims 1, 2, and 5-7, and 9 as set forth in the preceding sections. (*See supra* §VI.A.)

N. SNQ14: *Epler* in View of *Nagahama* and *Fan* Discloses or Suggests Claim 8

Epler in view of *Nagahama* and *Fan* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.B, as the inclusion of *Nagahama* does not detract from the relied upon disclosures in Section VI.B. (*See supra* §VI.B.)

O. SNQ15: *Epler* in View of *Nagahama* and *Aldaz* Discloses or Suggests Claim 10

Epler in view of *Nagahama* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.C, as the inclusion of *Nagahama* does not detract from the relied upon disclosures in Section VI.C. (*See supra* §VI.C.)

P. SNQ16: *Epler* in View of *Nagahama* and *Lester* Discloses or Suggests Claims 1, 2, 5-7, and 9

Epler in view of *Nagahama* and *Lester* discloses or suggests the limitations of claim 1, 2, 5-7, and 9 for substantially the same reasons discussed *supra* in Section VI.D, as the inclusion of *Nagahama* does not detract from the relied upon disclosures in Section VI.D. (*See supra* §VI.D.)

Q. SNQ17: *Epler* in View of *Nagahama*, *Lester*, and *Fan* Discloses or Suggests Claim 8

Epler in view of *Nagahama*, *Lester*, and *Fan* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.B, as the inclusion of *Nagahama* and *Lester* does not detract from the relied upon disclosures in Section VI.B. (*See supra* §VI.B.)

R. SNQ18: *Epler* in View of *Nagahama*, *Lester*, and *Aldaz* Discloses or Suggests Claim 10

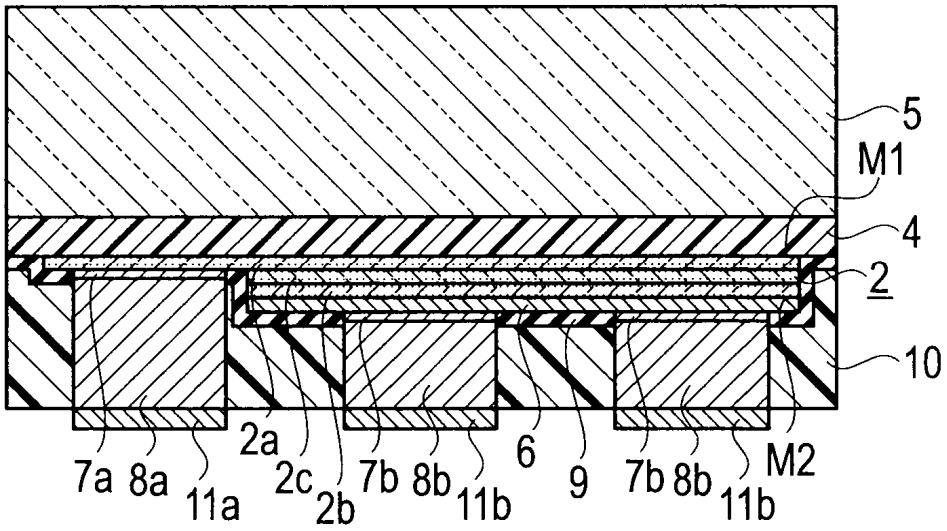
Epler in view of *Nagahama*, *Lester*, and *Aldaz* discloses or suggests the limitations of claim 8 for substantially the same reasons discussed *supra* in Section VI.C, as the inclusion of *Nagahama* does not detract from the relied upon disclosures in Section VI.C. (*See supra* §VI.C.)

S. SNQ19: *Shimokawa* Discloses Claims 1, 2, and 5-10

As explained below and in the attached declaration of Dr. Baker (Ex. PA-DEC), *Shimokawa* discloses the limitations of claims 1, 2, and 5-10 of the '822 patent. (Ex. PA-DEC, ¶125.)

1. Overview of *Shimokawa*

Shimokawa discloses an "optical semiconductor device" and relates to LED technology. (Ex. PA-3, 1:17-44, 4:27-29, 4:66, 9:50-56, FIG. 6.) An example optical semiconductor device is illustrated in Figure 6. (*Id.*, 4:27-29.)



(*Id.*, FIG. 6.)

As illustrated in Figure 6, *Shimokawa*'s lighting device includes a "light-transmissive layer 5." (*Id.*, 6:13-21, FIG. 6.) "The light-transmissive layer 5 is made of a transparent substrate made of a material such as optical glass or quartz." (*Id.*) Light-transmissive layer 5 may be formed on a fluorescent layer 4 "by, for example, applying a liquid glass onto the fluorescent layer 4 by spin coating, and then hardening the liquid glass." (*Id.*, 9:64-67.) The fluorescent layer 4 material may include "phosphor particles" to "convert blue light into long-wavelength light" or otherwise shape the spectrum of emitted light. (*Id.*, 5:62-6:12.) In addition, "fluorescent layer 4 is formed directly

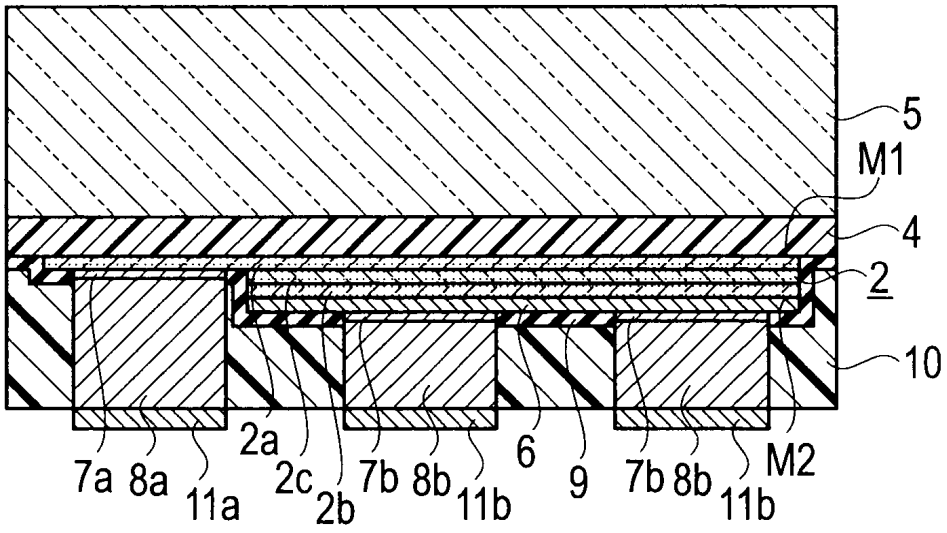
on the first main surface M1 of [a] light-emitting layer 2." (*Id.*, 9:59-61.) The light-emitting layer 2 comprises an "n-type semiconductor layer" 2a, "p-type semiconductor layer" 2b, and an "active layer" 2c, which together comprise a semiconductor LED. (*Id.*, 5:25-29.)

Second electrodes 7b of the optical semiconductor device are disposed in holes in an insulating layer 9, which are formed by sputtering passivation film around the electrodes. (*Id.*, 11:3-20, FIG. 6.) A first electrode 7a is similarly disposed in a separate hole in insulating layer 9. (*Id.*, 11:3-20.) A cavity extends from the insulating layer 9 hole and through layers 2b and 2c of the light-emitting layer 2 and a reflective layer 6, so as to form a second contact hole for electrode 7a. (*Id.*, 5:39-46, 6:27-44, 6:66-7:7, 11:3-20, FIGs. 2 and 6.)

2. Claim 1

a. A light emitting device, comprising:

To the extent the preamble is limiting, *Shimokawa* discloses this limitation. (Ex. PA-DEC, ¶129.) For example, *Shimokawa* discloses an "optical semiconductor device" ("light emitting device"). (Ex. PA-3, 4:27-29, 4:66, 9:50-56, FIG. 6.) The optical semiconductor device includes a light emitting layer 2.[5] (*Id.*, 4:66-5:1.) An example optical semiconductor device is illustrated in Figure 6, reproduced below. (*Id.*, FIG. 6.)

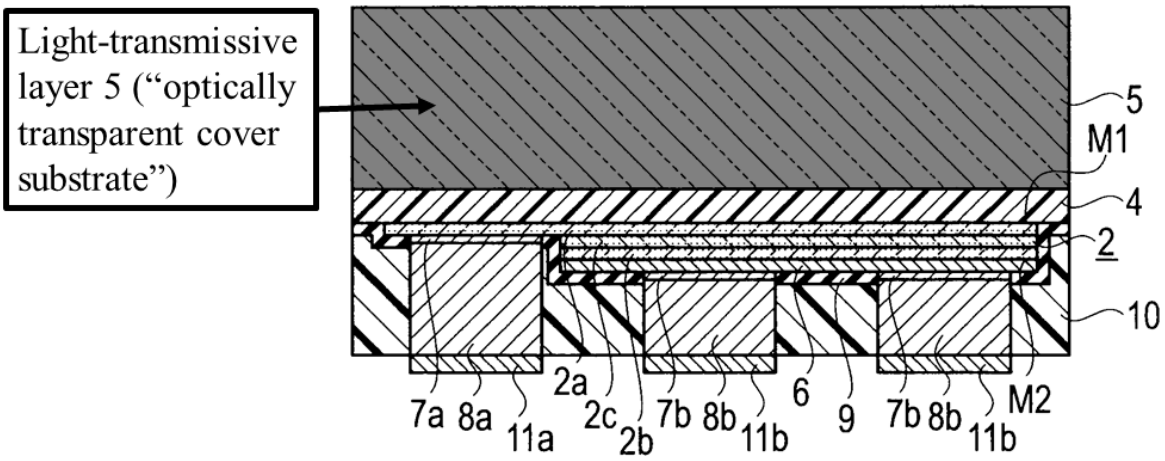


(*Id.*, FIG. 6.)

[5] Various features of the *Shimokawa* Figure 6 embodiment are described in the description of the *Shimokawa* first embodiment. (Ex. PA-3, 9:50-56.)

b. an optically transparent cover substrate;

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶130.) For example, *Shimokawa* discloses a "light-transmissive layer 5" ("optically transparent cover substrate"). (Ex. PA-3, 6:13-21, FIG. 7.) *Shimokawa* discloses that "[t]he light-transmissive layer 5 is made of a transparent substrate made of a material such as optical glass or quartz." (*Id.*, 6:13-21.) Light-transmissive layer 5 covers the remaining components of optical semiconductor device, as illustrated in Figure 6. (Ex. PA-3, FIG. 6; Ex. PA-DEC, ¶130.)

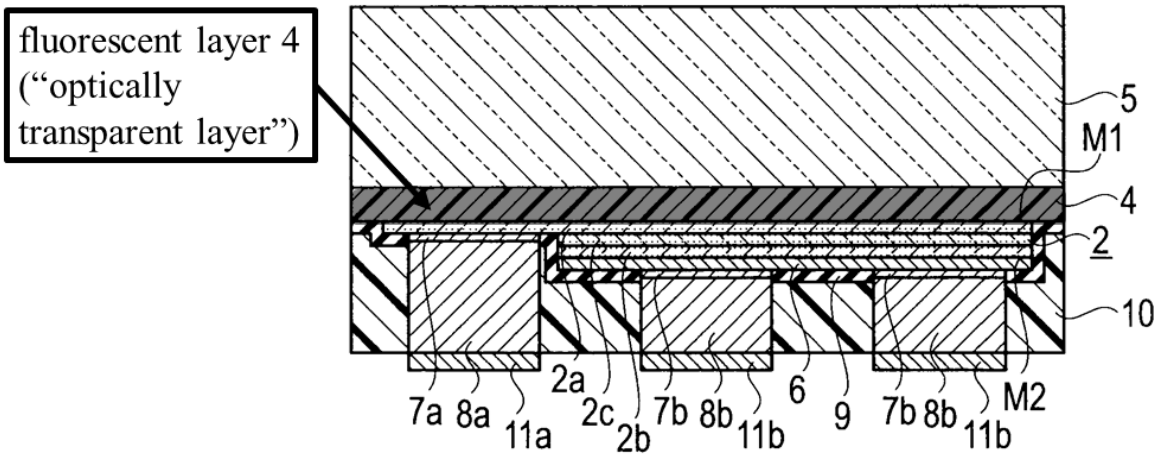


(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶130.)

c. an optically transparent layer attached to a bottom surface of said optically transparent cover substrate, said optically transparent layer including an optically definable material;

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶131-133.) For example, *Shimokawa* discloses "fluorescent layer 4" ("optically transparent layer"). (Ex. PA-3, 5:61, FIG. 6.) Fluorescent layer 4 is optically transparent given that light generated from active layer 2c emits from a surface of light-transmissive layer 5 by passing through fluorescent layer 4. (Ex. PA-3, 7:37-55, FIG. 6; Ex. PA-DEC, ¶131.) *Shimokawa* also discloses that fluorescent layer 4 may be formed from "silicone resin," which is a well-known transparent lighting material. (Ex. PA-3, 5:62-63; Ex. PA-DEC, ¶131; *see generally* Ex. PA-12, ¶[0009] ("Another method for forming a phosphor-containing layer can include coating a top surface of a semiconductor light emitting element with **a transparent resin such as** an epoxy resin, **a silicone resin** and the like in which phosphor particles have been dispersed (that is collectively referred to as a 'wavelength converting member' hereinafter), by means of a dispenser. In this case, the wavelength conversion member is coated over the top surface of the semiconductor light emitting element so as not to run over the

top surface of the element. This configuration can remarkably suppress color unevenness when compared with the configuration of FIG. 1.") (emphasis added); Ex. PA-13, ¶0003 ("[A] phosphor layer is formed, encapsulated with high transparent resin such as an epoxy resin or silicone resin, and the resin is formed in the form of lens to obtain light emitting diodes.").)



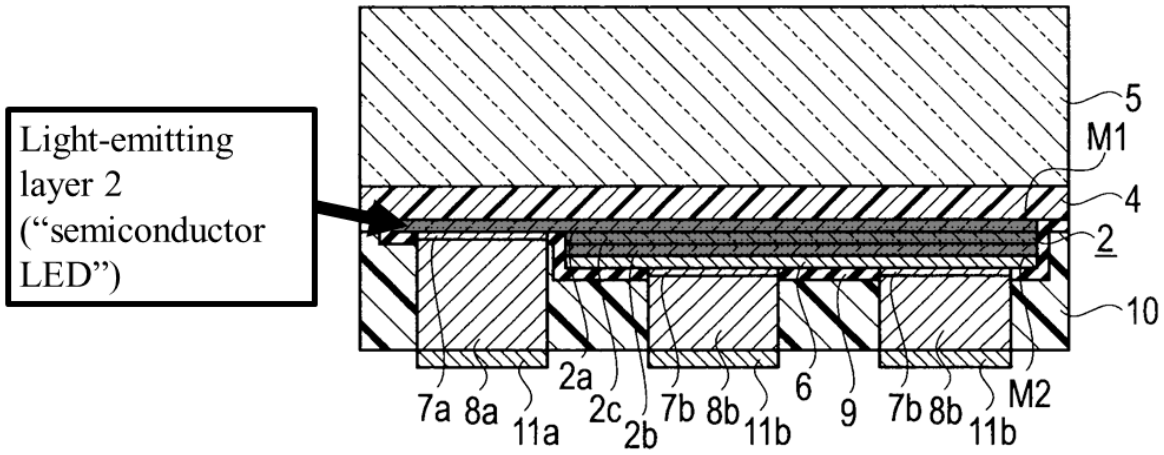
(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶131.)

Shimokawa discloses that fluorescent layer 4 ("optically transparent layer") may be "attached to a bottom surface of said optically transparent cover substrate," as claimed. (Ex. PA-DEC, ¶132.) For instance, *Shimokawa* discloses that the light-transmissive layer 5 may be formed on fluorescent layer 4 "by, for example, applying a liquid glass onto the fluorescent layer 4 by spin coating, and then hardening the liquid glass." (Ex. PA-3, 9:64-67; Ex. PA-DEC, ¶132.) The spin coating process attaches the fluorescent layer 4 to the bottom of light-transmissive layer 5 ("optically transparent cover substrate"). (Ex. PA-3, 9:64-67, FIG. 1; Ex. PA-DEC, ¶132.)

Shimokawa discloses that fluorescent layer 4 material may "includ[e] an optically definable material," as claimed, at least because the fluorescent layer may include one or more phosphors to help shape the color of emitted light. (Ex. PA-3, 5:62-64 ("The fluorescent layer 4 is formed by mixing phosphor particles in a silicone resin. The phosphor particles convert blue light into long-wavelength light."); FIG. 6; Ex. PA-DEC, ¶133.) The *Shimokawa* disclosure is consistent with the '822 patent, which also discloses a similar phosphor configuration. (Ex. PAT-A, 5:9-16.)

d. a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region, wherein said intrinsic region is between said positively-doped region and said negatively-doped region, and a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer;

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶¶134-137.) *Shimokawa* discloses "a semiconductor LED including a positively-doped region, an intrinsic region, and a negatively-doped region," as claimed. (Ex. PA-DEC, ¶134.) For instance, *Shimokawa* discloses a light-emitting layer 2 comprising an "n-type semiconductor layer" 2a, a "p-type semiconductor layer" 2b, and an "active layer" 2c, which together comprise a semiconductor LED. (Ex. PA-3, 5:25-29; Ex. PA-DEC, ¶134; *see generally* Ex. PA-14, ¶[0017] ("In the conventional nitride-based semiconductor LED, the n-type nitride semiconductor layer 120, the active layer 130, and the p-type nitride semiconductor layer 140 are sequentially formed on the substrate 110. Among them, the active layer 130 has a multi-quantum well structure including an InGaN layer.").)



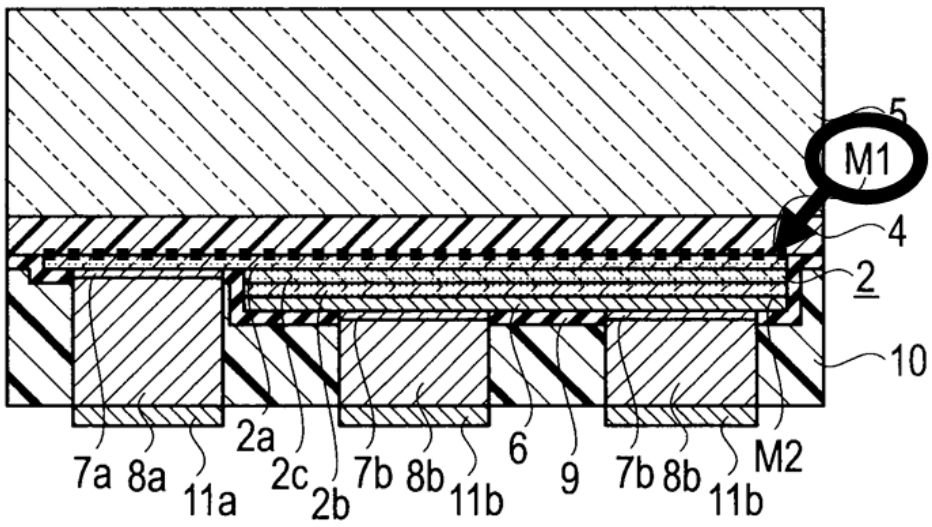
(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶134.) A POSITA would have understood that n-type semiconductor layer 2a is a negatively doped semiconductor material ("negatively-doped region") and p-type semiconductor layer 2b is a positively doped semiconductor material ("positively-doped region"). (Ex. PA-3, 5:25-29; Ex. PA-4, 1:61-65 ("electron 'holes' become the charge carriers and the doped silicon is referred to as positive or P-type silicon . . . additional electrons become the charge carriers and the doped silicon is referred to as negative or N-type silicon"); Ex. PA-5, ¶¶[0003]-[0005]; Ex. PA-DEC, ¶134.) Additionally, because active layer 2c does not include n-type or p-type materials, such as the materials used for layers 2a and 2b, active

layer 2c comprises an intrinsic region. (Ex. PA-3, 5:25-31; Ex. PA-DEC, ¶134; *see, e.g.*, PA-19, ¶[0004] (referring to an undoped region as an "intrinsic" region).)

Moreover, *Shimokawa* discloses that the light emitting layer 2 emits blue light and may include "InGaN layers." (Ex. PA-3, 5:25-33; Ex. PA-DEC, ¶135.) This type of semiconductor LED was conventional before the alleged time of invention and comprised n- and p-type regions that surround an undoped active region. (Ex. PA-DEC, ¶135; *see generally, e.g.*, Ex. PA-16, ¶[0004], ¶[0007] ("Generally, nitride-based semiconductor light-emitting devices are optical devices with a high output that generate short-wavelength light in the blue and green ranges and the like, and thus enable realization of the full color spectrum. . . . [T]he conventional nitride-based semiconductor light-emitting device 10 comprises . . . an n-type clad layer 13, an undoped active layer 15 and a p-type clad layer 17 deposited in this order . . . . The active layer 15 may have a multiple quantum well structure in which a plurality of GaN quantum barrier layers and a plurality of InGaN quantum well layers are alternately laminated."); Ex. PA-17, 1:14-45 ("Nitride semiconductors have been used to make high bright and pure green and blue LEDs for full color displays, traffic signals and light sources for image scanner and so on. These LED devices are made of laminated structures which basically comprise . . . a n-type GaN contact layer doped with Si, an single-quantum-well (SQW) or multi-quantum-well (MQW) active layer comprising InGaN, a p-type AlGaN clad layer doped with Mg and a p-type GaN contact layer doped with Mg. . . . As a typical LED device having the MQW active layer for getting a good efficiency and output, Japanese Patent Kokai Hei 10-135514 discloses a nitride semiconductor light emitting device which comprises a MQW light emitting layer comprising laminated structures of undoped GaN barrier layers and undoped InGaN quantum well layers between clad layers having a wider band gap than that of the barrier layer."); Ex. PA-18, ¶¶[0004]-[0008].). Thus, a POSITA would have understood that active layer 2c refers to a conventional undoped, intrinsic region. (Ex. PA-DEC, ¶135; *see, e.g.*, PA-19, ¶[0004] (referring to an undoped region as an "intrinsic" region).)

Shimokawa discloses that "wherein said intrinsic region is between said positively-doped region and said negatively-doped region," as claimed. (Ex. PA-DEC, ¶136.) For instance, *Shimokawa* discloses that "[t]he active layer 2c is held between the first and second cladding layers 2a and 2b." (Ex. PA-3, 5:29-31, FIG. 6 (illustrating the active layer 2c sandwiched between n-type semiconductor layer 2a and p-type semiconductor layer 2b); Ex. PA-DEC, ¶136.)

Shimokawa discloses that "a first surface of said semiconductor LED contacts a first portion of a bottom surface of said optically transparent layer," as claimed. (Ex. PA-DEC, ¶137.) For instance, *Shimokawa* discloses that "the fluorescent layer 4 is formed directly on the first main surface M1 of the light-emitting layer 2." (Ex. PA-3, 9:59-61.) Figure 6 also illustrates how a first surface of the light-emitting layer 2 ("semiconductor LED") contacts a bottom portion of fluorescent layer 4:

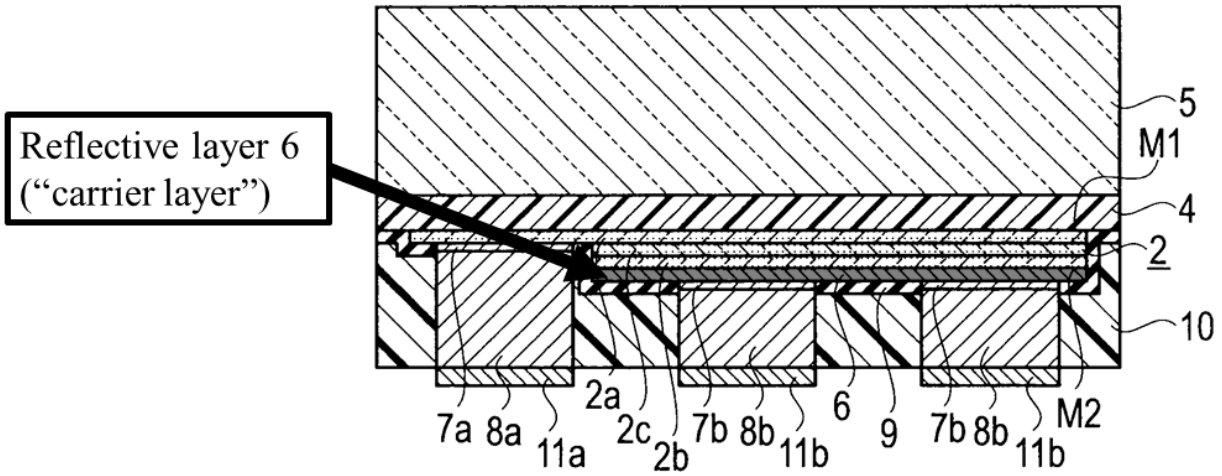


(Ex. PA-3, FIG. 6 (annotated to show contact), 9:59-61; Ex. PA-DEC, ¶137).

e. a carrier layer proximal to a second surface of said semiconductor LED, said first and second surfaces on opposing sides of said semiconductor LED;

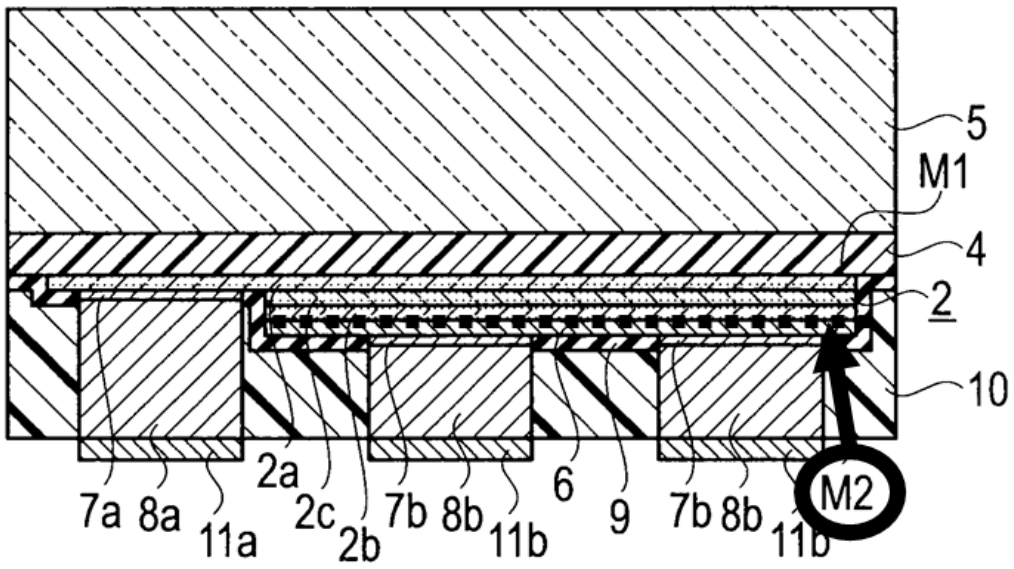
Shimokawa discloses this limitation, based at least on the broadest reasonable interpretation of the term "carrier layer." (Ex. PA-DEC, ¶¶138-140.) For example, *Shimokawa* discloses "reflective layer 6" ("carrier layer"). (Ex. PA-3, 5:14-15, FIG. 6; Ex. PA-DEC, ¶138.) "The reflective layer 6 is made of a metal such as Ag or Al." (Ex. PA-3, 6:28-29, FIG. 6.) The reflective layer 6 meets the term "carrier layer" under the broadest reasonable interpretation standard, at least because it supports the base of the semiconductor LED. (Ex. PA-3, 6:28-37, FIG. 6; Ex. PA-DEC, ¶138.) In fact, Patent Owner has applied the "carrier layer" term broadly in district court, as evidenced by Patent Owner's infringement allegations, which allege that even a thin metal interconnect layer corresponds to the claimed "carrier layer." (Ex. LIT-3, 11-12 (asserting that a copper interconnect layer is a carrier layer); Ex. PA-DEC, ¶138.) *See Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001) (citation omitted) ("A patent may

not, like a 'nose of wax,' be twisted one way to avoid anticipation and another to find infringement."). Thus, the annotated portion of Figure 6 below, which corresponds to reflective layer 6, discloses the claimed "carrier layer," based on Patent Owner's infringement allegations. (Ex. PA-DEC, ¶138.)



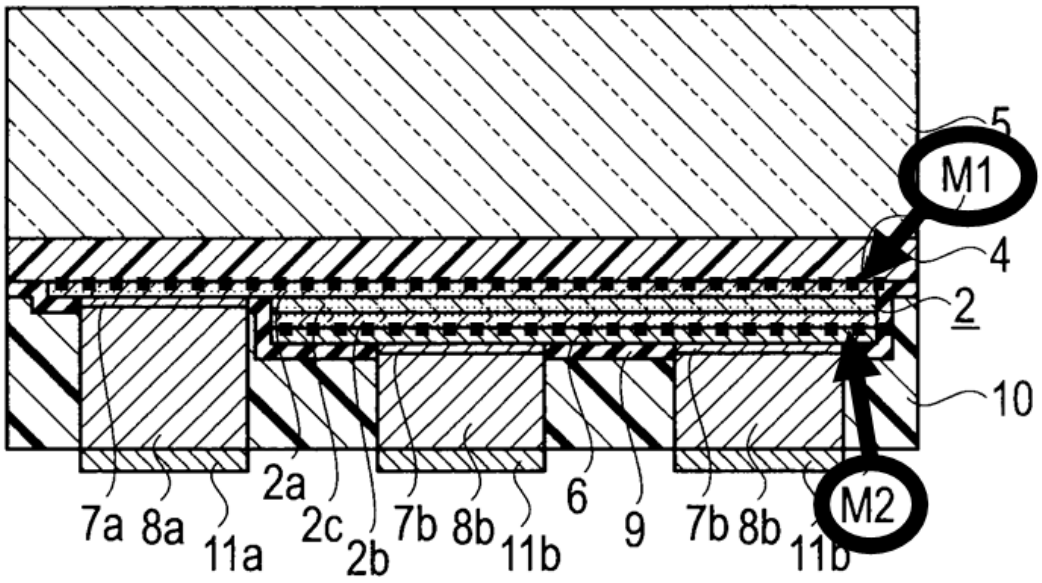
(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶138.)

Shimokawa's reflective layer 6 ("carrier layer") is "proximal to a second surface of said semiconductor LED," as claimed. (Ex. PA-DEC, ¶139.) For instance, *Shimokawa* discloses that "[t]he reflective layer 6 is provided on a first region of the second main surface M2 of the light-emitting layer 2." (Ex. PA-3, 5:10-12, FIG. 6; Ex. PA-DEC, ¶139.) The below annotated figure also illustrates this configuration:



(Ex. PA-3, FIG. 6 (annotated to show contact), 5:10-12; Ex. PA-DEC, ¶139).

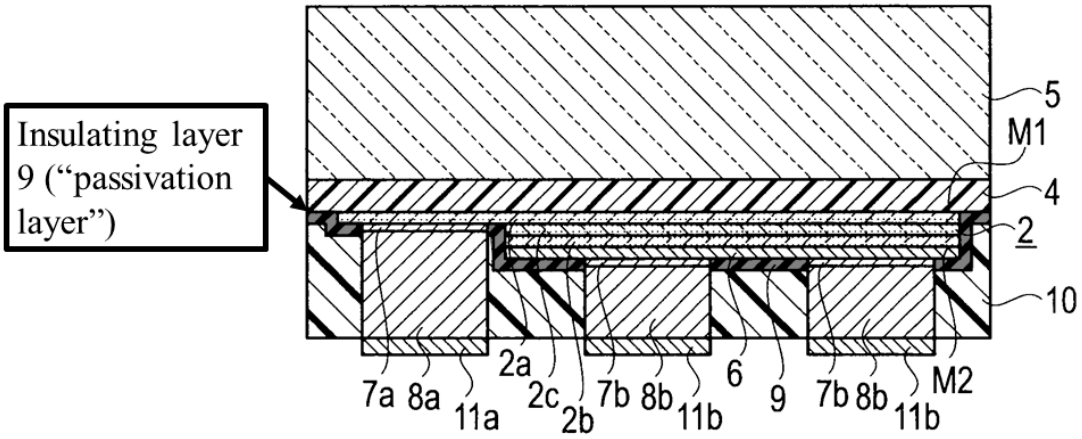
As illustrated in Figure 6 and described, the top of light-emitting layer 2 ("semiconductor LED") M1 ("first surface") and the bottom of the light-emitting layer 2 ("second surface") are on "opposing sides," as claimed:



(Ex. PA-3, FIG. 6 (annotated), 5:10-12, 9:59-61; Ex. PA-DEC, ¶140).

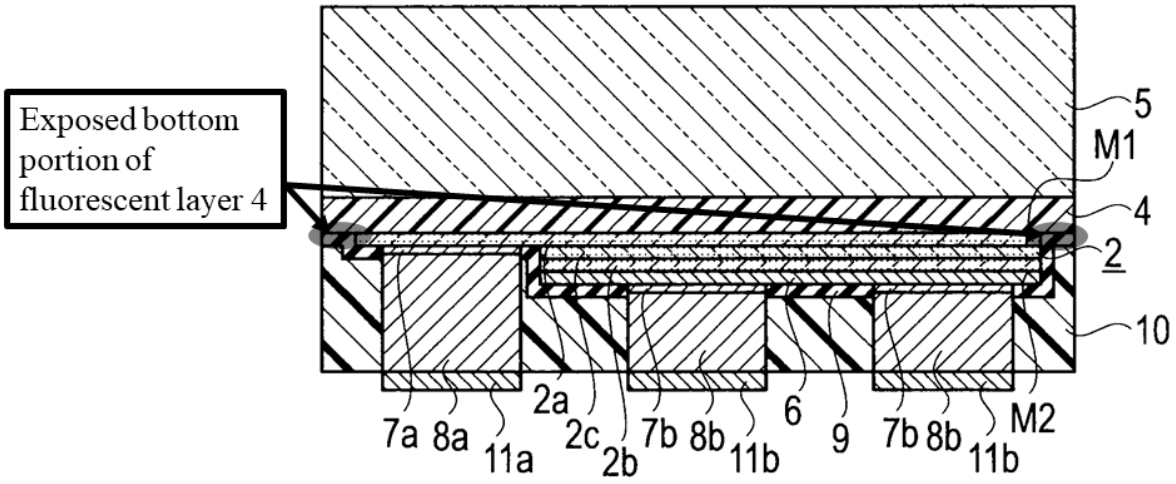
f. a passivation layer disposed on said carrier layer and on an exposed portion of said bottom surface of said optically transparent layer;

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶¶141-142.) For instance, *Shimokawa* discloses "insulating layer 9" ("passivation layer"). (Ex. PA-3, 5:4-5, FIG. 6; Ex. PA-DEC, ¶141.) "The insulating layer 9 is made of SiO, and functions as a passivation film (protective film)." (Ex. PA-3, 6:66-67.) As disclosed and illustrated in Figure 6 (and in Figures 1, 3, 4, and 7), insulating layer 9 is positioned on reflective layer 6 such that it is "disposed on" reflective layer 6 ("said carrier layer"):



(Ex. PA-3, FIG. 6 (annotated), 4:66-5:6; *see also id.*, FIGs. 1, 3, 4, and 7 (illustrating insulating layer 9 disposed on reflective layer 6); Ex. PA-DEC, ¶141).

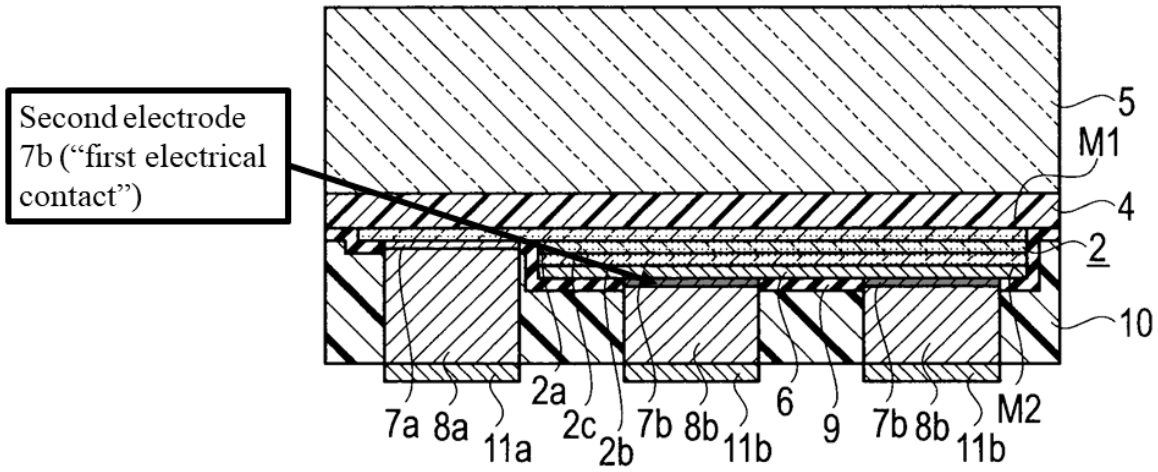
Shimokawa further discloses that insulating layer 9 ("passivation layer") is "on an exposed portion of said bottom surface of said optically transparent layer," as claimed. (Ex. PA-DEC, ¶142.) For instance, as disclosed and illustrated in Figure 6 (and in Figure 7), insulating layer 9 is positioned on a bottom portion of fluorescent layer 4 that is not covered by light-emitting layer 2 such that it is on an "exposed" bottom portion of fluorescent layer 4 ("said optically transparent layer") as claimed:



(Ex. PA-3, FIG. 6 (annotated), 4:66-5:6; *see also id.*, 10:18-25, FIG. 7 (illustrating insulating layer 9 disposed on fluorescent layer 4); Ex. PA-DEC, ¶142).

g. a first electrical contact disposed on said carrier layer in a first contact hole defined in said passivation layer; and

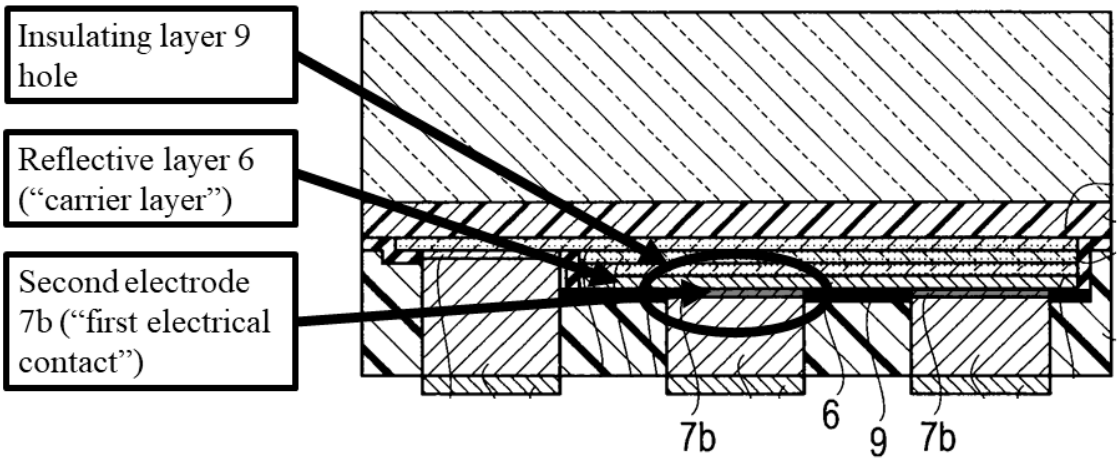
Shimokawa discloses this limitation. (Ex. PA-DEC, ¶¶143-144.) For instance, *Shimokawa* discloses "second electrode[] 7b" ("first electrical contact"). (Ex. PA-3, 4:66-5:6, FIG. 6; Ex. PA-DEC, ¶143.) "[C]urrent flows" through electrode 7b as an electrical contact to cause light emitting layer 2 to output light. (Ex. PA-3, 3:8-11, 6:59-61, 7:37-63, FIG. 6; Ex. PA-DEC, ¶143.) Two second electrodes 7b are illustrated below, either of which is a "first electrical contact." (Ex. PA-3, FIG. 6; Ex. PA-DEC, ¶143.)



(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶143.)

Shimokawa's second electrode 7b ("first electrical contact") is "disposed on said carrier layer in a first contact hole defined in said passivation layer," as claimed. (Ex. PA-DEC, ¶144.) For instance, *Shimokawa* discloses that "second electrodes 7b . . . are provided on the lower surface . . . of the reflective layer 6" ("carrier layer") during manufacturing, and accordingly are disposed on said carrier layer. (Ex. PA-3, 6:47-50, 5:14-15, FIG. 6; Ex. PA-DEC, ¶144.) After electrodes 7b are formed "on electrode portions" of the light-emitting layers, "passivation films . . . are formed by sputtering on regions other than the electrode portions of the light-emitting layers." (Ex. PA-3, 11:3-20, 5:9-11, FIG. 6; Ex. PA-DEC, ¶144.) This process surrounds second electrodes 7b with insulating layer 9 (which is made up of passivation films) given that non-electrode regions are surrounded by light-emitting layers. (Ex. PA-3, 6:66-7:7, FIG. 2; Ex. PA-DEC, ¶144.) *Shimokawa* also discloses that "insulating layer 9 entirely covers the light-emitting layer 2" except for electrode portions. (Ex. PA-3, 11:3-20; Ex. PA-DEC, ¶144.) Thus, second electrodes 7b are disposed on said carrier layer in one or more first contact layer holes in insulating layer 9, which are formed

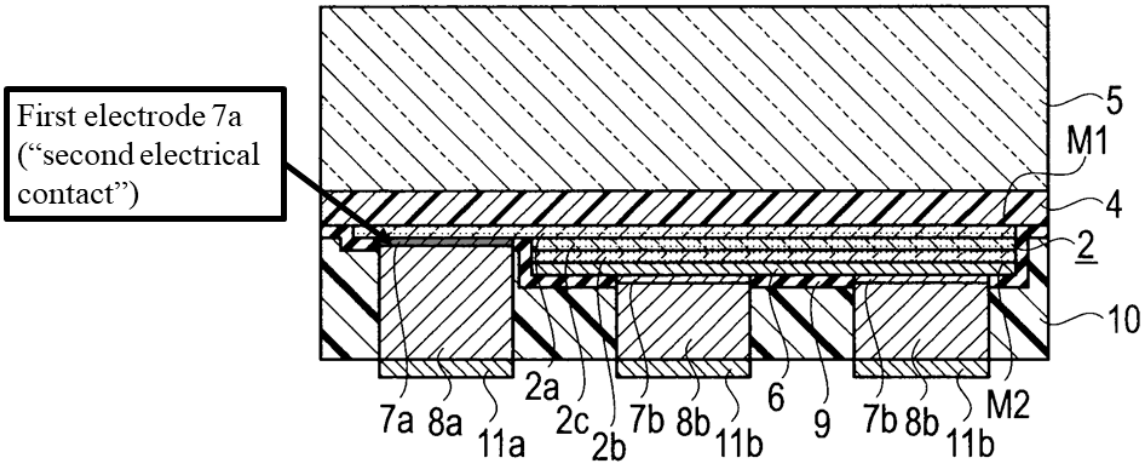
by sputtering passivation film around electrode portions. (Ex. PA-3, 11:3-20; Ex. PA-DEC, ¶144.) Figure 6 (and Figures 1, 3, 4, and 7) illustrates a cross-sectional view of this configuration, including the formed holes:



(Ex. PA-3, FIG. 6 (annotated) (illustrating that electrode 7b is layered on reflective layer 6 in at least one insulating layer 9 ("passivation layer") hole); Ex. PA-DEC, ¶144).

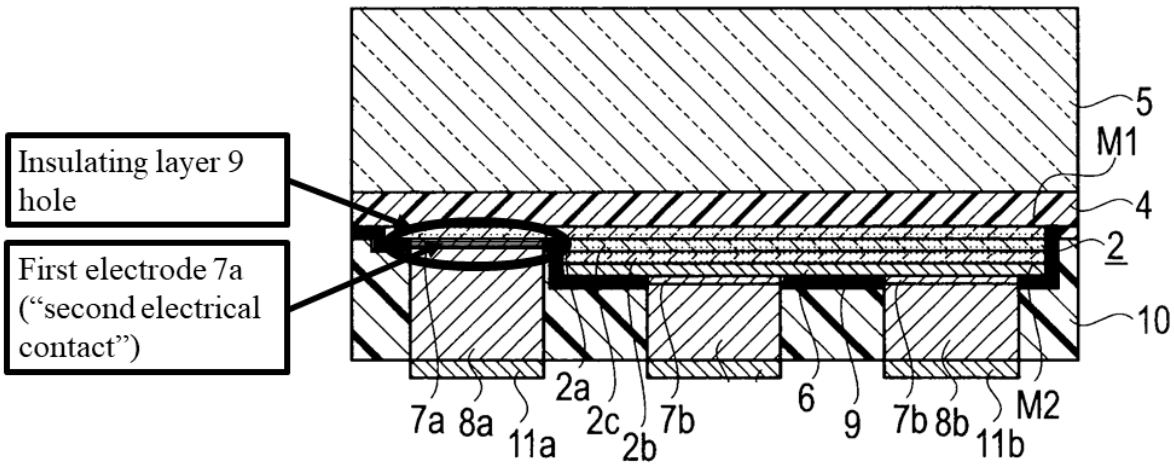
h. a second electrical contact disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED, said second electrical contact in electrical communication with said first surface of said semiconductor LED.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶¶145-49.) For instance, *Shimokawa* discloses "first electrode 7a" ("second electrical contact"). (Ex. PA-3, 4:66-5:6, FIG. 6; Ex. PA-DEC, ¶145.) "[C]urrent flows" through electrode 7a as an electrical contact to cause light emitting layer 2 to output light. (Ex. PA-3, 3:8-11, 6:51-61, 7:37-63, FIG. 6; Ex. PA-DEC, ¶145.)



(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶145.)

First electrode 7a ("second electrical contact") is "disposed in a second contact hole defined in said passivation layer," as claimed. (Ex. PA-DEC, ¶146.) Electrode 7a is formed on an "on electrode portion" of the light-emitting layers with an Ni/Au film. (Ex. PA-3, 11:3-20, 5:9-11, FIG. 6; Ex. PA-DEC, ¶146.) Thereafter, "passivation films . . . are formed by sputtering on regions other than the electrode portions of the light-emitting layers." (Ex. PA-3, 11:3-20, 5:11-13, FIG. 6; Ex. PA-DEC, ¶146.) This process surrounds first electrode 7a with insulating layer 9 (which is made up of passivation films) given that non-electrode regions are surrounded by light-emitting layers. (Ex. PA-3, 6:66-7:7, FIG. 2; Ex. PA-DEC, ¶146.) *Shimokawa* also discloses that "insulating layer 9 entirely covers the light-emitting layer 2" except for electrode portions. (Ex. PA-3, 11:3-20; Ex. PA-DEC, ¶146.) Thus, first electrode 7a is disposed in a second contact layer hole in insulating layer 9, which is formed by sputtering passivation film around electrode portions. (Ex. PA-3, 11:3-20; Ex. PA-DEC, ¶146.) Figure 6 (and Figures 1, 3, 4, and 7) illustrates a cross-sectional view of this configuration:

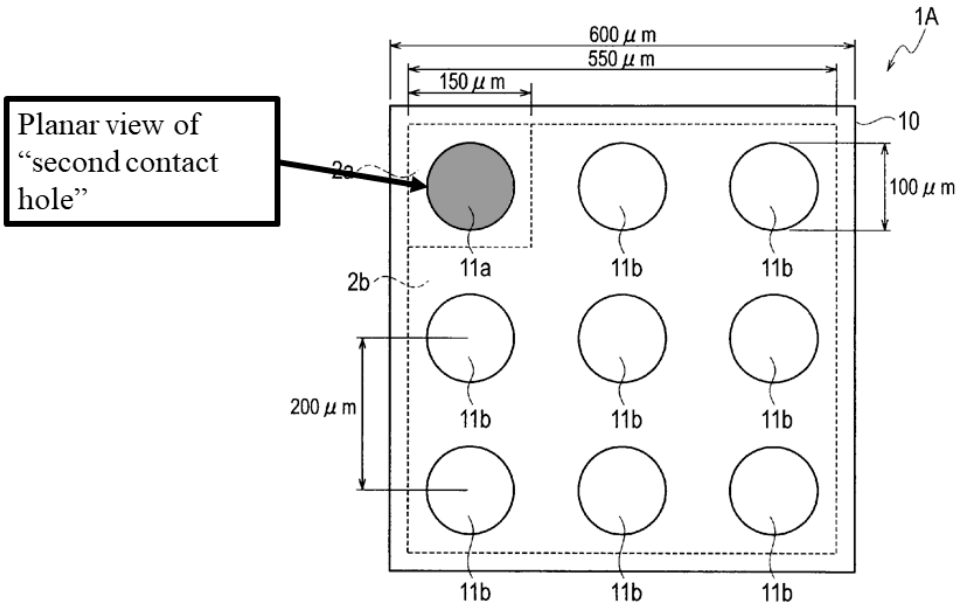


(Ex. PA-3, FIG. 6 (annotated); Ex. PA-DEC, ¶146.)

The second contact hole that the first electrode 7a ("second electrical contact") is in is also "defined in . . . said carrier layer, and said semiconductor LED," as claimed. (Ex. PA-DEC, ¶147.) As illustrated in Figure 2 and described, *Shimokawa* discloses that the first electrode 7a is formed in a cavity that does not include reflective layer 6 ("carrier layer") or layers 2b and 2c of the semiconductor LED. (Ex. PA-3, 5:39-46 ("As shown in FIG. 2, the planar shape of the first cladding layer 2a is a square 550 um on a side (see the dotted line of FIG. 2). **On a region, not including a corner region (a square 150 um on a side), of the lower surface . . . of the first**

cladding layer 2a" [see FIG. 6 above], **"the second cladding layer 2b is formed with the active layer 2c interposed therebetween.** The active layer 2c has the same shape and approximately the same area as the second cladding layer 2b.") (emphasis added), 6:27-44 ("**The reflective layer 6 is provided on the entire region (first region) of the lower surface (in FIG. 1) of the second cladding layer 2b** in the light-emitting layer 2. . . . The first electrode 7a, which is formed in a circle having a diameter of 100 um, is provided on an exposed region (second region) of the lower Surface (in FIG. 1) of the first cladding layer 2a in the light-emitting layer 2 (see FIG. 2).") (emphasis added), FIG. 2; *supra* §VI.G.2.d; Ex. PA-DEC, ¶147.)

FIG. 2



(Ex. PA-3, 5:9-46, 6:27-44, 6:66-7:7, 11:3-20, FIG. 2; Ex. PA-DEC, ¶147.) The cavity that extends from the insulating layer 9 hole (explained above) and through layers 2b, 2c, and 6 is a second contact hole for electrode 7a. (Ex. PA-3, 5:39-46, 6:27-44, FIGs. 2 and 6; Ex. PA-DEC, ¶147.) It is an opening through layers 2b, 2c, 6, and 9, as layers 2b, 2c, 6, and 9 are missing in the opening. (Ex. PA-3, 5:9-46, 6:27-44, 6:66-7:7, 11:3-20, FIGs. 2 and 6; Ex. PA-DEC, ¶147) Indeed, the claims do not specify that a hole must be formed by etching or drilling. (Ex. PA-DEC, ¶147.) Thus, and at least under the broadest reasonable interpretation, the *Shimokawa* hole is "defined in . . . said carrier layer, and said semiconductor LED." (Ex. PA-DEC, ¶147.)

Shimokawa's first electrode 7a ("second electrical contact") is "in electrical communication with said first surface of said semiconductor LED," as claimed. (Ex. PA-DEC,

¶148.) For instance, a "current" through electrodes 7a and 7b causes light emitting layer 2 to output light. (Ex. PA-3, 3:8-11, 5:12-14, 7:37-63, FIG. 6; Ex. PA-DEC, ¶148.) Because the current flows between electrodes 7a and 7b through light emitting layers 2 and the first surface of the semiconductor LED (*see supra* §VI.S.2.d) is included in this conduction path, first electrode 7a ("second electrical contact") is "in electrical communication with said first surface of said semiconductor LED." (Ex. PA-3, 3:8-11, 6:59-61, 7:37-63, FIG. 6; Ex. PA-DEC, ¶148.) Indeed, *Shimokawa* discloses that an electrical "potential" is supplied to the cladding layer 2a, which includes the first surface, through metal post 8a and electrode 7a. (Ex. PA-3, 7:37-63, FIG. 6; Ex. PA-DEC, ¶148.) For similar reasons, first electrode 7a is an "electrical contact that is in a conduction path with the first surface of the semiconductor LED," consistent with Seoul Semiconductor's proposed construction in district court. (*See supra* §IV; Ex. PA-3, 3:8-11, 6:59-61, 7:37-63, FIG. 6; Ex. PA-DEC, ¶148.)

3. Claim 2

a. The light emitting device of claim 1 wherein said optically definable material is disposed in a portion of said optically transparent layer.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶149.) As discussed previously, fluorescent layer 4 may comprise an "optically transparent layer." (*See supra* §VI.S.2.c; Ex. PA-3, 5:61, FIG. 6; Ex. PA-DEC, ¶149.) Furthermore, the "optically definable material" may be a phosphor as disclosed by *Shimokawa*. (*See supra* §VI.S.2.c; Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶149.) *Shimokawa* further discloses that "fluorescent layer 4 is formed by mixing phosphor particles in a silicone resin" such that the phosphor is "disposed in a portion of said optically transparent layer." (Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶149.) Disposing such a phosphor in the optically transparent layer shapes and defines the light spectrum that is emitted from the optical semiconductor device. (*See supra* §VI.S.2.c; Ex. PA-3, 5:62-64, 6:2-12; Ex. PA-DEC, ¶149.)

4. Claim 5

a. The light emitting device of claim 2 wherein said optically definable material is embedded in said portion of said optically transparent layer.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶150.) As discussed previously, fluorescent layer 4 may comprise an "optically transparent layer." (*See supra* §VI.S.2.c; Ex. PA-

3, 5:61, FIG. 6; Ex. PA-DEC, ¶150.) Furthermore, the "optically definable material" may be a phosphor as disclosed by *Shimokawa*. (*See supra* §VI.S.2.c; Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶150.) *Shimokawa* further discloses that "fluorescent layer 4 is formed by mixing phosphor particles in a silicone resin" such that the phosphor is "embedded in said portion of said optically transparent layer." (Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶150.) Embedding such a phosphor in the optically transparent layer shapes and defines the light spectrum that is emitted from the optical semiconductor device. (*See supra* §VI.S.2.c; Ex. PA-3, 5:62-64, 6:2-12; Ex. PA-DEC, ¶150.)

5. Claim 6

a. The light emitting device of claim 1 wherein said optically transparent layer is comprised of silicone.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶151.) As discussed previously, fluorescent layer 4 may comprise an "optically transparent layer." (*See supra* §VI.S.2.c; Ex. PA-3, 5:61, FIG. 6; Ex. PA-DEC, ¶151.) *Shimokawa* further discloses that "silicone resin [is] used for the fluorescent layer 4." (Ex. PA-3, 5:62-6:2, FIG. 6; Ex. PA-DEC, ¶151.)

6. Claim 7

a. The light emitting device of claim 6 wherein said optically definable material is comprised of phosphor.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶152.) The "optically definable material" may be a phosphor as disclosed by *Shimokawa*. (*See supra* §VI.S.2.c; Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶152.) *Shimokawa* further discloses that "fluorescent layer 4 is formed by mixing phosphor particles in a silicone resin." (Ex. PA-3, 5:62-64, FIG. 6; Ex. PA-DEC, ¶152.) Disposing such a phosphor in the optically transparent layer shapes and defines the light spectrum that is emitted from the optical semiconductor device. (*See supra* §VI.S.2.c; Ex. PA-3, 6:38-50; Ex. PA-DEC, ¶152.)

7. Claim 8

a. The light emitting device of claim 1 wherein said first and second electrical contacts are comprised of at least one of titanium, chrome, nickel, palladium, platinum, and copper.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶153.) As discussed previously, *Shimokawa* discloses second electrode 7b and first electrode 7a, which correspond to the first and second electrical contacts. (*See supra* §§VI.S.2.g-h.) *Shimokawa* further discloses that electrodes 7b and first electrode 7a may be formed of "Ni," which is the chemical symbol for "nickel." (Ex.

PA-3, 6:38-50; Ex. PA-DEC, ¶153; *see generally, e.g.*, PA-15, ¶[0008] (referring to nickel as chemical symbol Ni).)

8. Claim 9

a. The light emitting device of claim 1 wherein said passivation layer is comprised of at least one of SiO_2, SiN, AlN, Al_2O_3, an epoxy, and an electrophoretic deposited paint.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶154.) As discussed previously, *Shimokawa* discloses "insulating layer 9" ("passivation layer"). (*See supra* §VI.S.2.f.) *Shimokawa* further discloses that "[t]he insulating layer 9 is made of SiO_2" ("SiO_2"). (Ex. PA-3, 6:66, FIG. 6; Ex. PA-DEC, ¶154.)

9. Claim 10

a. The light emitting device of claim 1 wherein said first and second electrical contacts comprise an electroplated material.

Shimokawa discloses this limitation. (Ex. PA-DEC, ¶155.) As discussed previously, *Shimokawa* discloses second electrode 7b and first electrode 7a, which form the first and second electrical contacts. (*See supra* §§VI.S.2.g-h.) *Shimokawa* further discloses that metal posts 8a and 8b of the optical semiconductor device are provided on first and second electrodes 7a and 7b. (Ex. PA-3, 5:15-17, FIG. 6; Ex. PA-DEC, ¶155.) And the metal posts 8a and 8b are formed by "electroplating" the openings that the first and second electrodes 7a and 7b were formed into during manufacturing such that the "first and second electrical contacts comprise an electroplated material." (Ex. PA-3, 11:34-59, FIG. 6; Ex. PA-DEC, ¶155.)

T. SNQ20: *Shimokawa* in View of *Aldaz* Discloses or Suggests Claim 10

As explained below and in the attached declaration of Dr. Baker (Ex. PA-DEC), to the extent Patent Owner argues that *Shimokawa* does not disclose claim 10, *Shimokawa* and *Aldaz* disclose or suggest the limitations of claim 10 of the '822 patent. (Ex. PA-DEC, ¶156.)

1. Claim 10

a. The light emitting device of claim 1 wherein said first and second electrical contacts comprise an electroplated material.

To the extent Patent Owner argues that *Shimokawa* does not disclose the limitations of claim 10 (*see supra* §VI.S.9), *Shimokawa* in view of *Aldaz* suggests this limitation. (Ex. PA-DEC, ¶¶157-162.) *Shimokawa* does not explicitly disclose that its first and second electrical contacts discussed in Sections VI.S.2.g-h may be formed via an electroplating process (wherein the first

and second contacts would comprise electroplated material). However, based on the teachings of *Aldaz* and the state of the art, this feature would have been obvious. (Ex. PA-DEC, ¶157.)

For more context regarding this limitation, manufacturing techniques for electroplating one or more semiconductor LED layers were well established before the alleged time of invention. (Ex. PA-DEC, ¶158.) "Electrodeposition" (also known as electroplating) "ha[d] been used for decades" in the semiconductor industry before the alleged time of invention. (Ex. PA-30, 1818.) Indeed, electroplating processes were "widely recognized" as being "considerably simpler and more cost-effective than dry processes" to form semiconductor metals and could be used to create "either uniform films or complex-shaped objects." (*Id.*) Such "electrochemical technology ha[d] played a decisive role in the phenomenal advancement and growth of storage, interconnection, packaging and other aspects of the microelectronics industry." (Ex. PA-31, 1) The '822 patent does not claim or describe anything more than an application of such well-known and conventional electroplating manufacturing techniques. (*See* Ex. PAT-A, 7:40-54 (expressing that a metal layer may be "plated" in defined patterns), 9:19-21 (claim 10).).

Aldaz, as one example, discloses electroplating openings in an LED dielectric to form n and p contacts. (Ex. PA-DEC, ¶159.) For instance, *Aldaz* discloses a "semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region." (Ex. PA-11, abstract.) More specifically, *Aldaz*, like *Shimokawa*, discloses depositing a "dielectric layer" on an LED structure. (*Id.*, ¶[0030]; *see supra* §§VI.S.2.g-h.) Thereafter, "[o]penings for the n- and p-contacts are patterned into the dielectric, then the n- and p-contacts are formed in the openings, for example by electroplating, evaporation, or any other suitable technique." (Ex. PA-11, ¶[0030]; *see also id.*, ¶[0036].) Thus, *Aldaz* discloses forming first and second electrical contacts in dielectric openings via an electroplating process as claimed. (Ex. PA-DEC, ¶159.)

More generally, a POSITA would have understood that *Aldaz* is representative, as a variety of LED electroplating processes were understood during the relevant time period. (Ex. PA-DEC, ¶160; *see, e.g.*, Ex. PA-28, ¶[0040] ("The electrically conductive material 36 can be deposited by vacuum evaporation, sputtering, electroplating, or the like. . . . For electroplating, a thin seed layer (not shown) is deposited inside the vias 34 and the electrically conductive material 36 is electroplated to fill the vias 34 and to extend outside the vias 34. Extension or overflowing of the electroplated material outside of the vias is known as 'mushrooming' in the art. The electrically conductive material 36 lying outside of the vias 34 defines the connecting pads 42, 44."); Ex. PA-

32, ("Current spreading layer 44, p-electrode 46, and n-electrode 48 may be deposited by electroplating."); Ex. PA-10, ¶[0025] ("After etching, the structure has openings 24 and 26, as shown in FIG. 4, over the n-contact and p-contact metal, respectively. The photoresist 28 remaining from the photolithography step is left in place for the electroplating process. As mentioned previously, in current approaches to electroplating, a further masking and etching process, typically with photolithography, occurs to ensure connection between the ground plane and the electroplating seed layers of the n-contact and p-contact metals."); Ex. PA-33, Abstract.)

Thus, it would have been obvious to form the *Shimokawa* first and second electrical contacts via well-established electroplating processes, like taught by *Aldaz* and understood in the art. (Ex. PA-DEC, ¶161.) In combination, the *Shimokawa* first and second contacts (*see supra* §§VI.S.2.g-h) would be formed through insulating layer 9 as disclosed by *Aldaz* and others. (Ex. PA-DEC, ¶161.) A POSITA would have had good reason for manufacturing the contacts with such electroplating processes. (Ex. PA-DEC, ¶161.) For instance, a POSITA would have been motivated to use an electroplating technique to form the contacts at least because it was a "suitable technique" to manufacture the *Shimokawa* device. (Ex. PA-11, ¶[0030]; Ex. PA-DEC, ¶161.) Further, electroplated contacts provided "a more robust electrical connection" over other conventionally formed semiconductor contacts. (Ex. PA-2, 9:43-46; *see also, e.g.*, 1:20-4:49; Ex. PA-DEC, ¶161.) Indeed, as with any semiconductor device, a POSITA would have recognized that the *Shimokawa* lighting device would have benefited from increases in reliability, cost savings, manufacturability, etc., by electroplating its semiconductor metals. (Ex. PA-2, 14:24-43; Ex. PA-30, 1826 ("Many investigations have highlighted the advantages of electrodeposition, the main one being less costly fabrication.."); Ex. PA-DEC, ¶161.)

A POSITA would have had a reasonable expectation of success in modifying *Shimokawa* based on the teachings of *Aldaz*, at least because conventional electroplating was "relatively easy to control." (Ex. PA-2, 3:26-27; Ex. PA-DEC, ¶162.) Additionally, electroplating processes for LED contacts were well known. (*See, e.g.*, Ex. PA-10, ¶¶[0020]-[0021], [0026]-[0028], FIGs. 5-6 (disclosing techniques to electroplate n-contact metal 18 and p-contact metal 14 of an LED); Ex. PA-11, ¶[0030] ("Openings for the n- and p-contacts are patterned into the dielectric, then the n- and p-contacts are formed in the openings, for example by electroplating, evaporation, or any other suitable technique.").) Modifying *Shimokawa* based on the teachings of *Aldaz*, as discussed above, would have involved no more than an application of known technologies (e.g., semiconductor

metals and connections) according to known methods (e.g., electroplating techniques as disclosed by *Aldaz* and others) to yield the predictable result of electroplated metal contacts. (Ex. PA-DEC, ¶162.) *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

U. SNQ21: *Shimokawa* in View of *Han* Discloses or Suggests Claims 1, 2, and 5-10

Relevant to SNQ21, the claim 1 analysis set forth above explains how *Shimokawa* discloses a light-emitting layer 2 comprising an "n-type semiconductor layer" 2a, "p-type semiconductor layer" 2b, and an "active layer" 2c, which together comprise the claimed semiconductor LED. (*See supra* §VI.S.2.d; Ex. PA-3, 5:25-29; Ex. PA-DEC, ¶163.) As discussed above, *Shimokawa*'s active layer 2c discloses "an intrinsic region," as claimed. (*See supra* §VI.S.2.d.) *Shimokawa* does not, however, explicitly refer to active layer 2c as an "intrinsic" region. Thus, to the extent it is argued that *Shimokawa* does not disclose "an intrinsic region," as claimed, it would have been obvious for *Shimokawa*'s LED to include an undoped intrinsic region, similar to as taught by *Han*. (Ex. PA-DEC, ¶¶163-169.)

Conventional LEDs of the time comprised an undoped active layer. (Ex. PA-DEC, ¶164.) For example, gallium nitride (GaN) LEDs were well understood and "predominantly expected to replace existing light sources such as incandescent lamps, fluorescent lamps and mercury lamps." (Ex. PA-21, ¶[0002].) The typical GaN LED included an "undoped InGaN (an active layer . . .)" that was sandwiched between an n-type and a p-type layer. (*Id.*, ¶[0002], FIGs. 1-2.)

Han discloses one such conventional LED comprising an undoped active layer ("intrinsic region"). (Ex. PA-DEC, ¶165.) For instance, *Han* discloses a "conventional . . . nitride semiconductor LED." (Ex. PA-20, ¶[0007].) The conventional LED "includes . . . an n-type GaN layer-based clad layer 14, an active layer 16, and a p-type GaN layer-based clad layer" that are sequentially deposited on a substrate. (*Id.*, ¶[0007], FIG. 1.) To enhance light emitting efficiency, *Han* discloses that the active layer may be "formed of a multiple quantum well structure including an undoped GaN layer barrier layer and an undoped InGaN layer well layer." (*Id.*, ¶[0007].) Such an undoped active layer, often referred to as an "intrinsic" region (Ex. PA-DEC, ¶165; *see, e.g.*, PA-19, ¶[0004]), was well understood in the art. (Ex. PA-DEC, ¶165; *see*, e.g., Ex. PA-16, ¶[0004], ¶[0007] ("an undoped active layer . . . . The active layer 5 may have a multiple quantum well structure in which a plurality of GaN quantum barrier layers and a plurality of InGaN quantum well layers are alternately laminated"); Ex. PA-17, 1:14-45; Ex. PA-22, Abstract, ¶[0054]; Ex. PA-

23, ¶[0028]; Ex. PA-35, ¶[0033] ("As illustrated in FIG. 9, the active layer 105 has a multiple quantum well structure in which an undoped $In_{0.1}5Ga_{0.8}5N$ well layer (thickness: 4 nm) and an undoped $In_{0.2}Ga_{0.9}8N$ barrier layer (thickness: 8 nm) are formed in the order of a barrier layer, a well layer, a barrier layer, a well layer, a barrier layer, a well layer, and a barrier layer on then-type GaN light guide layer 104.").)

It would have been obvious for the active layer in *Shimokawa*'s LED structure to be an undoped active ("intrinsic") region, like taught by *Han* and understood in the art. (Ex. PA-DEC, ¶166.) For example, both *Shimokawa* and *Han* disclose the use of InGaN for the LED region (Ex. PA-3, 5:31-33; Ex. PA-20, ¶[0007]), and *Han* explains that the active region may be undoped (Ex. PA-20, ¶[0007]). Based on *Han*'s teachings, a POSITA would have had good reason to modify *Shimokawa*'s LED structure such that active layer 2c is an undoped active region, similar to as taught by *Han*, because, for example, such a configuration would have improved the efficiency of the *Shimokawa* lighting system. (Ex. PA-20, ¶[0007] (describing efficiency benefits associated with an LED that comprises an undoped, multiple quantum well structure); Ex. PA-17, 1:14-33 (same); Ex. PA-DEC, ¶166.) Additionally, "if [an] active layer is doped with impurities, [a] light emitting element is likely to be deteriorated" more quickly over time as compared to a light emitting element with an undoped active layer. (Ex. PA-35, ¶[0034]; Ex. PA-DEC, ¶166.) Including the *Han* active layer comprising undoped barrier and well layers in the *Shimokawa* LED structure would have "extend[ed] the life" and improved the reliability of the structure. (Ex. PA-35, ¶¶[0034], [0007], Abstract; Ex. PA-DEC, ¶166.)

As a POSITA would have appreciated, such a substitution of different types of active layers would have represented a simple substitution of one known element for another to obtain a predictable result, especially here, where *Shimokawa* itself suggests that active layer 2c is undoped, as discussed above in Section VI.S.2.d. (Ex. PA-DEC, ¶167.) Indeed, "when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious." *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (citation and internal quotation marks omitted). Furthermore, the modification would have been obvious to try. (Ex. PA-DEC, ¶167.) A POSITA would have appreciated that the active layer could have been doped or undoped. (*Id.*) Implementing the *Shimokawa* active layer as an undoped, intrinsic layer, as taught by *Han* and others, would have been an obvious choice. (*Id.*)

A POSITA would have had a reasonable expectation of success in modifying *Shimokawa* based on the teachings of *Han*, at least because the LED configuration was well understood in the art. (*See, e.g.*, Ex. PA-16, ¶[0004], ¶[0007]; Ex. PA-17, 1:14-33 (same); Ex. PA-20, ¶[0007]; Ex. PA-22, Abstract, ¶[0054]; Ex. PA-23, ¶[0028]; Ex. PA-DEC, ¶168.) And, as noted above, both *Shimokawa* and *Han* disclose the use of InGaN for the LED region. (Ex. PA-3, 5:31-33; Ex. PA-20, ¶[0007].) Modifying *Shimokawa* as discussed above would have involved no more than an application of known technologies (e.g., the LED structure described in *Shimokawa* and the active region described in *Han*) according to known methods (e.g., conventional LED manufacturing techniques, like those described in *Shimokawa* and *Han*) to yield the predictable result of an LED that includes an undoped active layer. (Ex. PA-DEC, ¶168.) *See KSR*, 550 U.S. at 416.

Shimokawa discloses the remaining features of claims 1, 2, and 5-10 as set forth in the preceding sections. (*See supra* §VI.S.)

V. SNQ22: *Shimokawa* in View of *Han* and *Aldaz* Discloses or Suggests Claim 10

Shimokawa in view of *Han* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.T, as the inclusion of *Han* does not detract from the relied upon disclosures in Section VI.T. (*See supra* §VI.T.)

W. SNQ23: *Shimokawa* in View of *Nagahama* Discloses or Suggests Claims 1, 2, and 5-10

Relevant to SNQ23, the claim 1 analysis set forth above explains how *Shimokawa* discloses a light-emitting layer 2 comprising an "n-type semiconductor layer" 2a, "p-type semiconductor layer" 2b, and an "active layer" 2c, which together comprise the claimed semiconductor LED. (*See supra* §VI.S.2.d; Ex. PA-3, 5:25-29; Ex. PA-DEC, ¶171.) As discussed above, *Shimokawa*'s active layer 2c discloses "an intrinsic region," as claimed. (*See supra* §VI.S.2.d.) *Shimokawa* does not, however, explicitly refer to active layer 2c as an "intrinsic" region. Thus, to the extent it is argued that *Shimokawa* does not disclose "an intrinsic region," as claimed, it would have been obvious for *Shimokawa*'s LED to include an undoped intrinsic region, similar to as taught by *Nagahama*. (Ex. PA-DEC, ¶¶171-177.)

Conventional LEDs of the time comprised an undoped active layer. (Ex. PA-DEC, ¶172.) For example, gallium nitride (GaN) LEDs were well understood and "predominantly expected to replace existing light sources such as incandescent lamps, fluorescent lamps and mercury lamps."

(Ex. PA-21, ¶[0002].) The typical GaN LED included an "undoped InGaN (an active layer . . .)" that was sandwiched between an n-type and a p-type layer. (*Id.*, ¶[0002], FIGs. 1-2.)

Nagahama discloses one such conventional LED comprising an undoped active layer ("intrinsic region"). (Ex. PA-DEC, ¶173.) For instance, *Nagahama* discloses a "fabrication method of a nitride semiconductor device comprising a nitride semiconductor . . . , such as a light emitting diode (LED)." (Ex. PA-36, 1:7-13.) The active layer of the LED includes an "un-doped" well layer that "increase[s] the light emitting efficiency of the light emitting device." (*Id.*, 20:3-24.), FIG. 1.)

It would have been obvious for the active layer in *Shimokawa*'s LED structure to be an undoped active ("intrinsic") region, like taught by *Nagahama* and understood in the art. (Ex. PA-DEC, ¶174.) For example, both *Shimokawa* and *Nagahama* disclose the use of InGaN for the LED region (Ex. PA-3, 5:31-33; Ex. PA-36, 20:4-24), and *Nagahama* explains that the active region may be undoped (Ex. PA-36, 20:4-21:9). Based on *Nagahama*'s teachings, a POSITA would have had good reason to modify *Shimokawa*'s LED structure such that active layer 2c is an undoped active region, similar to as taught by *Nagahama*, because, for example, such a configuration would have improved the efficiency of the *Shimokawa* lighting system and supported high output applications. (Ex. PA-36, 20:4-21:9; Ex. PA-DEC, ¶174.)

As a POSITA would have appreciated, such a substitution of different types of active layers would have represented a simple substitution of one known element for another to obtain a predictable result, especially here, where *Shimokawa* itself suggests that active layer 2c is undoped, as discussed above in Section VI.S.2.d. (Ex. PA-DEC, ¶175.) Indeed, "when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious." *See KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (citation and internal quotation marks omitted). Furthermore, the modification would have been obvious to try. (Ex. PA-DEC, ¶175.) A POSITA would have appreciated that the active layer could have been doped or undoped. (Ex. PA-DEC, ¶175.) Implementing the *Shimokawa* active layer as an undoped, intrinsic layer, as taught by *Nagahama* and others, would have been an obvious choice. (Ex. PA-DEC, ¶175.)

A POSITA would have had a reasonable expectation of success in modifying *Shimokawa* based on the teachings of *Nagahama*, at least because both *Shimokawa* and *Nagahama* disclose

the use of InGaN for the LED region. (Ex. PA-3, 5:31-33; Ex. PA-20, 20:4-24.) Modifying *Shimokawa* as discussed above would have involved no more than an application of known technologies (e.g., the LED structure described in *Shimokawa* and the active region described in *Nagahama*) according to known methods (e.g., conventional LED manufacturing techniques, like those described in *Shimokawa* and *Nagahama*) to yield the predictable result of an LED that includes an undoped active layer. (Ex. PA-DEC, ¶176.) *See KSR*, 550 U.S. at 416.

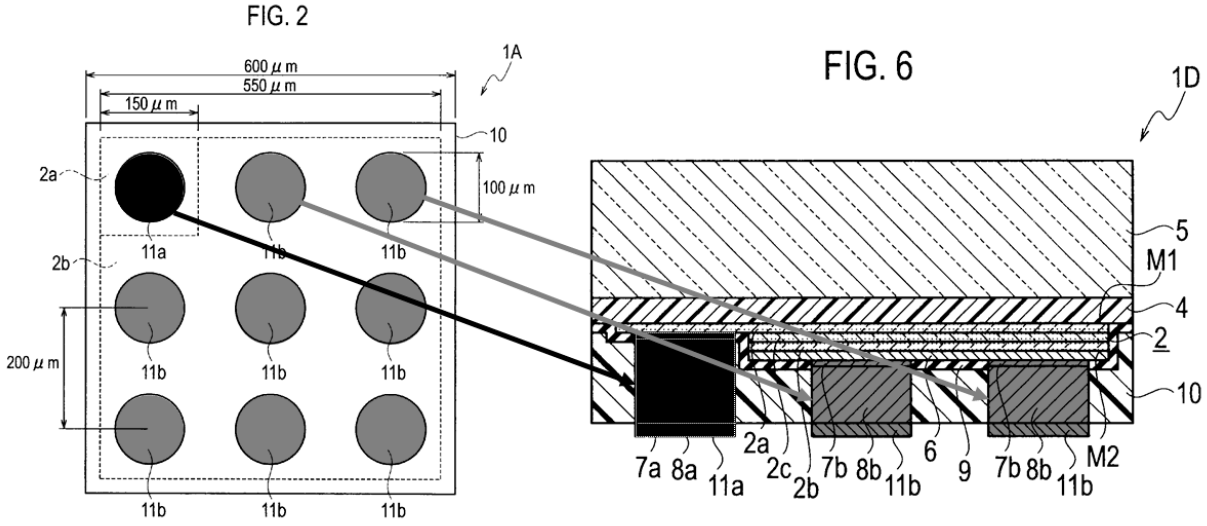
Shimokawa discloses the remaining features of claims 1, 2, and 5-10 as set forth in the preceding sections. (*See supra* §VI.S.)

X. SNQ24: *Shimokawa* in View of *Nagahama* and *Aldaz* Discloses or Suggests Claim 10

Shimokawa in view of *Nagahama* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.T, as the inclusion of *Nagahama* does not detract from the relied upon disclosures in Section VI.T. (*See supra* §VI.T.)

Y. SNQ25: *Shimokawa* in view *Keller* Discloses or Suggests Claims 1, 2, and 5-10

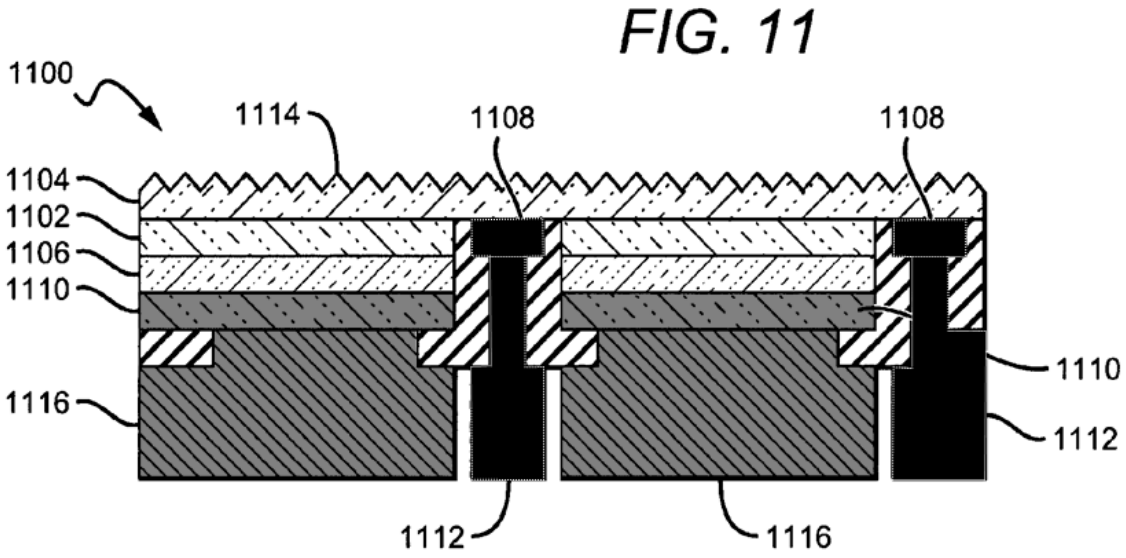
To the extent Patent Owner argues that *Shimokawa* does not disclose the limitations of claim 1.h (*see supra* §VI.S.2.h), *Shimokawa* in view of *Keller* suggests this limitation. (Ex. PA-DEC, ¶¶179-87.) As discussed previously, *Shimokawa* discloses a light-emitting layer 2 comprising an "n-type semiconductor layer" 2a, a "p-type semiconductor layer" 2b, and an "active layer" 2c, which together comprise a semiconductor LED. (*See supra* §VI.S.2.d; Ex. PA-3, 5:25-29; Ex. PA-DEC, ¶179.) *Shimokawa* further discloses forming a ***single electrode 7a on the n-type layer*** and forming a ***plurality of electrodes 7b on the p-type layer***, thereby forming a current path to power the LED semiconductor device. (*See supra* §VI.S.2.g-h; Ex. PA-3, 3:8-11, 4:66-5-6, 6:38-61, 7:37-63, FIG. 6; Ex. PA-DEC, ¶179.)



(Ex. PA-3, FIGs. 2, 6 (annotated) (illustrating that the *Shimokawa* device includes a plurality of p-region connections (grey), but only one n-region connection (black)), 3:8-11, 4:66-5-6, 6:38-61.) As explained below, it would have been obvious to form an additional n-type electrode in the *Shimokawa* device, such that it would include a plurality of n-type electrodes and a plurality of p-type electrodes as suggested by *Keller*. (Ex. PA-DEC, ¶179.)

Keller, like *Shimokawa*, relates to configurations for LED devices. (Ex. PA-37, title ("Wire Bond Free Wafer Level LED"), ¶¶[0004]-[0017] (discussing various configurations of prior art LED devices); Ex. PA-DEC, ¶180.) For instance, *Keller* describes a typical nitride LED that was known in the art. (*Id.*, ¶[0012].) Like the *Shimokawa* semiconductor LED, *Keller* discloses various configurations comprising an "active region" that is "interposed between" an "n-type layer" and a "p-type layer." (*Id.*, ¶¶[0012], [0072].)

Unlike the *Shimokawa* device, which includes a single n-region connection and a plurality of p-region connections, Keller discloses an LED that includes both a ***plurality of n-region connections*** and a ***plurality of p-region connections***. (Ex. PA-DEC, ¶181.) With respect to Figure 11, *Keller* discloses an active region 1102 that is interposed between an n-type layer 1104 and a p-type layer 1106. (Ex. PA-37, ¶[0072].) Critically, Keller discloses that "[t]he n-type layer 1104 is contacted in several locations by multiple n-pads 1108" and that "the p-type layer 1106 is contacted in several locations by multiple p-pads 1110." (*Id.*) The multiple n-pads 1108 and p-pads 1106 form n and p connections with multiple n-electrodes 1108 and multiple p-electrodes 1116, as illustrated in the following figure. (*Id.*, ¶[0072], FIG. 11.)



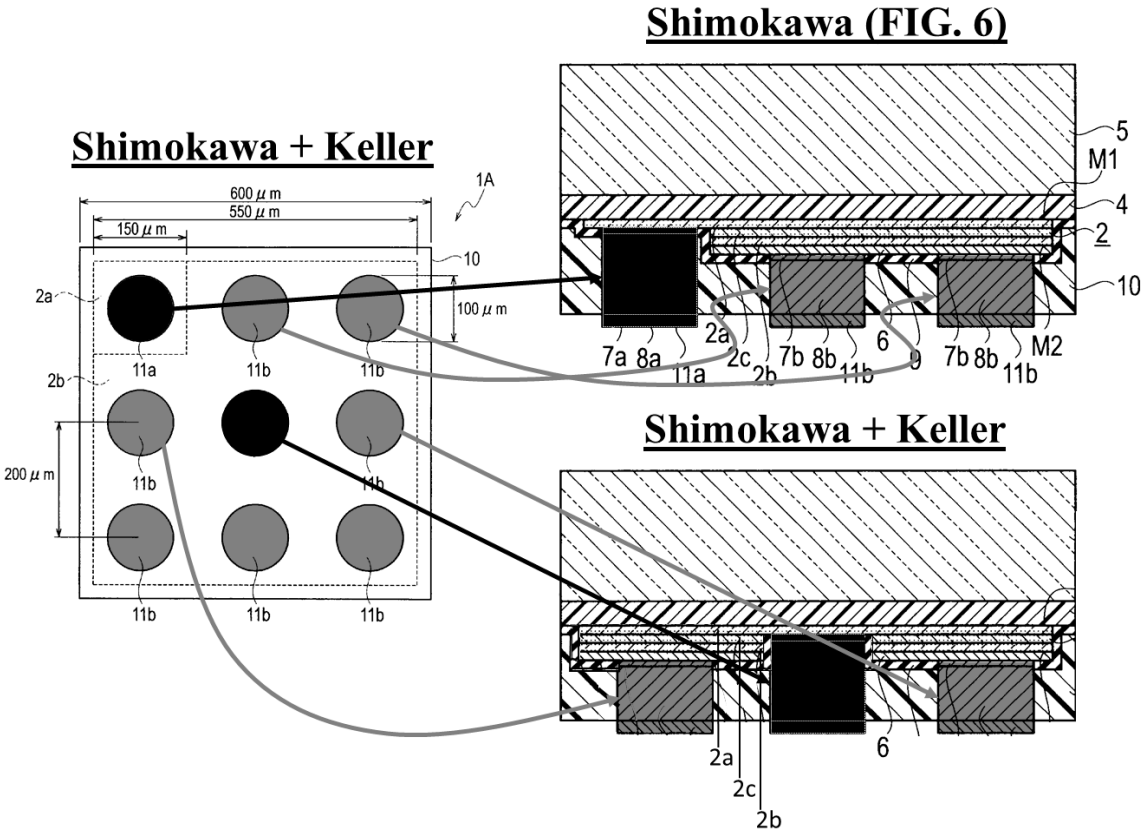
(*Id.*, ¶[0072], FIG. 11 (annotated) (illustrating that the *Keller* device includes a plurality of p-region connections (grey), and a plurality of n-region connections (black)).)

More specifically, *Keller* discloses "a second electrical contact disposed in a second contact hole defined in" a passivation layer and a semiconductor LED, as claimed. (Ex. PA-DEC, ¶182.) For instance, *Keller* discloses n-pad 1108 ("a second electrical contact"). (Ex. PA-37, ¶[0072], FIG. 11.) The n-pad 1108 is deposited in a via that is etched through the p-type layer 1106 and the active region 1102 of a semiconductor LED (*id.*, ¶[0073], FIG. 11) as well as a dielectric layer to expose the n-type layer 1104 (*id.*, ¶[0073] (citing the FIGs. 4a-g manufacturing process), ¶¶[0048]-[0057] (explaining how dielectric spacing material 416 is patterned in a via and etched away to form an n-region connection), FIGs. 4b-g (illustrating the same)).

Keller additionally discloses that "[t]he n-type layer 1104 is contacted in several locations by multiple n-pads 1108" and that "[m]ultiple n-electrodes 1112 . . . provide multiple electrical paths to the n-type layer 1104 through the n-pads 1108." (Ex. PA-37, ¶[0072], FIG. 11.) Because current flows between the n-electrodes 1112 and pads 1108 through the active region 1102 and p-layer 1106 and a first surface of the n-type layer semiconductor LED is included in this conduction path, *Keller* additionally discloses or suggests that an additional n-pad 1108 would be in electrical communication with a first surface of a semiconductor LED. (Ex. PA-37, ¶¶[0072], [0011]-[0013], FIG. 11; Ex. PA-DEC, ¶183.)

It would have been obvious to etch a contact hole through the *Shimokawa* passivation layer, carrier layer, and semiconductor LED to form an additional n-region contact, as suggested by

Keller. (Ex. PA-DEC, ¶184.) As discussed above, *Keller* describes etching away layers that separate a contact region of an LED from an n-type layer to form a second n-region contact. (Ex. PA-37, ¶[0073], FIG. 11.) *Keller* also discloses forming corner n-region contacts and non-corner n-region contacts (Ex. PA-36, FIG. 11), which provides guidance to modifying the *Shimokawa* device that only discloses a corner n-contact (Ex. PA-3, FIGs. 2, 6). Thus, modifying the *Shimokawa* device as suggested by *Keller* would entail etching or forming a hole through the *Shimokawa* "reflective layer 6" ("carrier layer"), as well as the "p-type semiconductor layer" 2b and the "active layer" 2c, to form an additional n-region contact. (Ex. PA-DEC, ¶184; *see supra* §§VI.S.2.d-e.) A passivation layer hole would further separate the new n-region contact from the other LED layers as suggested by *Keller*, and would have been required to avoid short circuiting semiconductor layers. (Ex. PA-37, ¶¶[0048]-[0049], [0073]; Ex. PA-DEC, ¶184.) The additional n-region contact would have been in "electrical communication with said first surface of said semiconductor LED," as described previously. (Ex. PA-DEC, ¶184.) The following figures illustrate an example configuration of the *Shimokawa-Keller* combination. (Ex. PA-DEC, ¶184.) However, a POSITA would have understood that multiple n-contacts at other locations would have been obvious for similar reasons, as suggested by *Keller*.



(Ex. PA-DEC, ¶184.)

A POSITA would have had good reason to modify *Shimokawa* as suggested by *Keller.* (Ex. PA-DEC, ¶185.) As compared to conventional LED devices comprising a single n-region contact (such as the *Shimokawa* device), the *Keller* configuration provides improved "current spreading" across substantially all of the n-type and p-type layers. (Ex. PA-37, ¶[0074]; Ex. PA-DEC, ¶185.) Furthermore, the configuration would have allowed for better scalability and enable the construction of differently sized LED devices. (Ex. PA-37, ¶[0074]; Ex. PA-DEC, ¶185.) Indeed, it was well understood in the art to use multiple n-region contacts as suggested by *Keller* for the efficiency benefits associated with better current distribution, less contact resistance, and better uniformity. (Ex. PA-38, ¶[0062] ("[M]aking multiple P and N contact pads on one LED result[s] in a better uniformity of the current distribution and spreading."); Ex. PA-39, ¶[0054] ("[I]t may be desirable to have multiple n-contact electrodes on n-doped GaN layer 34 to spread current density."); Ex. PA-40, ¶[0395] ("If the size of n-electrode 11 is small, contact resistance at the contact portion between n-electrode 11 and the nitride semiconductor substrate becomes larger, and hence voltage drop at the contact portion becomes lager. It may become necessary to arrange the n-electrodes 11 at a plurality of portions on the second main surface in order to alleviate the influence of the voltage drop.").)

A POSITA would have had a reasonable expectation of success in modifying *Shimokawa* based on the teachings of *Keller*, at least because the LED configuration was well understood in the art. (*See, e.g.*, Ex. PA-37, FIG. 11; Ex. PA-38, ¶[0062]; Ex. PA-39, ¶[0054]; Ex. PA-40, ¶[0395]; Ex. PA-DEC, ¶186.) And, as discussed previously, both *Shimokawa* and *Keller* pertain to the use of GaN semiconductors. (Ex. PA-3, 5:31-33; Ex. PA-37, ¶¶[0012], [0042].) Modifying *Shimokawa* as discussed would have involved no more than an application of known technologies (e.g., LEDs with multiple n- and p-region contacts) according to known methods (e.g., conventional LED manufacturing techniques, like those described in *Shimokawa* and *Keller*) to yield the predictable result of an LED that includes a second electrical contact disposed in a second contact hole defined in said passivation layer, said carrier layer, and said semiconductor LED, said second electrical contact in electrical communication with said first surface of said semiconductor LED. (Ex. PA-DEC, ¶186.) *See KSR*, 550 U.S. at 416.

Shimokawa discloses the remaining features of claims 1, 2, and 5-10 as set forth in the preceding sections. (*See supra* §VI.S.)

Z. SNQ26: *Shimokawa* in View of *Keller* and *Aldaz* Discloses or Suggests Claim 10

Shimokawa in view of *Keller* and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Section VI.T, as the inclusion of *Keller* does not detract from the relied upon disclosures in Section VI.T. (*See supra* §VI.T.)

AA. SNQ27: *Shimokawa* in View of *Keller* and *Han* Discloses or Suggests Claims 1, 2, and 5-10

Shimokawa in view of *Keller* and *Han* discloses or suggests the limitations of claims 1, 2, and 5-10 for substantially the same reasons discussed *supra* in Section VI.U, as the inclusion of *Keller* does not detract from the relied upon disclosures in Section VI.U. (*See supra* §VI.U.)

BB. SNQ28: *Shimokawa* in View of *Keller*, *Han*, and *Aldaz* Discloses or Suggests Claim 10

Shimokawa in view of *Keller*, *Han*, and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Sections VI.T-U, as the inclusion of *Keller* does not detract from the relied upon disclosures in Sections VI.T-U. (*See supra* §§VI.T-U.)

CC. SNQ29: *Shimokawa* in view *Keller* and *Nagahama* of Discloses or Suggests Claims 1, 2, and 5-10

Shimokawa in view of *Keller* and *Nagahama* discloses or suggests the limitations of claims 1, 2, and 5-10 for substantially the same reasons discussed *supra* in Section VI.W, as the inclusion of *Keller* does not detract from the relied upon disclosures in Section VI.W. (*See supra* §VI.W.)

DD. SNQ30: *Shimokawa* in view of *Keller*, *Nagahama*, and *Aldaz* Discloses or Suggests Claim 10

Shimokawa in view of *Keller*, *Nagahama*, and *Aldaz* discloses or suggests the limitations of claim 10 for substantially the same reasons discussed *supra* in Sections VI.T, W, as the inclusion of *Keller* does not detract from the relied upon disclosures in Sections VI.T, W. (*See supra* §§VI.T, W.)

VII. Detailed Explanation of the Pertinence and Manner of Applying the Prior Art to the Claims

A. Bases for Proposed Rejections of the Claims

The following is a quotation of pre-AIA 35 U.S.C. § 102 that forms the basis for all of the identified prior art:

> A person shall be entitled to a patent unless . . .
>
> (e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States

> before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language . . . .

The following is a quotation of pre-AIA 35 U.S.C. § 103(a) that forms the basis of all of the following obviousness rejections:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negative by the manner in which the invention was made.

The question under 35 U.S.C. § 103 is whether the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention. In *KSR International Co. v. Teleflex Inc*., 550 U.S. 398 (2007), the Court mandated that an obviousness analysis allow for "common sense" and "ordinary creativity," while at the same time not requiring "precise teachings directed to the specific subject matter of the challenged claim[s]." *KSR*, 550 U.S. at 418, 420-421. According to the Court, "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* at 416. In particular, the Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art." *Id.* at 401. The Court also stated that "when a patent simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the combination is obvious." *Id.* at 417.

The Office has provided further guidance regarding the application of *KSR* to obviousness questions before the Office.

> If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in

> the same way, using the technique is obvious unless its actual application is beyond his or her skill.

MPEP § 2141(I) (quoting *KSR* at 417.)

The MPEP identifies many exemplary rationales from *KSR* that may support a conclusion of obviousness. Some examples that may apply to this reexamination include:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of a known technique to improve similar devices in the same way;
- Applying a known technique to improve devices in the same way;
- Choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success ("obvious to try")

MPEP § 2141(III).

In addition, the Office has published *Post-KSR* Examination Guideline Updates. *See* Fed. Reg. Vol. 75, 53464 (the "Guideline Updates"). The Guideline Updates discuss developments after *KSR* and provide teaching points from recent Federal Circuit decisions on obviousness. Some examples are listed below:

> A claimed invention is likely to be obvious if it is a combination of known prior art elements that would reasonably have been expected to maintain their respective properties or functions after they have been combined.

Id. at 53646.

> A combination of known elements would have been prima facie obvious if an ordinary skilled artisan would have recognized an apparent reason to combine those elements and would have known how to do so.

Id. at 53648.

> Common sense may be used to support a legal conclusion of obviousness so long as it is explained with sufficient reasoning.

Id.

B. Proposed Rejections

Pursuant to 37 C.F.R. § 1.510(b)(2), Requester identifies claims 1, 2, and 5-10 as the claims for which reexamination is requested. The proposed rejections below, in conjunction with the analysis in Sections IV-V above and the attached declaration of Dr. Baker (Ex. PA-DEC), provide

a detailed explanation of the pertinence and manner of applying the prior art to each of claims 1, 2, and 5-10.

1. Proposed Rejection #1

Claims 1, 2, 5-7, and 9 are anticipated by or obvious over *Epler* under 35 U.S.C. §§ 102 and 103(a), as shown by the discussion above in Section VI.A and the declaration of Dr. Baker provided in Exhibit PA-DEC.

2. Proposed Rejection #2

Claim 8 is obvious over *Epler* in view of *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.B and the declaration of Dr. Baker provided in Exhibit PA-DEC.

3. Proposed Rejection #3

Claim 10 is obvious over *Epler* in view of *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.C and the declaration of Dr. Baker provided in Exhibit PA-DEC.

4. Proposed Rejection #4

Claims 1, 2, 5-7, and 9 are obvious over by *Epler* in view of *Lester* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.D and the declaration of Dr. Baker provided in Exhibit PA-DEC.

5. Proposed Rejection #5

Claim 8 is obvious over *Epler* in view of *Lester* and *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.E and the declaration of Dr. Baker provided in Exhibit PA-DEC.

6. Proposed Rejection #6

Claim 10 is obvious over *Epler* in view of *Lester* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.F and the declaration of Dr. Baker provided in Exhibit PA-DEC.

7. Proposed Rejection #7

Claims 1, 2, 5-7, and 9 are obvious over *Epler* in view of *Han* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.G and the declaration of Dr. Baker provided in Exhibit PA-DEC.

8. Proposed Rejection #8

Claim 8 is obvious over *Epler* in view of *Han* and *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.H and the declaration of Dr. Baker provided in Exhibit PA-DEC.

9. Proposed Rejection #9

Claim 10 is obvious over *Epler* in view of *Han* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.I and the declaration of Dr. Baker provided in Exhibit PA-DEC.

10. Proposed Rejection #10

Claims 1, 2, 5-7, and 9 are obvious over by *Epler* in view of *Han* and *Lester* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.J and the declaration of Dr. Baker provided in Exhibit PA-DEC.

11. Proposed Rejection #11

Claim 8 is obvious over *Epler* in view of *Lester*, *Han*, and *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.K and the declaration of Dr. Baker provided in Exhibit PA-DEC.

12. Proposed Rejection #12

Claim 10 is obvious over *Epler* in view of *Lester*, *Han*, and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.L and the declaration of Dr. Baker provided in Exhibit PA-DEC.

13. Proposed Rejection #13

Claims 1, 2, 5-7, and 9 are obvious over *Epler* in view of *Nagahama* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.M and the declaration of Dr. Baker provided in Exhibit PA-DEC.

14. Proposed Rejection #14

Claim 8 is obvious over *Epler* in view of *Nagahama* and *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.N and the declaration of Dr. Baker provided in Exhibit PA-DEC.

15. Proposed Rejection #15

Claim 10 is obvious over *Epler* in view of *Nagahama* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.O and the declaration of Dr. Baker provided in Exhibit PA-DEC.

16. Proposed Rejection #16

Claims 1, 2, 5-7, and 9 are obvious over by *Epler* in view of *Nagahama* and *Lester* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.P and the declaration of Dr. Baker provided in Exhibit PA-DEC.

17. Proposed Rejection #17

Claim 8 is obvious over *Epler* in view of *Lester*, *Nagahama*, and *Fan* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.Q and the declaration of Dr. Baker provided in Exhibit PA-DEC.

18. Proposed Rejection #18

Claim 10 is obvious over *Epler* in view of *Lester*, *Nagahama*, and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.R and the declaration of Dr. Baker provided in Exhibit PA-DEC.

19. Proposed Rejection #19

Claims 1, 2, and 5-10 are anticipated by *Shimokawa* under 35 U.S.C. § 102, as shown by the discussion above in Section VI.S and the declaration of Dr. Baker provided in Exhibit PA-DEC.

20. Proposed Rejection #20

Claim 10 is obvious over *Shimokawa* in view of *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.T and the declaration of Dr. Baker provided in Exhibit PA-DEC.

21. Proposed Rejection #21

Claims 1, 2, and 5-10 are obvious over *Shimokawa* in view of *Han* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.U and the declaration of Dr. Baker provided in Exhibit PA-DEC.

22. Proposed Rejection #22

Claims 10 is obvious over *Shimokawa* in view of *Han* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.V and the declaration of Dr. Baker provided in Exhibit PA-DEC.

23. Proposed Rejection #23

Claims 1, 2, and 5-10 are obvious over *Nagahama* in view of *Han* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.W and the declaration of Dr. Baker provided in Exhibit PA-DEC.

24. Proposed Rejection #24

Claims 10 is obvious over *Shimokawa* in view of *Nagahama* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.X and the declaration of Dr. Baker provided in Exhibit PA-DEC.

25. Proposed Rejection #25

Claims 1, 2, and 5-10 are obvious over *Shimokawa* in view of *Keller* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.Y and the declaration of Dr. Baker provided in Exhibit PA-DEC.

26. Proposed Rejection #26

Claim 10 is obvious over *Shimokawa* in view of *Keller* and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.Z and the declaration of Dr. Baker provided in Exhibit PA-DEC.

27. Proposed Rejection #27

Claims 1, 2, and 5-10 are obvious over *Shimokawa* in view of *Keller* and *Han* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.AA and the declaration of Dr. Baker provided in Exhibit PA-DEC.

28. Proposed Rejection #28

Claims 10 is obvious over *Shimokawa* in view of *Keller*, *Han*, and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.BB and the declaration of Dr. Baker provided in Exhibit PA-DEC.

29. Proposed Rejection #29

Claims 1, 2, and 5-10 are obvious over *Shimokawa* in view of *Keller* and *Nagahama* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.CC and the declaration of Dr. Baker provided in Exhibit PA-DEC.

30. Proposed Rejection #30

Claims 10 is obvious over *Shimokawa* in view of *Keller*, *Nagahama*, and *Aldaz* under 35 U.S.C. § 103(a), as shown by the discussion above in Section VI.DD and the declaration of Dr. Baker provided in Exhibit PA-DEC.

VIII. Conclusion

For the reasons set forth above, the Requester has established at least one substantial new question of patentability with respect to claims 1, 2, and 5-10 of the '822 patent. The analysis provided in this Request and in the declaration of Dr. Baker (Ex. PA-DEC) demonstrates the invalidity of claims 1, 2, and 5-10 in view of prior art that was not substantively considered by the Patent Office. Therefore, it is requested that this request for reexamination be granted and claims 1, 2, and 5-10 be cancelled.

As identified in the attached Certificate of Service and in accordance with 37 C.F.R. §§ 1.33(c) and 1.510(b)(5), a copy of this Request has been served, in its entirety, to the address of the attorney of record.

Respectfully submitted,

PAUL HASTINGS LLP

Dated: September 30, 2022

By: /Naveen Modi/
Naveen Modi
Reg. No. 46,224