UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SOLAREDGE TECHNOLOGIES LTD.,
Petitioner,

v.

KOOLBRIDGE SOLAR, INC.,
Patent Owner.

Patent No. 8,937,822
Filing Date: May 8, 2011
Issue Date: January 20, 2015
Title: SOLAR ENERGY CONVERSION AND UTILIZATION SYSTEM

Inter Partes Review No.: IPR2022-00008

PETITION 2 of 6 FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq*

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Ex. 1212:	Mohan, N., Power Electronics: Converters Applications and Design (2nd Ed. John Wiley & Sons. Inc.) ("Mohan")
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Ex. 1215:	Araújo, S. Highly Efficient Single-Phase Transformerless Inverters for Grid-Connected Photovoltaic Systems, IEEE Trans. on Industrial Elecs, vol. 57, no. 9 (Sept. 2010)
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	Elektrotechnik der Universität Gesamthochschule Kassel (2001, Kassel Univ. Press)
Ex. 1217:	Patel, H., Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I-Harmonic Elimination, IEEE Trans. on Industry Applications, Vol. 1A-9, No. 3 (May/June 1973) ("Patel")
Ex. 1218:	U.S. Patent Application Publication No. 2007/0278988 ("De")
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Ex. 1241:	J. G. Tracy and H. Pfitzer, “Achieving high efficiency in a double conversion transformerless UPS,” 31st Annual Conference of IEEE Industrial Electronics Society, 2005. (“Tracy-IEEE 2005”)
Ex. 1242:	McGraw-Hill Dictionary of Electrical and Electronic Engineering, 1984
Ex. 1243:	Excerpts of IEEE: The Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, IEEE Press 2000
Ex. 1244:	Tolbert et al., Multilevel Converters for Large Electric Drives, IEEE Trans. Ind. Apps., Vol 35, No. 1, Jan/Feb 1999 (“Tolbert”)
Ex. 1245:	Certified translation of Ex. 1255, Heribert Schmidt, Bruno Burger, & Klaus Kiefer. Wechselwirkungen zwischen Solarmodulen und Wechselrichtern, Fraunhofer Institute for Solar Power Systems, June 2007. (“Schmidt”)
Ex. 1246:	Myrzik, J. Topologische Untersuchungen zur Anwendung von tief/-hochsetzenden Stellern für Wechselrichter, Dissertation zur Erlangung des Grades eines Doktor-Ingenieurs (Dr. ing.) im Fachgebiet Elektrotechnik der Universität Gesamthochschule Kassel (2001, Kassel Univ. Press)
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Ex. 1251:	Certified translation of Ex. 1258, PCT Publication No. WO 2010/082265 ("Mori '265")
Ex. 1252:	Keith H. Billings, *Switchmode Power Supply Handbook*, McGraw Hill, 1989
Ex. 1253:	Marty Brown, *Power Supply Cookbook*, Butterworth-Heinemann, 1994
Ex. 1254:	U.S. Department of Commerce. International Trade Administration, *Electric Current Abroad*, 1998 Edition, reprinted Feb. 2002. ("ECA 1998/2002")
Ex. 1255:	Heribert Schmidt, Bruno Burger, & Klaus Kiefer. Wechselwirkungen zwischen Solarmodulen und Wechselrichtern. English translation: Interaction between Solar Modules and DC/AC Inverters, 2007
Ex. 1256:	Math H. Bollen, Irene Gu, *Signal Processing of Power Quality Disturbances*, Wiley-IEEE Press, 2006
Ex. 1257:	Symmetrical components, Wikipedia, https://en.wikipedia.org/wiki/Symmetrical_components, downloaded September 29, 2021
Ex. 1258:	PCT Publication No. WO 2010/082265 ("Mori '265")
Ex. 1259-1263:	Reserved
Ex. 1264:	Ostbayerisches Technologie-Transfer-Institute. V., Power Electronics for Photovoltaics, OTTI International Seminar, June 7-8, 2010
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MANDATORY NOTICES

37 C.F.R. § 42.8(b)(1)&(2): Real Parties in Interest & Related Matters.

The real party-in-interest is Petitioner SolarEdge Technologies Ltd. No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

The '822 Patent has been asserted against SolarEdge in the District of Delaware in *Koolbridge Solar, Inc. v. SolarEdge Technologies, Inc.*, No. 1:20-cv-01374-MN (D. Del.). The earliest date of service on Petitioner was October 12, 2020. The Patent Owner, after having been notified of Petitioner's intent to file IPRs against the '822 Patent, voluntarily dismissed its lawsuit without prejudice.

The references relied upon herein were not cited during prosecution. No arguments presented in this Petition were raised during prosecution of the '822 patent.

37 C.F.R. § 42.8(b)(3)&(4): Lead & Back-Up Counsel, and Service Information. Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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I. INTRODUCTION & RELIEF REQUESTED

U.S. Patent No. 8,937,822 (the "'822 patent") describes various configurations of well-known DC-AC inverters that convert direct current (DC) electrical power such as from a solar panel to alternating current (AC) electrical power using reversing switches arranged as: (1) a single-phase inverter with an H-bridge switch; (2) a single-phase inverter with multiple H-bridge switches in series; and (3) a three-phase inverter with half-bridge switches. Ex. 1202, ¶¶ 92-96. The '822 patent's claims add merely trivial requirements to these embodiments based on intrinsic properties of DC-AC inverters, such as common-mode AC waveforms appearing on the DC input lines, or well-known components like bi-directional DC-DC converters, switching controllers, a ground leak detector, and a common-mode filter. Mori (Japanese Patent Publication No. 2006-238630A), which is an example of a single-phase inverter with multiple H-bridge switches in series, alone and in combination with the additional secondary references in this petition, teaches these additional limitations.[1] Claims 1-13 and 20 of the '822 patent are unpatentable and should be cancelled.

[1] Other concurrently filed petitions use different base references teaching the other (*e.g.*, single-phase) inverter configurations.

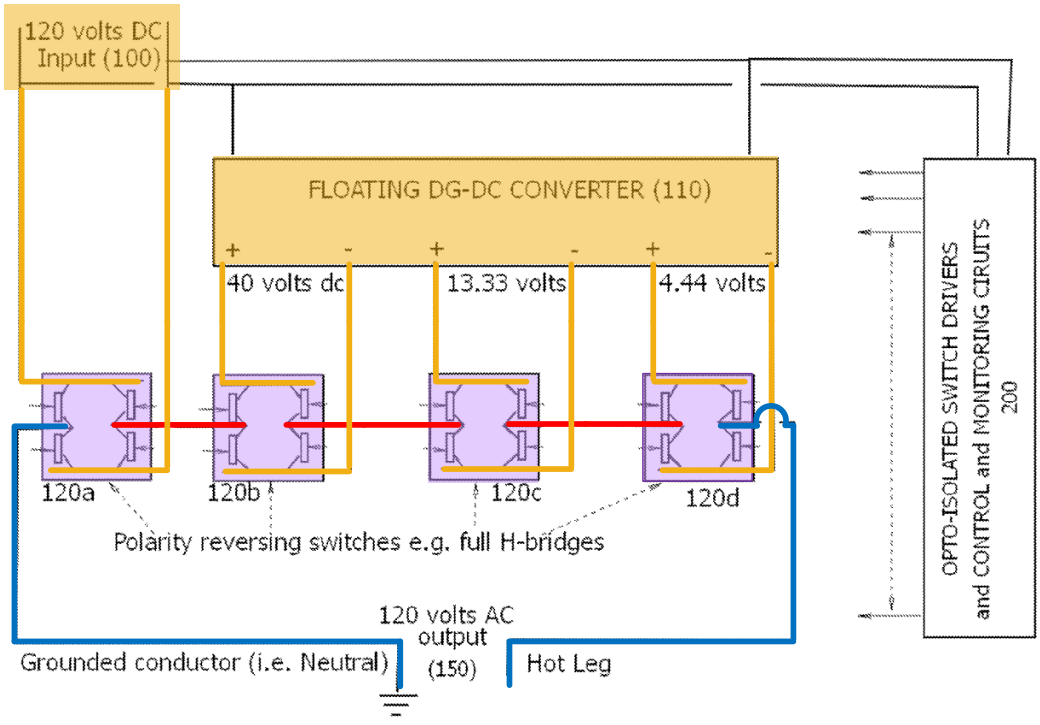
II. GROUNDS FOR STANDING & FEE PAYMENT

Petitioner certifies that the '822 patent is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting *inter partes* review challenging claims 1-13 and 20 on the identified grounds. The undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

III. OVERVIEW

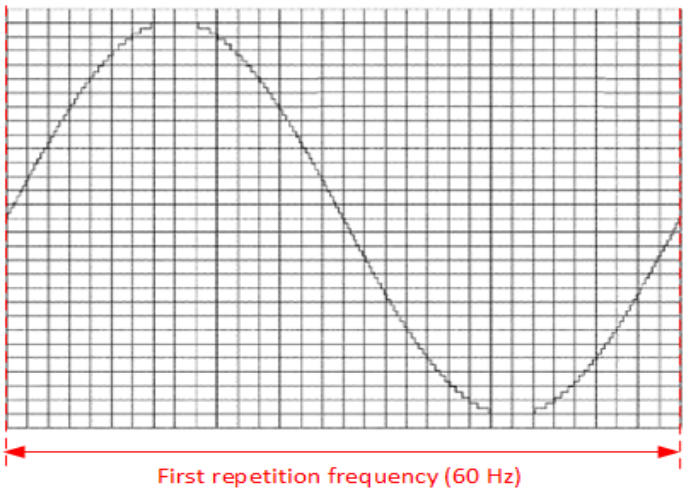
A. Brief Description of Alleged Invention

The '822 patent describes multiple well-known inverters, one of which is a single-phase, inverter using a plurality of H-bridges (**purple**), connected in series (**red**) to convert floating DC power sources (**orange**) to an AC output (**blue**):



Ex. 1201, Fig. 1 (annotated)

Id., Abstract, 3:17-36, 3:45-50, 3:53-57, 6:17-29, 6:49-59, 7:10-16, 7:39-43, 7:49-54; Ex. 1202, ¶¶ 61-65, 71-80. The floating DC-DC converter 110 converts the 120 volts DC input 100 to a plurality of floating DC voltages, each a successive power of 3 (*i.e.*, 40V, 13.33V, 4.44V). *Id.*, 6:46-52. The H-bridges output their voltage input multiplied respectively by four ternary digits (T4, T3, T2, T1), each having a value of +1, 0, or -1, thus producing a sum voltage as follows: 120v×T4+40v×T3+13.33v×T2+4.44v×T1. The ternary digits are controlled to produce a sequence of steps approximating a sinusoidal 60 Hz waveform:

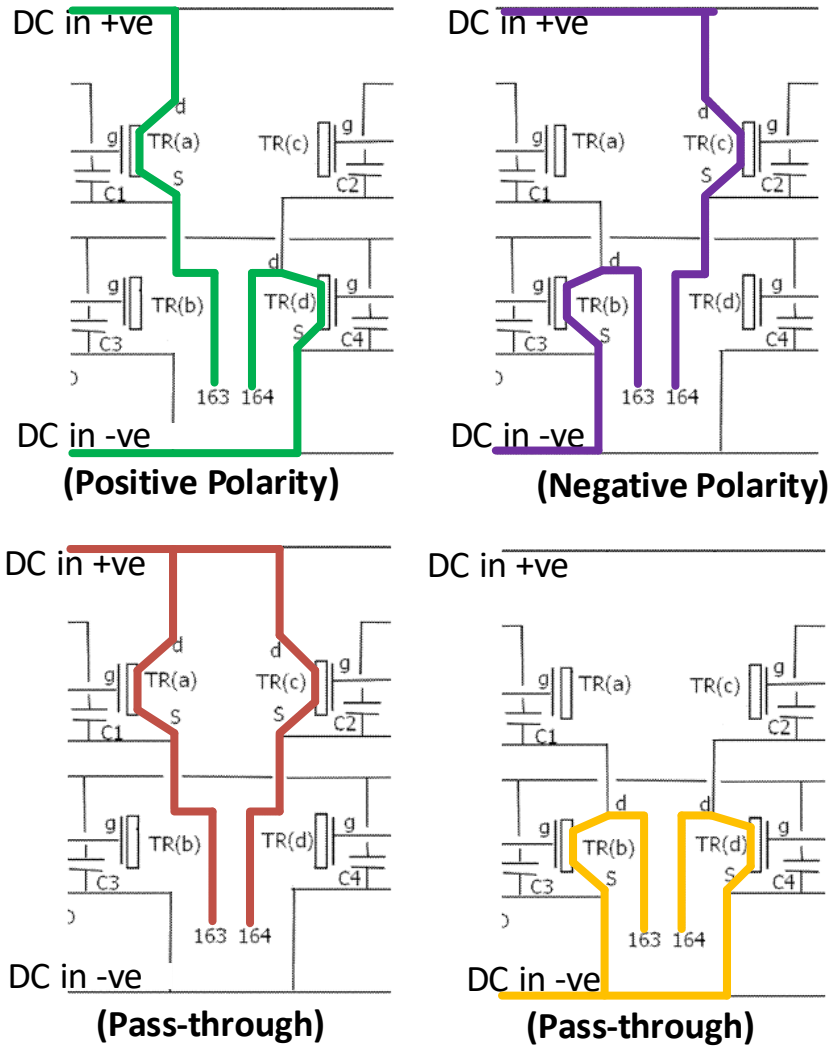


Ex. 1201, Fig. 12 (annotated)

Id., Abstract, 1:18-23, 3:61-4:10, 5:41-57, 7:39-43, 9:41-49, 9:60-64, 10:31-40; Ex. 1202, ¶¶ 67-70.

Each H-bridge switch connects a DC power source directly across the switch output (at terminals 163 and 164) with positive (+1) or negative (-1) polarity, or

bypasses the DC power source with either of two pass-through states (0) as shown below:



Ex. 1201, Fig. 3 (annotated)

Id., 1:36-39, 6:42-57, 7:7-16, 7:49-8:3, 9:41-10:5, 10:15-18, 10:35-40, 11:9-16, 11:32-37; Ex. 1202, ¶ 66. The direct connection made by H-bridge 120a, with alternating polarity, to the AC output terminal causes a 60Hz common-mode voltage

square wave superimposed at "[e]ach DC input terminal" of the 120V DC supply. Ex. 1201, 4:46-50, 10:35-40, 10:55-57, 27:10-11.

B. Prosecution History

The application that led to the '822 patent was filed May 8, 2011. Ex. 1222, p. 128. Claims 1 and 6 were rejected as obvious over U.S. Patent Nos. 7,082,040 (Raddi) and 4,320,449 (Carroll). *Id.* at 303-308. In response, the applicant amended claim 1 to recite "wherein the second repetition frequency is a multiple equal to the same said number N of said first repetition frequency," purportedly incorporating then-allowable claim 3 "to overcome the examiner's rejection of claim 1." *Id.*, p. 318-319. The applicant distinguished the amendment from claim 3: "Rather than specify N to be 1, 2 or 3[,] I have left it equal to the number of unique phases recited in claim 1." *Id.* The examiner allowed the claims based on the prior art allegedly lacking the feature "wherein the second repetition frequency is multiple equal to the same said number N of said first repetition frequency." *Id.*, p. 357-361. None of the prior art cited herein was cited during prosecution, and none is cumulative to the prior art relied upon by the examiner. Mori, the primary reference relied on herein, discloses an inverter with a floating DC supply voltage, which is fundamentally different from Raddi's AC-AC converter with an uninterrupted neutral from input to output that prevents the supply from floating, and fundamentally different from Carroll's cycloconverter connected to the outputs of an inverter for conditioning the

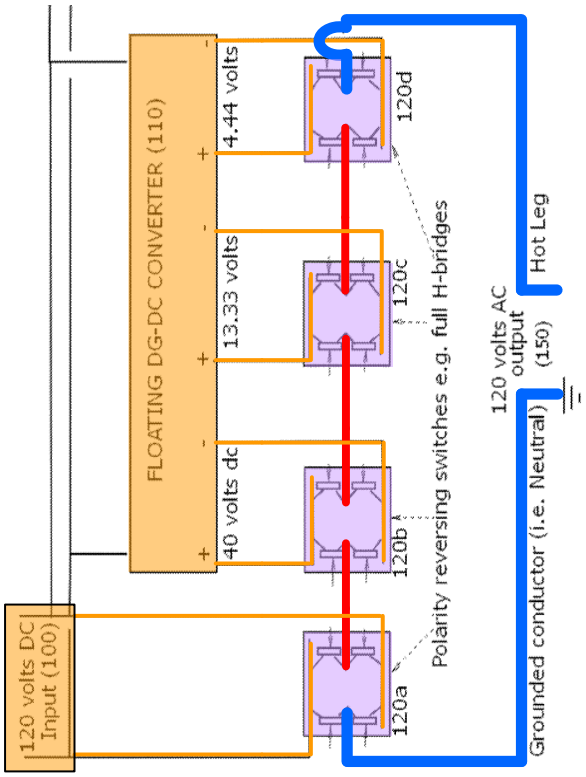
outputs for reactive loads. Ex. 1202, ¶¶ 81-91; Ex. 1201, cover; Ex. 1247, Abstract; Ex. 1248, 1:19-34, Fig. 1.

C. Scope and Content of the Prior Art

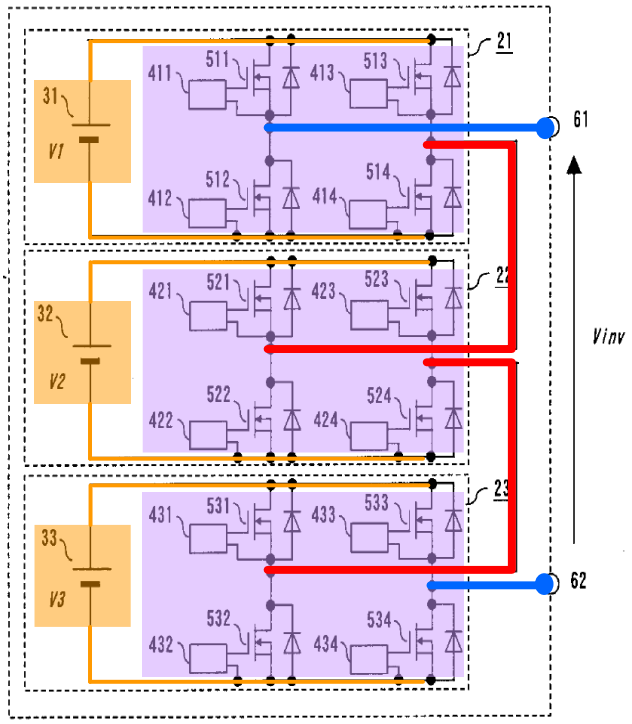
1. Japanese Patent Publication No. 2006-238630A ("Mori") (Ex. 1220, certified translation Ex. 1204)

Mori is a Japanese Patent Publication that published on September 7, 2006, making it prior art under 35 U.S.C. § 102(b).[2] Ex. 1202, ¶ 203. As shown in the side-by-side figures below, Mori (right-side) discloses a near identical inverter to that of the '822 patent (left-side), including multiple H-bridges (21, 22, 23) (**purple**) respectively receiving multiple floating DC voltage sources (V1, V2, V3) (**orange**), each a successive power of 3 (1V, 3V, 9V), with the H-bridge outputs connected in series (**red**) to generate an AC output (Vinv) (**blue**) at a first repetition frequency. Ex. 1204, ¶¶ [0002]-[0012], [0015]-[0016], [0019]-[0021], [0034]; Ex. 1202, ¶¶ 204-206; *compare* Ex. 1204, ¶¶ [0009]-[0012], Fig. 1 *with* Ex. 1201, 6:16-9:40, Fig. 1. The switching structures differ only in the number of voltage sources/H-bridges (four in the '822 patent's Figure 1, and three in Mori's Figure 1). Ex. 1204, ¶ [0011]; Ex. 1201, 6:25-26.

[2] Citations to 35 U.S.C. §§ 102 and 103 refer to the pre-AIA versions.



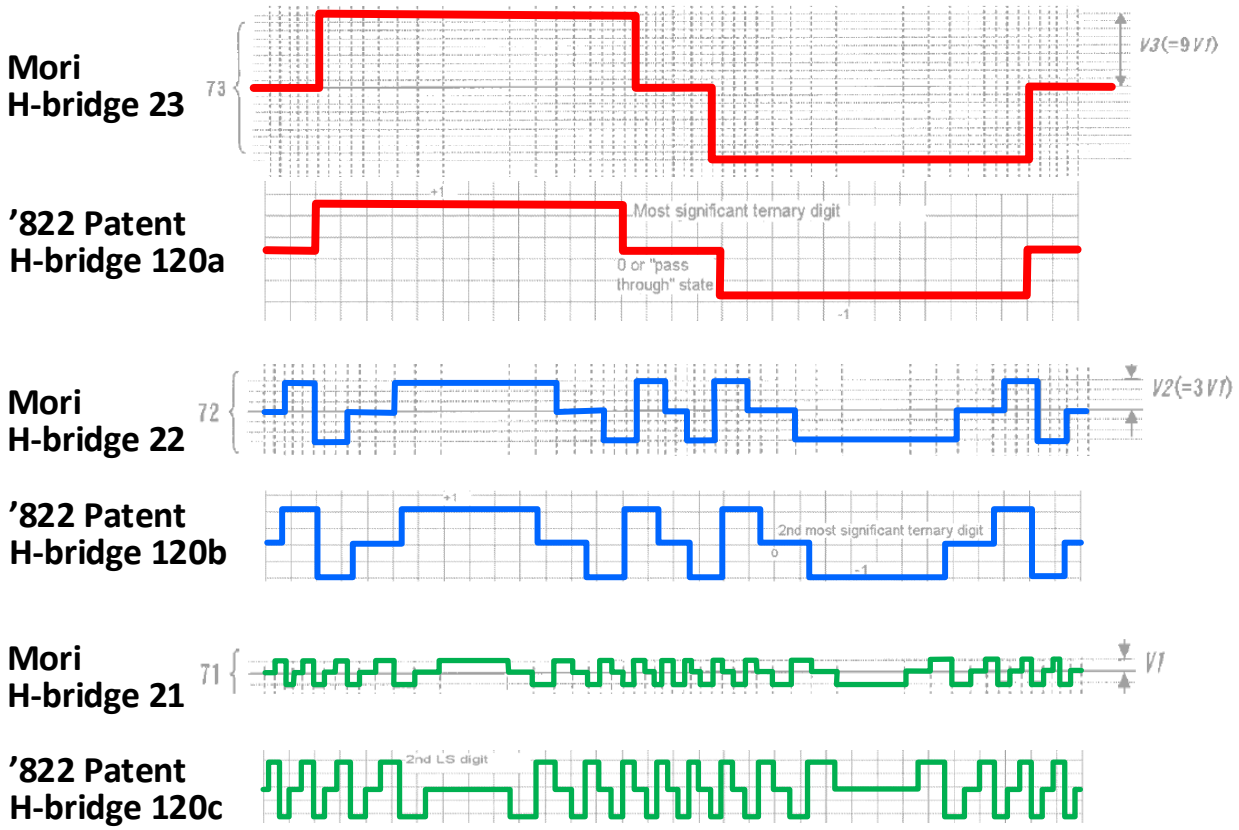
Ex. 1201, Fig. 1 (annotated)



Ex. 1204, Fig. 1 (annotated)

The switch timing of the two inverters is also the same, as shown in the annotated figures below, which juxtaposes the state switching (+1, 0, -1) of H-bridge 23, 22, and 21 from Figure 2 of Mori with that of H-bridges 120a, 120b, 120c of Figure 4 of the '822 patent, respectively. Ex. 1204, ¶¶ [0009]-[0012], Fig. 2; Ex. 1201, 9:51-11:45, Fig. 4; Ex. 1202, ¶¶ 207-209. As the '822 patent acknowledges, the switch timing of H-bridge 120a (illustrated below in **red**) causes a 60Hz common-mode voltage square wave superimposed on the terminals of the 120V DC supply. Ex. 1201, Abstract, 4:46-52, 10:35-57, 10:65-11:6, 35:54-58. Having an identical structure and timing to H-bridge 120a, Mori's H-bridge 23 necessarily

generates the same common-mode voltage on terminals of DC supply 33 (which outputs V3):

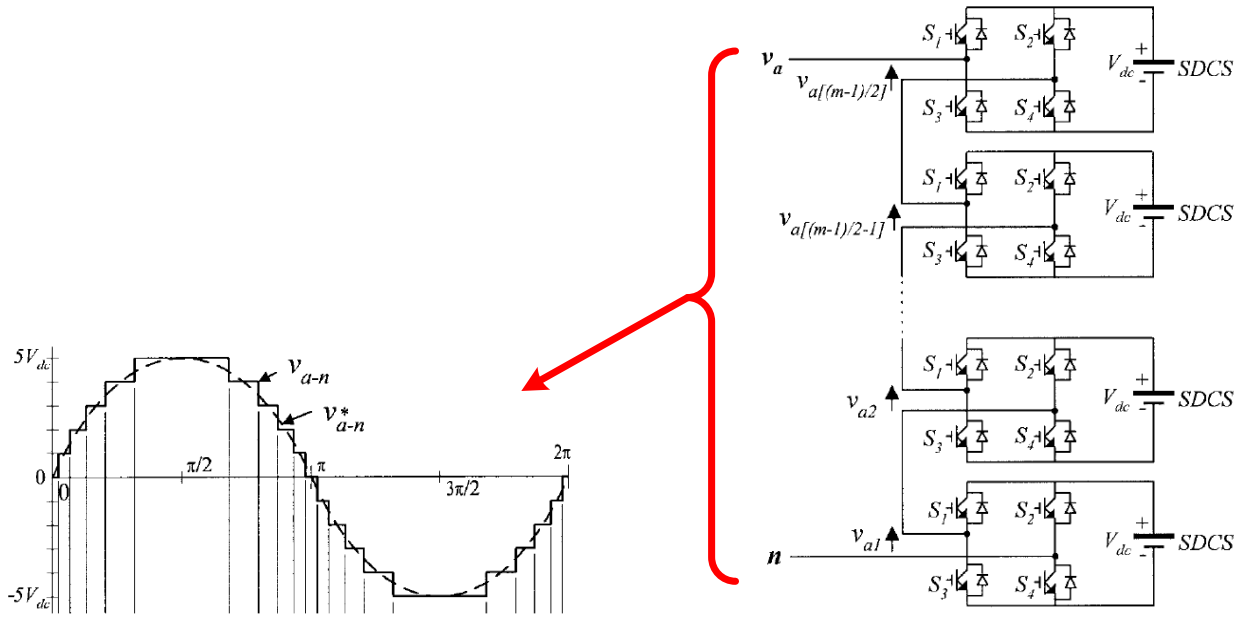


Ex. 1204, Fig. 2 (cropped, annotated); Ex. 1201, Fig. 4 (cropped, annotated)

Id., ¶¶ [0002], [0004], [0009]-[0012]; Ex. 1202, ¶¶ 208-212.

2. Tolbert, Multilevel Converters for Large Electric Drives, IEEE Trans. Ind. Apps., Vol 35, No. 1, Jan/Feb 1999 ("Tolbert") (Ex. 1244)

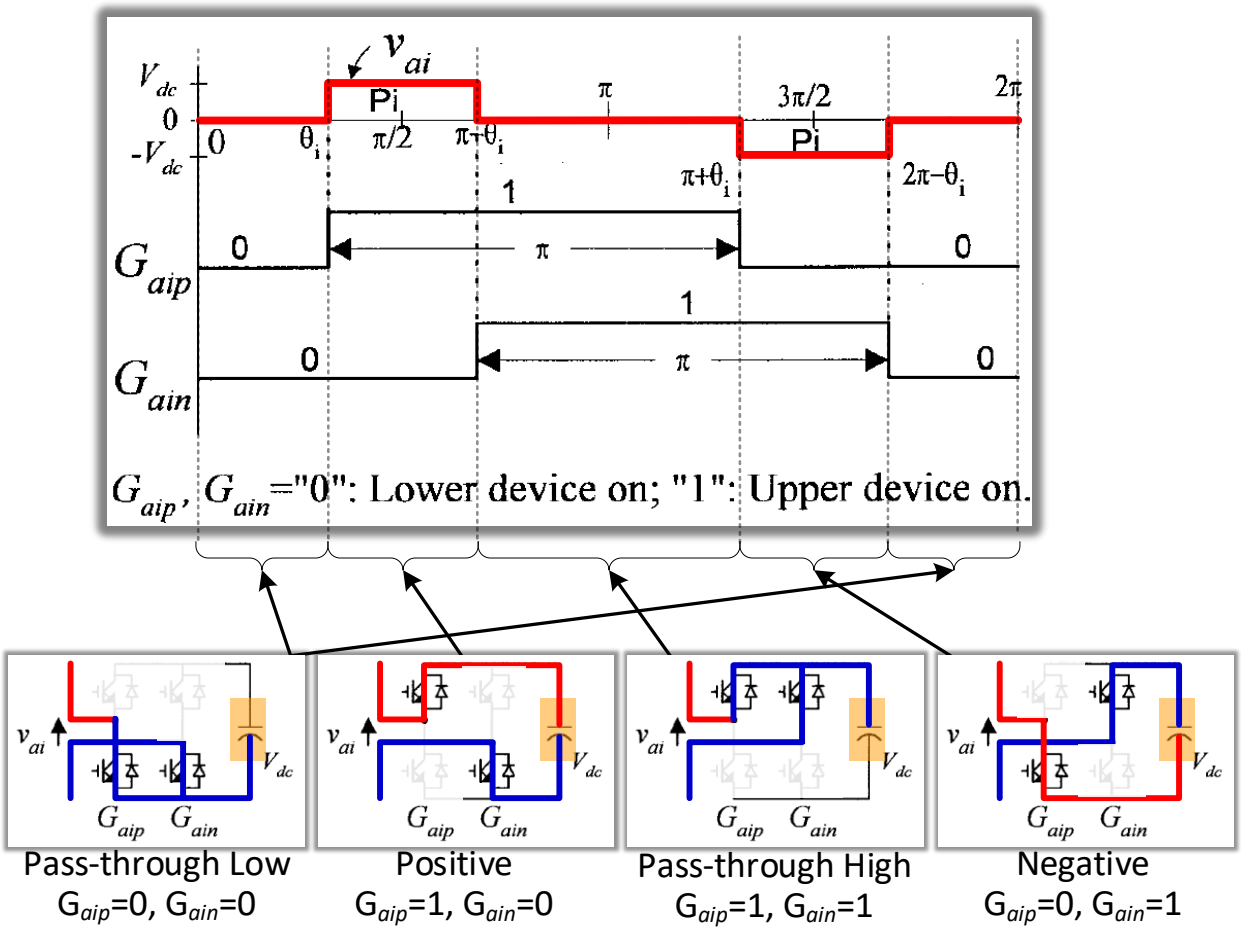
Tolbert was published in 1999, and is prior art under 35 U.S.C. § 102(b). Ex. 1223, ¶¶ 214-231 (Section III.J). Tolbert discloses an inverter having the same basic structure of Mori's inverter in which the outputs of multiple H-bridges are connected in series to generate an AC waveform.



Ex. 1244, Figs. 1, 2a (annotated)

Id., pp. 37-38; Ex. 1202, ¶¶ 213-215.

Each of Tolbert's H-bridges is controlled to output +V, 0, and –V (the same as Mori's H-bridge switch 33) according to 2 bits—G_{aip}, which controls transistors S1, S3 (on the left) in opposite states, and $G_{ain,}$ which controls transistors S2, S4 (on the right) in opposite states. Ex. 1202, ¶ 216; Ex. 1244, 37-38, Figs. 1, 2a. For each side of the H-bridge, a bit value of 1 turns on the top transistor and turns off the bottom transistor, and a bit value of 0 turns off the top transistor and turns on the bottom transistor. Ex. 1202, ¶ 216; Ex. 1244, Fig. 2b. These bits control the H-bridge sequentially into the pass-through low state, the positive state, the pass-through high state, and the negative state:

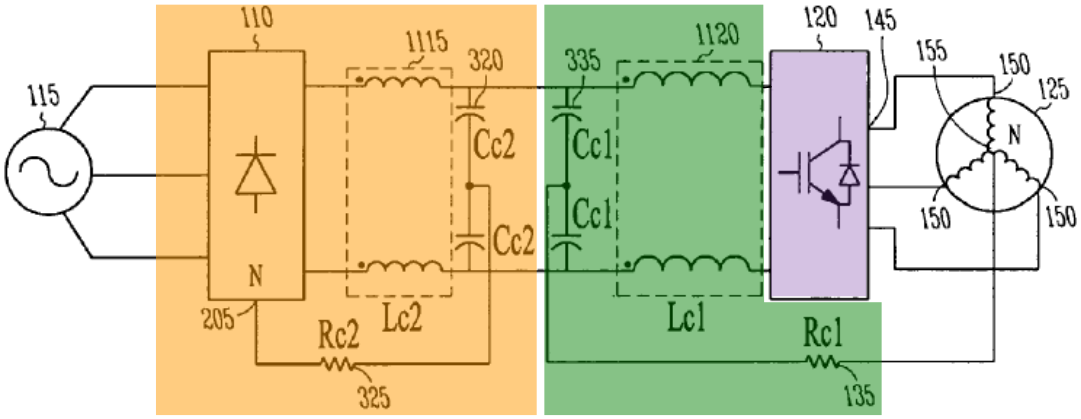


Ex. 1244, Fig. 2(b) (annotated)

Id., pp. 37-38; Ex. 1202, ¶ 216. These are identical to the H-bridge states in the '822 patent. *See* Section III.A, *supra*; Ex. 1202, ¶ 217.

3. U.S. Pat. App. Pub. No. 2007/0278988 ("De") (Ex. 1218)

De was published on December 6, 2007, making it prior art under 35 U.S.C. § 102(b). De discloses a common-mode filter (**green**), including a common-mode inductor 1120 and capacitors 335, connected between DC input terminals of inverter 1 (**purple**) and output terminals of a rectifier DC power source (**orange**):

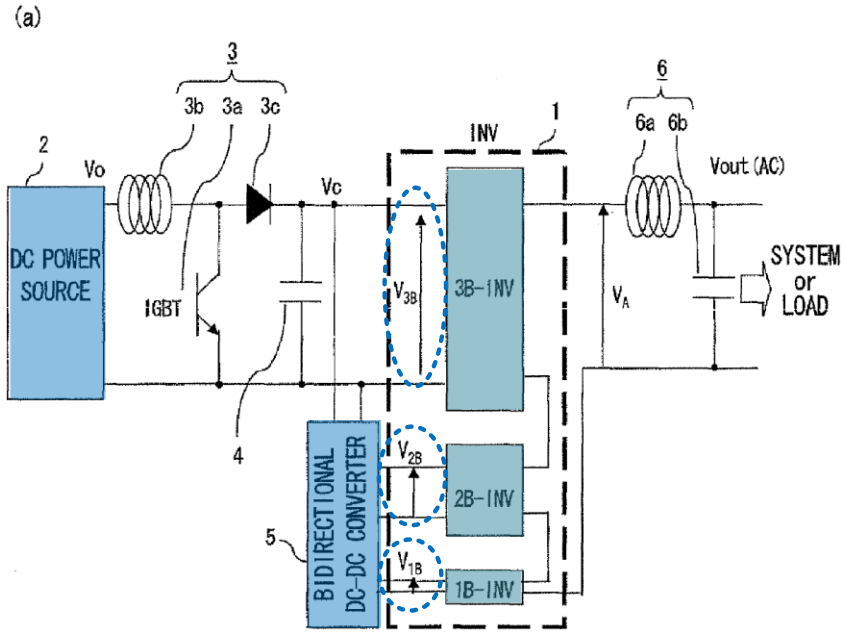


Ex. 1218, Fig. 12 (annotated)

Id., ¶¶ [0020], [0033]-[0034], [0037]-[0038]; Ex. 1202, ¶¶ 194-197.

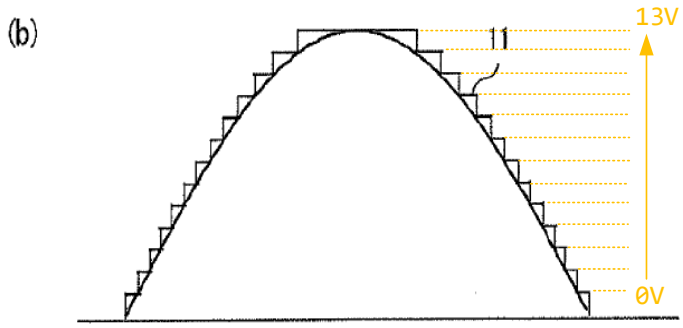
4. U.S. Patent Application Publication No. 2008/0192519 ("Iwata") (Ex. 1207)

Iwata was published on August 14, 2008, making it prior art under 35 U.S.C. § 102(b). Iwata discloses a DC-AC converter with multiple H-bridge inverters (3B-INV, 2B-INV, and 1B-INV) that are connected in series:



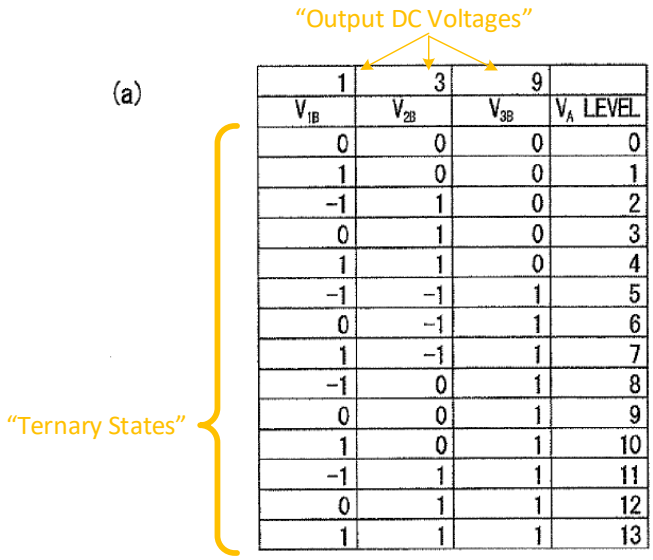
Ex. 1207, Fig. 1a (annotated)

Id., ¶¶ [0003], [0007]-[0009], [0045], Fig. 1b; Ex. 1202, ¶ 185. A bidirectional DC-to-DC converter 5 converts input voltage V_{3B} from a DC power source 2 to floating voltage supplies V_{1B} and V_{2B} with voltages at successive powers of 3 as inputs. Ex. 1207, ¶¶ [0045], [0049]-[0050] ("[T]he relation between V_{1B}, $V_{2B,}$ and V_{3B} is 1:3:9."), Fig. 1a. Iwata's DC-AC converter generates a "substantially sine wave-like output Voltage waveform 11" as shown in annotated Figure 2(b):



Ex. 1207, Fig. 2(b) (annotated)

Id., ¶ [0050]; Ex. 1202, ¶ 186. The values of that output waveform are expressed with a ternary number system having digits for V_{1B}, V_{2B}, and V_{3B}.



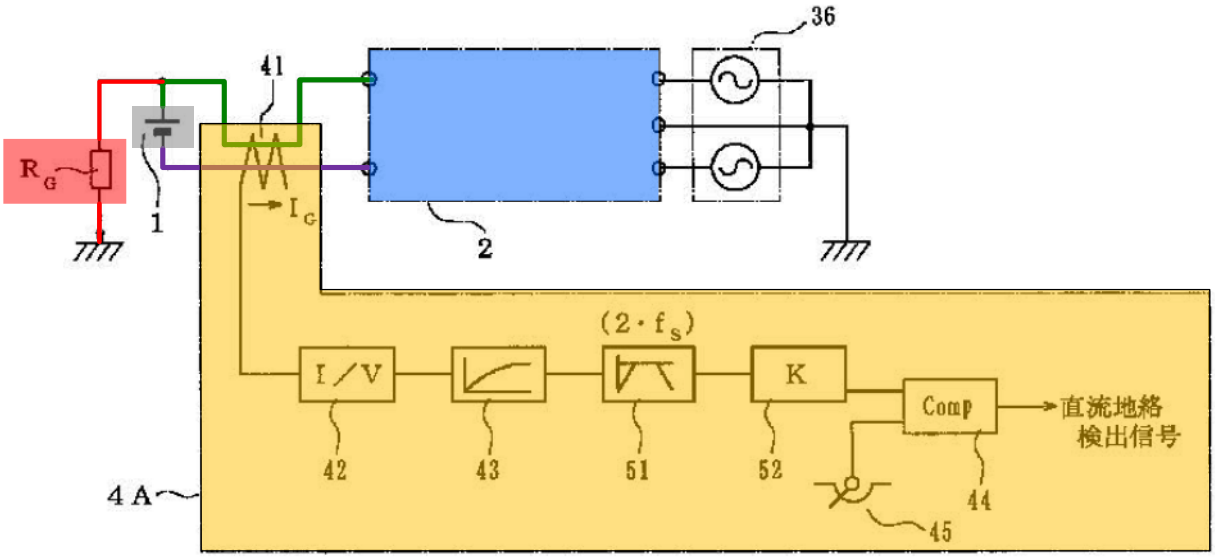
1	3	9	
V_{1B}	V_{2B}	V_{3B}	V_A LEVEL
0	0	0	0
1	0	0	1
-1	1	0	2
0	1	0	3
1	1	0	4
-1	-1	1	5
0	-1	1	6
1	-1	1	7
-1	0	1	8
0	0	1	9
1	0	1	10
-1	1	1	11
0	1	1	12
1	1	1	13

Ex. 1207, Fig. 2(a) (annotated)

Id., ¶ [0050]; Ex. 1202, ¶ 187. For a desired V_A output, each digit determines whether a respective H-bridge is controlled to one of three states: (a) a positive polarity state (+1), (b) an inverse polarity state (-1), and (c) a pass-through state (0). Ex. 1207, ¶ [0050]; Ex. 1202, ¶ 188.

5. Japanese Pat. App. Pub. No. JP 11-122819 ("Fujimoto") (Ex. 1233, certified translation Ex. 1234)

Fujimoto is a Japanese patent publication published on April 30, 1999, making it prior art under 35 U.S.C. § 102(b). Fujimoto describes a DC ground fault detector (**orange**) that includes current transformer 41 inserted in the positive (**green**) and negative (**purple**) conductors between Fujimoto's DC power supply 1 (**grey**) and inverter 2 (**blue**):

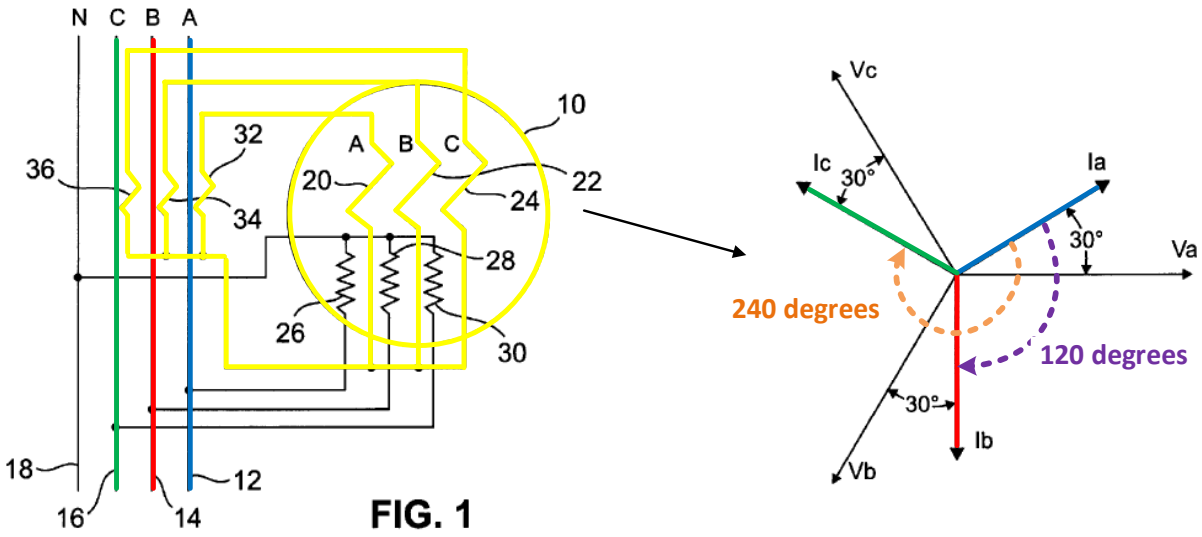


Ex. 1234, Fig. 1 (annotated)

Id., Fig. 3, ¶¶ [0005], [0008], [0010]; Ex. 1202, ¶¶ 190-193. In the event of a ground fault R_G (**red**), a "common current" I_G is induced with an AC component (I_{ac}), at twice the frequency of the AC output waveform of the inverter, which is detected by the DC ground fault detector. Ex. 1234, ¶¶ [0005]-[0007], [0010]-[0011]; Ex. 1202, ¶ 193.

6. U.S. Patent No. 6,112,158 ("Bond") (Ex. 1235)

Bond issued on August 29, 2000, making it prior art under 35 U.S.C. § 102(b). Bond discloses a watt-hour metering device 10 (**yellow**) with a utility120V/208V four wire wye service type connection with neutral at the center of the wye, and with power lines 12 (**blue**), 14 (**red**), and 16 (**green**) delivering current Ia (**blue**), Ib (**red**), and Ic (**green**) at unique phases spaced relatively 0, 120 and 240 degrees apart:

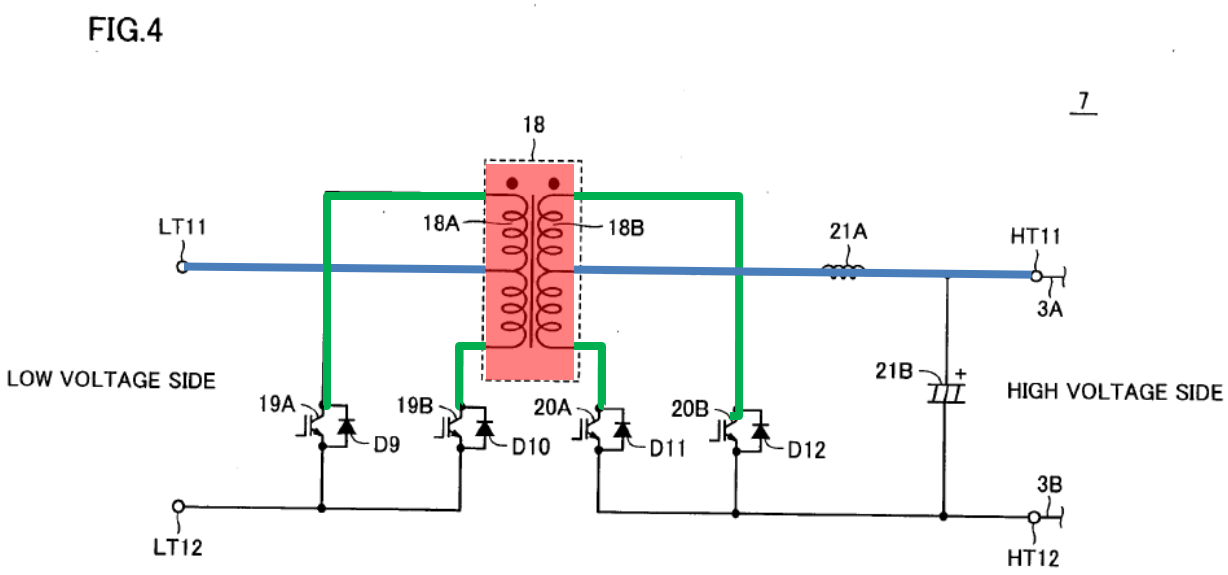


Ex. 1235, Figs. 1, 1a (annotated)

Id., 1:10-22, 1:26-49, 2:55-58, 3:16-23, 3:41-49, 4:4-11, 4:27-58 (table 2), 10:9-11; Ex. 1202, ¶¶ 198-202.

7. U.S. Patent Application Publication No. 2009/0086520 ("Nishimura") (Ex. 1208)

Nishimura was published on April 2, 2009, making it prior art under 35 U.S.C. § 102(b). Nishimura teaches the structure for the bidirectional DC-DC converter in Figure 2 of the '822 patent. Ex. 1208, ¶¶ [0091]-[0101], Fig. 4; Ex. 1201, 18:34-47, Fig. 2. Nishimura's bidirectional DC-DC converter includes center-tapped windings (**red**) that are connected to the positive terminal of the DC input or output (**blue**) with ends of the windings connected to the drains of N-Type MOSFET pairs (**green**):



Ex. 1208, Fig. 4 (annotated)

Id., ¶¶ [0091]-[0101]; Ex. 1202, ¶ 189.

IV. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

Petitioner requests review of claims 1–13 and 20 on the following grounds and references.

Grounds	References	Basis	Claims Challenged
1	Mori	102	1-3, 8-10, 12
2	Mori	103	1-3, 8-10, 12
3	Mori in view of Tolbert	103	1-3, 8-10, 12
4, 5	Mori/Mori-Tolbert in view of De	103	6, 20
6, 7	Mori/Mori-Tolbert in view of Fujimoto	103	4, 11
8, 9	Mori/Mori-Tolbert in view Bond	103	7

10, 11	Mori/Mori-Tolbert in view of Iwata and Nishimura	103	5, 13

The challenged claims are unpatentable based on these grounds as demonstrated by a preponderance of the evidence, including Dr. Baker's expert testimony (*e.g.*, Ex. 1202, ¶¶ 1-60, 132-184, 218-219, 392-395), and Dr. Mullins' expert testimony proving authenticity and public availability prior to May 8, 2011 of certain exhibits. Ex. 1223, ¶¶ 1-40, 41-65 (Ex. 1210), 66-79 (Ex. 1212), 232-248 (Ex. 1215), 268-285 (Ex. 1217), 80-93 (Ex. 1219), 130-154 (Ex. 1241), 214-231 (Ex. 1244), 249-267 (Ex. 1246), 332-353 (Ex. 1252), 193-213 (Ex. 1253), 172-192 (Ex. 1254), 155-171 (Ex. 1255), 308-331 (Ex. 1256), 94-111 (Ex. 1264), 112-129 (Ex. 1265), 354-356.

A. Level of Ordinary Skill

At the time of the alleged invention of the '822 patent, a person having ordinary skill in the art ("PHOSITA") would have had a bachelor's degree in electrical engineering or a similar discipline and three years of design experience with power electronics, including experience designing power converters. Ex. 1202, ¶¶ 20-23.

B. Claim Construction

The following terms could be construed as means-plus-function limitations. 37 C.F.R. § 42.104(b)(3). If the Board does not construe these as means-plus-

function limitations, they should be construed, along with all other claim terms, according to their ordinary and customary meaning, consistent with the prosecution history, to a PHOSITA at the time of the alleged invention. 37 C.F.R. § 42.100(b). Whether or not these are means-plus-function terms, the prior art discloses these limitations as addressed below. Ex. 1202, ¶¶ 97-99.

1. "DC to AC converter" (Claim 1)

To the extent "DC to AC converter" is found to be a means-plus-function term, it performs the function of "caus[ing] (1) an AC output waveform at said first repetition frequency and having a voltage relative to one of said at least one ground, neutral or reference potential terminals to appear with a unique phase at each of a number N at least equal to one of said set of live AC output terminals, and (2) a common-mode voltage waveform at a second repetition frequency to appear relative to one of said at least one ground, neutral or reference potential terminals and in the same phase on both of said positive and negative terminals of said DC power source, wherein the second repetition frequency is a multiple equal to the same said number N of said first repetition frequency." Ex. 1201, claim 1; Ex. 1202, ¶ 100.

The corresponding structures include four different inverter circuits. One inverter circuit, depicted in Figures 1 and 10, includes a plurality of H-bridges with series connected outputs and with inputs of each H-bridge connected to a different voltage source. Ex. 1201, 6:17-26, Figs. 1, 10; Ex. 1202, ¶¶ 101-105.

Another corresponding structure, in Figure 16, includes three half-bridge switches with inputs connected across a pair of DC input terminals, and each outputting a voltage phase through a respective inductor. Ex. 1201, Fig. 16; Ex. 1202, ¶ 107.

Two other structures are illustrated in Figures 15 and 24. Ex. 1202, ¶¶ 106, 108-109. The Figure 15 structure includes a single H-bridge with a single-phase output connected through an inductor. Ex. 1201, 23:27-44, Fig. 15. The Figure 24 structure is the same as in Figure 16, but with three additional H-bridges, each connected to a different one of the voltage phase outputs. Ex. 1201, 29:25-67, Fig. 24.

2. "A switch[ing] controller" (Claims 2 and 5)

To the extent "switch[ing] controller" in claims 2 and 5 is construed to be a means-plus function term, the claim 2 function is:

> [controlling a] first electronic switch . . . to connect said positive DC input terminal to the instantaneously most positive of said set of AC output terminals and said at least one ground, neutral or reference potential terminal alternating with connecting said negative DC input terminal to the instantaneously most negative of said set of AC output terminals and said at least one ground, neutral or reference potential terminal,

and the claim 5 function is:

for controlling the three-state electronic switches according to a sampled numerical representation of the desired AC output waveform expressed in a ternary number base.

Ex. 1201, claims 2, 5; Ex. 1202, ¶ 120.

The corresponding structures for both switch controllers include (1) "a microcontroller" with "memory"; or (2) "a crystal reference oscillator," "15-bit divider," and Read Only Memory (ROM) containing precomputed waveforms. Ex. 1201, 12:26-51, 24:8-12; Ex. 1202, ¶¶ 120-125.

3. "AC ground leak detector" (Claim 4)

To the extent "AC ground leak detector . . ." is construed to be a means-plus-function term, it performs the function of "detect[ing] an imbalance current at said second frequency and [] thereby provid[ing] a detection signal indicative of an unwanted leakage impedance from a DC conductor to ground." Ex. 1201, claim 4; Ex. 1202, ¶ 110. The corresponding structure is a current transformer including toroid 800 with a toroidal winding 801. Ex. 1201, 25:57-59, 31:65-32:20, 35:66-36:3, 41:21-22, Fig. 18; Ex. 1202, ¶¶ 110-114.

4. "bidirectional DC-to-DC converter" (Claims 5, 13)

To the extent "bidirectional DC-to-DC converter" in claims 5 and 13 is construed to be a means-plus function term, the claim 5 function is:

> converting the input voltage from said DC power source to a number of floating supplies of voltages equal to the input voltage divided or multiplied by successive powers of 3,

and the claim 13 function is:

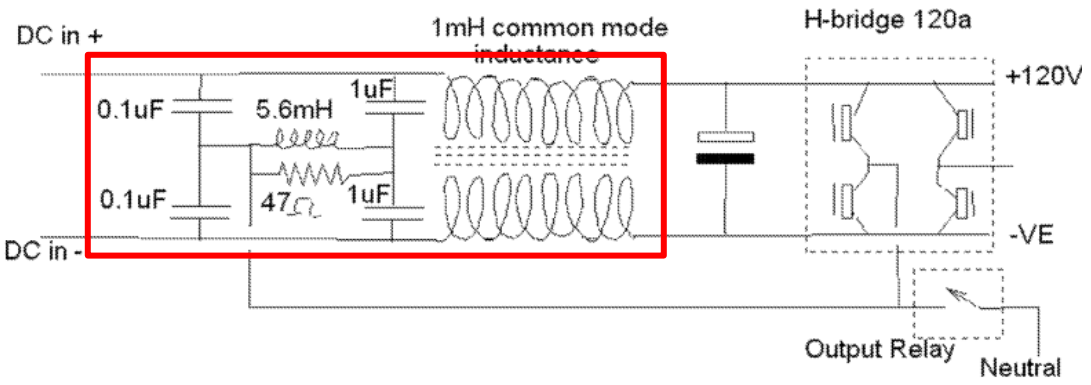
> to form, along with the DC source voltage, a set of floating DC supplies of voltages having voltage ratios of successive powers of 3.
>
> Ex. 1001, cls. 5, 13.

The corresponding structure for both claims is one or more transformers with windings that have turn ratios in proportion to the voltage ratios being output, where each winding corresponding to a floating supply is center tapped (or an equivalent structure). *Id.*, 15:29-34, 18:34-47, 19:5-23, Figs. 2, 10; Ex. 1202, ¶¶ 126-131.

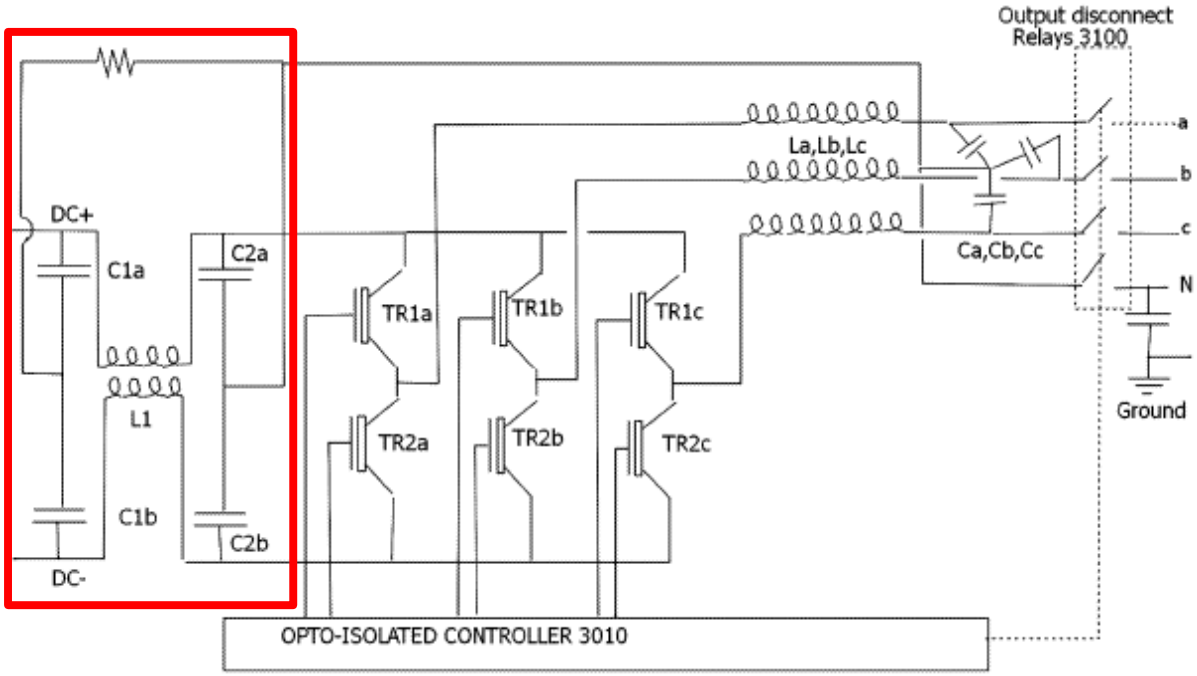
5. "common-mode filter" (Claim 6)

To the extent "common mode filter" is a means-plus-function term, it performs the claimed function of "(1) preventing high frequency components of the DC to AC converter internal waveforms being exported to said DC source and (2) minimizing overshoot of said common-mode waveform in order to minimize peak voltages on said positive and negative terminals." Ex. 1201, claims 6; Ex. 1202, ¶¶ 115-119. The corresponding structure is a filter comprising capacitors, inductors, and resistors arranged as shown in Figures 6 and 16 of the '822 patent:

FIGURE 6: COMMON MODE INPUT HASH FILTER



Ex. 1201, Fig. 6 (annotated)



Ex. 1201, Fig. 16 (annotated)

Id., 18:18-33; Ex. 1202, ¶¶ 117-118.

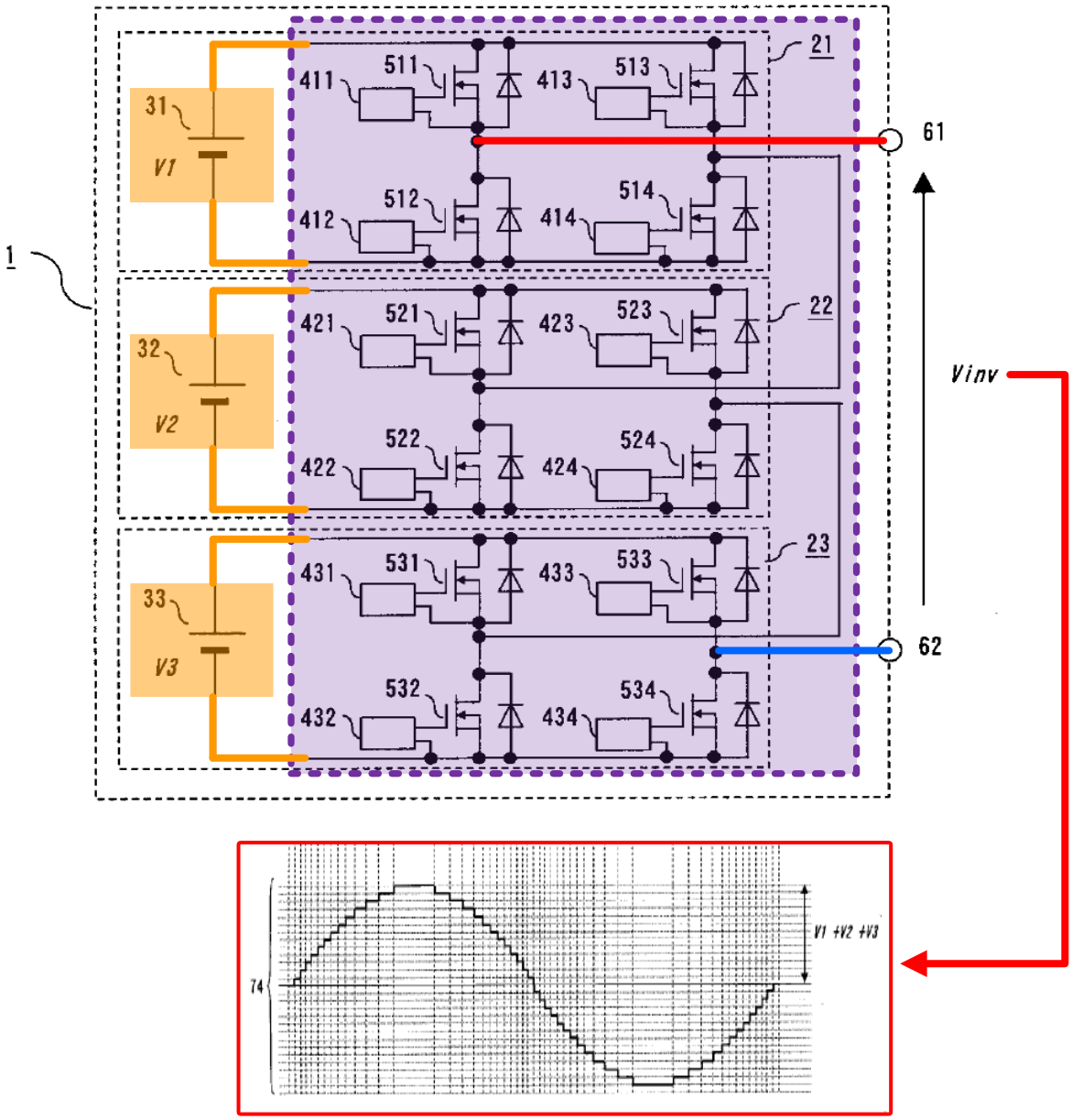
V. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Grounds 1-3: Mori Anticipates, and Mori Alone or in View of Tolbert Renders Obvious, Claims 1-3, 8-10, and 12

1. Independent Claim 1

a. [1A]: "A DC to AC conversion apparatus for converting power from a DC source to produce an power output waveform at a first repetition frequency, comprising"

To the extent the preamble is limiting, Mori discloses it. Ex. 1202, ¶¶ 220-225. As shown in Figures 1 and 2, Mori describes a "multiplex inverter 1" (claimed "DC to AC conversion apparatus") that comprises three single-phase inverters (21-23) (**purple**) that convert power from multiple DC sources (31-33) (**orange**) to produce an AC power output waveform (V_{inv}) at an output terminal (**red**) at a first repetition frequency (depicted in Figure 2):

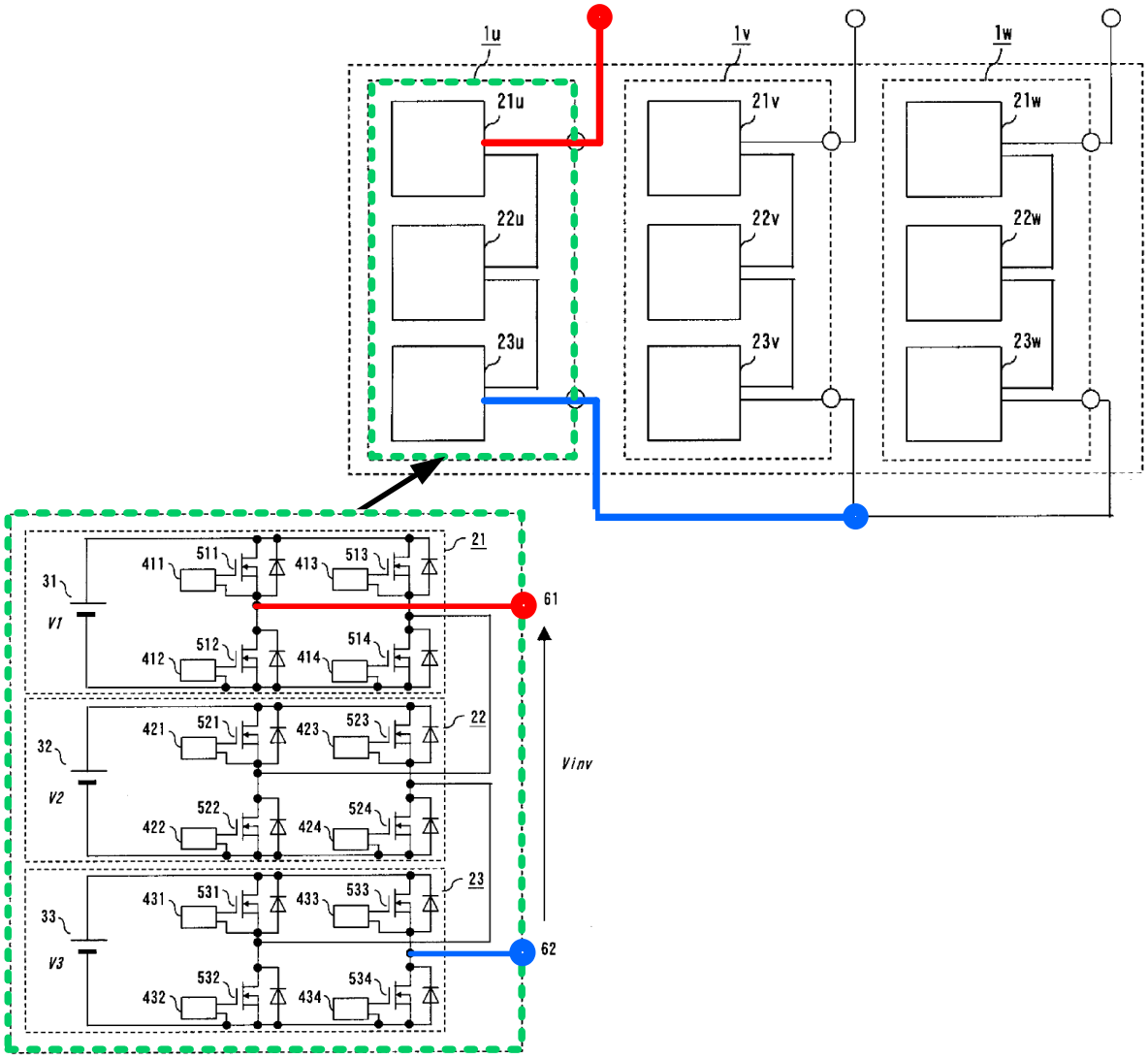


Ex. 1204, Figs. 1 (annotated), 2 (cropped and annotated)

Id., ¶¶ [0007], [0009], [0011]-[0012], [0034], Fig. 16; Ex. 1202, ¶¶ 221-223.

b. [1B-1C]: "a set of at least one live AC output terminals, at least one output terminal designated as a ground, neutral or reference potential terminal"

Mori's single-phase multiplex converter (**green**), either individually or as part of a three-phase device, has the claimed "set" of a live AC output terminal 61 (**red**) and a neutral terminal 62 (**blue**):



Ex. 1204, Figs. 1, 16 (annotated)

Ex. 1204, ¶¶ [0009], [0034]; Ex. 1202, ¶¶ 226-231.

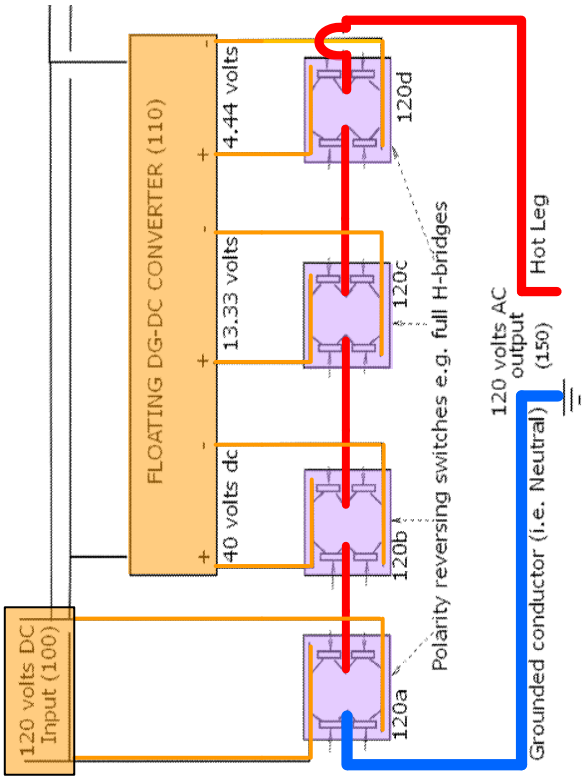
c. [1D]: "a floating DC power source having a positive and a negative terminal connected respectively to the positive and negative DC input terminals of a DC to AC converter"

Mori's inverter (*see* Section V.A.1.a, *supra*) has three DC power sources 31-33 (each a claimed "floating DC power source") each having positive and negative terminals (**orange**) connected respectively to the positive and negative DC input terminals of the DC-to-AC converter (**purple**), which includes three single-phase inverters 21-23 connected in series. Ex. 1204, Figs. 1 (annotated below), 16, ¶¶ [0009], [0034]; Ex. 1202, ¶ 232.

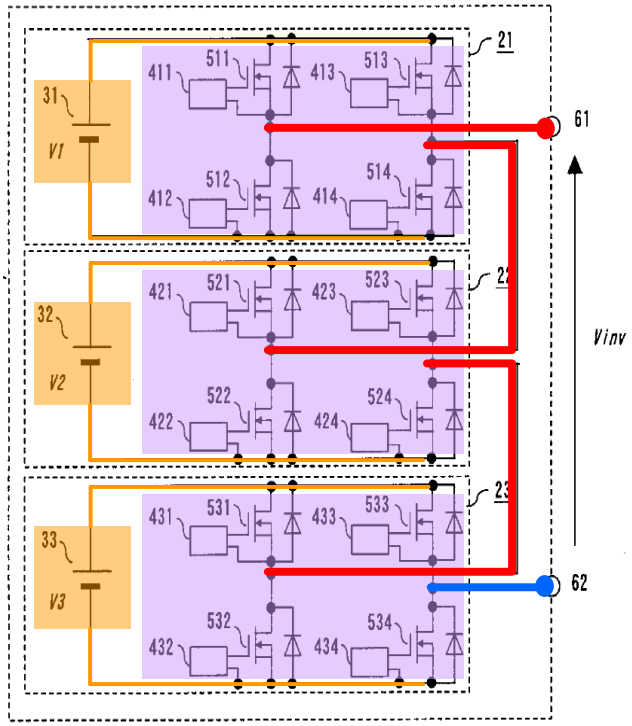
Like the DC power sources in the '822 patent, Mori's DC power sources 31-33 are floating, since their terminals are connected only to the inputs of the DC-to-AC converter at each respective single-phase inverter 21-23 and are not permanently tied to any established potential such as neutral terminal 62. Ex. 1202, ¶ 233; Ex. 1204, ¶ [0002]; Ex. 1201, 6:17-29, 9:51-60, 23:37-42; Ex. 1236, p. 6; Ex. 1242, p. 6.

As shown below, Mori (right-side) discloses a near identical or equivalent DC to AC converter structure to that of the '822 patent (left-side), with multiple H-bridges (Mori's "single phase converter[s]") having outputs connected in series to generate an AC output (V_{inv}) (**red**) with respect to neutral (**blue**). Ex. 1204, ¶¶ [0002]-[0012], [0015]-[0016], [0019]-[0021], [0034]; *compare* Ex. 1204, ¶¶ [0009]-[0012], Fig. 1 *with* Ex. 1201, 6:16-9:40, Fig. 1. The '822 patent discloses that any

multiple of H-bridges may be used, such as three as Mori discloses. Ex. 1204, ¶ [0011]; Ex. 1201, 6:25-26; Ex. 1202, ¶ 234.

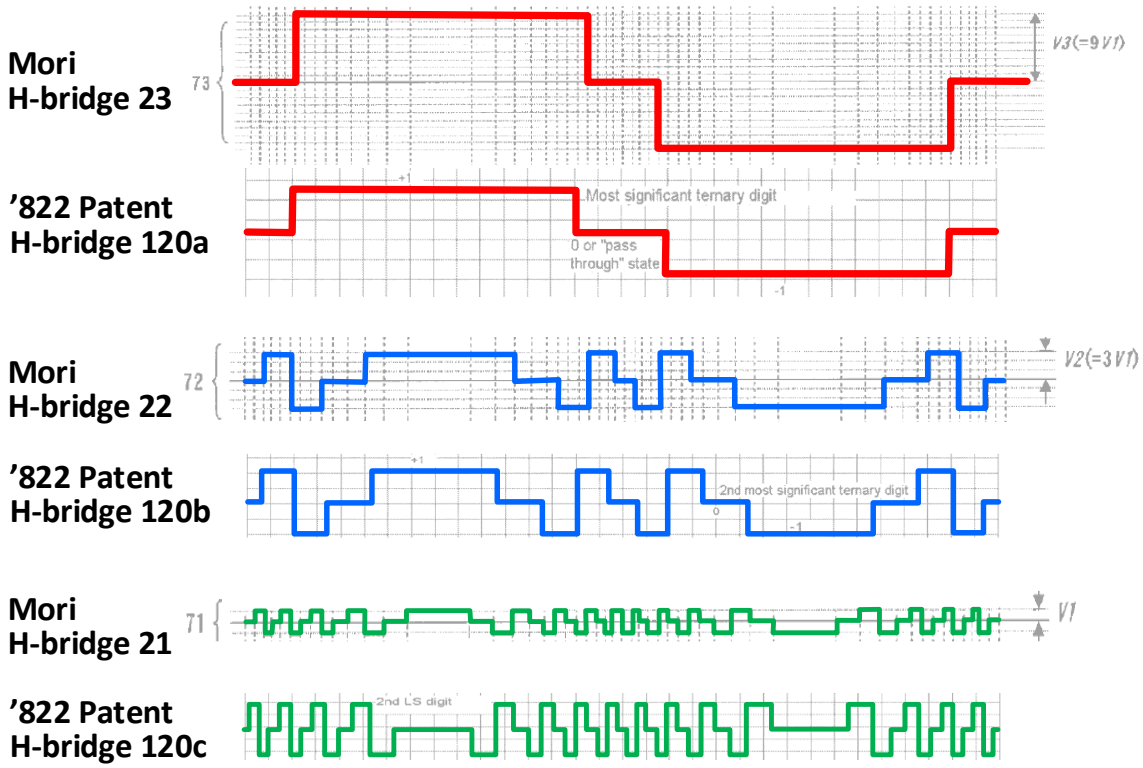


Ex. 1201, Fig. 1 (annotated)



Ex. 1204, Fig. 1 (annotated)

The H-bridge structures in Mori and the ’822 patent are insubstantially different, each including MOSFETs connected together in an identical arrangement. Ex. 1201, 7:51-55, 9:51-59, 12:39-51, 15:36-38; Ex. 1204, Fig. 4, ¶¶ [0009]-[0010], [0015]-[0019]. Moreover, the switch timing of the two inverters is also substantially identical, as shown in the comparative annotated figures below, which juxtaposes the state switching (+1, 0, -1) of H-bridges 23, 22, and 21 from Figure 2 of Mori with that of H-bridges 120a, 120b, 120c of Figure 4 of the ’822 patent, respectively.



Ex. 1204, Fig. 2 (cropped, annotated); Ex. 1201, Fig. 4 (cropped, annotated) Ex. 1204, ¶¶ [0002], [0009]-[0012]; Ex. 1201, 9:51-11:45; Ex. 1202, ¶ 235.

As discussed below (*see* Sections V.A.1.d, V.A.1.e, *infra*), Mori's inverter performs the same function recited with respect to elements [1E] and [1F] (converting power from a floating DC source to AC power with a corresponding common-mode voltage waveform on the DC input) in the same way (using cascaded H-bridges) for the same result (an AC sinewave output and common-mode waveform on the DC inputs). Ex. 1202, ¶ 236.

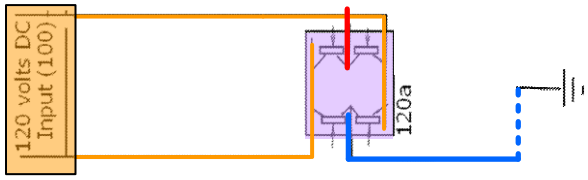
d. [1E]: "wherein the DC to AC converter causes: (1) an AC output waveform at said first repetition frequency and having a voltage relative to one of said at least one ground, neutral or reference potential terminals to appear with a unique phase at each of a number N at least equal to one of said set of live AC output terminals, and"

Mori's multiplex inverter (*see* Section V.A.1.a, *supra*) causes an AC output waveform (depicted as 74 in Figure 2) at a first repetition frequency with a unique phase (N=1) on terminal 61 (**red**) having a voltage V_{inv} relative to neutral 62 (**blue**) (claimed "ground, neutral, or reference potential terminal[]") depicted in Figure 1 (annotated above). Ex. 1202, ¶¶ 237-241; Ex. 1204, Figs. 1-3, ¶¶ [0007], [0009], [0011]-[0013].

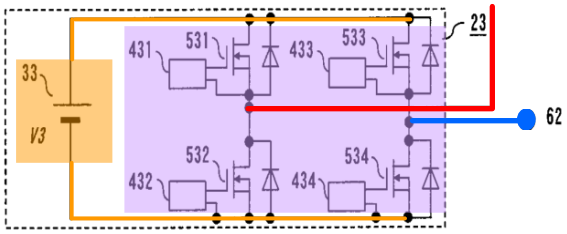
e. [1F]: "[wherein the DC to AC converter causes:] (2) a common-mode voltage waveform at a second repetition frequency to appear relative to one of said at least one ground, neutral or reference potential terminals and in the same phase on both of said positive and negative terminals of said DC power source, wherein the second repetition frequency is a multiple equal to the same said number N of said first repetition frequency."

Mori's circuit and switch timing, which are insubstantially different to that of the '822 patent, causes the identical "common-mode voltage waveform …" of element [1F]. Ex. 1202, ¶¶ 242, 261. As shown below, Mori's H-bridge 23 (**purple**) is connected at its input to DC power supply 33 (**orange**) (claimed "DC power source"), and connected at one of its output terminals to neutral 62 (**blue**) (claimed "ground, neutral, or reference potential terminal[]"), which is the same arrangement

as H-bridge 120a, the 120V DC power source, and the neutral terminal of the ’822 patent:



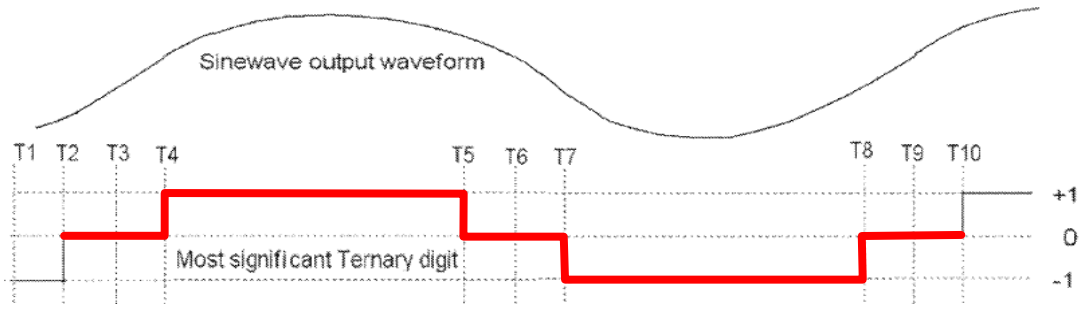
Ex. 1201, Fig. 1 (cropped, annotated)



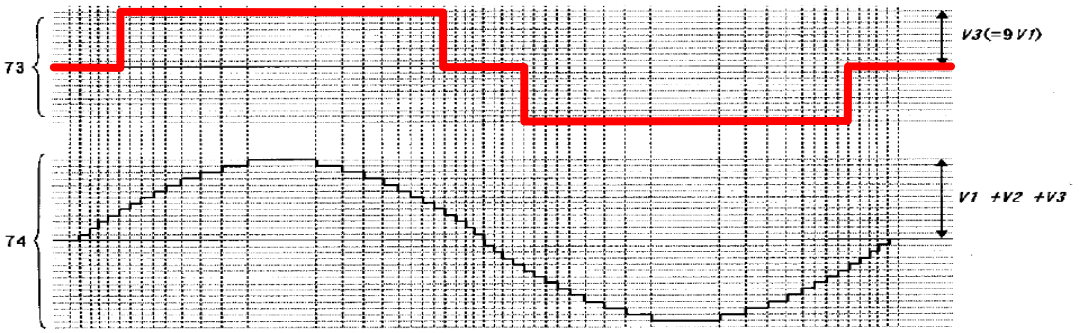
Ex. 1204, Fig. 1 (cropped, annotated)

Ex. 1202, ¶ 242; Ex. 1201, 7:51-55, 9:51-59, 12:39-51, 15:36-38; Ex. 1204, ¶¶ [0009]-[0010], [0015]-[0019].

To generate the AC output waveform (*see* Section V.A.1.d, *supra*), Mori’s H-bridge 23 modulates between three voltages (+V3, 0, -V3) in a cyclical pattern (**red**) at the same frequency as the sinewave output, which is identical to switching of H-bridge 120a of the ’822 patent:



Ex. 1201, Fig. 5 (cropped, annotated)

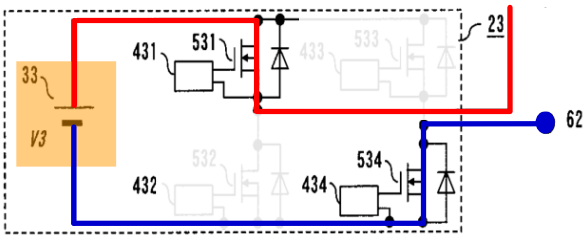


Ex. 1204, Fig. 2 (cropped, annotated)

Ex. 1202, ¶¶ 243-244; Ex. 1204, ¶¶ [0002], [0004], [0009]-[0012]; Ex. 1201, 10:40-57, 10:65-11:9, 18:21-26, 23:54-57. As the '822 patent acknowledges, this switching causes a 60Hz common-mode voltage square wave on the terminals of the 120V DC supply with respect to neutral. Ex. 1201, Abstract, 4:46-52, 10:35-57, 10:65-11:6, 35:54-58; Ex. 1245 at 9-11; Ex. 1264, 51-57, 302-310; Ex. 1265, 51-57, 323-337, 385-398; Ex. 1213, [0016], Figs. 1, 2, 5. Because Mori's H-bridge 23 has the identical structure and timing, it necessarily causes, and would have been understood to cause, the same common-mode voltage on the terminals of DC supply 33 with respect to neutral. Ex. 1204, Fig. 2, ¶¶ [0002], [0004], [0009]-[0012]; Ex. 1202, ¶ 245.

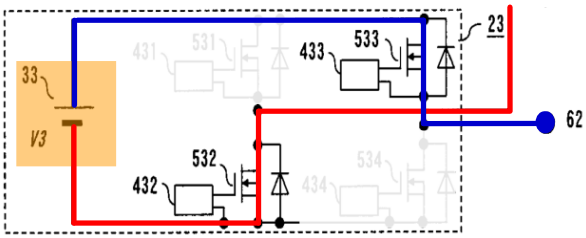
A PHOSITA would have understood that H-bridge 23 generates three output voltages (+V3, 0V, -V3) by connecting the DC supply 33 to the output terminals using the four possible states of the H-bridge that can generate such voltages (as annotated on Figure 1 of Ex. 1204, below):

- Positive State (+3V): transistors 531, 534 are on while transistors 532, 533 are off, connecting DC supply 33 in series between the output terminal (**red**) and neutral 62 (**blue**);



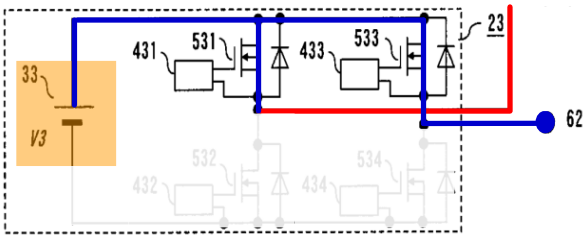
Ex. 1204, Fig. 1 (cropped, annotated)

- Negative State (-3V): transistors 532, 533 are on while transistors 531, 534 are off, connecting the DC supply 33 in series and in reverse polarity between the output terminal (**red**) and neutral 62 (**blue**);



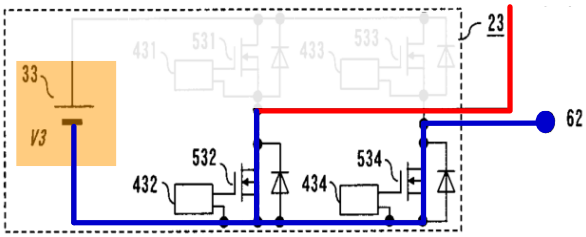
Id., Fig. 1 (cropped, annotated)

- Pass-through High State (0V): transistors 531, 533 are on while transistors 532, 534 are off, connecting the output terminal (**red**) directly to neutral 62 (**blue**); and



Id., Fig. 1 (cropped, annotated)

- Pass-through Low State (0V): transistors 532, 534 are on while transistors 531, 533 are off, connecting the output terminal (**red**) directly to neutral 62 (**blue**).

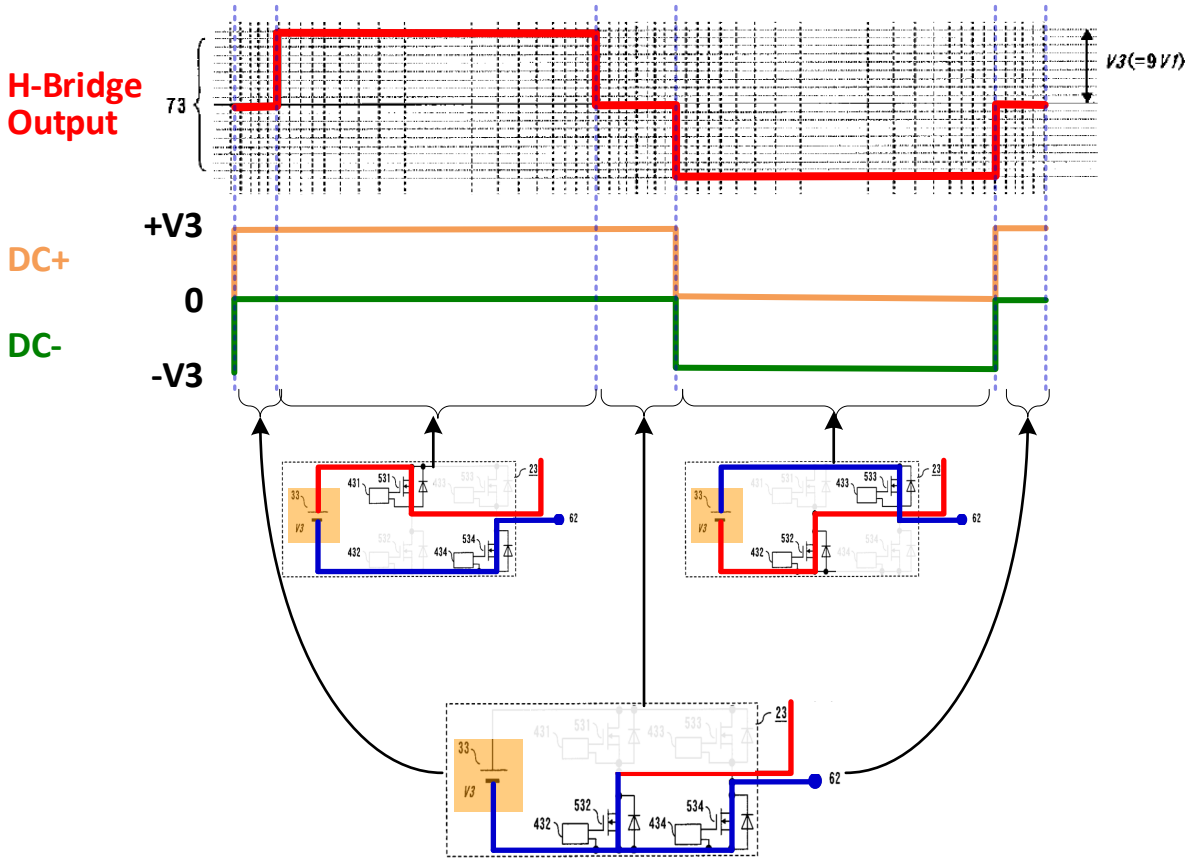


Id., Fig. 1 (cropped, annotated)

See Id., ¶¶ [0009]-[0011]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b; Ex. 1202, ¶ 246.

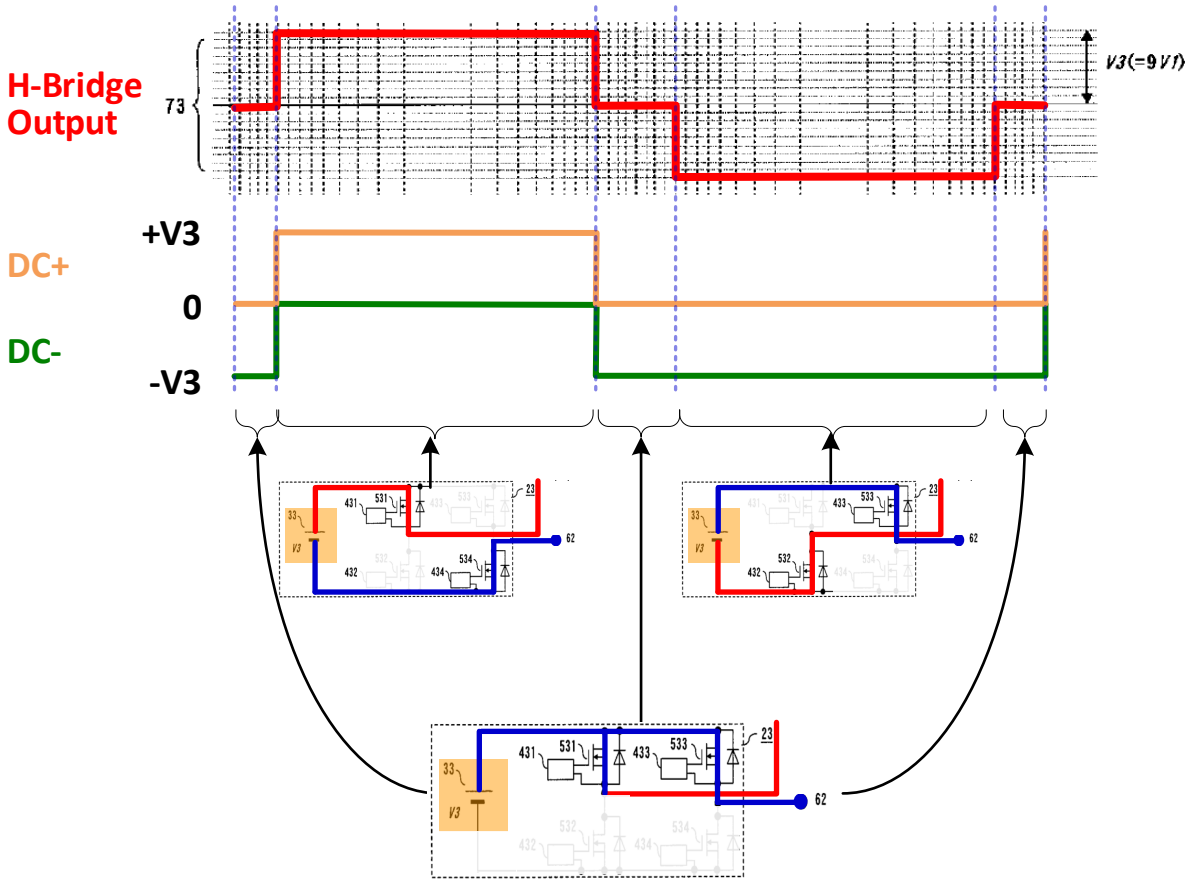
Using these states, as shown below, the output of H-bridge 23 is switched between the three voltages (+V3, 0, -V3) in its cyclical pattern (**red**), with either the positive or negative terminal of DC supply 33 being connected neutral 62 (**blue**). This causes the positive (**orange**) and negative (**green**) terminals of DC supply 33

to shift above (in the positive and pass-through low states) and below (in the negative and pass-through high states) the voltage on the neutral terminal 62 (**blue**). Ex. 1202, ¶ 247. As illustrated below, this pattern causes a common-mode square waveform to appear at the same frequency as the AC output waveform relative to neutral 62 and in the same phase on both DC+ and DC- terminals of DC supply 33, thus disclosing element [1E]. Ex. 1202, ¶¶ 247-250; Ex. 1204, ¶¶ [0009]-[0011]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b; Ex. 1245, pp. 10-11.



Ex. 1204, Figs. 1, 2 (cropped, annotated); Ex. 1202, ¶ 248.

In the drawing above where the pass-through low state is used, the positive half of the common-mode waveform (**orange** and **green**) is longer than the negative half of the waveform. Ex. 1202, ¶ 248. Alternatively, using the pass-through high state as shown below, the positive half is shorter than the negative half. *Id.*, ¶ 249.

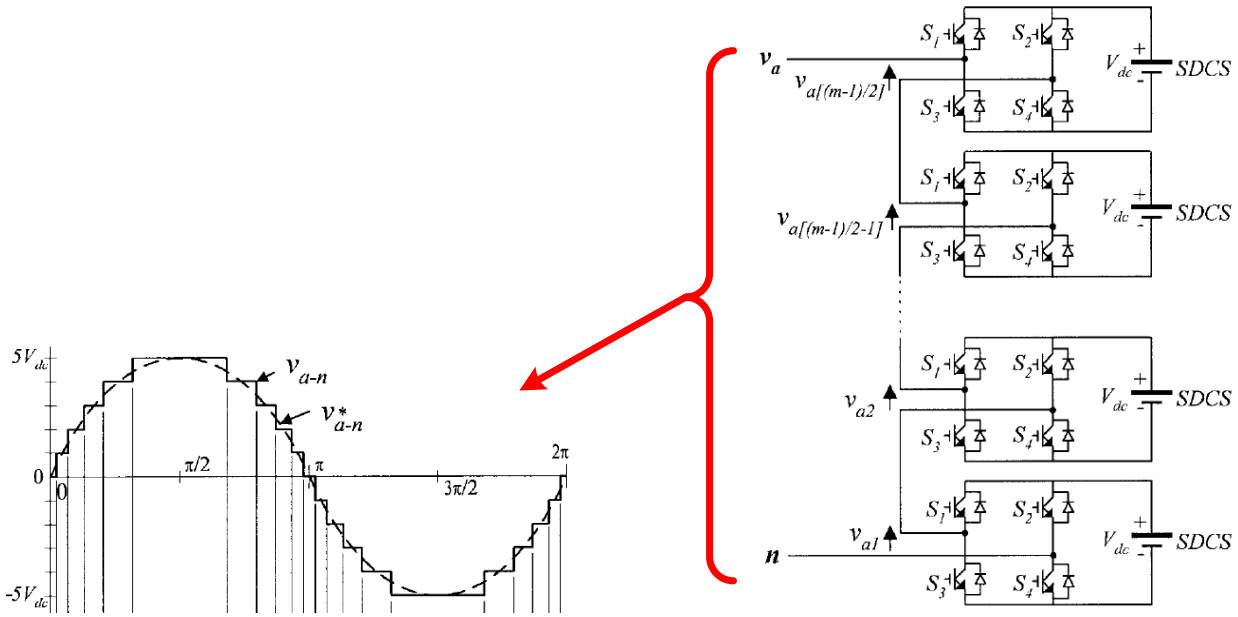


Ex. 1204, Figs. 1, 2 (cropped, annotated); Ex. 1202, ¶ 249.

Mori does not indicate which or if both of the two pass-through states are used to output 0 volts, but one must be used. And, it would have been obvious to use either or both pass-through states, given the limited number of possible schemes for producing Mori's waveforms. Ex. 1202, ¶ 250. Regardless, the difference in using

either pass-through state only slightly changes the generation of the common-mode voltage without changing the common-mode voltage frequency. *Id.* Thus, in any case, the common-mode square waveform has the same frequency as the AC output waveform as required by the claim. *Id.*, ¶¶ 248-251; Ex. 1204, ¶¶ [0009]-[0011]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b; Ex. 1245, pp. 10-11.

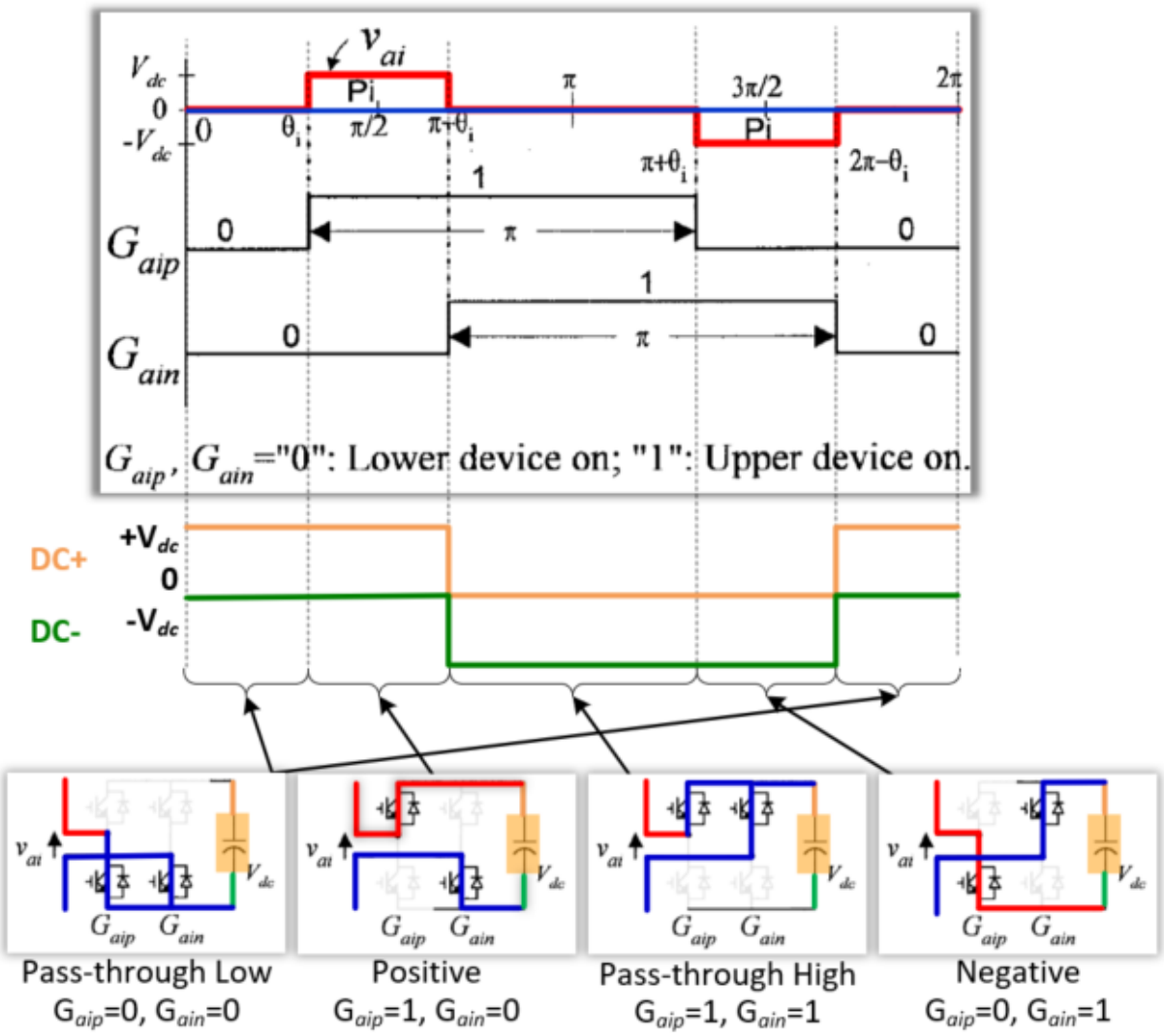
To the extent PO argues that Mori fails to disclose the H-bridge states that cause the claimed common-mode waveform, Tolbert does. Ex. 1202, ¶ 252. Like Mori, Tolbert discloses an inverter in which the outputs of multiple H-bridges are connected in series to generate an AC waveform.



Ex. 1244, Figs. 1 and 2(a) (cropped) (annotated)

Ex. 1202, ¶ 252; Ex. 1244, pp. 37-38.

In Tolbert, each H-bridge is controlled to output +V, 0, and –V (the same as Mori's H-bridge 23) according to 2 bits—G_{aip} which controls transistors S1, S3 in opposite states and G_{ain} which controls transistors S2, S4 in opposite states. Ex. 1202, ¶ 253; Ex. 1244, pp. 37-38, Figs. 1, 2a. For each side of the H-bridge (S1/S3 on the left and S2/S4 on the right), a bit value of 1 turns on the top transistor and turns off the bottom transistor, and a bit value of 0 turns off the top transistor and turns on the bottom transistor. Ex. 1202, ¶ 253; Ex. 1244, Fig. 2b. These bits control the H-bridge sequentially into the pass-through low state, the positive state, the pass-through high state, and the negative state, creating the common-mode waveform in element [1F] by shifting voltage on the positive (**orange**) and negative (**green**) DC input lines above and below neutral (**blue**) at the same frequency as the H-bridge output **(red**):



Ex. 1244, Fig. 2(b) (cropped, annotated)

Ex. 1202, ¶¶ 253-256; Ex. 1244, pp. 37-38.

A PHOSITA would have been motivated to use the control bits and sequence taught in Tolbert for controlling Mori's H-bridge 23 because they produce the same voltage outputs disclosed in Mori and because Tolbert teaches this sequence beneficially causes all of the switching devices in the H-bridge to conduct with equal times, equalizing the stress on each device. Ex. 1202, ¶ 257; Ex. 1244, pp. 37-38.

Moreover, such a combination would have been a simple substitution of one known element (Mori's H-bridge control timing) with another known element (Tolbert's H-bridge control timing) to obtain a predictable result (the same H-bridge output waveform and the same input common-mode waveform). Ex. 1202, ¶¶ 258-259.

A PHOSITA would have reasonably expected success in combining these elements as the combination merely requires applying simple logic to control known H-bridge switches, which was well within the level of ordinary skill in the art. *Id.*, ¶ 260.

2. Independent Claim 8

a. [8A]: "A method of converting power from a direct current source with improved efficiency to provide AC output power at a standard voltage and frequency and to a number of output terminals corresponding to the number of phases required, comprising:"

To the extent the preamble is limiting, Mori discloses it. Ex. 1202, ¶¶ 274-281. Mori describes a single-phase multiplex inverter 1 that converts power from multiple DC sources to produce a sine wave AC power output waveform (V_{inv}) at a single output terminal 61 (claimed "number of output terminals corresponding to the number of phases required"). Ex. 1204, Figs. 1-2, 16, ¶¶ [0007], [0009], [0011]-[0012], [0034]; Ex. 1202, ¶ 275.

Mori's inverter has "improved efficiency" because it reduces CPU processing load compared to prior inverters by using a digital arithmetic circuit, independent

from the CPU, to generate drive signals for H-bridge switches in the inverter. Ex. 1204, ¶¶ [0005]-[0008], [0022]. Further, Mori's inverter has "improved efficiency" by outputting "an extremely smooth voltage waveform," reducing filtering requirements. Ex. 1204, ¶¶ [0012]-[0013]; Ex. 1202, ¶ 277.

A PHOSITA would understand that Mori's AC output is "at a standard voltage and frequency." Ex. 1202, ¶¶ 276-278. Although the '822 patent does not indicate what is "standard," the '822 patent distinguishes AC voltages shaped as single-phase and three-phase sine waves (which have fixed amplitudes and frequencies) as being compatible with a greater variety of loads as compared to other forms of AC power (*e.g.*, square waves). Ex. 1201, 1:10-41. A PHOSITA would have understood that Mori's inverter is compatible with various loads, and thus its output AC voltages are "standard." Ex. 1204, ¶¶ [0001]-[0007]; Ex. 1202, ¶ 278. Accordingly, Mori's "highly accurate" single frequency sine wave voltage, for output to a load, is "at a standard voltage and frequency." Ex. 1202, ¶ 278; Ex. 1204, Figs. 2, 3, ¶¶ [0012]-[0013].

To the extent PO argues that Mori does not disclose a "standard voltage and frequency," these features would have been obvious, since as the '822 patent acknowledges, inverters were known to drive a variety of loads (*e.g.*, induction motors, cellphones, battery chargers, utility grids), and standards existed in the U.S. for powering such loads with sinusoidal voltage at specific amplitudes and

frequencies. Ex. 1202, ¶ 279; Ex. 1201, 1:10-41, 2:32-3:3, 17:51-52("60 Hz AC (in the US)"); 27:27-29, 37:38-43 ("US 277/480-volt service"), Ex. 1237, 2:43-57; Ex. 1238, ¶ [0057]; Ex. 1239, Figs. 1, 4-5, 1:25-29, 3:9-18; Ex. 1240, Fig. 3, 1:40-57, 5:42-44, 6:13-18; Ex. 1232, 14:58-61, 15:19-27, 23:32-34, 33:18-22, 37:40-43, 41:17-20, 48:58-67. Applying such standards for the purpose of making Mori's inverter useful in the U.S. would have been the simple application of a known technique (selecting a standardized voltage and frequency) to a known device (Mori's inverter) in the same way as every other inverter that operated with standardized power in the U.S. (*e.g.*, with a U.S. utility grid). Ex. 1202, ¶ 279. Applying such standards would have been obvious to try because there are a finite number of predictable solutions (due to the standardized voltage level and frequency of the U.S. utility grid) in which Mori's inverter is useful in the U.S., and a PHOSITA would have reasonably expected to succeed in making Mori's inverter useful. Ex. 1202, ¶ 280.

A PHOSITA would have had a high expectation of success in adapting Mori's inverter to such standards, since using them was pervasively well known and within the level of ordinary skill in the art. *Id.*; Ex. 1204, Figs. 2, 3, ¶¶ [0012]-[0013]; Ex. 1237, 2:43-57, Fig. 1.

b. [8B]: "configuring said direct current source to be floating"

Mori's DC power sources 31-33 are floating, since their terminals are connected only to the inputs of the inverter and are not permanently tied to any established potential such as neutral 62. Ex. 1202, ¶¶ 281-282; Ex. 1204, ¶ [0002]; Ex. 1201, 6:17-29, 9:51-60, 23:37-42; Ex. 1236, p. 6; Ex. 1242, p. 6. *See* Section V.A.1.c, *supra*.

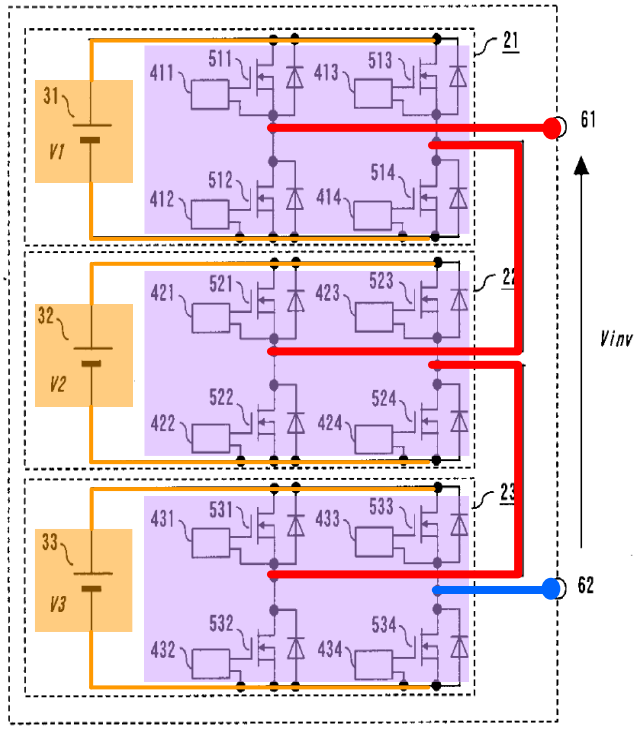
c. [8C]: "connecting the negative line from said direct current source to a first output terminal required to be instantaneously negative relative to all other output terminals

while deriving from the direct current source positive voltage line the instantaneous voltages required to be output from the other output terminals relative to said first terminal

in a rotating sequence with connecting the positive line from said direct current source to a next-in-sequence output terminal required to be instantaneously positive relative to all other output terminals

while deriving from the negative line of the direct current source the instantaneous voltages relative to said next-in-sequence terminal required to be output from the other terminals"

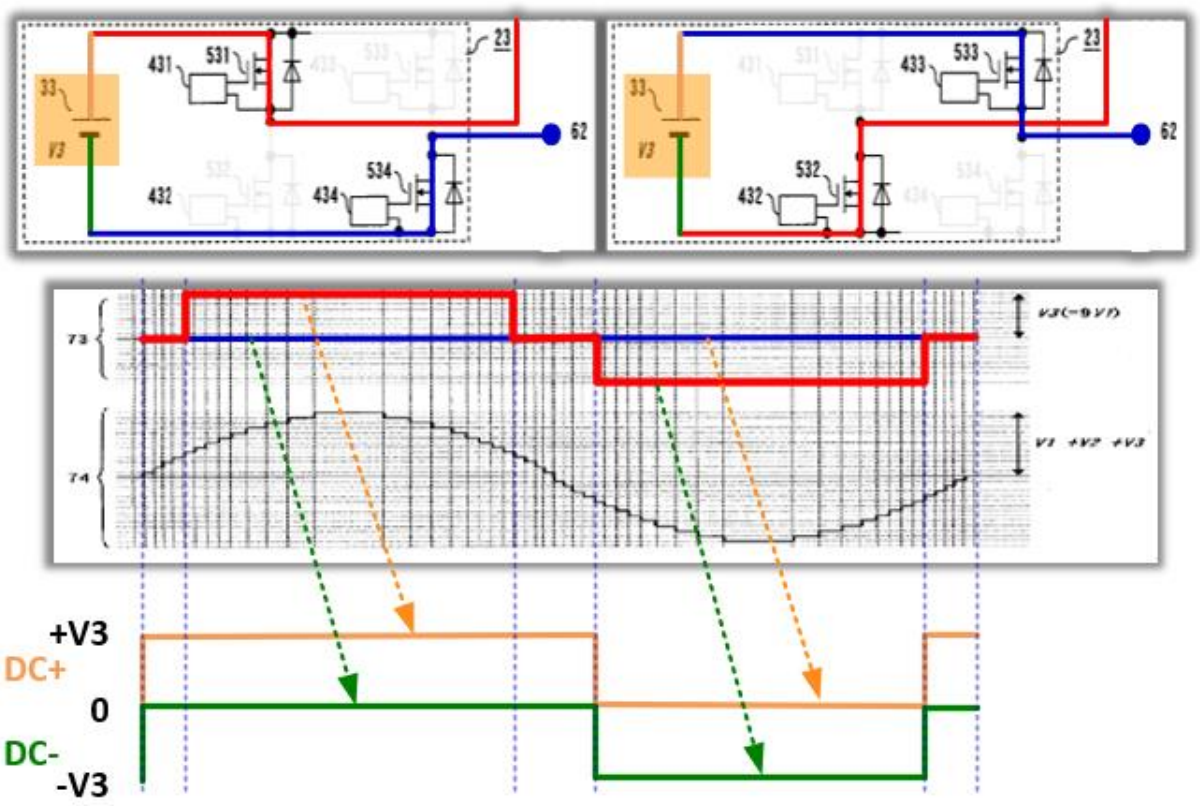
Mori discloses this limitation. Ex. 1202, ¶¶ 283-290. As discussed (*see* Sections V.A.1.a-c, *supra*), Mori's H-bridge 23 is connected at its input to DC supply 33 (claimed "direct current source"), connected at one output terminal (**red**) to output terminal 61 through H-bridges 21 and 22, and connected at its other output terminal directly to neutral 62 (**blue**):



Ex. 1204, Fig. 1 (annotated)

Ex. 1204, Fig. 2, ¶¶ [0007], [0009], [0011]-[0012], [0034]; Ex. 1202, ¶ 283.

To generate the sine wave output (*see* Sections V.A.1.d, *supra*), Mori and Mori-Tolbert teach modulating H-bridge 23 between three voltages (+V3, 0, -V3) in a cyclical pattern (**red** below, claimed "rotating sequence"), which alternatively connects DC supply 33 (in its positive state) to output terminals 61 (through H-bridges 21 and 22) and 62 during the positive half of the sine wave, and in reverse polarity (in its negative state) to those same terminals during the negative half of the sine wave:



Ex. 1204, Figs. 1, 2 (both cropped and annotated)

Ex. 1204, ¶¶ [0009]-[0011], [0015], [0018]-[0021]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b; Ex. 1202, ¶ 284.

While in the positive state during the positive half of the output sine wave, H-bridge 23 connects the negative DC input terminal to output terminal 62 (**blue**) (the "first output terminal") through switch 534, which, at that time, is "instantaneously negative" relative to the other output terminal 61 (**red**). Ex. 1202, ¶¶ 285-286; Section V.A.1.e, *supra*; Ex. 1204, Figs. 1, 2, ¶¶ [0009]-[0011], [0015], [0018]-[0021]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b.

While in the negative state during the negative half of the output sine wave, H-bridge 23 connects the positive DC input terminal to output terminal 62 (**blue**) through switch 533, which, at that time, is "instantaneously positive" relative to the other output terminal 61 (**red**) (claimed "next-in-sequence output terminal required to be instantaneously positive relative to all other output terminals"). Ex. 1202, ¶ 287; Section V.A.1.e, *supra*; Ex. 1204, Figs. 1, 2, ¶¶ [0009]-[0011], [0015], [0018]-[0021]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b.

During both sine wave halves, the sine wave output voltage on output terminal 61 is generated from the input terminal of DC supply 33 not connected to output terminal 62 (and from the other H-bridges 21 and 22) (claimed "deriving from the [direct current source positive/negative line] the instantaneous voltages…"). Ex. 1204, Figs. 1, 2, ¶¶ [0009]-[0011], [0015], [0018]-[0021]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b; Ex. 1202, ¶¶ 288-290.

d. [8D]: "selecting the timing of said rotating sequence such that a common mode waveform with a characteristic repetition frequency appears in phase on both the direct current source positive and negative lines."

Mori and Mori-Tolbert discloses this limitation. Ex. 1202, ¶¶ 291-297. As explained (*see* Sections V.A.1.e, V.A.2.c, *supra*), the structure, switch states, and timing of H-bridge 23 in Mori and Mori-Tolbert is the same as that of H-bridge 120a in the '822 patent, resulting in the same common-mode square wave, having the

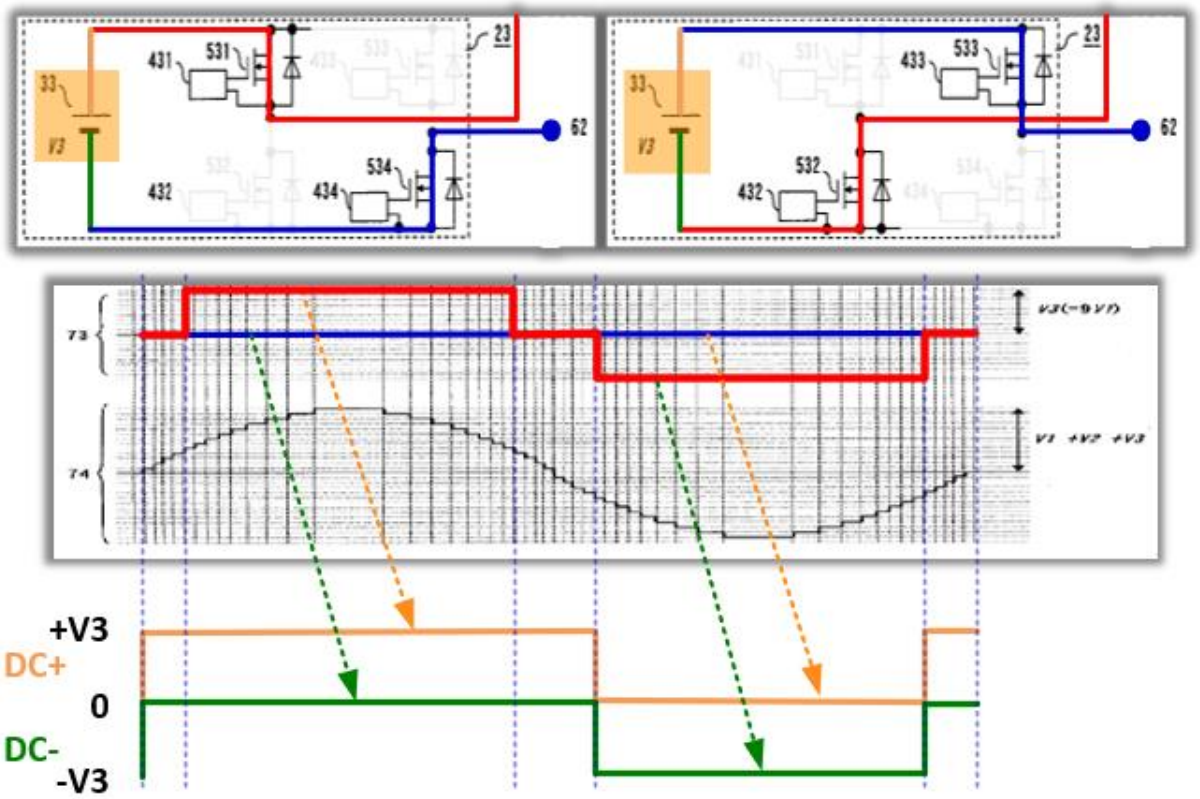
same frequency as the AC output waveform, superimposed in phase on both terminals of the DC supplies respectively connected to the inputs of the H-bridges. Ex. 1202, ¶¶ 291-297; Ex. 1201, 7:51-55, 9:51-59, 10:40-57, 10:65-11:9, 12:39-51, 15:36-38, 18:21-26, 23:54-57; Ex. 1204, Figs. 2, 4, ¶¶ [0002], [0004], [0009]-[0012], [0015]-[0019]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, Figs. 1, 2a, 2b, pp. 37-38; Ex. 1245, pp. 10-11; Ex. 1264, 51-57, 302-310; Ex. 1265, 51-57, 323-337, 385-398. Mori's multiplex inverter 1 selects "the timing of said rotating sequence such that a common mode waveform with a characteristic repetition frequency appears in phase on both" inputs from DC supply 33, thus teaching element [8D]. Ex. 1202, ¶ 294.

3. Dependent Claim 2

The apparatus of claim 1 wherein said DC to AC converter further comprises: a first electronic switch controlled by a switching controller to connect said positive DC input terminal to the instantaneously most positive of said set of AC output terminals and said at least one ground, neutral or reference potential terminal alternating with connecting said negative DC input terminal to the instantaneously most negative of said set of AC output terminals and said at least one ground, neutral or reference potential terminal

As explained (*see* Sections V.A.1.e, V.A.2.c, *supra*), Mori teaches that H-bridge 23, during the positive half of the output sine wave, connects the negative DC input terminal to neutral output terminal 62 (**blue**), which at this time is more negative than output terminal 61 (**red**), and during the negative half of the output sine wave, connects the positive DC input terminal to neutral output terminal 62

(**blue**), which at this time is more positive than output terminal 61 (**red**) (claimed "connect said positive DC input terminal to the instantaneously most positive [AC output terminal] and said [neutral] terminal alternating with connecting said negative DC input terminal to the instantaneously most negative [AC output terminal] and said [neutral] terminal"):



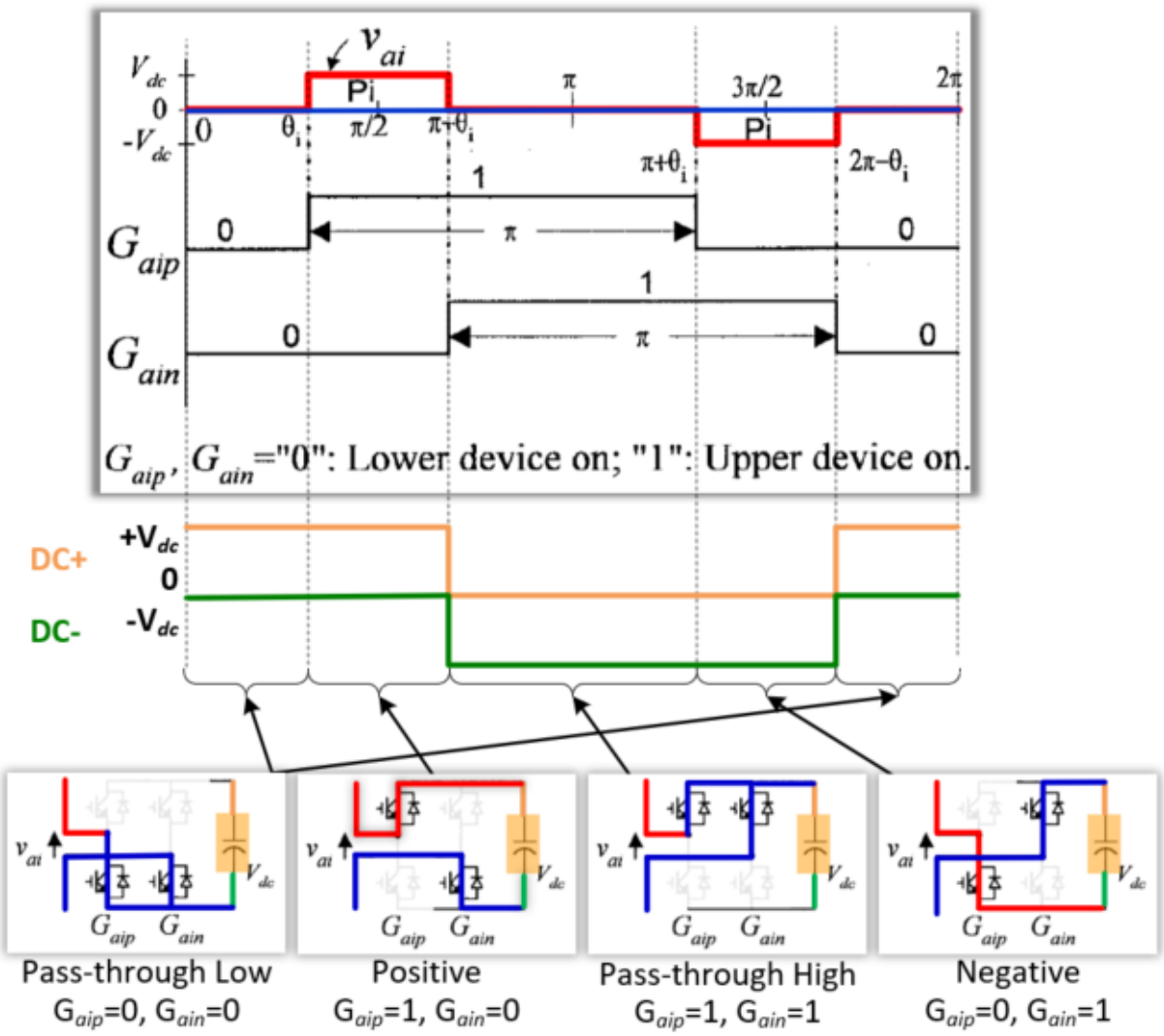
Ex. 1204, Figs. 1 and 2 (both cropped, annotated)

Id., ¶¶ [0009]-[0012], [0015], [0018]-[0021]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1202, ¶¶ 262-265; Section V.A.1.e, *supra*.

Alternatively, connecting the positive/negative DC input terminals to output terminal 61 (**red**) when it is "most positive" during the positive half of the sine wave

and "most negative" during the negative half of the sine wave also teaches claim 2. Ex. 1202, ¶¶ 262-263; Ex. 1204, ¶¶ [0009]-[0012], Fig. 2; Section V.A.1.e, *supra*.

As discussed in Section V.A.1.e, Mori's DC-to-AC converter uses the positive, negative, and at least one of two pass-through states in a manner that discloses claim 2's switching pattern. Ex. 1204, ¶¶ [0009]-[0012], Fig. 2. To the extent PO contends that Mori lacks disclosure of such states, Tolbert discloses a switching pattern that uses them to produce the same output in Mori, as shown below and discussed above in Section V.A.1.e. As shown below, Tolbert's switching pattern includes alternating between using the pass-through low state where the negative (**green**) terminal of DC supply V_{dc} is connected to the AC output terminal (**red**) and neutral (**blue**) and using the pass-through high state where the positive (**orange**) terminal of DC supply V_{dc} is connected to the AC output terminal (**red**) and neutral (**blue**):



Ex. 1244, Fig. 2 (cropped, annotated)

Ex. 1244, Fig. 2b, pp. 37-38; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1202, ¶¶ 266-268.

For the same reasons discussed in Section V.A.1.e (*e.g.*, to produce Mori's voltage waveforms), a PHOSITA would have been motivated to use the switching sequence as taught in Tolbert for Mori's H-bridge 23 and had a reasonable expectation of success. Ex. 1202, ¶¶ 257-260, 268. Thus, whether or not claim 2

requires alternating between both pass-through states, Mori and/or Mori-Tolbert teach claim 2. Ex. 1202, ¶¶ 268-269.

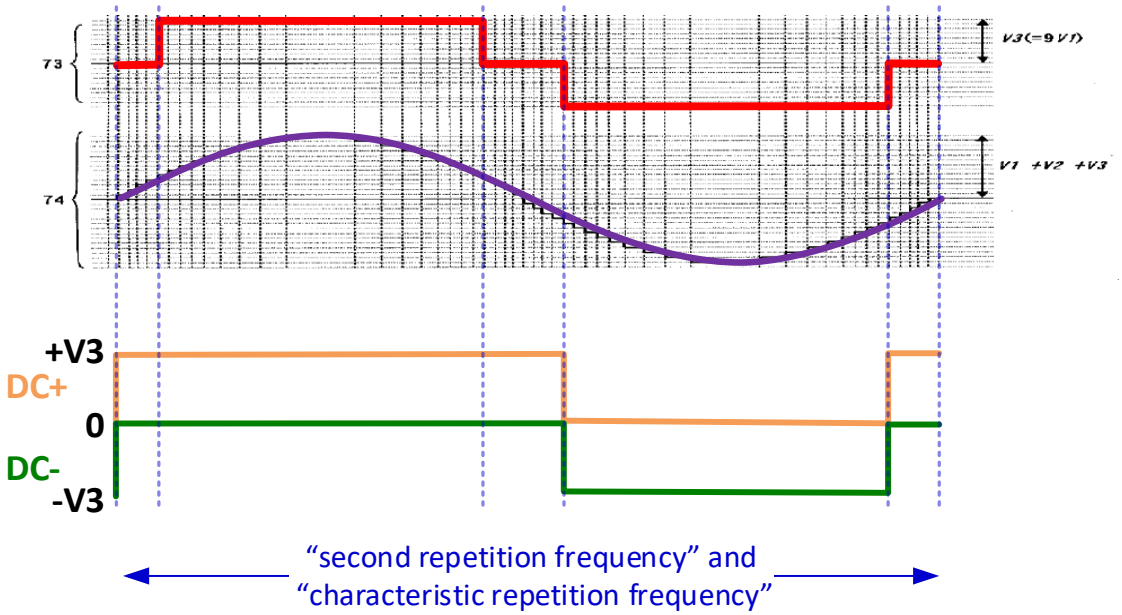
The '822 patent describes a corresponding structure of the "switching controller" as including "a microcontroller" with "memory." Ex. 1201, 12:26-51, 24:8-12; *see* Section IV.B.2, *supra*. Mori's control circuit (claimed "switching controller") performs claim 2's function and is similarly described as a "CPU (Central Processing Unit) 10 and a PLD (Programmable Logic Device) circuit 11" and a "microcomputer or a microcomputer-based controller such as a DSP (Digital Signal Processor)." Ex. 1202, ¶ 270; Ex. 1204, ¶¶ [0006]-[0008], [0015], Figs. 4, 9, 10, 13, 15. A PHOSITA would have understood that CPUs and microcomputers execute software stored in memory. Ex. 1202, ¶ 270. Both controllers are insubstantially different from and perform the same functions (as in claim 2) in the same way (controlling H-bridge using drive signals) for the same result (connecting positive and negative DC input terminals to the instantaneously most positive and negative of the AC output terminals and neutral). *Id.*, ¶ 271.

4. Dependent Claims 3 and 9

Claim 3: The DC to AC conversion apparatus of claim 1 wherein said second repetition frequency is a multiple equal to the same said number N of said first repetition frequency and said number N is equal to 1, 2 or 3.

Claim 9: The method of claim 8 in which said characteristic frequency is a multiple of 1, 2 or 3 times the AC output power frequency.

Mori's single-phase converter has one live AC output terminal—"N" is 1. *Id.*, ¶¶ 272-273. As explained (*see* Section V.A.1.e, V.A.2.d, *supra*), Mori's common-mode voltage waveform (**orange** and **green**) frequency (claimed "second repetition frequency" and "characteristic frequency") is the same as its AC output's frequency (**purple**) (claimed "first repetition frequency" and "AC output power frequency"):



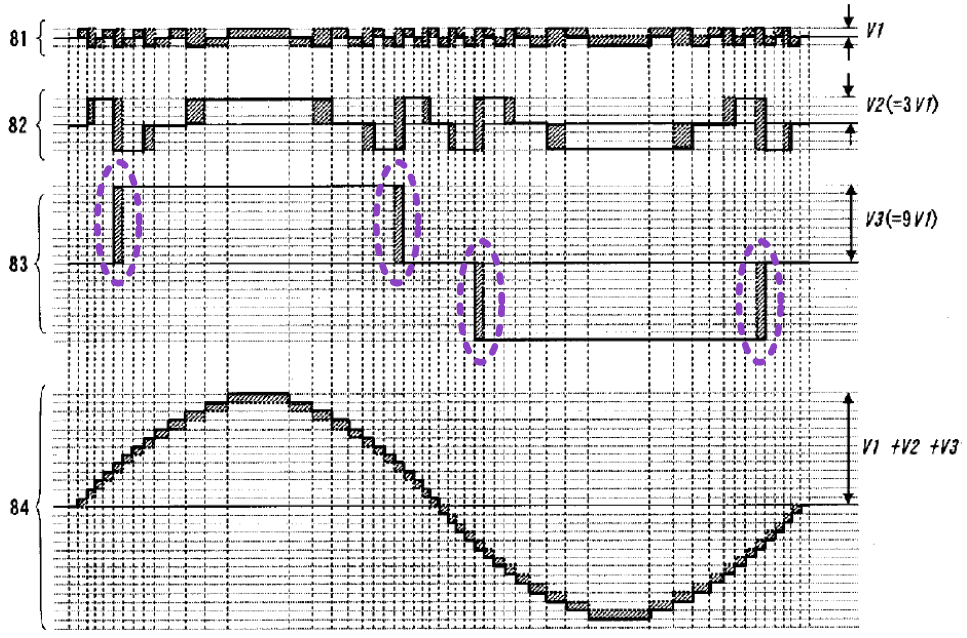
Ex. 1204, Fig. 2 (cropped, annotated)

Ex. 1204, ¶¶ [0002], [0004], [0009]-[0012]; Ex. 1202, ¶¶ 272-273, 298-299.

5. Dependent Claim 10

The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive line or negative line comprises using one of . . . (b) a pulse-width modulator.

Mori discloses this claim. Ex. 1202, ¶¶ 300-302. As explained, the "step of deriving instantaneous voltages from the direct current source positive line or negative line" is disclosed by the operation of H-bridge 23 in Mori and Mori-Tolbert. *See* Section V.A.2.c, *supra*; Ex. 1202, ¶ 301; Ex. 1204, Figs. 1, 2, ¶¶ [0009]-[0011], [0015], [0018]-[0021]. Mori further discloses PWM control unit 2 in CPU 10 (claimed "pulse-width modulator") that uses "PWM (Pulse Width Modulation) control [] together with gradation control" at the transitions between H-bridge states (**purple**):



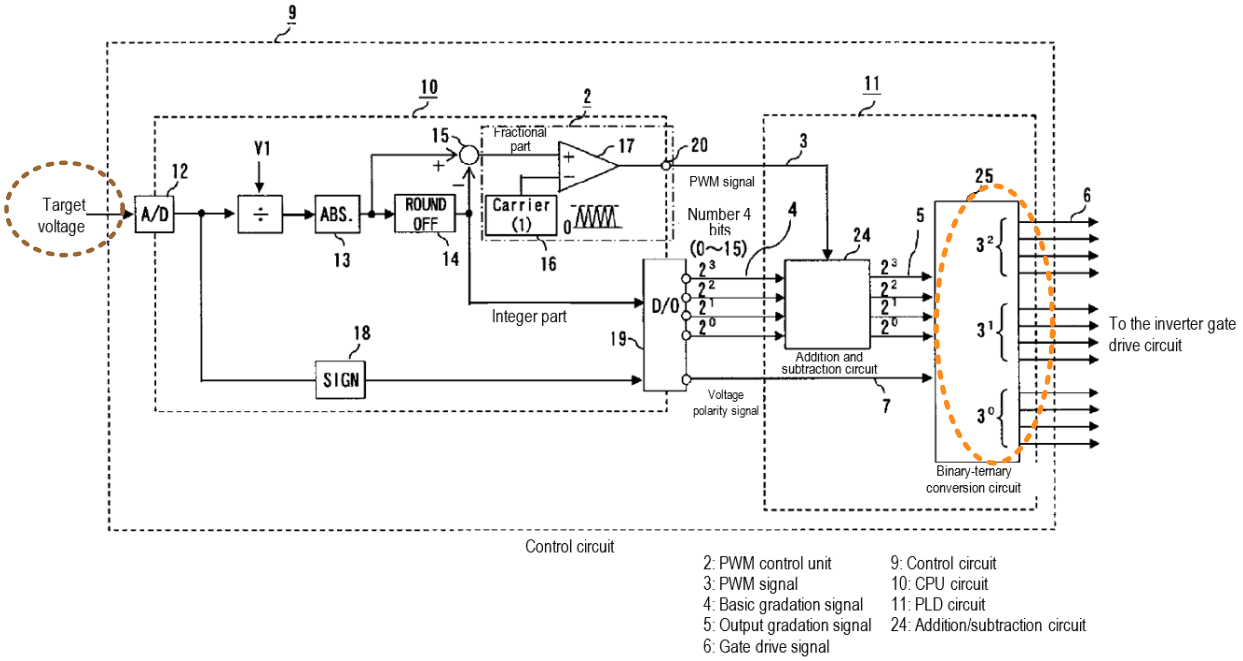
Ex. 1204, Fig. 3 (annotated)

Ex. 1204, Figs. 8-15, ¶¶ [0005], [0011], [0013]-[0015], [0017]-[0018], [0021]-[0034]; Ex. 1202, ¶¶ 301-302.

6. Dependent Claim 12

The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive line or negative line comprises expressing a desired voltage using a finite number of digits (T(n), T(n-1), T(n-2) . . . T3,T2,T1) in a ternary number system such that the instantaneously desired voltage is equal to 3^{m}[T(n)+T(n−1)/3+T(n−1)/9+. . . T1/$3^{(n-1)}$ or 3T(n)+T(n−1)+T(n−1)/3+. . . T1/$3^{(n-)}$] times the voltage from said direct current source, where the power m may be zero.

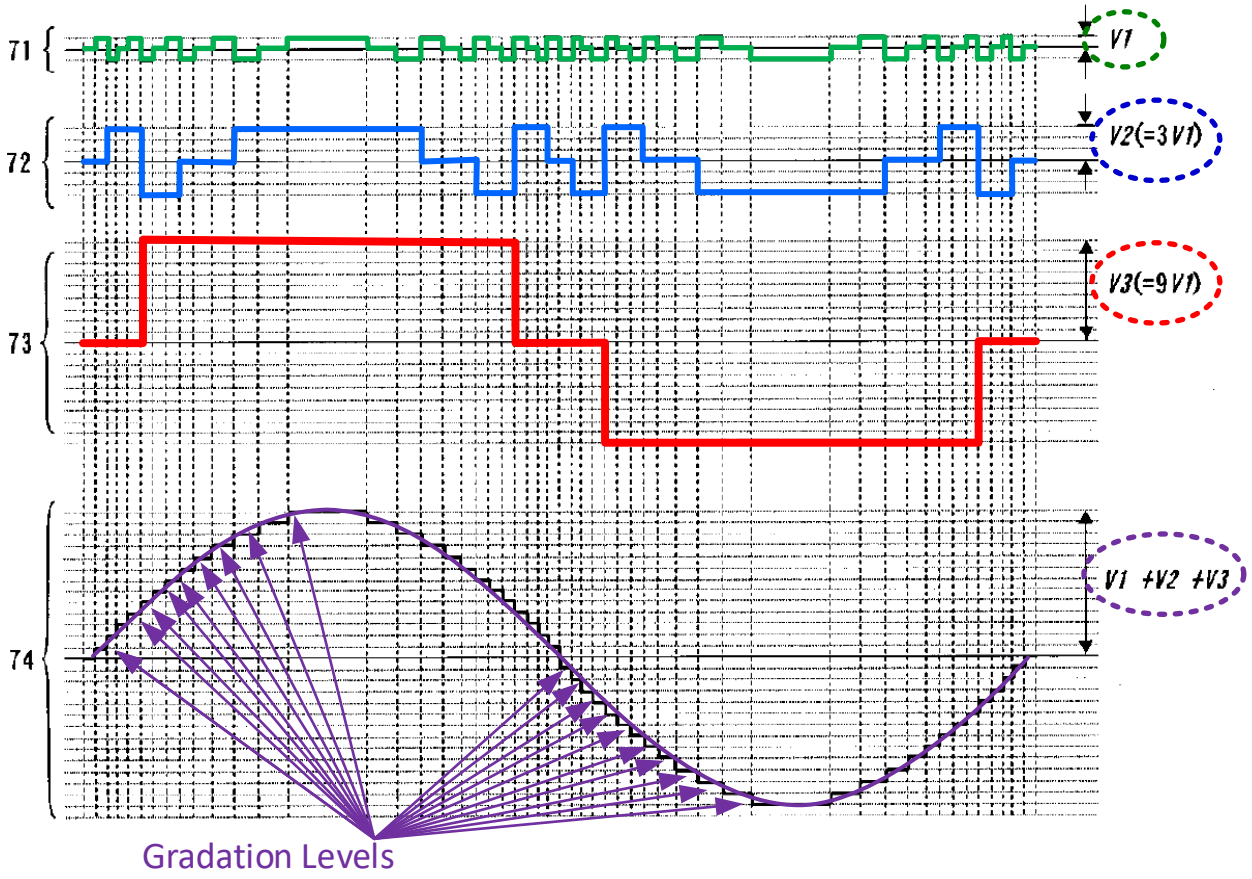
Mori and Mori-Tolbert teach "said step of deriving instantaneous voltages from the direct current source positive line or negative line." *See* Section V.A.2.c, *supra*; Ex. 1202, ¶¶ 303-314. Mori further discloses control circuit 9 that samples a target voltage (**brown**) (claimed "desired voltage") and converts the target voltage into a ternary number having three ternary digits (3^2, 3^1, 3^0) (**orange**) (claimed "finite number of digits ([] T3, T2, T1) in a ternary number system"):



Ex. 1204, Fig. 4 (annotated)

Ex. 1204, ¶¶ [0015]-[0019]; Ex. 1202, ¶ 304.

Each of Mori's H-bridges 23, 22, and 21 is controlled to output its respective input voltage—9V, 3V, and 1V—multiplied by the state (*i.e.*, +1, 0, -1) of the respective corresponding ternary digit (3^2, 3^1, 3^0) so that H-bridge 23 outputs +9V, 0V, or -9V (**red**), H-bridge 22 outputs +3V, 0V, or -3V **(blue**), and H-bridge 21 outputs +1V, 0V, or -1V (**green**)—with the outputs summed to generate a single-phase waveform (**purple**) as a sequence of small voltage gradations:



Ex. 1204, Fig. 2 (annotated)

Ex. 1204, ¶¶ [0002], [0007], [0011]-[0012], [0019]-[0020], claim 1; Ex. 1202, ¶ 305. Mori's instantaneously desired voltage for a phase is 9V*T3+3V*T2+1V*T1. Ex. 1202, ¶ 306.

Claim 12 further recites that the instantaneously desired voltage is equal to either of two recited formulas—one of which is reproduced and annotated below—times the voltage from the DC source:

$$3^{m}[\ T(n) + T(n-1)/3 + T(n-1)/9 + \ldots\ T1/3^{(n-1)}].$$

Ex. 1201, 42:66-43:7. A PHOSITA would have understood this formula as representing a weighted sum of ternary digits, with the multiplier (the weight) for

each digit defined by a sequence, with the beginning and end of the sequence given by the weights for T1 and T(n), and the middle expression (**blue**) providing a pattern for the weights of the intermediate digits. Ex. 1202, ¶¶ 307-308. However, for n ≥ 3, this middle expression has no discernible pattern, and thus cannot be understood. *Id.*, ¶ 308.

But for n=2, no intermediate digits exist, so a PHOSITA would have understood the formula to simplify to the first and last digit expressions (irrespective of what pattern the middle expression was intended to show for other n values). *Id.*, ¶ 309. Multiplying the formula by "the voltage from said direct current source," the formula for N=2 can be rewritten as:

$$\mathbf{V_{DC} * 3^m * [T2 + T1/3]}$$

Id. This formula is disclosed by Mori/Mori-Tolbert's control of H-bridges 22 and 23, which output ±3V and ±9V respectively, such that each instantaneous phase voltage is 9*T2+3*T1, for voltage steps where the output of H-bridge 21 is 0V. Ex. 1204, Fig. 2, ¶¶ [0002], [0007], [0011]-[0012], [0019]-[0020], claim 1; Ex. 1202, ¶ 310. This matches the above formula with m=0, but "m" can be scaled for different voltages V_{DC} (V_{DC}=V3=9V in this Mori/Mori-Tolbert combination). Ex. 1202, ¶ 310. The Mori/Mori-Tolbert combination as described above thus teaches claim 12.

Alternatively, it would also have been obvious to modify Mori/Mori-Tolbert to include only two H-bridges (removing H-bridge 21), such that Mori/Mori-Tolbert describes every voltage step with the formula 9*T3+3*T2 discussed above. It was known to include more or less H-bridge levels in Mori's design, with more H-bridges adding more voltage steps, and less H-bridges decreasing complexity, component count, and cost. *See e.g.*, Ex. 1244, pp. 36-37; Ex. 1231 (certified translation of Ex. 1230), Fig. 10, ¶ 24 (discussing simplicity of two-level H-bridge inverter); Ex. 1202, ¶ 311. This would have been nothing more than applying a known technique (reducing the H-bridges from three to two) to improve a similar device (by simplifying the design and reducing cost) in the same way as known to PHOSITAs. Ex. 1244, pp. 36-37; Ex. 1231, Fig. 10, ¶ 24; Ex. 1202, ¶ 312. Similarly, using two H-bridges would have been obvious to try since the design is scalable with only a finite number of possible levels being practical with a reasonable expectation of success. Ex. 1202, ¶ 312.

Moreover, varying the weighting of the multipliers would have been obvious to a PHOSITA in view of Mori/Mori-Tolbert and a PHOSITA's technical ability. *Id.*, ¶ 313. Mori expressly discloses six other ratios—1:2:4, 1:3:4, 1:3:5, 1:3:6, 1:3:7, and 1:2:8—and that pulse-width-modulating may be used to scale the magnitude of the inverter output from between 0 to V1, 0 to V2, and 0 to V3. Ex. 1204, Figs. 2-

3, ¶¶ [0002], [0011]-[0015]. Other references teach that other ratios were also known. Ex. 1244, pp. 37-38; Ex. 1207, Fig. 4, ¶ [0052]; Ex. 1202, ¶ 313.

The '822 patent does not describe its claimed weighting as novel or nonobvious or having any technical benefit over simply weighting by consecutive powers of three. Ex. 1202, ¶ 301. Unsurprisingly, mere changes in proportions or quantity do not render claims nonobvious. *Gardner v. TEC Systems, Inc*., 725 F.2d 1338, 1346, 1349 (Fed. Cir. 1984) (dimensional formula "made the application sound like something unique and inventive but had no real function"); *Iron Grip Barbell Co., Inc. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004) (a barbell weight having three openings for gripping was obvious in view of prior art's two and four openings). Furthermore, choosing an alternative weighting would have been nothing more than the obvious combining of prior art elements (Mori/Mori-Tolbert's inverter using multiple DC voltages) according to known methods (Mori's teaching of how different voltage ratios lead to different numbers and levels of voltage gradations to obtain a desired waveform and a PHOSITA's understanding of how to select the desired waveform optimized for a particular application) to obtain a predictable result (an inverter optimized for a particular application and filtering requirement). *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 91 USPQ2d 1225 (Fed Cir. 2009). Ex. 1202, ¶ 314.

Implementing Mori's inverter with different numbers of H-bridges (2 or 3) and with such alternative weighting ratios would have easily been within the level of ordinary skilled in the art and a PHOSITA would have had a reasonable expectation of success, since the implementation involves only the possible elimination of hardware (an H-bridge) with minimal or no modification to the control scheme, as evidence by Mori's disclosure of over 10 variations on weighting in Figure 4. *Id*.

B. Grounds 4, 5: Mori/Mori-Tolbert in view of De Renders Claims 6 and 20 Obvious

1. Dependent Claim 6

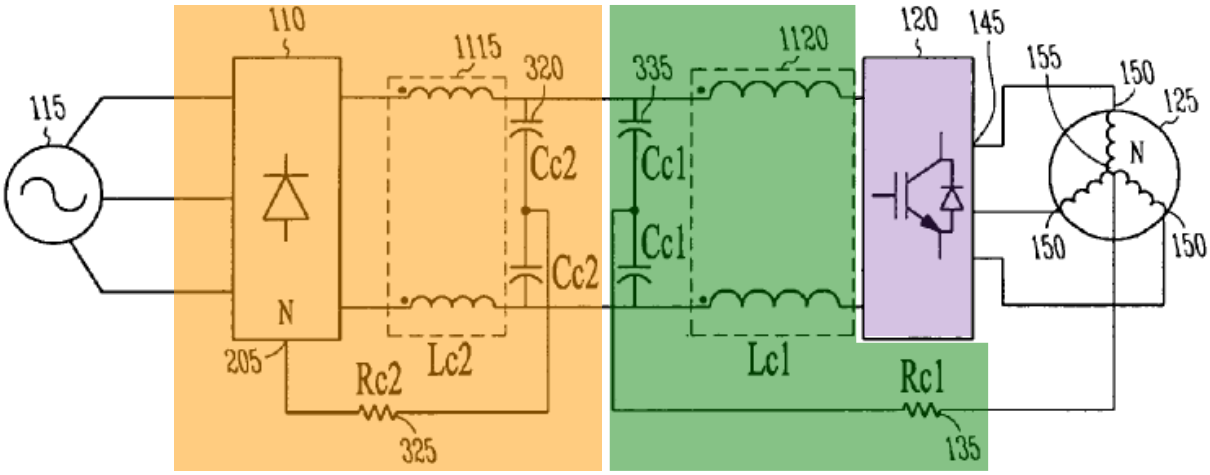
[6A] "The DC to AC conversion apparatus of claim 1, further comprising a common-mode filter connected between said DC to AC converter DC input terminals and said positive and negative terminals of said DC source, the common-mode filter being configured both"

[6B] "to prevent high frequency components of the DC to AC converter internal waveforms being exported to said DC source and"

[6C] "to minimize overshoot of said common-mode waveform in order to minimize peak voltages on said positive and negative terminals"

Mori and Mori-Tolbert do not disclose this claim, but De does. Ex. 1202, ¶¶ 315-326. Mori teaches that its DC sources 31-33 are generated from a three-phase converter that rectifies AC power into the multiple DC voltages. *Id.*, ¶ 318; Ex. 1204, ¶ [0002]. De discloses a similar configuration including an inverter (**purple**)

with a DC source generated from a three-phase rectifier circuit 11 (**orange**), but with an additional common-mode filter (Lc1, Cc1, Rc1) (**green**) connected between DC input terminals of the inverter (**purple**) and the positive and negative terminals of a DC source, as recited by element [6A].



Ex. 1218, Fig. 12 (annotated)

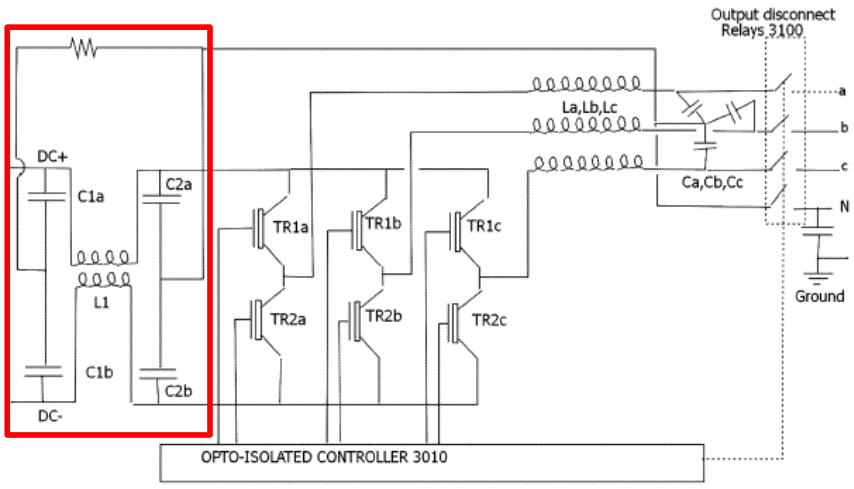
Id., ¶¶ [0020], [0033]-[0034], Fig. 11; Ex. 1202, ¶¶ 316-317.

A PHOSITA would have understood that De's inverter (like Mori's inverter) is a source of electromagnetic interference (EMI) in the form of common-mode noise caused by high frequency internal switching within the inverter. Ex. 1202, ¶¶ 318, 325; Ex. 1218, Abstract, ¶¶ [0001]-[0022]; Ex. 1204, ¶¶ [0005]-[0006], [0014]; Ex. 1210, pp. 1-2; Ex. 1241 at 943. De's filter prevents this common-mode noise from being exported to the DC source because De's inductor (Lc1) and capacitor (Cc1) form a low-pass common-mode filter loop with a resonant frequency (*i.e.*, the cutoff frequency above which waveforms are attenuated) selected to be one-third to one-

half of the inverter's internal switching frequency. Ex. 1218, ¶¶ [0021]-[0022]; Ex. 1202, ¶ 325. De's filter thus "prevent[s] high frequency components of the DC to AC converter internal waveforms being exported to said DC source" (element [6B]). *Id*.

Further, De's resistor (Rc1) "ensure[s] proper damping of the common-mode filter loop," which a PHOSITA would have understood to minimize common-mode voltage overshoot caused by the L-C filter resonating, and thus minimize peak voltages on the positive and negative inverter terminals as required in element [6C]. Ex. 1218, ¶ [0022]; Ex. 1210, pp. 6-9 (describing resistor for reducing overshoot at filter resonant frequency), Figs. 11-17; Ex. 1202, ¶ 326.

De's and the '822 patent's (Figure 16, below) common-mode filters are both second-order, low-pass L-C filters with equivalent structures.



Ex. 1201, Fig. 16 (annotated)

Ex. 1202, ¶¶ 322-324.

The exact multiples, values and arrangements of L, C, and R in De's common-mode filter are selected by a "designer with average skill" depending upon particular inverter parameters (*e.g.*, switching frequency), and thus any differences between the two filters is insubstantial. Ex. 1218, ¶ [0022]; Ex. 1210, pp. 6-9 (illustrating equivalent arrangements of L, C, and R for damping filter overshoot), Figs. 11-17; Ex. 1202, ¶ 323. The two filters perform the same function (filtering) in the same way (using passive components arranged as a second order filter) for the same result (reducing high frequency components and preventing overshoot). Ex. 1202, ¶ 323.

With similar DC sources and a similar switching scheme, a PHOSITA would have recognized that De's common-mode noise problem would apply equally to Mori and Mori-Tolbert, thus a PHOSITA would have been motivated to insert De's common-mode filter between Mori/Mori-Tolbert's DC power source (an AC-DC converter similar to De's rectifier) and Mori/Mori-Tolbert's inverter (similar to De's inverter) for the benefit of minimizing hazards caused by the inverter-generated high frequency common-mode leakage and to improve the electromagnetic compatibility of the inverter with other components in the system. Ex. 1218, ¶¶ [0001], [0021]-[0022], [0033]-[0034]; Ex. 1204, ¶¶ [0005]-[0006], [00014]; Ex. 1210, pp. 1-2; Ex. 1241 at 943; Ex. 1202, ¶ 318. Doing so would have been nothing more than the obvious use of a known technique (inserting De's common-mode filter between a power source and inverter) to improve a similar device (Mori's DC power source

and inverter) in the same way (by suppressing the common-mode current emitted by Mori's inverter). Ex. 1202, ¶¶ 319-320.

A PHOSITA would have reasonably expected success in combining these elements as the combination merely requires inserting additional filter components, and adjusting component values, which was well within the level of ordinary skill in the art. Ex.1218, ¶ [0022]; Ex. 1202, ¶ 321.

2. Dependent Claim 20

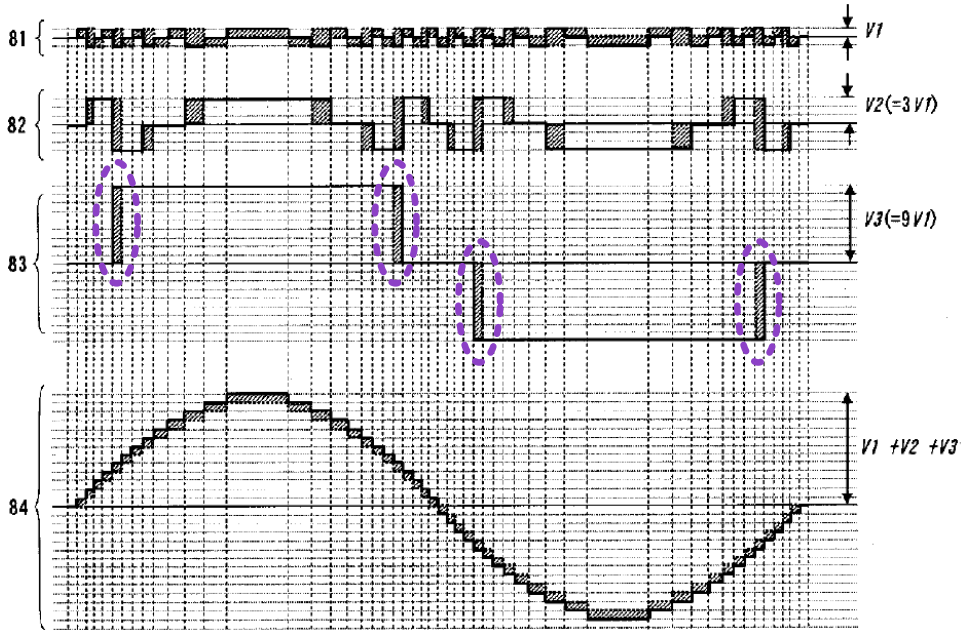
[20A] "The method of claim 8 in which connecting the positive line of said DC source to the instantaneously most positive of all output terminals alternating in a rotating sequence with connecting the negative line of said DC source to the most positive of all output terminals comprises connecting the DC source terminal to the selected output terminal through a common mode filter in order"

[20B] "to prevent high frequency components of said common-mode waveform being exported to said DC source and"

[20C] "to minimize overshoot of said common mode waveform in order to minimize peak voltages on said positive and negative terminals."

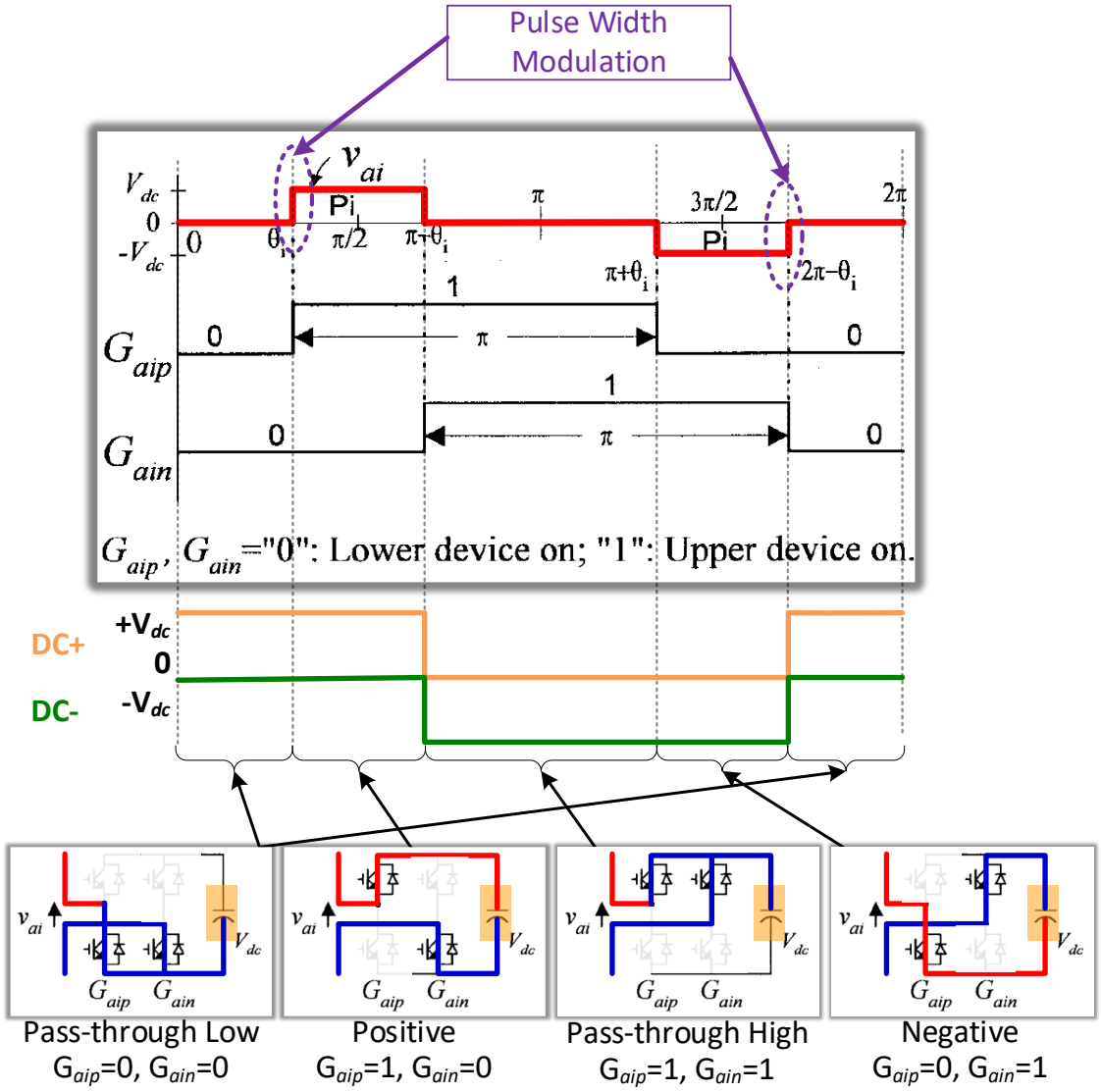
Mori-De and Mori-Tolbert-De teach this claim. Ex. 1202, ¶¶ 327-335. Element [20A] purportedly refers to element [8C] for connecting the positive and negative lines of the DC source in a rotating sequence to the "most positive" output terminal, but element [8C] recites a different limitation of connecting to the "most positive" and "most negative" output terminals in a rotating sequence. As explained (*see* Section V.A.2.c, *supra*), Mori discloses connecting the positive and negative

inputs in a rotating sequence respectively to the instantaneously "most positive" and "most negative" output terminals (**purple**) as in element [8C], while also pulse-width-modulating the H-bridges:



Ex. 1204, Fig. 3 (annotated)

See Section V.A.5, *supra*; Ex. 1202, ¶ 328. This pulse width modulating configures H-bridge 23 to alternate back-and-forth between (claimed "in a rotating sequence") the pass-through low and positive states during the positive half of the sine wave output or the pass-through low and negative states during the negative half of the sine wave output. *See* Section V.A.1.e, *supra*; Ex. 1202, ¶ 329. This occurs at, for example, the following state transitions:



Ex. 1244, Fig. 2(b) (cropped, annotated)

Ex. 1202, ¶ 330; Ex. 1244, pp. 37-38; Ex. 1204, ¶¶ [0009]-[0011]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1245, pp. 10-11. Rotating between the pass-through low and positive H-bridge states connects both DC lines to output terminal 61, which is "most positive" during the positive half of the sine wave output, and rotating between the pass-through low and negative H-bridge states connects both DC lines to output terminal 62, which is "most positive" during the negative half of

the sine wave output. Sections V.A.1.e, V.A.2.c, *supra*. Mori and Mori-Tolbert thus disclose the "connecting" steps of element [20A]. Ex. 1202, ¶¶ 327-331.

Mori-De/Mori-Tolbert-De, as explained with respect to claim 6, further teaches a common-mode filter between the inverter input terminals and the DC source that: prevents high frequency components of the inverter internal waveforms from being exported to the DC source; and minimizes common-mode voltage overshoot, which minimizes positive and negative terminal peak voltage. *See* Section V.B.1, *supra*. Thus, for the same reasons as discussed, Mori-De/Mori-Tolbert-De teaches elements [20B] and [20C]. *Id.*, ¶¶ 332-335.

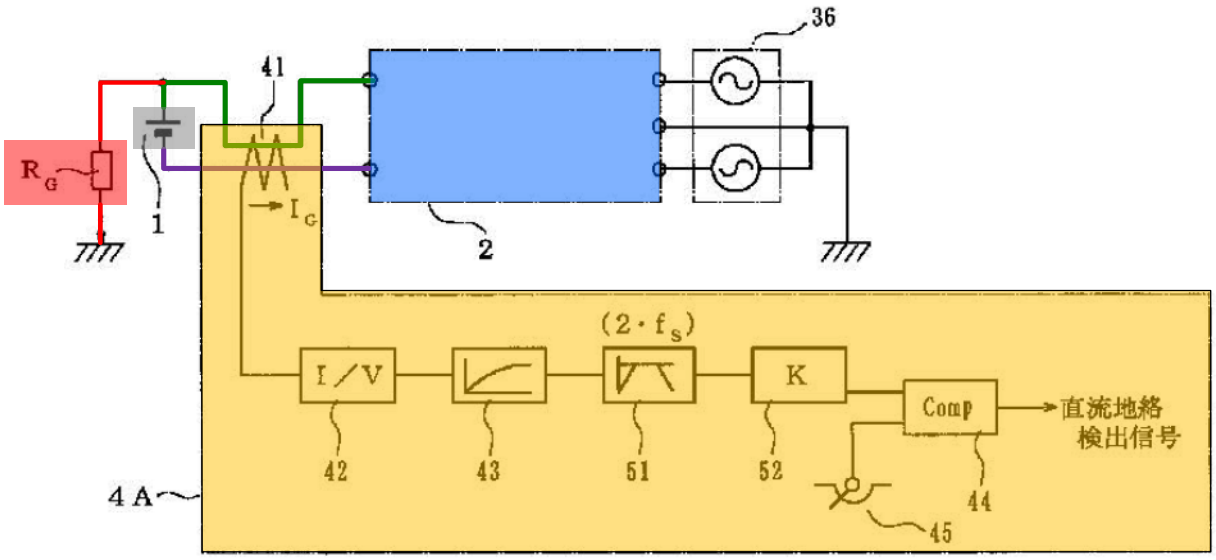
C. Grounds 6, 7: Mori/Mori-Tolbert in View of Fujimoto Renders Claims 4 and 11 Obvious

1. Dependent Claims 4 and 11

> **Claim 4: The apparatus of claim 1 further comprising an AC ground leak detector inserted in the positive and negative conductors between said DC source and said DC to AC converter, the AC ground leak detector being adapted to detect an imbalance current at said second frequency and to thereby provide a detection signal indicative of an unwanted leakage impedance from a DC conductor to ground.**
>
> **Claim 11: The method of claim 8 in which an unwanted leakage impedance to ground from a line of either polarity of said direct current source is detected by detecting a common-mode current with said common mode waveform at said characteristic repetition frequency.**

Mori/Mori-Tolbert does not describe claim 4's "ground leak detector" or claim 11's "detecting," but Fujimoto does. *Id.*, ¶¶ 336-351. Similar to Mori/Mori-

Tolbert, Fujimoto describes an inverter (**blue**) that converts power from a DC power supply (**grey**), which may be a solar cell, to AC power output to a three-wire power system 36 with a grounded center neutral point. Ex. 1234, ¶ [0002]. Fujimoto's system includes a DC ground fault detector (**orange**) with a current transformer 41 inserted in the positive (**green**) and negative (**purple**) DC conductors ("AC ground leak detector inserted in the positive and negative conductors between said DC source and said DC to AC converter" in claim 4). *Id.*, ¶¶ [0008], [0010], Fig. 1.



Ex. 1234, Fig. 1 (annotated)

Ex. 1234, Fig. 3, ¶¶ [0005], [0008], [0010]; Ex. 1202, ¶ 337.

DC current flow is normally balanced: current in the positive conductor (**green**) from the power source to the inverter equals the return current in the negative conductor (**purple**). Ex. 1231, ¶ [0005]; Ex. 1202, ¶ 338. If a ground fault resistance R_G (**red**) exists between the positive conductor and ground (claimed

"unwanted leakage impedance"), a difference in the positive and negative currents—*i.e.*, a "common current" I_G—is created with an AC component (I_{ac}) at twice the inverter AC output waveform frequency (claim 4's "imbalance current at the said second frequency" and claim 11's "common-mode current with said common-mode waveform at said characteristic repetition frequency"). Ex. 1234, Abstract, ¶¶ [0005]-[0007], [0010]-[0011], Fig. 4; Ex. 1202, ¶¶ 338, 350.

Fujimoto's detector isolates and amplifies (via band-pass filter 51 and amplifier 52) the AC component I_{ac} at two times the system frequency and compares it to a prescribed detection level 45 to indicate a fault (claim 4's "detection signal" and claim 11's "detecting"). Ex. 1234, ¶¶ Abstract, [0007], [0010]-[0011], Figs. 1-2; Ex. 1202, ¶¶ 339, 350.

A PHOSITA would have understood that I_{ac} was induced through R_G from a common-mode voltage generated by Fujimoto's (transformerless) inverter with the grounded center neutral point, and that Fujimoto's detector could easily be applied to each of the DC supplies of Mori/Mori-Tolbert's inverter, which similarly generates a common-mode voltage waveform on the DC inputs, for example, on the terminals of Mori's DC supply 33 (with respect to multiplex output terminal 62), and which may similarly be used with various DC sources having leakage due to ground faults. Ex. 1202, ¶¶ 340-346, 351; Ex. 1234, Fig. 3, Abstract, ¶¶ [0004],

[0008]; Ex. 1228, ¶¶ [0012]-[0021], [0029]; Ex. 1244, p. 37; *see* Section V.A.1.e, *supra*.

A PHOSITA would have been motivated to modify Mori/Mori-Tolbert's inverter to detect a leakage impedance at the input of Mori/Mori-Tolbert's H-bridges (*e.g.*, 23) and stop operation of the inverter as taught in Fujimoto to prevent hazards (*e.g.*, fire, component damage) and to comply with government safety standards, such as the 2008 National Electric Code. Ex. 1234, ¶¶ [0004]-[0005]; Ex. 1219, pp. 14-15; Ex. 1224, ¶¶ [0039], [0048], [0050]; Ex. 1202, ¶¶ 340-342.

Since each Mori/Mori-Tolbert H-bridge is similar to Fujimoto's inverter and both would produce similar common-mode voltages at DC inputs, such a modification would have been no more than applying a known technique (Fujimoto's ground fault detection) to improve a similar device (Mori/Mori-Tolbert's inverter generating a common-mode AC input voltage) in the same way (as Fujimoto's inverter generating a common-mode AC input voltage). Ex. 1202, ¶¶ 343-345.

A PHOSITA would have reasonably expected success in combining Mori/Mori-Tolbert and Fujimoto, yielding a predictable result of Mori/Mori-Tolbert's inverter with Fujimoto's detector to indicate a DC ground fault. *Id.*, ¶ 346. A PHOSITA would have understood that Fujimoto's band-pass filter could easily be adjusted to detect a ground fault with a frequency component such as the

common-mode frequency taught in Mori. *Id.*, ¶ 345. This would have been a routine matter of tuning Fujimoto's band-pass filter to the frequency of Mori/Mori-Tolbert's common-mode waveform, which was well within the level of ordinary skill in the art. *Id.*

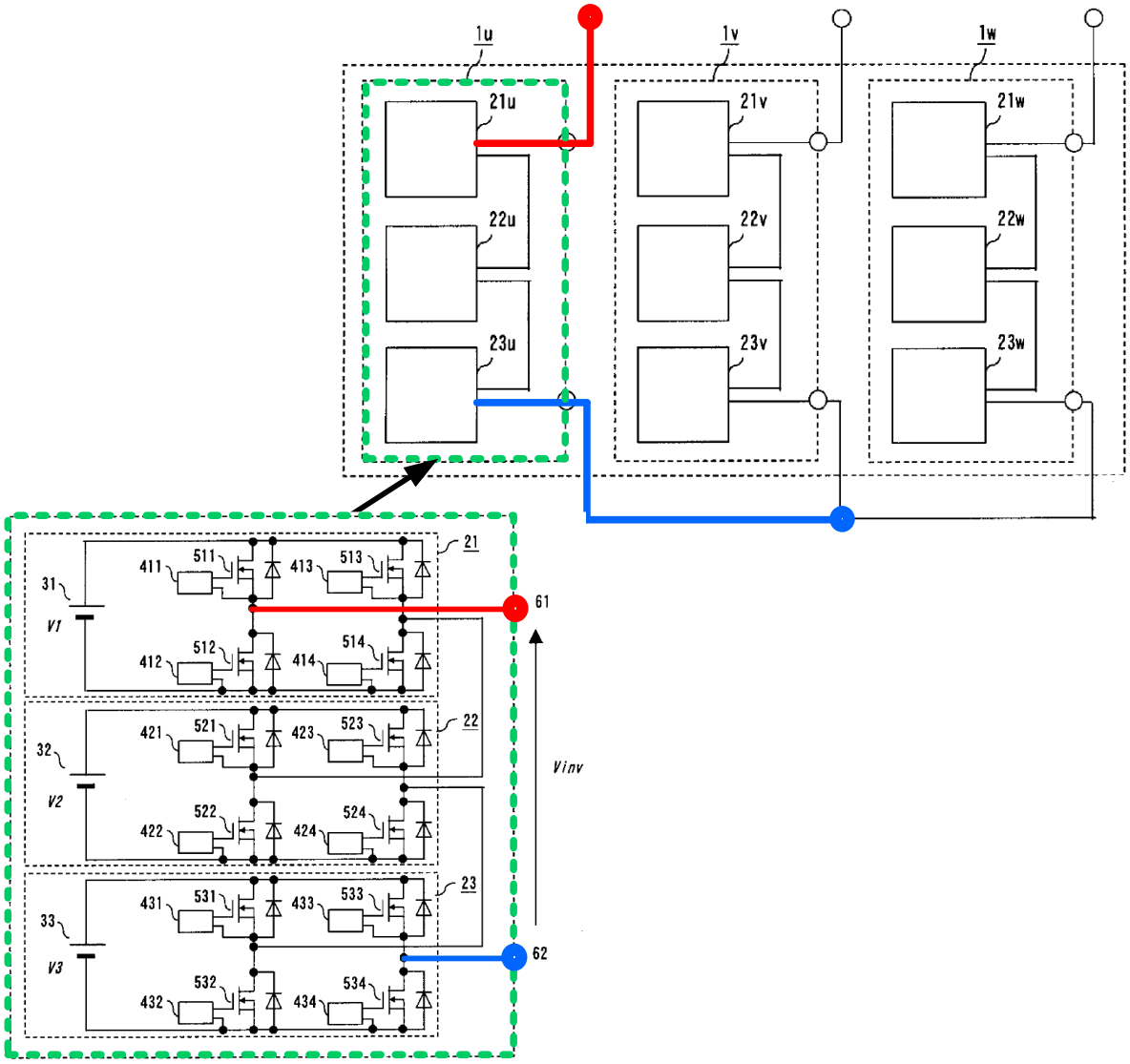
A PHOSITA would have recognized that Fujimoto's current transformer 41 (a well-known device having coils in which a primary current induces a proportional secondary current for measurement) is the same or an insubstantially different structure as the '822 patent's current transformer (toroid 800 and windings 801). *Id.*, ¶ 347; Ex. 1201, 31:65-32:20, 35:66-36:3, Fig. 18; Ex. 1234, ¶¶ [0005], [0008]; Ex. 1236, p. 5; Ex. 1242, p. 5; Ex. 1243, p. 5. Fujimoto's current transformer performs the same function (detecting a difference in the current flowing through the positive conductor and back through the negative conductor) in the same way (coupling to the positive and negative DC input lines) for the same result (outputting a ground fault signal). Ex. 1202, ¶ 347.

D. Grounds 8, 9: Mori/Mori-Tolbert in View of Bond Renders Claim 7 Obvious

1. Dependent Claim 7

A three-phase grid-interactive inverter operating according to claim 1 in which said set of AC output terminals comprises three terminals that deliver current at unique phases spaced relatively 0, 120 and 240 degrees apart through a watt-hour metering device to the three legs of a wye-connected 120/208-volt, three-phase, electric utility company service connection and said at least one ground, neutral or reference potential terminal is the neutral terminal at the center of the wye-connection.

Mori /Mori-Tolbert and Bond teach this claim. Ex. 1202, ¶¶ 352-362. Mori discloses that three of its single-phase multiplex inverters ("operating according to claim 1," *see* Section V.A.1, *supra*) may be connected together as a three-phase inverter, with the neutral terminals 62 connected together and the live AC output terminal 61 of each single-phase multiplex inverter providing one of the three phases:

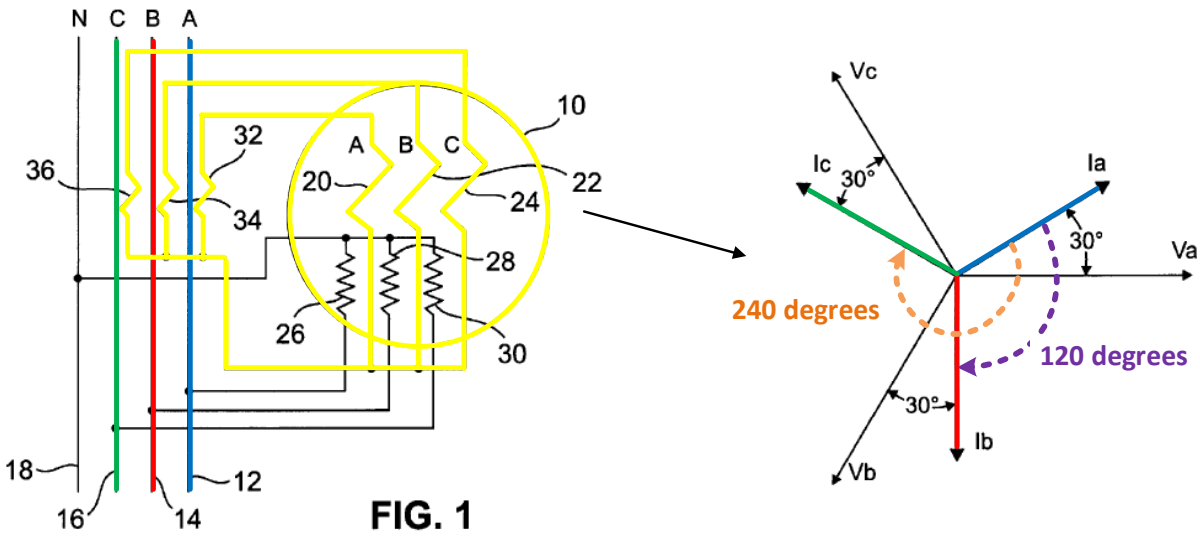


Ex. 1204, Figs. 1, 16 (annotated)

Ex. 1204, ¶¶ [0009], [0034]; Ex. 1202, ¶¶ 352-353.

Bond describes "a watt-hour metering device" 10 (**yellow**) for connecting customers to a utility grid with a four-wire wye service type connection with neutral center and with a 120-volt (line-to-neutral) (resulting in 208-volt (line-to-line)) output voltage (claimed "the three legs of a wye-connected 120/208-volt, three-phase, electric utility company service connection . . . neutral terminal at the center

of the wye-connection"). Ex. 1235, 1:10-22, 1:26-49, 2:55-58, 3:16-23, 3:41-49, 4:4-11, 4:27-58, 10:9-11, 12:32-43, Figs. 1, 1a; Ex. 1202, ¶¶ 356-357. Bond's power lines 12 (**blue**), 14 (**red**), and 16 (**green**) carry currents, between the customer and the grid, for three phases "approximately 120°" apart: Ia (**blue**), Ib (**red**), and Ic (**green**) for phases A, B, and C, respectively (claimed "current at unique phases spaced relatively 0, 120 and 240 degrees apart"):



Ex. 1235, Figs. 1 (left, annotated), 1a (right, annotated)

Ex. 1235, 3:41-49, 4:4-11, 10:9-11; Ex. 1202, ¶ 356.

It was well known to use inverters connected to DC power supplies for generation of AC power to be supplied to a utility grid (and thus be "grid interactive"), for example, when installed as part of a customer's photovoltaic system or an uninterruptable power supply in a home connected to the grid. Ex.

1244, p. 37 (disclosing fuel or solar cells connected a multi-level H-bridge inverter); Ex. 1205, Figs. 1-2, 1:10-46 (disclosing inverters used with rectifiers and/or batteries in an uninterruptable power supply); Ex. 1215, Fig. 1(c), pp. 3118-3120; Ex. 1219, pp. 14-19 (providing US requirements for photovoltaic systems including an inverter in a home); Ex. 1202, ¶ 359.

A PHOSITA would have been motivated to combine Mori/Mori-Tolbert's three-phase wye-connected inverter in such well-known systems for the generation of power, with Bond's 120/208 wye connected meter (by connecting Mori's three phases and neutral to Bond's three phases and neutral, respectively) for the reasons taught in Bond—monitoring energy usage by customers connected to the grid for billing, resource allocation planning, power factor tracking, and for error diagnostics—and because the 120/208V wye configuration was a "commonly used service type [that is] standardized and [] well known to those of ordinary skill in the art." Ex. 1235, 1:10-16, 1:27-40, 2:4-20, 3:16-23, 3:41-48, 4:4-11, 4:27-58, 9:15-19, 10:8-11, 14:7-9, Fig. 6 (4WY-120v); Ex. 1202, ¶¶ 358-359.

Such a modification would have been no more than combining prior art elements (Mori/Mori-Tolbert's three-phase inverter output in a grid connected system with Bond's watt-hour meter) according to known methods (measuring output current of three phases with a watt-hour meter) to yield predictable results (measuring the output of a standardized utility connection). Ex. 1202, ¶¶ 360-361.

A PHOSITA would have reasonably expected success in combining these elements as the combination merely entails connecting an inverter and a utility meter that is *standardized* and well within the level of ordinary skill in the art. Ex. 1235, 1:35-37; Ex. 1202, ¶ 362.

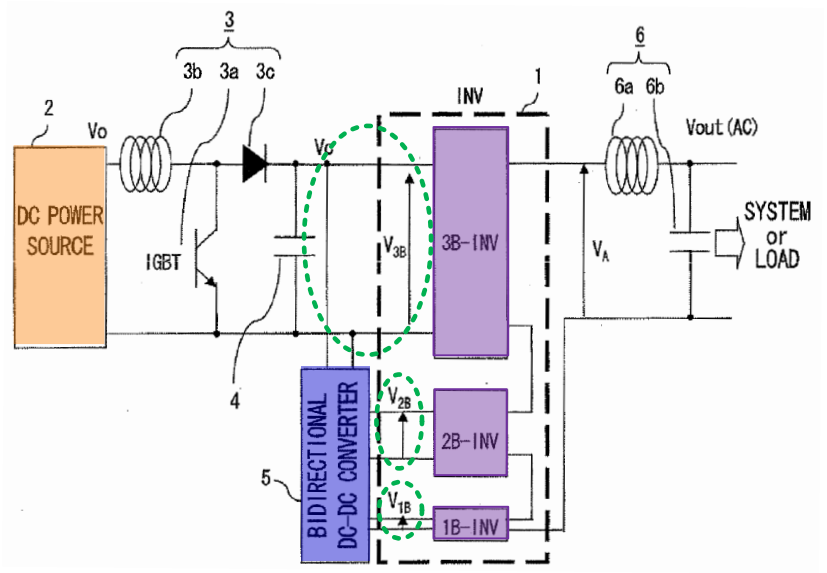
E. Grounds 10, 11: Mori/Mori-Tolbert in View of Iwata and Nishimura Renders Claims 5 and 13 Obvious

1. Dependent Claim 5

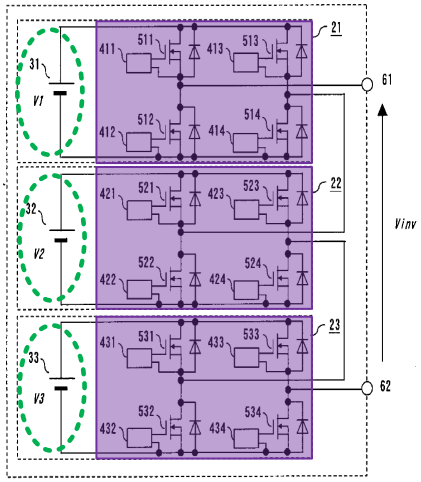
a. "The DC to AC conversion apparatus of claim 1 in which said DC to AC converter further comprises: A bidirectional DC-to-DC converter for converting the input voltage from said DC power source to a number of floating supplies of voltages equal to the input voltage divided or multiplied by successive powers of 3"

Mori and Mori-Tolbert further combined with Iwata and Nishimura disclose this element. Ex. 1202, ¶¶ 363-379. As discussed above for element [1D] (*see* Section V.A.1.c, *supra*), Mori discloses DC floating voltages V3, V2, and V1 that are 9V, 3V, and 1V, respectively.

Iwata discloses an inverter 1 (**purple**) substantially identical to Mori's inverter with the same floating supply voltages (**green**) having the same 9:3:1 ratio. Ex. 1202, ¶ 373; Ex. 1204, Fig. 1, ¶¶ [0011]-[0012], [0019]-[0020]; Ex. 1207, Figs. 1a, 1b, ¶¶ [0002]-[0003], [0046]-[0050], [0073].



Iwata (Ex. 1207)
Fig. 1a (annotated)



Mori (Ex. 1204),
Fig. 1 (annotated)

But instead of generating DC floating voltages from different DC power supplies as in Mori, Iwata's 9V DC supply voltage (V_{3B}) is generated directly from a DC power source (**orange**), and the 3V (V_{2B}) and 1V (V_{1B}) supply voltages are generated with a bidirectional DC-DC converter 5 (**blue**) connected to the DC power source (claimed "bidirectional DC-to-DC converter for converting the input voltage from said DC power source to a number of floating supplies of voltages equal to the input voltage divided [] by successive powers of 3"). Ex. 1202, ¶ 374; Ex. 1207, Figs. 1a, 1b, ¶¶ [0002]-[0003], [0046]-[0050], [0073].

A PHOSITA would have been motivated to modify Mori's inverter to generate the floating DC supply voltages from Iwata's solar battery/panel and bidirectional DC-DC converter to reduce pollution and electricity costs, and the combination of Iwata with Mori or Mori-Tolbert is nothing more than the simple

substitution of one known element (Mori's three-phase AC-DC converter) for another (Iwata's DC power solar battery/panel and DC-DC converter) to obtain predictable results (Mori's inverter powered from a solar battery/panel and DC-DC converter). Ex. 1202, ¶¶ 364-369, 375; Ex. 1207, ¶¶ [0002]-[0003].

A PHOSITA would have reasonably expected success since the combination merely entails implementing Mori's DC power supplies 31-33 with a DC power source and a bidirectional DC-to-DC converter, per Iwata. This swapping of interchangeable power supplies was well within the level of ordinary skill in the art. Ex. 1202, ¶ 376.

To the extent the "bidirectional DC-to-DC converter" is a means-plus-function term, Nishimura discloses an identical or insubstantially different structure to that in the '822 patent's Figure 2. Ex. 1202, ¶ 377. As shown below, Nishimura, in Figure 4 (top), depicts a bidirectional converter for a grid connected power supply, which includes center-tapped windings (**red**) connected to the positive terminal of the DC input or output (**blue**) and with ends connected to the drains of N-Type MOSFET pairs (**green**), like the '822 patent (bottom):

FIG.4

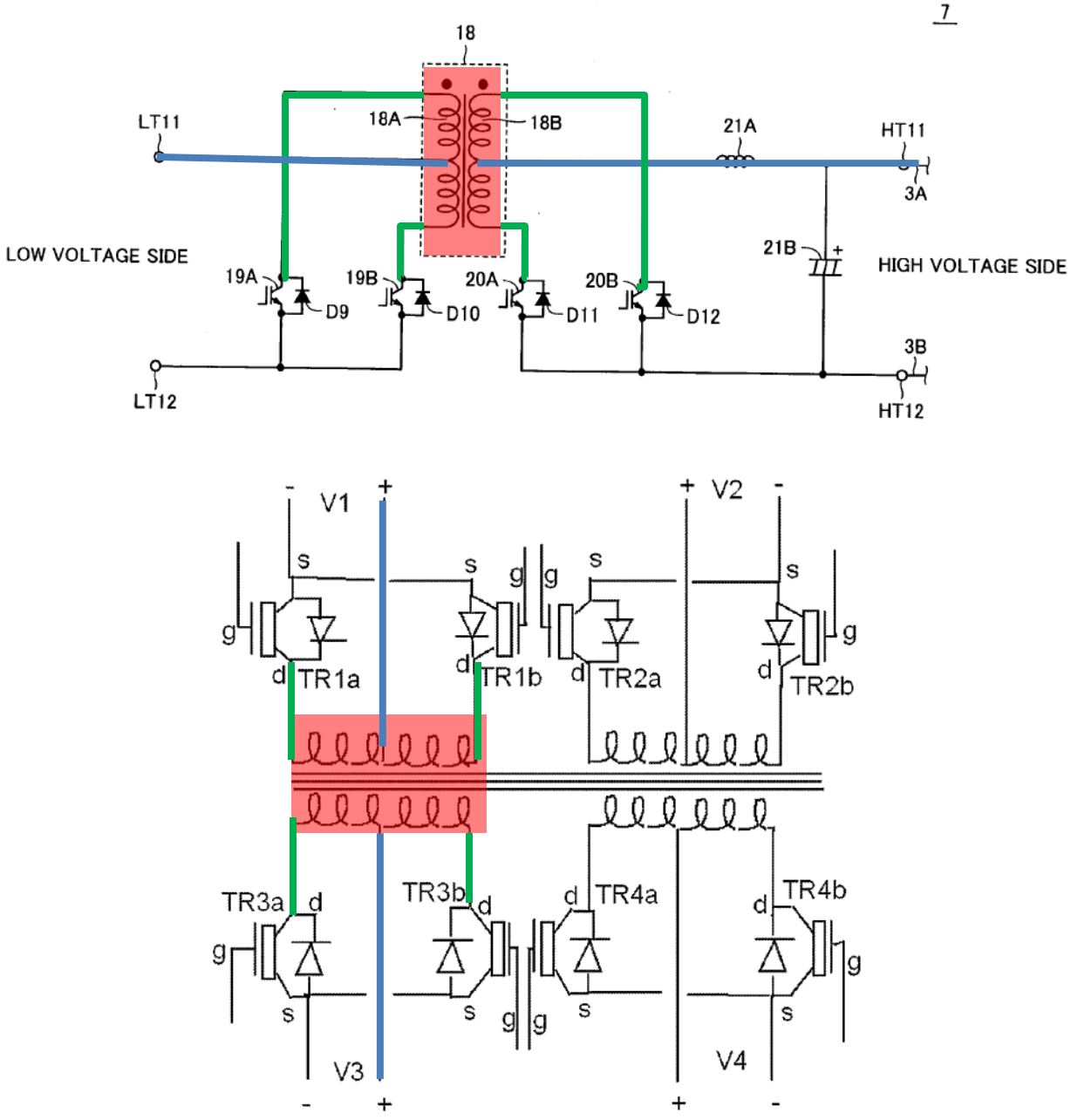


FIGURE 2: BIDIRECTIONAL DC-DC CONVERTER

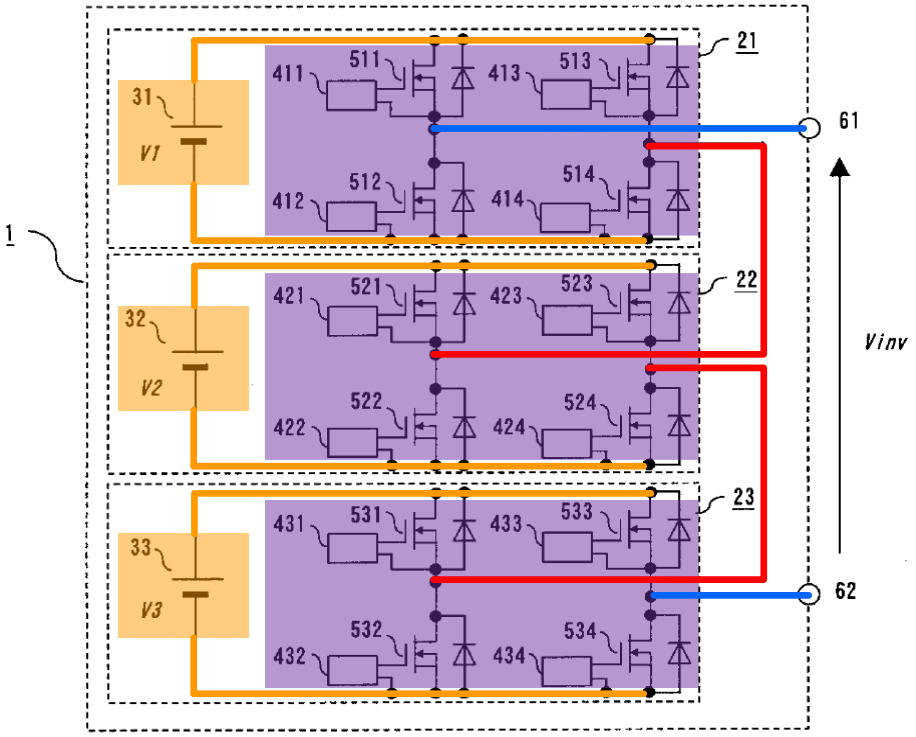
Ex. 1208, Fig. 4 (annotated, top); Ex. 1201, Fig. 2 (annotated, bottom)

Ex. 1201, 18:34-47; Ex. 1202, ¶ 377. Figure 2 of the '822 patent merely duplicates this structure (adding V2 and V4) to enable more than one voltage output (V2, V3, and V4) if the input is V1. Ex. 1202, ¶ 378.

A PHOSITA would have been motivated to use Nishimura's DC-to-DC converter with Mori and Iwata because: A) the split inductor coupling in this design requires only two transistors for each coil (*e.g*., as compared to a full bridge design) and requires less drive power supplies for powering the control signals of these transistors, thus reducing size, cost and weight; and B) the use of MOSFET transistors (*e.g.*, instead of using diodes as in Figures 2 and 5) in each port improves efficiency of the converter. Ex. 1208, ¶¶ [0098], [0108]-[0109]; Ex. 1202, ¶¶ 370, 379. Further, using Nishimura's DC-DC converter in this manner is merely a simple substitution of one known (Iwata's bidirectional DC-DC converter) with another known element (Nishimura's DC-DC converter) to obtain a predictable result. Ex. 1202, ¶¶ 370-371, 379. A PHOSITA would have reasonably expected success in using Nishimura's DC-to-DC converter as the bi-directional DC-DC converter in Mori and Iwata because it would have merely required swapping out one bi-directional DC-DC converter for another, which was well within the level of ordinary skill in the art. *Id*.

b. "a number of three-state electronic switches each in the form of an H-bridge, each with a pair of input terminals connected to one of the DC power source and said floating voltage supplies from said bidirectional DC to DC converter, and a pair of output terminals, the outputs terminals of said electronic H-bridge switches being directly connected in series and one end of the series connected output terminal pairs being connected to at least one of said set of AC output terminals"

Mori/Mori-Tolbert and Iwata teach this limitation. Ex. 1202, ¶¶ 380-382. Mori discloses three H-bridges (**purple**) that each output a positive, negative, or zero voltage (claimed "number of three-state electronic switches each in the form of an H-bridge"), each with "a pair of input terminals" (**orange** lines) connected to floating voltages 31-33, and each with a pair of output terminals that are "directly connected in series" (**red**) with one end connected to an "AC output terminal[]" (Vinv) (**blue**)**:**



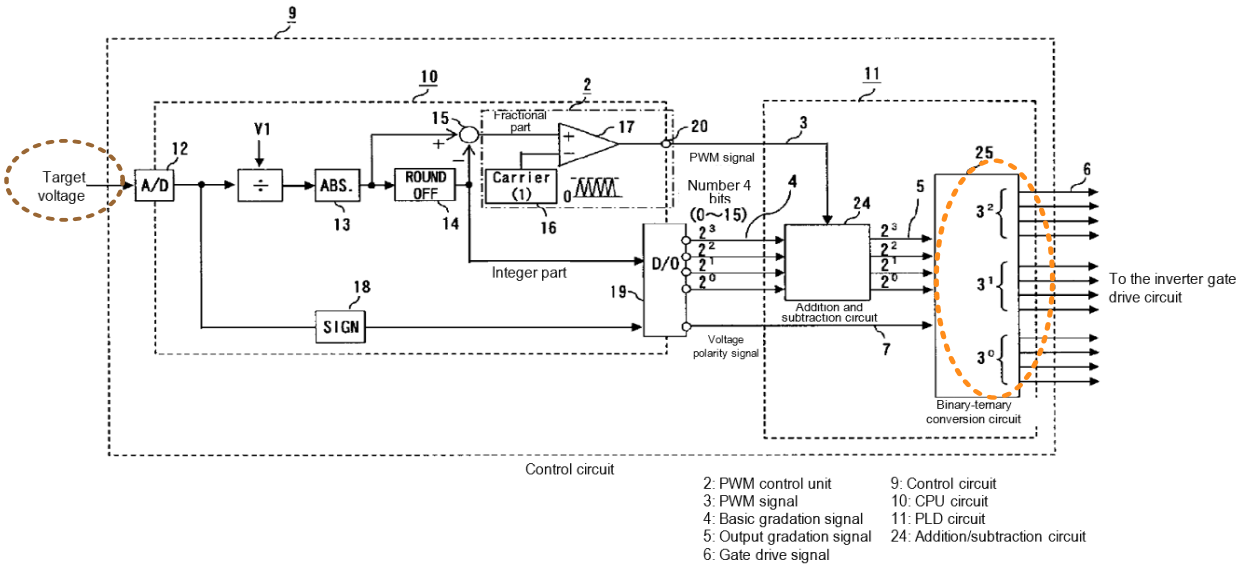
Ex. 1204, Fig. 1 (annotated)

Ex. 1202, ¶ 380; Ex. 1204, ¶¶ [0002]-[0012], [0015]-[0016], [0019]-[0021], [0034]; *see* Section V.A.1.c, *supra*.

As discussed above (Section V.E.1.a, *supra*), Iwata teaches generating the 9V supply (Mori's V3 and Iwata's V_{3B}) with a DC power source and generating the 3V (Mori's V2 and Iwata's V_{2B}) and 1V (Mori's V1 and Iwata's V_{1B}) with the bidirectional DC-DC converter 5 (claimed "each with a pair of input terminals connected to one of the DC power source and said floating voltage supplies from said bidirectional DC to DC converter"). Ex. 1202, ¶ 381; Ex. 1207, Abstract, Figs. 1a, 1b, ¶¶ [0002]-[0003], [0046]-[0050], [0073]. As discussed (*see* Section V.E.1.a, *supra*), a PHOSITA would have been motivated (and would have reasonably been expected in succeeding) to modify Mori's inverter to generate the floating DC supply voltages from Iwata's solar battery/panel and bidirectional DC-DC converter to reduce pollution and electricity costs, with the combination being nothing more than the simple substitution of one known element (Mori's DC power supplies) for another (Iwata's DC power source and DC-DC converter) to obtain predictable results (Mori's inverter powered from a DC source and DC-DC converter). Ex. 1202, ¶¶ 381-382; Ex. 1207, ¶¶ [0002]-[0003].

c. "a switch controller for controlling said three-state electronic switches according to a sampled numerical representation of the desired AC output waveform expressed in a ternary number base, each ternary digit of a numerical sample determining whether a respective switch is controlled to one of the three output states (a) first polarity state, (b) inverse polarity state and (c) pass-through state, wherein the pass through state allows current flow in the H-bridge output circuit without connecting the DC input voltage in series with the H-bridge output terminals, the first polarity state causes the [] DC input voltage to be connected in series with the H-bridge output terminals with a first polarity and the inverse polarity state causes the DC input voltage to be connected in series with the H-bridge output terminals with an opposite polarity to the first polarity state."

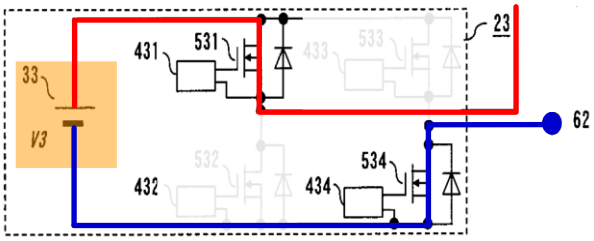
Mori and Mori-Tolbert disclose this element. Ex. 1202, ¶¶ 383-387. Mori discloses a control circuit 9 (claimed "switch controller"), which samples a target voltage (**brown**) (claimed "desired AC output waveform") and converts the target voltage into a number of gradation levels expressed as a ternary number having three ternary digits (3^0, 3^1, 3^2) (**orange**) (claimed "ternary number base"):



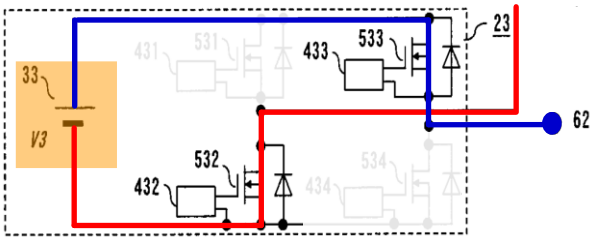
Ex. 1204, Fig. 4 (annotated)

Ex. 1204, ¶¶ [0015]-[0019]; Ex. 1202, ¶ 383.

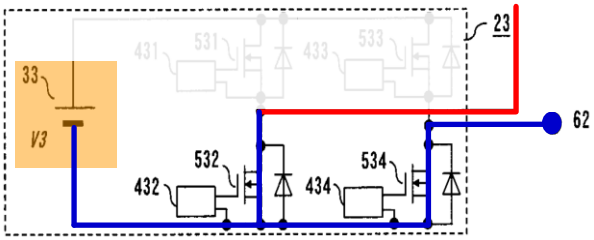
Each ternary digit 3^0, 3^1, 3^2 (along with polarity signal 7) controls Mori's H-bridges 21, 22, and 23, respectively, to output a positive, negative, or zero voltage, which as explained above (*see* Section V.A.1.e, *supra*) are generated by Mori's H-bridge (and alternatively Tolbert's H-bridge) in positive ("first polarity"), negative ("inverse polarity"), and either of two pass-through ("pass-through) states:



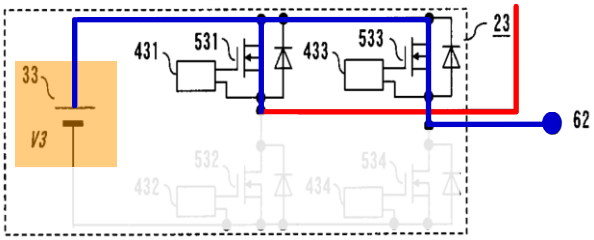
Positive Voltage (+3V)



Negative Voltage (-3V)



Pass-through Low (0V)



Pass-through High (0V)

Ex. 1202, ¶ 384; Ex. 1204, ¶¶ [0009]-[0011], [0019]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b (illustrating 3 output levels from four H-bridge states). The above illustrates that: A) in the pass-through states (outputting zero voltage), current flows **(**between **red** and **blue**) in the H-bridge without connecting the DC input voltage in series with the H-bridge output terminals; B) in the positive (first polarity) state, the DC input voltage is connected in series with the H-bridge output terminals; and C) in the negative (inverse polarity) state, the DC input voltage is connected in series with the H-bridge output terminals with an opposite polarity to the first polarity state. Ex. 1202, ¶ 385; Ex. 1204, ¶¶ [0009]-[0011], [0019]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38.

As discussed (*see* Section V.A.1.e, *supra*), to the extent PO argues that Mori fails to disclose the H-bridge states, a PHOSITA would have been motivated to use Tolbert's sequence of these states for Mori's H-bridges because such a combination would have been a simple substitution of one known element (Mori's H-bridge control timing) with another known element (Tolbert's H-bridge control timing) to obtain a predictable result (producing the same output waveform and the same input common-mode waveform), and because Tolbert's sequence causes all of the switching devices in the H-bridge to conduct with equal times, equalizing the stress on each device. Ex. 1202, ¶ 386; Ex. 1244, Fig. 2(b), pp. 37-38. A PHOSITA would have reasonably expected success in combining these elements as the combination merely requires applying simple logic to control known H-bridges, which was well within the level of ordinary skill in the art. Ex. 1202, ¶ 386.

The '822 patent describes a corresponding structure of the "switch controller as including "a microcontroller" with "memory." Ex. 1201, 12:26-51, 24:8-12; *see* Section IV.B.2, *supra*. Mori's control circuit performs claim 5's function and is similarly described as a "CPU (Central Processing Unit) 10 and a PLD (Programmable Logic Device) circuit 11" and a "microcomputer or a microcomputer-based controller such as a DSP (Digital Signal Processor)." Ex. 1202, ¶ 387; Ex. 1204, ¶¶ [0006]-[0008], [0015], Figs. 4, 9, 10, 13, 15. A PHOSITA would have understood that CPUs and microcomputers execute software stored in

memory. Ex. 1202, ¶ 387. Both controllers are insubstantially different from and perform the same functions (as in claim 5) in the same way (controlling H-bridges using drive signals) for the same result (connecting positive and negative DC input terminals to the instantaneously most positive and negative of the AC output terminals and neutral). *Id*.

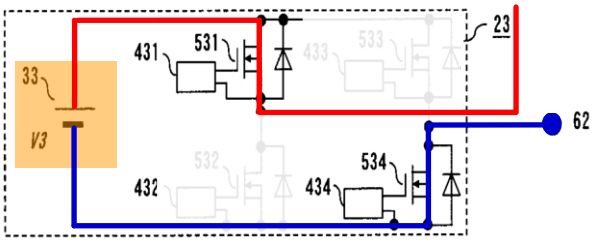
2. Dependent Claim 13

> **The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive and negative lines comprises the steps of:**
>
> **using a bidirectional DC-to-DC converter to form, along with the DC source voltage, a set of floating DC supplies of voltages having voltage ratios of successive powers of 3;**
>
> **selecting one or more of said floating DC supplies to be directly connected in series to an AC output, with or without a polarity reversal, such that the algebraic sum of the selected voltages and polarities equals the desired instantaneous voltage of the AC output.**

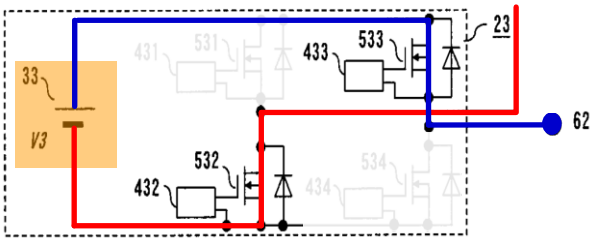
As explained, Mori and Mori-Tolbert teach "deriving instantaneous voltages from the direct current source positive and negative lines." *See* Section V.A.2.c, *supra*. And as explained for claim 5, Mori and Mori-Tolbert each further combined with Iwata and Nishimura teach a bidirectional DC-to-DC converter for converting the input voltage from a DC power source to two floating supplies of voltages equal to the input voltage divided or multiplied by "successive powers of 3." *See* Section V.E.1.a, *supra*. For the same reasons, Mori-Iwata-Nishimura and Mori-Tolbert-

Iwata-Nishimura also teach "using a bidirectional DC-to-DC converter to form, along with the DC source voltage, a set of floating DC supplies of voltages having voltage ratios of successive powers of 3." Ex. 1202, ¶¶ 388-391; Ex. 1207, Abstract, Figs. 1a, 1b, ¶¶ [0002]-[0003], [0046]-[0050], [0073]. To the extent "bidirectional DC-to-DC converter" in claim 13 is a means-plus-function term, Iwata-Nishimura teaches the identical or equivalent claim 13 structure for the same reasons discussed above for claim 5, since the structure disclosed in '822 patent for both of these claims is the same (Figure 2). *See* Section V.E.1.a, *supra*; Ex. 1202, ¶ 389.

As explained above (*see* Sections V.A.1.e, V.E.1.c, *supra*), these voltages are generated by controlling the H-bridge into positive ("first polarity") and negative ("inverse polarity") states, which directly connect the DC supply in series with the AC output with and without a polarity reversal:



Positive Voltage (+3V)



Negative Voltage (-3V)

Ex. 1202, ¶ 390; Ex. 1204, ¶¶ [0009]-[0011]; Ex. 1212, pp. 215-217; Ex. 1217, p. 311, Fig. 4; Ex. 1244, pp. 37-38, Fig. 2b (illustrating 3 output levels from the four h-bridge states).

Mori discloses that control circuit 9 samples a target voltage, converts the target voltage into one of a number of gradation levels (claimed "desired instantaneous voltage of the AC output"), and controls the H-bridges, into positive, negative, and pass-through states to output the gradation level as the series sum of the H-bridge outputs (claimed "such that algebraic sum of the selected voltages and polarities equals the desired instantaneous voltage of the AC output"). Ex. 1202, ¶ 391; Ex. 1204, ¶¶ [0007], [0012], [0015]-[0019], claim 1.

F. CONCLUSION

For the foregoing reasons, *inter partes* review of claims 1-13 and 20 of the '822 patent should be instituted and these claims should be canceled.

Dated: October 11, 2021

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CERTIFICATION UNDER 37 CFR § 42.24(D)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,961, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,786 words as counted by the Word Count feature of Microsoft Word and 175 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of the Petition for *Inter Partes* Review in connection with U.S. Patent No. 8,937,822 and supporting evidence to be served via FedEx. Priority Overnight on October 11, 2021, on the following:

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An electronic courtesy copy is concurrently being e-mailed to the following:

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CLAIM LISTING APPENDIX

U.S. Pat. No. 8,937,822

Designation	Claim Language
Claim 1	
[1A]	1. DC to AC conversion apparatus for converting power from a DC source to produce an power output waveform at a first repetition frequency, comprising
[1B]	a set of at least one live AC output terminals,
[1C]	at least one output terminal designated as a ground, neutral or reference potential terminal;
[1D]	a floating DC power source having a positive and a negative terminal connected respectively to the positive and negative DC input terminals of a DC to AC converter
[1E]	wherein the DC to AC converter causes: (1) an AC output waveform at said first repetition frequency and having a voltage relative to one of said at least one ground, neutral or reference potential terminals to appear with a unique phase at each of a number N at least equal to one of said set of live AC output terminals, and
[1F]	[wherein the DC to AC converter causes:] (2) a common-mode voltage waveform at a second repetition frequency to appear relative to one of said at least one ground, neutral or reference potential terminals and in the same phase on both of said positive and negative terminals of said DC power source, wherein the second repetition frequency is a multiple equal to the same said number N of said first repetition frequency.
Claim 2	
2	2. The apparatus of claim 1 wherein said DC to AC converter further comprises: A first electronic switch controlled by a switching controller to connect said positive DC input terminal to the instantaneously most positive of said set of AC output terminals and said at least one ground, neutral or reference potential terminal alternating with connecting said negative DC input terminal to the instantaneously most negative of said set of AC output terminals and said at least one ground, neutral or reference potential terminal.
Claim 3	

Designation	Claim Language
3	3. The DC to AC conversion apparatus of claim 1 wherein said second repetition frequency is a multiple equal to the same said number N of said first repetition frequency and said number N is equal to 1, 2 or 3.
Claim 4	
4	4. The apparatus of claim 1 further comprising an AC ground leak detector inserted in the positive and negative conductors between said DC source and said DC to AC converter, the AC ground leak detector being adapted to detect an imbalance current at said second frequency and to thereby provide a detection signal indicative of an unwanted leakage impedance from a DC conductor to ground.
Claim 5	
[5A]	5. The DC to AC conversion apparatus of claim 1 in which said DC to AC converter further comprises: a bidirectional DC-to-DC converter for converting the input voltage from said DC power source to a number of floating supplies of voltages equal to the input voltage divided or multiplied by successive powers of 3;
[5B]	A number of three-state electronic switches each in the form of an H-bridge, each with a pair of input terminals connected to one of the DC power source and said floating voltage supplies from said bidirectional DC to DC converter, and a pair of output terminals, the outputs terminals of said electronic H-bridge switches being directly connected in series and one end of the series connected output terminal pairs being connected to at least one of said set of AC output terminals;
[5C]	A switch controller for controlling said three-state electronic switches according to a sampled numerical representation of the desired AC output waveform expressed in a ternary number base, each ternary digit of a numerical sample determining whether a respective switch is controlled to one of the three output states (a) first polarity state, (b) inverse polarity state and (c) pass-through state, wherein the pass-through state allows current flow in the H-bridge output circuit without connecting the DC input voltage in series with the H-bridge output terminals, the first polarity state causes the the DC input voltage to be connected in series with the H-bridge

Designation	Claim Language
	output terminals with a first polarity and the inverse polarity state causes the DC input voltage to be connected in series with the H-bridge output terminals with an opposite polarity to the first polarity state.
Claim 6	
[6A]	6. The DC to AC conversion apparatus of claim 1, further comprising a common-mode filter connected between said DC to AC converter DC input terminals and said positive and negative terminals of said DC source, the common-mode filter being configured both
[6B]	to prevent high frequency components of the DC to AC converter internal waveforms being exported to said DC source and
[6C]	to minimize overshoot of said common-mode waveform in order to minimize peak voltages on said positive and negative terminals.
Claim 7	
7	7. A three-phase grid-interactive inverter operating according to claim 1 in which said set of AC output terminals comprises three terminals that deliver current at unique phases spaced relatively 0, 120 and 240 degrees apart through a watt-hour metering device to the three legs of a wye-connected 120/208-volt, three-phase, electric utility company service connection and said at least one ground, neutral or reference potential terminal is the neutral terminal at the center of the wye-connection.
Claim 8	
[8A]	8. A method of converting power from a direct current source with improved efficiency to provide AC output power at a standard voltage and frequency and to a number of output terminals corresponding to the number of phases required, comprising
[8B]	Configuring said direct current source to be floating;
[8C]	connecting the negative line from said direct current source to a first output terminal required to be instantaneously negative relative to all other output terminals while deriving from the direct current source positive voltage line the instantaneous voltages required to be output from the other output terminals

Designation	Claim Language
	relative to said first terminal, in a rotating sequence with connecting the positive line from said direct current source to a next-in-sequence output terminal required to be instantaneously positive relative to all other output terminals while deriving from the negative line of the direct current source the instantaneous voltages relative to said next-in-sequence terminal required to be output from the other terminals;
[8D]	selecting the timing of said rotating sequence such that a common mode waveform with a characteristic repetition frequency appears in phase on both the direct current source positive and negative lines.
Claim 9	
9	9. The method of claim 8 in which said characteristic frequency is a multiple of 1, 2 or 3 times the AC output power frequency.
Claim 10	
10	10. The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive line or negative line comprises using one of (a) a delta-sigma approximator having a high switching frequency; (b) a pulse-width modulator; or (c) approximations to said instantaneous voltages based on a finite number of digits in a ternary number system.
Claim 11	
11	11. The method of claim 8 in which an unwanted leakage impedance to ground from a line of either polarity of said direct current source is detected by detecting a common-mode current with said common mode waveform at said characteristic repetition frequency.
Claim 12	
12	12. The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive line or negative line comprises expressing a desired voltage using a finite number of digits (T(n), T(n-1), T(n-2) . . . T3,T2,T1) in a ternary number system such that the instantaneously desired voltage is equal to $3^{m}[T(n)+T(n-1)/3+T(n-1)/9+. . . T1/3^{(n-1)}$ or

Designation	Claim Language
	$3T(n)+T(n-1)+T(n-1)/3+...T1/3^{(n-)}$] times the voltage from said direct current source, where the power m may be zero.
Claim 13	
[13A]	13. The method of claim 8 in which said step of deriving instantaneous voltages from the direct current source positive and negative lines comprises the steps of:
[13B]	using a bidirectional DC-to-DC converter to form, along with the DC source voltage, a set of floating DC supplies of voltages having voltage ratios of successive powers of 3;
[13C]	selecting one or more of said floating DC supplies to be directly connected in series to an AC output, with or without a polarity reversal, such that the algebraic sum of the selected voltages and polarities equals the desired instantaneous voltage of the AC output.
Claim 14	
[14A]	14. In a solar energy installation comprising a photovoltaic solar array and a DC to AC converter having a DC input with positive and negative conductors routed in parallel with an array grounding conductor and an AC output having an output waveform with an output repetition frequency, a method of detecting a ground leak in the DC wiring to the solar array, comprising:
[14B]	creating a common-mode AC probe signal waveform from said DC to AC converter at a characteristic repetition frequency that is in phase on both said DC positive and negative input conductors;
[14C]	passing said positive and negative conductors from the array through a detector adapted to detect an unusual current with said common mode waveform at said characteristic repetition frequency and upon detection of said unusual current providing an indication of the presence of an unwanted ground leak.
Claim 15	
15	15. The method of claim 14 in which the characteristic repetition frequency of said probe signal waveform is 1, 2 or 3 times the AC output repetition frequency of said DC to AC converter.
Claim 16	

Designation	Claim Language
16	16. The method of claim 15, further comprising a storage battery charged by said solar array, in which said probe signal and unusual current detector also detect unwanted ground leaks from the DC conductors leading to and from said battery.
Claim 17	
17	17. The method of claim 14 in which said common-mode AC probe signal waveform corresponds to the changing value of a selected digit within a multi-digit number sequence representing said AC output waveform.
Claim 18	
18	18. The method of claim 14 in which said detection of an unusual current comprises measuring an output signal having said common mode waveform with one or more current transformers encircling either said positive and negative conductors only or encircling said positive and negative conductors and said array grounding conductor.
Claim 19	
19	19. The method of claim 14 in which said detection of an unusual current comprises correlating said common mode waveform with the output signal from one or more current transformers encircling either said positive and negative conductors only or encircling said positive and negative conductors and said array grounding conductor.
Claim 20	
[20A]	20. The method of claim 8 in which connecting the positive line of said DC source to the instantaneously most positive of all output terminals alternating in a rotating sequence with connecting the negative line of said DC source to the most positive of all output terminals comprises connecting the DC source terminal to the selected output terminal through a common mode filter in order
[20B]	to prevent high frequency components of said common-mode waveform being exported to said DC source and
[20C]	to minimize overshoot of said common-mode waveform in order to minimize peak voltages on said positive and negative terminals.