UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SOLAREDGE TECHNOLOGIES LTD.,
Petitioner,

v.

KOOLBRIDGE SOLAR, INC.,
Patent Owner.

Patent No. 10,784,710
Filing Date: August 14, 2017
Issue Date: September 22, 2020
Title: TRANSFORMERLESS DC TO AC CONVERTER

Inter Partes Review No.: IPR2022-00013

PETITION 1 of 3 FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq*.

TABLE OF CONTENTS

EXHIBITS

Ex. 1001:	U.S. Patent No. 10,784,710 ("the '710 patent")
Ex. 1002:	Declaration of R. Jacob Baker, Ph.D., P.E.
Ex. 1003:	Certified Prosecution History for the '710 patent
Ex. 1004:	U.S. Patent Application Publication No. 2008/0192519 ("Iwata")
Ex. 1005:	Japanese Patent Application Publication No. 2006-238630 ("Mori '630")
Ex. 1006:	Certified translation of Japanese Patent Application Publication No. 2006-238630 ("Mori '630")
Ex. 1007:	Certified translation of PCT Publication No. WO 2010/082265 ("Mori '265")
Ex. 1008:	U.S. Patent No. 5,400,237 ("Flanagan")
Ex. 1009:	U.S. Patent No. 7,088,601 ("Tracy")
Ex. 1010:	Electric Current Abroad, 1998 Edition
Ex. 1011:	U.S. Patent No. 6,750,391 ("Bower")
Ex. 1012:	K. H. Ahmed, S. J. Finney and B. W. Williams, *Passive Filter Design for Three-Phase Inverter Interfacing in Distributed Generation, Compatibility in Power Electronics*, CPE 2007, IEEE, pp. 1-9, 2007 ("Ahmed")
Ex. 1013:	Certified translation of PCT Publication No. WO 2010/055713 ("Koyama")
Ex. 1014:	U.S. Patent Application Publication No. 2009/0086520 ("Nishimura")
Ex. 1015:	U.S. Patent No. 8,576,591 ("Phadke")
Ex. 1016:	PCT Publication No. WO 2010/082265 ("Mori '265")
Ex. 1017:	PCT Publication No. WO 2010/055713 ("Koyama")

Ex. 1018:	Mark W. Earley Ed., *National Electrical Code® Handbook*, Eleventh Edition, 2008
Ex. 1019:	U.S. Patent No. 5,285,372 ("Huynh")
Ex. 1020:	U.S. Patent Application Publication No. 2005/0275368 ("Sippola")
Ex. 1021:	Keith H. Billings, *Switchmode Power Supply Handbook*, McGraw Hill, 1989
Ex. 1022:	Marty Brown, *Power Supply Cookbook*, Butterworth-Heinemann, 1994
Ex. 1023:	Certified Prosecution History for the U.S. Patent No. 8,937,822
Ex. 1024:	Certified Prosecution History for the U.S. Patent No. 9,735,703
Ex. 1025:	Japanese Patent Application Publication No. 2004-7941 ("Suzuki")
Ex. 1026:	Certified translation of Japanese Patent Application Publication No. 2004-7941 ("Suzuki")
Ex. 1027:	Reserved
Ex. 1028:	Reserved
Ex. 1029:	Reserved
Ex. 1030:	Reserved
Ex. 1031:	L. M. Tolbert, F. Z. Peng and T. G. Habetler, *Multilevel Converters for Large Electric Drives*, IEEE Transactions on Industry Applications, Vol. 35, No. 1, pp. 36-44, 1999 ("Tolbert")
Ex. 1032:	Reserved
Ex. 1033:	Reserved
Ex. 1034:	Reserved

Ex. 1035:	Certified translation of Heribert Schmidt, Bruno Burger, & Klaus Kiefer. Wechselwirkungen zwischen Solarmodulen und Wechselrichtern. English translation: Interaction between Solar Modules and DC/AC Inverters, 2007
Ex. 1036:	U.S. Patent No. 6,112,158 (“Bond”)
Ex. 1037:	Patel, H., Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I-Harmonic Elimination, IEEE Trans. on Industry Applications, Vol. 1A-9, no. 3 (May/June 1973) (“Patel”)
Ex. 1038:	U.S. Patent No. 7,046,534 (Schmidt)
Ex. 1039:	Declaration of Dr. James L. Mullins

SolarEdge Technologies Ltd ("Petitioner") petitions for *inter partes* review and cancellation of claims 1-17 of U.S. Patent No. 10,784,710 ("the '710 patent") (Ex. 1001).

I. MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1)&(2): Real Parties in Interest & Related Matters

The real party-in-interest is Petitioner SolarEdge Technologies Ltd. No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

The '710 Patent has been asserted against SolarEdge in the District of Delaware in *Koolbridge Solar, Inc. v. SolarEdge Technologies, Inc.*, No. 1:20-cv-01374-MN (D. Del.). The earliest date of service on SolarEdge was October 12, 2020. The Patent Owner, after having been notified of Petitioner's intent to file IPRs against the '710 Patent, voluntarily dismissed its lawsuit without prejudice.

The references relied upon herein were not cited during prosecution. No arguments presented in this Petition were raised during prosecution of the '710 patent.

B. 37 C.F.R. § 42.8(b)(3)&(4): Lead & Back-Up Counsel, and Service Information

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

Lead Counsel Frederic M. Meeker (Reg. No. 35,282) fmeeker@bannerwitcoff.com **First Back-Up Counsel** John R. Hutchins (Reg. No. 43,686) jhutchins@bannerwitcoff.com **Additional Back-Up Counsel** Michael Cuviello (Reg. No. 59,255) mcuviello@bannerwitcoff.com Banner & Witcoff, Ltd., 1100 13th Street, NW, Suite 1200 Washington, DC 20005 Tel: 202-824-3000 Fax: 202-824-3001	**Additional Back-Up Counsel** Paul Qualey (Reg. No. 45,027) pqualey@bannerwitcoff.com

Please address all correspondence to counsel at this address shown above. Petitioner consents to electronic service by email at the following address and the above emails: SolarEdgeIPRService@bannerwitcoff.com.

II. COMPLIANCE WITH THE REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Payment of Fees

The undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

B. Grounds for Standing

Petitioner certifies that the ’710 patent is available for review and that Petitioner is not barred or estopped from requesting review challenging claims 1-17.

III. SUMMARY OF ARGUMENT

U.S. Patent No. 10,784,710 (“the ’710 patent”) describes a well-known inverter, a device that converts “direct-current” (DC) electrical power (a type of power received from a battery and/or solar panel) to “alternating-current” (AC) electrical power (a type of power used in a home). The type of inverter claimed uses multiple DC supply voltages as inputs and sums these voltages together in different combinations over a time sequence to approximate a desired AC sinusoid wave. The inverter does this by connecting the DC supply voltages to the inputs of a plurality of “reversing switches” (also called “H-bridges”). Each switch is controlled so that it outputs either: (1) its DC supply voltage, (2) its DC supply voltage with negative polarity, or (3) zero volts. This is called “ternary” control, since the switches are controlled to be placed into one of three states: the +1, -1, or 0 state. The outputs of the switches are connected in series, and via control of the switch states their sum output voltage gradually steps up and down to generate a sequence of voltages approximating the sine wave.

At the time the ’710 patent was first filed, such inverters and the concepts behind their design and implementation were well-known in the art. Ex. 1002, ¶¶

61-106. Iwata (U.S. Patent Application Publication No. 2008/0192519, Ex. 1004), which is relied upon in this petition, is just one example of prior art disclosing the structure of the '710 patent. The dependent claims challenged herein add only obvious features that were also in the prior art and are taught in Iwata and additional secondary references relied on herein.

Accordingly, claims 1-17 of the '710 patent are unpatentable and should be cancelled.

IV. OVERVIEW OF THE '710 PATENT

A. Brief Description

Figure 1 of the '710 patent illustrates a top-level block diagram of the claimed inverter.

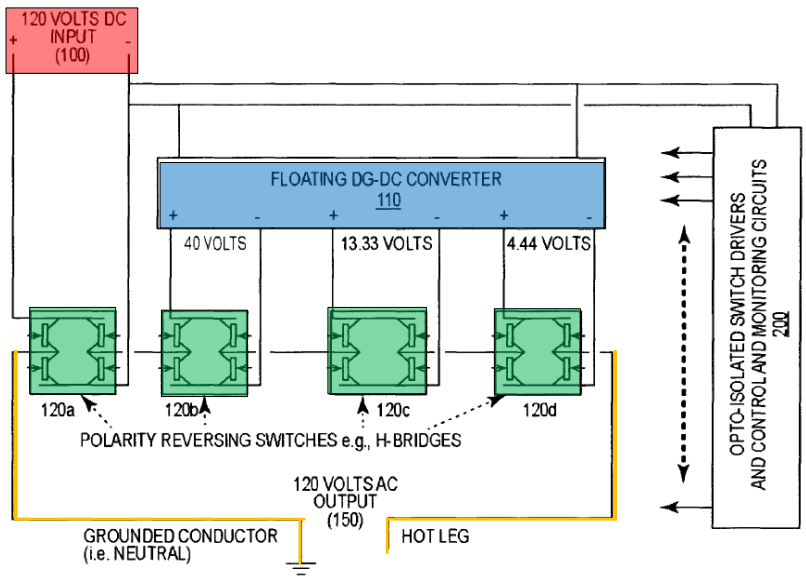


FIG. 1

Ex. 1001, Fig. 1 (annotated)

As shown above, the inverter has a 120V DC input (**red**) and a 120V AC output (**yellow**). Ex. 1001, 1:18-23, 2:41-43, 4:11-29, 5:41-52, 6:65-7:7, 7:57-65, 8:18-20; Ex. 1002 ¶ 93. This output is identified in the patent as being "transformerless," to distinguish it from inverters that couple their switches to the AC output using electrical transformer(s). Ex. 1003, pp. 294-296. The inverter includes a bidirectional DC-DC converter (**blue**) that converts the DC input voltage to three additional DC voltages—40V, 13.33V, and 4.44V. Ex. 1001, 3:61-4:10, 6:65-7:7, 15:12-19, 16:30-32, 19:36-50; Ex. 1002 ¶ 94. The 120V, 40V, 13.33V, and 4.44V DC voltages are connected to inputs of four "polarity reversing switches" (H-bridges) 120a, 120b, 120c, and 120d (**green**). Ex. 1001, Abstract, 3:61-4:10, 5:41-52, 6:65-7:7, 7:31-42, 10:16-23, 15:17-19, 19:36-38, Fig. 2. Each switch can be controlled based on a ternary control signal to apply a multiplier of +1, -1, or 0 to the input voltage. Ex. 1001, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 6:65-7:7, 7:23-28, 8:33-54; Ex. 1002 ¶¶ 95-96. A control value of +1 causes the DC supply at the switch input to be connected with the switch output resulting in the DC supply voltage being output from the switch with a positive polarity. A control value of -1 causes the DC supply at the switch input to be connected in reverse polarity to the switch output resulting in the DC supply voltage being output from the switch with a negative polarity. A control signal of 0 causes the DC supply to be bypassed, resulting in 0 voltage being output from the switch. *Id.*

The outputs of the switches are connected in series, thus generating a sum voltage (**yellow**) of the positive, negative, and bypassed supply voltages, depending on the state of the ternary control signals to each of the switches. Ex. 1001, Abstract, 1:18-23, 2:41-43, 3:61-4:29, 5:41-52, 6:65-7:7, 7:31-42, 7:57-65, 8:18-20, 10:16-23, 15:17-19, 19:36-38, Fig. 2; Ex. 1002 ¶ 97. For example, for ternary valued (+1, -1, 0) signals T4, T3, T2, and T1 controlling switches 120a, 120b, 120c, and 120d, respectively, the inverter sum output voltage would be (120*T4)+(40*T3)+(13.33*T2)+(4.44*T1) volts. Ex. 1001, 7:23-65. If all switches output their associated positive voltage (T4, T3, T2, and T1 all equal +1), the output voltage would be 120+40+13.33+4.44=177.77 volts, but if the 4.44 volt switch changes to output 0 volts (T1=0), the summed output voltage would become 120+40+13.33=173.33 volts. Ex. 1001, 7:65-8:5; Ex. 1002 ¶¶ 98-100.

By controlling the switch states in a certain sequence, a sinusoidal waveform is produced at the AC output, as seen below in Fig. 12. Ex. 1001, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 7:23-36, 7:60-8:7, 9:26-10:40.

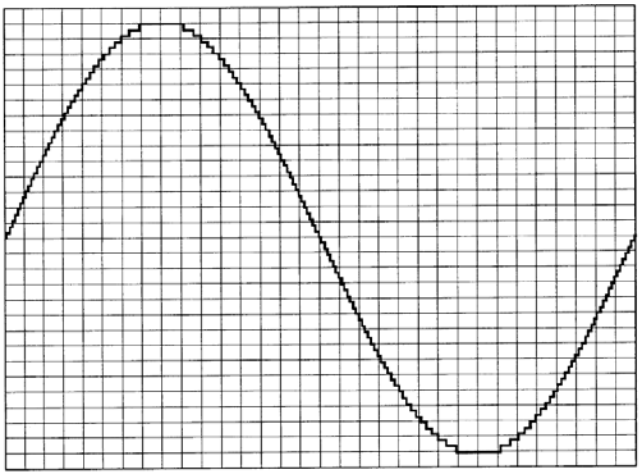


FIG. 12

Ex. 1001, Fig. 12

B. Prosecution History

The application that led to the ’710 patent was filed August 14, 2017. Ex. 1002 ¶ 107. Following rejection of certain claims as being anticipated by U.S. Patent No. 4,180,853 to Scorso (Ex. 1003, p. 188), PO argued that Scorso lacked the required ternary control of the switches. *Id.*, 229-232. The Examiner then rejected the claims over Scorso in view of U.S. Patent No. 5,373,433 to Thomas, which taught ternary control of H-bridge switches in an inverter. *Id.*, 261-268. In response, PO amended the claims to require a “transformerless” output and that the outputs of the plurality of switches are “directly” connected in series to output a sum voltage that approximates the desired waveform. *Id.*, 286. PO argued that the outputs of the H-bridge switches in Thomas were passed across transformers, before the outputs were summed to approximate the desired waveform. *Id.*, 294-296. PO did not dispute that the ternary control was taught in the art. *Id.*

The Examiner allowed the claims, referencing the lack in the prior art of the output of ternary-controlled switches directly connected in series to output a voltage approximating the desired waveform. *Id.*, 312-313; Ex. 1002 ¶¶ 107-112.

C. Earliest Priority Date for the Claims

The earliest possible priority date for the '710 patent claims is the filing date of U.S. Patent Application No. 13/103,070, May 8, 2011. Ex. 1001; Ex. 1002, ¶ 116.

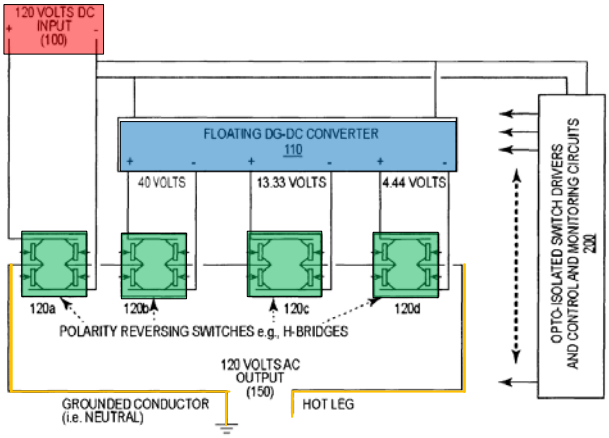
V. OVERVIEW OF PRIOR ART

A. Iwata

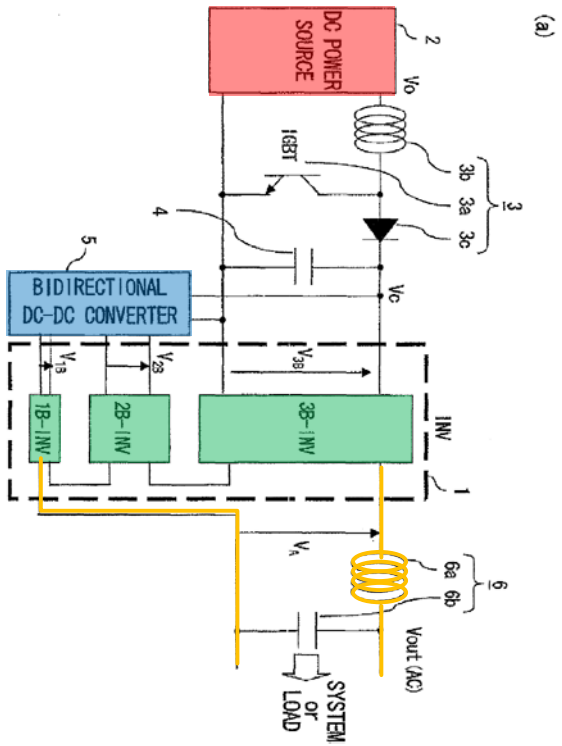
Iwata (Ex. 1004) is a U.S. Patent Application Publication published on August 14, 2008, making it prior art under 35 U.S.C. § 102(b).[1] Ex. 1002, ¶ 122.

As shown below, Iwata discloses an inverter similar to that in the '710 patent. *Compare* Ex. 1001, Fig. 1 *with* Ex. 1004, Fig, 1(a); Ex. 1002, ¶ 123.

[1] Citations to 35 U.S.C. §§ 102 and 103 refer to the pre-AIA versions.



Ex. 1001, Fig. 1 (annotated)



Ex. 1004, Fig. 1(a) (annotated)

As shown above on the right, Iwata's inverter has a DC power source (**red**) and AC output V_A (**yellow**). Ex. 1004, Abstract, [0045], [0047]. It includes a bidirectional DC-DC converter (**blue**) that converts the DC input into a set of DC voltages V_{1B} and V_{2B}. Ex. 1004, [0048], [0077], [0084], [0097], Fig. 1(a). The single-phase inverters 1B-INV, 2B-INV and 3B-INV (**green**) have DC input voltages V_{1B} (from the DC to DC converter), V_{2B} (from the DC to DC converter), and V_{3B} (from the DC power source), respectively. Ex. 1004, [0048]-[0049], [0051]; Ex. 1002, ¶¶ 124-125.

As shown below, Iwata, again like the '710 patent, discloses that each of the single-phase inverters consists of switching devices, such as transistors in an H-

bridge configuration (**green**). *Compare* Ex. 1001, 8:33-40, Fig. 3 *with* Ex. 1004, [0046], Fig. 1(b); Ex. 1002, ¶¶ 126, 95, 102-105.

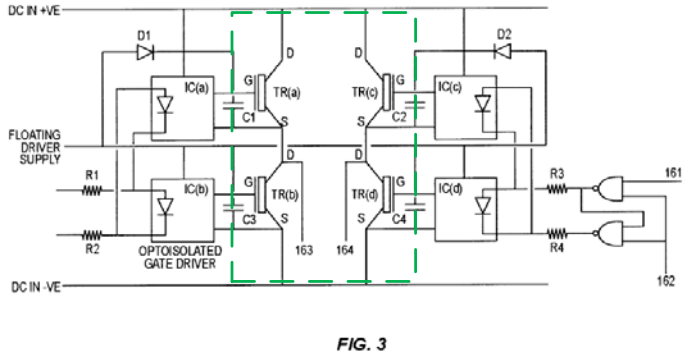
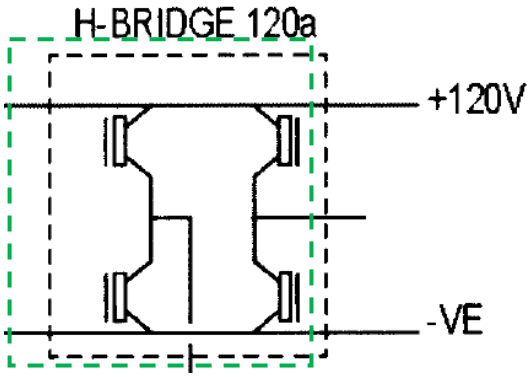


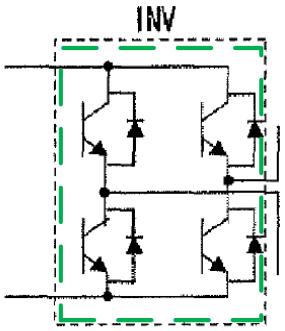
FIG. 3

Ex. 1001, Fig. 3 (annotated)



Ex. 1001, Fig. 6 (excerpted, annotated)

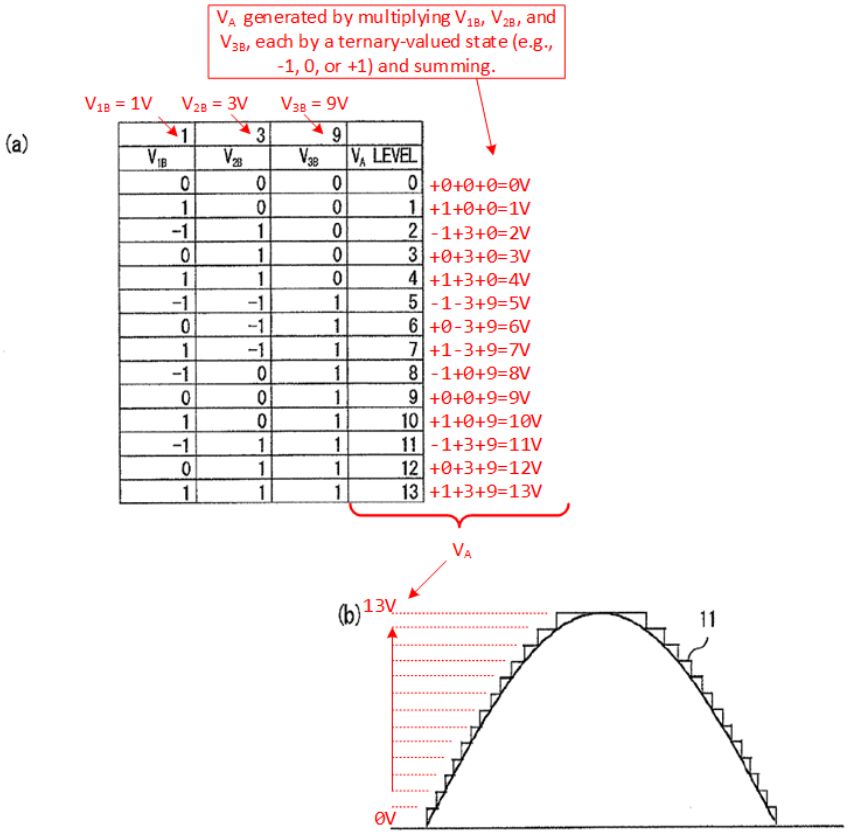
(b)



Ex. 1004, Fig. 1(b) (annotated)

In Iwata, each single-phase inverter has a different DC supply voltage and is controlled so that, depending on the state of the switching circuit, the inverter will output either the DC supply voltage, the inverse of the DC supply voltage, or zero volts. Ex. 1004, [0047], [0050], [0059]. The switch states can be controlled based on a ternary system with a value of +1 associated with positive DC voltage, -1 associated with negative DC voltage, and 0 associated with zero voltage. Ex. 1004, [0050], Fig. 2(a). As shown below, by controlling the states of the switching devices

over time and summing the outputs of the inverters (*i.e.*, 1B-INV, 2B-INV and 3B-INV), an AC output wave is generated. Ex. 1004, Abstract, [0007]-[0009], [0047], [0050]-[0051], [0059], [0101], Figs. 2, 4; Ex. 1002, ¶ 127.



Ex. 1004, Fig. 2 (annotated)

As shown above, voltages V_{1B}, V_{2B}, and V_{3B} are the DC voltage inputs for 1B-INV, 2B-INV, and 3B-INV, respectively, and the control states (*i.e.*, +1, 0, -1) of the switching circuits of those inverters are shown in the first three columns of Figure 2(a). Ex. 1004, [0050], Fig. 2(a). The V_A voltage, which is the sum of the output voltages of 1B-INV, 2B-INV, and 3B-INV, is shown in the fourth column and is

also shown graphically in Figure 2(b), approximating a sinewave. Ex. 1004, [0050], Fig. 2(b); Ex. 1002, ¶ 128.

B. Bower

Bower (Ex. 1011) is a U.S. Patent issued on June 15, 2004, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 129.

Bower discloses inverters that can connect to both utility grids and residences. Ex. 1011, 2:19-26, 2:32-46, 2:55-64, 10:16-29, 10:47-65, 11:11-18, 12:34-44, Figs. 1-5, 7, 11, 13. Bower's inverters provide AC power at voltages and frequencies used in standard households, such as "120V or any other single-phase voltage with one terminal grounded that is intended to be connected to the neutral conductor in the house." Ex. 1011, 10:16-29; Ex. 1002, ¶ 130.

Bower teaches methods for connecting an inverter with a two-terminal output (such as that of Iwata or the '710 patent) to an electrical grid having two hot input terminals and a single neutral terminal in accordance with the NEC 2008 standards. Ex. 1011, 6:66-7:2, 10:16-11:18, Figs. 3-7, 11. Bower teaches the AC output of these inverters can provide AC power across a hot terminal and a neutral terminal. Ex. 1011, 10:21-29, 11:11-18, Figs. 3, 7, 11; Ex. 1002, ¶¶ 131-132.

C. Mori ’630

Mori ’630 (Ex. 1005, certified translation Ex. 1006) is a Japanese Patent Application published on September 7, 2006, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 197.

Mori ’630 teaches an inverter comprising a plurality of single-phase inverters, each connected to a different floating DC power source, and each connected in series to form a single multiplex inverter. Ex. 1006, Fig. 1, [0009]. Each of the single-phase inverters is composed of switching elements, such as a plurality of MOSFETs, in an H-bridge configuration that are controlled by ternary-valued signals produced by a control circuit. Ex. 1006, [0009]-[0012], [0015]. The outputs of each floating DC power source are connected to inputs of a corresponding H-bridge switch. Ex. 1006, Fig. 1. Mori ’630 teaches connecting the H-bridge switch with the highest associated DC voltage to the neutral output terminal. Ex. 1006, [0009]-[0012]; Ex. 1002, ¶¶ 198-199.

D. Mori ’265

Mori ’265 (Ex. 1016, certified translation Ex. 1007) is a PCT Published International Application published on July 22, 2010, making it prior art under 35 U.S.C. § 102(a). Ex. 1002, ¶ 233.

Mori ’265 teaches a power converter that combines the outputs of a plurality of inverters to generate a desired AC output waveform. Ex. 1007, [0047], Fig. 14.

Each inverter has transistors in an H-bridge configuration and outputs one of three levels (+V, -V, or 0). Ex. 1007, [0011], [0028], [0032], [0047], Figs. 11, 14. Mori '265 explains the ternary control signals that are generated to place the switches into either a +1, -1, or 0 state. Ex. 1007, [0011], [0028], [0032], [0048]-[0050], Fig. 11; Ex. 1002, ¶ 234. Gate driving signals which are controlled by a pair of binary bits (RX and RY) are sent to the gates of the switching devices of each of the inverters. Ex. 1007, [0031], [0050]. There are four possible patterns for the binary values of these two bits (*i.e.*, 00, 01, 10, and 11) and each such pattern places an H-bridge switch into one of its three possible states. Ex. 1007, [0031]-[0032], [0050]. Particularly, one combination places a switch into the +1 state, another places the switch into the -1 state, and the remaining two combinations place the switch into the 0 state. Ex. 1007, [0032], [0050]; Ex. 1002, ¶ 234.

E. Flanagan

Flanagan (Ex. 1008) is a U.S. Patent issued on March 21, 1995, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 247.

Flanagan teaches a programmed PWM controller for controlling an inverter comprising three pairs of inverter switches. Ex. 1008, Abstract, 4:64-68. Flanagan's controller outputs a sequence of gating signals to generate the desired inverter output. Ex. 1008, 5:18-29. Specifically, the memory of the controller stores a series of drive data words, each of which includes both a driveword for controlling the

switch states of the inverter and a drivetime word providing timing information within the PWM sequence. Ex. 1008, 5:29-34; Ex. 1002, ¶ 248. The first driveword and corresponding drivetime word are retrieved from the memory and output onto data buses. Ex. 1008, 5:55-6:35. When the address counter is incremented, the next driveword and corresponding drivetime word in the sequence are retrieved and output onto the data buses. Ex. 1008, 5:55-6:35. This procedure is repeated for each drive data word in the sequence to control the inverter to produce the desired output voltages at the desired times. Ex. 1008, 6:35-50; Ex. 1002, ¶ 248.

F. Tracy

Tracy (Ex. 1009) is a U.S. Patent issued on August 8, 2006, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 260.

Tracy teaches a power converter apparatus that can include, as shown below, a battery (**red**) as an uninterruptable power supply (UPS) as the DC power source for an inverter. Ex. 1009, 1:6-47, 4:50-59, 5:1-6, 5:41-52, 6:46-49. As Tracy states, batteries were commonly used as the DC power source for inverters to provide auxiliary power. Ex. 1009, 1:10-16; Ex. 1002, ¶ 261.

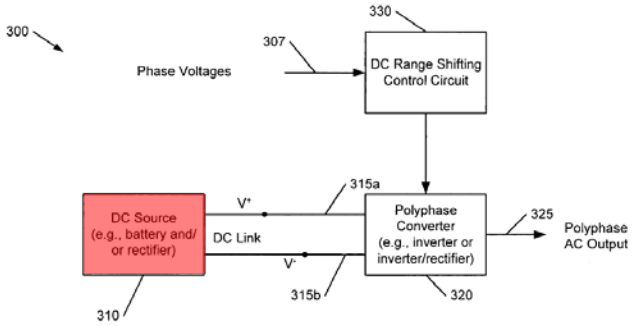


FIG. 3

Ex. 1009, Fig. 3 (annotated)

G. **Nishimura**

Nishimura (Ex. 1014) is a U.S. Patent Application Publication first published on April 2, 2009, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 268.

Nishimura provides a structure for a bidirectional DC-DC converter similar to the structure of the ’710 patent, including center-tapped windings (**red**) that are connected to the positive terminal of the DC input or output (**blue**) with ends of the windings connected to the drains of N-Type MOSFET pairs (**green**):

FIG.4

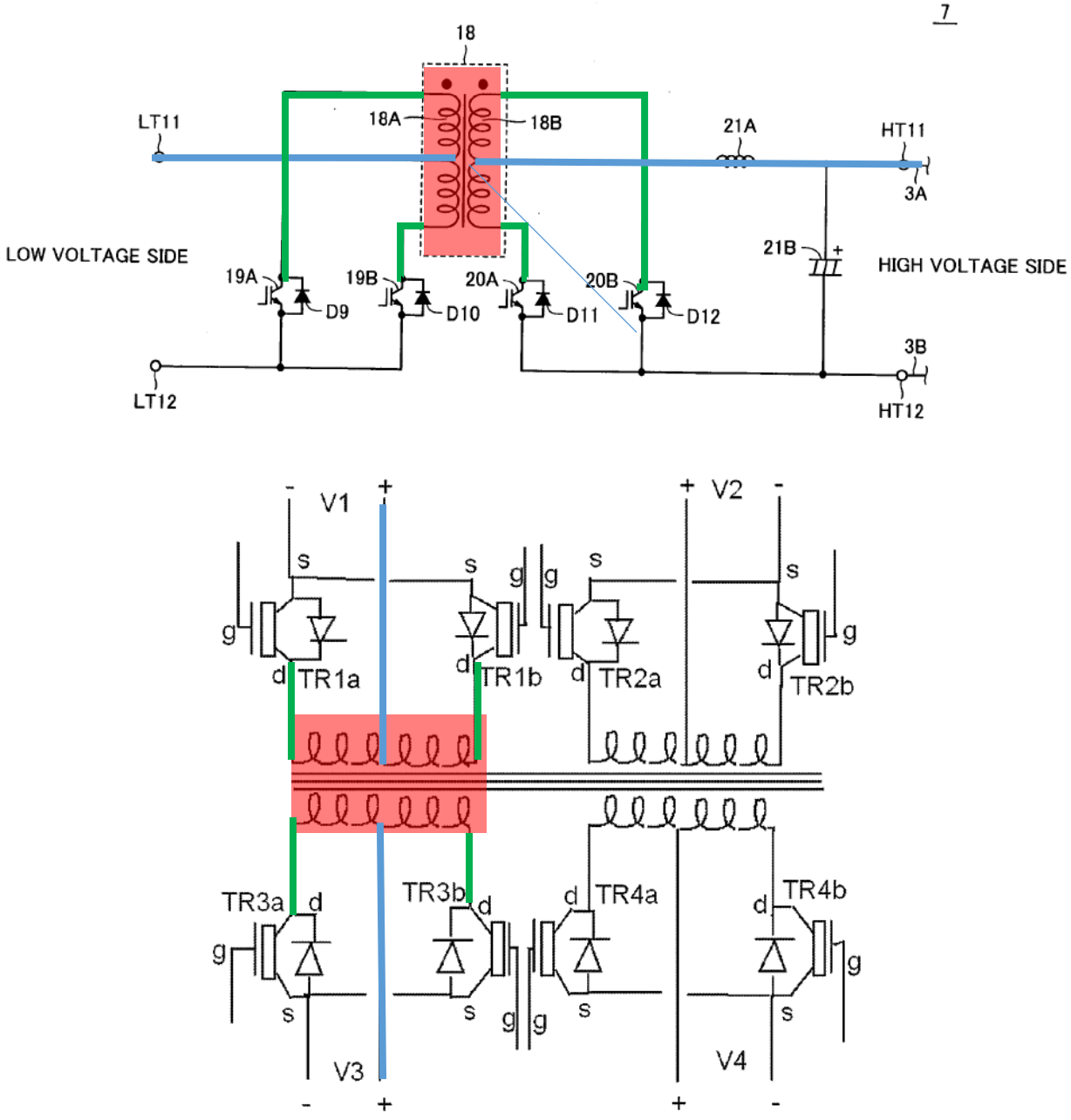


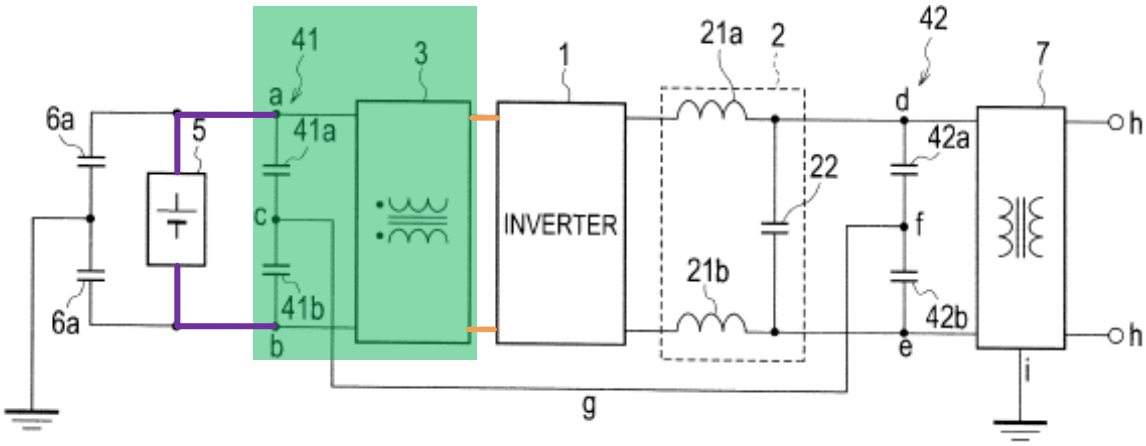
FIGURE 2: BIDIRECTIONAL DC-DC CONVERTER

Ex. 1014, [0091]-[0101], Fig. 4 (annotated, top); Ex. 1001, 18:34-47, Fig. 2. (annotated, bottom); Ex. 1002, ¶ 269.

H. **Koyama**

Koyama (Ex. 1017, certified translation Ex. 1013) is a PCT Published International Application published on May 20, 2010. Koyama is prior art under 35 U.S.C. § 102(a). Ex. 1002, ¶ 276.

As shown in figure 5 below, Koyama discloses a common mode filter (**green**), including a first common mode choke coil 3a and capacitors 41a, 41b, connected between DC input terminals of an inverter 1 (**orange**) and positive and negative terminals of DC power source 5 (**purple**). Ex. 1013, [0005]-[0008], [0012], [0024]-[0026], [0030]-[0031], [0036]-[0038], Figs. 1, 5; Ex. 1002, ¶ 277.



Ex. 1017, Fig. 5 (annotated).

I. Phadke

Phadke (Ex. 1015) is a U.S. Patent issued on November 5, 2013, based on an application filed on December 22, 2010, making it prior art under 35 U.S.C. § 102(e). Ex. 1002, ¶ 314.

Phadke discloses DC to DC converters for photovoltaic arrays to provide power for an inverter. Ex. 1015, 1:14-16, 3:57-65, 4:32-41, 4:66-5:6, Fig. 2; Ex. 1002, ¶ 315. Within the converters, Phadke discloses a switch and a resistor inserted in parallel between two stages, as shown in Figure 6 below:

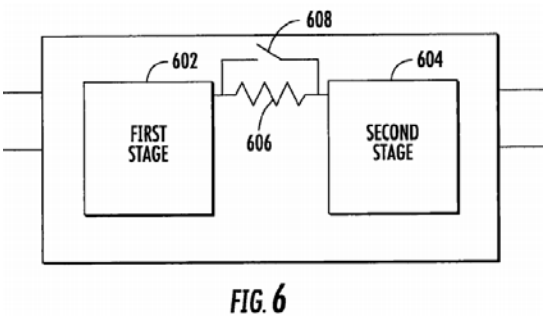


FIG. 6

Ex. 1015, Fig. 6

To protect the circuit during startup, the switch is held open so that the resistor limits the amount of current flowing to the second stage. Ex. 1015, 7:1-8, 7:19-27; Ex. 1002, ¶¶ 316-317. Once a certain threshold is reached, the switch 608 is closed, thus removing any impedance between the two stages. Ex. 1015, 7:8-11.

J. **Ahmed**

Ahmed (Ex. 1012) is an article published and available to the public in 2007, making it prior art under 35 U.S.C. § 102(b). Ex. 1002, ¶ 287; Ex. 1039, ¶¶ 41-65.

Ahmed discloses a design method for low pass LC filters to reduce switching frequency harmonics of inverters. Ex. 1012, 1, Fig. 1 (reproduced below); Ex. 1002, ¶ 288.

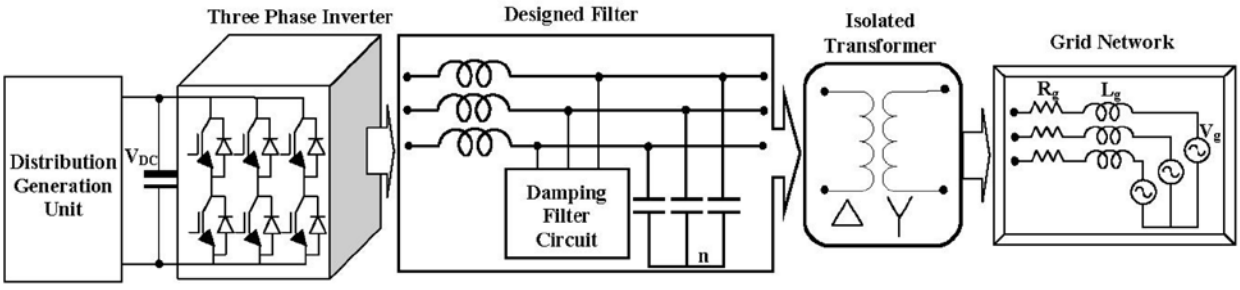


Fig. 1. Block diagram of the proposed interfacing system

Ahmed identifies the problem in such filters of resonance between the inductor (L) and capacitor (C) components, and provides a solution to reduce resonance by adding a damping circuit, which includes a resistor with an additional capacitor and/or inductor. Ex. 1012, 7-8, Figs. 13-15; Ex. 1002, ¶ 289.

VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1–17 on the following grounds. Ex. 1002 ¶¶ 117-118.

Ground	References	Basis	Claims Challenged
A	Iwata in view of Bower	§ 103(a)	1-3, 5, 7-8, 10-12
B	Iwata-Bower in view of Mori ’630	§ 103(a)	4, 7-8, 12
C	Iwata-Bower, in view of Mori ’265	§ 103(a)	6
D and E	Iwata-Bower and Iwata-Bower-Mori ’630, each in view of Flanagan	§ 103(a)	9
F	Iwata-Bower, in view of Tracy	§ 103(a)	10-11

G and H	Iwata-Bower and Iwata-Bower-Tracy, each in view of Nishimura	§ 103(a)	10-11
I and J	Iwata-Bower and Iwata-Bower-Tracy, each in view of Koyama	§ 103(a)	13
K, L, M, and N	Iwata-Bower, Iwata-Bower-Tracy, Iwata-Bower-Mori ’630, and Iwata-Bower-Tracy-Mori ’630, each in view of Koyama and Ahmed	§ 103(a)	14-15
O	Iwata-Bower, in view of Ahmed	§ 103(a)	16
P	Iwata-Bower, in view of Phadke	§ 103(a)	17

None of the prior art listed in the table above was before the examiner during prosecution of the ’710 patent.

B. Level of Ordinary Skill

A person having ordinary skill in the art (“PHOSITA”) would have had a bachelor’s degree in electrical engineering or a similar discipline, and three years of design experience with power electronics, including experience designing power converters. Ex. 1002, ¶¶ 20-23.

C. Claim Construction

All claim terms herein should be given their ordinary and customary meaning to a PHOSITA, consistent with the prosecution history, as they would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b). Petitioner does not contend for this IPR that the claims include any means-plus-function limitations, but

identifies the following claim elements in case the Board finds them to be means-plus-function elements. 37 C.F.R. § 42.104(b)(3).

1. "a switch selection signal generator operative to"

To the extent the Board finds this is a means-plus-function term in claims 7-9, the function is to produce ternary-valued selection signals as set forth in claims 7-9, respectively, and the corresponding structure is controller 200 illustrated in Figure 1 or controller 202-2 illustrated in Figure 11, which include a microcontroller, microprocessor, or an equivalent structure that send the signals to switch driving circuits. Ex. 1001, 12:54-56, 13:21-27, 13:33-47, 15:39-41, 16:48-51, 16:61-63, Figs. 1, 11; Ex. 1002, ¶¶ 119-120.

2. "bi-directional DC-DC conversion circuitry operative to"

To the extent the Board finds this is a means-plus-function term in claims 10 and 11, the function is to derive the lower voltage values (claim 10) or lower mean power (claim 11) from the battery and the corresponding structure is windings on one or more transformers which have turn ratios in proportion to the voltage ratios being output wherein each winding corresponding to the lower voltage values or lower mean power is center tapped, or an equivalent structure. Ex. 1001, 16:30-32, 19:41-48, 20:9-28, Fig. 2; Ex. 1002, ¶ 121.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

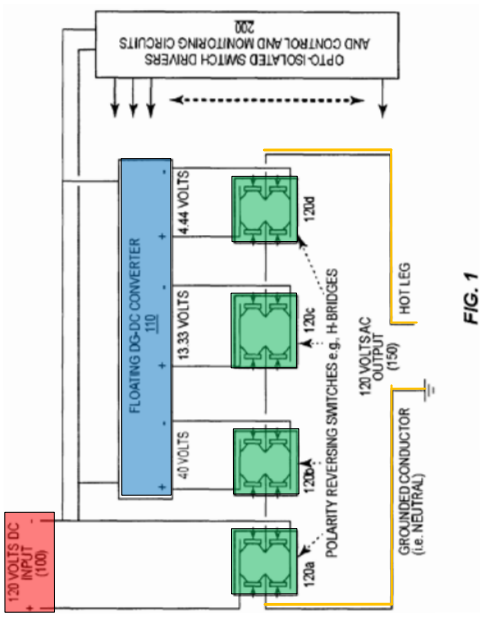
A. Ground A: Claims 1-3, 5, 7-8, and 10-12 are Rendered Obvious by Iwata in View of Bower

1. Independent Claim 1

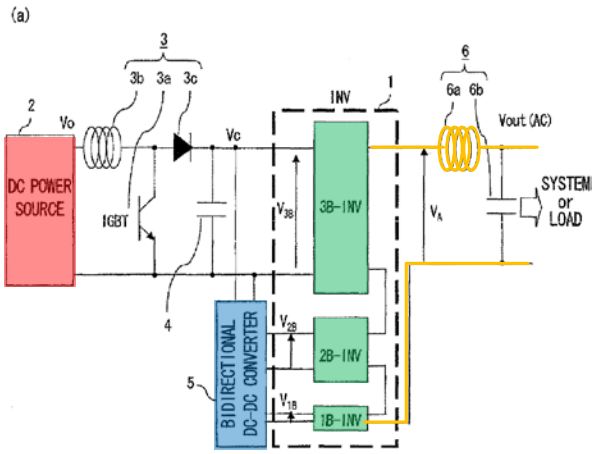
Elements [1A]-[1F] are rendered obvious by Iwata in view of Bower. Ex. 1002, ¶¶ 19, 34-49, 122-156.

a. [1A]: "A DC to AC converter having"

As shown below, Iwata discloses a DC to AC inverter similar to that in the '710 patent with an output that approximates a sinewave by summing the output of a set of series-connected single-phase inverters, each single-phase inverter consisting of a switching circuit. *Compare* Ex. 1001, 6:65-7:7, Fig. 1 *with* Ex. 1004, Abstract, [0007]-[0009], [0046]-[0048], [0056], [0059], [0101], Fig. 1(a); Ex. 1002, ¶¶ 133-135.



Ex. 1001, Fig. 1 (annotated)

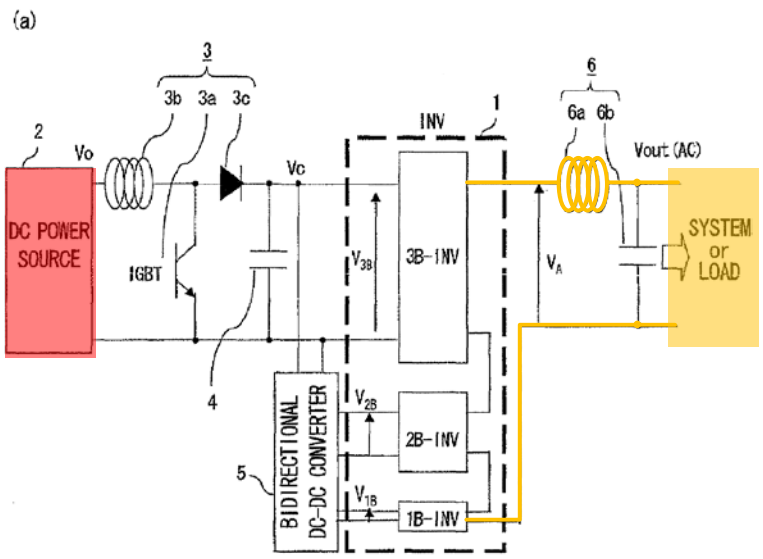


Ex. 1004, Fig. 1(a) (annotated)

Thus, Iwata discloses [1A].

b. [1B] "a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,"

Iwata's power conversion apparatus discloses a DC to AC converter that is operative to convert DC power [DC input (**red**)] to an AC power [AC output Vout (AC) (**yellow**)] as shown in Figure 1(a) below. Ex. 1004, [0001], [0006]-[0009], [0050]-[0053], [0061], [0078], [0090], [0097], [0119], Figs. 1, 2, 4, 5; Ex. 1002, ¶ 136. Iwata's inverter outputs a desired voltage and waveform by generating different voltage levels through different combinations of the outputs of inverters 1B-INV, 2B-INV, and 3B-INV to produce "a substantially sine wave-like output voltage waveform 11" as generally shown in Figure 2(b), which may have, for example, an AC output of 200V. *See, e.g.*, Ex. 1004, [0050]-[0053], [0061], [0078], [0090], [0097], [0119], Figs. 2, 4, 5, 13, 15; Ex. 1002, ¶ 136.



Ex. 1004, Fig. 1(a) (annotated)

Iwata's inverter, shown in Figure 1(a) above, does not include a transformer between the series-connected inverters 1B-INV, 2B-INV, and 3B-INV (H-bridge switches) and the output Vout (AC), and thus the output is "transformerless." *Compare* Ex. 1004, [0047], Fig. 1 ("Vout (AC)") *with* Ex. 1001, 7:60-61, Fig. 1 ("120VOLTS AC OUTPUT (150)"); Ex. 1001, 2:44-47 (admitting transformerless inverters were known in the prior art); Ex. 1002, ¶ 137.

Thus, Iwata discloses [1B].

c. [1C]: "and to output the AC power between hot and neutral output terminals,"

Based on Iwata's teachings and his general knowledge, a PHOSITA would have found it obvious that Iwata's inverter would output AC power between hot and neutral output terminals. Ex. 1002, ¶¶ 138-141. To the extent Iwata does not teach this, it would have been obvious in view of Bower. Ex. 1002, ¶¶ 142-144.

Iwata teaches outputting AC power across a pair of terminals connected to a system or load. Ex. 1004, Abstract, [0006], [0047], [0059], [0101], [0119], Figs. 1, 14, 16-18; Ex. 1002, ¶ 139. A PHOSITA would understand a "system" in Iwata to include an AC electrical grid, for example one in compliance with the National Fire Protection Association (NFPA) 70 National Electrical Code 2008 Edition (NEC 2008) that is cited repeatedly in the '710 patent and was the most widely adopted installation code in the United States. Ex. 1002, ¶ 139; Ex. 1001, 25:5-9, 32:8-11, 33:4-6; Ex. 1018, 7-8; Ex. 1039, ¶¶ 66-79. A PHOSITA would also understand that a residential single-phase AC electrical grid input would include three wires: two hot (or line) wires and one neutral wire. Ex. 1018, 11-12 (Exhibit 100.12); Ex. 1002, ¶ 139.

Therefore, when attaching a single-phase inverter having a two-wire output (*e.g.*, Iwata's inverter) to a residential single-phase AC electrical grid input, there would only be two options: (1) connect the two output terminals of Iwata's inverter to the two hot wires of the AC electrical grid (*e.g.*, 240 VAC), or (2) connect one output terminal of Iwata's inverter to a hot wire of the AC electrical grid and the other output terminal of Iwata's inverter to the neutral wire of the AC terminal (*e.g.*, 120VAC). Ex. 1002, ¶¶ 140-141. The second (indeed, either) option would have been obvious as one of only two choices, because a PHOSITA would have followed safety standards, including NEC 2008, which allows for connecting inverters, such

as that disclosed in Iwata, between hot and neutral terminals of a grid for medium sized residential hybrid photovoltaic systems. Ex. 1018, 24 (Exhibit 690.4); Ex. 1002, ¶ 141. A PHOSITA would have had a high expectation of success in following the standard to connect the inverter in such a manner. Ex. 1018, 8; Ex. 1002, ¶ 141; *see also* Ex. 1011, 10:18-29.

To the extent Iwata does not teach an inverter that outputs AC power between hot and neutral terminals, Bower does. Bower discloses inverters within a PV system that can be used to provide single-phase AC power to, among other things, a utility grid or a residence. Ex. 1011, 2:19-26, 2:32-46, 2:55-64, 10:16-29, 10:47-65, 11:11-18, 12:34-44, Figs. 1-5, 7, 11, 13; Ex. 1002, ¶ 142. As shown in the example below, the AC output of these inverters can provide AC power across a hot terminal (**red**) and a neutral terminal (**green**) in accordance with the NEC 2008 standards, including having the neutral terminal connected to ground circuit 50. Ex. 1011, 10:21-38, 11:11-18, Figs. 3, 7, 11; Ex. 1002, ¶ 142.

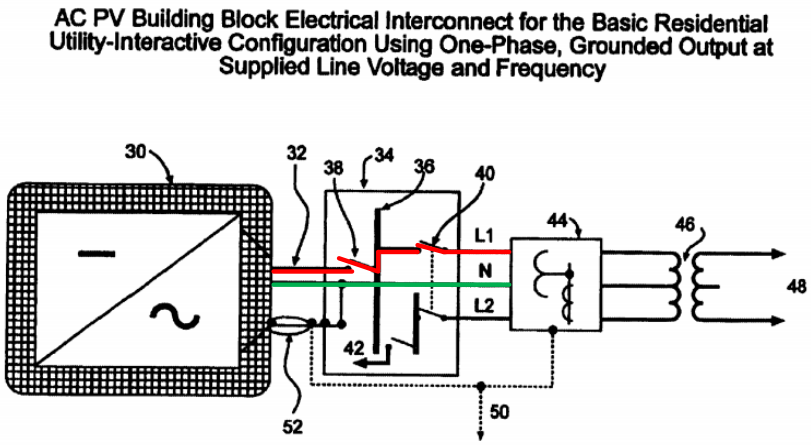


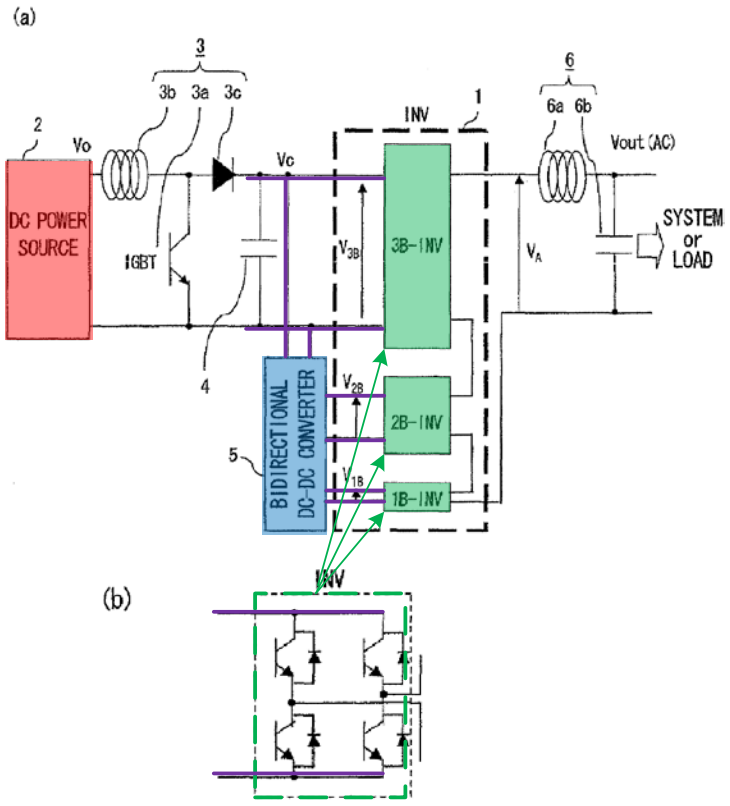
Fig. 3

Ex. 1011, Fig. 3 (annotated)

It was obvious to use a known technique (attaching the AC outputs of a two terminal inverter to an AC electrical grid so that one terminal is hot and the other is neutral as taught in Bower) to a improve a similar device (Iwata's inverter) in the same way (connecting the output terminals of an inverter to an AC electrical grid). Ex. 1002, ¶ 143. A PHOSITA was familiar with connecting the output terminals of an inverter to an AC electrical grid so that one terminal was hot and the other was neutral, and would have had the skills to do so, providing an expectation of success. Ex. 1002, ¶¶ 143, 67-69.

Thus, Iwata in view of Bower renders [1C] obvious. Ex. 1002, ¶¶ 138-144.

d. [1D]: "the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and"



Ex. 1004, Fig. 1 (annotated)

As highlighted in Figure 1(a) above, Iwata's inverter comprises "a plurality of controlled switches" (**green**), described as three single-phase inverters 3B-INV, 2B-INV and 1B-INV. Ex. 1004, [0045]-[0049]. Each switch includes a plurality of switching devices arranged in an H-bridge switch like those disclosed in the '710 patent. Ex. 1004, [0046], Fig. 1; Ex. 1002, ¶¶ 145-146. As will be discussed in more detail in relation to Element [1E] below, these switches are controlled to produce

positive, negative, or zero voltages from their respective DC power sources. Ex. 1004, [0047], [0050], [0059], Figs. 2, 4-5; Ex. 1002, ¶¶ 149-151.

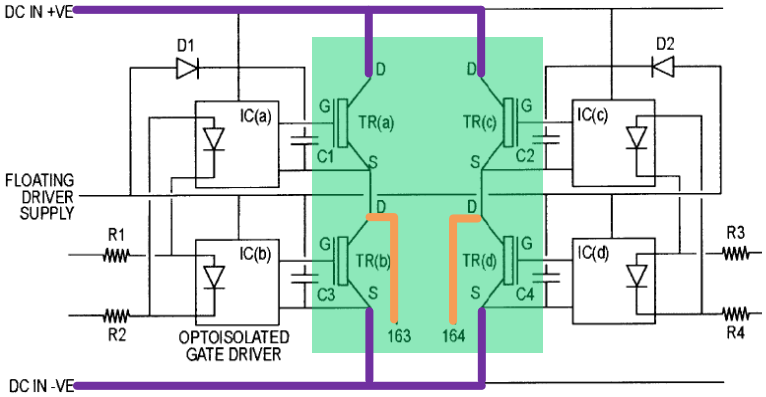
Each of these switches have input connections (highlighted in **purple** above) connected to and receiving DC power from an associated DC power source (highlighted in **red** and **blue** above), which is either DC power source 2 (for the 3B-INV switches) or bidirectional DC-DC converter (for the 1B-INV and 2B-INV switches). Ex. 1004, [0046], [0048]-[0049], [0077], [0083]-[0084], [0097], [0100], [0103]-[0111], Figs. 1, 14, 16-18; Ex. 1002, ¶ 147. In Iwata's embodiment from Fig. 1, for example, V_{1B}, V_{2B}, and V_{3B} are the DC power source voltage inputs, respectively, for the plurality of switches 1B-INV, 2B-INV and 3B-INV. Ex. 1004, [0049], Fig. 1; Ex. 1002, ¶ 147. Further, "V_{3B}, V_{2B}, and V_{1B} are controlled to have predetermined voltage ratio by the DC-DC converter 5," which can include 1:2:4 or 1:3:9. Ex. 1004, [0048], [0050], [0051], Figs. 2, 4-5.

Thus, Iwata discloses [1D]. Ex. 1002, ¶¶ 145-148.

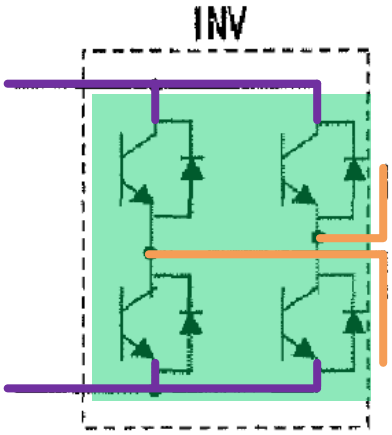
e. [1E]: "each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,"

Iwata's inverters are arranged and controlled identically to the H-bridge switches disclosed in the '710 patent (as shown in the comparison figures below) via a ternary-valued selection signal to operate in three states Iwata refers to as +1, -1,

and 0. Ex. 1004, [0046], [0050]-[0051], [0059], Figs. 2, 4-5; Ex. 1001, 7:23-28, 8:33-54, 9:58-64, 11:5-13, 11:26-35, Fig. 3; Ex. 1002, ¶ 149.



Ex. 1001, Fig. 3 (annotated)



Ex. 1004, Fig. 1(b) (annotated)

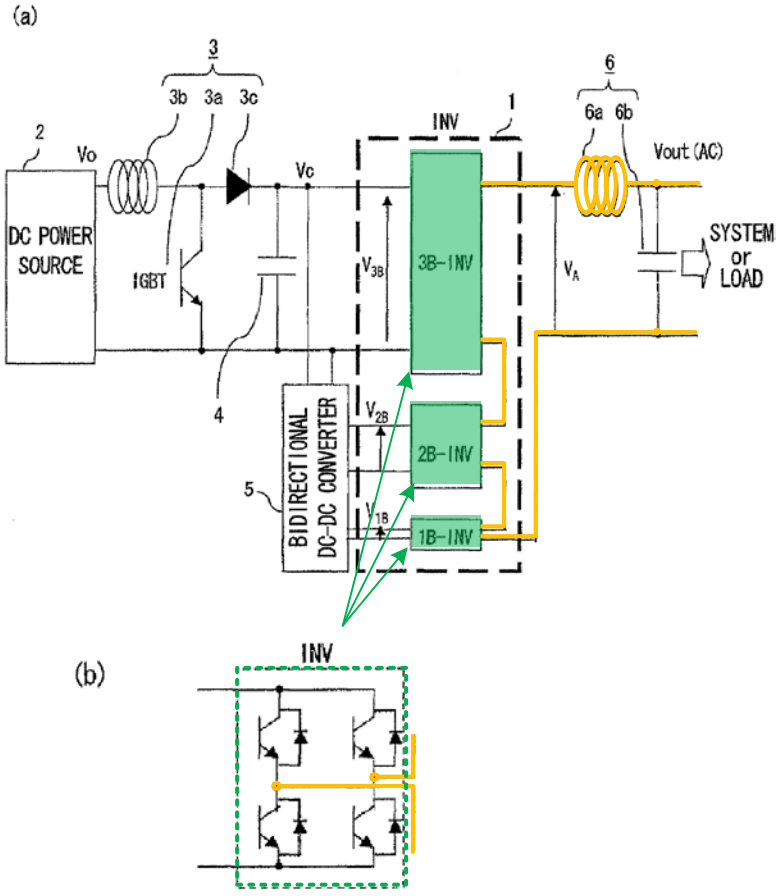
For example, in Iwata's Embodiment 1, the 1B-INV, 2B-INV and 3B-INV inverters can each output either a positive or negative (*i.e.*, "inverted polarity") voltage of their respective input voltage (*e.g.*, V_{1B}, V_{2B}, or V_{3B}), or a zero voltage based on whether the inverter's respective switches are controlled to be in the +1, -1, or 0 state. Ex. 1004, [0047], [0050], Figs. 1-2; Ex. 1002, ¶ 150. Thus, as required by element [1E], Iwata's switches "hav[e] a power output connection operative to output a selected one of: (a) the associated DC voltage" in response to an associated +1 multiplier value of the selection signal, "(b) the associated DC voltage having an inverted polarity," in response to an associated -1 multiplier value of the selection signal, and "(c) zero voltage" in response to a 0 multiplier value of the selection signal. Ex. 1004, [0050]-[0051], Figs. 2, 4; Ex. 1002, ¶¶ 150-151. This is described

in more detail with an example from Figure 2 of Iwata, immediately below. Section VII.A.1.f, *infra*.

Thus, Iwata discloses [1E].

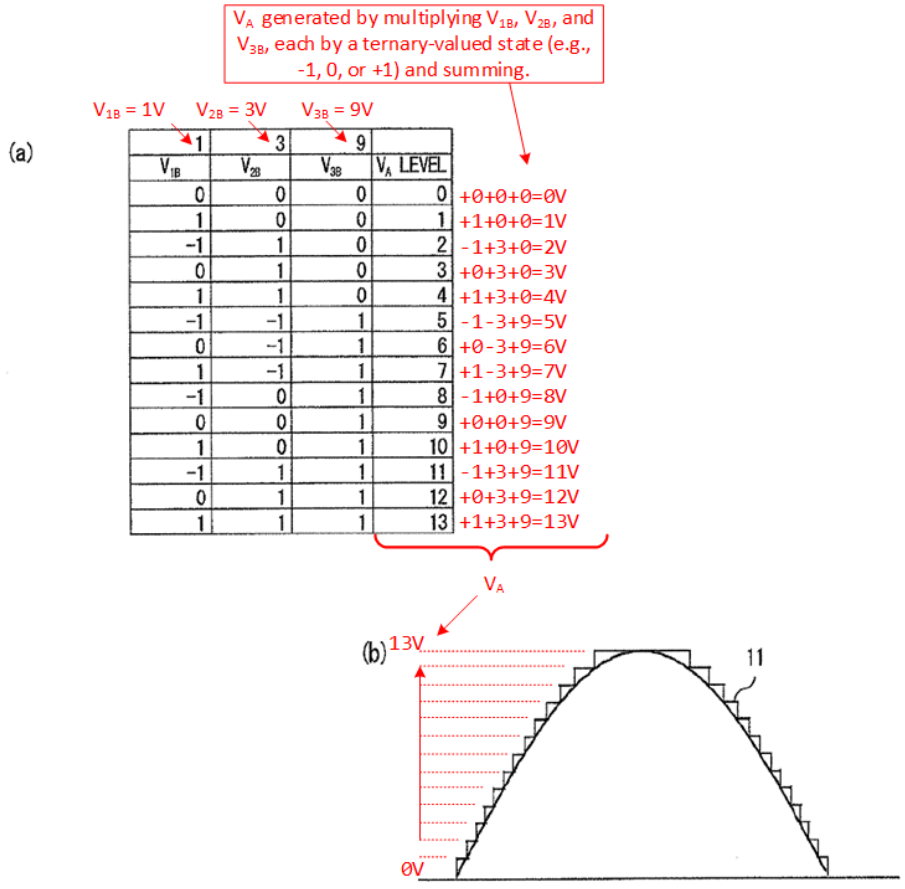
f. [1F]: "the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform."

As shown below, the outputs of Iwata's switches (**green**) are directly connected in series (**yellow**). Ex. 1004, Abstract, [0007]-[0009], [0045], [0051], [0100], Figs. 1, 14, 16-18; Ex. 1002, ¶ 152.



Ex. 1004, Fig. 1 (annotated)

Because the outputs of Iwata's switches are directly connected in series, output V_A is the sum of the outputs of inverters 1B-INV, 2B-INV and 3B-INV in Iwata's Figure 1. Ex. 1004, Abstract, [0007]-[0009], [0047], [0056], [0059], [0101]; Ex. 1002, ¶ 153. As discussed above for Element [1E], the Iwata inverters are each controlled to output either an associated DC voltage (*e.g.*, V_{1B}, V_{2B}, or V_{3B}), or the inverted polarity of that associated DC voltage, or a zero voltage based on a multiplier value of +1, -1, or 0, respectively. Ex. 1004, [0047], [0050], Fig. 1; Ex. 1002, ¶ 153.



Ex. 1004, Fig. 2 (annotated)

The DC power source voltage inputs V_{1B}, V_{2B}, and V_{3B} are in a ratio of 1:3:9, as indicated in the top row of Figure 2(a). Ex. 1004, [0050], Fig. 2(a). The multipliers applied by the switches 1B-INV, 2B-INV, and 3B-INV are shown in the first three columns of Figure 2(a), under the second "V_{1B}, V_{2B}, and V_{3B}" row. Ex. 1004, [0050], Fig. 2(a). The V_A voltage, which is the sum of the output voltages of 1B-INV, 2B-INV, and 3B-INV, is shown in the fourth column of Figure 2(a), under the "V_A LEVEL" entry in the second row. Ex. 1004, [0050], Fig. 2(a); Ex. 1002, ¶ 154.

Rows 3-16 of Figure 2(a) indicate 14 different voltage levels that can be obtained at V_A resulting from multiplying each inverter voltage (1, 3, or 9) by the listed multiplier value (0, +1, -1), and summing the multiplied values as annotated in red to the right of the table. Ex. 1004, [0050], [0053], [0061], Fig. 2(a); Ex. 1002, ¶ 155. These voltage levels are selected based on controlling the state of 1B-INV, 2B-INV, and 3B-INV, to produce the substantially sinewave-like output voltage waveform of Figure 2(b) that is inputted into a smoothing filter. Ex. 1004, Abstract, [0007]-[0009], [0047], [0050]-[0051], [0053], [0059], [0061], [0101], Figs. 2, 4, 5; Ex. 1002, ¶ 155.

Thus, Iwata discloses [1F]. Ex. 1002, ¶¶ 152-156.

2. Claims 2 and 5

Claim 1, from which claims 2 and 5 depend, is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claim 2 further requires "at least some of the DC voltages associated with the plurality of controlled switches have different values," and claim 5 further requires that "each associated DC voltage differs from another DC voltage nominally by a factor of 3." Ex. 1001, claim 2.

Iwata discloses its DC voltages (*i.e.*, V_{1B}, V_{2B}, and V_{3B}) having voltages that differ from one another by a factor of 3, *e.g.*, having a 1:3:9 ratio (*e.g.*, V_{1B}=1V, V_{2B}=3V, and V_{3B}=9V). Ex. 1004, Abstract, [0050]-[0051], [0053], [0060]-[0061], [0079], [0085], [0094], Figs. 2, 4; Ex. 1002, ¶¶ 159, 162.

Thus, Iwata discloses the additional limitations of claims 2 and 5. Ex. 1002, ¶¶ 157-163.

3. Claim 3

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claim 3 depends from claim 1 and requires "the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household electricity supply frequency." Ex. 1001, claim 3. The '710 patent does not state what is "standard," but for something to be "standard," it would necessarily be well-known. Ex. 1002, ¶ 166. Thus, claim 3 merely requires that the desired output voltage and waveform be one that is already so well-known as to have been

established as a standard electricity supply.

It was obvious that Iwata's inverter would be used to output a waveform with the voltage and frequency of a standard household electricity supply. Iwata discloses that its inverter can be connected to a system or load or applied to an uninterruptible power supply. Ex. 1004, Abstract, [0047], [0059], [0101], [0119]; Ex. 1002, ¶ 166. An uninterruptible power supply provides, among other things, emergency power to buildings when power grids fail. Ex. 1002, ¶ 166. Further, Iwata may produce an AC waveform with a voltage of 200 V, which is a standard household voltage for Japan. Ex. 1004, [0005], [0053], [0061], [0085]; Ex. 1010, 22; Ex. 1002, ¶ 166.

Bower discloses the use of an inverter to convert DC power of a solar grid to AC power for use within a standard household, having a standard household frequency. Ex. 1011, 2:55-64, 8:34-36, 10:16-29, 10:47-11:18; Ex. 1002, ¶ 167. Specifically, Bower outputs single-phase 240V, 60Hz AC power or "power at 120V or any other single-phase voltage with one terminal grounded that is intended to be connected to the neutral conductor in the house." Ex. 1011, 10:16-29; Ex. 1002, ¶¶ 167-168. Sixty hertz is a standard household frequency. *Id*.

It was obvious to use a known technique (producing an AC waveform with the voltage and frequency used in a standard household) to improve a similar device (Iwata's inverter) in the same way (Iwata produces AC power for a standard household). Ex. 1002, ¶¶ 169-170. A PHOSITA was familiar with designing an

inverter to produce AC power for use in a household and had the skills to do so, providing an expectation of success. *Id.*

Thus, Iwata in view of Bower renders claim 3 obvious. Ex. 1002, ¶¶ 164-171.

4. Claims 7 and 8

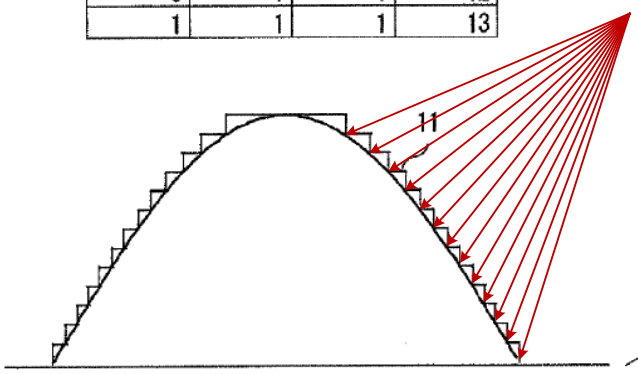
Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claims 7 and 8 each depend from claim 1 and require "a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce [] sets of switch selection signals." Ex. 1001, claims 7, 8.

As described above in Section VII.A.1, Iwata teaches the DC to AC converter of claim 1 that uses a set of ternary-valued selection signals (*e.g.*, +1, -1, 0) to control a plurality of H-bridge switches. Ex. 1004, [0050]-[0051], Figs. 2, 4; Ex. 1002, ¶ 174. This is disclosed, for example, in Iwata's Fig. 2, which shows a "gradational output voltage control operation" being applied to control the sum voltage output waveform 11 (Fig. 2(b)) with a set of ternary-valued selection signals (Fig. 2(a)) sent to each of the H-Bridge switches at different instances in time. Ex. 1004, [0047]-[0050]. Iwata further discloses applying "PWM control" (Fig. 3) to improve the accuracy of the voltage waveform. Ex. 1004, [0050]-[0051]. The sum voltage output, after filtering, is shown as the smooth curves in Figures 2(b) and 3. Ex. 1002, ¶ 174.

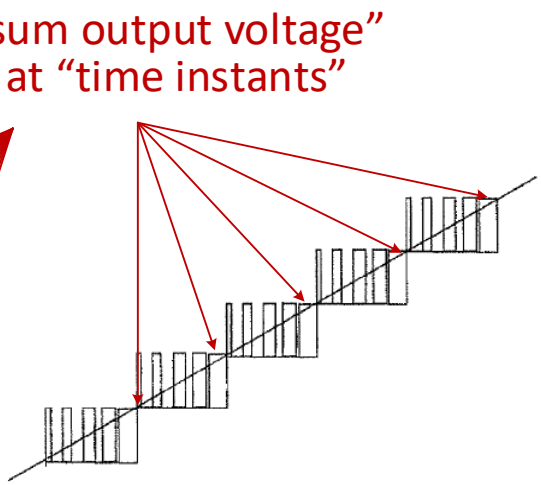
(a)

1	3	9	
V_{1B}	V_{2B}	V_{3B}	V_A LEVEL
0	0	0	0
1	0	0	1
−1	1	0	2
0	1	0	3
1	1	0	4
−1	−1	1	5
0	−1	1	6
1	−1	1	7
−1	0	1	8
0	0	1	9
1	0	1	10
−1	1	1	11
0	1	1	12
1	1	1	13

(b)



Ex. 1004, Fig. 2 (annotated)



Ex. 1004, Fig. 3 (annotated)

A PHOSITA would have understood that "gradational" and "PWM" control disclosed in Iwata would have included a signal generator (*i.e.*, a "switch selection signal generator") generating the ternary-valued control signals sent to the H-bridge switches to create the desired output sum. Ex. 1002, ¶ 175.

Claim 7 further requires the sets of switch selection signals to be produced "at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants." Ex. 1001, claim 7. Claim 8 further requires the sets of switch

selection signals to be "sequential" and the generator to be "configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals." Ex. 1001, claim 8.

As annotated, for instance, in Figures 2(b) and 3 above, Iwata discloses sequential time instants at which each new set of switch selection signals produce a sum output voltage that approximates "the instantaneous voltage values of the desired waveform" (smooth curves in Figures 2(a) and 3). Ex. 1002, ¶ 177. These sum output voltages at the time instants are the "best approximation ... at the given instants" as recited in claim 7, and "a better approximation ... at that time instant than the immediately previously output set of switch selection signals" as recited in claim 8, because: for gradational output voltage control (Fig. 2b), the sum voltage is set equal to the desired waveform at each time instant (Fig. 2b); and for PWM (Fig. 3), the voltage level and width of each pulse accurately approximate the instantaneous voltage and better approximates the instantaneous voltage than the previous pulse at the previous time instant. Ex. 1002, ¶ 177. Iwata teaches these claims 7 and 8 limitations also because, the sum voltage at the time instants, after

filtering, *equal* the desired waveform, a result that Iwata obtains by making "better" and "best" approximations.

Thus, the additional limitations of claims 7 and 8 are taught by Iwata in view of Bower. Ex. 1002, ¶¶ 172-178.

5. Claim 10

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, *supra*. Claim 10 depends from claim 1 and requires "the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery." Ex. 1001, claim 10.

Iwata discloses a bidirectional DC-DC converter 5 operative to derive the lower voltage DC power sources from the primary DC power source 2 generating V_{3B} (the highest voltage input to inverter 3B-INV). Ex. 1004, [0046], [0048], [0077], [0083], [0097]-[0098], [0100], [0103]-[0104], [0108]; Ex. 1002, ¶ 181. Iwata's inverter may be used in a power conditioner for a decentralized power source. One example uses a solar battery as its DC power source. Ex. 1004, [0001]-[0003]. Iwata further discloses that the inverter is used in an "uninterruptible power supply" (UPS), which would obviously include a battery to provide uninterrupted power as the backup power source, when the primary power source was

disconnected or not operating. Ex. 1004, [0119]; Ex. 1009, 1:6-47; Ex. 1002, ¶¶ 181-182.

Thus, the additional limitations of claim 10 are taught by Iwata alone and in view of Bower. Ex. 1002, ¶¶ 179-183.

6. Claim 11

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, *supra*. Claim 11 depends from claim 1 and requires "the DC power source supplying the highest mean power is a battery and the DC power sources supplying lower mean power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery." Ex. 1001, claim 11.

As explained with respect to claim 10, Iwata discloses a bidirectional DC-DC converter 5 operative to derive the lower voltage DC power sources from the primary DC power source 2, and that the inverter may have a solar battery as that source or be used in an "uninterruptible power supply," which teaches that a battery would be included as a backup DC power source. Ex. 1004, [0046], [0048], [0077], [0083], [0097]-[0098], [0100], [0103]-[0104], [0108]; Ex. 1002, ¶ 186; section VII.A.1, *supra*.

While claim 10 recites the *voltage value* of the different DC power supplies, claim 11 recites the *mean power* of the different DC power supplies. *See* Ex. 1001, claims 10, 11. But in the context of Iwata's inverter, this is not a meaningful

distinction. Ex. 1002, ¶ 187. Mean power is the average power output over a certain time period, and power is calculated by multiplying the voltage by the current. Ex. 1002, ¶188. In Iwata, the DC power source (V_{3B}) is taught to have a voltage higher than the other two power sources (V_{1B} and V_{2B}), for example so that the voltage ratio for the three sources is 1:3:9, and the switches are controlled in such a way that the mean power of that source (which is proportional to the voltage) would be higher than the other two. Ex. 1004, [0050]-[0051], Figs. 2, 4; Ex. 1002, ¶ 189. This is the same as is disclosed in the '710 patent, which also has a voltage ratio of 1:3:9 and a similar switching pattern. *See, e.g.*, Ex. 1001, 11:5-18, Fig. 4; Ex. 1002, ¶ 189.

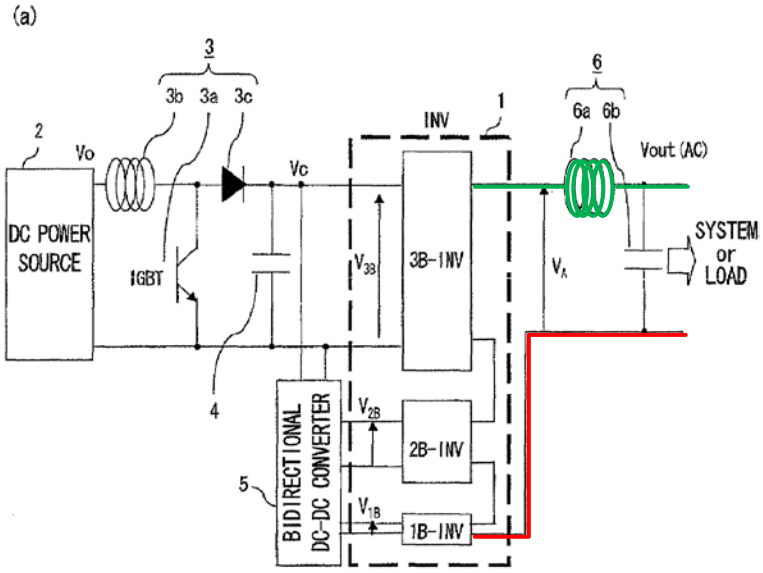
Thus, the additional limitations of claim 11 are taught by Iwata in view of Bower. Ex. 1002, ¶¶ 184-190.

7. Claim 12

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claim 12 further requires that "one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal." Ex. 1001, claim 12.

As discussed above, it would have been obvious that one of the output terminals of the inverter is neutral. Section VII.A.1, *supra*. For example and as shown below, the top output terminal (**green**) of the DC to AC converter as taught

by Iwata-Bower can represent neutral, and this terminal is connected to the switches of inverter 3B-INV, which is at the end of the series of inverters and has input voltage V_{3B}. Ex. 1004, [0046], [0048]-[0049], [0056], [0060], [0077], [0098], [0105], Figs. 1, 14, 16-18; Ex. 1011, 10:21-38, 11:11-18, Figs. 3, 7, 11; Ex. 1002, ¶ 193.



Ex. 1004, Fig. 1 (annotated)

Iwata discloses that input voltage V_{3B} is the highest voltage of the other DC voltages, for example V_{1B}, V_{2B}, and V_{3B}, are in a ratio of 1:3:9. Ex. 1004, [0048], [0050]-[0051], [0060], [0079], [0085], [0094], [0110], Figs. 2, 4, 5; Ex. 1002, ¶ 194. It would have been obvious to a PHOSITA to have either the top or the bottom output be connected to neutral since there are only two possibilities, and choosing between them would be a case of choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. Ex. 1002, ¶ 194. A PHOSITA would have understood the benefits of connecting Iwata's 3B-INV inverter, which

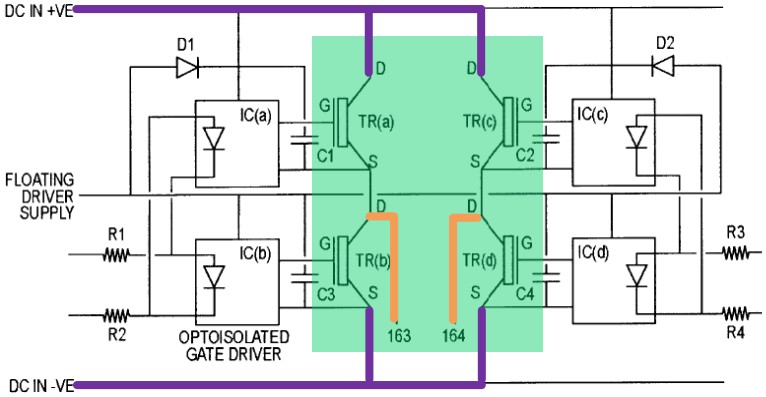
has the highest DC voltage, to the neutral terminal because this arrangement may reduce common mode voltage and electromagnetic interference. Ex. 1004, Figs. 2, 4; Ex. 1002, ¶¶ 194-195.

Thus, Iwata in view of Bower render obvious the additional limitations of claim 12. Ex. 1002, ¶¶ 191-196.

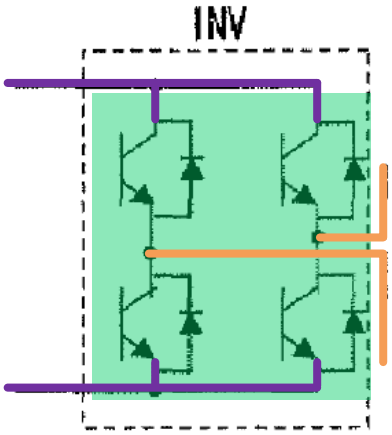
B. Ground B: Claims 4, 7-8, and 12 are Rendered Obvious by Iwata-Bower, in View of Mori '630

1. Claim 4

Claim 4 depends from claim 1 and further recites: "wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals." Ex. 1001, claim 4. As explained above in Section VII.A.1, Iwata-Bower teaches the DC to AC converter of claim 1. Ex. 1002, ¶ 202. As also explained above with respect to claim 2, Iwata's controlled switches are connected in H-bridge configurations like those disclosed in the '710 patent:



Ex. 1001, Fig. 3 (annotated)



Ex. 1004, Fig. 1(b) (annotated)

Moreover, the DC power supply input to these switches are in the same configuration as in the ’710 Patent. Section VII.A.1, *supra*; Ex. 1002, ¶¶ 203-204. The floating DC power sources (circled in dashed blue lines) along with their outputs (shown in solid blue) of the ’710 Patent are shown on the below left, while the floating DC power sources (circled in dashed blue lines) along with their output connections (shown in solid blue) of Iwata are shown on the below right:

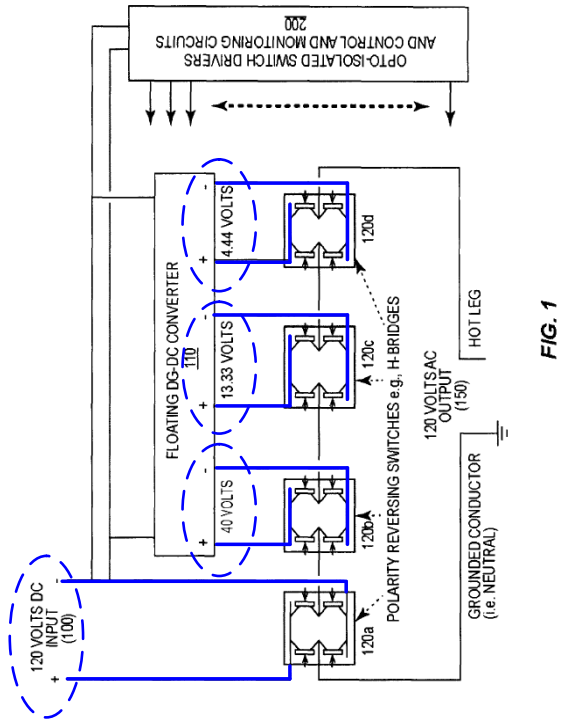
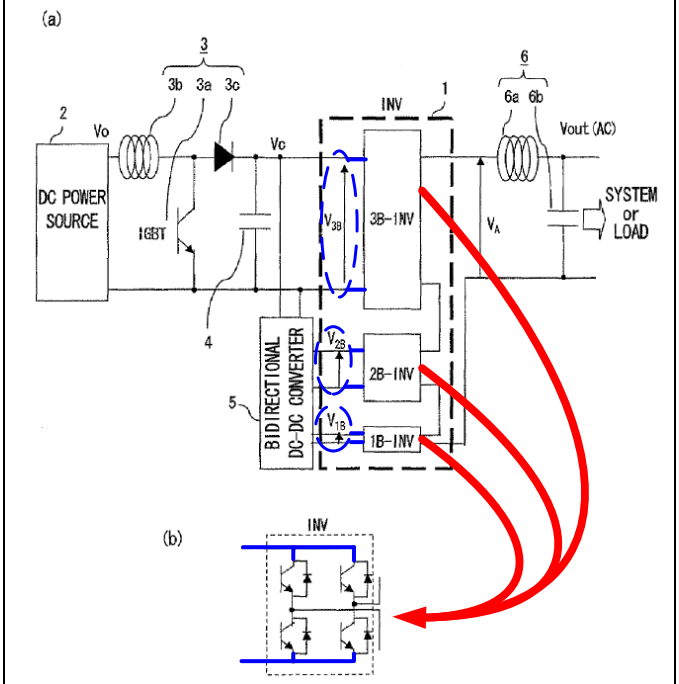
’710 Patent	Iwata
	

FIG. 1

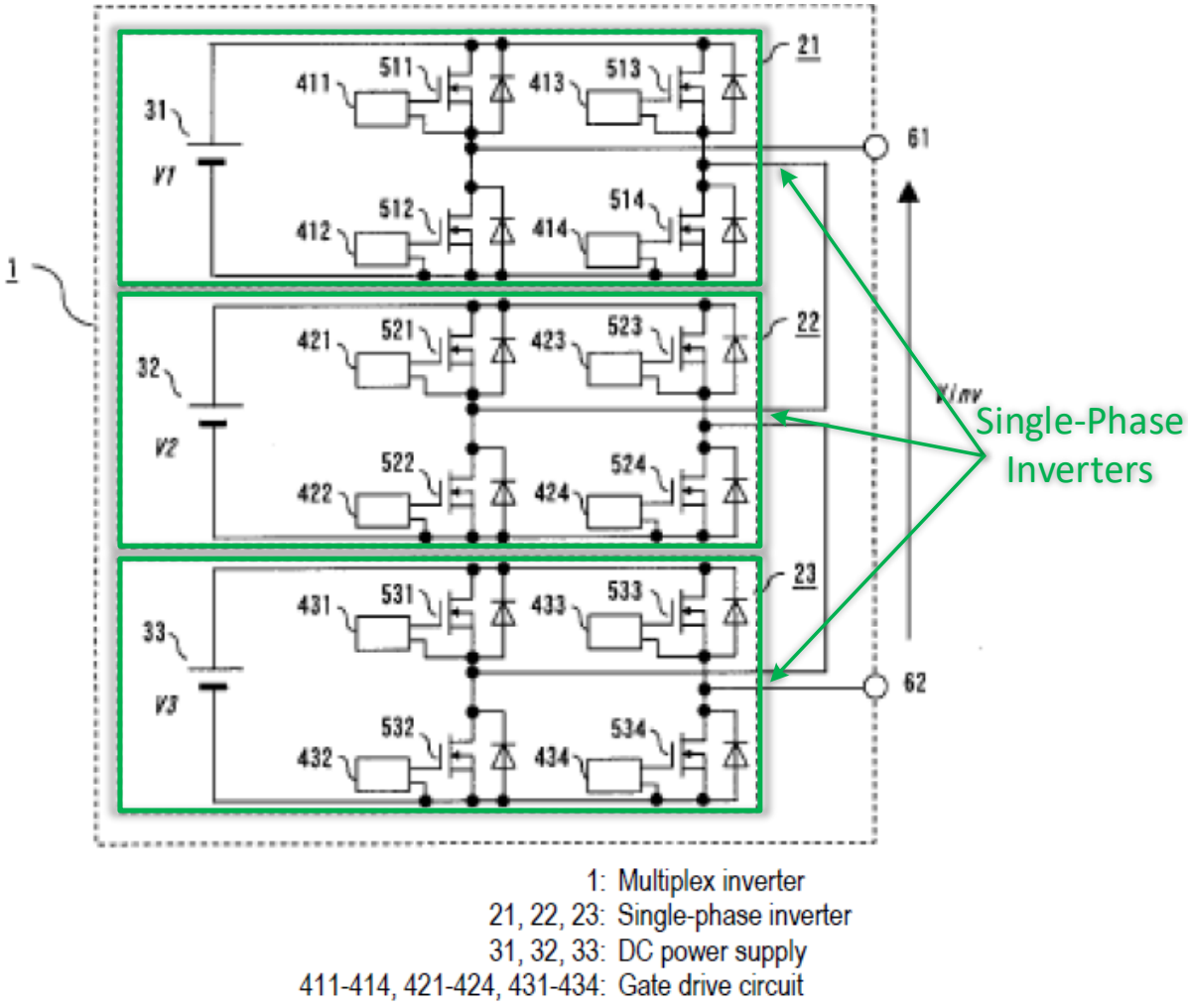
In both the ’710 Patent and Iwata, the output terminals of each DC power source are connected to input terminals of a corresponding H-bridge switch. Ex. 1001, Fig. 1, 7:57-60; Ex. 1004, [0046], [0048], Figs. 1(a), 1(b), 17-18. The switches can change the series arrangement of the voltage sources (*e.g.*, sometimes connecting them in a positive polarity, sometimes connecting them in the reverse polarity, or bypassing them) to generate different sum series voltages. Ex. 1002, ¶ 205. For example, inverter 3B-INV alternatively connects either the plus or minus of the V_{3B} input terminals to the Vout (AC) terminal while connecting the opposite V_{3B} input terminal in series to the other voltage sources through inverters 2B-INV

and 1B-INV. This requires (as is illustrated in Figure 1(a)) the DC power source V_C across capacitor 4 to be floating with respect to the output and with respect to the other DC power sources. The DC power sources V_{2B} and V_{1B} operate in a similar manner and are further offset from the Vout (AC) terminal by the varying voltage output by the adjacent 3B-INV inverter. Thus, the DC power sources V_{2B} and V_{1B} are likewise floating. Ex. 1002, ¶¶ 205, 101-102. Furthermore, Iwata's power sources are not grounded which is consistent with the statement during prosecution of the '710 patent that "[a]s well known in the art, a 'floating' output of a power supply is one that is not referenced to a set voltage, such as chassis or earth ground." Ex. 1003, p. 291.

Thus, Iwata teaches the claimed "wherein the controlled switches are ... connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals," just as shown in the '710 Patent. Ex. 1002, ¶¶ 202-206.

It would have further been obvious to use MOSFETs as Iwata's "controlled switches" as further disclosed in Mori '630. Mori '630 teaches a nearly identical inverter to that of Iwata, comprising a plurality of single-phase inverters ("controlled switches"), each associated with a different DC power source, each configurable to output the associated DC source multiplied by +1, -1, or 0, and all connected in series

to form a single multiplex inverter that outputs a sine wave. Ex. 1006, [0009]-[0012], Figs. 1-3; Ex. 1002, ¶ 207.



Ex. 1006, Fig. 1 (annotated)

Each of Mori '630's single-phase inverters is composed of "self-extinguishing semiconductor switching element" switching elements, which may be IGBTs or MOSFETs. Ex. 1006, [0009], Figs. 1-3. Whether to use a MOSFET or IGBT would have been merely a design choice to a PHOSITA depending upon the application and convenience. Ex. 1002, ¶ 208.

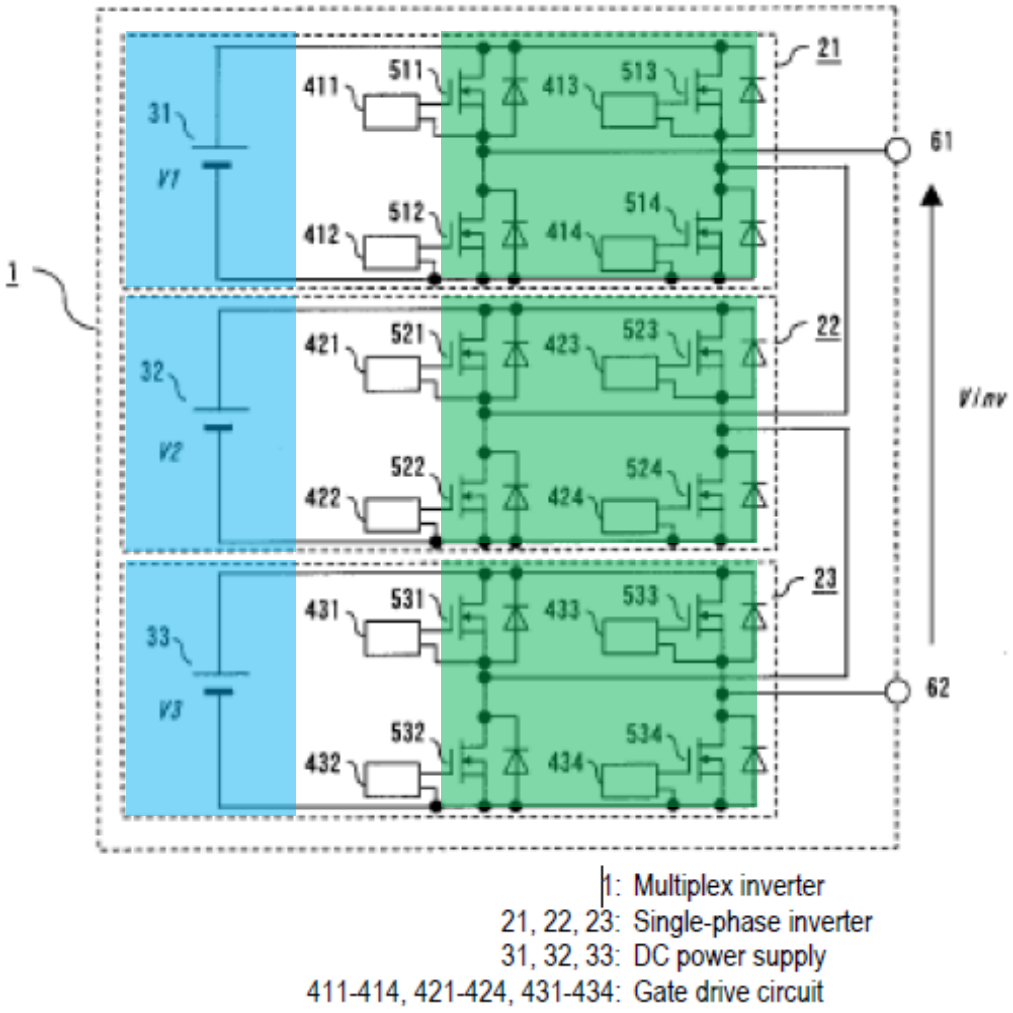
Thus, implementing Iwata's switches with MOSFET switches, as taught by Mori '630, was obvious as the simple substitution of one known element (the transistor H-bridge switches of Iwata) for another (MOSFET H-bridge switches of Mori '630) to obtain predictable results (the switches operate and are controlled in the same fashion). Ex. 1002, ¶ 209. Likewise, this was the use of a known technique (making H-bridge switches out of MOSFETs) to improve a similar device (Iwata's H-bridge switches) in the same way. Ex. 1002, ¶ 210. A PHOSITA would have had a reasonable expectation of success in using Mori '630's MOSFETs because MOSFETs had been used in switches for decades, and Mori '630 teaches how to connect and control MOSFETs in an H-bridge configuration. Ex. 1006, [0009]-[0010]; Ex. 1002, ¶¶ 210, 78-79.

Thus, the combination of Iwata-Bower in view of Mori '630 render obvious claim 4. Ex. 1002, ¶¶ 200-211.

2. Claims 7 and 8

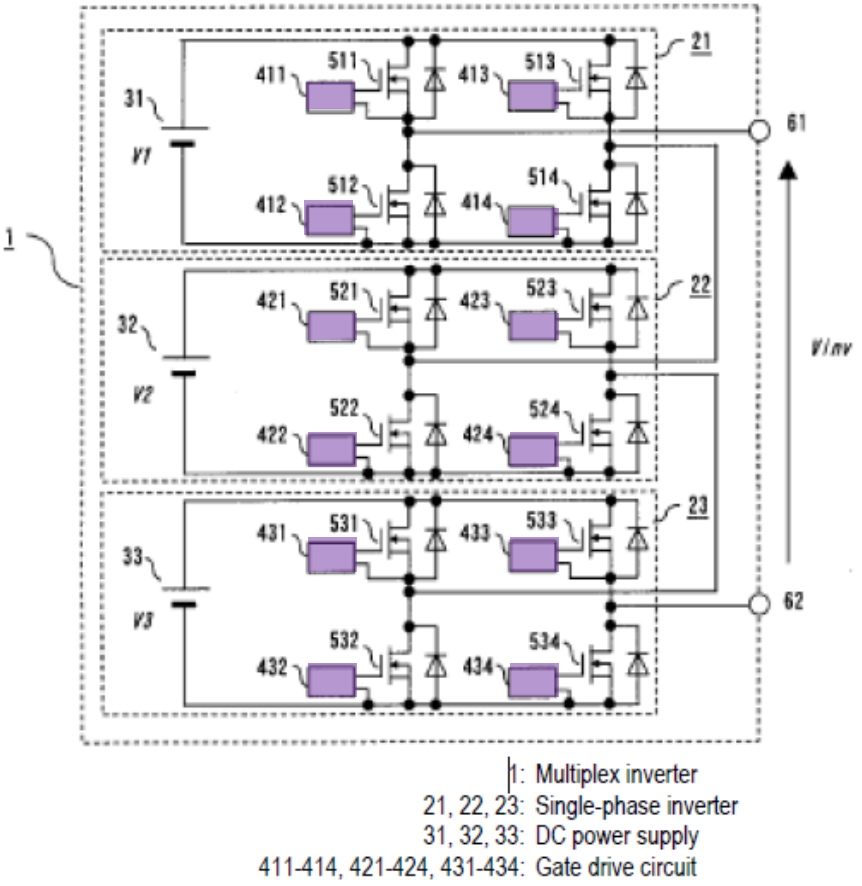
To the extent PO argues that Iwata-Bower does not disclose claims 7 and 8 as shown above in Section VII.A.4, Mori '630 discloses these claims.

Mori '630, like Iwata, teaches an inverter comprising series-connected individual single-phase inverters (**green**) consisting of H-bridges and attached to a respective DC power source (**blue**), as shown below. Ex. 1006, [0009]-[0010], claim 1, Fig. 1; Ex. 1002, ¶ 215.



Ex. 1006, Fig. 1 (annotated)

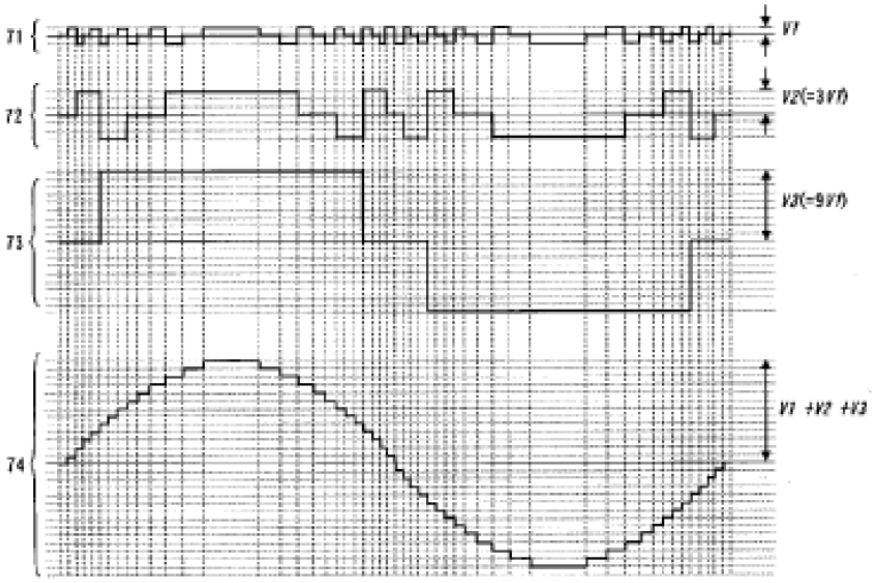
Mori ’630 further describes gate drive circuitry (**purple** below) that applies a predetermined voltage for turning each switch on and off based on a gate drive signal generated by a control circuit (*i.e.*, a “switch signal generator”). Ex. 1006, [0010]-[0011], [0015]-[0033], Figs. 1, 4, 9, 10, 13, 15; Ex. 1002, ¶ 216.



Ex. 1006, Fig. 1 (annotated)

Mori ’630 also teaches this gate control signal is a set of ternary-valued selection signals (*i.e.*, +1, 1, 0) that control the plurality or set of H-bridge switches at given time instants so that the sum output of those switches provides an approximation to the instantaneous voltage values of the desired waveform. Ex. 1006, [0009], [0011]-[0012], [0015], [0018]-[0022], [0029], [Solution]; Ex. 1002, ¶ 217. Figure 2, for example, shows a sum voltage output (74) approximating a desired sinusoidal waveform when H-bridge output voltages V1-V3 are set to 1V,

3V, and 9V, respectively. Ex. 1006, [0011]-[0012], [0019]; Ex. 1004, Abstract, [0050], [0053], [0060]-[0061], [0079], [0085], [0094], Figs. 2, 4; Ex. 1002, ¶ 217.



Ex. 1006, Fig. 2

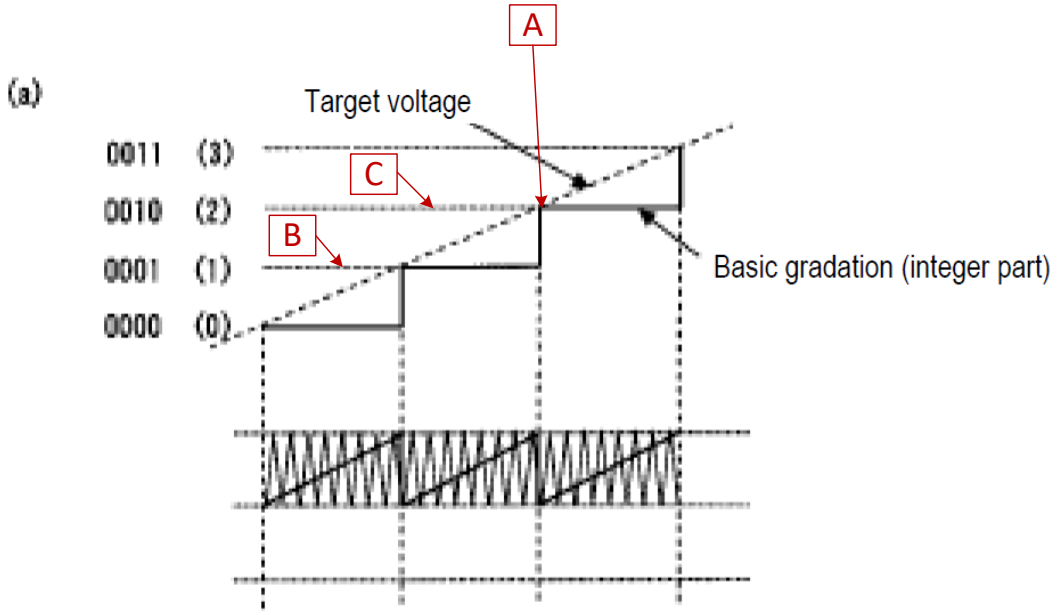
Implementing Iwata, which requires the receipt by the H-bridge switches of control signals to create the three possible states for each H-bridge (*e.g.*, +1, -1, 0), with the control circuit of Mori ’630, which generates that same type of control signal was an obvious combining of prior art elements (the control circuit of Mori ’630 with Iwata’s inverter) according to known methods (using such control signals for H-bridge switches) to yield predictable results (the H-bridges receive the appropriate control signals at the appropriate time to generate a sum output voltage that approximates the desired waveform). Ex. 1002, ¶ 218.

To the extent that the “switch selection signal generator” is a means-plus-function term, it is still met by the proposed combination. As explained above, the

function recited in the claim following the words "configured to" are performed by the proposed combination. Ex. 1002, ¶ 219. To the extent there is corresponding structure in the '710 patent for producing these signals, it is controller 200, which includes a microcontroller, or an equivalent structure that sends the signals to switch driving circuits. Ex. 1001, 12:54-56; 13:45-47, Fig. 1; Ex. 1002, ¶ 219. Mori '630 similarly discloses a control circuit 9, which includes a microcomputer or a microcomputer-based controller that sends signals to gate drive circuits. Ex. 1006, [0010], [0015], Figs. 4, 9, 10, 13, 15; Ex. 1002, ¶ 219. Mori '630's control circuit is the equivalent structure of the '710 patent's switch selection signal generator. Ex. 1002, ¶¶ 219-220. Further, combining Iwata's inverter, which requires control signals to control the states for each H-bridge, with Mori '630's control circuit and its structure, which generates the necessary control signals, is the obvious improvement of a similar device (Iwata's system) in the same way (sending gate drive signals to switch driving circuits). *Id*. A PHOSITA had the skills to implement this known control circuit structure, providing a reasonable expectation of success. *Id*.

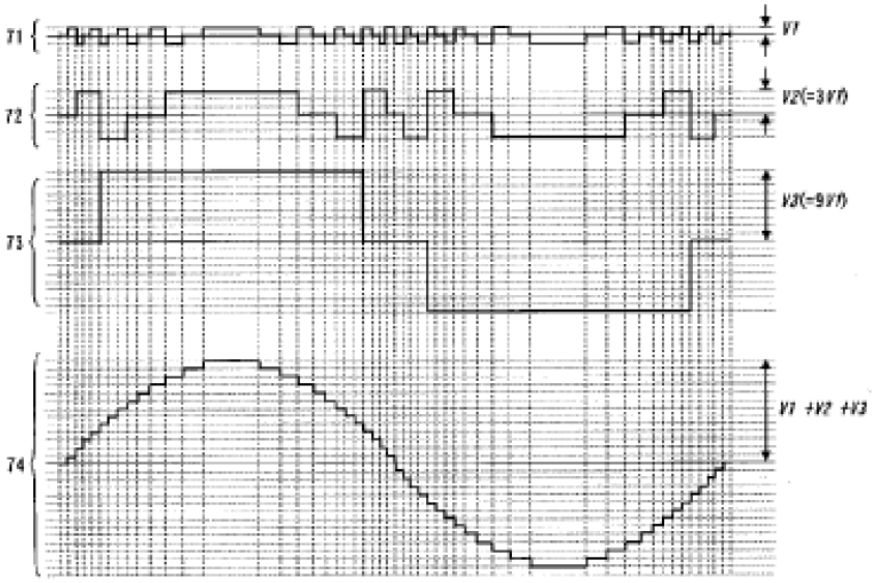
Thus, whether or not "switch selection signal generator" is a means-plus-function term, the combination of Iwata-Bower-Mori '630 discloses it as recited in claims 7 and 8.

Mori ’630 discloses various methods to calculate the sequential sets of control signals. Ex. 1006, [0021]-[0022], [0028]-[0031], Figs. 2, 8, 12, 14; Ex. 1002, ¶ 222. For example, Fig. 8 of Mori ’630 below shows the target voltage (the “desired waveform”) and basic gradation output (the “sum output voltage”), which changes at each time instant (*e.g.*, “A”) to a new value (*e.g.*, “C”) that equals the target voltage, from a previous value (*e.g.*, “B”) that is less than the target voltage so that sum output voltage equals the target voltage at each time instant and further using PWM control to improve the approximation. Ex. 1006, [0020]-[0021]; Ex. 1002, ¶ 222.



Ex. 1006, Fig. 8(a)

As another example, Figure 2 shows a similar result but using only the integer gradation. Ex. 1006, [0012], Fig. 2; Ex. 1002, ¶ 222.



Ex. 1006, Fig. 2

Thus, Mori ’630’s control circuit produces sets of switch selection signals in which “the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants” as in claim 7, and produces sequential sets of switch selection signals in which each “new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals” as in claim 8. Ex. 1002, ¶ 223.

Thus, Iwata-Bower-Mori ’630 renders claims 7 and 8 obvious. Ex. 1002, ¶¶ 212-224.

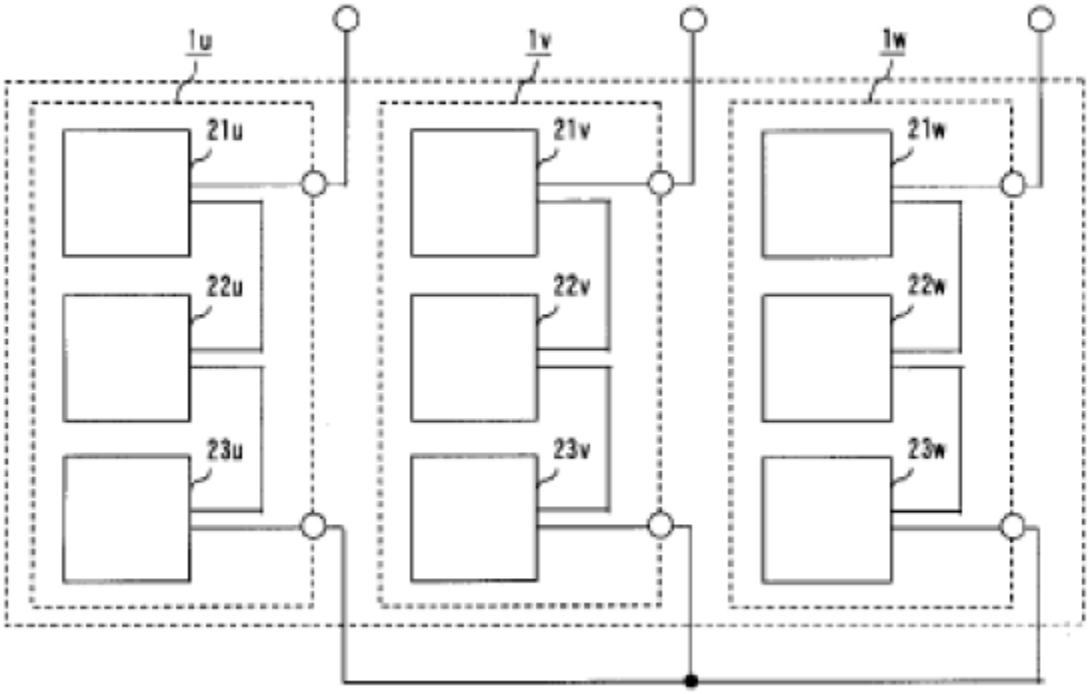
3. Claim 12

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claim 12 depends from claim 1 and requires "one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal." Ex. 1001, claim 12.

As described above in Section VII.A.1, it would have been obvious in view of Iwata-Bower to connect the AC output power of the inverter across a pair of terminals connected to a system or load, with bottom output terminal being "hot" and the top output terminal (connected to the switch with the highest associated DC voltage) being "neutral." To the extent Patent Owner argues otherwise, a PHOSITA would have recognized this implementation to be further obvious in view of Mori '630.

Mori '630 teaches that three of its single phase inverters, which as discussed above are nearly identical to the inverter of Iwata, can be connected in a three phase system as shown in Figure 16 (below). Ex. 1006, [0034]-[0035], Fig. 16. As shown in the figure, the output terminal connected to the 23u, 23v, and 23w H-bridge circuits in the three inverters are connected together at a common point, while the other output terminals of the three inverters are connected to the three "hot" output terminals. *Id.*, Ex. 1002, ¶ 228. A PHOSITA would have understood that the

common connection point is a “neutral”. Ex. 1002, ¶ 228. This is consistent with how the ’710 patent depicts neutral. E.g., Ex. 1001, Fig. 16.



Ex. 1006, Fig. 16

As shown in Fig. 16 of Mori ’630, the “23” H-bridge switch in each of the inverters is connected to the neutral terminal, and is also the switch with the highest associated DC voltage, V_3, as required by claim 12. Ex. 1006, [0002], [0009]-[0012], Fig. 1, 16; Ex. 1002, ¶ 229.

A PHOSITA would have been motivated to connect the single-phase inverter as taught by Iwata-Bower, discussed above with respect to claim 1, with the output of the highest voltage inverter (INV-3B in Iwata) connected to neutral as taught by Mori ’630, in order expand the capability of the Iwata-Bower designs to three-phase

AC systems. For example, such a combination would have been useful for powering three-phase AC loads (*e.g.*, motors) or a three-phase AC utility grid from a plurality of photovoltaic panels that would provide the DC input power. Ex. 1002, ¶ 230. In doing so, Iwata's H-bridge inverter 3B-INV having "the highest associated DC voltage" (V_{3B}) would have been connected to the common "neutral output terminal" as taught in Mori '630 as required by claim 12. Thus, the combination of Iwata-Bower-Mori'630 represents the obvious combination of prior art elements (Iwata-Bower's single phase inverters and Mori's highest-voltage output connected to neutral) in a known manner (making the connections taught by Mori '630) to achieve predictable results (the highest-voltage inverter is connected to neutral). Ex. 1002, ¶ 230.

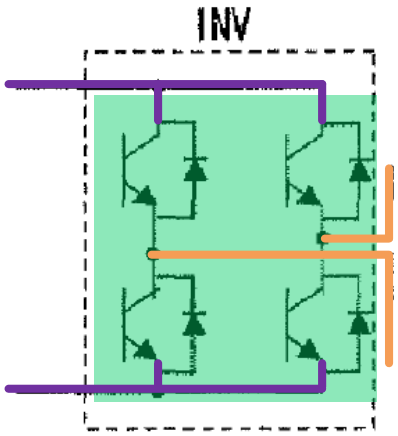
Such a modification was within the skill set of a PHOSITA, providing a reasonable expectation of success, since Mori '630 teaches the exact manner in which to connect the single-phase inverters, which are nearly identical to those of Iwata, in the three-phase configuration having the common neutral. Ex. 1006, Fig. 1, Fig. 16; Ex. 1004, Fig. 1; Ex. 1002, ¶ 231. Moreover, the topology and operation of three single-phase inverters as one three-phase inverter as disclosed in Mori '630 was already a widely-adopted architecture in the art. Ex. 1002, ¶ 231.

Thus, Iwata-Bower-Mori '630 renders obvious claim 12. Ex. 1002, ¶¶ 225-232.

C. Ground C: Claim 6 is Rendered Obvious by Iwata-Bower, in View of Mori '265

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, *supra*. Claim 6 depends from claim 1 and requires "the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value." Ex. 1001, claim 6.

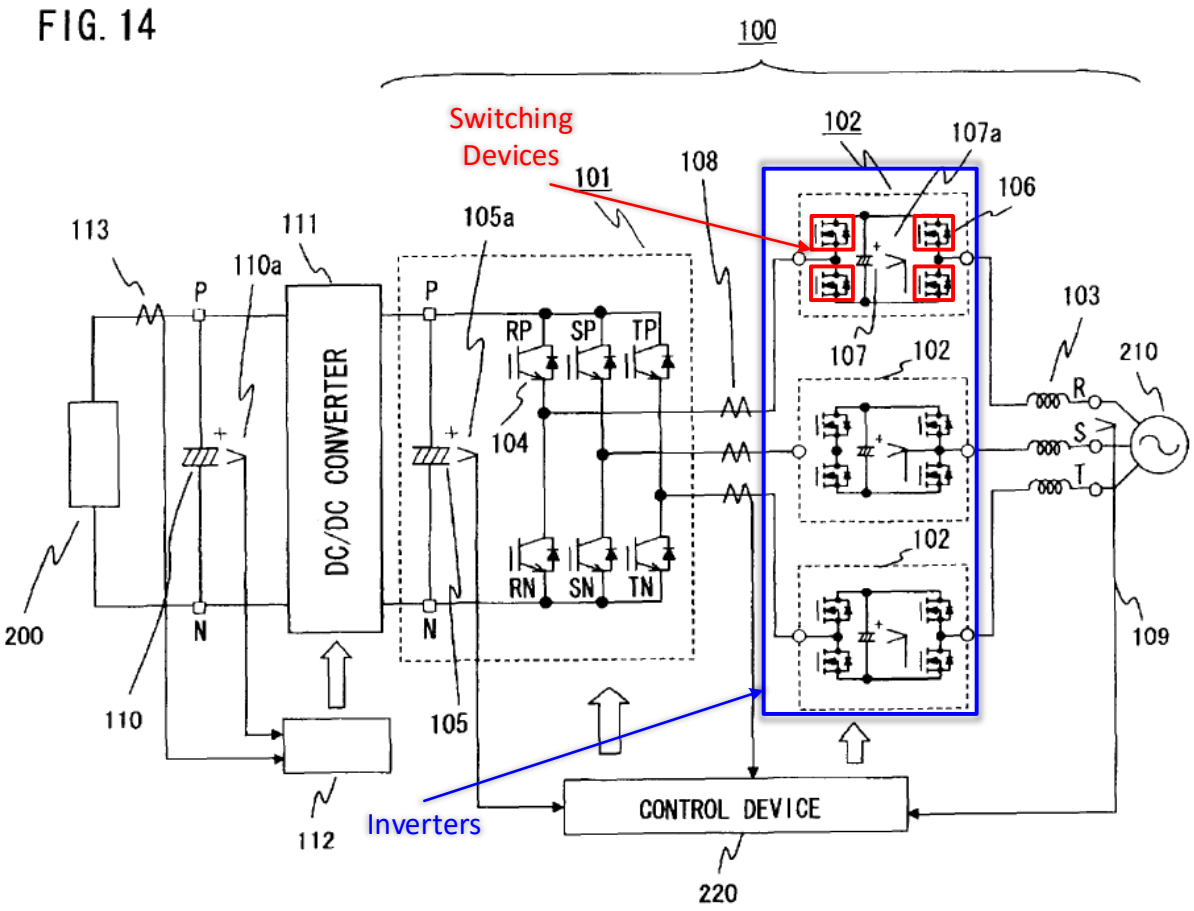
As discussed in Section VII.A.1above, Iwata's H-bridges are controlled such that they output the supply voltage (V), the negative of its supply voltage (-V), or zero volts (0). Ex. 1004, [0047], [0050], Fig. 2(a); Ex. 1002, ¶ 238. As shown in Figure 1(b), the H-bridges are a group of four transistors each receiving a signal (not shown) on its gate, which turns the transistor "on" or "off." By turning only certain transistors on, the H-bridge will be placed in either the "+1", "-1" or "0" states to output the +V, -V, and 0 volts, respectively. Ex. 1002, ¶ 238.



Ex. 1004, Fig. 1(b) (annotated)

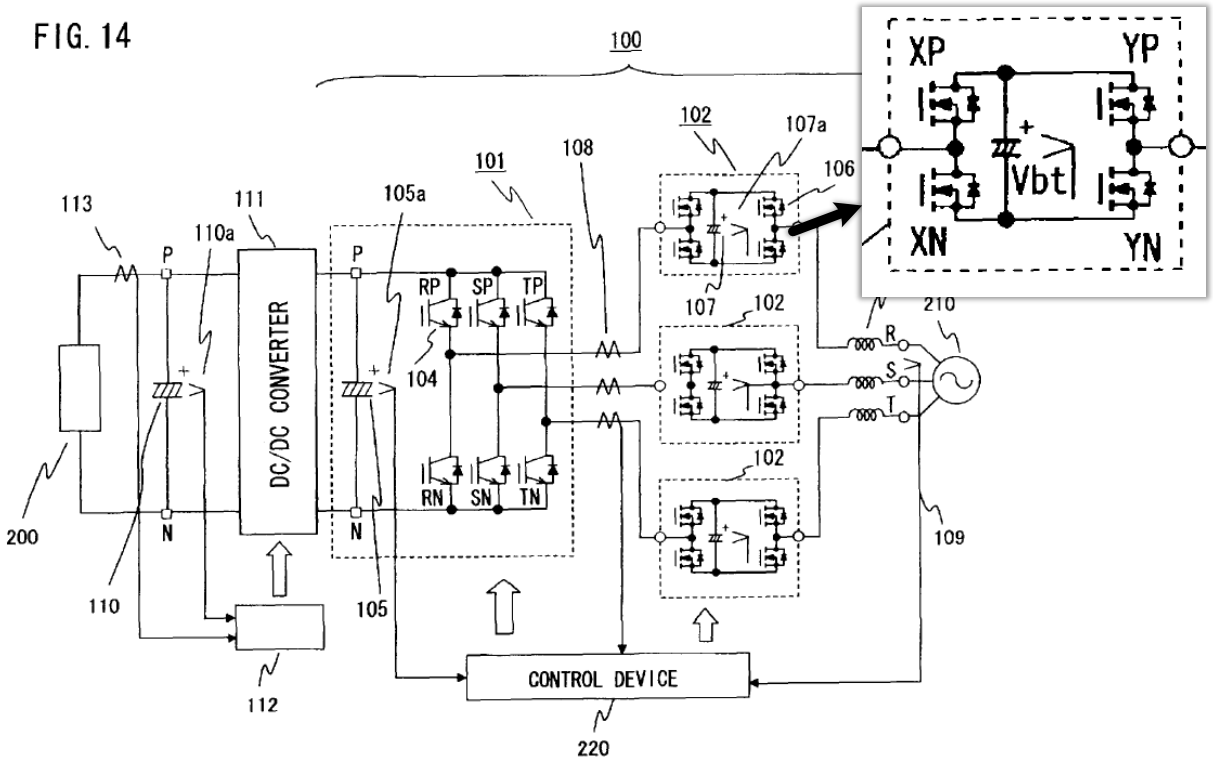
While Iwata discloses that its ternary-valued selection signals control each H-bridge, and thus the four signals controlling the four transistors, Iwata does not explicitly disclose that the ternary-valued selection signals comprise pairs of binary bits as recited in claim 6. Ex. 1002, ¶ 239. However, this was a common control scheme for H-bridge switches, and is disclosed by Mori '265. *Id.*

Mori '265, like Iwata, teaches a power converter that uses H-bridge structures in an inverter to output one of three levels: -V, 0, or +V, based on a combination of ON and OFF states of the transistors in the H-bridge. Ex. 1007, [0011], [0028], [0047]-[0050], Fig. 14 (transistors 106, highlighted below). Ex. 1002, ¶ 240.



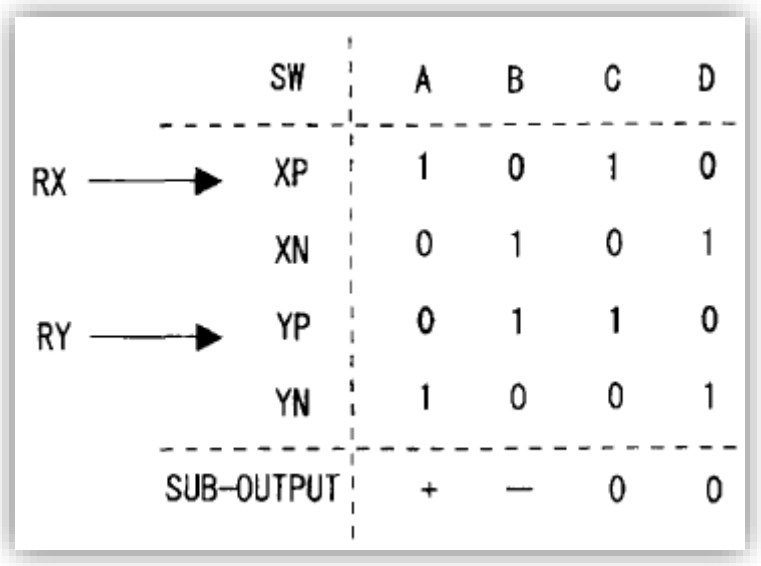
Ex. 1007, Fig. 14 (annotated)

In particular, gate driving signals are sent to the gates of the transistors (XP, YP, XN, YN) of each of the H-bridges, shown in Figs. 1 and 14 below. Ex. 1007, [0031], [0050]. Ex. 1002, ¶ 241.



Ex. 1007, Figs. 1 (excerpted) and 14

The value of the four gate driving signals is determined based on two binary control signals RX and RY (*i.e.*, a pair of "binary bits . . . having in total four combinations of possible values,"). Ex. 1007, [0031], [0050], Fig. 11 (reproduced below). Ex. 1002, ¶ 242.



	SW	A	B	C	D
RX →	XP	1	0	1	0
	XN	0	1	0	1
RY →	YP	0	1	1	0
	YN	1	0	0	1
	SUB-OUTPUT	+	—	0	0

Ex. 1007, Fig. 11

As illustrated in Figure 11, RX may have one of two values such that the first value causes XP and XN to be 1 and 0, respectively, and the second value causes XP and XN to be 0 and 1, respectively. Ex. 1007, [0032]; Ex. 1002, ¶ 243. Likewise, RY may have one of two values such that the first value causes YP and YN to be 1 and 0, respectively, and the second value causes YP and YN to be 0 and 1, respectively. *Id.* Each column (A, B, C, and D) indicates the states of the four switching devices XP, XN, YP, and YN in an H-bridge for each of the four possible combinations of binary values RX and RY. As shown in the last row of the table, one of the combinations (*i.e.*, A) places the H-Bridge into the "+1" state, one of the combinations (*i.e.*, B) places the H-Bridge into the "-1" state, and two of the combinations (*i.e.*, C and D) place the H-bridge into the "0" state, thus disclosing

the claim 6 feature of "two of the four combinations represent the zero multiplier value." Ex. 1002, ¶ 243.

A PHOSITA would have been motivated to use Mori '265's two-bit control signal encoding in Iwata because it is efficient and eliminates superfluous control logic for Iwata's ternary-valued control signal. Ex. 1002, ¶ 244. This is an obvious combination of prior art elements (Iwata's H-bridge switches and Mori '265's two-bit control signal) in a known manner (providing Mori '265's two-bit control signal to control Iwata's H-bridge switches) to achieve predictable results (the H-bridges are controlled to generate four output states: positive, negative, and two zero states). Ex. 1002, ¶¶ 244, 85-86, 102.

This modification was within the skill set of a PHOSITA, who was familiar with H-bridge switches and basic control logic needed to implement the two-bit control signals, providing a reasonable expectation of success. Ex. 1002, ¶ 245.

Thus, the combination of Iwata-Bower in view of Mori '265 renders obvious claim 6. Ex. 1002, ¶¶ 235-246.

D. Grounds D and E: Claim 9 is Rendered Obvious by Iwata-Bower and Iwata-Bower-Mori '630, Each in View of Flanagan

Claim 8 is taught by Iwata-Bower, and Iwata-Bower-Mori '630. Sections VII.A.4, VII.B.2, *supra*. Claim 9 depends from claim 8, and recites: "[the] DC to AC ... further comprising, where the desired waveform is repetitive: memory operative to store precomputed sequential sets of switch selection signals and the

associated time instants at which each set is to be output; and wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times." Ex. 1001, claim 9.

As discussed above in Sections VII.A, VII.B, Iwata-Bower, and Iwata-Bower-Mori '630 teach an inverter that outputs an approximate sinewave (the recited "where the desired waveform is repetitive"). Mori '630's control circuit 9, incorporated into Iwata-Bower-Mori '630, includes a PWM controller implemented with a CPU and PLD, which a PHOSITA would understand to include memory. Ex. 1006, [0015]; Ex. 1002, ¶ 252.

Flanagan also teaches a programmed PWM controller ("switch selection signal generator") for controlling a DC/AC inverter. Ex. 1008, Abstract. Flanagan's inverter is a full-bridge, three-phase inverter with three pairs of inverter switches. Ex. 1008, 4:64-68, Figs. 1, 2. Flanagan teaches a gating signal to control the state of the inverter's individual switches. Ex. 1008, 5:5-8; Ex. 1002, ¶ 253.

Flanagan's PWM controller includes a memory, a cycle counter, an address counter, a comparator, and a clock. Ex. 1008, 5:24-29. The controller outputs a sequence of gating signals (referred to as "drivewords") to the control line to generate the desired inverter output. Ex. 1008, 5:18-23; Ex. 1002, ¶ 254.

Specifically, the controller memory stores a series of drive data words, each of which includes both a driveword for controlling the switch states of the inverter and a drivetime providing timing information within the PWM sequence (the recited "memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output"). Ex. 1008, 5:29-35; Ex. 1002, ¶ 255. The first drive data word (*e.g.*, first driveword and corresponding drivetime) is retrieved from the memory and output onto data buses. Ex. 1008, 5:55-6:35. When the address counter is incremented, the next drive data in the sequence (*e.g.*, the next driveword and corresponding drivetime) are retrieved from the memory and output onto the data buses. *Id*. This procedure is repeated for each drive data word in the PWM sequence (the recited retrieval of "the precomputed sequential sets of switch selection signals and associated time instants from the memory" to "output the switch selection signals at the associated times.") Ex. 1008, 6:35-50; Ex. 1002, ¶ 255.

A PHOSITA would have been motivated to implement Iwata-Bower's or Iwata-Bower-Mori '630's signal generator to include the memory and functionality of Flanagan's programmed PWM controller because using a series of precomputed signals reduces or eliminates the need for processing power dedicated to calculating the signals in real time. Ex. 1002, ¶ 256. This modification represents the combination of prior art elements (the switch selection signal generator of Iwata-

Bower or Iwata-Bower-Mori '630 and the use of Flanagan's programmed controller) in a known manner (programming the signal generator to store and retrieve the precomputed signals using the pre-stored timing sequence) to achieve predictable results (the reliable generation of a series of control signals at the appropriate times). *Id*.

This implementation as described above required nothing more than the use of basic digital logic and memory devices, which a PHOSITA was familiar with, providing a reasonable expectation of success. Ex. 1002, ¶ 257.

To the extent the "switch selection signal generator" is a means-plus-function term in claim 9, Iwata-Mori '630-Flanagan teaches this element for the same reasons described in claim 7. Section VII.B.2, *supra*. Additionally, Flanagan teaches the same, or equivalent memories as disclosed in the '710 patent. Ex. 1002, ¶ 258.

Thus, Iwata-Bower and Iwata-Bower-Mori '630, in combination with Flanagan each render obvious claim 9. Ex. 1002, ¶¶ 249-259.

E. Ground F: Claims 10-11 are Rendered Obvious by Iwata-Bower, in View of Tracy

As explained in Sections VII.A.5, VII.A.6, claims 10 and 11 are taught by Iwata-Bower. Sections VII.A.5, VII.A.6, *supra*. To the extent PO argues the "battery" of claims 10 and 11 is not taught by Iwata-Bower, Tracy discloses the use of a battery (**red**) as a backup power source for an inverter in a uninterruptable power

supply (UPS) as shown in Figure 3 below. Ex. 1009, 1:6-47, 4:50-59, 5:1-6, 5:41-52, 6:46-49, Figs. 1-3; Ex. 1002, ¶ 265.

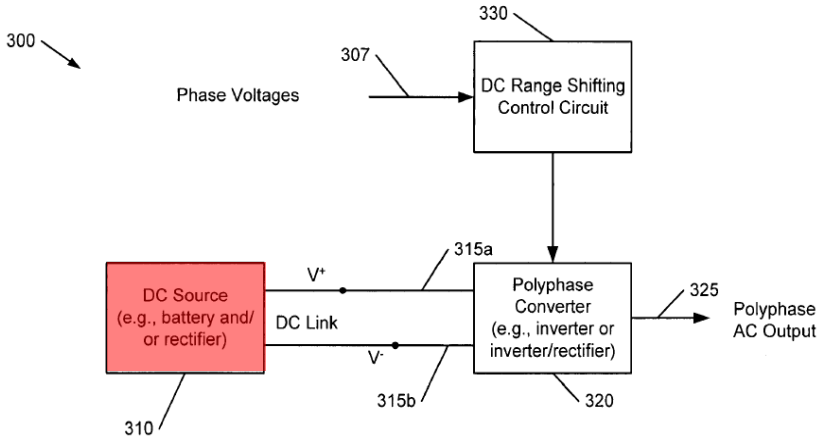


FIG. 3

Ex. 1009, Fig. 3 (annotated)

The use of Tracy's battery as an uninterruptible DC power source in Iwata's inverter was obvious as the simple substitution of one known element (Tracy's battery as an uninterruptible DC power source) for another (Iwata's uninterruptible power source) to yield predictable results (the battery serves as a reliable uninterruptible DC power source having the highest voltage value). Ex. 1004, [0119]; Ex. 1009, 5:41-52, 6:46-49, Figs. 1-3. Ex. 1002, ¶ 266. A PHOSITA was familiar with batteries as beneficial DC power sources for inverters, and had the skills to implement Iwata with a battery as the highest voltage power source. Ex.

1002, ¶ 266. Tracy itself explains that this use of batteries was well known in the art. Ex. 1009, 1:6-47.

Thus, Iwata-Bower, in view of Tracy, renders obvious claims 10 and 11 for the reasons stated above in sections VII.A.5, VII.A.6, and for these further reasons. Ex. 1002, ¶¶ 262-267.

F. Grounds G and H: Claims 10-11 are Rendered Obvious by Iwata-Bower and Iwata-Bower-Tracy, Each in View of Nishimura

To the extent that the "bi-directional DC-DC conversion circuitry" of claims 10 and 11 is a means-plus-function term, Nishimura discloses an equivalent structure. Ex. 1014, Fig. 4, [0091]-[0101]; Ex. 1002, ¶¶ 269, 273. As explained above, the function recited in the claim following the words "operative to" are performed by the proposed combination. Ex. 1002, ¶ 273; Sections VII.A.5, VII.A.6, *supra*. To the extent there is corresponding structure in the '710 patent for deriving the lower voltage values from the battery, it is Figure 2 which includes transformer windings, which have turn ratios in proportion to the voltage ratios wherein the lower voltage windings are center-tapped. Ex. 1001, 19:41-48, 20:9-28, Fig. 2; Ex. 1002, ¶ 273. Nishimura similarly discloses a voltage converting unit, which includes multiple center-tapped windings in proportion to the desired voltages. Ex. 1014, [0070], [0071], Fig. 2; Ex. 1002, ¶ 273. Nishimura's voltage converting unit is the equivalent structure of the '710 patent's bi-directional DC-DC conversion circuitry. Ex. 1002, ¶ 274. Further, implementing Iwata's bidirectional

DC-DC converter with Nishimura's variable windings to produce different DC voltages that are lower than the primary DC power source would be the simple substitution of one known element (Nishimura's voltage converting unit) for another (Iwata's bi-directional DC-DC converter) with predictable results (creation of different DC input voltages for Iwata's switches). *Id*. A PHOSITA had the skills to implement this known circuit structure and would have had a reasonable expectation of success. *Id*.

To the extent "bi-directional DC-DC conversion circuitry" is a means-plus-function term, the combination of Iwata-Bower, and Iwata-Bower-Tracy, each in view of Nishimura renders obvious claims 10 and 11. Ex. 1002, ¶¶ 270-275; Sections VII.A.5, VII.A.6, VII.E, *supra*.

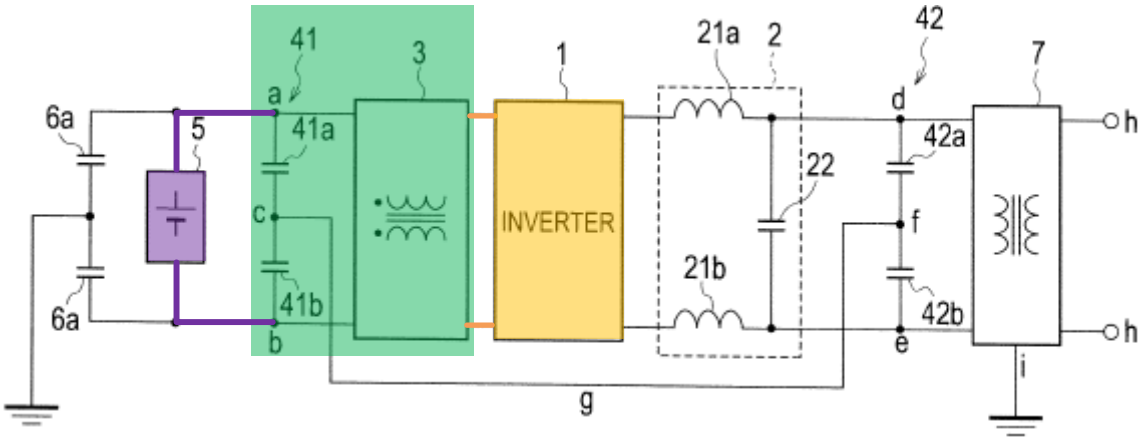
G. Grounds I and J: Claim 13 is Rendered Obvious by Iwata-Bower and Iwata-Bower-Tracy, each in view of Koyama

Claim 1 is taught by Iwata-Bower. Section VII.A.1, s*upra*. Claim 13 depends from claim 1 and requires "the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch." Ex. 1001, claim 13; Ex. ¶¶ 278-280.

As explained above with respect to claims 10 and 11, Iwata-Bower and Iwata-Bower-Tracy each teach using a battery (*e.g.*, in a UPS) as the DC power source 2 for Iwata's inverter, which is also the DC power source for Iwata's 3B-INV H-bridge (controlled switch). Ex. 1004, [0119]; Ex. 1009, 1:6-47, 5:41-52, 6:46-49, Figs. 1-

3; Ex. 1002, ¶ 281. These combinations as disclosed above thus teach "wherein the associated DC power source of one of the controlled switches is a battery." Section VII.A.5, VII.A.6, VII.E, *supra*.

Koyama further includes a common mode filter (**green**) interposed between an inverter 1 (**orange**) and a floating DC power source 5 (**purple**), such as between Iwata's inverter 1 and DC power source 2, as further recited in claim 13. Ex. 1013, [0005]-[0007], [0012]-[0013], [0024]-[0026], [0030]-[0031], [0036]-[0038], Figs. 1, 4, 5; Ex. 1002, ¶ 277, 282.



Ex. 1013, Fig. 5 (annotated).

Koyama explains that floating DC power sources (described as a solar cell, fuel cell, or battery) may include stray capacitances 6 between the terminals of the DC power source and ground, which can provide a path for common mode leakage current. Ex. 1013, [0012]-[0013], [0002]-[0003], [0016]-[0018], [0026], [0036]-[0038], Figs. 1, 4, 5; Ex. 1002, ¶ 283. Moreover, common mode noise generated by

the inverter may cause impermissible EMI. Ex. 1002, ¶ 284. A PHOSITA would have been motivated to add Koyama's common mode filter between the floating battery (*e.g.*, of Iwata's or Tracy's UPS battery and other DC power sources) and Iwata's inverter (including the 3B-INV H-bridge) to suppress common-mode currents and minimize EMI. Ex. 1013, [0012]-[0013], [0019]-[0021]; Ex. 1002, ¶ 284.

Iwata-Bower, and Iwata-Bower-Tracy, each combined with Koyama, which disclose claim 13 as described above, represents the obvious use of a known technique (inserting Koyama's common mode filter between a power source and inverter) to improve a similar device (Iwata's inverter fed by Iwata's or Tracy's battery) in the same way (by suppressing the common mode current and EMI). The combination merely requires inserting filter components and adjusting component values, which was well within the skill of a PHOSITA. Ex. 1002, ¶¶ 285-286.

H. Grounds K, L, M, and N: Claims 14-15 are Rendered Obvious by Iwata-Bower, Iwata-Bower-Tracy, Iwata-Bower-Mori '630, and Iwata-Bower-Tracy-Mori '630, All in view of Koyama and Ahmed

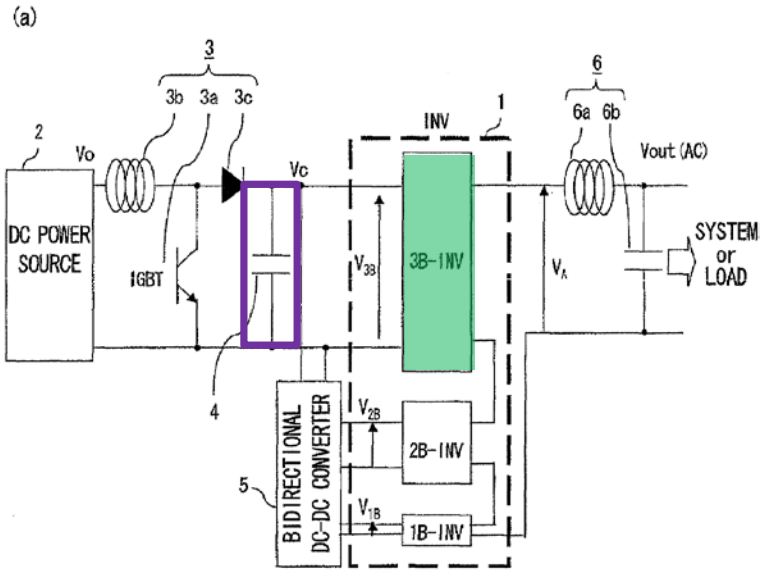
Claim 12 is taught by Iwata-Bower and Iwata-Bower-Mori '630 (Grounds A and B). Sections VII.A.7, VII.B.3, s*upra*. Claim 14 depends from claim 12, and claim 15 depends from claim 14. Claims 14 and 15 recite specific circuit components of "the common mode filter" connected between "DC power input terminals of the controlled switch" and "the battery," but there is no antecedent

common mode filter or battery in claim 12, from which claims 14 and 15 depends. Ex. 1002, ¶ 293. Regardless, as explained below, Iwata-Bower and Iwata-Bower-Mori '630, each alone or in view of Tracy, and further in view of Koyama and Ahmed render claims 14 and 15 obvious. Ex. 1002, ¶¶ 290-303.

As explained above with respect to claim 13, it was obvious to connect Koyama's common mode filter between a DC power source (a battery as disclosed in Iwata or Tracy) and the Iwata inverter to reduce the common mode leakage current and EMI emitted by the inverter in the Iwata-Bower (Ground A) and Iwata-Bower-Tracy (Ground F) combinations. Section VII.A, VII.E, *supra*. Iwata-Bower-Mori '630 (Ground B) is identical to Iwata-Bower (Ground A) with respect to the connection between the DC power source and the input to the inverter, and thus it would have been obvious to combine Koyama alone (or Koyama and Tracy) with Iwata-Bower-Mori '630 (Ground B) in the same way and for the same reasons discussed above with respect to Iwata-Bower-Tracy (Ground F) (combining Tracy's battery with Iwata's inverter), and Iwata-Bower-Koyama and Iwata-Bower-Tracy-Koyama (Grounds I and J) (combining Koyama's common mode filter between the battery and Iwata's inverter). Sections VII.A, VII.B, VII.E, VII.G *supra*. Ex. 1002, ¶ 294.

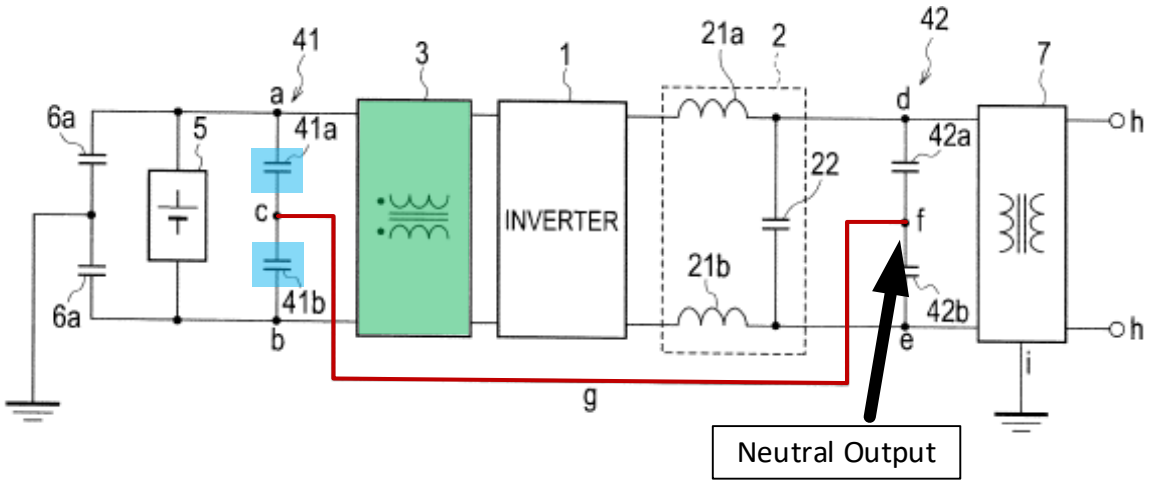
Further, Iwata and Koyama, combined with Ahmed, teach the common mode filter structures of claims 14 and 15. As shown below, Iwata teaches (in **purple**) the

claim 14 “capacitor connected between DC power input terminals of a controlled switch” (in **green**). Ex. 1004, [0045], [0048], [0058], Figs. 1, 4, 14, 16-18; Ex. 1002, ¶ 295.



Ex. 1004, Fig. 1(a) (annotated)

Koyama, as shown below discloses the claim 14 “common-mode choke” [**green**] connected between a DC power source 5 (*e.g.*, Iwata’s or Tracy’s battery) and the DC power input terminals of the controlled switch 1 (*e.g.*, Iwata’s 3B-INV H-bridge). Ex. 1013, [0029], [0036]-[0038], Figs. 4-5. Ex. 1002, ¶ 296.



Ex. 1013, Fig. 5 (annotated).

Koyama also teaches the claim 14 "first pair capacitors [**blue**] connected respectively from positive and negative terminals of the battery [*e.g.*, Iwata's or Tracy's Battery as DC power source 5] to the neutral output terminal [Iwata's, Bower's, or Mori '630's neutral output terminal as AC neutral point f]." Ex. 1013, [0024]-[0026], [0030]-[0031], [0035]-[0038], Figs. 4-5; Ex. 1002, ¶ 297.

Ahmed teaches to modify Koyama's first pair of capacitors to add a damping circuit meeting the remaining claim 14 and 15 limitations. Specifically, Ahmed identifies the problem in filters such as the one disclosed in Koyama of resonance between inductors and capacitor components, which may lead to ringing, voltage overshoot and instability at particular resonant frequencies. Ex. 1012, Abstract, 6; Ex. 1020, [0018]-[0019], [0027]; Ex. 1002, ¶ 298. To reduce this resonance, *e.g.*, Ahmed teaches that an LC filter as shown on the left in the figures below can be modified by adding a series-connected resistor and capacitor (**blue**), or additionally

modified with an additional inductor in parallel with the resistor (**green**). Ex. 1002, ¶ 298.

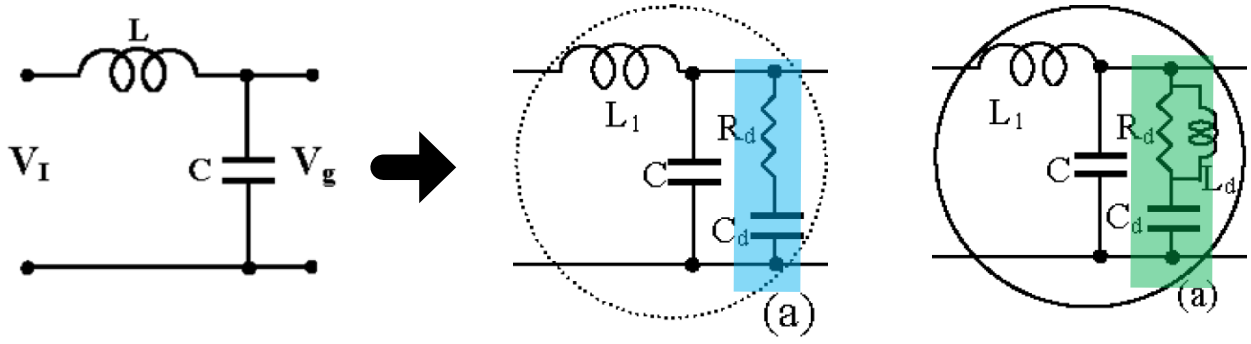
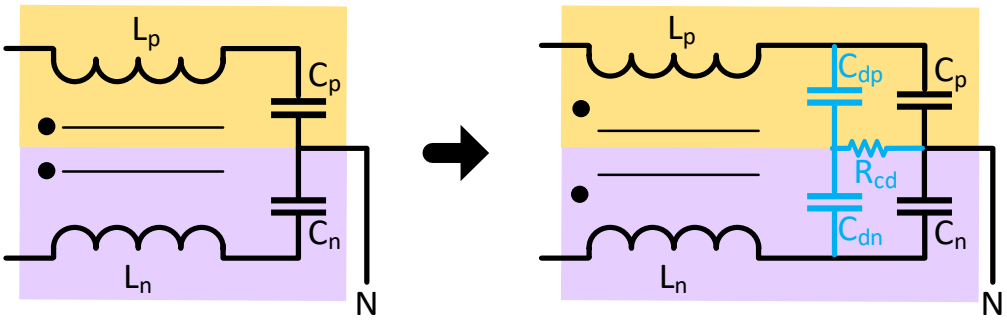


Fig. 2(b) (excerpt) Fig. 14(a) (excerpt) Fig. 15(a) (excerpt)

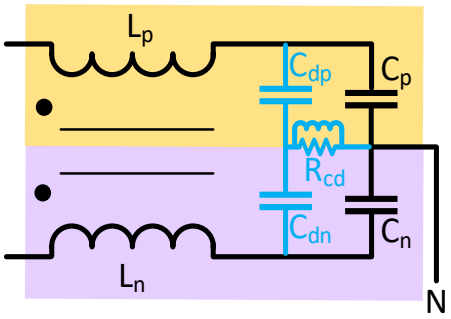
Ex. 1012, Figs. 2(b), 14(a), 15(a) (excerpted and annotated)

A PHOSITA at the time would have understood how to apply these damping techniques taught to the equivalent common mode versions of these filters, which are illustrated below. Ex. 1002, ¶ 299.



In the left figure, the common mode LC filter disclosed in Koyama includes a top half (**orange**) and a bottom half (**purple**). Each half is analogous to the filter illustrated in the Ahmed Figure 2(b) above having a single series inductor and a capacitor connected between the power line (positive or negative) and neutral. A

PHOSITA would have understood that each half of the common mode filter would be modified according to the teachings of Ahmed to add a capacitor (C_{dp} and C_{dn}) analogous to C_d in Figure 14(a) connected through a resistor R_{cd} to neutral, where R_{cd} is the parallel equivalent of two resistors R_d in Ahmed Figure 14(a), one for each half of the common mode filter (shown above). Similarly, Ahmed teaches to add an inductor analogous to L_d in Figure 15a in parallel with R_{cd}, as shown below. Ex. 1002, ¶ 300.



Koyama as modified by Ahmed above, thus discloses the claim 14 "damping resistor connected to the neutral output terminal; and a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal," and the claim 15 "inductor connected in parallel with said damping resistor." Ex. 1002, ¶ 301.

Using Ahmed's damping circuits as described above to modify Koyama's common mode filter would reduce resonance in the filter. The addition of the inductor in parallel with damping resistor provides the additional benefit of reducing power dissipation of the damping circuit. Ex. 1012, 7, 9; Ex. 1002, ¶ 302. As such,

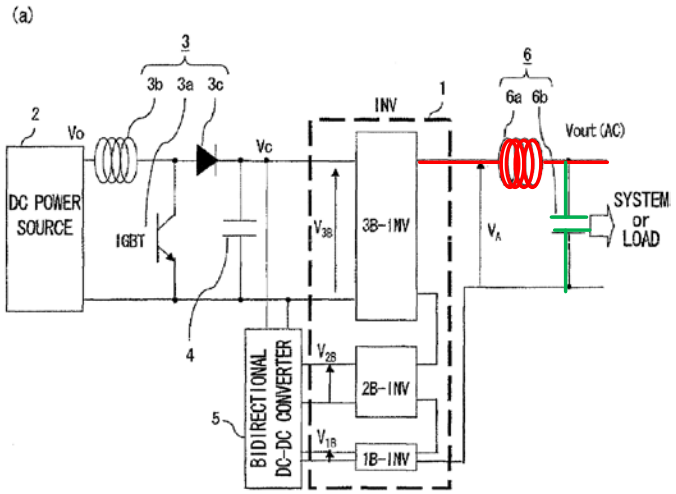
these combinations which disclose all of the features of claims 14 and 15, represent the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Koyama's common mode LC filter) in the same way (by suppressing the resonance between the choke and capacitors and reducing power dissipation of the damping resistor). A PHOSITA was familiar with designing passive LC filter circuits, and would have had the skills to do so, resulting in an expectation of success. Ex. 1002, ¶¶ 302-303.

I. Ground O: Claim 16 is Rendered Obvious by Iwata-Bower, in View of Ahmed

Claim 1 is taught by Iwata-Bower. Section VII.A.1, *supra*. Claim 16 depends from claim 1 and requires "a low-pass output filter comprising: an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal; a first capacitor connected across the hot and neutral output terminals; a damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." Ex. 1001, claim 16; Ex. 1002 ¶¶ 304-307.

Iwata-Bower discloses a low-pass filter comprising an inductor (**red**) connected between the sum voltage at the end of the series connection of switches and what can be the hot output terminal, and a first capacitor (**green**) connected

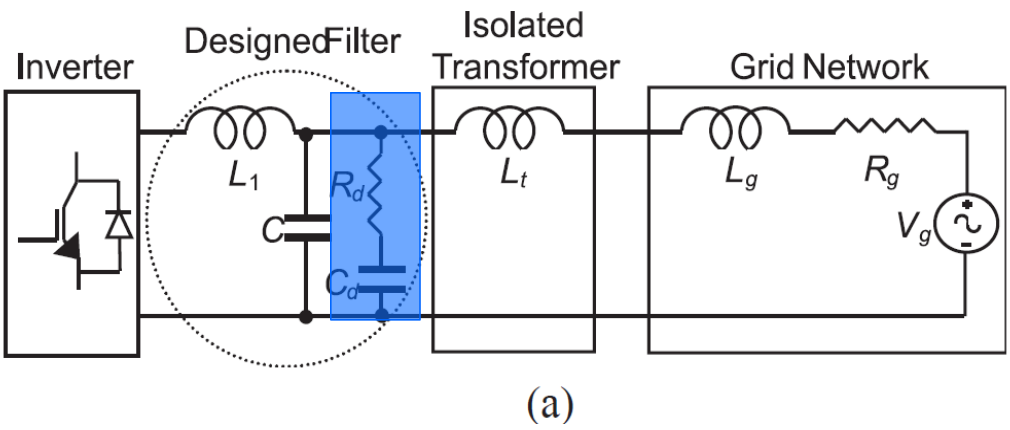
across the hot and neutral output terminals. Ex. 1004, [0003], [0047], [0101], Figs. 1, 7, 14, 16-18; Ex. 1002, ¶ 308. *See* Section VII.A.1.c.



Ex. 1004, Fig. 1(a) (annotated)

As discussed above in relation to claim 1, it was obvious for the top output terminal connected to the inductor in Iwata and Iwata-Bower to be the hot terminal as required by claim 16. Ex. 1002, ¶ 309; Section VII.A.1, *supra*.

Ahmed teaches to modify Iwata's low pass filter to include the remaining claim 16 elements. Ahmed discloses that LC filters can resonate, causing instability in the system, and adds a damping circuit (blue) with a resistor connected in series with a capacitor across the grid terminals (shown below) to attenuate those effects. Ex. 1012, 6-9 Figs. 1, 14; Ex. 1002, ¶ 310.



Ex. 1012, Fig. 14(a) (annotated)

A PHOSITA would have recognized that connecting the capacitor and series resistor in reverse order makes no functional difference (which is also how they are oriented in Figure 8 of the '710 Patent). Thus, Ahmed teaches the claim 16 "damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." Ex. 1002, ¶ 311.

Modifying Iwata's low pass filter by adding Ahmed's damping RC circuit would reduce unwanted resonance effects. Ex. 1012, 6-9; Ex. 1002, ¶ 312. As such, the combination of Iwata-Bower with Ahmed, which disclose all of the limitations of claim 16, represents the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Iwata's output LC filter) in the same way (by suppressing the resonance between the inductor and capacitor). A PHOSITA was familiar with filtering the output from inverters, and

would have had the skills to do so, resulting in an expectation of success. Ex. 1002, ¶¶ 312-313.

J. Ground P: Claim 17 is Rendered Obvious by Iwata-Bower, in View of Phadke

Claim 1 is taught by Iwata in view of Bower. Section VII.A.1, s*upra*. Claim 17 depends from claim 1 and requires:

> "a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
>
> one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source to the controlled switch when the in-rush current has dropped below a threshold."

Ex. 1001, claim 13.

Iwata does not disclose claim 17's start-up in-rush current limiting circuit, but Phadke does. As shown below, Phadke discloses DC to DC converters (**blue**) attached between photovoltaic (PV) arrays (**red**) to provide power sources for an inverter (**green**). Ex. 1015, 1:14-16, 3:57-65, 4:32-41, 4:66-5:6; Ex. 1002, ¶ 321.

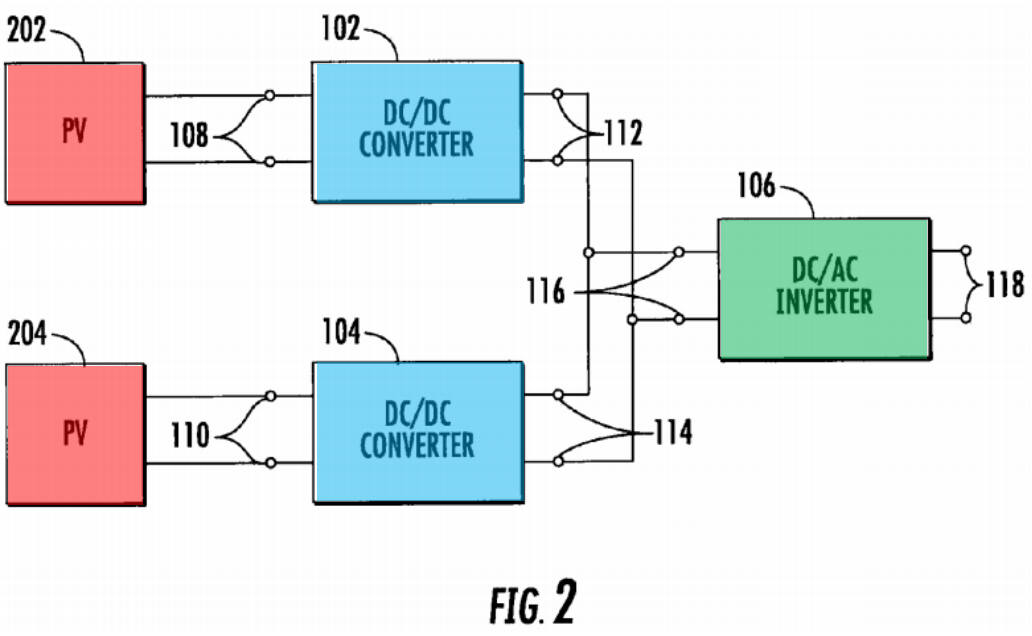


FIG. 2

Ex. 1015, Fig. 2 (annotated)

Within the DC to DC converters, Phadke discloses the use of two stages with a switch 608 and resistor 606 inserted in parallel between the two stages, as shown in Figure 6 below. Ex. 1002, ¶ 322.

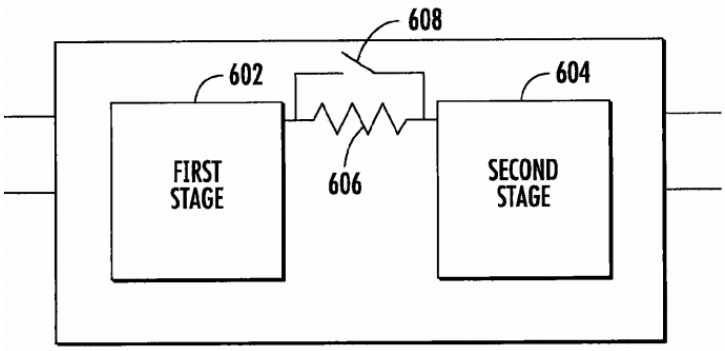


FIG. 6

Ex. 1015, Fig. 6

During the circuit's startup or to protect the circuit from damage before a load is connected correctly, Phadke discloses that switch 608 is held open so that resistor

606 (“a series impedance”) is inserted to provide a high resistance path, limiting current flow to the second stage. Ex. 1015, 7:1-8, 7:19-27, *see also* 8:20-34, Fig. 7; Ex. 1002, ¶ 323. Once a certain threshold of current or voltage is reached, switch 608 is closed, thus removing any impedance between the two stages by effectively shorting resistor 606. Ex. 1015, 7:8-11, 8:44-56. Thus, Phadke discloses the “start-up in-rush current limiting circuit” of claim 17. Ex. 1002, ¶ 323.

It was obvious to use Phadke’s startup circuit between one of Iwata’s power sources and the controlled H-bridge switches. This would have been combining known elements (Phadke’s startup circuit and Iwata power sources providing power to its H-bridge switches) according to known methods (inserting the startup circuit between the power source and inverter as taught in Phadke) to yield predictable results (protecting Iwata’s H-bridge circuitry by limiting the amount of current entering the switches during startup). Ex. 1002, ¶ 324. A PHOSITA was familiar with startup circuits, and would have had the skills to insert one between a power source and a switch, resulting in an expectation of success. Ex. 1002, ¶¶ 324, 106.

Iwata-Bower in view of Phadke renders claim 17 obvious. Ex. 1002, ¶¶ 318-325.

VIII. CONCLUSION

Inter partes review should be instituted and claims 1-17 canceled. Ex. 1002, ¶¶ 326-328.

Dated: October 8, 2021

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282
Customer No. 115801
Banner & Witcoff, Ltd.
1100 13th Street, NW
Suite 1200
Washington, DC 20005
(202) 824-3000
(202) 824-3001
fmeeker@bannerwitcoff.com

CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,930, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,822 words as counted by the Word Count feature of Microsoft Word and 108 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: October 8, 2021

By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282
Customer No. 115801
Banner & Witcoff, Ltd.
1100 13th Street, NW
Suite 1200
Washington, DC 20005
(202) 824-3000
(202) 824-3001
fmeeker@bannerwitcoff.com

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of the Petition for *Inter Partes* Review in connection with U.S. Patent No. 10,784,710 and supporting evidence to be served via FedEx Priority Overnight on October 8, 2021, on the following:

COATS & BENNETT, PLLC (24112)
1400 CRESCENT GREEN, SUITE 300
CARY, NC 27518

An electronic courtesy copy is concurrently being e-mailed to the following:

RLEMISCH@KLEHR.COM
AARON@APB-LAW.COM
BBOERMAN@SHERIDANROSS.COM
MMILLER@SHERIDANROSS.COM
MISHELE@APB-LAW.COM
PSCHA@SHERIDANROSS.COM
RBRUNELLI@SHERIDANROSS.COM
SBRENNECKE@KLEHR.COM

Dated: October 8, 2021 By: /Frederic M. Meeker/

Frederic M. Meeker
Reg. No. 35,282

CLAIM LISTING APPENDIX

U.S. Pat. No. 10,784,710

Designation	Claim Language
Claim 1	
[1A]	1. A DC to AC converter having
[1B]	a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,
[1C]	and to output the AC power between hot and neutral output terminals,
[1D]	the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and
[1E]	each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,
[1F]	the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform.
Claim 2	
2	2. The DC to AC converter of claim 1 wherein at least some of the DC voltages associated with the plurality of controlled switches have different values.
Claim 3	
3	3. The DC to AC converter of claim 1 wherein the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household electricity supply frequency.
Claim 4	
4	4. The DC to AC converter of claim 1 wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals.
Claim 5	

Designation	Claim Language
5	5. The DC to AC converter of claim 1 wherein each associated DC voltage differs from another DC voltage nominally by a factor of 3.
Claim 6	
6	6. The DC to AC converter of claim 1 wherein the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value.
Claim 7	
[7A]	7. The DC to AC converter of claim 1 further comprising:
[7B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sets of switch selection signals, at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants.
Claim 8	
[8A]	8. The DC to AC converter of claim 1 further comprising:
[8B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sequential sets of switch selection signals, and being configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals.
Claim 9	
[9A]	9. The DC to AC converter of claim 8 further comprising, where the desired waveform is repetitive:
[9B]	memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output; and
[9C]	wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times.

Designation	Claim Language
Claim 10	
10	10. The DC to AC converter of claim 1 wherein the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery.
Claim 11	
11	11. The DC to AC converter of claim 1 wherein the DC power source supplying the highest mean power is a battery and the DC power sources supplying lower mean power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery.
Claim 12	
12	12. The DC to AC converter of claim 1 wherein one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal.
Claim 13	
13	13. The DC to AC converter of claim 1 wherein the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch.
Claim 14	
[14A]	14. The DC to AC converter of claim 12 wherein the common mode filter comprises:
[14B]	a capacitor connected between DC power input terminals of the controlled switch;
[14C]	a common-mode choke connected between the battery and the DC power input terminals of the controlled switch;
[14D]	a first pair capacitors connected respectively from positive and negative terminals of the battery to the neutral output terminal;
[14E]	a damping resistor connected to the neutral output terminal; and
[14F]	a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal.
Claim 15	

Designation	Claim Language
15	15. The DC to AC converter of claim 14 further comprising an inductor connected in parallel with said damping resistor.
Claim 16	
[16A]	16. The DC to AC converter of claim 1 further comprising a low-pass output filter comprising:
[16B]	an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal;
[16C]	a first capacitor connected across the hot and neutral output terminals;
[16D]	a damping resistor connected to the neutral output terminal; and
[16E]	a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal.
Claim 17	
[17A]	17. The DC to AC converter of claim 1 further comprising a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
[17B]	one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source to the controlled switch when the in-rush current has dropped below a threshold.