UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SOLAREDGE TECHNOLOGIES LTD.,
Petitioner,

v.

KOOLBRIDGE SOLAR, INC.,
Patent Owner.

Patent No. 10,784,710
Filing Date: August 14, 2017
Issue Date: September 22, 2020
Title: TRANSFORMERLESS DC TO AC CONVERTER

Inter Partes Review No.: IPR2022-00014

PETITION 2 OF 3 FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq*.

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Ex. 1136:	U.S. Patent No. 6,112,158 (“Bond”)
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Ex. 1138:	U.S. Patent No. 7,046,534 (Schmidt)
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SolarEdge Technologies Ltd ("Petitioner") petitions for *inter partes* review and cancellation of claims 1-17 of U.S. Patent No. 10,784,710 ("the '710 patent") (Ex. 1101).

I. MANDATORY NOTICES

A. 37 C.F.R. § 42.8(b)(1)&(2): Real Parties in Interest & Related Matters

The real party-in-interest is Petitioner SolarEdge Technologies Ltd. No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

The '710 patent has been asserted against SolarEdge in the District of Delaware in *Koolbridge Solar, Inc. v. SolarEdge Technologies, Inc.*, No. 1:20-cv-01374-MN (D. Del.). The earliest date of service on SolarEdge was October 12, 2020. The Patent Owner ("PO"), after having been notified of Petitioner's intent to against the '710 Patent, voluntarily dismissed its lawsuit without prejudice.

The references relied upon herein were not cited during prosecution. No arguments presented in this Petition were raised during prosecution of the '710 patent.

B. 37 C.F.R. § 42.8(b)(3)&(4): Lead & Back-Up Counsel, and Service Information

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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II. COMPLIANCE WITH THE REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Payment of Fees

The undersigned authorizes the charge of any required fees to Deposit Account No. 19-0733.

B. Grounds for Standing

Petitioner certifies that the ’710 patent is available for review and that Petitioner is not barred or estopped from requesting review challenging claims 1-17.

III. SUMMARY OF ARGUMENT

U.S. Patent No. 10,784,710 (“the ’710 patent”) describes a well-known inverter, a device that converts “direct-current” (DC) electrical power (a type of power received from a battery and/or solar panel) to “alternating-current” (AC) electrical power (a type of power used in a home). The type of inverter claimed uses multiple DC supply voltages as inputs and sums these voltages together in different combinations over a time sequence to approximate a desired AC sinusoid wave. The inverter connects the DC supply voltages to the inputs of a plurality of “reversing switches” (also called “H-bridges”). Each switch is controlled to output either: (1) its DC supply voltage, (2) its DC supply voltage with negative polarity, or (3) zero volts. This is called “ternary” control, since the switches are controlled to be placed into one of three states: the +1, -1, or 0 state. The switch outputs are connected in series, and via control of the switch states their sum output voltage gradually steps up and down to generate a sequence of voltages approximating the sine wave.

At the time the ’710 patent application was filed in 2011, such inverters and the concepts behind their design and implementation were well-known. Ex. 1102, ¶¶ 61-106. Suzuki (Japanese Patent Application Publication No. 2004-7941, Ex.

1126), which is relied upon in this petition, is just one example of prior art disclosing the structure of the '710 patent. The dependent claims challenged herein add only obvious features that were also in the prior art and are taught in Suzuki and additional secondary references relied on herein.

Accordingly, claims 1-17 of the '710 patent are unpatentable and should be cancelled.

IV. OVERVIEW OF THE '710 PATENT

A. Brief Description

Figure 1 of the '710 patent (annotated below) illustrates a top-level block diagram of the claimed inverter.

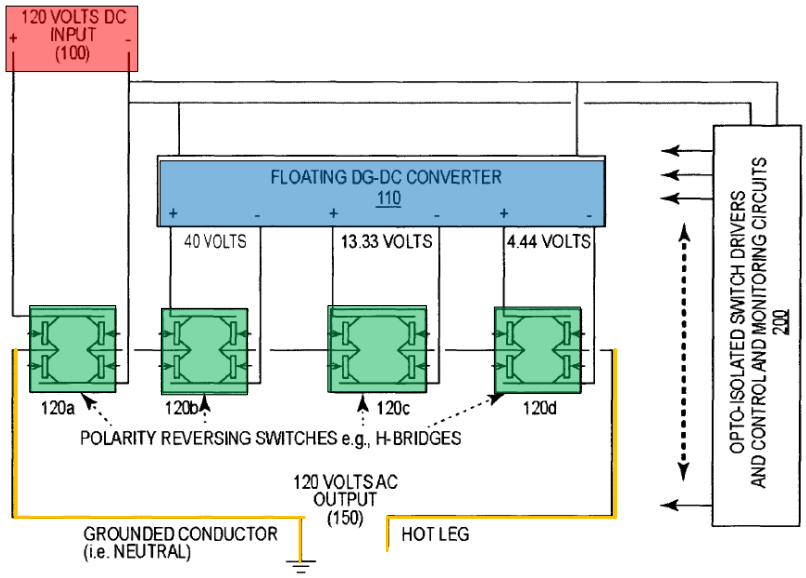


FIG. 1

Ex. 1101, Fig. 1 (annotated)

As shown above, the inverter has a 120V DC input (**red**) and a 120V AC output (**yellow**). Ex. 1101, 1:18-23, 2:41-43, 4:11-29, 5:41-52, 6:65-7:7, 7:57-65,

8:18-20; Ex. 1102, ¶ 93. This output is identified in the patent as being "transformerless," to distinguish it from inverters that couple their switches to the AC output using electrical transformer(s). Ex. 1103, pp. 294-296. The inverter also includes a bidirectional DC-DC converter (**blue**) that converts the DC input voltage to three additional DC voltages—40V, 13.33V, and 4.44V. Ex. 1101, 3:61-4:10, 6:65-7:7, 15:12-19, 16:30-32, 19:36-50; Ex. 1102, ¶ 94. The 120V, 40V, 13.33V, and 4.44V DC voltages are respectively connected to inputs of four "polarity reversing switches" (H-bridges) 120a, 120b, 120c, and 120d (**green**). Ex. 1101, Abstract, 3:61-4:10, 5:41-52, 6:65-7:7, 7:31-42, 10:16-23, 15:17-19, 19:36-38, Fig. 2. Each switch can be controlled based on a ternary control signal to apply a multiplier of +1, -1, or 0 to the input voltage. Ex. 1101, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 6:65-7:7, 7:23-28, 8:33-54; Ex. 1102, ¶ 95-96. A control value of +1 causes the DC supply at the switch input to be connected with the switch output resulting in the DC supply voltage being output from the switch with a positive polarity. A control value of -1 causes the DC supply at the switch input to be connected in reverse polarity to the switch output resulting in the DC supply voltage being output from the switch with a negative polarity. A control signal of 0 causes the DC supply to be bypassed, resulting in 0 voltage being output from the switch. *Id.*

The outputs of the switches are connected in series, thus generating a sum voltage (**yellow**) of the positive, negative, and bypassed supply voltages, depending on the state of the ternary control signals to each of the switches. Ex. 1101, Abstract, 1:18-23, 2:41-43, 3:61-4:29, 5:41-52, 6:65-7:7, 7:31-42, 7:57-65, 8:18-20, 10:16-23, 15:17-19, 19:36-38, Fig. 2; Ex. 1102, ¶ 97. For example, for ternary valued (+1, -1, or 0) signals T4, T3, T2, and T1 controlling switches 120a, 120b, 120c, and 120d, respectively, the inverter sum output voltage would be (120*T4)+(40*T3)+(13.33*T2)+(4.44*T1) volts. Ex. 1101, 7:23-65. If all switches output their associated positive voltage (T4, T3, T2, and T1 all equal +1), the output voltage would be 120+40+13.33+4.44=177.77 volts, but if the 4.44 volt switch changes to output 0 volts (T1=0), the summed output voltage would become 120+40+13.33=173.33 volts. Ex. 1101, 7:65-8:5; Ex. 1102, ¶¶ 98-100.

Switch states can be controlled to produce a sinusoidal waveform, as seen below in Figure 12. Ex. 1101, Abstract, 1:18-23, 3:61-4:10, 5:41-52, 7:23-36, 7:60-8:7, 9:26-10:40.

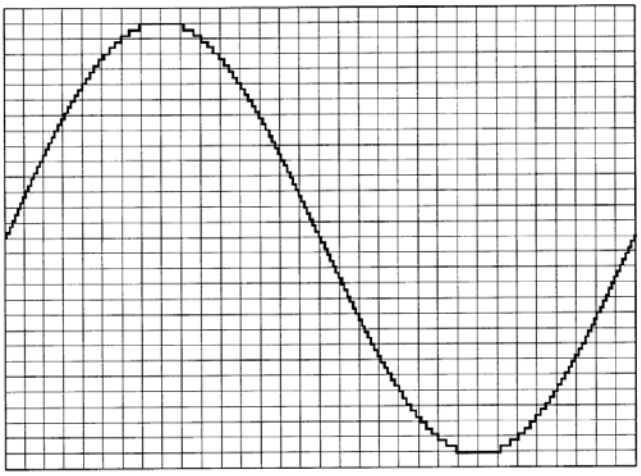


FIG. 12

Ex. 1101, Fig. 12

B. Prosecution History

The application that led to the ’710 patent was filed August 14, 2017. Ex. 1102, ¶ 107. Following an initial rejection of certain claims as being anticipated by U.S. Patent No. 4,180,853 to Scorso (Ex. 1103, 188), PO argued that Scorso lacked the required ternary control of the switches. *Id.*, 229-232. The Examiner then rejected the claims over Scorso in view of U.S. Patent No. 5,373,433 to Thomas, which taught ternary control of H-bridge switches in an inverter. *Id.*, 261-268. PO then amended the claims to require a “transformerless” output and to require that the outputs of the plurality of switches are “directly” connected in series to output a sum voltage that approximates the desired waveform. *Id.*, 286. PO argued that the outputs of the H-bridge switches in Thomas were passed across transformers, and then the output of those transformers were summed to approximate the desired

waveform. *Id.*, 294-296. PO did not dispute that the ternary control of H-bridge switches was taught in the art. *Id.*

The Examiner issued a notice of allowance, referencing the lack in the prior art of the output of ternary controlled switches directly connected in series to output a sum voltage approximating the desired AC waveform. *Id.*, 312-313; Ex. 1102, ¶¶ 107-112.

C. Earliest Priority Date for the Claims

The earliest entitled possible priority date for the '710 patent claims is the filing date of U.S. Patent Application No. 13/103,070, May 8, 2011. Ex. 1102, ¶ 116.

V. OVERVIEW OF PRIOR ART

A. Suzuki

Suzuki (Ex. 1125, certified translation Ex. 1126) is a Japanese Patent Application published on January 8, 2004, making it prior art under 35 U.S.C. § 102(b).[1] Ex. 1102, ¶ 122.

Suzuki discloses a single-phase inverter similar to that in the '710 patent. *Compare* Ex. 1101, Fig. 1 *with* Ex. 1126, Fig. 14; Ex. 1102, ¶ 123.

[1] Citations to 35 U.S.C. §§ 102 and 103 refer to the pre-AIA versions.

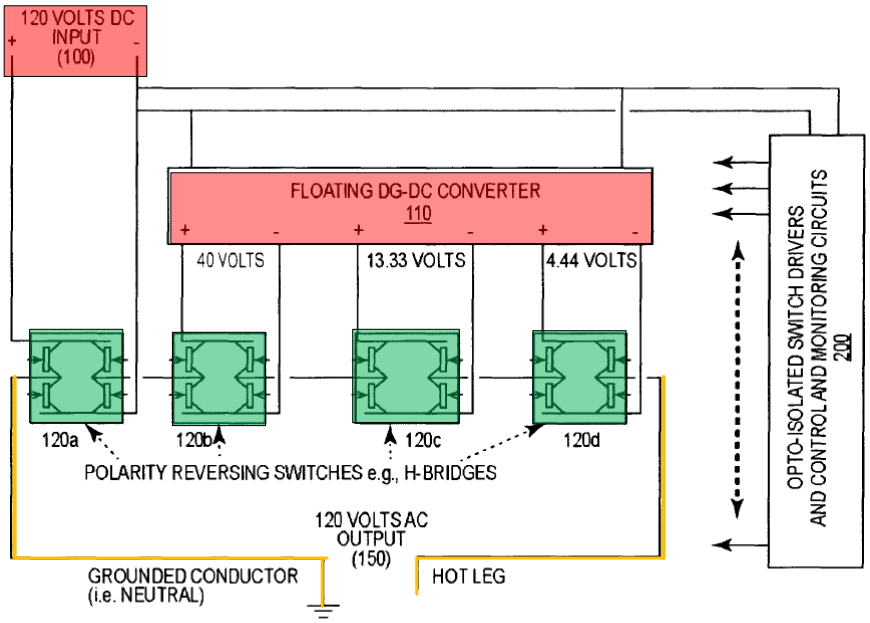
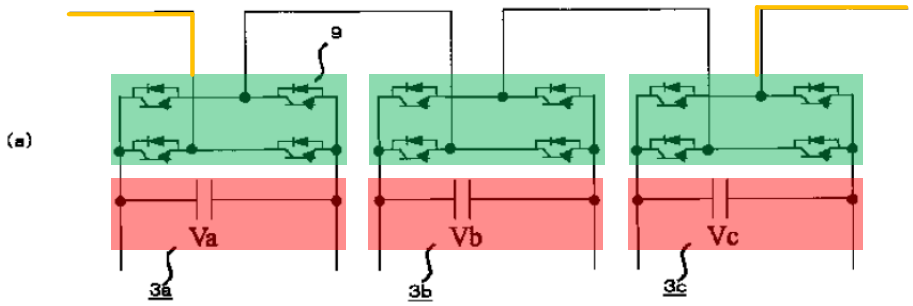


FIG. 1



Ex. 1101, Fig. 1 (annotated, top); Ex. 1126, Fig. 14(a) (annotated, bottom)

Suzuki's inverter has DC power sources (**red**) providing DC voltages Va, Vb, and Vc to single-phase inverters 3a, 3b, and 3c (**green**). Ex. 1126, [Summary], [0006], [0017]-[0018], [0027], [0060], Figs. 3, 14(a); Ex. 1102, ¶ 124. The single-phase inverters 3a, 3b, and 3c are connected in series and output an AC signal (**yellow**). Ex. 1126, [0006], [0017]-[0018], [0027], [0060], Figs. 3, 14(a); Ex. 1102, ¶ 124.

Suzuki, again like the ’710 patent, discloses that each of the single-phase inverters consists of switching devices, such as transistors in an H-bridge configuration (**green**). *Compare* Ex. 1101, 8:33-40, Fig. 3, 6 *with* Ex. 1126, [0017], [0027], Figs. 3, 14(a); Ex. 1102, ¶ 125.

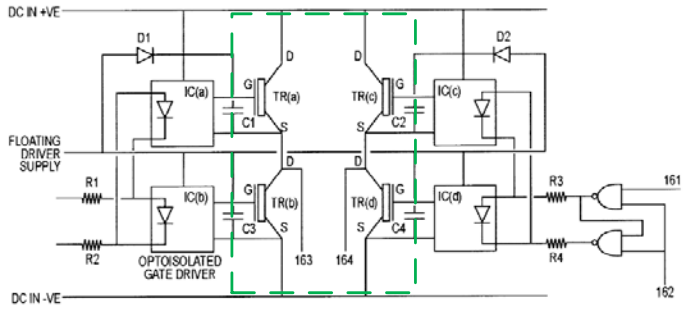
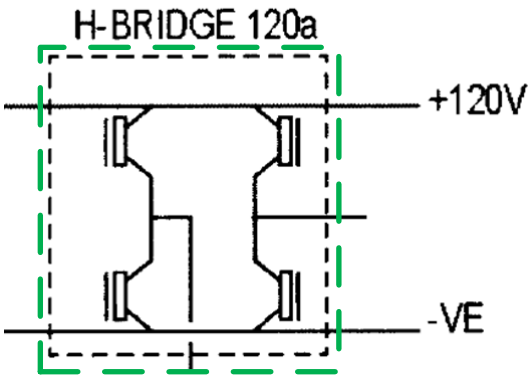
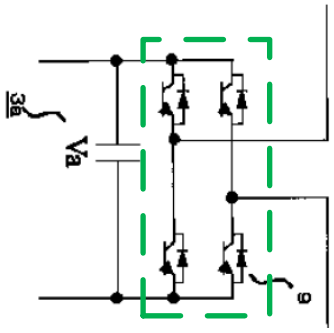


FIG. 3

Ex. 1101, Fig. 3 (annotated)



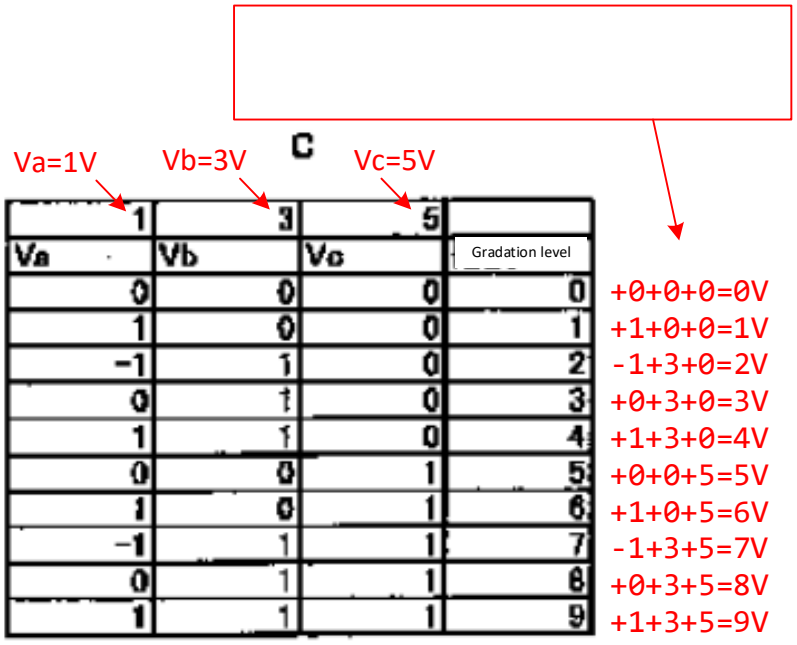
Ex. 1101, Fig. 6 (excerpted, annotated)



Ex. 1126, Fig. 14(a) (excerpted, annotated)

In Suzuki, each single-phase inverter 3a, 3b, and 3c has a different DC supply voltage and is controlled so that, depending on the switch state, the inverter will output either the DC supply voltage, the inverse of the DC supply voltage, or zero volts. Ex. 1126, [0018]-[0019], Fig 4; Ex. 1102, ¶ 126. The switch states can be controlled based on a ternary system with a value of +1 associated with the positive

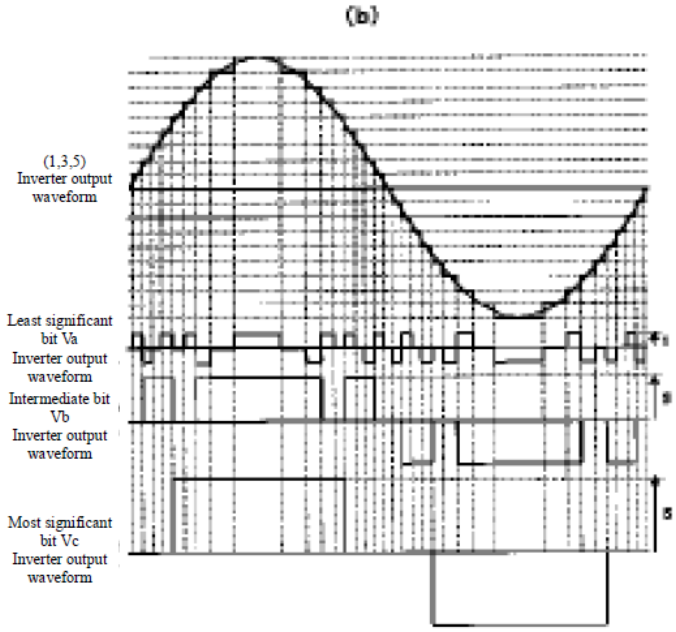
DC voltage, -1 associated with the negative of the DC voltage, and 0 associated with zero voltage. Ex. 1126, [0018]-[0019], Fig 4. By controlling the states of the switching devices over time and summing the outputs of the inverters (3a, 3b, and 3c), an AC output wave is generated. Ex. 1126, [Summary], [0018]-[0019], Figs. 4, 5; Ex. 1102, ¶ 126.



Ex. 1126, Fig. 4(c) (annotated)

Voltages Va, Vb, and Vc are the DC voltage inputs for 3a, 3b, and 3c, respectively, and the control states (+1, 0, -1) of the switching circuits of those inverters are shown in the first three columns of Figure 4(c). Ex. 1126, [0018], Fig. 4(c); Ex. 1102, ¶ 127. The gradation level or output voltage, which is the sum of the output voltages of 3a, 3b, and 3c, is shown in the fourth column of Figure 4(c) and

is also shown graphically below in Figure 5(b), approximating a sinewave. Ex. 1126, [0018]-[0019], Fig. 5(b); Ex. 1102, ¶ 127.



Ex. 1126, Fig. 5(b)

B. Nishimura

Nishimura (Ex. 1114) is a U.S. Patent Application Publication first published on April 2, 2009, making it prior art under 35 U.S.C. § 102(b). Ex. 1102, ¶ 188.

Nishimura discloses an inverter for converting DC to AC using a bridge circuit. Ex. 1114, [0058]-[0059], Fig. 1; Ex. 1102, ¶ 189. Nishimura further discloses that its inverter can output at 50 Hz and 200V, which is standard household voltage and frequency in Japan. Ex. 1114, [0058]; Ex. 1110, 22; Ex. 1102, ¶ 189.

C. Mori ’630

Mori ’630 (Ex. 1105, certified translation Ex. 1106) is a Japanese Patent Application published on September 7, 2006, making it prior art under 35 U.S.C. § 102(b). Ex. 1102, ¶ 213.

Mori ’630 teaches an inverter comprising a plurality of single-phase inverters, each connected to a different floating DC power source, and each connected in series to form a single multiplex inverter. Ex. 1106, Fig. 1, [0009]; Ex. 1102, ¶ 214. Each of the single-phase inverters is composed of switching elements, such as MOSFETs, in an H-bridge configuration that are controlled by ternary-valued control signals produced by a control circuit. Ex. 1106, [0009]-[0012], [0015]; Ex. 1102, ¶ 215. The output terminals of each floating DC power source are connected to input terminals of a corresponding H-bridge. Ex. 1106, Fig. 1. Mori ’630 teaches connecting the H-bridge with the highest associated DC voltage to the neutral output terminal. Ex. 1106, [0009]-[0012]; Ex. 1102, ¶ 215.

D. Tolbert

Tolbert (Ex. 1131) is an article published and available to the public in 1999, making it prior art under 35 U.S.C. § 102(b). Ex. 1139, ¶¶ 117-134; Ex. 1102, ¶ 199.

Tolbert teaches a power converter that combines the outputs of a plurality of inverters to generate an AC output waveform. Ex. 1131, p. 37, Fig. 1. Like Suzuki

and Mori ’630, each inverter has transistors in an H-bridge configuration and outputs one of three levels (+V, -V, or 0) based on the combinations of the ON and OFF states of the transistors. Ex. 1131, pp. 37-38, Fig. 2; Ex. 1102, ¶ 200. Tolbert explains the ternary control signals that are generated to place the switches into either a +1, -1, or 0 state. Ex. 1131, pp. 37-38, Figs. 1, 2; Ex. 1102, ¶ 201. Gate driving signals, *e.g.*, a pair of binary bits (G_{aip} and G_{ain}), are sent to the switching devices of each of the inverters. Ex. 1131, pp. 37-38, Fig. 2. There are four possible patterns for the binary values of these two bits (*i.e.*, 00, 01, 10, and 11) and each such pattern places an H-bridge into one of its three possible states. Ex. 1131, pp. 37-38. Specifically, one combination places a switch into the +1 state, another places the switch into the -1 state, and the remaining two combinations place the switch into the 0 state. Ex. 1131, pp. 37-38, Fig. 2; Ex. 1102, ¶ 201.

E. Kumar

Kumar (Ex. 1128) is a U.S. Patent that issued on December 1, 1992, making it prior art under 35 U.S.C. § 102(b). Ex. 1102, ¶ 229.

Kumar discloses a programmed PWM controller for controlling a DC/AC inverter including memories containing tables of switching signals that are output to control the state of the inverter’s individual switches. Ex. 1128, 1:6-16, 4:49-5:23, 6:17-50, Fig. 1; Ex. 1102, ¶ 230.

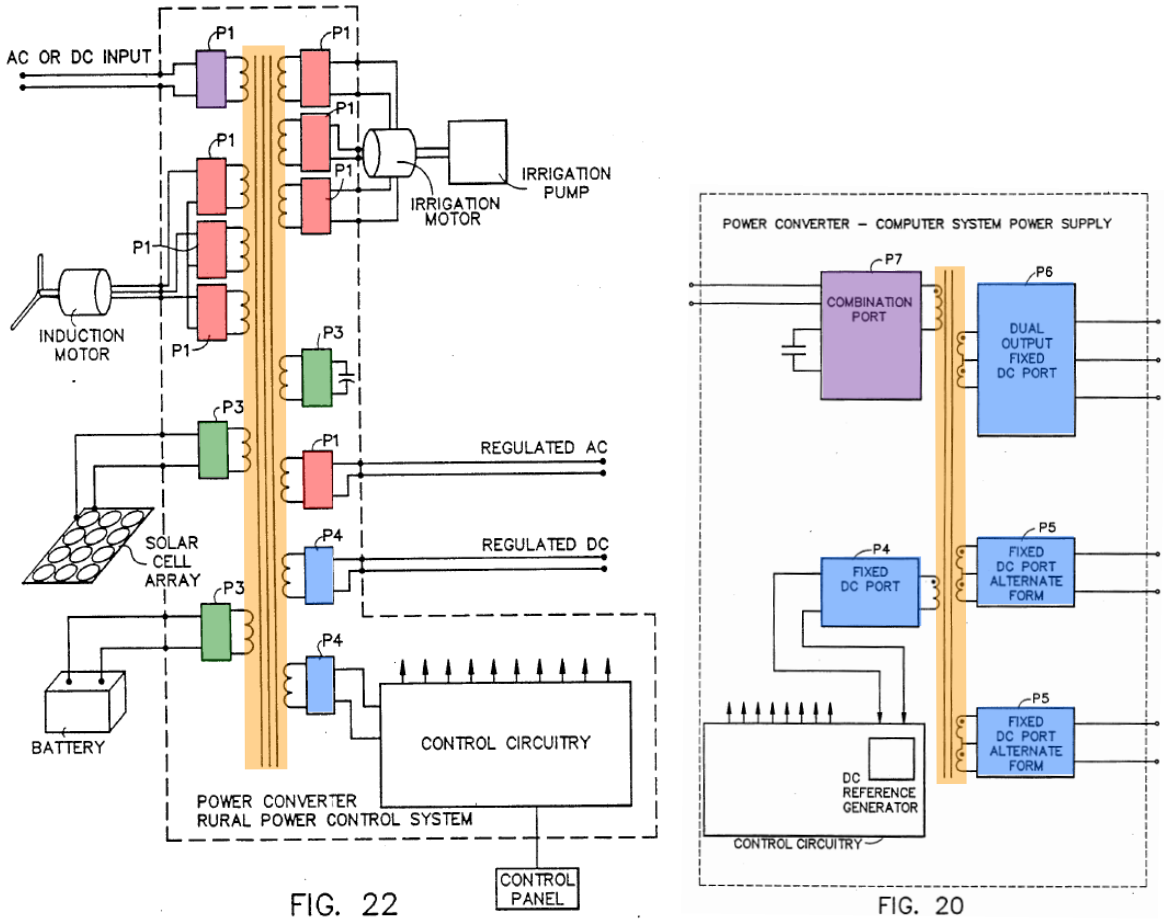
Specifically, a first PROM of the controller stores a set of "pattern tables" containing firing pattern signals defining the on/off status of the inverter's switching devices, and a second PROM stores a set of "angle tables" storing transition times for the inverter control signals (the recited "memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output"). Ex. 1128, 4:56-62, 5:53-67; Ex. 1102, ¶ 231. Based on the required frequency and voltage of the AC signal, the microprocessor selects the pattern and angle table to be used. Ex. 1128, 6:5-15; Ex. 1102, ¶ 231. The microprocessor loads the beginning address of the pattern table into the address counter and the transition times from the angle table are written into the timing circuits. Ex. 1128, 5:41-66; Ex. 1102, ¶ 231. As the timing circuits time out, the address counter is advanced and the PROM sequences through the firing signals of the pattern table which are output to the inverter. Ex. 1128, 5:7-23, 5:39-40; Ex. 1102, ¶ 231.

F. Ball

Ball (Ex. 1127) is a U.S. Patent that issued on July 2, 1991, making it prior art under 35 U.S.C. § 102(b). Ex. 1102, ¶ 243.

Ball discloses a universal bidirectional power converter (two examples shown below) with a single transformer (**orange**) that transfers power between two or more bidirectional ports. Ex. 1127, 11:25-33, 11:65-12:4, 13:60-14:5, 19:16-32, 19:52-61,

21:20-65, 23:33-34, 24:62-25:11, 25:58-61, 36:64-68, 50:20-30, 50:58-51:8, 52:10-14, Figs. 20, 22; Ex. 1102, ¶ 244. The ports must include one fixed DC voltage port (**blue**), and the remainder of the ports may include any combination of other fixed DC (**blue**), variable DC (**green**), AC (**red**), and AC/DC combination (**purple**) voltage ports. Ex. 1127, 21:33-65, 22:37-48, 37:17-20, 40:41-46, 53:20-26; Ex. 1102, ¶ 244. Thus, one of the disclosed implementations of Ball's bidirectional converter will convert a fixed DC voltage to other DC voltages, *i.e.*, is a bidirectional DC to DC converter. Ex. 1102, ¶ 244.



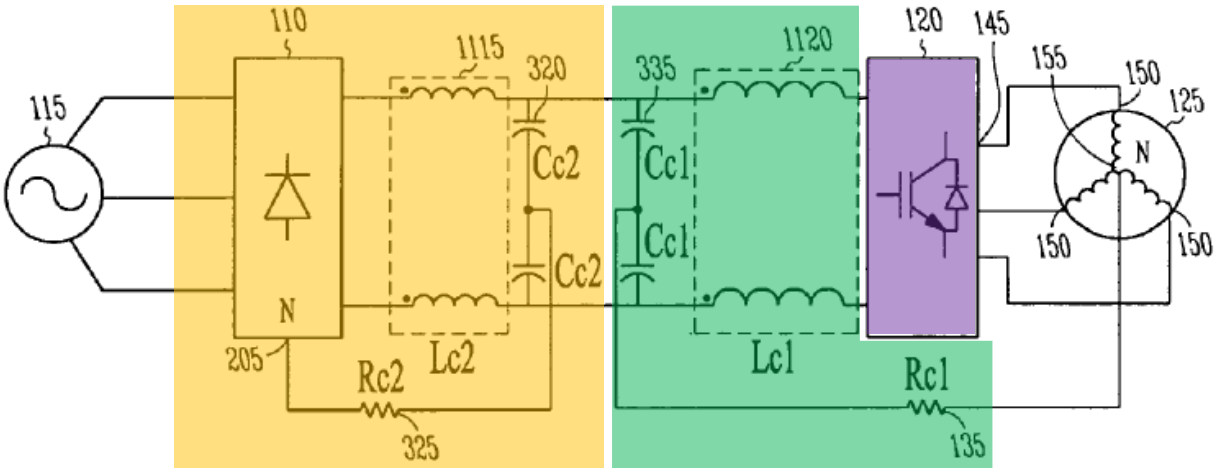
Ex. 1127, Figs. 20 and 22 (annotated)

The fixed DC voltage port, which is connected to a DC source of power such as a battery, generates an equal-duty-cycle square wave with a fixed frequency, phase, and amplitude within the transformer. Ex. 1127, 12:5-27, 13:9-23, 22:12-20, 22:37-48, 31:44-32:2, 32:7-11, 34:43-35:4, 44:34-42, 44:52-60, 52:22-32, 52:53-62; Ex. 1102, ¶ 245. Each remaining port includes a control loop that causes the port to convert power (whether AC, DC, or both) at its terminals to/from a square wave at the transformer winding, which is "locked" to the same frequency, phase and amplitude established by the first fixed DC voltage port. Ex. 1127, 32:52-33:8, 43:31-38; Ex. 1102, ¶ 245.

G. **De**

De (Ex. 1129) is a U.S. Patent Application Publication published on December 6, 2007. De is prior art under 35 U.S.C. § 102(b). Ex. 1102, ¶ 260.

As shown in Figure 12, De discloses a common mode filter (**green**), including a common mode inductor 1120 and capacitors 335, connected between DC input terminals of inverter 120 (**purple**) and positive and negative terminals of DC power source (**orange**). Ex. 1129, [0020], [0033]-[0034], Figs. 11-12; Ex. 1102, ¶ 261.

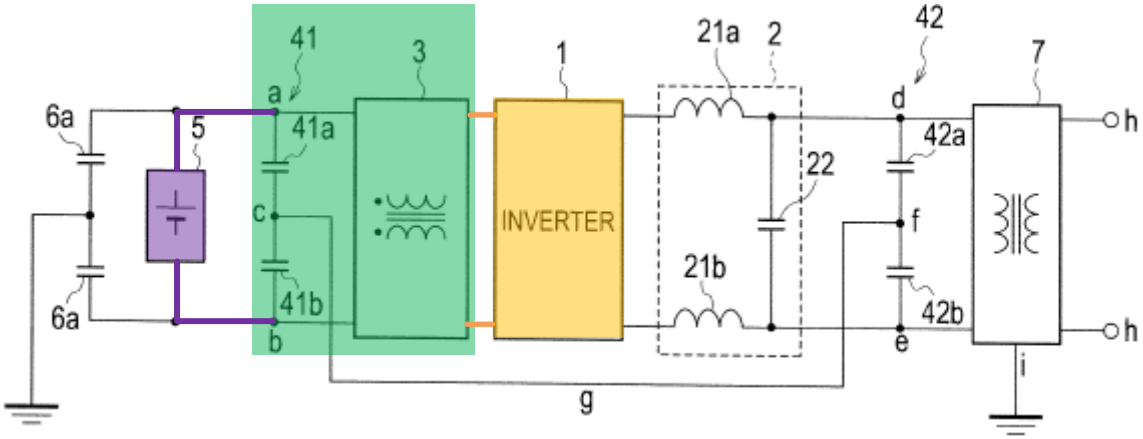


Ex. 1129, Fig. 12 (annotated)

H. Koyama

Koyama (Ex. 1117, certified translation Ex. 1113) is a Published International Application published on May 20, 2010. Koyama is prior art under 35 U.S.C. § 102(a). Ex. 1102, ¶ 271.

As shown in Figure 5, Koyama discloses a common mode filter (**green**), including a first common mode choke coil 3a and capacitors 41a, 41b, connected between DC input terminals of an inverter 1 (**orange**) and positive and negative terminals of DC power source 5 (**purple**). Ex. 1113, [0005]-[0008], [0012], [0024]-[0026], [0030]-[0031], [0036]-[0038], Figs. 1, 5; Ex. 1102, ¶ 272.

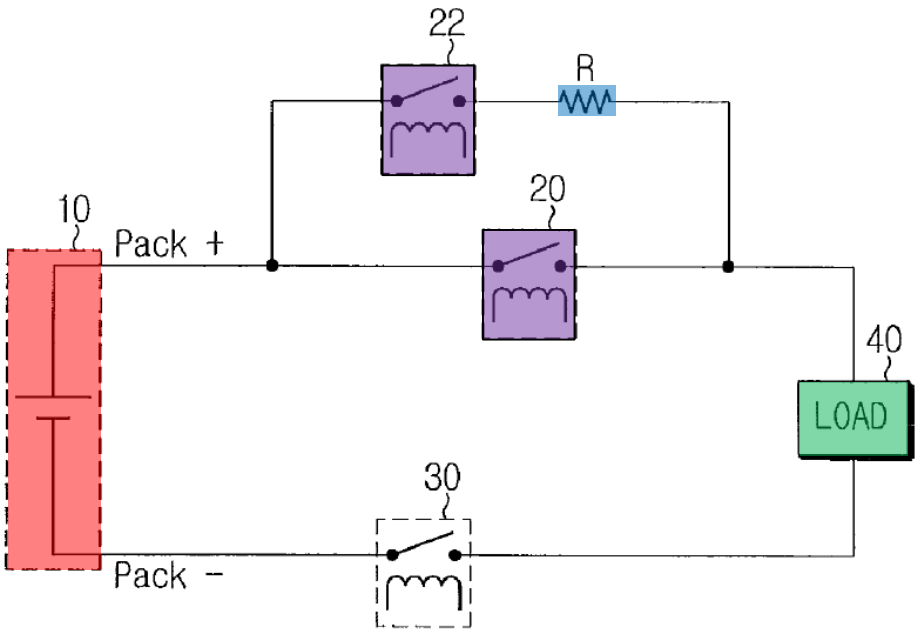


Ex. 1113, Fig. 5 (annotated)

I. Kang

Kang (Ex. 1130) is a U.S. Patent Application Publication published on June 3, 2010, making it prior art under 35 U.S.C. § 102(a) and (e). Ex. 1102, ¶ 308.

As shown in Figure 1, Kang discloses a DC power source 10 (**red**) providing power to a load 40 (**green**) and between the power source and load are interposed switches 20 and 22 (**purple**), and resistor R (**blue**). Ex. 1130, [0009]-[0011], Fig. 1; Ex. 1102, ¶ 309.



Ex. 1130, Fig. 1 (annotated)

To prevent damage from in-rush current when a load is being connected, switch 22 is turned on (*i.e.*, closed) while switch 20 is kept off (*i.e.*, open) so that resistor R ("a series impedance") is inserted to provide a high resistance path, limiting current flow to the load. Ex. 1130, [0011]-[0012], Fig. 1; Ex. 1102, ¶ 310. Once a predetermined time has passed which allows a certain threshold of current or voltage to be reached, switch 20 is turned on and switch 22 is turned off, thus removing any impedance between the power source and load. Ex. 1130, [0011]-[0012]; Ex. 1102, ¶ 310.

J. Ahmed

Ahmed (Ex. 1112) is an article published and available to the public in 2007, making it prior art under 35 U.S.C. § 102(b). Ex. 1139, ¶¶ 41-65; Ex. 1102, ¶ 282.

Ahmed discloses a design method for low pass LC filters to reduce switching frequency harmonics of inverters. Ex. 1112, p. 1, Fig. 1; Ex. 1102, ¶ 283.

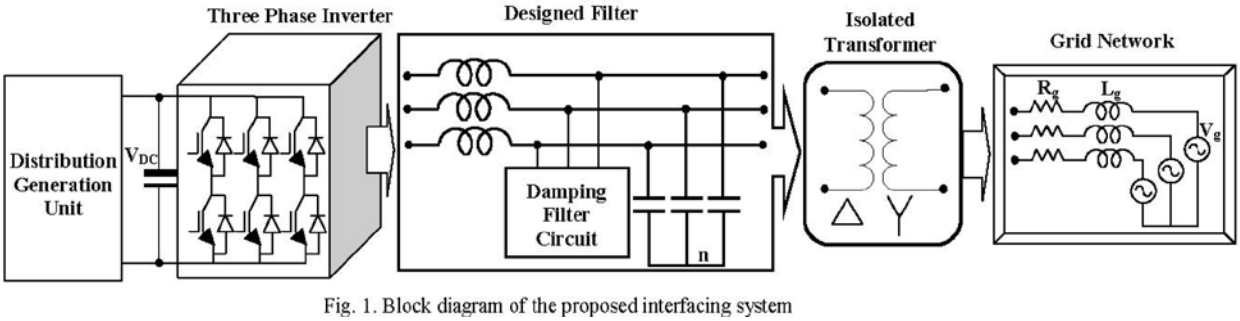


Fig. 1. Block diagram of the proposed interfacing system

Ex. 1112, Fig. 1

Ahmed identifies the problem in such filters of resonance between the inductor (L) and capacitor (C) components, and provides a solution to reduce resonance by adding a damping circuit, which includes a resistor with an additional capacitor and/or inductor. Ex. 1112, pp. 7-8, Figs. 13-15; Ex. 1102, ¶ 284.

VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. Claims for Which Review is Requested and Grounds on Which Challenge Is Based

Petitioner requests review of claims 1–17 on the following grounds. Ex. 1102, ¶¶ 117-118.

Ground	References	Basis	Claims Challenged
A	Suzuki	§ 103(a)	1-5, 7-8, 12
B	Suzuki in view of Nishimura	§ 103(a)	3
C	Suzuki in view of Tolbert	§ 103(a)	6

D	Suzuki in view of Mori ’630	§ 103(a)	7-8
E and F	Suzuki and Suzuki-Mori ’630, each in view of Kumar	§ 103(a)	9
G	Suzuki in view of Ball	§ 103(a)	10-11
H	Suzuki-Ball in view of De	§ 103(a)	13
I	Suzuki-Ball in view of Koyama	§ 103(a)	13
J	Suzuki-Ball in view of Koyama and Ahmed	§ 103(a)	14-15
K	Suzuki in view of Ahmed	§ 103(a)	16
L	Suzuki in view of Kang	§ 103(a)	17

None of the prior art listed above was considered during prosecution. Ex. 1101, cover.

B. Level of Ordinary Skill

A person having ordinary skill in the art (“PHOSITA”) would have had a bachelor’s degree in electrical engineering or a similar discipline, and three years of design experience with power electronics, including experience designing power converters. Ex. 1102, ¶¶ 20-23.

C. Claim Construction

All claim terms herein should be given their ordinary and customary meaning. Petitioner does not contend for this IPR that the claims include any means-plus-function limitations, but identifies the following claim elements, including their

respective structures, in the case the Board finds them to be means-plus-function elements. 37 C.F.R. § 42.104(b)(3).

1. "a switch selection signal generator operative to"

To the extent the board finds this is a means-plus-function term in claims 7-9, the function is to produce ternary-valued selection signals as set forth in claims 7-9, respectively, and the corresponding structure is controller 200 illustrated in Figure 1 or controller 202-2 illustrated in Figure 11, which include a microcontroller, microprocessor, or an equivalent structure that send the signals to switch driving circuits. Ex. 1101, 12:54-56, 13:21-27, 13:33-47, 15:39-41, 16:48-51, 16:61-63, Figs. 1, 11; Ex. 1102, ¶¶ 119-120.

2. "bi-directional DC-DC conversion circuitry operative to"

To the extent the board finds this is a means-plus-function term in claims 10 and 11, the function is to derive the lower voltage values (claim 10) or lower mean power (claim 11) from the battery and the corresponding structure is windings on one or more transformers which have turn ratios in proportion to the voltage ratios being output wherein each winding corresponding to the lower voltage values or lower mean power is center tapped, or an equivalent structure. Ex. 1101, 16:30-32, 19:41-48, 20:9-28, Fig. 2; Ex. 1102, ¶ 121.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A: Claims 1-5, 7-8, and 12 are Rendered Obvious by Suzuki

1. Independent Claim 1

Elements [1A]-[1F] are rendered obvious by Suzuki. Ex. 1102, ¶¶ 19, 34-49, 122-151.

a. [1A]: "A DC to AC converter having"

Suzuki discloses a DC to AC inverter similar to that in the '710 patent with an output that approximates a sinewave by summing the output of a set of series-connected single-phase inverters, each single-phase inverter consisting of a switching circuit. *Compare* Ex. 1101, 6:65-7:7, Fig. 1 *with* Ex. 1126, [Summary], [0016]-[0020], [0027], Figs. 6, 14(a); Ex. 1102, ¶ 130.

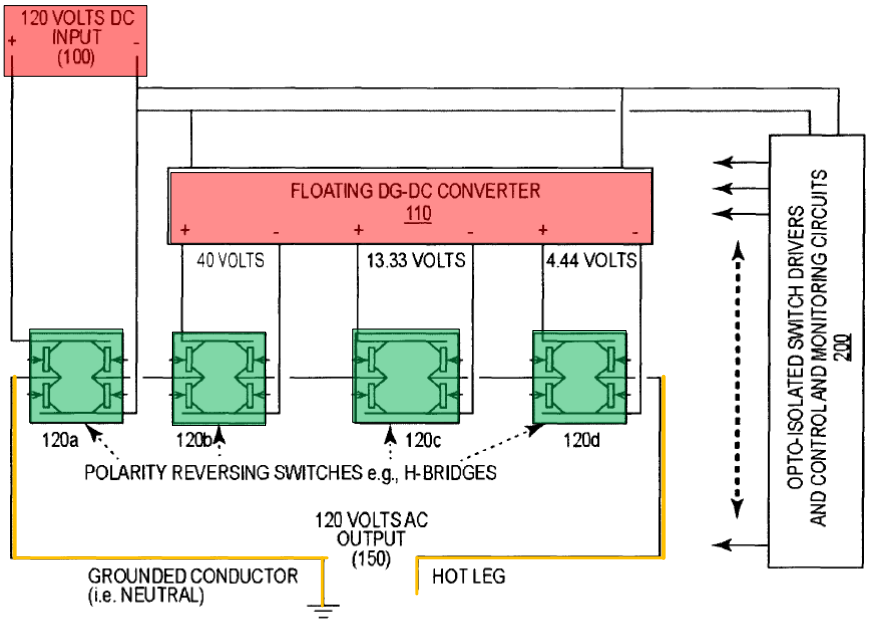
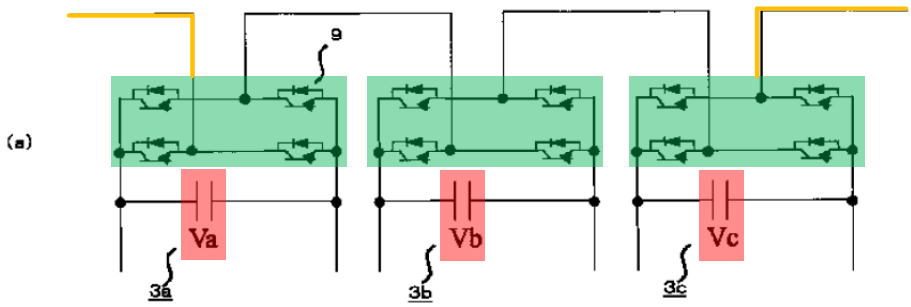


FIG. 1

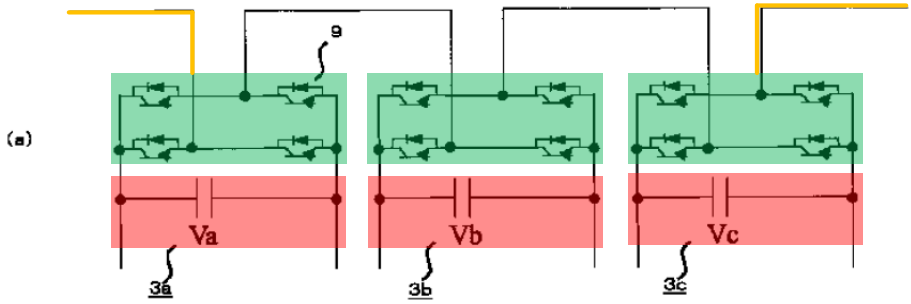


Ex. 1101, Fig. 1 (annotated, top); Ex. 1126, Fig. 14(a) (annotated, bottom)

Suzuki also discloses that three of these single-phase DC to AC inverters, such as shown in Figure 14, may also be used as part of a larger, three-phase DC to AC inverter, such as shown in Figure 6. Ex. 1126, [Summary], [0016]-[0020]; Ex. 1102, ¶ 130. Thus, Suzuki discloses [1A]. Ex. 1102, ¶ 130.

b. [1B] "a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,"

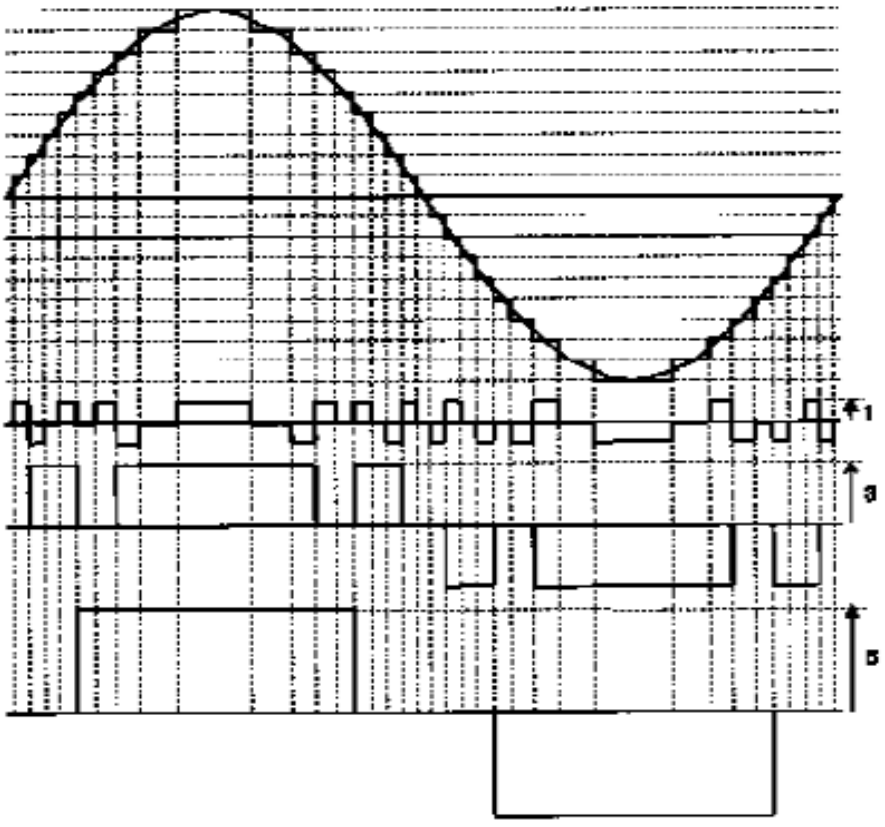
Suzuki's power conversion apparatus discloses a DC to AC converter that is operative to convert DC power (**red**) to AC power (**yellow**) as shown in Figure 14(a) below. Ex. 1126, [Summary], [0017]-[0019], [0027], Figs. 4, 5, 14(a); Ex. 1102, ¶ 131.



Ex. 1126, Fig. 14(a) (annotated)

As shown in Figure 14(a), Suzuki's inverter does not include a transformer between the series connected inverters 3a, 3b, and 3c (H-bridge switches) and the output, and thus the output is "transformerless." Ex. 1126, [0017]-[0018], [0027], Fig. 14(a); Ex. 1101, 2:44-47 (admitting transformerless inverters were known in the prior art); Ex. 1102, ¶ 132.

Suzuki's inverter outputs a desired voltage and waveform by generating different voltage levels through different combinations of the outputs of inverters 3a, 3b, and 3c to produce "a sine wave output gradation" as shown in Figure 5. Ex. 1126, [0017]-[0019], Figs. 4, 5; Ex. 1102, ¶ 133.



Ex. 1126, Fig. 5(b)

Thus, Suzuki discloses [1B]. Ex. 1102, ¶¶ 131-133.

c. [1C]: "and to output the AC power between hot and neutral output terminals,"

Based on Suzuki's teachings and his general knowledge, a PHOSITA would have found it obvious that Suzuki's inverter would output AC power between hot and neutral output terminals. Ex. 1102, ¶¶ 134-139.

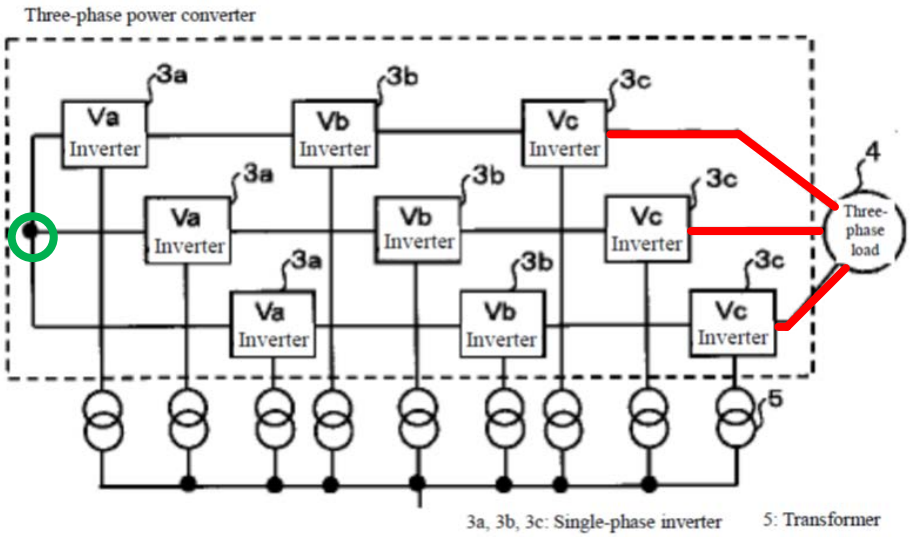
Suzuki teaches single-phase inverters connected in series to output AC power to a load. Ex. 1126, [0006], [0060]; Ex. 1102, ¶ 135. A PHOSITA would understand a "load" in Suzuki to include an AC electrical grid, for example one in compliance with the National Fire Protection Association (NFPA) 70 National Electrical Code 2008 Edition (NEC 2008) that is cited repeatedly in the '710 patent and was the most widely adopted installation code in the United States. Ex. 1102, ¶ 135; Ex. 1101, 25:5-9, 32:8-11, 33:4-6; Ex. 1118, 7-8. A PHOSITA would also understand that a residential single-phase AC electrical grid input would include three wires: two hot (or line) wires and one neutral wire. Ex. 1118, 11-12 (Exhibit 100.12); Ex. 1102, ¶¶ 135-136.

Therefore, when attaching a single-phase inverter having a two-wire output (*e.g.*, Suzuki's single-phase inverter) to a residential single-phase AC electrical grid input, there would only be two options: (1) connect the two output terminals of Suzuki's inverter to the two hot wires of the AC electrical grid (*e.g.*, 240 VAC), or (2) connect one output terminal of Suzuki's inverter to a hot wire of the AC electrical

grid and the other output terminal of Suzuki's inverter to the neutral wire of the AC terminal (*e.g.*, 120 VAC). Ex. 1102, ¶ 137. The second (indeed, either) option would have been obvious as one of only two choices, because a PHOSITA would have followed safety standards, including NEC 2008, which allows for connecting inverters between hot and neutral terminals of a grid for medium sized residential hybrid photovoltaic systems. Ex. 1118, 24 (Exhibit 690.4); Ex. 1102, ¶ 137. Moreover, since the NEC 2008 "is intended for use by capable engineers and electrical contractors in the design and/or installation of electrical equipment," a PHOSITA would have had a high expectation of success in following the standard to connect the inverter in such a manner. Ex. 1118, 8; Ex. 1102, ¶ 137.

Furthermore, Suzuki shows single-phase inverters connected between neutral and hot output terminals. Suzuki teaches that three of its series-connected single-phase inverters can be connected in a three-phase system as shown in Figure 1. Ex. 1126, [0016]-[0017], [0027], [0031], Figs. 1, 6, 14(a), 18; Ex. 1102, ¶ 138. In other words, a three-phase inverter comprises three of the single-phase inverters, with each single-phase inverter including three sets of H-bridges connected in series and having an output between a hot and a neutral terminal. Each of the three single-phase inverters shares the same common neutral terminal and has a different hot terminal. Ex. 1102, ¶ 138. As shown in Figure 1, the output terminal connected to the three 3a H-bridge circuits in the three inverters are connected together at a

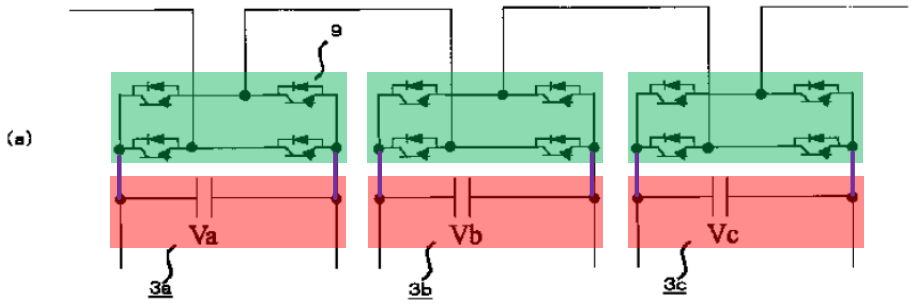
common point (**green**), while the other output terminals of the three inverters are connected to the three-phase load 4. *Id.* A PHOSITA would have understood that the common connection point (**green**) is "neutral," having the midpoint average voltage of the other three "hot" output terminals (**red**). *Id.*; Ex. 1118, 11-12 (Exhibit 100.12).



Ex. 1126, Fig. 1 (annotated)

Thus, Suzuki renders [1C] obvious. Ex. 1102, ¶¶ 134-139.

d. [1D]: "the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and"



Ex. 1126, Fig. 14(a) (annotated)

Suzuki's inverter comprises "a plurality of controlled switches" (**green**), described as three single-phase inverters 3a, 3b, and 3c. Ex. 1126, [0017]-[0018], [0027], Fig. 14(a); Ex. 1102, ¶ 140. Each switch includes a plurality of switching devices arranged in an H-bridge switch like those disclosed in the '710 patent as shown in the comparison figures below. Ex. 1126, [0027], Figs. 3, 14(a); Ex. 1102, ¶¶ 140-141. As discussed in more detail in relation to Element [1E] below, these switches are controlled to produce positive, negative, or zero voltages from their respective DC power sources. Ex. 1126, [0017]-[0018], Figs. 4-5; Ex. 1102, ¶ 141.

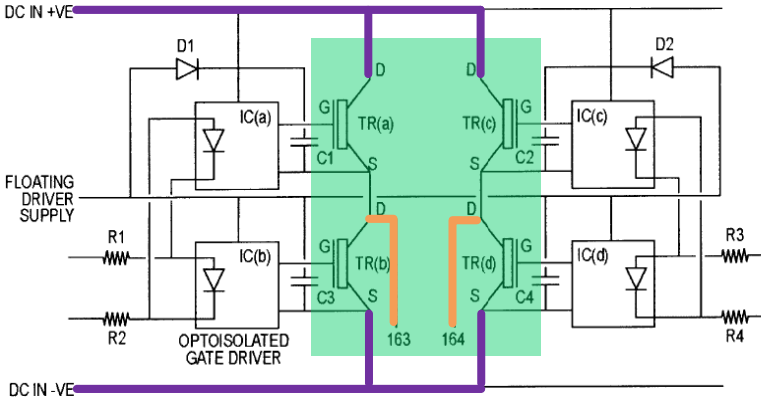
Each of these switches have input connections (highlighted in **purple** above) connected to and receiving DC power from an associated DC power source (highlighted in **red** above), which is a capacitor providing DC voltages Va, Vb, and Vc to single-phase inverters 3a, 3b, and 3c, respectively. Ex. 1126, [0017]-[0018],

[0027], Fig. 14(a); Ex. 1102, ¶ 142. Further, "Va, Vb, and Vc have different values (Va < Vb < Vc) and the relationship thereof is either 1:2:4, 1:3:4, 1:3:5, 1:3:6, 1:3:7, 1:3:8, or 1:3:9." Ex. 1126, [0018], Figs. 4-5.

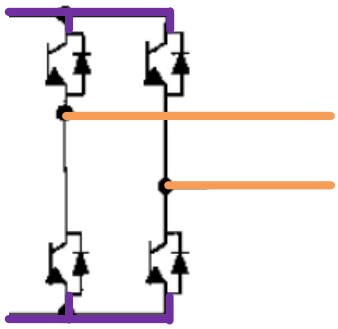
Thus, Suzuki discloses [1D]. Ex. 1102, ¶¶ 140-143.

e. [1E]: "each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,"

Suzuki's inverters are arranged and controlled identically to the H-bridge switches disclosed in the '710 patent (as shown in the comparison figures below) via a ternary-valued selection signal to operate in three states (+1, -1, and 0) as shown in Figure 4. Ex. 1126, [0017]-[0019], Figs. 3-5; Ex. 1101, 7:23-28, 8:33-54, 9:58-64, 11:5-13, 11:26-35, Fig. 3; Ex. 1102, ¶ 144.



Ex. 1101, Fig. 3 (annotated)



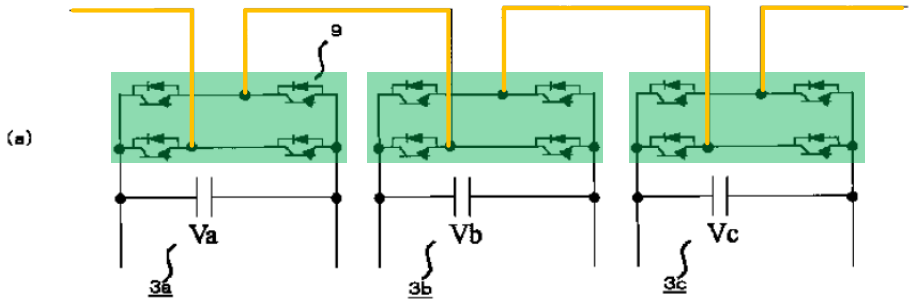
Ex. 1126, Fig. 3(a) (excerpted, annotated)

For example, in Table C of Figure 4, the 3a, 3b, and 3c inverters can each output either the positive or negative (*i.e.*, "inverted polarity") of their respective input voltage (*e.g.*, Va, Vb, or Vc), or zero voltage based on whether the inverter's respective switches are controlled to be in the +1, -1, or 0 state. Ex. 1126, [0018]-[0019], Fig. 4; Ex. 1102, ¶ 145. Thus, as required by element [1E], Suzuki's switches "hav[e] a power output connection operative to output a selected one of: (a) the associated DC voltage" in response to an associated +1 multiplier value of the selection signal, "(b) the associated DC voltage having an inverted polarity," in response to an associated -1 multiplier value of the selection signal, and "(c) zero voltage" in response to a 0 multiplier value of the selection signal. Ex. 1126, [0018]-[0019], Fig. 4; Ex. 1102, ¶¶ 145-146. This is described in more detail with an example from Figure 4 of Suzuki, immediately below. Section VII.A.1.f., *infra*.

Thus, Suzuki discloses [1E]. Ex. 1102, ¶¶ 144-146.

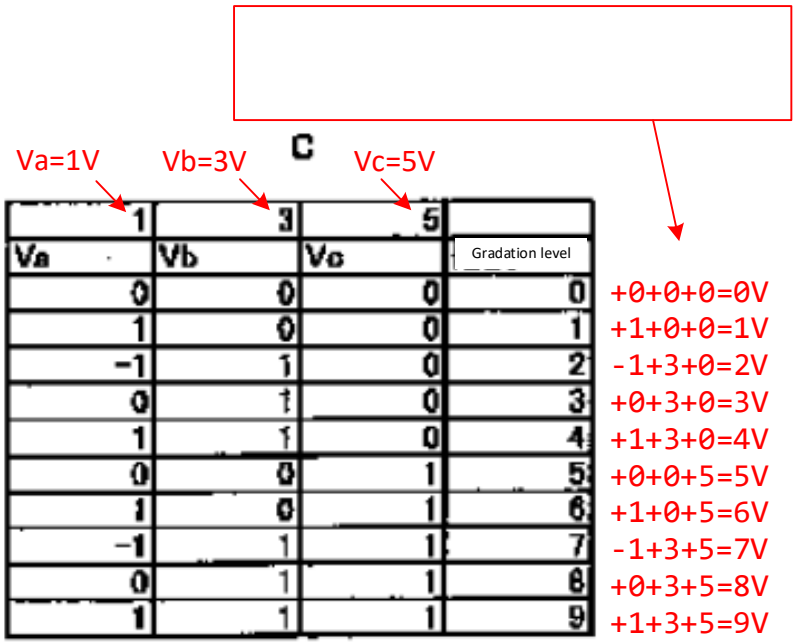
f. [1F]: "the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform."

As shown below, the outputs of Suzuki's switches (**green**) are directly connected in series (**yellow**). Ex. 1126, [Summary], [0006], [0018]-[0019], [0027], [0060], Fig. 14(a); Ex. 1102, ¶ 147.



Ex. 1126, Fig. 14(a) (annotated)

Because the outputs of Suzuki's switches are directly connected in series, the output is the sum of the outputs of inverters 3a, 3b, and 3c in Suzuki's Figure 14(a). Ex. 1126, [Summary], [0006], [0018]-[0019], [0027], [0060], Fig. 14(a); Ex. 1102, ¶ 148. As discussed above for Element [1E], the Suzuki inverters (3a, 3b, and 3c) are each controlled to output either an associated DC voltage (Va, Vb, or Vc), or the inverted polarity of that associated DC voltage, or zero voltage based on a multiplier value of +1, -1, or 0, respectively. Ex. 1126, [0018]-[0019], Fig. 4; Ex. 1102, ¶ 148.



Ex. 1126, Fig. 4(c) (annotated)

In the particular example of Figure 4(c), the DC power source voltage inputs Va, Vb, and Vc are in a ratio of 1:3:5, as indicated in the top row of Figure 4(c). Ex. 1126, [0019], Fig. 4(c). The multipliers applied by the switches 3a, 3b, and 3c are shown in the first three columns of Figure 4(c), under the second "Va, Vb, Vc" row. Ex. 1126, [0019], Fig. 2(a); Ex. 1102, ¶ 149. The output voltage, which is the sum of the output voltages of 3a, 3b, and 3c, is shown in the fourth column of Figure 4(c), under the "Gradation level" entry. Ex. 1126, [0019], Fig. 4(c); Ex. 1102, ¶ 149.

Rows 3-12 of Figure 4(c) indicate 10 different voltage levels that can be obtained by multiplying each inverter voltage (1, 3, or 5) by the listed multiplier value (0, +1, -1), and summing the multiplied values as annotated in red. Ex. 1126, [0019], Fig. 4(c); Ex. 1102, ¶ 150. These voltage levels are selected based on

controlling the state of 3a, 3b, and 3c, to produce the substantially sinewave-like output voltage waveform of Figure 5(b). Ex. 1126, [0018]-[0019], Figs. 4, 5; Ex. 1102, ¶ 150.

Thus, Suzuki discloses [1F]. Ex. 1102, ¶¶ 148-151.

2. Claims 2 and 5

Claim 1, from which claims 2 and 5 depend, is taught by Suzuki. Section VII.A.1, s*upra*. Claim 2 further requires "at least some of the DC voltages associated with the plurality of controlled switches have different values," and claim 5 further requires that "each associated DC voltage differs from another DC voltage nominally by a factor of 3." Ex. 1101, claim 2.

Suzuki discloses DC voltages (Va, Vb, and Vc) having voltages that differ from one another by various ratios, including a factor of 3, *e.g.*, having a 1:3:9 ratio (Va=1V, Vb=3V, and Vc=9V), as shown in Figure 4(g). Ex. 1126, [0018]-[0019], Fig. 4(g); Ex. 1102, ¶¶ 154, 157.

Thus, Suzuki discloses the additional limitations of claims 2 and 5. Ex. 1102, ¶¶ 152-158.

3. Claim 3

Claim 1 is taught by Suzuki. Section VII.A.1, s*upra*. Claim 3 depends from claim 1 and requires "the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household

electricity supply frequency." Ex. 1101, claim 3. The '710 patent does not state what is "standard," but for something to be "standard," it would necessarily be well-known. Ex. 1102, ¶ 161. Thus, claim 3 requires that the desired output voltage and waveform be one that is already so well-known as to have been established as a standard electricity supply.

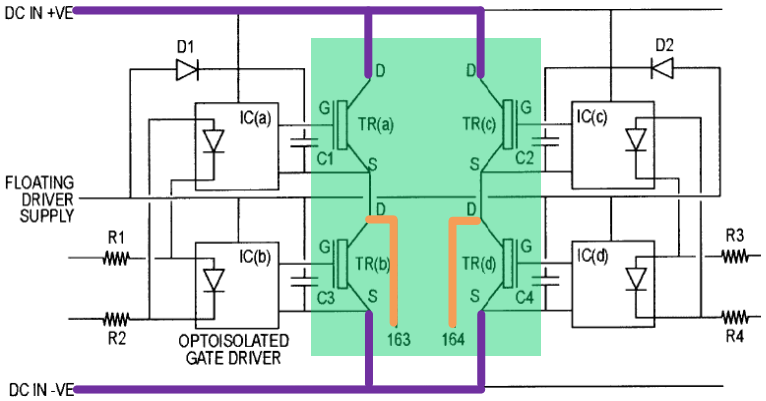
It was obvious that Suzuki's inverter could be used to output a waveform with the voltage and frequency suitable for a standard household electricity supply. In particular, Suzuki discloses that its inverter can provide a smooth AC output waveform to a load. Ex. 1126, [0001], [0005]-[0006], [0018]-[0019]; Ex. 1102, ¶ 161.

A PHOSITA was familiar with voltage and frequency suitable for a standard household electricity supply, for example 120 or 240 V and 60 Hz for households in the United States. Ex. 1102, ¶ 161. It was obvious to use a known technique (producing an AC waveform with the voltage and frequency used in a standard household) to improve a similar device (Suzuki's inverter) in the same way (Suzuki produces a smooth AC output waveform). Ex. 1102, ¶ 162. A PHOSITA was familiar with designing an inverter to produce AC power for use in a household and had the skills to do so, providing an expectation of success. Ex. 1102, ¶ 163.

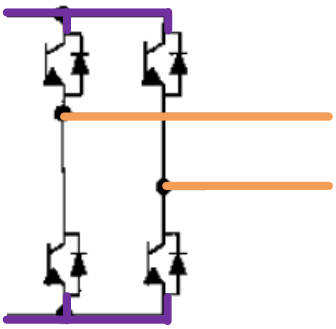
Thus, Suzuki renders claim 3 obvious. Ex. 1102, ¶¶ 159-164.

4. Claim 4

Claim 4 depends from claim 1 and further recites: "wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals." Ex. 1101, claim 4. As explained above in Section VII.A.1.d., Suzuki teaches the DC to AC converter of claim 1, and Suzuki's controlled switches are connected in H-bridge configurations like those disclosed in the '710 patent:



Ex. 1101, Fig. 3 (annotated)



Ex. 1126, Fig. 3(a) (excerpted, annotated)

Suzuki further discloses that the switching elements in its H-bridge (referred to as a "full bridge" in Suzuki) can be MOSFETs. Ex. 1126, [0017] ("Alternatively … a MOSFET … may be used."); Ex. 1102, ¶¶ 167-168.

Moreover, the DC power supply inputs to these switches are in the same configuration as in the '710 patent. Ex. 1102, ¶ 169. The floating DC power sources

(circled in dashed blue) along with their outputs (shown in solid blue) of the ’710 patent are shown on the below top, while the floating DC power sources (circled in dashed blue) along with their output connections (shown in solid blue) of Suzuki are shown on the below bottom:

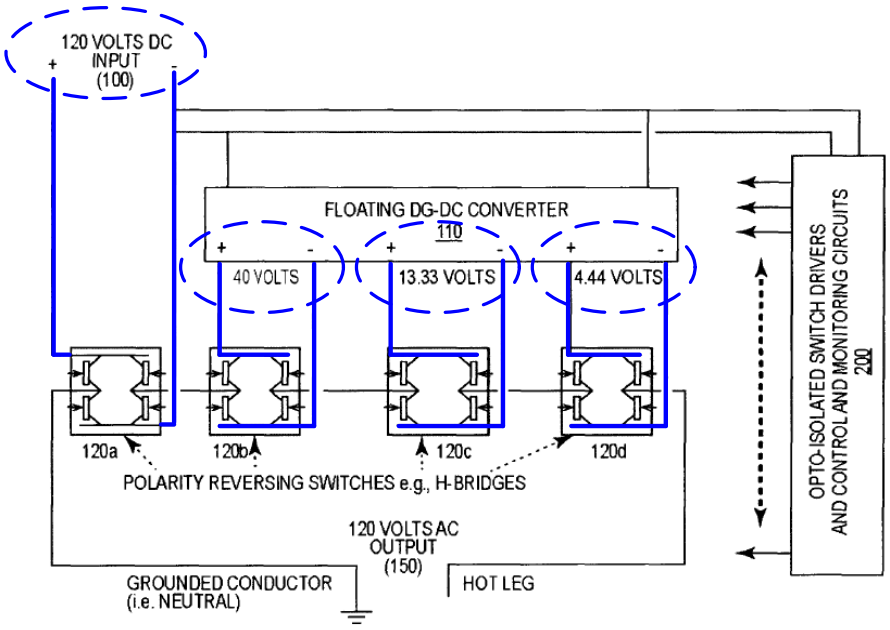
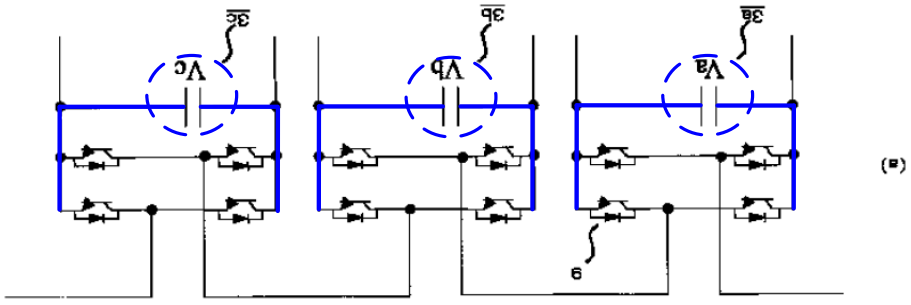


FIG. 1



Ex. 1101, Fig. 1 (annotated, top); Ex. 1126, Fig. 14(a) (rotated, annotated, bottom)

In both the ’710 patent and Suzuki, the output terminals of each DC power source are connected to input terminals of a corresponding H-bridge. Ex. 1101, Fig.

1, 7:57-60; Ex. 1126, Figs. 3, 14, [0017]-[0018]; Ex. 1102, ¶ 170. The switches can change the series arrangement of the voltage sources (*e.g.*, sometimes connecting them in a positive polarity, sometimes connecting them in the reverse polarity, or bypassing them) to generate different sum voltages. Ex. 1102, ¶ 170. For example, inverter 3c of Suzuki alternatively connects either the positive or negative of the Vc input terminals to the output terminal while connecting the opposite Vc input terminal in series to the other voltage sources through inverters 3a and 3b. This requires (as illustrated in Fig. 14(a)) the DC power source Vc to be floating with respect to the output and with respect to the other DC power sources. The DC power sources Va and Vb operate in a similar manner and are further offset from the output terminal by the varying voltage output by the adjacent 3c inverter. Thus, the DC power sources Va and Vb are likewise floating. Ex. 1102, ¶¶ 170, 101-102. Furthermore, Suzuki's power sources are not grounded which is consistent with the statement during prosecution of the '710 patent that "[a]s well known in the art, a 'floating' output of a power supply is one that is not referenced to a set voltage, such as chassis or earth ground." Ex. 1103, p. 291.

Thus, Suzuki renders obvious claim 4. Ex. 1102, ¶¶ 165-171.

5. Claims 7 and 8

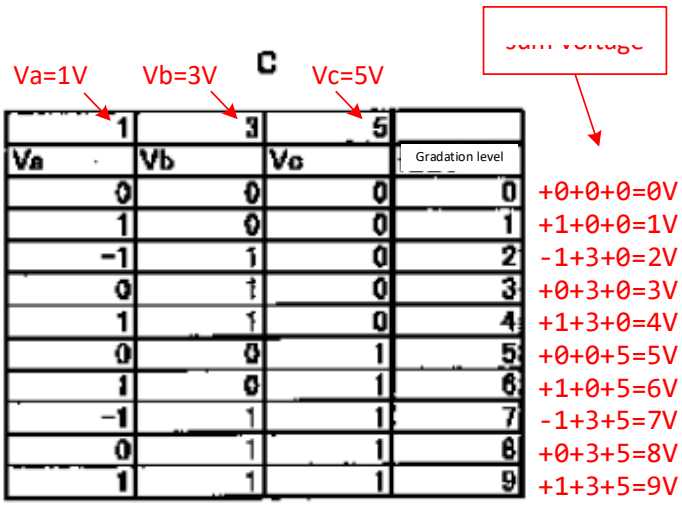
Claim 1 is taught by Suzuki. Section VII.A.1., s*upra*. Claims 7 and 8 each depend from claim 1 and require "a switch selection signal generator operative to

produce the ternary-valued selection signals, the switch selection signal generator being configured to produce [] sets of switch selection signals." Ex. 1101, claims 7, 8. Claim 7 further requires that the produced signal sets be "such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants," and claim 8 requires that the signal sets be produced such that each "new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals." *Id.*

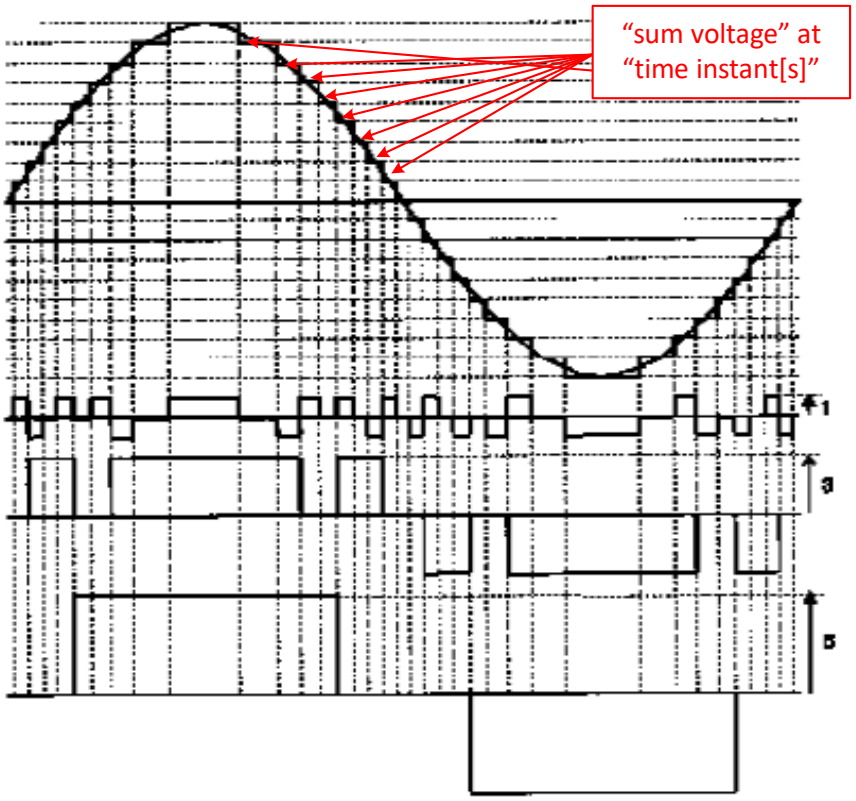
As described above in Section VII.A.1.a., Suzuki teaches the DC to AC converter of claim 1 that uses a set of ternary-valued selection signals (+1, -1, 0) to control a plurality of H-bridge switches. Ex. 1126, [0017]-[0019], Fig. 4; Ex. 1102, ¶ 174. This is disclosed, for example, in Suzuki's Figures 4 and 5, which show a combination of inverters 3a, 3b, and 3c producing a "sine wave output gradation" (Figure 5(b)) based on a set of ternary-valued selection signals (Figure 4(c)) sent to each of the H-bridge switches at different instances in time. Ex. 1126, [0018]-[0019]. Suzuki further describes that the output waveform can be smoothed using PWM control of one or more of inverters 3a, 3b, and 3c. *Id.*, [0020]-[0022], Figs. 7-8; Ex. 1102, ¶ 174.

A PHOSITA would have understood that the "gradation" and "PWM" control disclosed in Suzuki would have included a signal generator (*i.e.*, a "switch selection signal generator") generating the ternary-valued control signals sent to the H-bridge switches to create the desired output sum. Ex. 1102, ¶ 175.

Claim 7 further requires the sets of switch selection signals to be produced "at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants." Ex. 1101, claim 7. Claim 8 further requires the sets of switch selection signals to be "sequential" and the generator to be "configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals." *Id.*, claim 8.



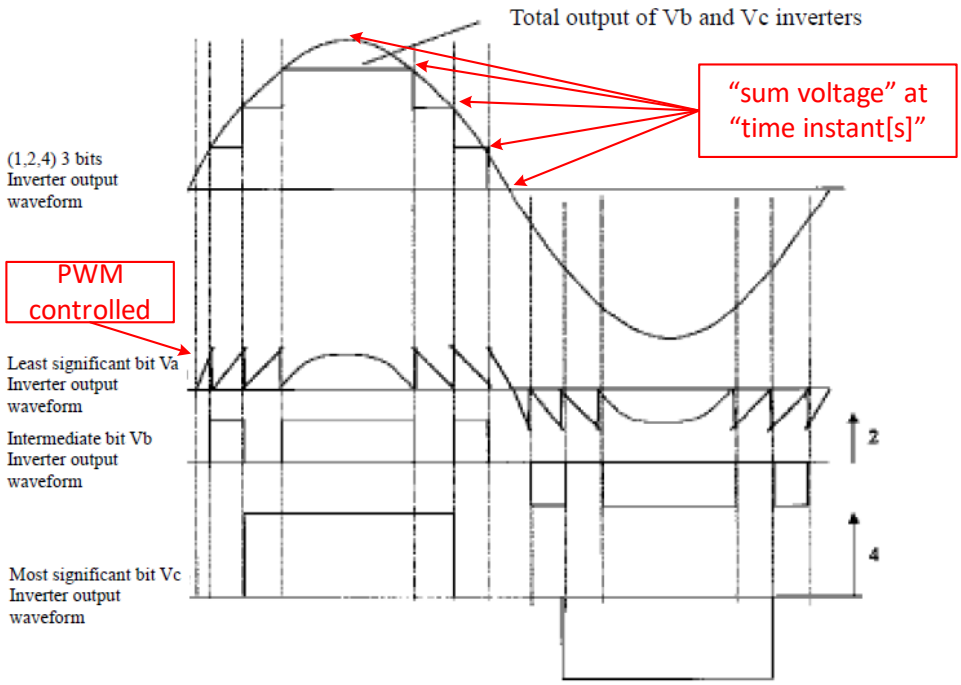
1	3	5	
Va	Vb	Vc	Gradation level
0	0	0	0
1	0	0	1
-1	1	0	2
0	1	0	3
1	1	0	4
0	0	1	5
1	0	1	6
-1	1	1	7
0	1	1	8
1	1	1	9



Ex. 1126, Figs. 4(c) and 5(b) (annotated)

As annotated in Figures 4(c) and 5(b), Suzuki discloses sequential time instants at which each new set of switch selection signals produce a sum output voltage using gradation levels that momentarily best approximates "the instantaneous voltage values of the desired waveform" (smooth curve in Figure 5(b)) as required by claim 7. Ex. 1102, ¶ 177. It also discloses sequential switch selection signals sent at time instants that cause the new sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform than that caused by the immediately previously output set of switch selection signals.

As shown in Figure 8, Suzuki also discloses sequential time instants at which each new set of switch selection signals are sent to produce a sum output voltage using PWM control that best approximates "the instantaneous voltage values of the desired waveform" (smooth curve in Figure 8). *Id.*, ¶ 178.



Ex. 1126, Fig. 8 (annotated)

These sum output voltages at the time instants are the "best approximation . . . at the given instants" as recited in claim 7, and "a better approximation . . . at that time instant than the immediately previously output set of switch selection signals" as recited in claim 8, because: for gradational output voltage control (Figure 5(b)), the sum voltage is fixed as long as that value is the nearest approximation to the desired waveform and is set to the next adjacent value at the instant that value

becomes the nearest approximation; and for PWM (Figure 8), the voltage level and width of each pulse accurately approximate the instantaneous voltage and better approximates the instantaneous voltage than the previous pulse at the previous time instant. Ex. 1102, ¶ 179. Suzuki teaches these claims 7 and 8 limitations also because the sum voltage at the time instants match the desired waveform, a result that Suzuki could not have obtained without making the required "better" and "best" approximations.

Thus, the additional limitations of claims 7 and 8 are taught by Suzuki. *Id.*, ¶¶ 172-179.

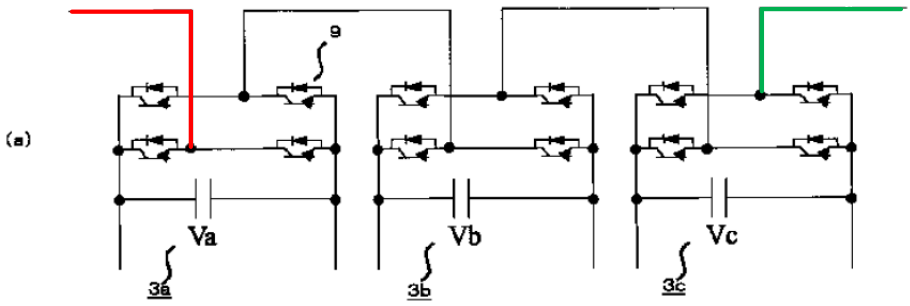
6. Claim 12

Claim 1 is taught by Suzuki. Section VII.A.1., s*upra*. Claim 12 further requires that "one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal." Ex. 1101, claim 12.

Suzuki discloses that input voltage Vc is the highest of the DC voltages ("Va<Vb<Vc"), for example disclosing the voltage ratios of 1:3:5 and 1:3:9 for voltages Va, Vb, and Vc, respectively. Ex. 1126, [0018]-[0019], Figs. 4-5; Ex. 1102, ¶ 183. Moreover, Vc is input into switch 3c, the output of which is one of the end

terminals of the series connection. Ex. 1126, [0018]-[0020], Fig. 14(a); Ex. 1102, ¶ 183.

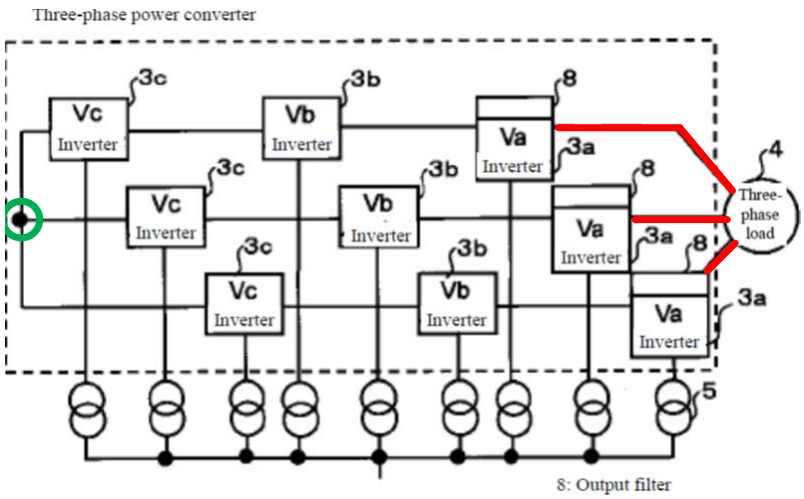
As discussed above, it would have been obvious that one of the output terminals of the inverter is neutral as taught by Suzuki because there are a limited number of options for connecting a single-phase inverter having a two-wire output to a residential single-phase AC electrical grid input. Section VII.A.1.c, *supra*. For example, and as shown below, the right output terminal (**green**) of the DC to AC converter as taught by Suzuki can represent neutral, in which this terminal is connected to the switches of single-phase inverter 3c, which is at the end of the series of inverters and has input voltage Vc. Ex. 1126, [0017]-[0019], Figs. 6, 14; Ex. 1102, ¶ 182.



Ex. 1126, Fig. 14(a) (annotated)

Furthermore, Suzuki teaches that three of its series-connected single-phase inverters can be connected in a three-phase system as shown in Figure 6 below. Ex. 1126, [0020], Fig. 6. As shown in Figure 6, the output terminal connected to the

three 3c inverters are connected together at a common point, while the other output terminals of the three inverters are connected to the three-phase load 4. *Id.*; Ex. 1102, ¶ 184. A PHOSITA would have understood that the common connection point (**green**) is "neutral" having the midpoint average voltage of the other three "hot" output terminals (**red**). Ex. 1102, ¶ 184; *See also* Ex. 1118, 11-12 (Exhibit 100.12).



Ex. 1126, Fig. 6 (annotated)

Figure 6 shows the 3c inverter (being associated with the highest voltage input) being attached to neutral. Even so, to a PHOSITA, it would have been obvious to have either output (left or right output of Figure 14(a)) be connected to neutral since there are only two possibilities (both of which are shown in Suzuki, *e.g.*, in Figures 1 and 6), and choosing between them would be a case of using an "obvious to try" solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success. Ex. 1102, ¶ 185. A PHOSITA would further have understood the benefits of connecting Suzuki's 3c

inverter, which has the highest DC voltage, to the neutral terminal (as shown in Figure 6) because this arrangement reduces electromagnetic interference produced due to inverter 3c's lower switching frequency. Ex. 1126, Figs. 4-6; Ex. 1102, ¶ 186.

Thus, Suzuki renders obvious the additional limitations of claim 12. Ex. 1102, ¶¶ 180-187.

B. Ground B: Claim 3 is Rendered Obvious by Suzuki in View of Nishimura

To the extent PO argues that Suzuki does not disclose claim 3 as shown above in Section VII.A.3., Suzuki in view of Nishimura discloses this claim.

Suzuki discloses that its inverter can provide a smooth AC output waveform to a load. Ex. 1126, [0001], [0005]-[0006], [0018]-[0019]; Ex. 1102, ¶ 193.

Like Suzuki, Nishimura discloses an inverter for converting DC to AC power using a bridge circuit. Ex. 1114, [0058]-[0059], Fig. 1; Ex. 1102 ¶ 194. Nishimura further discloses that its inverter can output at 50 Hz and 200V, which is a standard household voltage and frequency in Japan. Ex. 1114, [0058]; Ex. 1110, 22; Ex. 1102, ¶ 194.

It was obvious to use a known technique (producing an AC waveform with the voltage and frequency used in a standard household) to improve a similar device (Suzuki's inverter) in the same way (Suzuki produces a smooth AC output waveform). Ex. 1102, ¶¶ 195-196. A PHOSITA was familiar with designing an

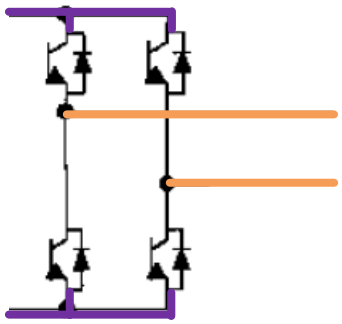
inverter to produce AC power for use in a household and had the skills to do so, providing an expectation of success. *Id.*, ¶ 197.

Thus, Suzuki in view of Nishimura renders claim 3 obvious. *Id.*, ¶¶ 188-198.

C. Ground C: Claim 6 is Rendered Obvious by Suzuki in View of Tolbert

Claim 1 is taught by Suzuki. Section VII.A.1, *supra*. Claim 6 depends from claim 1 and requires "the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value." Ex. 1101, claim 6.

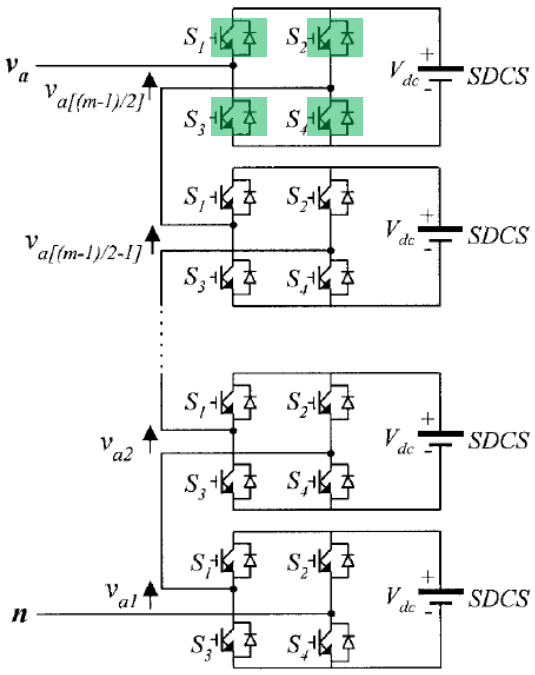
As discussed in Section VII.A.1.e above, Suzuki's H-bridges are controlled such that they output the supply voltage (V), the negative of the supply voltage (-V), or zero volts (0). Ex. 1126, [0017]-[0019], Figs. 4-5; Ex. 1102, ¶ 205. As shown in Figure 3(a), the H-bridges are a group of four transistors each receiving a signal (not shown) on its gate, which turns the transistor "on" or "off." By turning only certain transistors on, the H-bridge will be placed in either the "+1", "-1" or "0" states to output the +V, -V, and 0 volts, respectively. Ex. 1102, ¶ 205.



Ex. 1126, Fig. 3(a) (excerpted, annotated)

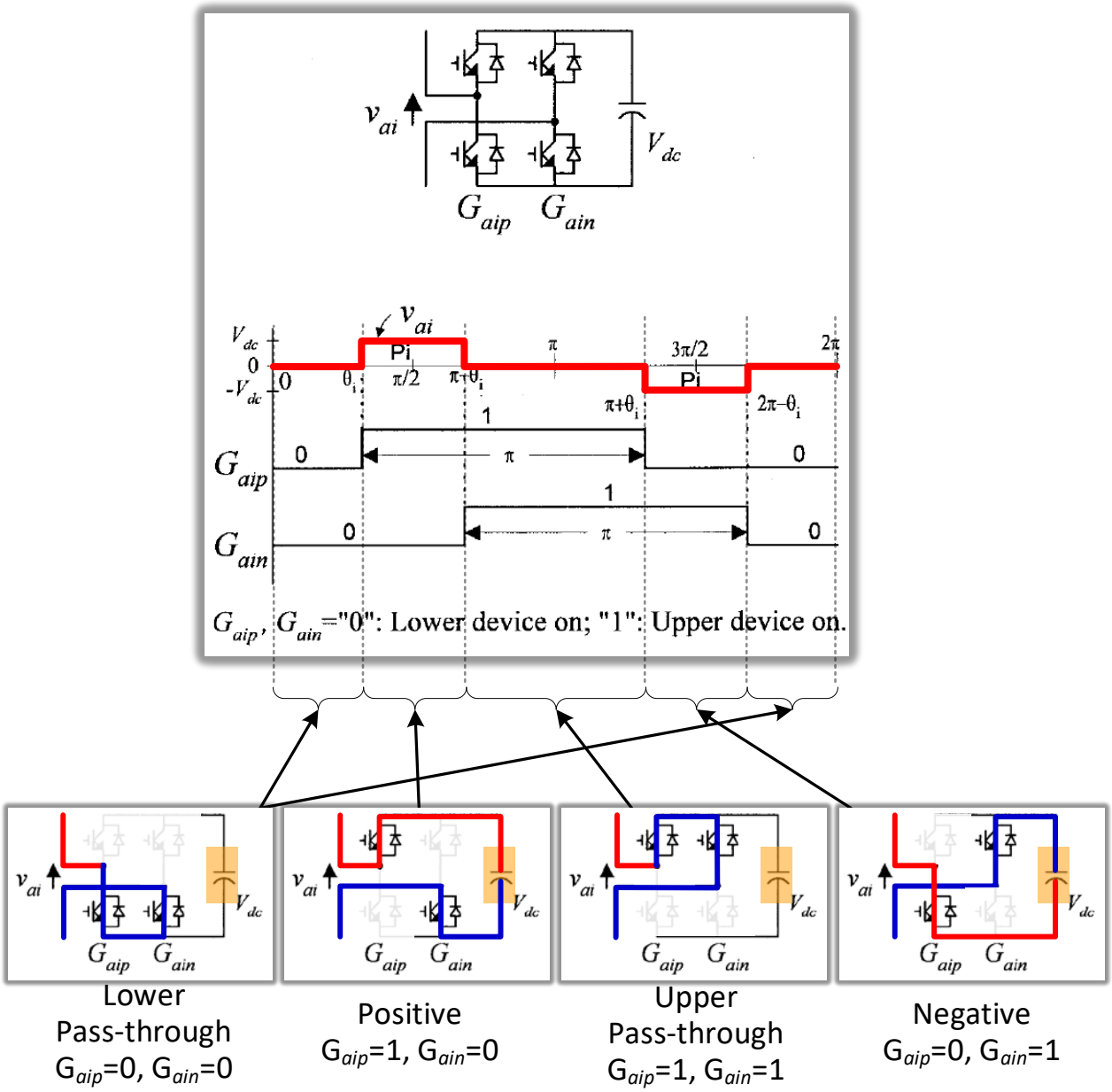
While Suzuki discloses that its ternary-valued selection signals control each H-bridge, and thus the four signals controlling the four transistors, Suzuki does not explicitly disclose that the ternary-valued selection signals comprise pairs of binary bits as recited in claim 6. Ex. 1102, ¶ 206. However, this was a common control scheme for H-bridge switches, and is disclosed by Tolbert. *Id.*

Tolbert, like Suzuki, teaches a power converter that uses H-bridges in an inverter to output one of three levels: -V, 0, or +V, based on a combination of ON and OFF states of the transistors in the H-bridge. Ex. 1131, p. 37, Fig. 1 (transistors S_1-S_4, highlighted **green** below); Ex. 1102, ¶ 207.



Ex. 1131, Fig. 1 (annotated)

Tolbert discloses that each H-bridge is controlled to output +V, 0, and –V according to 2 bits—G_{aip} which controls transistors S_1 and S_3 on the left in opposite states and G_{ain} which controls transistors S_2 and S_4 on the right in opposite states. Ex. 1131, Figs. 1, 2b, pp. 37-38; Ex. 1102, ¶ 208. For each side of the H-bridge, a bit value of 1 turns on the upper transistor and turns off the lower transistor, and a bit value of 0 turns off the upper transistor and turns on the lower transistor. Ex. 1131, Fig. 2b; Ex. 1102, ¶ 208. These pairs of bits (G_{aip} and G_{ain}) have "four combinations of possible values" and control the H-bridge sequentially into the lower pass-through (zero) state (G_{aip}, G_{ain} = 0, 0), the positive state (G_{aip}, G_{ain} = 1, 0), the upper pass-through (zero) state (G_{aip}, G_{ain} = 1, 1), and the negative state (G_{aip}, G_{ain} = 0, 1), as shown below:



Ex. 1131, Fig. 2(b) (annotated)

As illustrated in Figure 2(b), the lower pass-through and the upper pass-through states correspond to zero volts on v_{ai} (**red** line), thus disclosing the claim 6 feature of "two of the four combinations represent the zero multiplier value." Ex. 1102, ¶ 209.

A PHOSITA would have been motivated to use Tolbert's two-bit control signal encoding in Suzuki because it is efficient and because Tolbert teaches this sequence can be used to cause all of the switching devices in the H-bridge to conduct with equal times, thus making the stress on each device equal. Ex. 1131, pp. 37-38; Ex. 1102, ¶ 210. This is an obvious combination of prior art elements (Suzuki's H-bridge switches and Tolbert's two-bit control signal) in a known manner (providing Tolbert's two-bit control signal to control Suzuki's H-bridges) to achieve predictable results (the H-bridges receive a two-bit encoded signal that enables the generation of four states: positive, negative, and two zero states). Ex. 1102, ¶¶ 210-211, 85-86, 102.

This modification was within the skill set of a PHOSITA, who was familiar with H-bridge switches and basic control logic needed to implement the two-bit control signals, providing a reasonable expectation of success. *Id.*, ¶ 211.

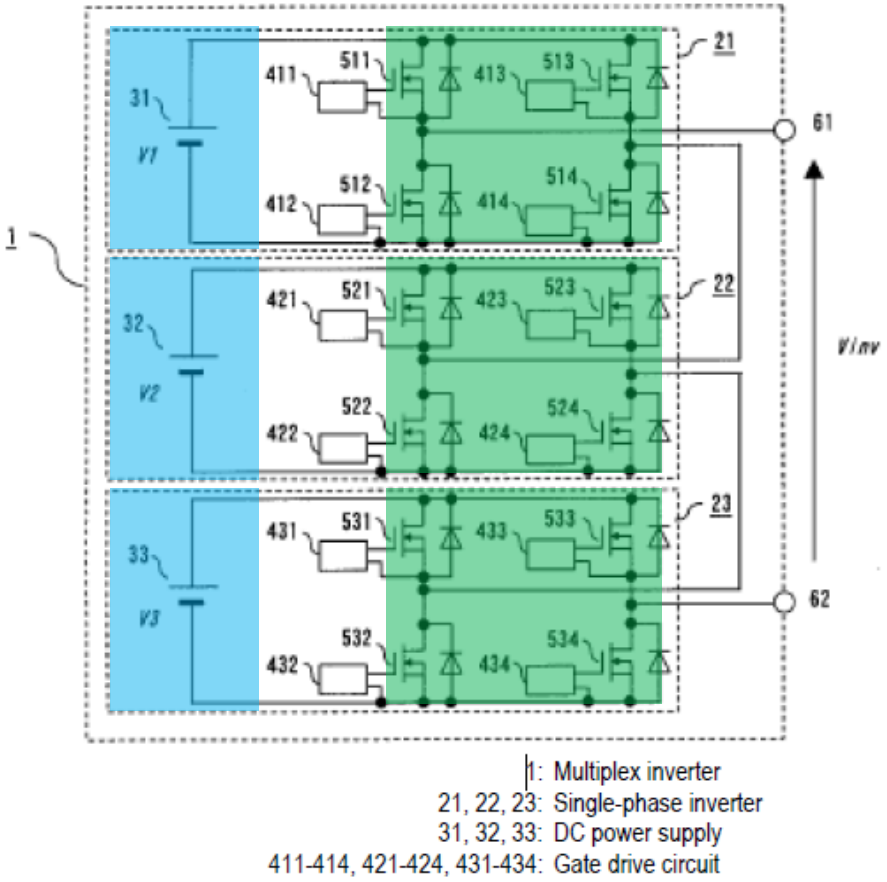
Thus, the combination of Suzuki in view of Tolbert renders obvious claim 6. Ex. 1102, ¶¶ 199-212.

D. Ground D: Claims 7-8 are Rendered Obvious by Suzuki in View of Mori '630

1. Claims 7 and 8

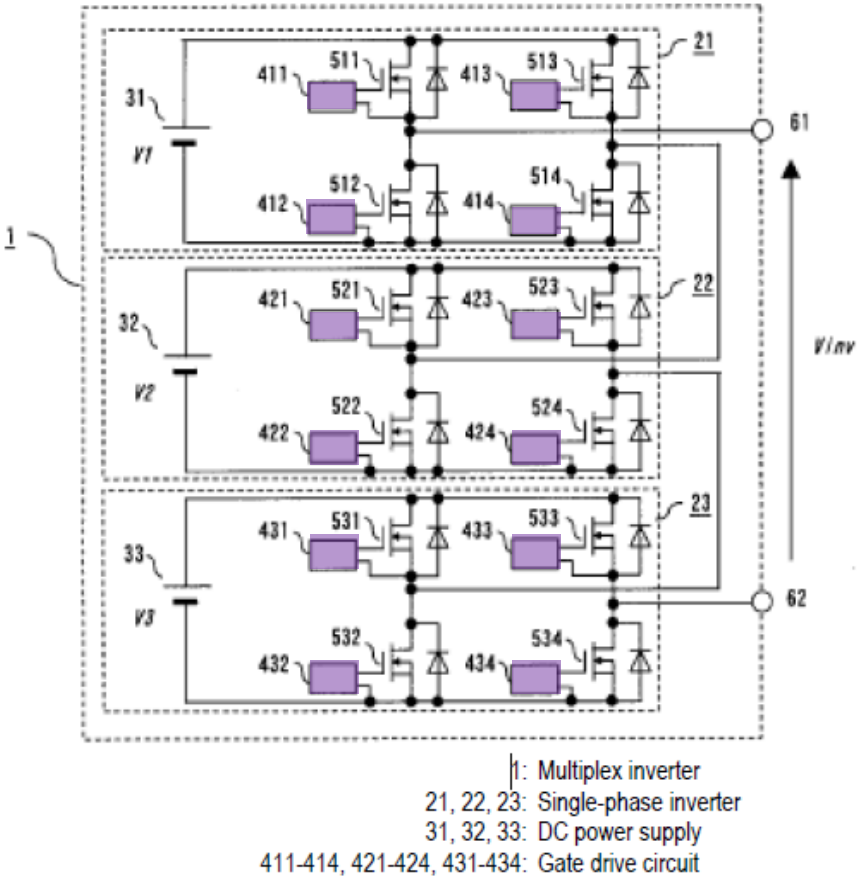
To the extent PO argues that Suzuki does not disclose claims 7 and 8 as shown above in Section VII.A.5., Mori '630 discloses these claims.

Mori ’630, like Suzuki, teaches an inverter comprising series connected individual single-phase inverters (**green**) consisting of H-bridges and attached to a respective DC power source (**blue**), as shown below. Ex. 1106, [0009]-[0010], claim 1, Fig. 1; Ex. 1102, ¶ 219.



Ex. 1106, Fig. 1 (annotated)

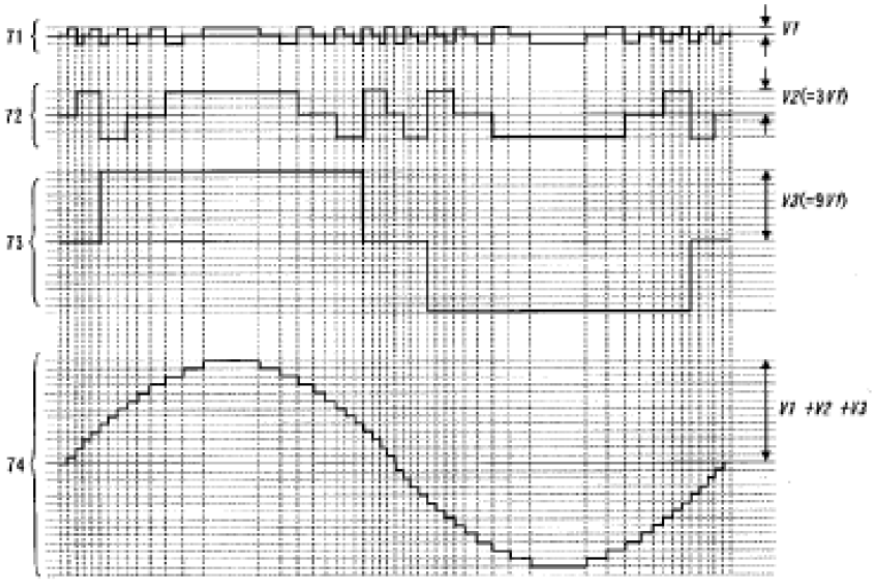
Mori ’630 further describes gate drive circuitry (**purple** below) that applies a predetermined voltage for turning each switch on and off based on a gate drive signal generated by a control circuit (*i.e.*, a “switch signal generator”). Ex. 1106, [0010], [0011], [0015]-[0033], Figs. 1, 4, 9-10, 13, 15; Ex. 1102, ¶ 220.



Ex. 1106, Fig. 1 (annotated)

Mori ’630 also teaches this gate control signal is a set of ternary-valued selection signals (+1, 1, 0) that control the plurality or set of H-bridge switches at given time instants so that the sum output of those switches provides an approximation to the instantaneous voltage values of the desired waveform. Ex. 1106, [0009], [0011]-[0012], [0015], [0018]-[0022], [0029], [Solution]; Ex. 1102, ¶ 221. Figure 2, for example, shows a sum voltage output (74) approximating a desired sinusoidal waveform when H-bridge output voltages V1-V3 are set to 1V, 3V, and 9V, respectively (the same voltage ratio disclosed in Suzuki and the ’710

patent). Ex. 1106, [0011]-[0012], [0019]; Ex. 1126, [Summary], [0018]-[0019], Figs. 4-5; Ex. 1102, ¶ 221.



Ex. 1106, Fig. 2

Implementing Suzuki, which requires the receipt by the H-bridge switches of control signals to create the three possible states for each H-bridge (+1, -1, 0), with the control circuit of Mori ’630, which generates that same type of control signal was an obvious combining of prior art elements (the control circuit of Mori ’630 with Suzuki’s inverter) according to known methods (Suzuki’s system, which uses such control signals for its H-bridge switches) to yield predictable results (the H-bridges receive the appropriate control signals at the appropriate time to generate a sum output voltage that approximates the desired waveform). Ex. 1102, ¶ 222.

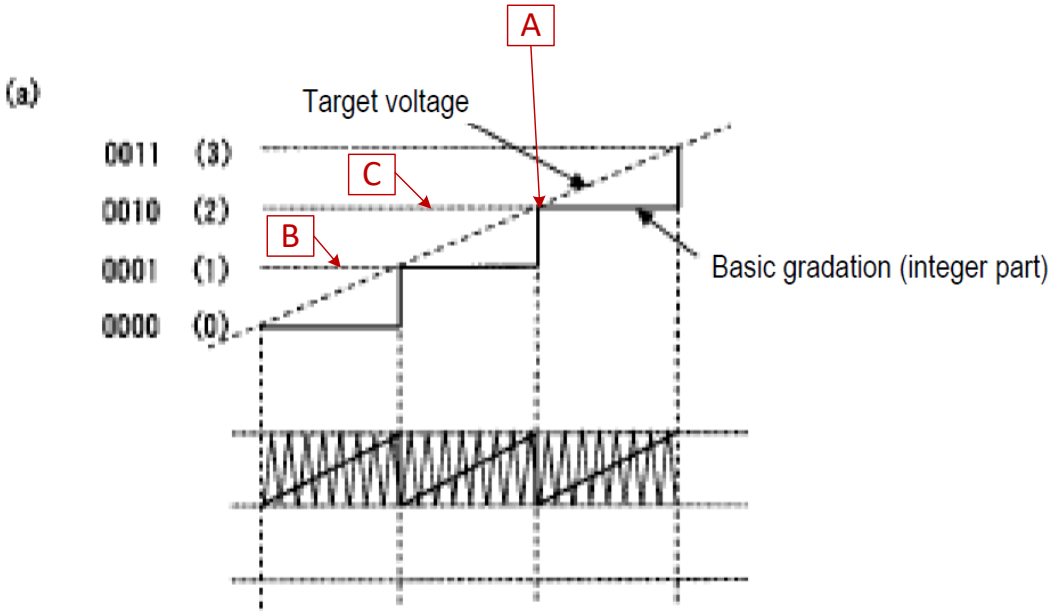
To the extent that the “switch selection signal generator” is a means-plus-function term, it is still met by the proposed combination. As explained above, the

function recited in the claim following the words "configured to" are performed by the proposed combination. *Id.*, ¶ 223. To the extent there is corresponding structure in the '710 patent for producing these signals, it is controller 200, which includes a microcontroller, or an equivalent structure that sends the signals to switch driving circuits. Ex. 1101, 12:54-56, 13:45-47, Fig. 1; Ex. 1102, ¶ 223. Mori '630 similarly discloses a control circuit 9, which includes a microcomputer or a microcomputer-based controller that sends signals to gate drive circuits. Ex. 1106, [0010], [0015], Figs. 4, 9, 10, 13, 15; Ex. 1102, ¶ 223. Mori '630's control circuit is the equivalent structure of the '710 patent's switch selection signal generator. Ex. 1102, ¶¶ 223-224. Further, combining Suzuki's inverter, which requires control signals to control the states of for each H-bridge, with Mori '630's control circuit and its structure, which generates the necessary control signals, is the obvious improvement of a similar device (Suzuki's system) in the same way (sending gate drive signals to switch driving circuits). A PHOSITA had the skills to implement this known control circuit structure, providing a reasonable expectation of success. *Id.*

Thus, whether or not "switch selection signal generator" is a means-plus-function term, the combination of Suzuki-Mori '630 discloses the claims 7 and 8 feature of "a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce [sequential] sets of switch selection signals."

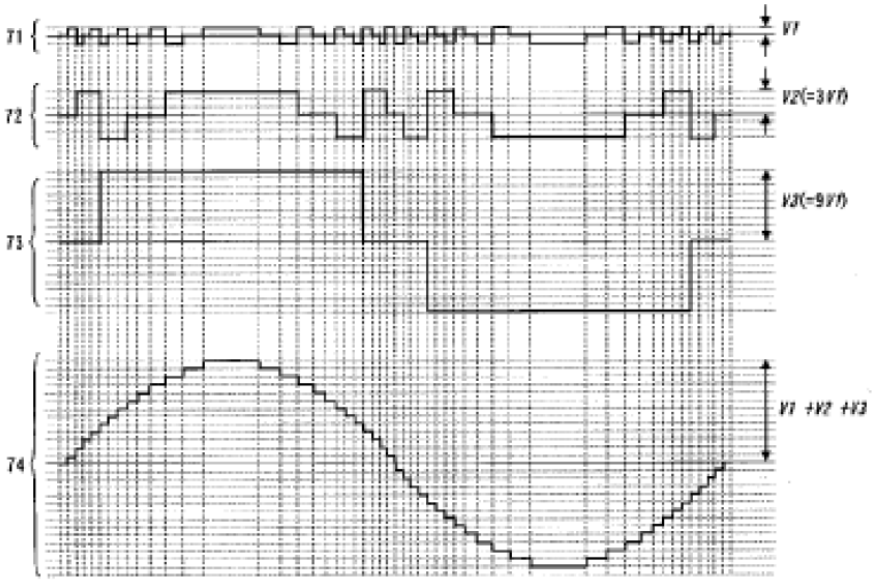
Claim 7 further requires the sets of switch selection signals to be produced "at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants." Ex. 1101, claim 7. Claim 8 further requires the sets of switch selection signals to be "sequential" and the generator to be "configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals." Ex. 1101, claim 8.

Mori '630 discloses various methods to calculate the sequential sets of control signals. Ex. 1106, [0021]-[0022], [0028]-[0031], Figs. 2, 8, 12, 14; Ex. 1102, ¶ 226. For example, Figure 8 of Mori '630 below shows the target voltage (the "desired waveform") and basic gradation output (the "sum output voltage"), which changes at each time instant (*e.g.*, "A") to a new value (e.g., "C") that equals the target voltage, from a previous value (e.g., "B") that is less than the target voltage so that sum output voltage equals the target voltage at each time instant and further using PWM control to improve the approximation. Ex. 1106, [0020]-[0021]; Ex. 1102, ¶ 226.



Ex. 1106, Fig. 8(a)

As another example, Figure 2 shows a similar result but using only the integer gradation. Ex. 1106, [0012], Fig. 2; Ex. 1102, ¶ 226.



Ex. 1106, Fig. 2

In this manner, Mori ’630’s control circuit produces sets of switch selection signals in which “the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants” as recited in claim 7, and produces sequential sets of switch selection signals in which each “new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals” as recited in claim 8. Ex. 1101, claims 7, 8; Ex. 1102, ¶ 227.

Thus, Suzuki-Mori ’630 renders claims 7 and 8 obvious. Ex. 1102, ¶¶ 213-228.

E. Grounds E and F: Claim 9 is Rendered Obvious by Suzuki and Suzuki-Mori ’630, Each in View of Kumar

Claim 8 is taught by Suzuki and by Suzuki-Mori ’630. Sections VII.A.5., *supra*. Claim 9 depends from claim 8, and recites: “[the] DC to AC . . . further comprising, where the desired waveform is repetitive: memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output; and wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times.” Ex. 1101, claim 9.

As discussed above in Sections VII.A.1.f and VII.D.1, Suzuki and Suzuki-Mori '630 teach an inverter that outputs an approximate sinewave (the recited "where the desired waveform is repetitive") using PWM control. Mori '630 further teaches that its control circuit 9 includes a PWM controller implemented with a CPU and PLD, which a PHOSITA would understand to include memory. Ex. 1106, [0015]; Ex. 1102, ¶ 235.

Kumar also teaches a programmed PWM controller ("switch selection signal generator") for controlling a DC/AC inverter. Ex. 1128, 1:6-16, 4:49-56; Ex. 1102, ¶ 236. Kumar teaches a sequence of switching signals that are output to control the state of the inverter's individual switches. Ex. 1128, 4:49-53, 6:17-50; Ex. 1102, ¶ 236.

Kumar's controller includes multiple memories (PROMs) containing data tables as well as a microprocessor, writable timing circuits, an address counter, and other circuitry. Ex. 1128, 4:49-5:23, Fig. 1; Ex. 1102, ¶ 237.

Specifically, a first PROM of the controller stores a set of "pattern tables" containing firing pattern signals defining the on/off status of the inverter's switching devices, and a second PROM stores a set of "angle tables" storing transition times for the inverter control signals (the recited "memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output"). Ex. 1128, 4:56-62, 5:53-67; Ex. 1102, ¶ 238. Based on

the required frequency and voltage of the AC signal, the microprocessor selects the pattern and angle table to be used. Ex. 1128, 6:5-15; Ex. 1102, ¶ 238. The microprocessor loads the beginning address of the pattern table into the address counter and the transition times from the angle table are written into the timing circuits. Ex. 1128, 5:41-66; Ex. 1102, ¶ 238. As the timing circuits time out the address counter is advanced and the PROM sequences through the firing signals of the pattern table which are output to the inverter. Ex. 1128, 5:7-23, 5:39-40; Ex. 1102, ¶ 238.

A PHOSITA would have been motivated to implement Suzuki and Suzuki-Mori ’630’s signal generator to include the memory and stored value and time data of Kumar’s programmed PWM controller because using a series of precomputed signals simplifies the control arrangement and is inexpensive and versatile. Ex. 1128, 1:63-2:6; Ex. 1102, ¶ 239. This modification represents the combination of prior art elements (the switch selection signal generator of Suzuki or Suzuki-Mori ’630 and the use of Kumar’s programmed controller) in a known manner (programming the signal generator to store and retrieve the precomputed signals using the pre-stored timing sequence) to achieve predictable results (the reliable and straightforward generation of a series of control signals at the appropriate times). Ex. 1102, ¶¶ 239-240.

Implementing the switch selection signal generators and generating gating signals according to Kumar as described above required nothing more than the use of basic digital logic and memory devices, which a PHOSITA was familiar with, providing a reasonable expectation of success. *Id.*, ¶ 240.

To the extent the "switch selection signal generator" is a means-plus-function term in claim 9, Suzuki-Mori '630-Kumar teaches this element for the same reasons described in claim 7. Section VII.D.1, *supra*. Additionally, Kumar teaches the same, or equivalent memories as disclosed in the '710 patent. *Id.*, ¶ 241.

Thus, Suzuki and Suzuki-Mori '630, each in combination with Kumar renders obvious claim 9. *Id.*, ¶¶ 229-242.

F. Ground G: Claims 10-11 are Rendered Obvious by Suzuki in View of Ball

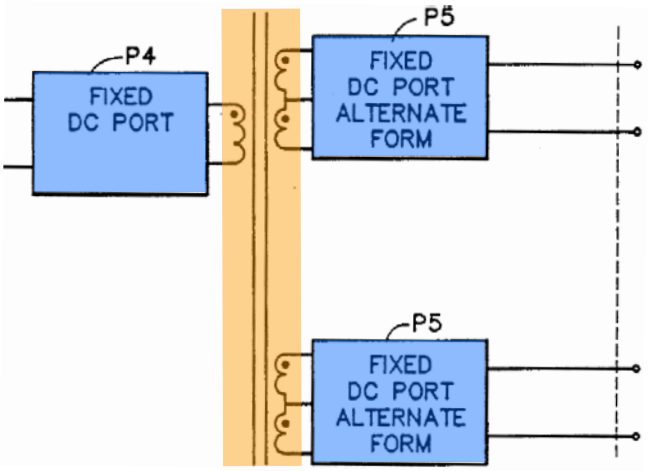
1. Claim 10

Claim 1 is taught by Suzuki. Section VII.A.1, *supra*. Claim 10 depends from claim 1 and requires "the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery." Ex. 1101, claim 10.

While Suzuki teaches using AC-to-DC converters to derive the DC voltage inputs to its H-bridge circuits from an AC power source (Ex. 1126, [0016]), a PHOSITA would have recognized that rather than using an AC power source to

indirectly provide the DC voltage inputs, a DC power source, such as the battery of Ball, could be used to directly provide the DC voltage inputs. A PHOSITA would have known, *e.g.*, that a battery could provide the DC voltage input directly to Suzuki's highest voltage inverter 3c and the additional lower DC voltages could be derived through DC-to-DC conversion. Ex. 1102, ¶ 249.

Ball discloses a universal converter with a transformer (**orange**) that transfers power between two or more bi-directional fixed DC voltage ports (**blue**) (or other types of AC and AC/DC combination ports) and can be powered by a battery. Ex. 1127, 11:26-12:22, 21:20-32, 23:33-34; Ex. 1102, ¶ 250.



Ex. 1127, Fig. 20 (excerpted and annotated).

One of Ball's fixed DC voltage ports is connected to a battery and controlled to generate a high frequency, equal duty cycle, square wave on its transformer winding with an amplitude equal to the voltage output by the battery. Ex. 1127, 12:5-22, 21:33-51; Ex. 1102, ¶ 251. The other ports lock onto this square wave

through their transformer windings to transfer power bi-directionally between the ports, where the ratio of DC voltages between the ports is determined by the ratio of turns on the transformer. Ex. 1127, 32:52-68, 42:5-13; Ex. 1102, ¶ 251. Each of the ports is floating with respect to the other ports because the ports are isolated from each other by the transformer coupling and further isolation is provided by transformer isolation of the signals controlling the ports. Ex. 1127, 11:1-4, 24:1-8, Figs. 16, 20, 22; Ex. 1102, ¶ 251. Ball also describes how its universal converter can be used in conjunction with a battery in an uninterruptible power supply (Figure 16) as well as illustrates use of a battery in a rural power control system (Figure 22). Ex. 1127, 48:15-45, 50:62-51:9, Figs. 16, 22; Ex. 1102, ¶ 252.

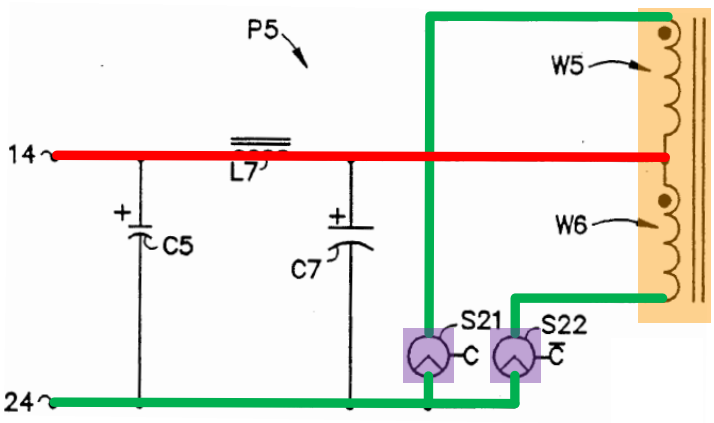
A PHOSITA would have been motivated to use Ball's battery and universal converter to power Suzuki's H-bridges, because Ball's universal converter is capable of providing any required number of floating DC voltages (such as are used by Suzuki), and because the battery of Ball as a DC power source allows for the use of Suzuki as an uninterruptible power supply. Ex. 1127, 48:15-45; Ex. 1102, ¶ 254.

A PHOSITA would have had a reasonable expectation for success in combining Suzuki with Ball, since Ball describes precisely how its circuit is controlled and structured with schematics and how to set the ratio of voltages at its ports (with the ratio of the transformer windings) to the ratios required by Suzuki (*e.g.*, 9:3:1). Making the circuit connections of Ball's DC voltage ports to Suzuki's

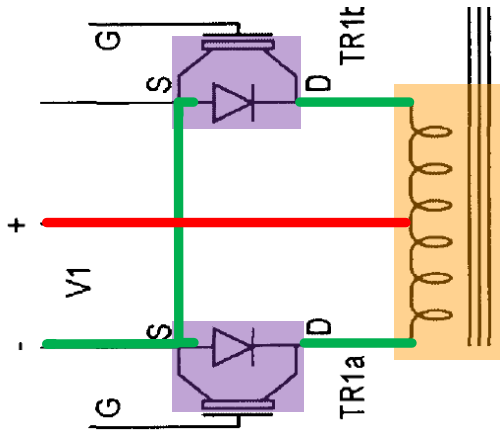
H-bridge voltage inputs are basic engineering skills of a PHOSITA. Ex. 1102, ¶ 255.

To the extent that the "bi-directional DC-DC conversion circuitry" of claim 10 is a means-plus-function term, Ball discloses an equivalent structure. Ex. 1127, Fig. 8; Ex. 1102, ¶ 256. As explained above, the function recited in the claim following the words "operative to" are performed by the proposed combination. Ex. 1102, ¶ 256. To the extent there is corresponding structure in the '710 patent for deriving the lower voltage values from the battery, it is Figure 2, which includes windings, which have turns ratios in proportion to the voltage ratios. Ex. 1101, 19:41-43, 20:9-28, Fig. 2; Ex. 1102, ¶ 256.

The structure of Ball's converter with multiple fixed DC voltage ports (left) is identical to, or insubstantially different from, that of the '710 patent's bidirectional DC-DC converter port (right), with a coil (**orange**) coupled to a central transformer, a center tap of the coil connected to a positive terminal (**red**), and ends of the coil coupled to a negative terminal (**green**) through respective MOSFET switches (**purple**). Ex. 1101, 19:36-20:2; Ex. 1127, 38:60-39:17, 39:29-40, 39:67-40:7, 40:17-19, 42:7-36, Figs. 2, 3, 8, 13; Ex. 1102, ¶ 257.



Ex. 1127, Fig. 8 (annotated)



Ex. 1101, Fig. 2 (excerpt, annotated)

These fixed DC voltage ports are controlled in the same manner with a high frequency square wave signal driving respectively the gates of the two MOSFET switches (*e.g.*, S21/S22 in Ball or Tr1a/Tr1b in the '710 patent) in each port. Ex. 1101, 19:39-20:2; Ex. 1127, 22:12-20, 34:59-35:4, 40:30-36, 40:48-51, 42:8-12, 44:34-42, 44:52-60, 46:8-14, 53:20-26, Figs. 8, 12, 13; Ex. 1102, ¶ 258. Voltages on the inputs/outputs of the fixed DC voltage ports are also determined the same way—by the turn ratios of the port's respective coils. Ex. 1101, 19:41-44; Ex. 1127, 42:8-12, 44:52-60, 53:20-26; Ex. 1102, ¶ 258.

Thus, the additional limitations of claim 10 are taught by Suzuki in view of Ball. Ex. 1102, ¶¶ 243-259.

2. Claim 11

Claim 1 is taught by Suzuki. Section VII.A.1, *supra*. Claim 11 depends from claim 1 and requires "the DC power source supplying the highest mean power is a

battery and the DC power sources supplying lower mean power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery." Ex. 1101, claim 11.

As explained with respect to claim 10, Suzuki-Ball discloses a universal converter that transfers power between two or more bi-directional fixed DC voltage ports and can be powered by a battery. Ex. 1127, 11:26-12:22, 21:20-32; Ex. 1102, ¶¶ 249-252.

While claim 10 focuses on the *voltage value* of the different DC power supplies, claim 11 focuses the *mean power* of the difference DC power supplies. *See* Ex. 1101, claims 10, 11. But in the context of Suzuki's inverter, this is not a meaningful distinction. Ex. 1102, ¶ 253. Mean power is the average power output over a certain time period, and power is calculated by multiplying the voltage by the current. Ex. 1102, ¶ 253. In Suzuki, the DC power source Vc is taught to have a voltage higher than the other two power sources (Va and Vb), for example so that the voltage ratio for the three sources is 1:3:9, and the switches are controlled in such a way that the mean power of that source (which is proportional to the voltage because the three sources share the same current) would be higher than the other two. Ex. 1126, [0018]-[0019], Fig. 4; Ex. 1102, ¶ 253. This is the same as is disclosed in the '710 patent, that also has a voltage ratio of 1:3:9 and a similar switching pattern. *See, e.g.*, Ex. 1101, 11:5-18, Fig. 4; Ex. 1102, ¶ 253.

Also as explained with respect to claim 10, to the extent that the "bi-directional DC-DC conversion circuitry" of claim 11 is a means-plus-function term, Ball discloses an equivalent structure. Section VII.F.1, *supra*.

Thus, the additional limitations of claim 11 are taught by Suzuki in view of Ball. Ex. 1102, ¶¶ 243-259.

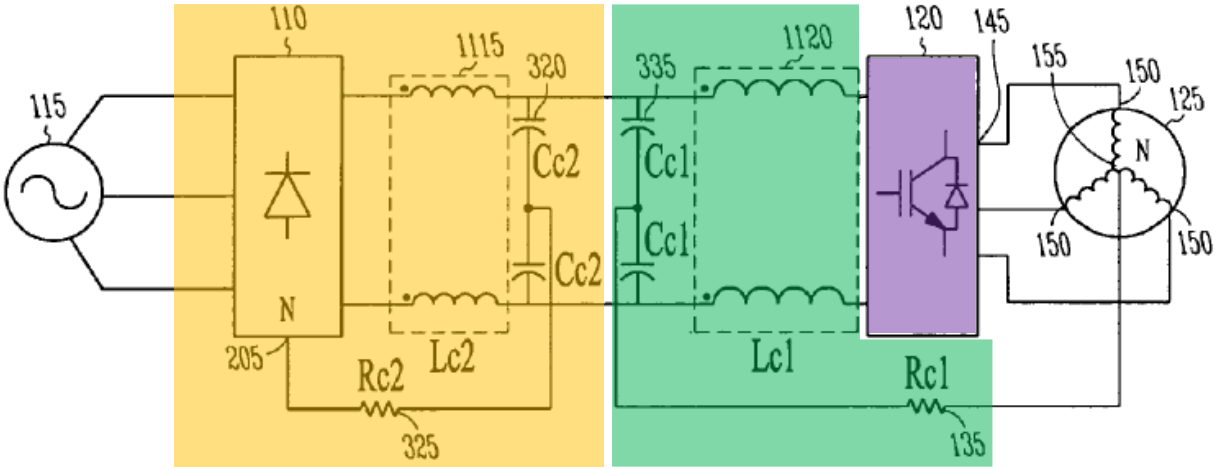
G. Ground H: Claim 13 is Rendered Obvious by Suzuki-Ball in view of De

Claim 1 is taught by Suzuki. Section VII.A.1, s*upra*. Claim 13 depends from claim 1 and requires "the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch." Ex. 1101, claim 13.

As explained above with respect to claims 10 and 11, Suzuki-Ball teaches using a battery (*e.g.*, in a UPS) as the DC power source for Suzuki's inverter 3c H-bridge (controlled switch). Ex. 1126, [0017]-[0019]; Ex. 1127, 48:15-45, 50:62-51:9, Figs. 16, 22; Ex. 1102, ¶ 265. This combination as disclosed above thus teaches "wherein the associated DC power source of one of the controlled switches is a battery." Section VII.F, *supra*.

De discloses a common mode filter (**green**), including a common mode inductor 1120 and capacitors 335, interposed between a DC power source (**orange**) and an inverter 120 (**purple**), such as between Suzuki's inverter 3c and DC power

source as further recited in claim 13. Ex. 1129, [0020], [0033]-[0034], Figs. 11-12; Ex. 1102, ¶ 266.



Ex. 1129, Fig. 12 (annotated)

De also discloses that an inverter is a source of electromagnetic interference (EMI) in the form of common mode noise (voltage and current). Ex. 1129, [0001], [0022]; Ex. 1102, ¶ 267. A PHOSITA would have been motivated to add De's common mode filter between the battery (*e.g.*, Ball's UPS battery and other DC power sources) and Suzuki's inverter (including the 3c H-bridge) to suppress common-mode currents and minimize EMI. Ex. 1129, [0020]-[0022]; Ex. 1102, ¶¶ 268-269.

As such, Suzuki-Ball combined with De represents the obvious use of a known technique (inserting De's common mode filter between a power source and inverter) to improve a similar device (Suzuki's inverter fed by Ball's battery) in the same way (by suppressing the common mode current and EMI emitted by Suzuki's

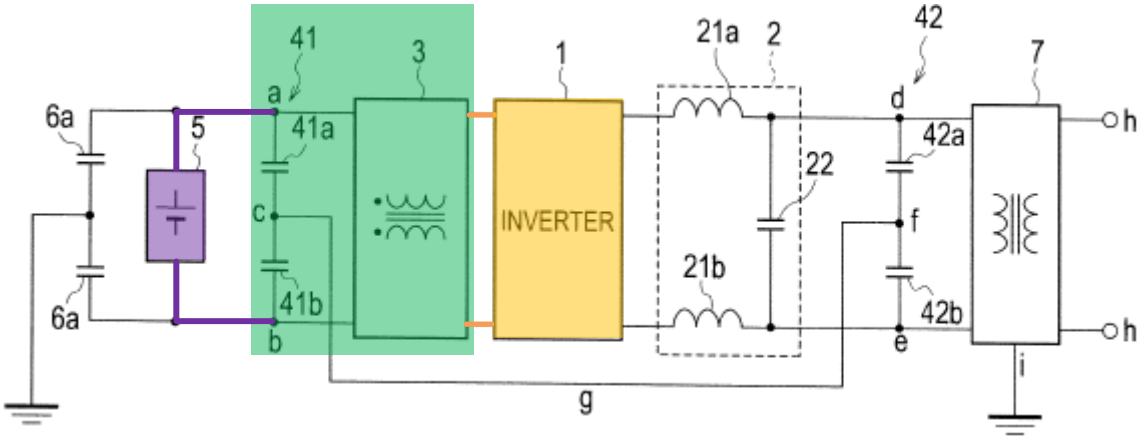
inverter). The combination merely requires inserting additional filter components and adjusting component values, which was well within the level of ordinary skill in the art. Ex. 1102, ¶¶ 260-270.

H. Ground I: Claim 13 is Rendered Obvious by Suzuki-Ball in view of Koyama

To the extent PO argues that Suzuki-Ball-De does not disclose claim 13 as shown above in Section VII.G, Suzuki-Ball in view of Koyama discloses this claim.

As explained above, Suzuki-Ball teaches using a battery (*e.g.*, in a UPS) as the DC power source for Suzuki's inverter 3c H-bridge (controlled switch). Ex. 1126, [0017]-[0019]; Ex. 1127, 48:15-45, 50:62-51:9, Figs. 16, 22; Ex. 1102, ¶ 276. This combination as disclosed above thus teaches "wherein the associated DC power source of one of the controlled switches is a battery." Section VII.F, *supra*.

Koyama discloses a common mode filter (**green**) interposed between an inverter 1 (**orange**) and a floating DC power source 5 (**purple**), such as between Suzuki's inverter 3c and DC power source as further recited in claim 13. Ex. 1113, [0005]-[0007], [0012]-[0013], [0024]-[0026], [0030]-[0031], [0036]-[0038], Figs. 1, 4, 5; Ex. 1102, ¶¶ 272, 277.



Ex. 1113, Fig. 5 (annotated).

Koyama explains that floating DC power sources (described as a solar cell, fuel cell, or battery) may include stray capacitances 6 between the terminals of the DC power source and ground, which can provide a path for common mode leakage current. Ex. 1113, [0012]-[0013], [0002]-[0005], [0016]-[0018], [0026], [0036]-[0038]; Ex. 1102, ¶ 278. Moreover, common mode noise generated by the inverter may cause impermissible electromagnetic interference (EMI). Ex. 1102, ¶ 279. A PHOSITA would have been motivated to add Koyama's common mode filter between the battery (*e.g.*, Ball's UPS battery and other DC power sources) and Suzuki's inverter (including the 3c H-bridge) to suppress common-mode currents and minimize EMI. Ex. 1113, [0012]-[0013], [0019]-[0021]; Ex. 1102, ¶ 279.

As such, Suzuki-Ball combined with Koyama represents the obvious use of a known technique (inserting Koyama's common mode filter between a power source and inverter) to improve a similar device (Suzuki's inverter fed by Ball's battery) in

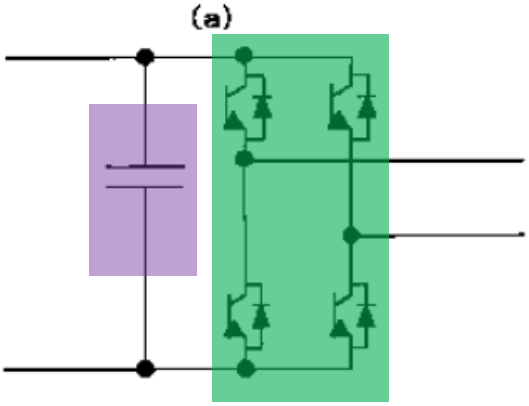
the same way (by suppressing the common mode current and EMI emitted by Suzuki's inverter). The combination merely requires inserting additional filter components and adjusting component values, which was well within the level of ordinary skill in the art. Ex. 1102, ¶¶ 271-281.

I. Ground J: Claims 14-15 are Rendered Obvious by Suzuki-Ball in view of Koyama and Ahmed

Claim 12 is taught by Suzuki. Section VII.A.6, s*upra*. Claim 14 depends from claim 12, and claim 15 depends from claim 14. Claims 14 and 15 recite specific circuit components of "the common mode filter" connected between "DC power input terminals of the controlled switch" and "the battery," but there is no antecedent common mode filter or battery in claim 12, from which claims 14 and 15 depend. Ex. 1102, ¶ 288. Regardless, Suzuki-Ball in view of Koyama and Ahmed renders claims 14 and 15 obvious. Ex. 1102, ¶¶ 282-298.

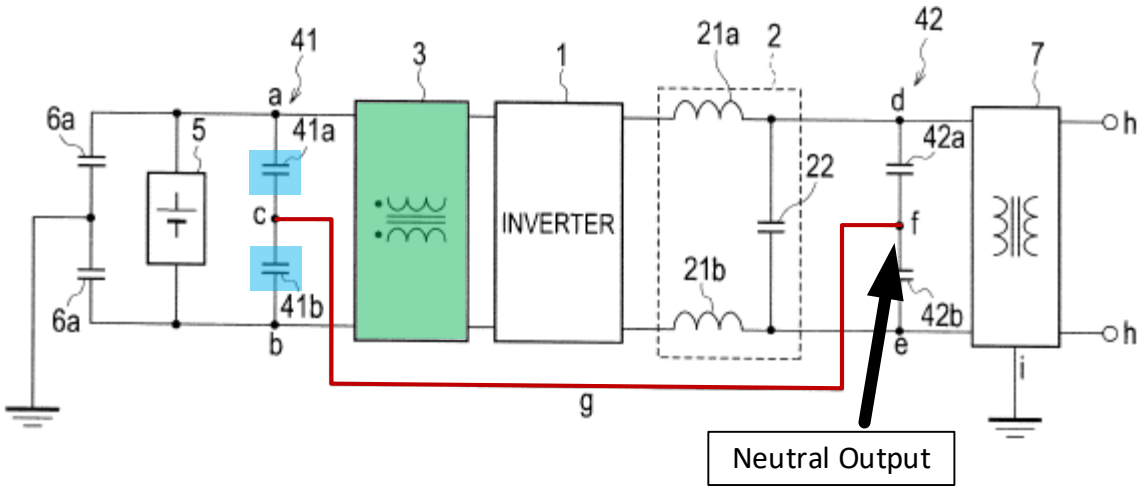
As explained above with respect to claim 13, it was obvious to connect Koyama's common mode filter between a DC power source (a battery as disclosed in Suzuki-Ball) and the Suzuki inverter to reduce the common mode current and EMI emitted by the inverter. Section VII.H, *supra*. Ex. 1102, ¶ 289.

Further, Suzuki-Ball and Koyama, combined with Ahmed, teach the common mode filter structures of claims 14 and 15. As shown below, Suzuki teaches (in **purple**) the claim 14 "capacitor connected between DC power input terminals of a controlled switch" (in **green**). Ex. 1126, [0017], Fig. 3(a); Ex. 1102, ¶ 290.



Ex. 1126, Fig. 3(a) (annotated)

Koyama, as shown below discloses the claim 14 "common-mode choke" (**green)** connected between a DC power source 5 (*e.g.*, Suzuki-Ball's battery) and the DC power input terminals of the controlled switch 1 (*e.g.*, Suzuki's 3c H-bridge). Ex. 1113, [0029], [0036]-[0038], Figs. 4, 5; Ex. 1102, ¶ 291.



Ex. 1113, Fig. 5 (annotated).

Koyama also teaches the claim 14 "first pair capacitors [**blue**] connected respectively from positive and negative terminals of the battery [*e.g.*, Suzuki-Ball's

Battery as DC power source 5] to the neutral output terminal [Suzuki's neutral output terminal as AC neutral point f]." Ex. 1113, [0024]-[0026], [0030]-[0031], [0035]-[0038], Figs. 4, 5; Ex. 1102, ¶ 292.

Ahmed teaches to modify Koyama's first pair of capacitors to add a damping circuit meeting the remaining claim 14 and 15 limitations. Specifically, Ahmed identifies the problem in filters such as that disclosed in Koyama of resonance between inductors and capacitor components, which may lead to ringing, voltage overshoot and instability at particular resonant frequencies. Ex. 1112, Abstract, 6; *see also* Ex. 1120, [0018]-[0019], [0027]; Ex. 1102, ¶ 293. To reduce this resonance, *e.g.*, Ahmed teaches that an LC filter as shown on the left in the figures below can be modified by adding a series-connected resistor and capacitor (**blue**), or additionally modified with an additional inductor in parallel with the resistor (**green**). Ex. 1102, ¶ 293.

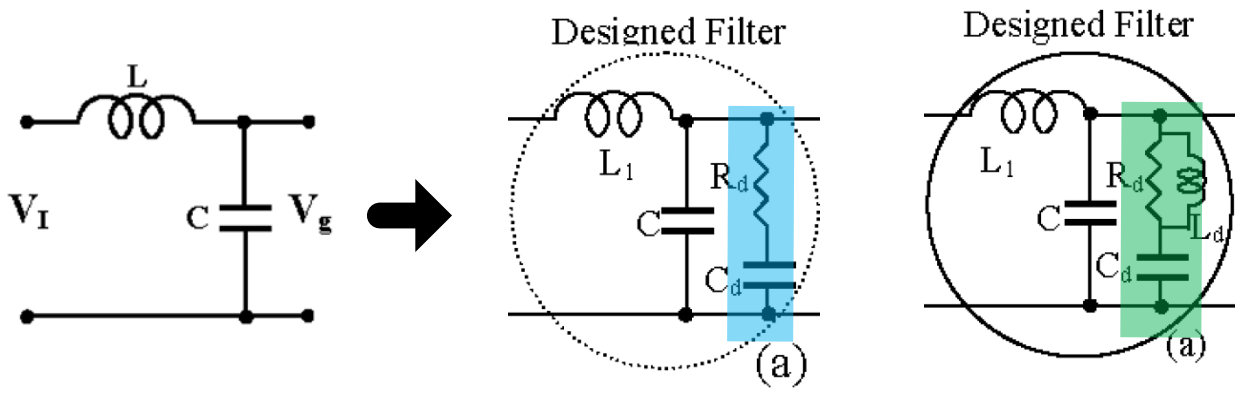


Fig. 2(b) (excerpt) Fig. 14(a) (excerpt) Fig. 15(a) (excerpt)

Ex. 1112, Figs. 2(b), 14(a), 15(a) (excerpted and annotated)

A PHOSITA at the time would have understood how to apply these damping techniques taught to the equivalent common mode versions of these filters, which are illustrated below. Ex. 1102, ¶ 294.

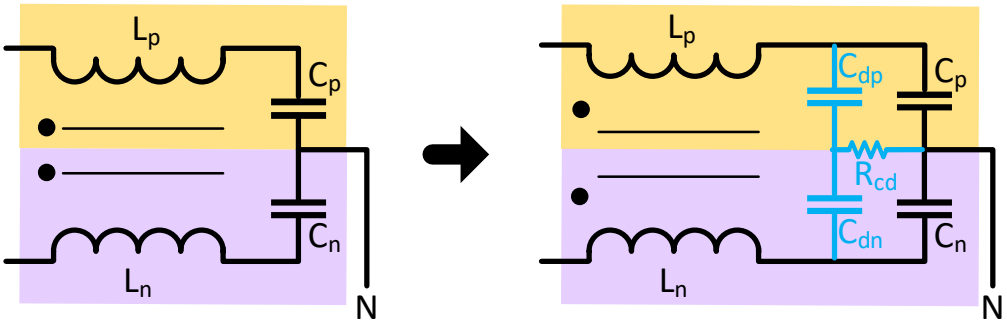


Illustration combining filter of Ex. 1113, Fig 5 and Ex. 1112, Fig 14(a)

In the left figure, the common mode LC filter disclosed in Koyama includes a top half (**orange**) and a bottom half (**purple**). Each half is analogous to the filter illustrated in the Ahmed figure 2(b) above having a single series inductor and a capacitor connected between the power line (positive or negative) and neutral. A PHOSITA would have understood that each half of the common mode filter would be modified according to the teachings of Ahmed to add a capacitor (C_{dp} and C_{dn}) analogous to C_d in Figure 14(a) connected through a resistor R_{cd} to neutral, where R_{cd} is the parallel equivalent of two resistors R_d in Ahmed Figure 14(a), one for each half of the common mode filter (shown above). Similarly, Ahmed teaches to add an inductor analogous to L_d in Figure 15a in parallel with R_{cd}, as shown below. Ex. 1102, ¶ 295.

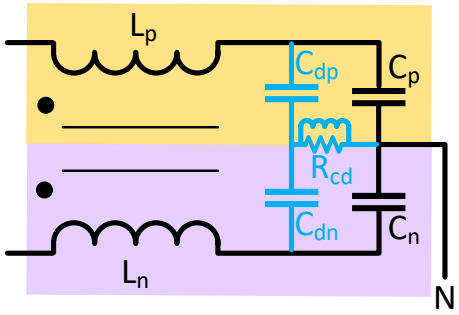


Illustration combining filter of Ex. 1113, Fig 5 and Ex. 1112, Fig 15(a)

Koyama as modified by Ahmed above, thus discloses the claim 14 "damping resistor connected to the neutral output terminal; and a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal," and the claim 15 "inductor connected in parallel with said damping resistor." Ex. 1102, ¶ 296.

Using Ahmed's damping circuits as described above to modify Koyama's common mode filter would reduce resonance in the filter. The addition of the inductor in parallel with damping resistor provides the additional benefit of reducing power dissipation of the damping circuit. Ex. 1112, 7, 9; Ex. 1102, ¶ 297. As such, these combinations which disclose all of the features of claims 14 and 15, represent the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Koyama's common mode LC filter) in the same way (by suppressing the resonance between the choke and capacitors and reducing power dissipation of the damping resistor). A PHOSITA was familiar with

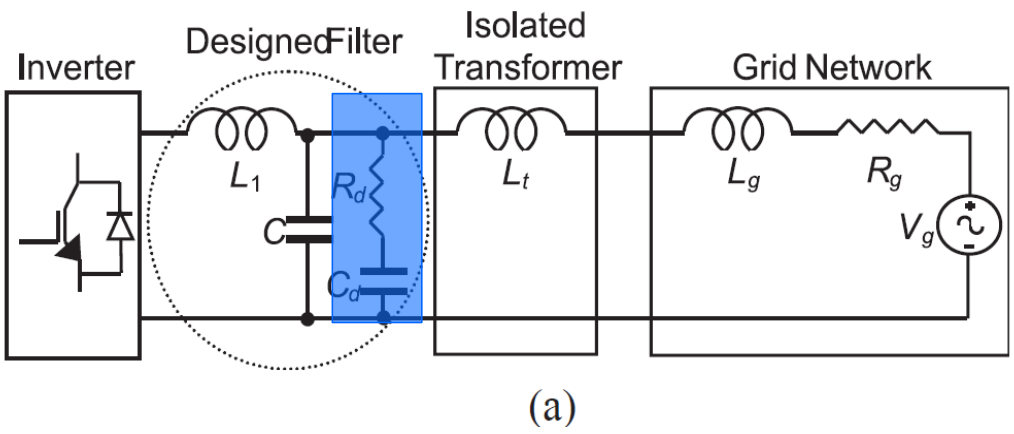
designing passive LC filter circuits, and would have had the skills to do so, resulting in an expectation of success. Ex. 1102, ¶¶ 282-298.

J. Ground K: Claim 16 is Rendered Obvious by Suzuki in View of Ahmed

Claim 1 is taught by Suzuki. Section VII.A.1, s*upra*. Claim 16 depends from claim 1 and requires "a low-pass output filter comprising: an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal; a first capacitor connected across the hot and neutral output terminals; a damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." Ex. 1101, claim 16.

Suzuki discloses that a smoothing filter can be connected to the "hot" output of its single-phase inverter. Ex. 1126, [0017]-[0019]. A PHOSITA would understand Suzuki's smoothing filter to be a LC low pass filter (and Suzuki illustrates its smoothing filter as including an inductor and capacitor in Figure 2(a)). Ex. 1126, [0017], Fig. 2(a). Ex. 1102, ¶ 303.

Ahmed teaches to modify Suzuki's low pass filter to include the remaining claim 16 elements. Ahmed discloses that LC filters can resonate, causing instability in the system, and adds a damping circuit (**blue**) with a resistor connected in series with a capacitor across the grid terminals (shown below) to attenuate those effects. Ex. 1112, 6-9, Figs. 1, 14; Ex. 1102, ¶ 304.



Ex. 1112, Fig. 14(a) (annotated)

A PHOSITA would have recognized that connecting the capacitor and series resistor in reverse order makes no functional difference (which is also how they are oriented in Figure 8 of the '710 patent). Thus, Ahmed teaches the claim 16 "damping resistor connected to the neutral output terminal; and a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal." Ex. 1102, ¶ 305.

Modifying Suzuki's low pass filter by adding Ahmed's damping RC circuit would reduce unwanted resonance effects. Ex. 1112, 6-9; Ex. 1102, ¶ 306. Therefore, the combination of Suzuki with Ahmed, which disclose all of the limitations of claim 16, represents the obvious use of a known technique (inserting Ahmed's damping circuits in an LC filter) to improve a similar device (Suzuki's output LC filter) in the same way (by suppressing the resonance between the inductor and capacitor). A PHOSITA was familiar with filtering the output from inverters,

and would have had the skills to do so, resulting in an expectation of success. Ex. 1102, ¶¶ 299-307.

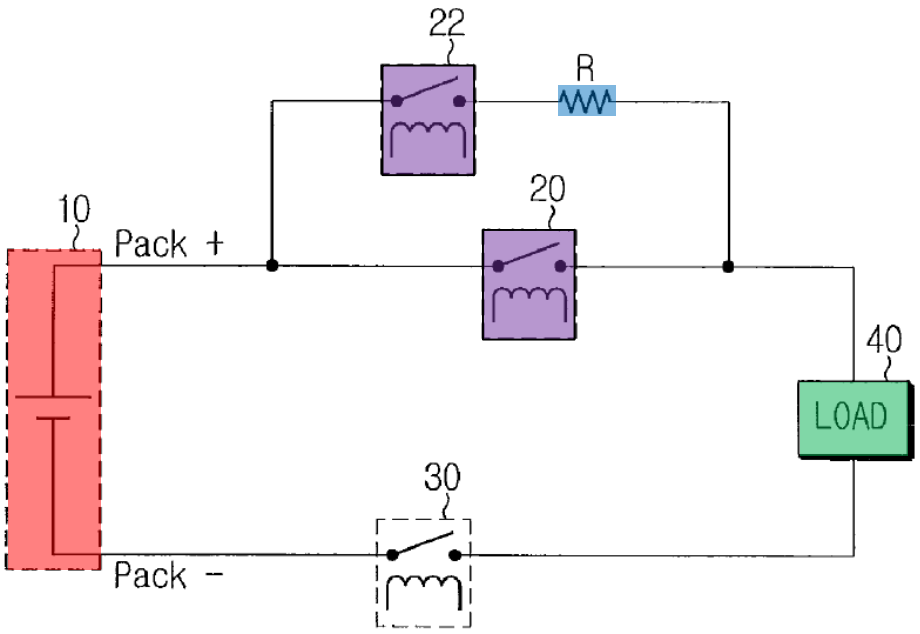
K. Ground L: Claim 17 is Rendered Obvious by Suzuki in View of Kang

Claim 1 is taught by Suzuki. Section VII.A.1, s*upra*. Claim 17 depends from claim 1 and requires:

> "a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
>
> one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source to the controlled switch when the in-rush current has dropped below a threshold."

Ex. 1101, claim 17.

Suzuki does not disclose claim 17's "start-up in-rush current limiting circuit" between its DC power sources and controlled switches, but Kang does. As shown below, Kang discloses a DC power source 10 (**red**) providing power to a load 40 (**green**) and between the power source and load are interposed switches 20 and 22 (**purple**) (the recited "one or more switches"), and resistor R (**blue**) (the recited "series impedance"). Ex. 1130, [0009]-[0011], Fig. 1; Ex. 1102, ¶ 314.



Ex. 1130, Fig. 1 (annotated)

To prevent damage from in-rush current when a load is being connected, Kang discloses that switch 22 is turned on (closed) while switch 20 is kept off (open) so that resistor R ("a series impedance") is inserted to provide a high resistance path, limiting current flow to the load. Ex. 1130, [0011]-[0012], Fig. 1; Ex. 1102, ¶ 315. Once a predetermined time has passed which allows a certain threshold of current or voltage to be reached, switch 20 is turned on and switch 22 is turned off, thus removing any impedance between the power source and load. Ex. 1130, [0011]-[0012]; Ex. 1102, ¶ 315. Thus, Kang discloses a "start-up in-rush current limiting circuit" that, when inserted into Suzuki, meets claim 17. Ex. 1102, ¶ 315. As used in Suzuki, the switches would be arranged so that the series impedance R is inserted between the DC power source and the controlled switch of Suzuki when the DC to

AC converter is initially powered on and no electrical load is connected to an AC output. This protects the circuitry against current in-rush. Then, as taught in Kang, when the current falls below a threshold, the switches are arranged to remove the series impedance, thus connecting the DC power source to the controlled switch. Ex. 1102, ¶ 315.

A PHOSITA would have understood that initially applying power to an inverter causes in-rush current that can be damaging to the inverter or a connected load, and that it is necessary for the inverter to reach a stable voltage and current before applying a load. Ex. 1102, ¶ 316. It was obvious to use Kang's startup circuit between one of Suzuki's power sources and the controlled H-bridge switches to prevent such damage. This would have been combining known elements (Kang's in-rush limiting startup circuit and Suzuki's power sources providing power to its H-bridges) according to known methods (inserting the startup circuit between the power source and load as taught in Kang) to yield predictable results (protecting Suzuki's H-bridge circuitry by limiting the amount of current entering the switches during startup). Ex. 1102, ¶ 316. A PHOSITA was familiar with startup circuits, and would have had the skills to insert one between a power source and a switch, resulting in an expectation of success. Ex. 1102, ¶¶ 316, 106.

Thus, Suzuki in view of Kang renders claim 17 obvious. Ex. 1102, ¶¶ 308-317.

VIII. CONCLUSION

Inter partes review should be instituted and claims 1-17 should be canceled. Ex. 1102, ¶¶ 318-320.

Dated: October 8, 2021

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CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for Inter Partes Review totals 13,958, which is less than the 14,000 allowed under 37 CFR § 42.24(a)(1)(i). This total includes 13,846 words as counted by the Word Count feature of Microsoft Word and 112 words used in annotations.

Pursuant to 37 C.F.R. § 42.24(a)(1), this count does not include the table of contents, the table of authorities, mandatory notices under § 42.8, the certificate of service, this certification of word count, the claims listing appendix, or appendix of exhibits.

BANNER & WITCOFF, LTD

Dated: October 8, 2021

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of the Petition for *Inter Partes* Review in connection with U.S. Patent No. 10,784,710 and supporting evidence to be served via FedEx Priority Overnight on October 8, 2021, on the following:

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CLAIM LISTING APPENDIX

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Designation	Claim Language
Claim 1	
[1A]	1. A DC to AC converter having
[1B]	a transformerless output, and operative to convert DC power to an AC power having a desired voltage and waveform,
[1C]	and to output the AC power between hot and neutral output terminals,
[1D]	the DC to AC converter comprising: a plurality of controlled switches, each having a power input connection operative to accept DC power from an associated DC power source at an associated DC voltage, and
[1E]	each controlled switch further having a power output connection operative to output a selected one of: (a) the associated DC voltage, (b) the associated DC voltage having an inverted polarity, and (c) zero voltage, in response to an associated ternary-valued selection signal representing the multiplier values +1, −1, or 0 respectively,
[1F]	the power output connections of the plurality of switches being directly connected in series to output a sum voltage approximating the desired AC output voltage and waveform.
Claim 2	
2	2. The DC to AC converter of claim 1 wherein at least some of the DC voltages associated with the plurality of controlled switches have different values.
Claim 3	
3	3. The DC to AC converter of claim 1 wherein the desired voltage is a voltage of a standard household electricity supply and the desired waveform is sinusoidal at a standard household electricity supply frequency.
Claim 4	
4	4. The DC to AC converter of claim 1 wherein the controlled switches are MOSFETs connected in H-bridge configurations, and the associated DC power sources are floating relative to each other and relative to the DC to AC converter hot and neutral output terminals.
Claim 5	

Designation	Claim Language
5	5. The DC to AC converter of claim 1 wherein each associated DC voltage differs from another DC voltage nominally by a factor of 3.
Claim 6	
6	6. The DC to AC converter of claim 1 wherein the ternary-valued selection signals comprise pairs of binary bits, each bit pair having in total four combinations of possible values, of which two of the four combinations represent the zero multiplier value.
Claim 7	
[7A]	7. The DC to AC converter of claim 1 further comprising:
[7B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sets of switch selection signals, at given time instants, such that the sum voltage output is momentarily the best approximation to the instantaneous voltage values of the desired waveform at the given instants.
Claim 8	
[8A]	8. The DC to AC converter of claim 1 further comprising:
[8B]	a switch selection signal generator operative to produce the ternary-valued selection signals, the switch selection signal generator being configured to produce sequential sets of switch selection signals, and being configured to produce each new set of switch selection signals at a time instant at which the new set of switch selection signals would cause the sum voltage to be a better approximation to an instantaneous voltage value of the desired waveform at that time instant than the immediately previously output set of switch selection signals.
Claim 9	
[9A]	9. The DC to AC converter of claim 8 further comprising, where the desired waveform is repetitive:
[9B]	memory operative to store precomputed sequential sets of switch selection signals and the associated time instants at which each set is to be output; and
[9C]	wherein the switch selection signal generator is operative to retrieve the precomputed sequential sets of switch selection signals and associated time instants from the memory, and to output the switch selection signals at the associated times.

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Claim 10	
10	10. The DC to AC converter of claim 1 wherein the DC power source having the highest voltage value is a battery and the DC power sources having lower voltages values comprise bi-directional DC-DC conversion circuitry operative to derive the lower voltage values from the battery.
Claim 11	
11	11. The DC to AC converter of claim 1 wherein the DC power source supplying the highest mean power is a battery and the DC power sources supplying lower mean power comprise bi-directional DC-DC conversion circuitry operative to derive the lower mean power from the battery.
Claim 12	
12	12. The DC to AC converter of claim 1 wherein one of the power output connections of the controlled switch having the associated DC power source of the highest associated DC voltage is one of the end terminals of the series connection, and is connected to the neutral output terminal.
Claim 13	
13	13. The DC to AC converter of claim 1 wherein the associated DC power source of one of the controlled switches is a battery, and further comprising a common-mode filter interposed between the battery and the controlled switch.
Claim 14	
[14A]	14. The DC to AC converter of claim 12 wherein the common mode filter comprises:
[14B]	a capacitor connected between DC power input terminals of the controlled switch;
[14C]	a common-mode choke connected between the battery and the DC power input terminals of the controlled switch;
[14D]	a first pair capacitors connected respectively from positive and negative terminals of the battery to the neutral output terminal;
[14E]	a damping resistor connected to the neutral output terminal; and
[14F]	a second pair of capacitors connected respectively from the positive and negative terminals of the battery to the other end of the damping resistor than the neutral terminal.
Claim 15	

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15	15. The DC to AC converter of claim 14 further comprising an inductor connected in parallel with said damping resistor.
Claim 16	
[16A]	16. The DC to AC converter of claim 1 further comprising a low-pass output filter comprising:
[16B]	an inductor connected between the sum voltage at the end of the series connection of switches and the hot output terminal;
[16C]	a first capacitor connected across the hot and neutral output terminals;
[16D]	a damping resistor connected to the neutral output terminal; and
[16E]	a second capacitor connected from the hot output terminal to the other end of the damping resistor than the neutral terminal.
Claim 17	
[17A]	17. The DC to AC converter of claim 1 further comprising a start-up in-rush current limiting circuit interposed between at least one of the controlled switches and its associated DC power source, the start-up in-rush current limiting circuit comprising:
[17B]	one or more switches operative to insert a series impedance between the DC power source and the controlled switch when the DC to AC converter is initially powered on and no electrical load is connected to an AC output, and further operative to remove the series impedance and connect the DC power source to the controlled switch when the in-rush current has dropped below a threshold.