UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

UNIFIED PATENTS, LLC

Petitioner

v.

ARIGNA TECHNOLOGY LIMITED

Patent Owner

IPR2022-00285

U.S. Patent 7,049,850

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT 7,049,850
CHALLENGING CLAIM 7

PETITIONER'S EXHIBIT LIST[1]

EX1001	U.S. Patent 7,049,850 by Kazuhiro Shimizu ("'850 patent")
EX1002	Prosecution History of U.S. Patent No. 7,049,850 ("'850 FH")
EX1003	Declaration of Dr. R. Jacob Baker ("Baker")
EX1004	*Curriculum Vitae* of Dr. R. Jacob Baker
EX1005	U.S. Patent 6,452,365 by Gourab Majumdar et al. ("*Majumdar*")
EX1006	U.S. Patent 6,545,510 by Timothy B. Cowles ("*Cowles*")
EX1007	U.S. Patent Application Publication 2003/0012040 by Shoichi Orita et al. ("Orita")
EX1008	Victor P. Nelson et al., "Digital Logic Circuit Analysis & Design," Prentice Hall, 1995
EX1009	Declaration of Kevin Jakel
EX1010	U.S. Patent 6,774,674 by Kazuaki Okamoto et al. ("Okamoto")
EX1011	Order, *Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.*, No. 2:21-cv-00172-JRG, ECF No. 37 (E.D. Tex. Aug. 24, 2021) (Gilstrap)
EX1012	Docket Control Order, *Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.*, 2:21-cv-00172-JRG, ECF No. 126 (E.D. Tex. Nov. 15, 201) (Gilstrap)
EX1013	Ejup N. Ganic, "The McGraw-Hill Handbook of Essential Engineering Information and Data," R. R. Donnelly & Sons Co., 1991
EX1014	U.S. Patent 5,608,237 by Yoshiaki Aizawa et al. ("Aizawa")
EX1015	U.S. Patent 5,838,027 by Ho-Hym Kim et al. ("Kim")
EX1016	Docket Navigator Printout of litigations filed by Patent Owner in 2021
EX1017	Complaint for Patent Infringement, *Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.*, No. 2:21-cv-00172-JRG, ECF No. 1 (E.D. Tex. May 20, 2021) (Gilstrap)

[1] Citations to non-patent document exhibits are to the original page numbering in the exhibits, unless the numbering added in accordance with 37 CFR § 42.63(d)(2)(i) is specifically referenced.

EX1018	Complaint for Patent Infringement, *Arigna Tech. Ltd., v. General Motors Co. et al.*, No. 2:21-cv-00174-JRG, ECF. No. 1 (E.D. Tex. May 20, 2021) (Gilstrap)
EX1019	Complaint for Patent Infringement, *Arigna Tech. Ltd. v. Daimler AG et al.*, No. 2:21-cv-00175-JRG, ECF No. 1 (E.D. Tex. May 20, 2021) (Gilstrap)
EX1020	Andrew T. Dufresne et al., "How reliable are trial dates relied on by the PTAB in the Fintiv analysis," 1600 PTAB & Beyond, October 29, 2021, available at https://www.1600ptab.com/2021/10/how-reliable-are-trial-dates-relied-on-by-the-ptab-in-the-fintiv-analysis/# (last accessed December 8, 2021)
EX1021	Docket Sheet, *Fintiv, Inc. v. Apple Inc.*, No. 1:21-cv-00896-ADA (W.D. Tex.) (Albright) (printed December 8, 2021)
EX1022	Joint Claim Construction and Prehearing Statement, *Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.*, No. 2:21-cv-00172-JRG, ECF No. 136 (E.D. Tex. Dec. 3, 2021) (Gilstrap)
EX1023	Exhibit A to Joint Claim Construction and Prehearing Statement, *Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.*, No. 2:21-cv-00172-JRG, ECF No. 136-1 (E.D. Tex. Dec. 3, 2021) (Gilstrap)

I. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

Under 37 C.F.R. § 42.8(b)(1), Unified Patents, LLC ("Unified" or "Petitioner") certifies that Unified is the real party-in-interest, and further certifies that no other party exercised control or could exercise control over Unified's participation in this proceeding, the filing of this petition, or the conduct of any ensuing trial. In view of *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1242-44 (Fed. Cir. 2018), Unified has submitted voluntary discovery in support of its certification. *See* EX1009 (Declaration of Kevin Jakel).

B. Related Matters

According to assignment records, U.S. Patent No. 7,049,850 ("the '850 patent" (EX1001)) is currently assigned to Arigna Technology Limited ("Patent Owner").

As of the filing date of this Petition, and to the best knowledge of Petitioner, the '850 patent is or has been involved in:

Case Caption	Filed	Number	Court
Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al.	May 20, 2021 (Pending)	2:21-cv-00172	E.D. Tex.
Arigna Tech. Ltd. v. General Motors Co. et al.	May 20, 2021 (Pending)	2:21-cv-00174	E.D. Tex.
Arigna Tech. Ltd. v. Daimler AG et al.	May 20, 2021 (Pending)	2:21-cv-00175	E.D. Tex.

As of the filing date of this Petition, and to the best knowledge of Petitioner, the '850 patent has been involved in the following IPR proceeding before the Office.

Petitioner	**IPR No.**	**Petition filed**
Volkswagen Group of America, Inc.	IPR2022-00147	November 9, 2021

C. Lead and Back-up Counsel and Service Information

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Please address all correspondence to lead and back-up counsel. Petitioner consents to electronic service and asks Patent Owner to do the same.

II. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '850 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an IPR challenging the patent claims on the grounds identified in this Petition.

III. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Under Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner challenges claim 7 ("challenged claim") of the '850 patent.

The '850 patent was filed on February 19, 2004, and issued on May 23, 2006.[2] The '850 patent claims priority to Japanese Patent Application No. 2003-119641, filed on April 24, 2003 (hereinafter "priority date of the '850 patent").[3] All prior art

[2] The '850 patent issued from an application filed prior to the enactment of the America Invents Act ("AIA"). Thus, the pre-AIA statutory framework applies.

[3] Petitioner takes no position as to the validity of the priority claim and reserves the right to challenge the validity of that claim in the event Patent Owner attempts to

cited in this Petition predates the priority date of the '850 patent.

A. Prior Art Patents and Publications

The following references are pertinent to the ground of unpatentability explained below:

1. U.S. Patent 6,452,365 by Majumdar et al. ("*Majumdar*," EX1005). *Majumdar* was filed August 13, 2001, and issued on September 17, 2002. *Majumdar* is therefore prior art under 35 U.S.C. §§ 102(a), (b) and (e).
2. U.S. Patent 6,545,510 by Cowles ("*Cowles*," EX1006). *Cowles* was filed on December 10, 2001, and issued on April 8, 2003. *Cowles* is therefore prior art under 35 U.S.C. § 102(a) and (e).

Majumdar and *Cowles* were not considered or cited during prosecution of the '850 patent.

B. Statutory Grounds for Challenges

This Petition, supported by the declaration of Dr. R. Jacob Baker ("Baker" (EX1003)), requests cancellation of claim 7 under the Ground listed below:

Ground #1: Claim 7 of the '850 patent is obvious under 35 U.S.C. § 103(a) over *Majumdar* in view of *Cowles*.

assert the priority claim.

IV. U.S. PATENT 7,049,850[4]

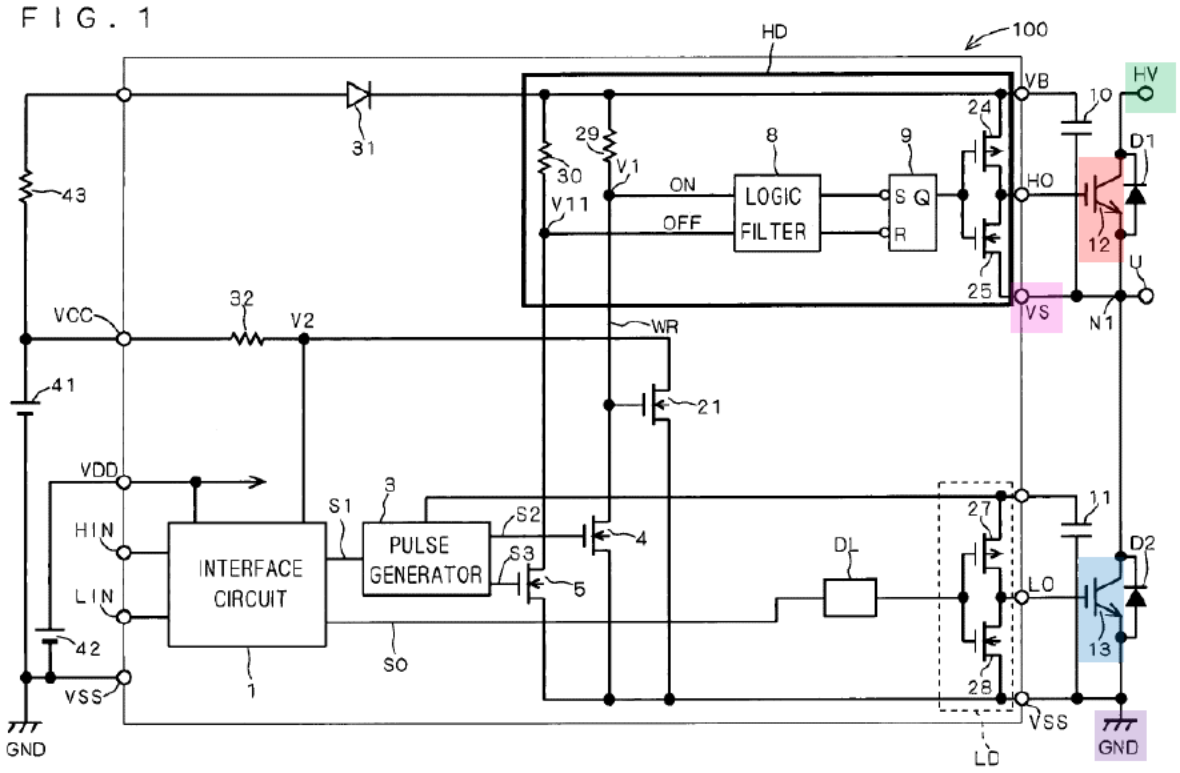
A. Summary of the '850 Patent

The '850 patent relates to a high voltage integrated circuit (HVIC) for driving power devices such as integrated gate bipolar transistors (IGBTs). EX1001, 1:10-24, 5:26-34. Figure 1 of the '850 patent below illustrates an HVIC 100 in which a **first power device 12** (e.g., IGBT) and a **second power device 13** (e.g., IGBT) are connected in series between a **high side (HV) power line** and a **low side (ground potential (GND)) power line**, to form a half-bridge power device. EX1001, 5:26-32. A load U (e.g., a motor) is connected to a node N1 between the series-connected power devices 12, 13. EX1001, 5:32-34.

The '850 patent explains that "the power device 12 switches between a potential at the node N1 used as a reference potential and the **potential (HV)** at a high side power line, and is called a high side power device." EX1001, 5:35-38. Further, "[t]he power device 13 switches between the ground potential used as a reference potential and the potential at the node N1, and is called a low side power device." EX1001, 5:39-41. Thus, as shown in Figure 1, the HVIC 100 includes a

[4] Unless otherwise specified, all **bold** and ***bold italics*** emphasis below has been added. Text in *italics* is used to signify claim language, while reference names are also *italicized*.

first switching device 12 and a **second switching device 13** connected in series and interposed between a **high main power potential (HV)** and a **low main power potential (GND)**.



'850 patent (EX1001), Fig. 1 (annotated)

In Figure 1, the **first switching device 12** is a high side switching device, and the **second switching device 13** is a low side switching device. The '850 patent is related to addressing the "shoot-through" phenomenon in which the **high side switching device** and the **low side switching device** are turned on at the same time, resulting in a short circuit. EX1001, 1:20-24. To prevent this, the **potential VS** (at

node N1) between the **high side switching device** and the **low side switching device** may be monitored. EX1001, 1:39-40. However, the '850 patent explains that "the **potential VS** usually reaches several hundred volts. Thus, it is impossible to monitor the **potential VS** within the HVIC." EX1001, 1:40-42. Because the '850 patent alleges it is "impossible to monitor the **potential VS** within the HVIC," the '850 patent proposes to monitor another voltage that is considered to be "substantially equal to the **potential VS**," as described in Section IV.B below. EX1001, 1:40-42, 19:44-49.

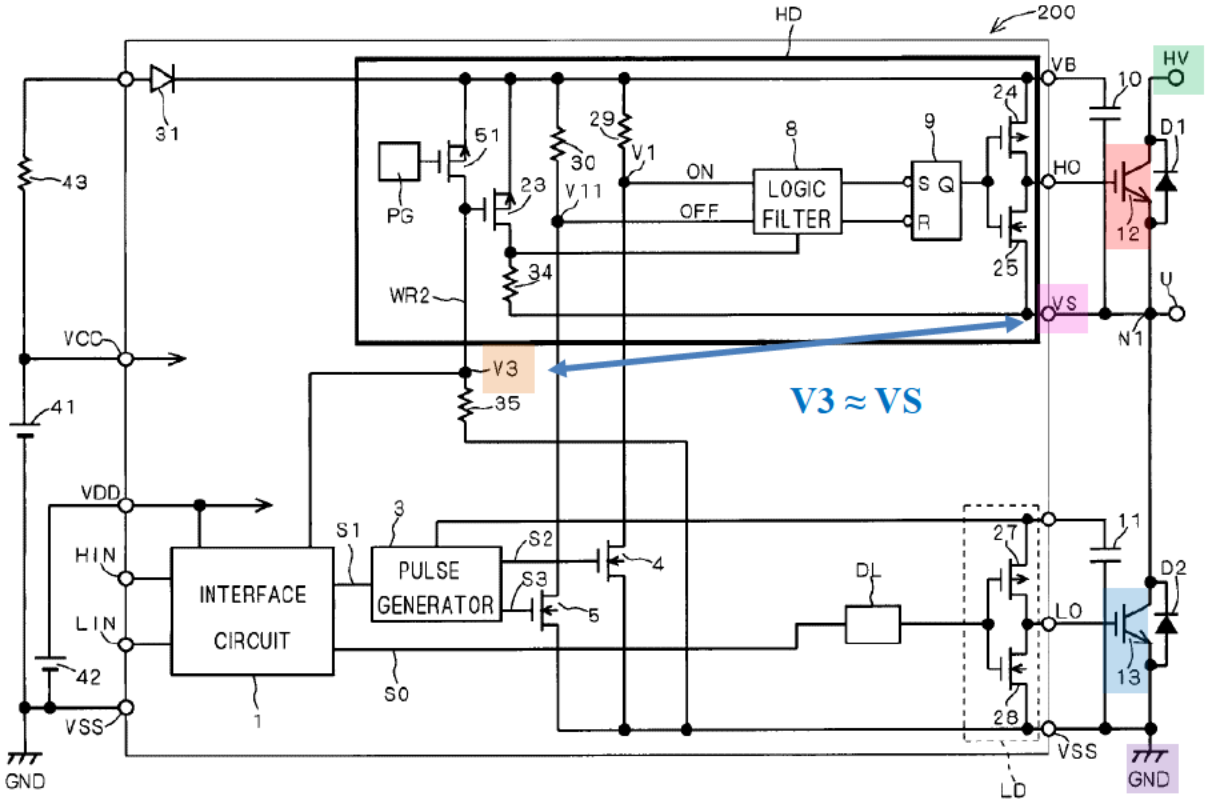
B. Claim 7 and the Second Embodiment

Claim 7 corresponds to the second embodiment illustrated in Figure 25 of the '850 patent, which illustrates a configuration of an HVIC 200 (the claimed "*semiconductor device*"). EX1001, 19:1-67; EX1003, ¶ 48. The '850 patent explains that "[c]omponents shown in FIG. 25 similar to those in the HVIC 100 in FIG. 1 are indicated by the same reference numerals." EX1001, 19:7-9; EX1003, ¶ 48.

In view of the above-described object of avoiding the "shoot-through" phenomenon and the alleged "impossib[ility]" of monitoring the **potential VS** between the **high side switching device 12** and the **low side switching device 13**, the second embodiment proposes an alternative solution to monitoring the **potential VS**. With reference to Figure 25 below, the '850 patent explains that "the inventor

paid attention to the fact that the **potential V3** at the HPMOS transistor 51 can be considered substantially equal to the **potential VS**, and he has reached a technical idea of detecting the **potential VS** by monitoring the **potential V3**." EX1001, 19:44-49. Thus, in the second embodiment, the '850 patent proposes to monitor the **potential V3**, rather than the **potential VS**, because the **potential V3** is considered to be "substantially equal to the **potential VS**." *Id.*

FIG. 25



'850 patent (EX1001), Fig. 25 (annotated)

With reference to Figure 25 above, claim 7 recites a semiconductor device

(HVIC 200) performing drive control of first and second switching devices (12, 13) connected in series and interposed between a high main power potential (HV) and a low main power potential (GND, VSS is at GND).[5] The semiconductor device of claim 7 comprises a high potential part (HD) including a control part (logic filter 8) configured to control conduction/non-conduction of a high side switching device (12) which is one of the first and second switching devices (12, 13). EX1001, 19:10-18.

The semiconductor device of claim 7 also comprises a reverse level shift part (transistor 51) configured to level-shift a signal from the high potential part (HD) to supply the level-shifted signal to a low side logic circuit (interface circuit 1) operating on the basis of the low main power potential (VSS, which is at GND). EX1001, 19:19-41.

In addition, the semiconductor device of claim 7 comprises a voltage detecting device (transistor 23) provided in the high potential part (HD) and configured to detect a potential (V3) at an output line of the reverse level shift part (transistor 51) and to supply a logic value based on the potential for the control part (logic filter 8), thereby causing the control part (logic filter 8) to control conduction/non-conduction

[5] VSS is an abbreviation for Voltage Source Source (the voltage at the source terminal of a transistor).

of the high side switching device (12). EX1001, 19:19-27, 19:42-64.

C. Prosecution History

The '850 patent issued from U.S. Application 10/780,735 ("the '735 application") (EX1002). During prosecution, the examiner issued only one Office Action. EX1002, 27-34. The examiner rejected prosecution claims 7 and 20 (corresponding to issued claims 7 and 20) as being anticipated by U.S. Patent 6,774,674 by Okamoto et al. ("Okamoto," EX1010).[6] EX1002, 30. In response, the applicant conducted an interview with the examiner (EX1002, 26), and argued, without presenting any claim amendments, that Okamoto (EX1010) did not disclose the feature of "a voltage detecting device provided in said high potential part," as recited in claims 7 and 20. EX1002, 23-24. Instead, the applicant argued that Okamoto discloses a level shifting circuit that employs a timing control device to limit a time that high and low parts are in "on" states, and alleged that "Okamoto's timing control device or level shifting circuit is different than a voltage detecting device." EX1002, 24.

The examiner then allowed the '735 application. EX1002, 4-12. In the Notice

[6] In the Office Action, the examiner allowed claims 1-6 and 13-19, and indicated that dependent claims 8-12 and 21-26 (depending from claims 7 and 20) would be allowable if rewritten in independent form. EX1002, 30-31.

of Allowance, the examiner indicated that claim 7 was allowed because the prior art considered during prosecution did not disclose:

> a voltage detecting device provided in said high potential part and configured to detect a potential at an output line of said reverse level shift part and to supply a logic value based on said potential for said control part, thereby causing said control part to control conduction/non-conduction of said high side switching device.

EX1002, 8-9.

The "voltage detecting device" in claim 7 of the '850 patent is identified below as limitations [7.3.1] and [7.3.2].

As described in Section VI.A.4 below, limitations [7.3.1] and [7.3.2] are rendered obvious by prior art (*Majumdar* and *Cowles*) not considered by the examiner. EX1003, ¶ 55.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") at and before the earliest effective filing date of the challenged claims would have had a bachelor's degree in electrical engineering, physics, or a related subject, and one to two years of work experience in semiconductor devices. Less experience can be remedied with additional education (e.g., a Master's degree), and likewise, less education can be remedied with additional work experience (e.g., 5-6 years). EX1003, ¶¶ 56-60.

V. CLAIM CONSTRUCTION

The terms of the challenged claims are to be construed "in accordance with the ordinary and customary meaning of such claim[s] as understood by a [POSITA] and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-1313 (Fed. Cir. 2005). A POSITA would apply the ordinary and customer meaning to all terms in the challenged claim, such that no specific claim construction is necessary.

In parallel district court litigation involving the '850 patent, the parties have agreed to the following constructions of terms in claim 7.

Term of Claim 7	**Agreed Construction in District Court**
"first and second switching devices connected in series and interposed between a high main power potential and a low main power potential" (portion of claim 7 preamble)	This portion is limiting.
"low side"	"outside of high potential part"
"to supply a logic value…for said control part"	"to supply a logic value…to said control part"

EX1022, 2.

Petitioner has applied each of the above constructions in showing that the prior art teaches all the limitations of claim 7. For example, in Section VI.A.4[7.0] below,

Petitioner has shown how *Majumdar* discloses the preamble of claim 7. In Section VI.A.4[7.2] below, Petitioner has shown how *Majumdar* discloses a "low side logic circuit" outside of the high potential part. In Section VI.A.4[7.3.1], Petitioner has shown how *Majumdar* discloses a voltage detecting device configured to supply a logic value to the control part.

In the parallel district court litigation involving the '850 patent, Patent Owner argued that the district court should construe each of the following terms according to their plain and ordinary meaning.

- "performing drive control of" in the preamble of claim 7 (EX1023, 1);
- "high main power potential" (EX1023, 2);
- "high potential part" (EX1023, 4);
- "a reverse level shift part" (EX1023, 6); and
- "output line" (EX1023, 7).

Petitioner has construed each of the above five terms according to their plain and ordinary meaning. In Section IV.A.4 below, Petitioner has shown how the prior art teaches and renders obvious all limitations of claim 7.

VI. CLAIM 7 IS UNPATENTABLE

A. Ground 1: Claim 7 would have been obvious over *Majumdar* in view of *Cowles*

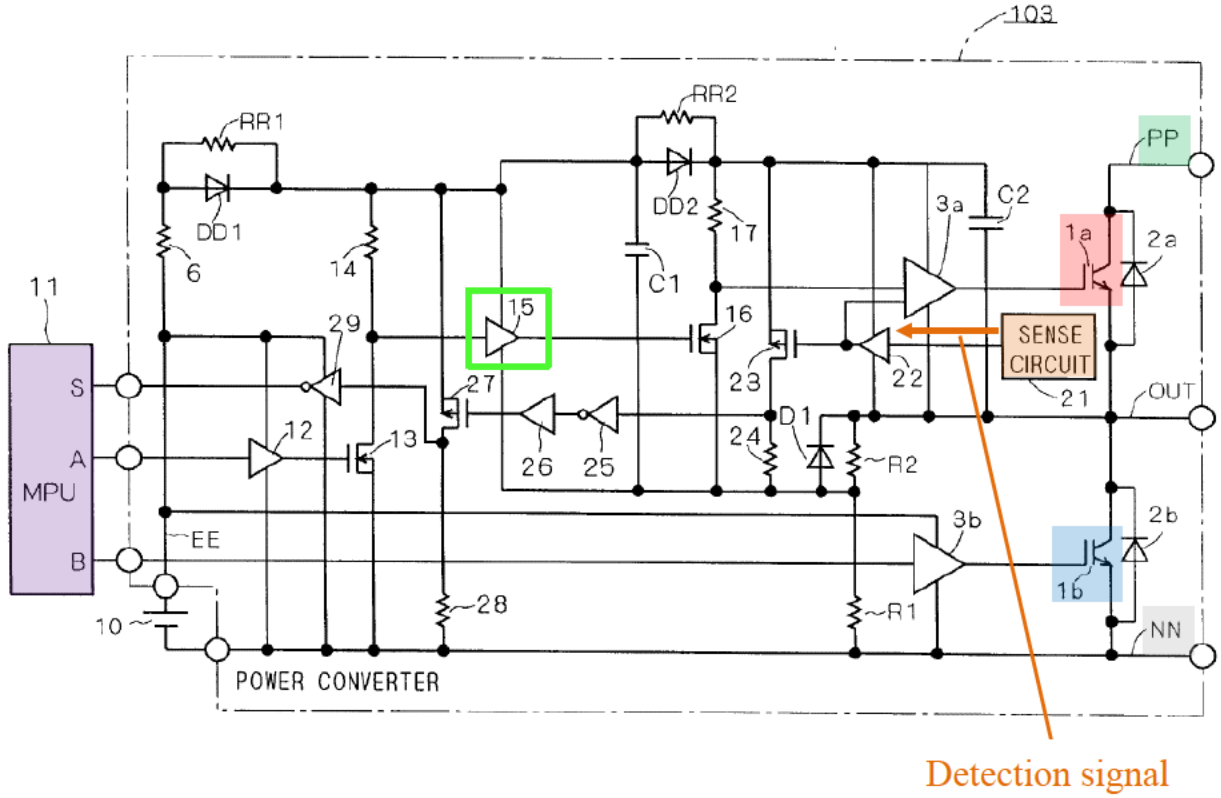
1. Overview of *Majumdar*

Like the '850 patent, *Majumdar* relates to a power converter that includes an HVIC for driving high-side and low-side power switching elements connected in series. EX1005, 1:8-13, 1:24-42. As shown in Figure 6 below, *Majumdar* discloses a power converter 103 that includes a **first power switching element 1a** (e.g., IGBT) connected in series with a **second power switching element 1b** (e.g., IGBT) between a **high potential power line PP** and a **low potential power line NN** (e.g., ground). EX1005, 8:46-52.[7] Like the '850 patent, *Majumdar* discloses that a load

[7] This citation relates to the description of *Majumdar*'s first embodiment illustrated in Figure 2. This description is also applicable to *Majumdar*'s third embodiment illustrated in Figure 6. Relative to the first embodiment in Figure 2, *Majumdar* explains that the third embodiment in Figure 6 additionally includes a sense circuit 21, and another level shift circuit (switching element 27) for level shifting a detection signal from the sense circuit 21. EX1005, 10:54-62. The arrangement of the switching elements 1a, 1b in series between the high and low potential power lines NN, PP in Figure 6 is the same as the arrangement in Figure 2. Dr. Baker's

is connected to a connecting portion of the **first power switching element 1a** and the **second power switching element 1b** at wiring OUT. EX1005, 8:55-59; EX1003, ¶ 90.

FIG. 6



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 90

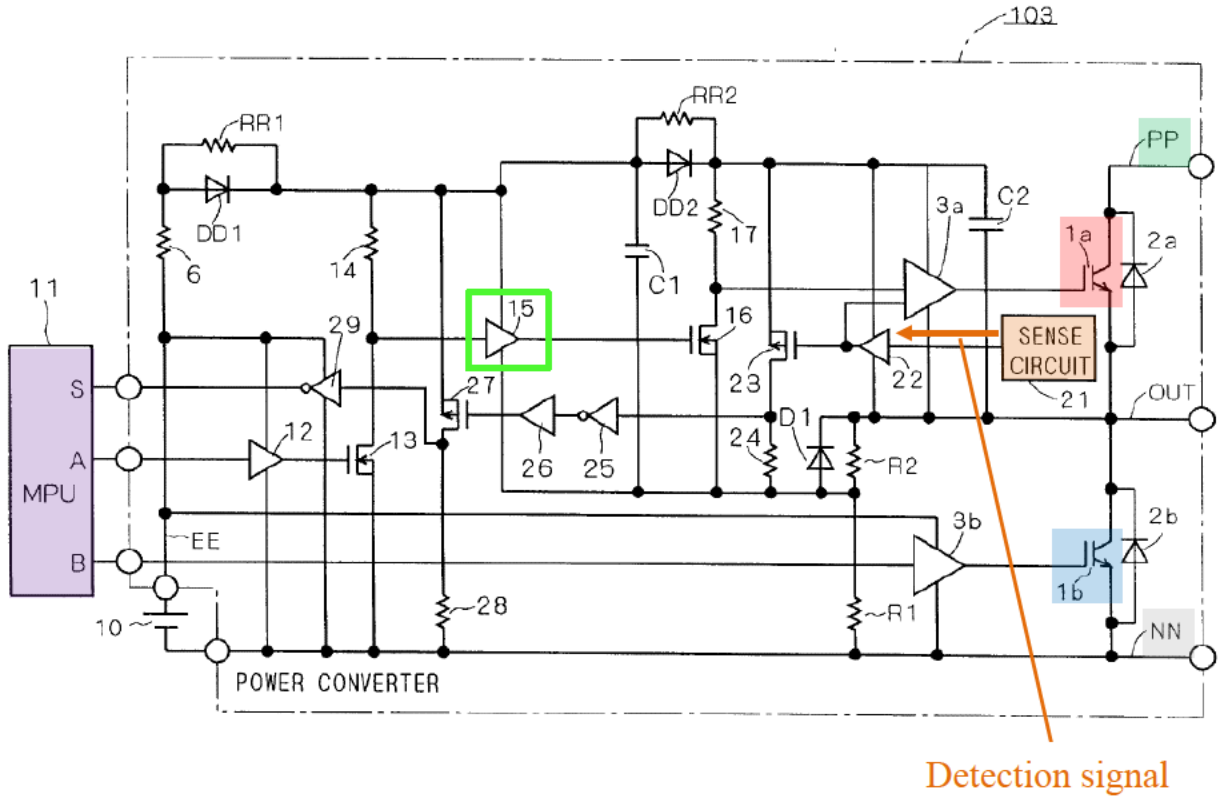
Like the '850 patent, *Majumdar* is concerned with the operation of the **first power switching element 1a** during operation with the **second power switching**

declaration explains in more detail the embodiments of Figures 2 and 6 and their corresponding features. EX1003, ¶¶ 74-89.

element 1b. *Majumdar* includes a **sense circuit 21** that detects, based on the potential at the wiring OUT, a magnitude of current flowing to the **first power switching element 1a** and a temperature of the **first power switching element 1a**. EX1005, 10:62-11:5. The **sense circuit 21** outputs a detection signal to a **microcomputer 11**, which in turn outputs (1) a control signal A for driving the **first power switching element 1a** via a high-side driving circuit 3a and (2) a control signal B for driving the **second power switching element 1b** via a low-side driving circuit 3b. EX1005, 11:3-5 (sense circuit 21 outputs detection signal), 9:20-25 (driving circuits 3a, 3b respectively drive switching elements 1a, 1b), 9:55-57 (microcomputer 11 outputs control signals A, B for respectively driving switching elements 1a, 1b). EX1003, ¶ 91.

Thus, like the '850 patent, *Majumdar* adjusts the operation of the power converter based on the voltage between the **first power switching element 1a** and the **second power switching element 1b**. As discussed in Section VI.A.4 below, the **buffer 15** in *Majumdar*'s Figure 6 above performs the same features of the voltage detecting device in claim 7 of the '850 patent—the feature that led to allowance of claim 7. EX1003, ¶ 98.

FIG. 6



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 91

Further, the **buffer 15** in *Majumdar*'s Figure 6 is a different circuit element and performs a different operation than the level shifting circuit of Okamoto (EX1010). As discussed above in Section IV.C, prosecution claim 7 (corresponding to issued claim 7) was rejected as being anticipated by Okamoto. The applicant argued that Okamoto prevents a malfunction of a power device by employing a level shift circuit that includes a timing control mechanism to limit a time that both high-side and low-side switching devices are in the "on" state. EX1002, 24 (citing EX1010, 4:9-15). The applicant argued that "Okamoto's timing control device or

level shifting circuit is different than a voltage detecting device." EX1002, 24; EX1003, ¶ 99.

Unlike Okamoto's timing control device, as discussed in Section VI.A.4[7.3.1] below, the **buffer 15** in *Majumdar*'s Figure 6 above performs the same features of, and discloses or renders obvious, the voltage detecting device in claim 7 of the '850 patent, because the **buffer 15** detects a potential at an output line of a reverse level shift part (output line of switching element 13). EX1003, ¶ 1000.

2. Overview of *Cowles*

Cowles is directed to an "Input Buffer and Method for Voltage Level Detection." EX1006, Title. *Cowles* teaches that it was well-known to configure a buffer as a voltage detector. EX1003, ¶ 101. *Cowles* explains that "input buffers are configured for optimizing voltage detection. Through use of input buffers configured as voltage detectors, a determination can be made whether to initiate or cease a particular system function." EX1006, 1:15-21. Further, *Cowles* explains that a buffer may be used to detect the level of voltage supplied to an integrated circuit, "including the detection of specified ranges for which an integrated circuit is designed, prohibiting operation of the integrated circuit if the level of voltage is outside the specified range, or determining whether a threshold level has been reached before permitting operation of a particular application within the integrated circuit." EX1006, 1:21-28. *Cowles* explains that "buffers configured as voltage

detectors are configured to operate for only one threshold level, i.e., trip for only one point, to confirm whether the voltage level is above or below the threshold level." EX1006, 1:29-32. For example, *Cowles* notes that buffers configured as voltage detectors are "generally designed to provide for two states of operation, i.e., the input buffer is configured to accept high or low voltage signals from external sources and then provide a logic state to the integrated circuit corresponding to the high or low signals." EX1006, 1:61-67; EX1003, ¶ 101.

Thus, *Cowles* teaches that it was well-known to configure a buffer to detect a voltage (e.g., a threshold voltage) and output a logic signal when the threshold voltage is detected. EX1003, ¶ 102.

Cowles is analogous art to the '850 patent. The '850 patent's Field of the Invention section states that "[t]he present invention relates to a semiconductor device, and more particularly, to a high voltage integrated circuit." EX1001, 1:10-11. *Cowles* is within the same field of endeavor, as it describes that "[i]nput buffers have been long used in various analog and digital applications," and that "input buffers input buffers are configured for optimizing voltage detection." EX1005, 1:15-18. *Cowles* discloses, for example, that input buffers configured as voltage detectors can be connected to the input terminals of transistors. EX1005, 2:8-16. Thus, *Cowles* is directed to optimizing the use of input buffers as voltage detectors for semiconductor devices, and is therefore directed to the same field of endeavor as

the ’850 patent, i.e., semiconductor devices. EX1003, ¶ 103.

3. Overview of Challenge to Claim 7

As shown in Section VI.A.4 below, *Majumdar*, which was not considered during prosecution, discloses or at least renders obvious the arrangement of the semiconductor device of claim 7, including the high potential part (limitation [7.1]), the reverse level shift part (limitation [7.2]), and the voltage detecting device (limitations [7.3.1] and [7.3.2]). As discussed in Section VI.A.4[7.3.1] below, the **buffer 15** in *Majumdar*’s Figure 6 performs the same features of the voltage detecting device in claim 7 of the ’850 patent—the feature that led to allowance of claim 7. EX1003, ¶ 105.

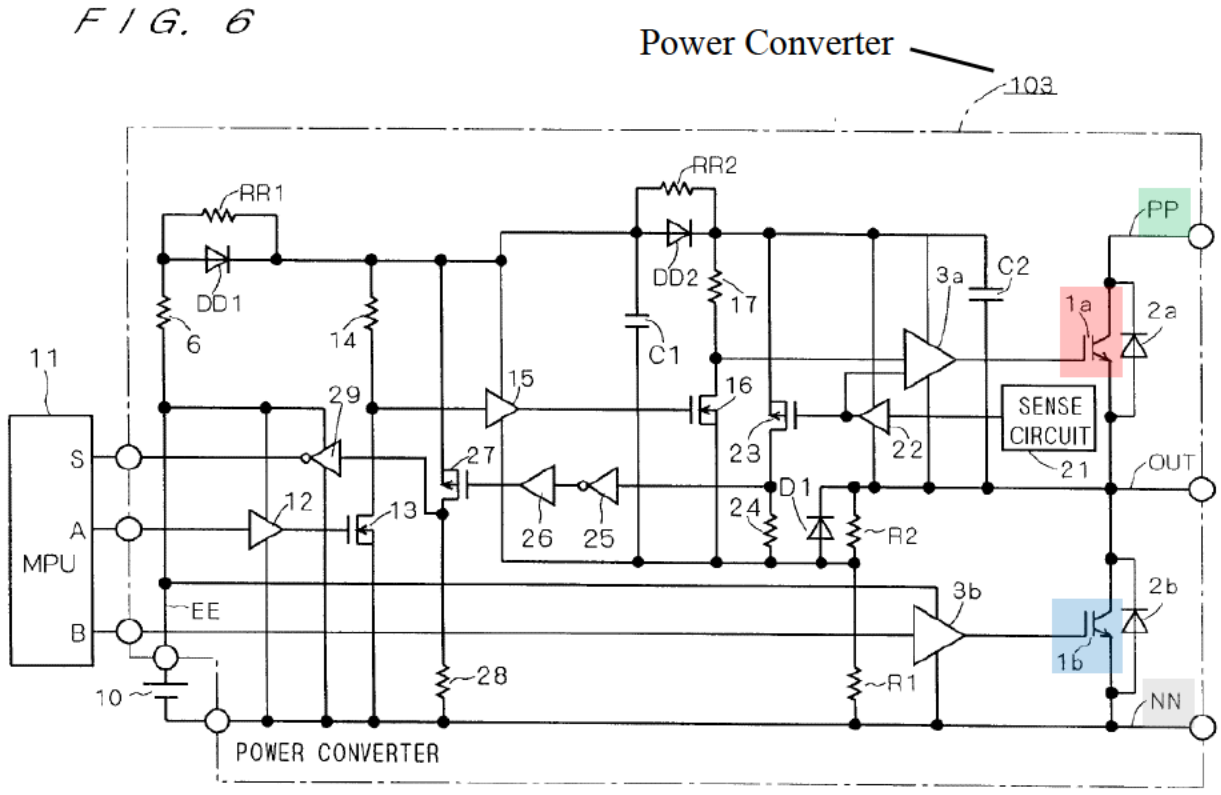
It was well-known in the art that a buffer detects a voltage. EX1003, ¶ 106. To the extent that *Majumdar* does not explicitly disclose that its buffer 15 detects a voltage, *Cowles* is cited to show that it was well-known to configure a buffer to detect a voltage. Like *Majumdar*, *Cowles* was not considered during prosecution of the ’850 patent. Reasons to combine *Majumdar* with *Cowles* are provided in Section VI.A.4[7.3.1] below. EX1003, ¶ 106.

4. Claim 7 would have been obvious over *Majumdar* in view of *Cowles*

[7.0] A semiconductor device performing drive control of first and second switching devices connected in series and interposed between a high main power potential and a low main power potential, comprising:

Majumdar discloses or at least renders obvious the preamble of claim 7. EX1003, ¶ 107.

As shown in Figure 6 below, *Majumdar* discloses a power converter 103 (*semiconductor device*) that includes a **first power switching element 1a** (e.g., IGBT) (*first switching device*) connected in series with a **second power switching element 1b** (e.g., IGBT) (*second switching device*). EX1005, 8:46-52; EX1003, ¶ 108.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 108

The power converter 103 is a *semiconductor device* because the power converter 103 includes numerous semiconductor components, such as **first power switching element 1a** (e.g., IGBT) (*first switching device*) connected in series with a **second power switching element 1b** (e.g., IGBT) (*second switching device*). EX1005, 8:46-52. Transistors such as IGBTs (i.e., insulated gate bipolar transistors) are well-known to be semiconductor devices. EX1005, 1:1:38-40 (explaining that IGBT is an abbreviation for "insulated gate bipolar transistor"); EX1013, 16.89 ("A transistor is a semiconductor amplifier."); EX1014, 1:8-10 ("The present invention

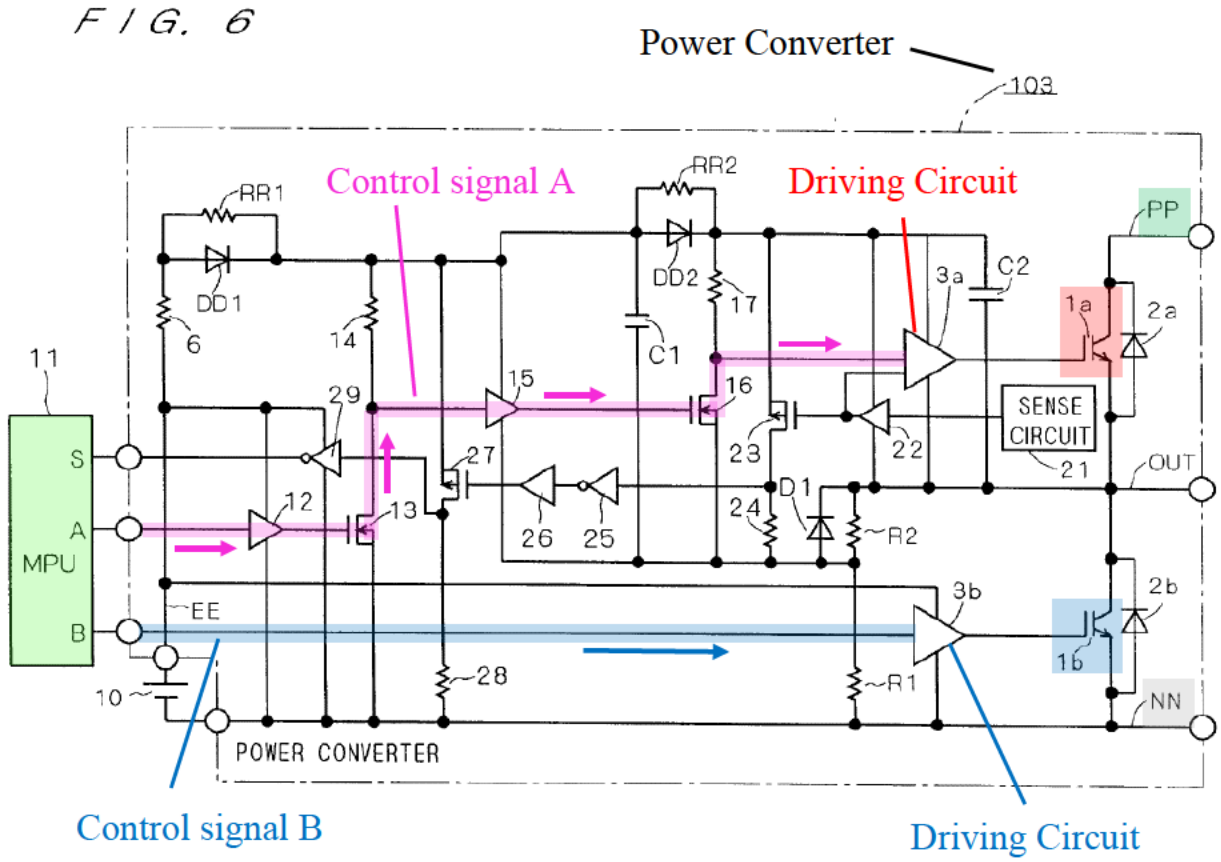
relates to a semiconductor device such as an integrated gate bipolar transistor (IGBT)…."); EX1015, 1:12-14 ("The present invention relates in general to a semiconductor device, and more particularly, to an insulated gate bipolar transistor (IGBT)…."); EX1003, ¶ 109.

As shown in Figure 6, the **first power switching element 1a** (*first switching device*) and **second power switching element 1b** (*second switching device*) are interposed between a **high potential power line PP** (*high main power potential*) and a **low potential power line NN** (e.g., ground) (*low main power potential*).[8] EX1005, 8:46-52; EX1003, ¶ 110.

As shown in Figure 6, *Majumdar* discloses that the **first power switching element 1a** (*first switching device*) is driven by a driving circuit 3a, and the **second**

[8] In *Majumdar*, the arrangement of the switching elements 1a, 1b in series between the high and low potential power lines NN, PP in Figure 6 (third embodiment) is the same as the arrangement in Figure 2 (first embodiment), as noted above in Section VI.A.1. *Majumdar*'s third embodiment illustrated in Figure 6 additionally includes a sense circuit 21, and another level shift circuit for level shifting a detection signal from the sense circuit 21. EX1005, 10:54-62; Dr. Baker's declaration explains in detail how *Majumdar's* third embodiment includes features corresponding to those described with reference to *Majumdar's* first embodiment. EX1003, ¶¶ 74-89.

power switching element 1b (*second switching device*) is driven by a driving circuit 3b. EX1005, 9:20-25 ("Outputs of the driving circuits 3a and 3b are connected to control electrodes (gates in the example of the IGBTs) of the power switching elements 1a and 1b so that the driving circuits 3a and 3b drive the power switching elements 1a and 1b, respectively."), 8:42-46 (driving circuits 3a, 3b comprised in power converter). *Majumdar* explains that "[t]he **microcomputer [MPU] 11** outputs a **control signal A** for driving the power switching element 1a and a **control signal B** for driving the power switching element 1b," where the **control signal A** is input to the driving circuit 3a, and the **control signal B** is input to the driving circuit 3b. EX1005, 9:55-61. The microcomputer 11, driving circuit 3a, and driving circuit 3b thus perform *drive control* of the **first power switching element 1a** (*first switching device*) and **second power switching element 1b** (*second switching device*). EX1003, ¶ 110.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 110

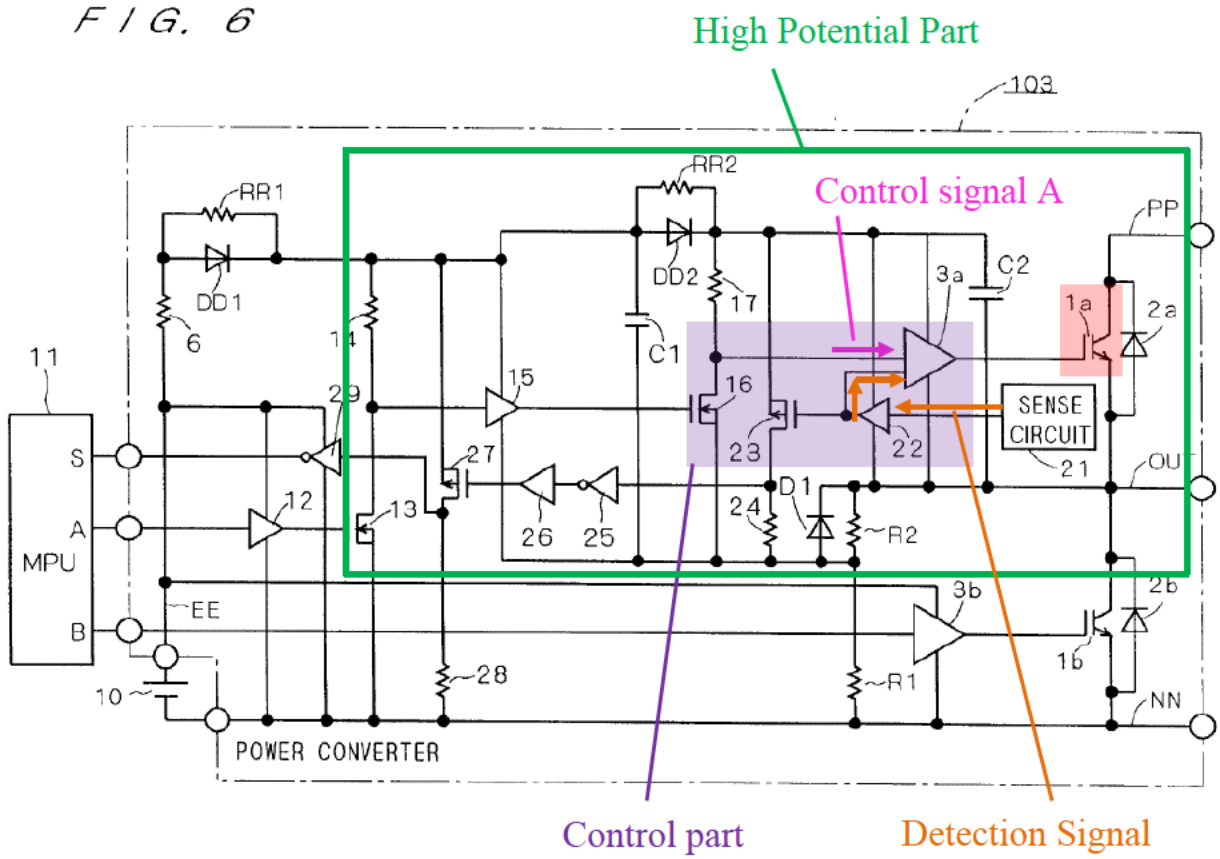
Accordingly, *Majumdar* discloses or at least renders obvious limitation [7.0]. EX1003, ¶ 111.

[7.1] a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices;

Majumdar discloses or at least renders obvious limitation [7.1]. EX1003, ¶ 112.

As shown in Figure 6 below, *Majumdar*'s power converter 103 comprises a *high potential part* (denoted in **green box**) that includes a ***control part*** (driving

circuit 3a, switching elements 16, 23, and buffer 22) configured to control conduction/non-conduction of the **first power switching element 1a** (*a high side switching device*) which is one of the first and second switching devices (1a, 1b). EX1003, ¶ 113.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 113

As discussed above with respect to limitation [7.0], the driving circuit 3a drives the **first power switching element 1a** (*high side switching device*) based on **control signal A** transmitted by the microcomputer (MPU) 11 via switching element 16. EX1005, 9:20-25, 9:55-61. *Majumdar* discloses that the driving circuit 3a drives

the control electrode of the **first power switching element 1a** (*high side switching device*), which is turned ON or OFF. EX1005, 9:20-29; EX1003, ¶ 114; *see also* EX1003, ¶¶ 92-98 (explaining how the power converter 103 in *Majumdar*'s Figure 6 operates).

Further, as shown in Figure 6 above, *Majumdar* discloses that the power converter includes a sense circuit 21 that outputs a **detection signal** based on the operation state of the **first power switching element 1a** (*high side switching device*). EX1005, 10:55-67. *Majumdar* discloses that "[t]he **detection signal** output from the sense circuit 21 is input to both the switching element 23 and the driving circuit 3a through a buffer 22. When a value of the **detection signal** exceeds a predetermined range, the driving circuit 3a drives the power switching element 1a to be turned OFF." EX1005, 11:21-26. Thus, *Majumdar* discloses that the **first power switching element 1a** (*high side switching device*) is driven ON or OFF by the driving circuit 3a based on the **control signal A** received via the switching element 16 or the **detection signal** received via the buffer 22. EX1005, 9:20-25, 9:55-61, 11:21-26; EX1003, ¶ 115.

Accordingly, as shown in Figure 6 above, *Majumdar* discloses or at least renders obvious a *high potential part* (denoted in **green box**) including a ***control part*** (driving circuit 3a, switching elements 16, 23, and buffer 22) *configured to control conduction/non-conduction* (ON/OFF) *of a high side switching device* (the

first power switching element 1a), *which is one of said first and second switching devices*, as recited in limitation [7.1]. EX1003, ¶ 116.

Thus, *Majumdar* discloses, or at least renders obvious limitation [7.1]. EX1003, ¶ 117.

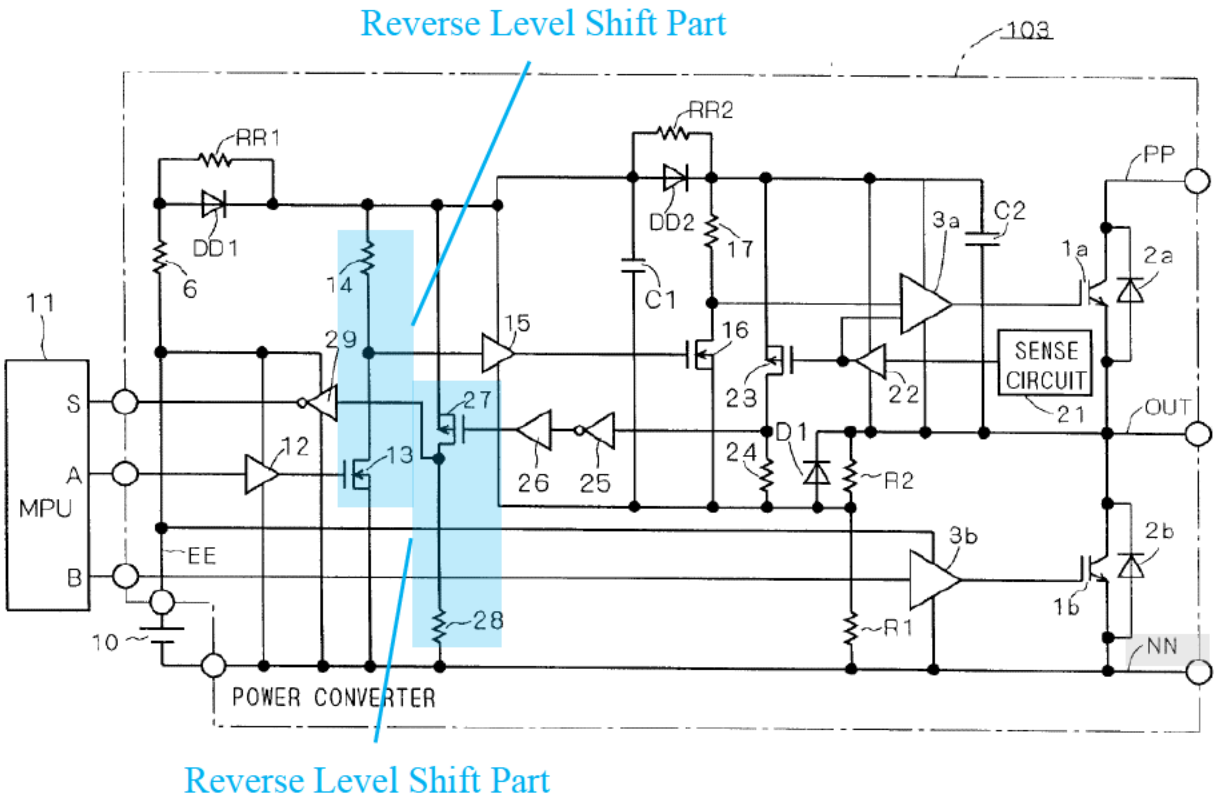
[7.2] a reverse level shift part configured to level-shift a signal from said high potential part to supply the level-shifted signal to a low side logic circuit operating on the basis of said low main power potential; and[9]

Majumdar discloses or at least renders obvious limitation [7.2]. EX1003, ¶ 118. As shown in Figure 6 below, *Majumdar* discloses a **reverse level shift part** (switching element 27, resistor 28, switching element 13, and resistor 14). As discussed in more detail below, *Majumdar* expressly discloses that the switching element 27, resistor 28, switching element 13, and resistor 14 collectively constitute a "level shift circuit." EX1005, 11:8-12. Therefore, the switching element 27, resistor 28, switching element 13, and resistor 14 collectively correspond to the

[9] As discussed above in Section IV.B, claim 7 corresponds to the second embodiment (Figure 25) of the '850 patent. In describing the second embodiment shown in Figure 25, the '850 patent admits that the arrangement of the reverse level shift-part was known in the art. EX1001, 19:42-44 ("[P]roviding a high voltage transistor such as the HPMOS transistor 51 in the high side for use as a reverse level shift transistor has conventionally been performed."). EX1003, ¶ 119.

reverse level shift part, as shown in Figure 6. EX1003, ¶ 120.

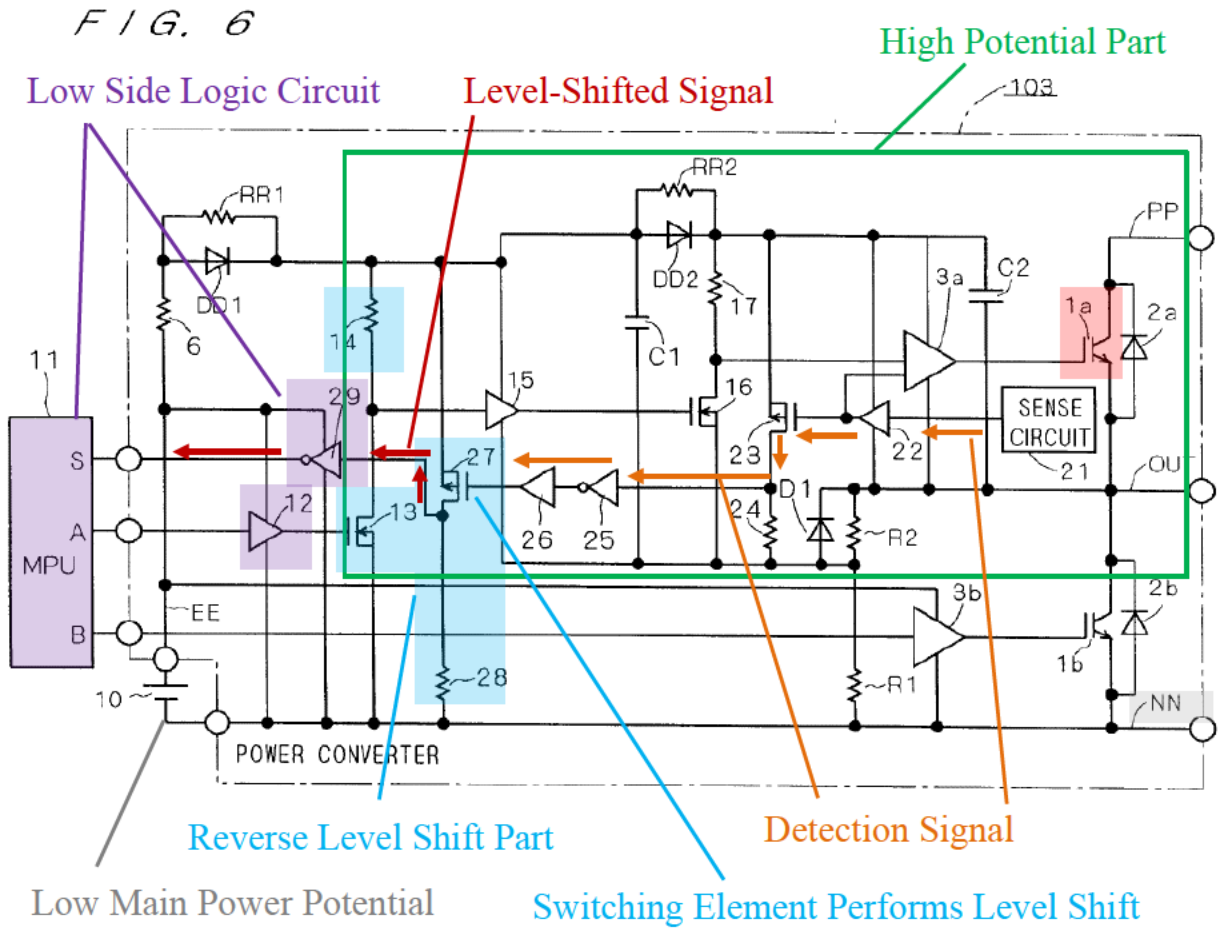
FIG. 6



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 120

As shown in Figure 6 below, *Majumdar* discloses that the **reverse level shift part** (switching element 27, resistor 28, switching element 13, and resistor 14) is configured to level shift a signal from the **high potential part** (the **detection signal**) to supply the **level-shifted signal** to a **low side logic circuit** (inverter 29, microcomputer (MPU) 11, and buffer 12) operating on the basis of the **low main power potential**. As shown in Figure 6 below, the **low side logic circuit** (inverter 29, microcomputer (MPU) 11, and buffer 12) are outside of the **high potential part**.

EX1003, ¶ 121.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 121

As described above with respect to limitation [7.1], *Majumdar* discloses that "[t]he **detection signal** output from the sense circuit 21 is input to both the switching element 23 and the driving circuit 3a through a buffer 22." EX1005, 11:21-26. As shown in Figure 6 above, *Majumdar* discloses that the **detection signal** is outputted to the switching element 23 and is then outputted to an inverter 25, a buffer 26, and a switching element 27. EX1005, 11:18-21. *Majumdar* discloses that "[t]he level

shift circuit for transmitting the **detection signal** carries out a **level shift in a reverse direction** to the level shift circuit for transmitting a control signal A. In other words, the power converter 103 comprises a **series circuit of a switching element 27 and a resistive element 28 in addition to a series circuit of the switching element 13 and the resistive element 14 as the level shift circuit I1** (FIG. 1)." EX1005, 11:5-12. Thus, *Majumdar* discloses that a **reverse level shift part** (switching element 27, resistor 28, switching element 13, and resistor 14) performs a ***level-shift*** (in the reverse direction) of the **detection signal**, and the reverse level-shifted signal is transmitted to an inverter 29 and then is transmitted to the MPU 11 as signal S, as shown in Figure 6. EX1005, 11:5-12 (describing level shifting of detection signal), 10:54-62 (explaining that the power converter comprises a "level shift circuit for level shifting the detection signal in two stages and **transmitting the same signal to the microcomputer 11**."). EX1003, ¶ 122.

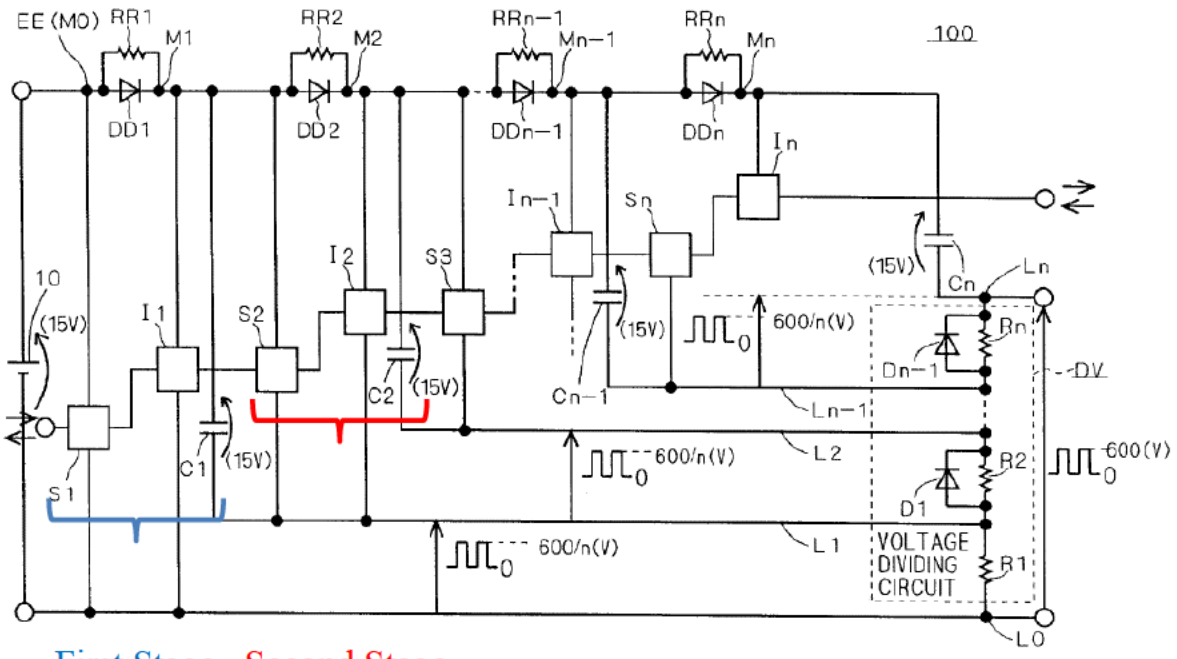
As shown in the juxtaposed Figures 1 and 6 below, *Majumdar* discloses that:

- the switching element 27, resistor 28, switching element 13, and resistor 14 collectively correspond to the **reverse level shift part**, as shown in annotated Figure 6 above; and
- the inverter 29, buffer 12, and MPU 11 collectively correspond to the **low side logic circuit**, as shown in annotated Figure 6 above.

EX1003, ¶ 123.

As shown in Figure 1 below, *Majumdar* discloses a signal level shifting circuit 100 that comprises a series of stages of signal transmitting circuits (S1, S2…Sn), level shift circuits (I1, I2…In), capacitors (C1, C2…Cn), diodes (DD1, DD2…DDn), and resistive elements (RR1, RR2…RRn) that progressively, in stepwise fashion, level shift signals at each stage. EX1005, 7:14-22 (describing stages, where n ≥ 2), 7:64-8:4 (describing level shifting over n stages), 8:5-15 (describing signal transmission at each stage based on voltage held at corresponding capacitor), 8:16-18 (describing stepwise level shifting over a plurality of stages). Figure 1 is annotated below to illustrate the first two stages. EX1003, ¶ 124.

FIG. 1



First Stage Second Stage

Majumdar (EX1005), Fig. 1 (annotated); EX1003, ¶ 124

Majumdar discloses that the signal level converter shown in Figure 1 is "used in power converters 101 to 110 according to the following [first to sixth] embodiments" shown in Figures 2-15. EX1005, 7:14-16. Thus, the signal level converter shown in Figure 1 of *Majumdar* is used in the power converter 103 shown in the above-described Figure 6 of *Majumdar*. *Id*.; EX1003, ¶ 125.

With reference to Figure 6, *Majumdar* discloses that "the power converter 103 comprises a series circuit of a switching element 27 and a resistive element 28 in addition to a series circuit of the switching element 13 and the resistive element 14 **as the level shift circuit I1 (FIG. 1)**." EX1005, 11:8-12. Further, *Majumdar* discloses that "[t]he power converter 103 further comprises an inverter 29 in addition to the buffer 12 **as the signal transmitting circuit S1** [in Figure 1]." EX1005, 11:18-20. Thus, *Majumdar* discloses that:

- the switching element 27, resistor 28, switching element 13, and resistor 14 collectively correspond to the **reverse level shift part**, as shown in annotated Figure 6 above; and
- the inverter 29, buffer 12, and MPU 11 collectively correspond to the **low side logic circuit**, as shown in annotated Figure 6 above.

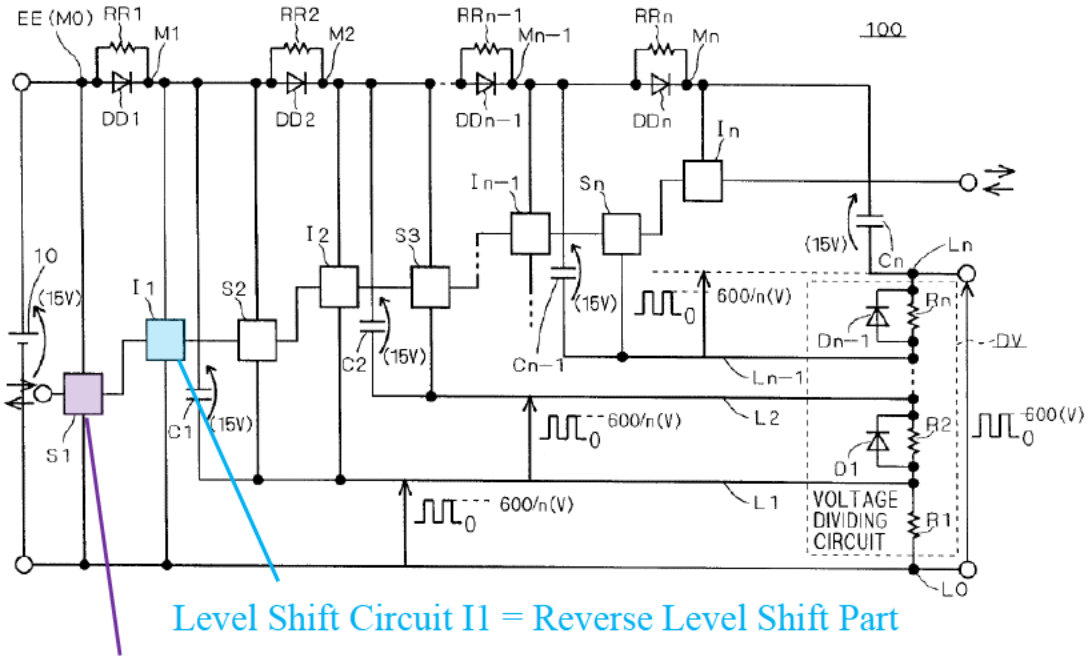
EX1003, ¶ 126. The MPU 11 is part of the **low side logic circuit** because the MPU receives the level-shifted detection signal from the inverter 29 (at input S) and transmits the control signal A to the buffer 12, as described above. EX1005, 9:55-

61 (MPU 11 outputs control signal A), 10:54-62 (level-shifted detection signal transmitted to MPU 11). The following juxtaposition of Figures 1 and 6 shows that:

- the switching element 27, resistor 28, switching element 13, and resistor 14 collectively correspond to the **reverse level shift part** in Figure 6, which is the **level shift circuit I1** in Figure 1; and
    - "[T]he power converter 103 comprises a series circuit of a switching element 27 and a resistive element 28 in addition to a series circuit of the switching element 13 and the resistive element 14 as the **level shift circuit I1** (FIG. 1)." EX1005, 11:8-12.
- the inverter 29, buffer 12, and MPU 11 collectively correspond to the **low side logic circuit** in Figure 6, which is the signal transmitting circuit S1 in Figure 1.
    - "The power converter 103 further comprises an inverter 29 in addition to the buffer 12 as the **signal transmitting circuit S1** [in Figure 1]." EX1005, 11:18-20. The MPU 11 is part of the **low side logic circuit** as described above.

EX1003, ¶ 127.

FIG. 1

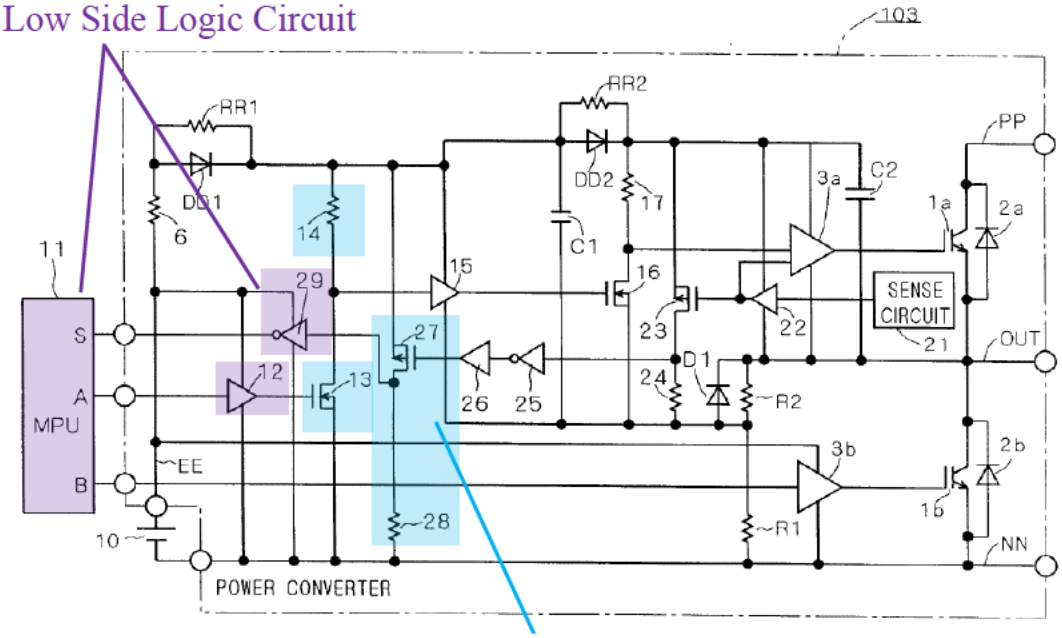


Level Shift Circuit I1 = Reverse Level Shift Part

Signal Transmitting Circuit S1 = Low Side Logic Circuit

FIG. 6

Low Side Logic Circuit



Reverse Level Shift Part

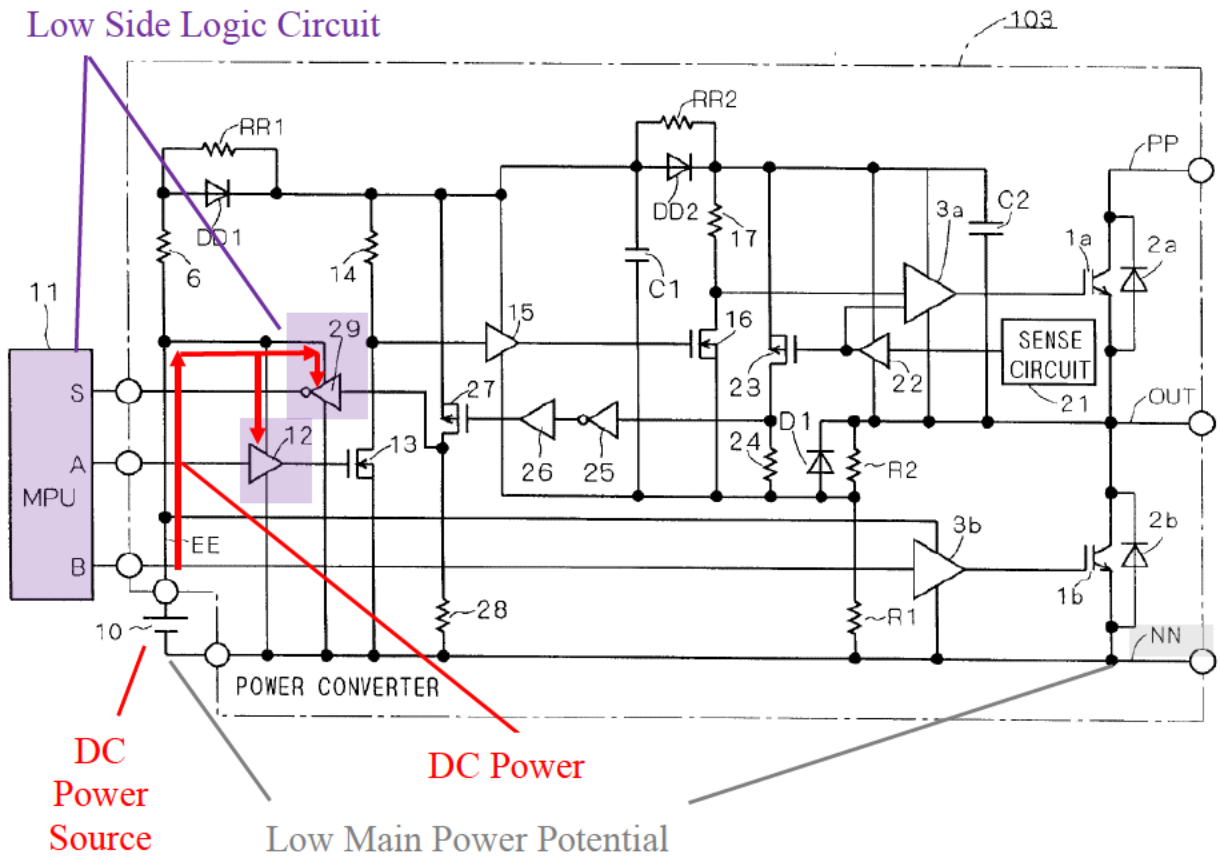
Majumdar (EX1005), Figs. 1 and 6 (annotated); EX1003, ¶ 127

Accordingly, *Majumdar* discloses or at least renders obvious *a reverse level shift part* (the switching element 27, resistor 28, switching element 13, and resistor 14 in Figure 6, which correspond to the level shift circuit I1 in Figure 1) *configured to level-shift a signal* (switching element 27 level shifts detection signal) *from said high potential part* (**detection signal** transmitted from sense circuit 21 in the **high potential part**) *to supply the level-shifted signal to a low side logic circuit* (inverter 29, MPU 11, and buffer 12) *operating on the basis of said low main power potential*, as recited in limitation [7.2]. EX1003, ¶ 128.

As shown in Figure 6 below, the inverter 29 and buffer 12 are both connected to the **low main power potential (NN)** (e.g., ground) and thus operate on the basis of the low main power potential. EX1005, 8:48-52 (describing low main potential power line NN). The inverter 29 and buffer 12 receive a DC voltage as a source voltage. EX1005, 8:5-15 (describing signal level transmitting circuit I1, which includes the inverter 29 and buffer 12, as receiving a DC source voltage), 11:18-20 (inverter 29 and buffer 12 included in signal level transmitting circuit I1), 10:15-16 (DC power source 10 set to 15 volts). As shown in Figure 6, the DC source voltage 10 is also connected to the **low main power potential (NN)** (e.g., ground). EX1005, 7:50-53. Further, as shown in Figure 6, the microcomputer (MPU) 11 is connected to the DC power source 10. EX1005, 9:43-45. The MPU 11 requires power to, among other things, output the control signals A, B for operation of the high-side

and low-side power switching elements 1a, 1b, and monitor the operation state of the high-side power switching element 1a by receiving the level-shifted detection signal. EX1005, 9:55-57 (MPU 11 outputting control signals A, B), 10:55-67 (MPU 11 receiving level-shifted detection signal and monitoring the operation state of the high-side power switching element 1a based on the detection signal). Thus, all component elements of the **low side logic circuit** (inverter 29, buffer 12, and MPU 11) operate on the basis of the **low main power potential**. EX1003, ¶ 129.

FIG. 6



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 129

Further, it is well-known that an inverter is a logic circuit. *See* EX1008, 110-111 (textbook explaining that an inverter, which is commonly referred to as a NOT gate, is a logic circuit for outputting binary values of 0 or 1). Likewise, a microcomputer is a logic circuit. *See* EX1008, 12 (explaining that a "digital computer is a system whose functional elements consist of arithmetic/logic units (ALUs), control units, memory or storage units, and input/output (I/O) equipment."). Thus, the inverter 29 and MPU 11 in *Majumdar*'s Figure 6, which are part of the

low side logic circuit, are logical circuit elements. EX1003, ¶ 130. The same would at least have been obvious. A POSITA would have found it obvious to implement the inverter 29 as a logic circuit because the inverter 29 transmits the detection signal (at input S) as outputted from the switching element 27 to the microcomputer (MPU) 11 as part of the signal transmitting circuit S1 in Figure 1, as described above. EX1005, 11:18-20. *Majumdar* discloses that the switching element 27 is a p-channel type high voltage MOSFET (metal oxide semiconductor field effect transistor). EX1005, 11:15-117. Thus, the inverter 29 would transmit the detection signal as a logic signal to the MPU 11, which operates as digital computer. EX1008, 12; EX1003, ¶ 130.

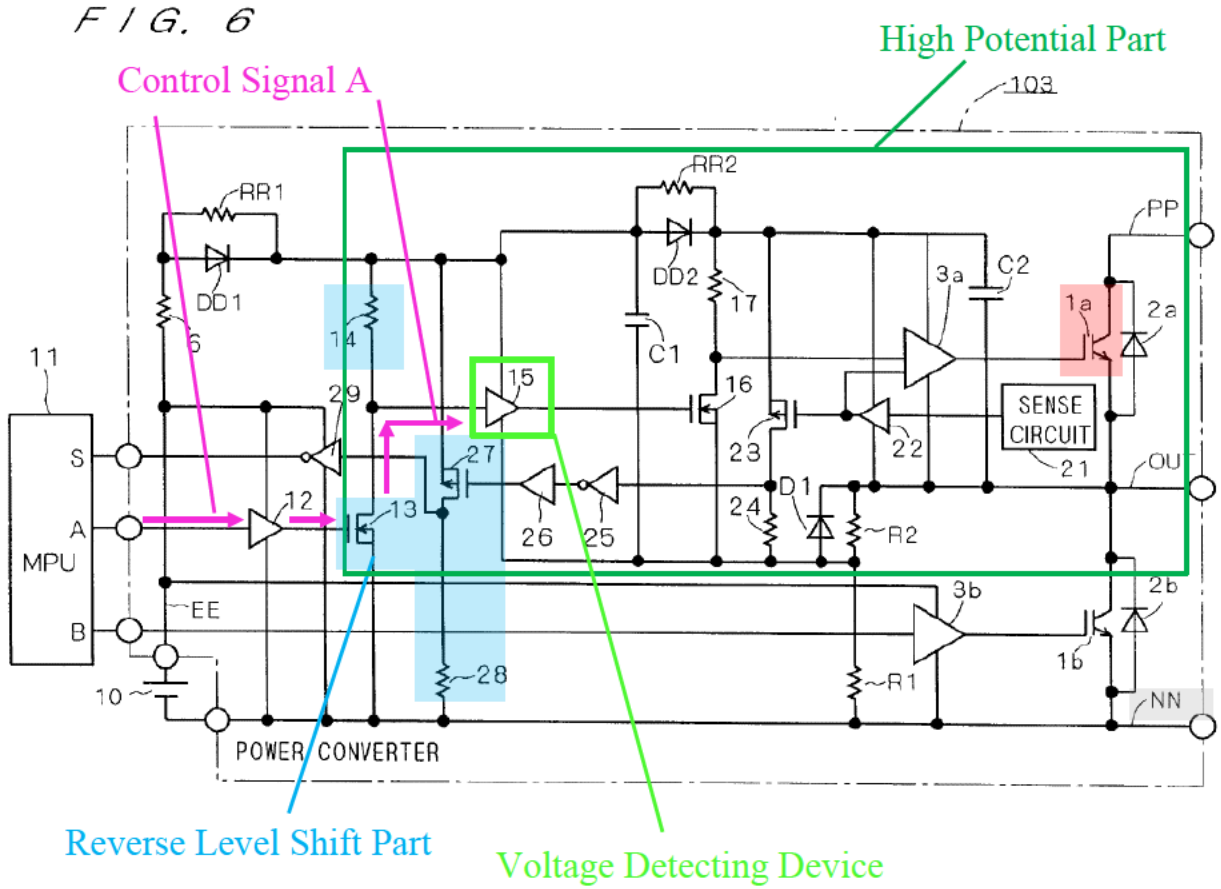
Accordingly, *Majumdar* discloses or at least renders obvious limitation [7.2] for the above reasons. EX1003, ¶ 131.

[7.3.1] a voltage detecting device provided in said high potential part and configured to detect a potential at an output line of said reverse level shift part and to supply a logic value based on said potential for said control part,

Limitation [7.3.1] is rendered obvious by *Majumdar* and *Cowles*. EX1003, ¶ 132. As shown in Figure 6 of *Majumdar* below, the **buffer 15** in the **high potential part** corresponds to the claimed *voltage detecting device*. EX1003, ¶ 133.

As described above with respect to limitation [7.0], the MPU 11 outputs a **control signal A** for driving the power switching element 1a via the driving circuit 3a. EX1005, 9:55-61. The **control signal A** is transmitted from the MPU 11

through the buffer 12 and is then level-shifted by the switching element 13, as shown in Figure 6. EX1005, 9:57-60. As described above with respect to limitation [7.2], *Majumdar* discloses that the switching element 27, resistor 28, switching element 13, and resistor 14 in Figure 6 collectively correspond to the **reverse level shift part** (level shift circuit I1 in Figure 1). EX1005, 11:8-12. Thus, *Majumdar* discloses that the **control signal A** is transmitted to the **reverse level shift part** (switching element 13) and is then level shifted before being transmitted to the **buffer 15** (the claimed *voltage detecting device*), as shown in Figure 6. EX1003, ¶ 134.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 134

As shown in the juxtaposition of Figures 1 and 6 below, *Majumdar* discloses that the **buffer 15** (the claimed *voltage detecting device*) corresponds to the signal transmitting circuit S2 in Figure 1, which receives a level-shifted signal from the level shift circuit I1 (i.e., the **reverse level shift part**, which includes the switching element 27, resistor 28, switching element 13, and resistor 14 in Figure 6). EX1005, 9:37-39 (explaining that the power converter comprises "a buffer 15 as the signal transmitting circuit S2"), 11:8-12, 11:20-21 (signal transmitting circuit S2 includes buffer 15); EX1003, ¶ 135.

FIG. 1 Signal Transmitting Circuit S2 = Voltage Detecting Device

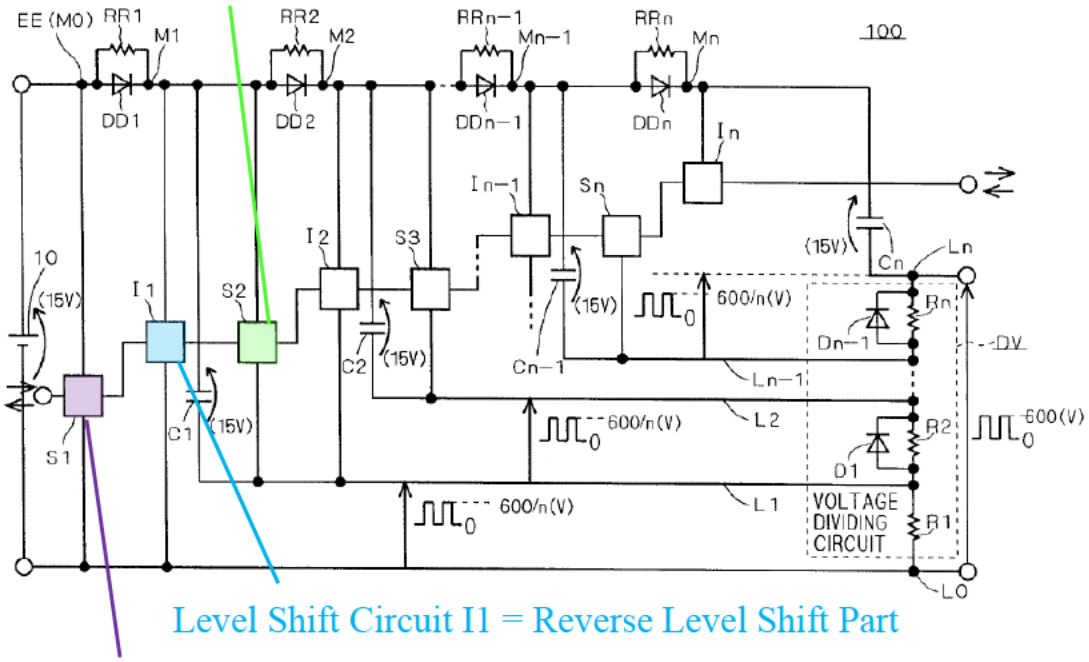
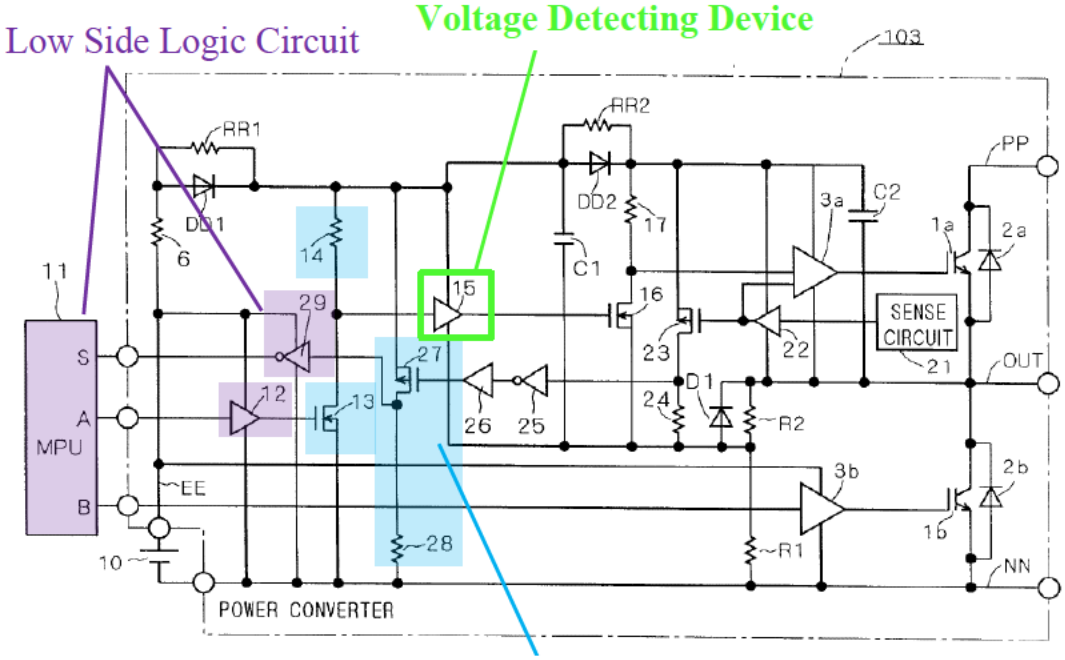
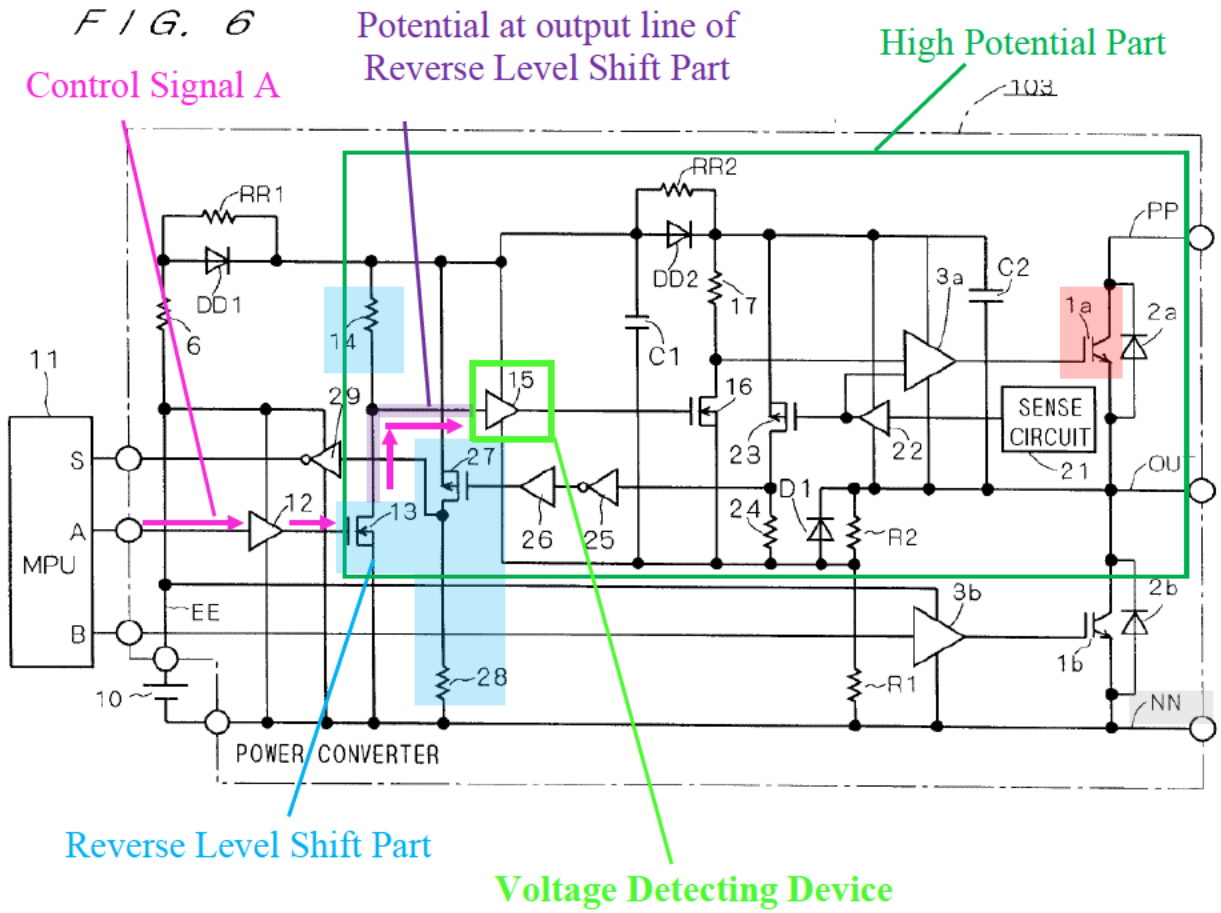


FIG. 6



Majumdar (EX1005), Figs. 1 and 6 (annotated); EX1003, ¶ 135

As shown in Figure 6 below, *Majumdar* discloses that the **buffer 15** (the claimed *voltage detecting device*) receives the potential at an output line (e.g., interconnect line) of the **reverse level shift part** (i.e., the potential at the output line of the switching element 13, which (1) receives the **control signal A** and (2) is part of the **reverse level shift part**). As shown in Figure 6, the output line of the **reverse level shift part** connects the switching element 13 to the **buffer 15** and thus is an interconnect line in the **high potential part**. EX1003, ¶ 136.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 136

Thus, the **buffer 15** in Figure 6 teaches the claimed *voltage detecting device*, because the **buffer 15** receives the output of the **reverse level shift part** (switching element 13 receiving level-shifted **control signal A**), and supplies a logic value based on the potential for the control part (driving circuit 3a, buffer 22) (i.e., the level-shifted control signal A, which is based on the detection signal from the sense circuit 21). EX1005, 11:18-21 (describing buffer 15 as corresponding to the "signal transmitting circuit S2" in Fig. 1), 10:55-62 and 11:21-23 (describing that level-shifted detection signal is transmitted to the microcomputer 11 via the switching element 23), 9:55-61 ("[t]he microcomputer 11 outputs a control signal A for driving the power switching element 1a."); EX1003, ¶ 137.

As shown in Figure 6 above, the **buffer 15** is provided in the **high potential part**. EX1003, ¶ 138. Thus, *Majumdar* discloses that the **buffer 15** (the claimed *voltage detecting device*) is provided in the **high potential part** and receives a potential at an output line of the **reverse level shift part** (output of switching element 13) and supplies a logic value (**control signal A**) to the control part based on the potential for the control part (driving circuit 3a, buffer 22) (i.e., the level-shifted control signal A, which is based on the detection signal from the sense circuit 21). EX1003, ¶ 138.

Majumdar does not expressly disclose that the buffer detects a voltage. EX1003, ¶ 139. However, as taught by *Cowles* (EX1006), it was well-known to

configure a buffer to detect a voltage. *Cowles* is directed to an "Input Buffer and Method for Voltage Level Detection." EX1006, Title. In its "Background of the Invention" section, *Cowles* teaches that it was well-known to configure a buffer as a voltage detector. EX1006, 1:14-2:17; EX1003, ¶ 139. *Cowles* explains that "input buffers are configured for optimizing voltage detection. Through use of input buffers configured as voltage detectors, a determination can be made whether to initiate or cease a particular system function." EX1006, 1:15-21. Further, *Cowles* explains that a buffer may be used to detect the level of voltage supplied to an integrated circuit, "including the detection of specified ranges for which an integrated circuit is designed, prohibiting operation of the integrated circuit if the level of voltage is outside the specified range, or **determining whether a threshold level has been reached before permitting operation of a particular application within the integrated circuit**." EX1006, 1:21-28. *Cowles* explains that "buffers configured as voltage detectors are configured to operate for only one threshold level, i.e., trip for only one point, to **confirm whether the voltage level is above or below the threshold level**." EX1006, 1:29-32. For example, *Cowles* notes that buffers configured as voltage detectors are "generally designed to provide for two states of operation, i.e., the input buffer is configured to accept high or low voltage signals from external sources and then provide a logic state to the integrated circuit corresponding to the high or low signals." EX1006, 1:61-67. Thus, *Cowles* teaches

that it was well-known to configure a buffer to detect a voltage (e.g., a threshold voltage) and output a logic signal when the threshold voltage is detected. EX1003, ¶ 140.

As an example, *Cowles* discloses a buffer that is configured as a voltage detector in Figure 1 below. In the prior art example below, *Cowles* discloses that an **input voltage** is compared to a **reference voltage** to determine whether the **input voltage** is above or below a **reference voltage** (threshold voltage). If the input voltage is above the threshold voltage, a first logic state is output (e.g., a high signal), but if the input voltage is below the threshold voltage, a second logic state is output (e.g., a low signal). EX1006, 1:67-2:28; EX1003, ¶ 141.

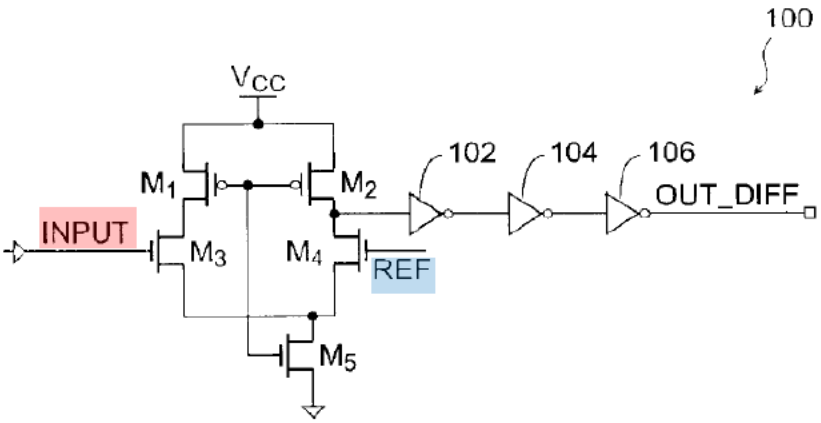


FIG. 1
(PRIOR ART)

Cowles (EX1006), Fig. 1 (annotated); EX1003, ¶ 141

Thus, *Cowles* teaches that it was known to configure a buffer to detect a

voltage (e.g., whether the voltage is above or below a reference voltage). EX1003, ¶ 142. A POSITA would have been motivated to modify Majumdar's buffer 15 (voltage detecting device) to detect whether the voltage input to the buffer 15 from the output of the reverse level shift part (switching element 13) above or below a reference, or threshold, voltage to supply a control signal to switching element 16. As shown in Figure 1 below, the reference (e.g., threshold) voltage may be obtained by performing a voltage division of the source voltage (Vcc). EX1003, ¶ 142.

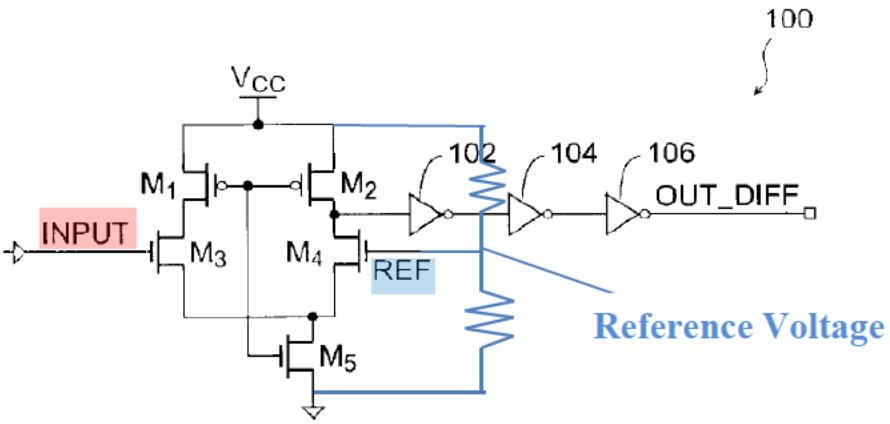


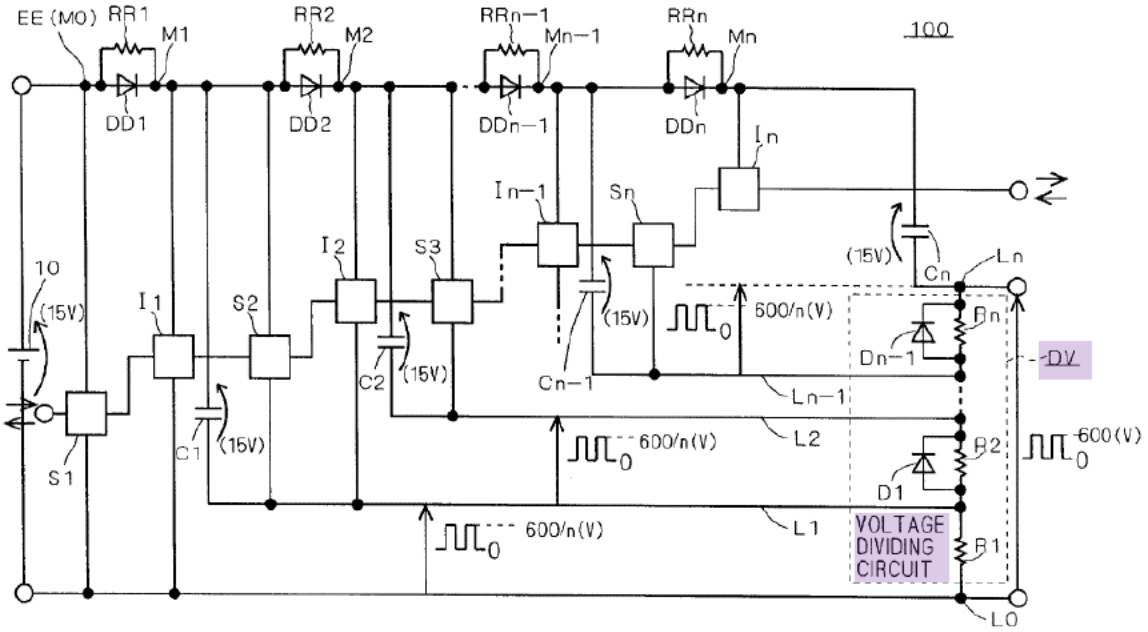
FIG. 1
(PRIOR ART)

Cowles (EX1006), Fig. 1 (annotated); EX1003, ¶ 142

Dividing a voltage (e.g., source voltage) across two resistors in series was well-known in the art. For example, as shown in Figure 1 below, *Majumdar* discloses a voltage dividing circuit DV that divides a source voltage (e.g., 600 volts) between two or more resistors R1 to Rn connected in series. EX1005, 7:23-54;

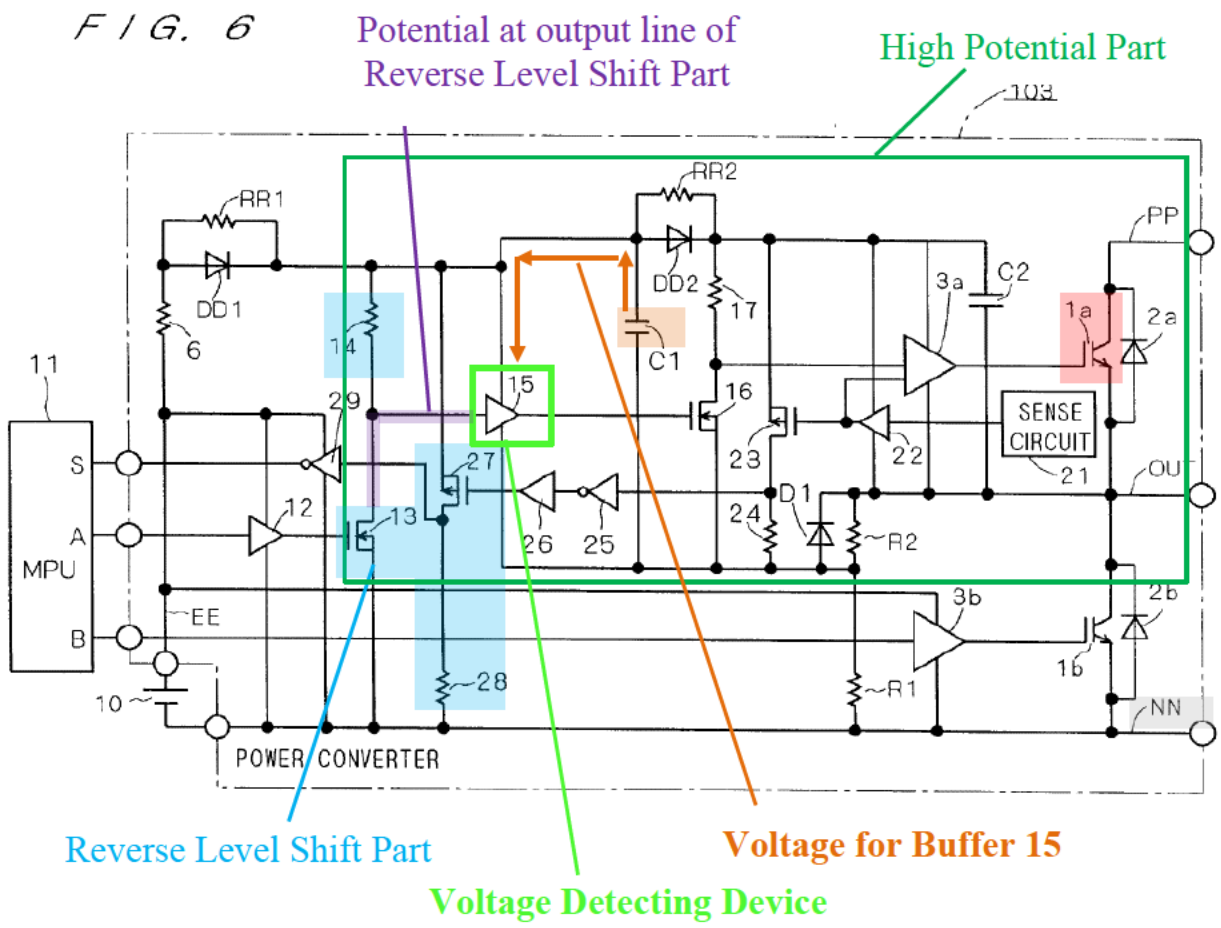
EX1003, ¶ 143.

FIG. 1



Majumdar (EX1005), Fig. 1 (annotated); EX1003, ¶ 143

As shown in Figure 6 below, *Majumdar* discloses that "[t]he buffer 15 receives a supply of a source voltage through a voltage held by a capacitor C1." EX1005, 9:48-49. *Majumdar* discloses that capacitor C1 holds a level-shifted voltage of 15 volts for buffer 15 (e.g., the top of buffer 15 is at 315 volts, and the bottom of buffer 15 is at 300 V). EX1005, 10:24-29, 10:16-17; EX1003, ¶ 144.



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 144

In view of *Cowles*' disclosure of the advantage of determining whether an input voltage is above or below a reference (threshold) voltage and then outputting a logic value based on the determination, a POSITA would have been motivated to modify *Majumdar*'s **buffer 15** (*voltage detecting device*) to determine whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is above a reference, or threshold, voltage. EX1003, ¶ 145. *Cowles* teaches it is advantageous, particularly when transmitting signals to integrated circuits, as in

Majumdar, to configure buffers as voltage detectors so that "a determination can be made whether to initiate or cease a particular system function." EX1006, 1:15-21. For example, *Cowles* explains that a buffer may be used to detect the level of voltage supplied to an integrated circuit, "including the detection of specified ranges for which an integrated circuit is designed, prohibiting operation of the integrated circuit if the level of voltage is outside the specified range, or **determining whether a threshold level has been reached before permitting operation of a particular application within the integrated circuit**." EX1006, 1:21-27. *Cowles* explains that "buffers configured as voltage detectors are configured to operate for only one threshold level, i.e., trip for only one point, to **confirm whether the voltage level is above or below the threshold level**." EX1006, 1:29-32; EX1003, ¶ 145.

Thus, a POSITA would have been motivated to modify *Majumdar*'s **buffer 15** to detect whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is above a reference, or threshold, voltage, and if so, to transmit the control signal A to the drive circuit 3a for turning ON/OFF the high-side switching device 1a. EX1003, ¶ 146. As explained by *Cowles*, buffers configured as voltage detectors are "generally designed to provide for two states of operation, i.e., the input buffer is configured to accept high or low voltage signals from external sources and then provide a logic state to the integrated circuit corresponding to the high or low signals." EX1006, 1:61-67. A POSITA would

therefore have been motivated to modify *Majumdar*'s **buffer 15** to detect whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is at a sufficient voltage level, and if so, output a logic signal to ensure that the drive circuit 3a receives the required signal to drive the high-side switching device as intended. EX1003, ¶ 146.

A POSITA would have been motivated to modify *Majumdar*'s **buffer 15** to detect the voltage at the output line of the switching element 13 (**reverse level shift part**) and thereby provide a state of operation to the switching element 16 for operation of the driving circuit 3a (which drives the high-side switching element 1a), based on whether the output voltage of the reverse level shift part is at the threshold value for operation of the high-side control part. As noted above, *Cowles* teaches that buffers configured as voltage detectors may "**detect a voltage level when it is in a 'high' condition, i.e., greater than a threshold voltage, and in a 'low' condition, i.e., lower than a threshold voltage**." EX1006, 2:1-7; EX1003, ¶ 147.

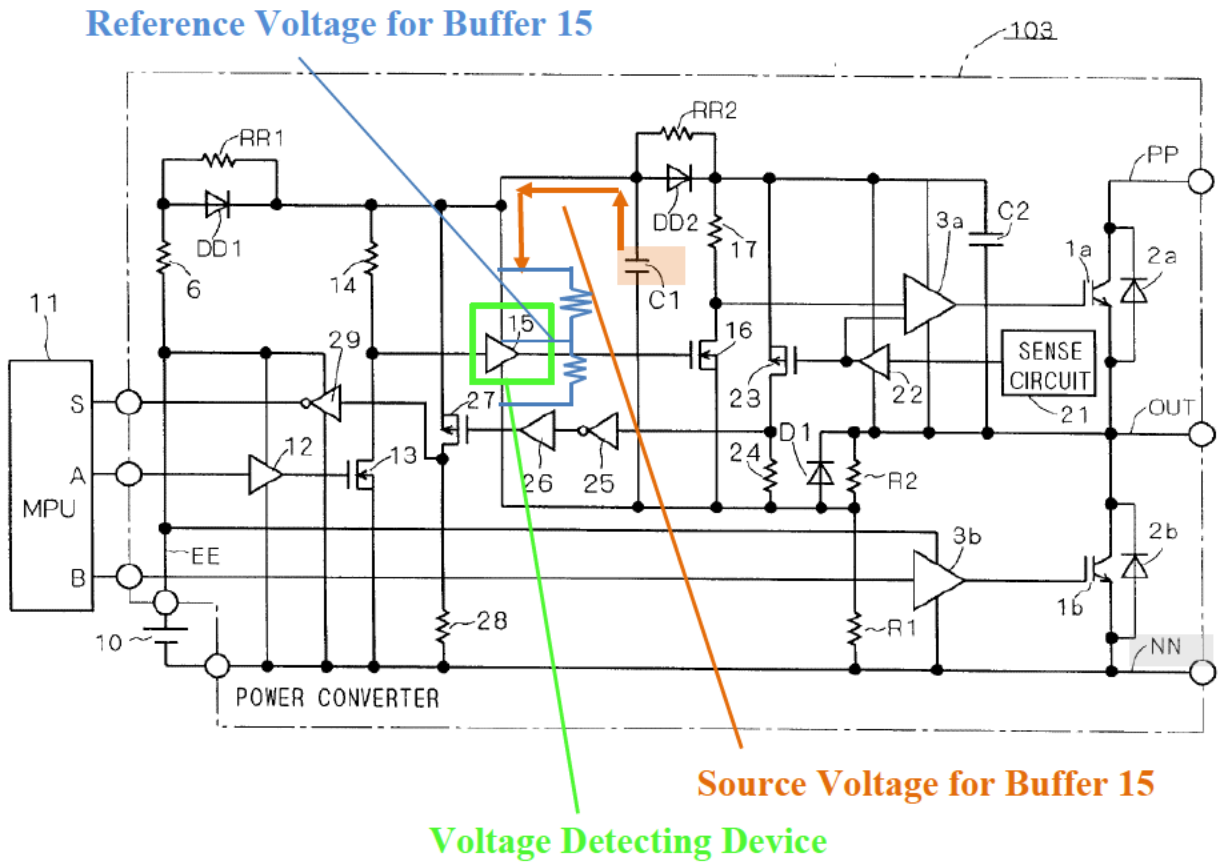
A POSITA would have been motivated to make this modification because it is the combination of prior art elements (*Majumdar*'s **buffer 15** with a buffer configured as a voltage detector, as taught by *Cowles*) according to known methods (configuring a buffer as a voltage detector, as taught by *Cowles*) to yield the predictable result of detecting whether the voltage at the input of *Majumdar*'s buffer 15 exceeds a threshold voltage for the purpose of controlling the high-side control

part. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); EX1003, ¶ 148. Further, a POSITA would have been motivated to make this modification because it involves the use of a known technique (configuring a buffer to detect voltages, as taught by *Cowles*) to improve a similar device (*Majumdar*'s power converter) in the same way. *See KSR*, 550 U.S. at 401; EX1003, ¶ 148.

A POSITA would have had a reasonable expectation of success in making this modification, because *Cowles* teaches how to configure a buffer to detect a voltage based on a reference or threshold voltage. As described above with respect to Figure 1, *Cowles* teaches how to configure a buffer to detect whether an input voltage is greater than a reference voltage. EX1006, 1:67-2:28. As described above with respect to Figure 6, *Majumdar* discloses that "[t]he buffer 15 receives a supply of a source voltage through a voltage held by a capacitor C1." EX1005, 9:48-49. Thus, a POSITA would have had a reasonable expectation of success in configuring *Majumdar*'s **buffer 15** to determine whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is above a reference voltage. For example, a POSITA would have been motivated to obtain a reference voltage for *Majumdar*'s **buffer 15** based on the source voltage supplied to **buffer 15** by capacitor C1 (e.g., by using a voltage divider as shown above with respect to *Cowles*' reference voltage, and as shown in the modification of Figure 6 below). As described above, *Majumdar* discloses a voltage dividing circuit DV in Figure 1 that

divides a source voltage between two or more resistors R1 to Rn connected in series. EX1005, 7:23-54. Therefore, a POSITA would have been motivated to make the above modification to *Majumdar*'s **buffer 15** and would have had a reasonable expectation of success in doing so. EX1003, ¶ 149.

FIG. 6

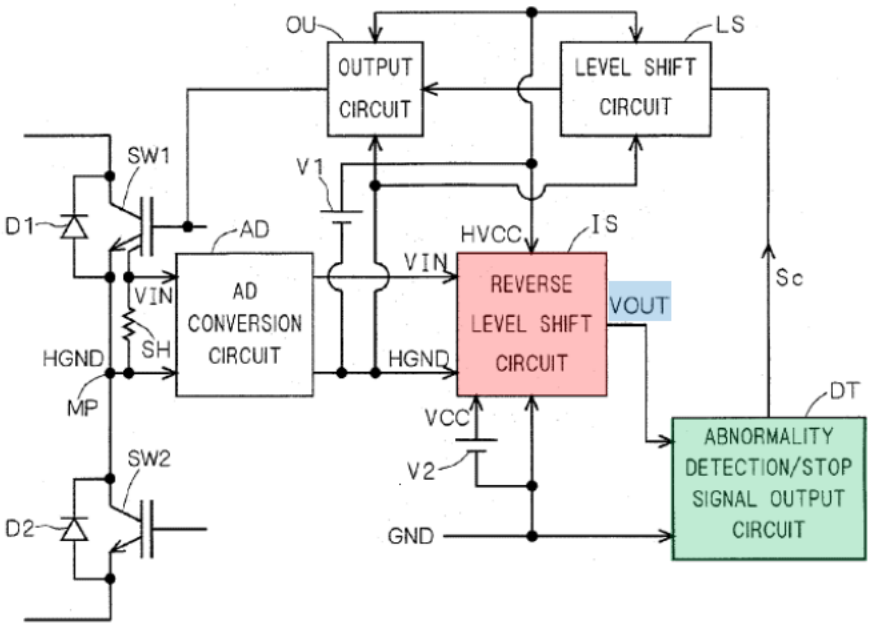


Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 149

A POSITA would have been motivated to modify to *Majumdar*'s **buffer 15** to determine whether the voltage at the output line of the switching element 13 (***reverse level shift part***), which represents the control signal A, is above a reference

voltage to facilitate determining whether the high-side switching element 1a is operating properly. For example, with reference to Figure 6 below, U.S. Patent Application Publication 2003/0012040 by Orita et al. ("Orita," EX1007) discloses the desirability of determining whether the **output voltage (VOUT)** of a **reverse level shift circuit IS** represents an abnormal condition, and then outputting a logic signal (stop signal Sc) from an **abnormality detection/stop signal output circuit DT** (logic circuit) if so to stop the operation of the high-side switching element SW1. EX1007, ¶ [0008]; EX1003, ¶ 150.

FIG. 6



Orita (EX1007), Fig. 6 (annotated); EX1003, ¶ 150

Thus, it was well-known that the output voltage of a reverse level shifter may

be used to detect whether there is an abnormal voltage and to control a high-side transistor based on that detection. EX1003, ¶ 151. A POSITA therefore would have been motivated to modify *Majumdar*'s **buffer 15** to detect the voltage at the output line of the switching element 13 (***reverse level shift part***) and thereby provide a state of operation to the switching element 16 for operation of the driving circuit 3a (which drives the high-side switching element 1a), based on whether the output voltage of the reverse level shift part is at the threshold value for operation of the high-side control part. EX1003, ¶ 151.

Modifying *Majumdar*'s **buffer 15** in view of *Cowles* to determine whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is above a reference voltage would not alter how *Majumdar*'s **buffer 15** would transmit the **control signal A** to the switching element 16 and driving circuit 3A in *Majumdar*'s disclosure itself. Rather, modifying *Majumdar*'s **buffer 15** to determine whether the voltage at the output line of the switching element 13 (**reverse level shift part**) is above a reference voltage would advantageously ensure that the high-side switching 1a is correctly turned on when the **control signal A** is at a voltage above the reference voltage, as taught by *Cowles*. EX1006, 1:67-2:28. *Majumdar* does not expressly disclose that the **buffer 15** transmits the control signal A when it is above a reference voltage, as taught by *Cowles*. However, a POSITA would have been motivated to implement this well-known implementation detail in

Majumdar, because this modification would promote accuracy in turning on the high-side switching element 1a via the **control signal A** when *Majumdar*'s the **buffer 15** detects it to be above a threshold voltage, as taught by *Cowles*. EX1003, ¶ 152.

Therefore, limitation [7.3.1] is rendered obvious by *Majumdar* in view of *Cowles*. EX1003, ¶ 153.

[7.3.2] thereby causing said control part to control conduction/non-conduction of said high side switching device.

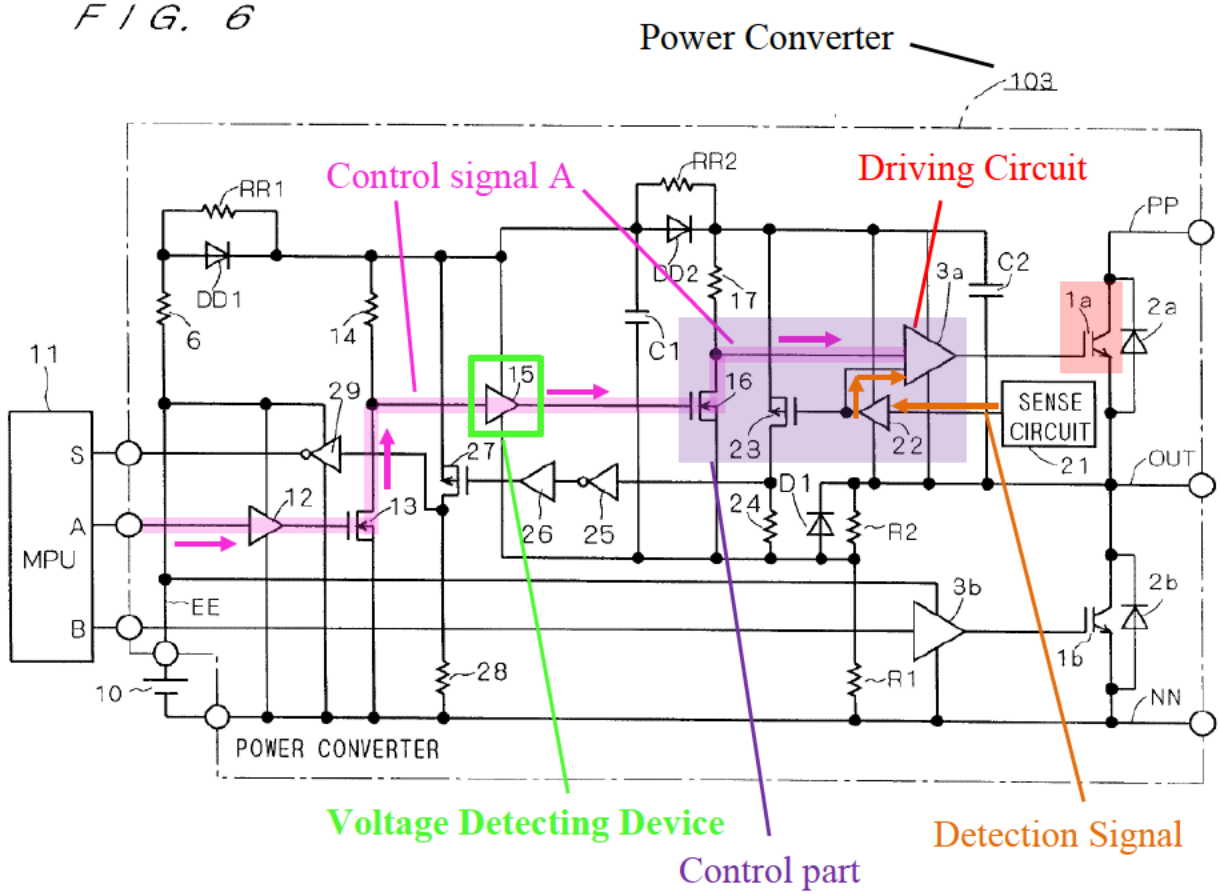
Limitation [7.3.2] is rendered obvious by *Majumdar* in view of *Cowles*. EX1003, ¶ 154.

As described above with respect to limitation [7.3.1], *Majumdar* and *Cowles* render obvious the claimed *voltage detecting device*. In particular, a POSITA would have been motivated to modify the **buffer 15** of *Majumdar*'s Figure 6 to detect a potential at an output line of the **reverse level shift part** (output of switching element 13) and supply a logic value (**control signal A**) based on the potential for the control part (driving circuit 3a, buffer 22) (i.e., the level-shifted control signal A, which is based on the detection signal from the sense circuit 21). EX1003, ¶ 155.

As shown in Figure 6 below, *Majumdar* discloses that the microcomputer (MPU) 11 outputs a **control signal A**, which is transmitted by the **buffer 15** (*voltage detecting device*) to the driving circuit 3a, which in turn controls operation of the

high-side switching device 1a. EX1005, 9:55-57 (MPU 11 transmits control signal A for control of the high-side switching device 1a), 9:37-39 (buffer 15 functions as signal transmitting circuit S2), 9:20-25 (output of driving circuit 3a drives high-side switching device 1a); EX1003, ¶ 156.

FIG. 6



Majumdar (EX1005), Fig. 6 (annotated); EX1003, ¶ 156

As described above with respect to limitation [7.1], the driving circuit 3a is part of the claimed ***control part*** (driving circuit 3a, switching elements 16, 23, and buffer 22), which controls conduction/non-conduction of the **first power switching**

element 1a (*high side switching device*) based on the **control signal A** and the **detection signal** output from the buffer 22, as shown above in Figure 6. EX1005, 9:20-25 (driving circuit 3a controls high-side switching device 1a), 9:55-61 (MPU 11 outputs control signal A), 11:21-26 ("When a value of the **detection signal** exceeds a predetermined range, the driving circuit 3a drives the power switching element 1a to be turned OFF."). EX1003, ¶ 157.

Thus, *Majumdar*'s **buffer 15** (*voltage detecting device*) causes the driving circuit 3a (*control part*) to control conduction/non-conduction (ON/OFF) of the **first power switching element 1a** (*high side switching device*). Therefore, *Majumdar* in view of *Cowles* render obvious limitation [7.3.2]. EX1003, ¶ 158.

Accordingly, for the above reasons, claim 7 is rendered obvious by *Majumdar* and *Cowles*. EX1003, ¶ 159.

VII. DISCRETIONARY INSTITUTION

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§ 325(d) or § 314(a) to deny institution of this Petition.

A. The Board Should Not Exercise Discretion to Deny Institution Under § 325(d)

The Board should not exercise its discretion under § 325(d) to deny institution because the prior art references relied on in the ground of challenge (*Majumdar* and *Cowles*) were not cited by the examiner during prosecution of the '850 patent or

cited in an Information Disclosure Statement. There is no record in the prosecution history that either *Majumdar* or *Cowles* were considered in connection with the '850 patent. Therefore, discretionary denial under § 325(d) would be inappropriate because none of the asserted prior art was previously presented to the Office. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7-9 (PTAB Feb. 13, 2020) (precedential) (first part of *Advanced Bionics* framework is not met because the same or substantially prior art or arguments were not previously presented to the Office).

Further, the prior art cited in the ground of challenge in this Petition (*Majumdar* and *Cowles*) is not cumulative of the prior art considered during prosecution. As discussed above in Section IV.C, the applicant argued that the prior art considered during prosecution (Okamoto) did not disclose the feature of "a voltage detecting device provided in said high potential part," as recited in claim 7. EX1002, 23-24. However, *Majumdar* and *Cowles* teach this feature. Therefore, *Majumdar* and *Cowles* are not cumulative of prior art considered during prosecution. Accordingly, discretionary denial under § 325(d) would be inappropriate because there is no "overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art." *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017) (precedential).

Further, discretionary denial under § 325(d) would also be inappropriate based on prior art cited for claim 7 in an IPR petition filed by Volkswagen Group of America, Inc. (IPR2022-00147, Paper 2) ("Volkswagen Petition"). Volkswagen did not cite either *Majumdar* or *Cowles* in its challenge of claim 7 of the '850 patent. Instead, Volkswagen challenged claim 7 as being anticipated by U.S. Patent Application Publication 2003/0012040 by Shoichi Orita et al. ("Orita") (EX1007). Volkswagen Petition, 14. Orita is cited in this Petition as additional background information in the analysis of limitation [7.3] to show that it was known to use the output voltage of a reverse level shifter to detect whether there is an abnormal voltage and to control a high-side transistor. *See* Section VI.A.4[7.3], *infra*. However, as detailed in the Volkswagen Petition, Orita teaches limitation [7.3] differently than the combination of *Majumdar* and *Cowles*. Orita discloses an inverter in the high potential part for detecting a voltage at the output line of a reverse level shift circuit. *See* Volkswagen Petition, 48-52. On the other hand, *Majumdar* and *Cowles* teach a buffer that is configured as a voltage detector, as discussed in the analysis of limitation [7.3.1] above. Accordingly, the ground of challenge in this Petition based on *Majumdar* and *Cowles* is not cumulative to the anticipation ground in the Volkswagen Petition based on Orita.

Accordingly, the Board should not exercise its discretion to deny institution under § 325(d).

B. The Board Should Not Exercise its Discretion Under § 314(a) to Deny Institution

The Board should not exercise its discretion to deny institution under the *General Plastic* or *Fintiv* frameworks.

1. Denial Under *General Plastic* Would be Inappropriate

As noted above in Section VII.A, Volkswagen previously filed an IPR petition against the '850 patent. The Board should not exercise its discretion to deny institution of this Petition under *General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 15-16 (PTAB Sept. 6, 2017) (Section II.B.4.i precedential) ("*General Plastic*"). None of *General Plastic* factors 1-7 weigh in favor of institution.

Under the first *General Plastic* factor, the Board considers "whether the same petitioner previously filed a petition directed to the same claims of the same patent." *Id*., 16. Petitioner has not previously filed an IPR petition or any other administrative challenge to the '850 patent. Petitioner has challenged claim 7 of the '850 patent, whereas Volkswagen has challenged claims 1, 7, 8, 10, 13, and 20 of the '850 patent. Thus, Petitioner is not challenging the same claims as Volkswagen. Therefore, *General Plastic* factor 1 weighs in favor of institution. Further, Petitioner is not related to Volkswagen and is not a co-defendant with Volkswagen. Consequently, none of the considerations set forth in *Valve* for related petitioners apply to this

proceeding. *Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11 at 9 (PTAB Apr. 2, 2019) (precedential). Petitioner is not a defendant, real party-in-interest, or privy of Volkswagen, and Petitioner is not involved in the district court litigation between Patent Owner and Volkswagen. *See* EX1009 (Jakel Declaration).

Under the second *General Plastic* factor, the Board considers "whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it." Petitioner became aware of the prior art cited in this Petition after Patent Owner began its campaign of asserting the '850 patent against numerous automobile companies in May 2021. The Volkswagen Petition was filed one month before this Petition. Petitioner did not base its challenge to claim 7 in view of prior art cited in Volkswagen's Petition. Petitioner prepared its challenge to claim 7 based on its own independent prior art search and analysis of the prior art after Patent Owner began its assertion campaign.

The third *General Plastic* factor weighs in favor of institution. This Petition was filed before Patent Owner filed any preliminary response to the Volkswagen Petition. Therefore, Petitioner did not base its challenge to claim 7 on any preliminary response or institution decision in the Volkswagen IPR. The fourth to seventh *General Plastic* factors likewise weigh in favor of institution because Petitioner filed this Petition promptly within finding the asserted prior art (*Majumdar* and *Cowles*)—prior art that is not cited in the Volkswagen Petition.

Further, Petitioner is unaware of any factor that would negatively impact the finite resources of the Board or the Board's ability to issue a final determination within one year of instituting this proceeding.

Therefore, all *General Plastic* factors weigh in favor of institution.

2. The *Fintiv* Factors Weigh in Favor of Institution

Patent Owner has asserted the '850 patent in multiple litigations ("the parallel litigations"), as noted below. According to public filings, Patent Owner has asserted the '850 patent against at least six different manufacturers in the parallel litigations: BMW, General Motors Company, Honda Motor Company, Nissan Motor Company, Ltd., Daimler AG, Volkswagen AG and related affiliates. *See* EX1017-EX1019. These litigations were filed on May 20, 2021.

Petitioner is not a defendant, real party-in-interest, or privy of any district court defendant, and Petitioner is not involved in any of the parallel litigations. *See* Jakel Declaration (EX1009). Petitioner has not communicated with any district court litigant regarding this Petition, the parallel litigations, or the '850 patent. *Id.*

Case Caption	Filed	Number	Court
Arigna Tech. Ltd. v. Bayerische Motoren Werke AG et al. ("BMW Case")	May 20, 2021 (Pending)	2:21-cv-00172	E.D. Tex.
Arigna Tech. Ltd. v. General Motors Co. et al. ("GM Case")	May 20, 2021 (Pending)	2:21-cv-00174	E.D. Tex.
Arigna Tech. Ltd. v. Daimler AG et	May 20, 2021	2:21-cv-00175	E.D. Tex.

al. ("Daimler Case")	(Pending)		

On August 24, 2021, the district court issued an order consolidating the GM Case and the Daimler Case with the lead BMW Case. EX1011, 1-2. Thus, all three of the parallel litigations have the same schedule. EX1012 (Docket Control Order in BMW Case).

In *Apple Inc. v. Fintiv, Inc.*, the Board set forth six factors guiding discretion under § 314(a) by considering efficiency, fairness, and the merits in view of an earlier trial date. IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv*"). The *Fintiv* factors weigh in favor of institution.

a. *Fintiv* factor 1 is neutral (possibility of stay)

Fintiv factor 1 weighs in favor of institution or is at least neutral. According to public information, there is no indication in any of the parallel litigations whether the district court will grant or deny a stay motion if this proceeding is instituted. No district court litigant knew of this Petition before it was filed. Jakel Declaration (EX1009). Petitioner is not in communication with any district court litigant and is not aware of its plans regarding a stay.

According to public information, Petitioner is not aware of any stay motion having been filed. Given that a stay motion has not yet been filed, the Board should not infer the outcome of that motion. *See Dish Network L.L.C. v. Broadband iTV,*

Inc., IPR2020-01359, Paper 15 at 11 (PTAB Feb. 15, 2021) ("It would be improper to speculate…what the Texas court might do regarding a motion to stay when a stay had not yet been requested). Without "specific evidence" of how the court would rule on any stay motion, this factor is neutral. *Sand Revolution II, LLC v. Cont'l Intermodal Grp.—Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative). Thus, this factor is speculative at best, neither weighing for nor against discretionary denial.

b. *Fintiv* factor 2 weighs in favor of institution or is neutral (proximity of trial date to final written decision).

Fintiv factor 2 is neutral or only slightly in favor of denial. The Board would issue a final written decision in this proceeding by approximately June 2023. While the district court has currently scheduled a trial date of July 11, 2022 in the lead BMW Case (EX1012, 1), the Board should not place too much reliance on this date because district court trials are often subject to change. *See In re Apple Inc.*, 979 F.3d 1332, 1344 n. 5 (Fed. Cir. 2020) (anticipating district court trial dates "frequently calls for speculation" because "scheduled trial dates are often subject to change."). While the Board "generally takes courts' trial schedules at face value," *Apple Inc. v Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (PTAB May 12, 2020) ("*Fintiv DI*"), the Board's reliance on district courts' scheduled trial dates to deny institution has generally been misplaced. *See* EX1020, 2-3 (study showing that

scheduled trial dates relied on to support discretionary denials overwhelmingly turned out to be incorrect). For example, the Board exercised its discretion to deny institution in *Fintiv DI* because the parallel district court proceeding (Case No. 1:21-cv-00896-ADA (W.D. Tex.)) was scheduled to go to trial on March 8, 2021, approximately two months before the Board would issue a final written decision. *Fintiv DI*, 13. However, the district court proceeding has still not gone to trial nine months after the scheduled trial date that led to discretionary denial in *Fintiv DI*. EX1021, 52. The Board should therefore not place too much emphasis on scheduled trial dates that often change.

Further, the interests of efficiency, fairness, and patent quality favor institution, even if a speculative district trial date occurred before the Board would issue a final written decision. Thus, *Fintiv* factor 2 is neutral or only slightly in favor of denial.

c. *Fintiv* factor 3 favors institution or is neutral (investment in parallel proceedings).

Fintiv factor 3 favors institution or is at least neutral. The parallel litigations are all at an early stage. There has been minimal investment to date. According to public information, the district court defendants were scheduled to serve preliminary invalidity contentions on November 10, 2021, and the parties will file a joint claim construction statement on December 3, 2021. EX1012, 5, 4. The district court

scheduled a claim construction hearing for February 16, 2022. While the parties and the district court will have made some investment in the parallel litigations, there will be much more investment after the Board issues an institution decision (by June 2022) as the parties prepare for the currently scheduled trial date (even assuming that date holds). Thus, *Fintiv* factor 3 favors institution due to the minimal investment in the parallel litigations, or is at least neutral.

d. *Fintiv* Factor 4 favors institution (overlap in issues).

According to public information, Patent Owner has asserted claim 7 in the parallel litigations. However, any degree of overlap between this proceeding and the parallel litigations is unknown because Petitioner is not a party to any of the parallel litigations and thus has no knowledge of the invalidity contentions in those proceedings. Further, Petitioner has not communicated with any of the district court defendants about their litigation strategies (EX1009), and thus has not coordinated with any district court litigant about their invalidity defenses. Should Patent Owner argue in favor of discretionary denial based on any overlap between the asserted ground in this proceeding and any district court invalidity contentions, Patent Owner should make such invalidity contentions of record to allow Petitioner and the Board to address the degree of overlap.

e. *Fintiv* factor 5 weighs in favor of institution (overlap of parties)

Fintiv factor 5 weighs heavily in favor of institution. Petitioner is not a defendant in any of the parallel litigations, and is not a real party-in-interest, or in privity with any of the district court defendants. *See Fintiv*, Paper 11 at 13-14 ("If a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution under *NHK*.").

f. *Fintiv* factor 6 favors institution (other circumstances, including merits).

Finally, *Fintiv* factor 6 strongly weighs in favor of institution. The merits of the Petition are extremely strong. *Fintiv*, Paper 11 at 14-15 ("[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record, this fact has favored institution."). The Petition demonstrates that the prior art discloses the very limitations that the examiner found to be allowable over the art considered during prosecution. *See* Section VI.A.4[7.3.1]-[7.3.2].

Further, with respect to factor 6, Patent Owner is a litigious entity and serial filer of infringement suits. In 2021, Patent Owner has brought ten (10) infringement actions against hi-tech and automobile companies in the U.S. District Court for the Western District of Texas, the U.S. District Court for the Eastern District of Texas, and the International Trade Commission—all forums with accelerated trial schedules. *See* EX1016. Since May 2021, Patent Owner has accused BMW,

General Motors Company, Honda Motor Company, Nissan Motor Company, Ltd., Daimler AG, Mercedes-Benz USA, LLC, Volkswagen AG and related affiliates of infringing the ’850 patent, and may assert the ’850 patent against other automobile companies in a staggered fashion in the future. *See* EX1017-EX1019. The Board should not deny this meritorious challenge to the ’850 patent, only to permit Patent Owner to continue to assert invalid claim 7 of the ’850 patent against the current defendants and any additional defendants Patent Owner may target in its assertion campaign. Reaching a determination as to the unpatentability of claim 7 of the ’850 patent would be in the interest of efficiency and patent quality.

Thus, the *Fintiv* factors weigh against discretionary denial.

VIII. CONCLUSION

For the reasons above, Petitioner asks that the Patent Office order an *inter partes* review trial for claim 7, and then cancel claim 7 as unpatentable.

Respectfully submitted,

December 9, 2021

/Raghav Bajaj/
Raghav Bajaj
Counsel for Petitioner
Registration No. 66,630

IX. CERTIFICATE OF WORD COUNT

Under 37 C.F.R. § 42.24, the undersigned attorney for the Petitioner, Unified Patents, LLC, declares that the argument section of this Petition (Sections II-VIII) has 11,965 words, according to the word count tool in Microsoft Word™.

/Raghav Bajaj/
Raghav Bajaj
Counsel for Petitioner
Registration No. 66,630

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Unified Patents, LLC Petitioner	§ § § § §	Petition for *Inter Partes* Review U.S. Patent No. 7,049,850

CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. §§ 42.105 and 42.6, that service was made on the Patent Owner as detailed below.

Date of service	December 9, 2021
Manner of service	Federal Express
Documents served	Petition for *Inter Partes* Review, including Exhibit List; Exhibits 1001 through 1023
Persons served	Oblon, McClelland, Maier & Neustadt, L.L.P. 1940 Duke Street Alexandria, Virginia 22314

A courtesy copy of the Petition and Exhibits 1001 through 1023 has been served on Patent Owner's litigation counsel:

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