UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., and
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner

v.

SONRAI MEMORY LTD.,

Patent Owner

U.S. PATENT NO. 7,159,766

Case IPR2022-TBD

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, "Samsung" or "Petitioner") request *inter partes* review of Claims 1, 3-6, 8, 10-14, 16, 19-21, 25-28, 39, 45, 47-50, 54-58, 60 ("Challenged Claims") of U.S. Patent No. 7,159,766 (the "'766 Patent") (Ex. 1001).

I. INTRODUCTION

The '766 Patent is directed to creating a disconnect condition under the USB standard when a USB device connected to a USB host controller becomes inactive. This disconnect, referred to in the '766 Patent as an "electrical disconnect," is created without unplugging or uncoupling the device from the host controller. Instead, an electrical state specified in the USB standard is created over the data lines between the device and the host controller that causes the host controller to make a determination that the device has been physically uncoupled from it when in fact it has not. The purported benefit of this scheme is that it results in power savings when the USB device is not active. As discussed below, however, this power-saving scheme was well-known in the prior art years before the January 20, 2004 priority date.

II. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Petitioner challenges the patentability of the Challenged Claims and requests that they be cancelled.

A. Prior Art Patents and Printed Publications

Petitioner's challenge is based on the following prior-art references:

- **Cohen (Ex. 1005) -** U.S. Patent App. Pub. No. 2002/0138776 to Cohen *et al.*, published on September 26, 2002, is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (b).
- **Maemura (Ex. 1006)** - U.S. Patent No. 6,076,119 to Maemura *et al*., issued on June 13, 2000, is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (b).
- **USB 2.0 (Ex. 1007) -** "Universal Serial Bus Specification," Revision 2.0 (2000), is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (b).
- **Tornai (Ex. 1008**) - U.S. Patent No. 5,408,668 to Tornai, issued on April 18, 1995, is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (b).
- **USB 1.0 (Ex. 1016) -** "Universal Serial Bus Specification," Revision 1.0 (1996), is prior art under at least pre-AIA 35 U.S.C. § 102(a) and (b).

B. Relief Requested

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. § 103. The specific grounds of the challenge are set forth below, and are supported by the Declaration of R. Jacob Baker Ph.D., P.E. (Ex. 1003).

Ground	Claims	Proposed Statutory Rejection
I	1, 3, 6, 8, 10-11, 13-14, 16, 21, 25-26, 28, 39, 45, 47, 50, 54-55, 57, 58	Obvious under § 103 in view of Cohen and USB 2.0
II	4-5, 19, 20, 48-49, 60	Obvious under § 103 in view of Cohen, USB 2.0, and Tornai
III	1, 6, 8, 10-14, 21, 25-27, 45, 50, 54-58	Obvious under § 103 in view of Maemura and USB 2.0 and/or USB 1.0

III. OVERVIEW OF THE TECHNOLOGY

The '766 Patent relates to the USB standard, and specifically to creating a USB disconnected state for purposes of power savings when a USB device connected to a host controller, such as a hub or peripheral device, becomes inactive. USB is a standardized, serial bus technology for connecting peripherals to computers. Ex. 1003 ¶39. The operative USB standard as of the 2004 priority date was the USB 2.0 standard, released in 2000. Ex. 1007, Cover.

A. USB Architecture and Topology

The basic architecture of USB involves the connection of devices with a host, forming a USB system. Ex. 1007, 15-16; Ex. 1003 ¶39. A host refers to the computer system that manages the USB system, and the host communicates with the devices via an interface referred to as a host controller. Ex. 1007, 6; *see also id*., 15-84, 275-96. There is only one host controller in any USB system, which may be implemented in a combination of hardware, firmware, or software. *Id*. A hub that

is integrated within the host system and attached directly to the host controller is referred to as the "root hub." Ex. 1007, 8, 16.

USB devices fall into two categories: hubs and functions. Ex. 1003 ¶40. Hubs provide attachment points to the USB bus, while functions are devices, such as a mouse or keyboard, that provide capabilities to the system. Ex. 1007, 4, 6, 17, 24. The USB topology is a pyramid, with the root hub and host at the top:

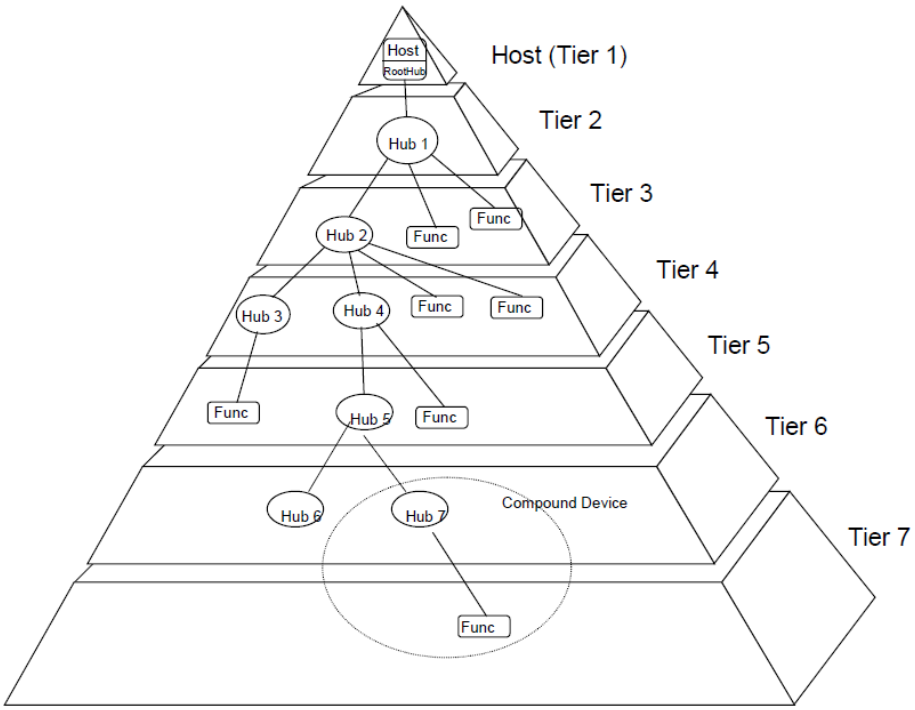


Figure 4-1. Bus Topology

Ex. 1007, 16, Fig. 4-1. All devices connect to the host via the host controller directly or indirectly. Ex. 1007, 16, 29-30; Ex. 1003 ¶40.

B. USB Cabling and Device Connections

Per the USB standard operative years before the priority date, host controllers and devices are connected using a four-wire cable or connection:

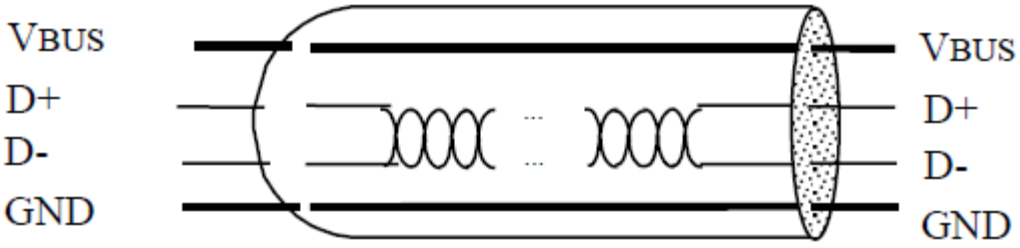


Figure 4-2. USB Cable

Ex. 1007, 17-18, Fig. 4-2. D+ and D- are a pair of differential data lines, while V_{BUS} and GND are used to deliver power to USB devices. *Id.*; Ex. 1003 ¶41.

USB 2.0 permits USB devices to operate at three speeds: low-speed, full-speed, and high-speed. Ex. 1007, 1, 12, 17; Ex. 1003 ¶42. The manner in which a USB device connects to a USB host controller (or other upstream device) depends on the speed of the device. As shown in Figures 7-20 and 7-21 from USB 2.0, reproduced below, full-speed devices are terminated with a pull-up resistor, R_{pu}, on the D+ line. Low-speed devices, on the other hand, are terminated with a pull-up resistor on the D- line. A "pull-up" resistor is a resistor connected to power that pulls the line into a high state, which USB 2.0 defines as greater than V_{IH} (min) or 2.0 volts. Ex. 1007, 141, Table 7-7. Termination refers to "[p]assive components attached at the end of cables to prevent signals from being reflected or echoed." Ex. 1007, 9.

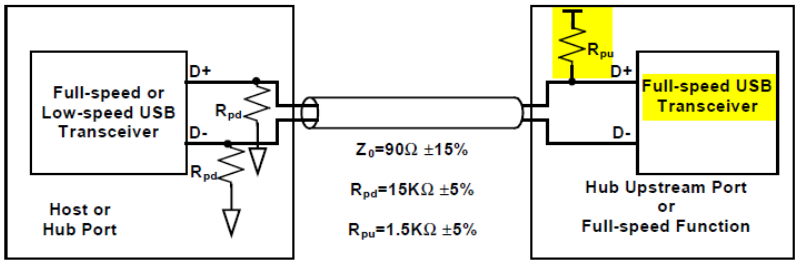


Figure 7-20. Full-speed Device Cable and Resistor Connections

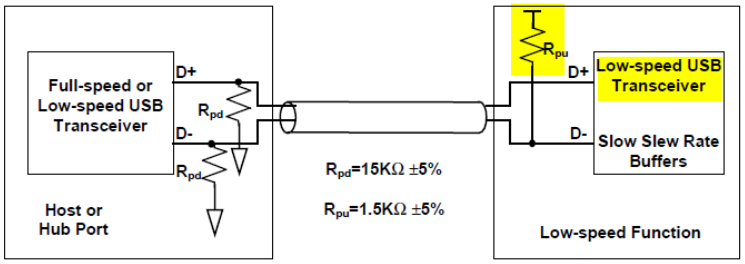


Figure 7-21. Low-speed Device Cable and Resistor Connections

Ex. 1007, Figs. 7-20, 7-21 (annotated).

A host or other upstream USB device (left side of Figures 7-20 and 7-21) will assume a device is connected to it if either D+ or D- is pulled above a threshold value for a predetermined period of time, for example 2.0 volts for 2.5 µs. Ex. 1007, 149, Tables 7-7, 7-13; Ex. 1003 ¶43. Per the USB standard, a full-speed device will pull up this high voltage on the D+ line, while a low-speed device will pull up this high voltage on the D-. Ex. 1007, 141, Figs. 7-27, 7-28; Ex. 1003 ¶43. High-speed devices initially connect as full-speed devices, but then execute a specified low-level electrical protocol to transition to high-speed signaling. Ex. 1007, 151, 154; Ex. 1003 ¶43.

Assuming a successful connection, the host controller will monitor the voltage on the D+ and D- lines. Ex. 1007, 316. Per USB 2.0, if the host controller is not sending data to the device and the voltage drops below 0.8 volts on both D+ (full-speed) and D- (low-speed)—referred to in the USB standard as a "Single-ended 0," or SE0, state—for more than 2.5 μs, a "disconnect condition is indicated." Ex. 1007, 149, Tables 7-2, 7-7, 7-13; Ex. 1003 ¶44. In this condition, the host controller will assume that the device has been disconnected by unplugging or physically removing the connection to the device. *Id*. The USB 2.0 standard in Chapter 7 explains this as follows:

> When no function is attached to the downstream facing port of a host or hub in low-/full-speed, the pull-down resistors present there will cause both D+ and D- to be pulled below the single-ended low threshold of the host or hub transceiver when that port is not being driven by the hub. This creates an SE0 state on the downstream facing port. A disconnect condition is indicated if the host or hub is not driving the data lines and an SE0 persists on a downstream facing port for more than TDDIS (see Figure 7-26). The specifications for TDDIS and TDCNN are defined in Table 7-13.

Ex. 1007, 149. Per the USB standard, the host controller handles these electrical interactions with the device on behalf of the host. *Id*., 277.

A summary of the relationship between the D+ and D- levels on a USB connector and the port configurations discussed in this section is shown below:

D+	D-	Port Configuration
Low	Low	No device connected (SE0)
High	Low	Full-Speed
Low	High	Low-Speed
High	High	Abnormal condition (SE1)

Ex. 1003 ¶45. These disconnect states are also specified in the USB 1.0 and 1.1 versions of the standard. Ex. 1016, 116; Ex. 1017, 134.

A disconnect of a high-speed device is determined "by sensing the doubling in differential signal amplitude across the D+ and D- lines that can occur when the device terminations are removed," *i.e.*, when the connecting cable is unplugged. Ex. 1007, 151; *see also id*., 121, 140-41, Tables 7-1, 7-3; Ex. 1003 ¶46.

As discussed below, the '766 Patent creates a USB disconnect condition or state without unplugging any cables or physically removing a connection by manipulating the pull-up resistor and/or tri-state buffers to create a low voltage on the D+ and/or D- lines that they are connected to, for example, by removing the resistor or setting the buffers to a very high impedance, a well-known technique known as tri-stating. Ex. 1001, 6:5-11; Ex. 1003 ¶47. This effectively creates an open line condition at the host, which electrically mimics the unplugging of the cable from the USB device, and is interpreted by the host as such per the USB standard. Ex. 1007, 121-23, 149, Tables 7-1, 7-3; *see also id*., 119-94, 309-18; Ex. 1003 ¶47.

As also discussed below, however, this electrical disconnect technique was well-known in the art before the 2004 priority date, and is disclosed in the Cohen reference, among many others.

IV. U.S. PATENT NO. 7,159,766

The ’766 Patent issued on January 9, 2007, from U.S. Application No. 10/762,767 (Ex. 1002, “the ’767 Application”), which was filed on January 20, 2004.

A. Claims

The ’766 Patent has 82 claims. Claims 1, 3-6, 8, 10-14, 16, 19-21, 25-28, 39, 45, 47-50, 54-58, 60 are challenged herein, of which six are independent.

B. Specification

The ’766 Patent purports to disclose a power-savings scheme whereby a USB device that is not active is electrically disconnected without unplugging or otherwise physically uncoupling the device from the host controller. This is done by manipulating the D+ and D- lines in order to artificially create a disconnect condition as specified in USB 2.0, which would ordinarily be created by unplugging the USB cable.

For example, Figure 3 of the ’766 Patent reproduced below shows USB host controller 211 connected to USB card reader 301 by a standard USB cable having Vbus, D+, D-, and GND lines:

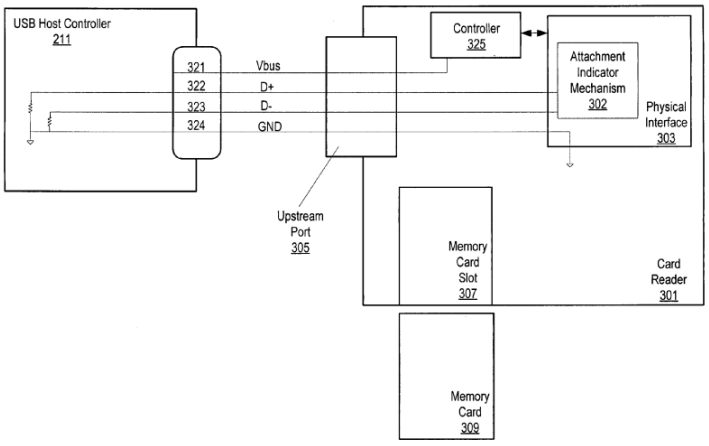


FIG. 3

Ex. 1001, Fig. 3.

As the '766 Patent explains, when memory card 309 is removed from the memory slot, the card reader becomes inactive because it is not performing any functions. According to the '766 Patent, because the card reader is now inactive, the electrical conditions on the data lines are manipulated in order create an electrical state that makes the host controller think that the card reader has been unplugged or physically disconnected when in fact it has not. The '766 Patent describes this process as follows:

> In some embodiments, if no memory card 309 is inserted in the card reader 301 (i.e., the card reader 301 is not in an active state) or the card reader 301 is turned off, an algorithm (e.g., stored in firmware on the card reader 301) may be implemented in the card reader 301 to electrically disconnect the card reader 301 from the USB host controller 211. … For full speed devices to electrically disconnect, the pull up resistor may be electrically removed (i.e., set to a high impedance or "tri-stated") from the D+ line. The USB host controller may interpret this as a disconnect. To electrically disconnect high speed

> devices, the D+ and D− lines may both be tri-stated (set to a high impedance).

Ex. 1001, 5:60-6:11.

For full-speed USB devices, the '766 Patent teaches that electrically removing the pull-up resistor from the D+ line will be interpreted by the host controller as a physical disconnect, even though the host and device remain physically attached via the USB cable. Ex. 1001, 6:16-20; Ex. 1002, 80. As Dr. Baker explains, the host controller interprets this as a physical disconnect because electrically removing the D+ resistor has the effect of driving the D+ line low, creating an SE0 state. Ex. 1003 ¶51. This is precisely the disconnect state described in Section 7.1.7.3 of the USB 2.0 standard (and in section 7.1.4.1 of USB 1.0 and section 7.1.7.1 of USB 1.1), which a host controller is required to interpret as a physical disconnect. Ex. 1007, 141. For high-speed USB devices, the '766 Patent teaches to tri-state both the D+ and D- lines. Ex. 1001, 6:20-22. As Dr. Baker explains, this has the effect of creating an open line condition on the D+ and D- lines, which is what the USB 2.0 standard specifies for a disconnect condition in high-speed devices. Ex. 1003 ¶51.

Thus, the '766 Patent is doing nothing more than creating the disconnect states specified by the USB standard without physically disconnecting the device from the host controller, which the host controller interprets as a physical disconnect as required by the USB standard, even though the host and device are still physically connected. Ex. 1003 ¶52.

This interpretation by the host controller of a physical disconnect when none has occurred is captured in the claim element "wherein the device being electrically disconnected from the host controller causes an appearance to the host controller that the device is not coupled to the host controller." The only supporting disclosure in the '766 Patent is the reference to creating a USB disconnect state on the USB cable: "For full speed devices to electrically disconnect, the pull up resistor may be electrically removed (i.e., set to a high impedance or 'tri-stated') from the D+ line. ***The USB host controller may interpret this as a disconnect***." Ex. 1001, 6:16-20. There is no other supporting disclosure in the specification, and thus this element is merely recognizing the fact that a USB host controller will interpret an SE0 state as a physical disconnect, as specified in the USB standards.

C. Summary of the Prosecution History

The application that led to the '766 Patent was filed on January 20, 2004. Ex. 1001, Cover; Ex. 1002, 201. The Applicant originally presented 59 claims. Ex. 1002, 201. Over the course of the prosecution, the Applicant amended many of the independent claims to overcome prior-art rejections. *Id*., 47-58, 148-55. These amendments included the addition of limitations that recite "wherein the device being electrically disconnected from the host controller causes an appearance to the host controller that the device is not coupled to the host controller" and "wherein a sideband signal is used to signal the device to electrically reconnect after the device

has been electrically disconnected." *Id*. On October 6, 2006, the Examiner issued the Notice of Allowance. *Id*., 20.

D. Person of Ordinary Skill in the Art

As explained in Dr. Baker's declaration, a person of skill in the art as of January 20, 2004 (the earliest effective filing date of the '766 Patent) would have had at least a Bachelor's degree in Electrical Engineering, Computer Engineering, or an equivalent technical degree, and two or more years of experience with peripheral device interconnect technologies, such as USB. Additional education would compensate for less experience, and vice-versa. Ex. 1003 ¶37.

V. CLAIM CONSTRUCTION

Claim terms "shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b) (2018); *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). Petitioner submits that the Board does not need to construe any claim term for purposes of evaluating the prior art in this Petition.[1]

[1] While there are a number of claim-construction disputes in the pending ITC investigation, those issues are directed to Patent Owner's infringement allegations, and do not need to be addressed to resolve any of the invalidity issues presented here.

VI. OVERVIEW OF THE PRIOR ART

A. Cohen

Cohen discloses a USB system in which a USB hub is connected to a host computer system. Ex. 1005, [0002], [0018], [0020]. If no devices are attached to the hub's downstream USB ports, such that the hub is inactive, then the hub is electrically disconnected from the host without physically disconnecting the hub from the host controller, just as described and claimed in the '766 Patent. *Id*., Abstract, [0005], [0020]. But even though the host controller and hub are physically connected, the host controller believes they are not. *Id*. The benefit of this disconnection scheme is that it allows the host computer to enter a low power state when the hub is inactive, conserving power. *Id*.

For example, Cohen discloses a USB system in Figure 2:

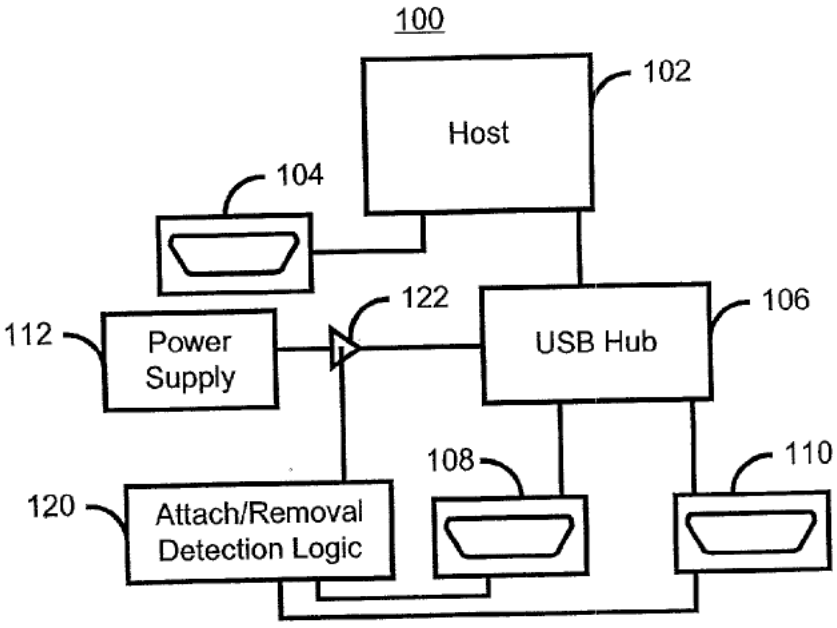
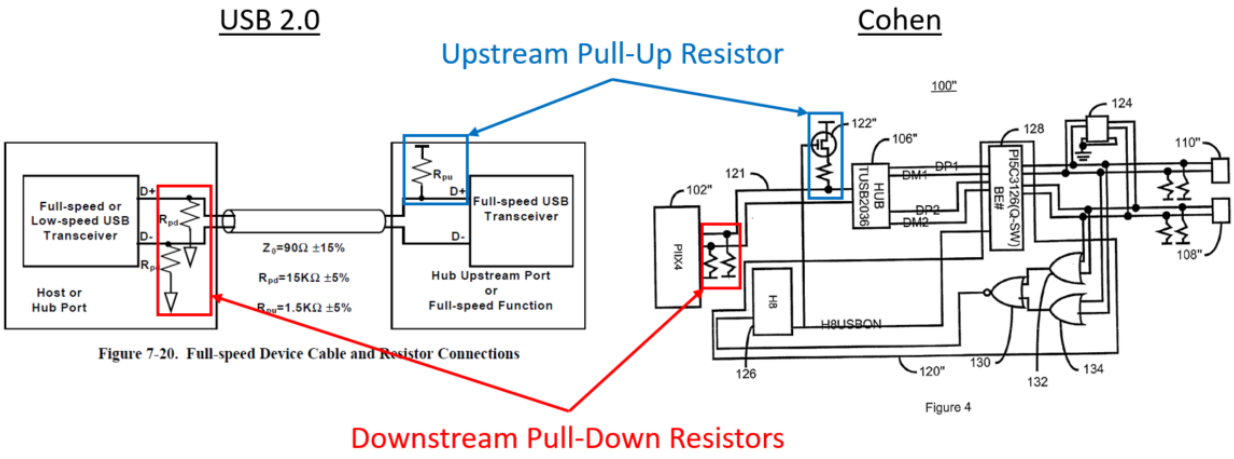


Figure 2

Ex. 1005, Fig. 2. The USB system includes host 102 connected to USB hub 106. The hub 106 includes ports 108 and 110 to which USB devices may connect. Ex. 1005, [0015]-[0016]. The hub also includes attach/removal detection logic 120, which detects when devices have been plugged into or unplugged from ports 108 and 110. *Id*. If devices have been removed from both ports, such that the hub has no function to perform and is therefore inactive, attach/removal detection logic 120 transmits a sideband signal (*i.e.*, not over the USB bus) to the hub's connector 122, which disconnects hub 106 from its power supply. *Id*. As a result, the host 102 can no longer recognize that it is connected to hub 106, even though they are still connected by a USB cable. When a device is then connected to one of the ports, and the hub becomes active, attach/removal detection logic 120 signals the hub to re-connect the USB hub to power, which is then recognized by the USB host. *Id*., [0017].

Cohen discloses a second embodiment in Figures 3 and 4, with Figure 4 providing a detailed block diagram. Ex. 1005, [0020]. This embodiment is exactly the same disconnect scheme disclosed in the '766 Patent. As shown in Figure 4, USB hub 106″ is connected to processor 102″ inside a USB host via line 121. Because this is a USB system, a POSITA would understand that line 121 includes differential D+ and D- lines, per the USB standard. Ex. 1003 ¶55. A pull-up resistor is connected to one of the data lines in the hub, while pull-down resistors are

connected to the data lines in the host. *Id.*; Ex. 1005, Fig. 4. As the following side-by-side comparison shows, this architecture is exactly the same as that shown in the USB standard for a full-speed USB device or hub connected to a host, except for the presence of FET 122″:



Ex. 1007, Fig. 7-20; Ex. 1005, Fig. 4 (annotated).

As Cohen explains, FET 122″ allows the USB hub to be electrically disconnected from the host controller:

> The connector 122" is a FET. Thus, the connector 122" is not a connector in the traditional sense of the word in that the connector 122" does not physically decouple the USB hub 106" from the processors 102". Instead, the connector 122" is a connector in the sense that it allows the USB hub 106″ to be logically coupled or decoupled from the processor 102″. When a USB device is connected to a USB connector 108″ or 110″, the attach/removal detection logic 120″ provides a signal (H8USBON) that is on. When this signal is on, the FET 122″ is turned on. Thus, the line 121 between the processors 102″ and the USB hub 106″ is driven high when a USB device is connected to one of the connectors 108″ or 110″. As a result, the USB hub 106″ is connected to the processors 102″ only when the USB connector 108″ or 110″ is in use. Thus, the processors 102″ only recognize the USB hub 106″ as a USB device when the USB connector 108″ or 110″ is

> being used. At other times, the processors 102″ behave as though the USB hub 106″ ***is not present in the computer system 100"***.

Ex. 1005, [0020]. As Dr. Baker explains, this is exactly what the '766 Patent discloses when it states that, "[f]or full speed devices to electrically disconnect, the pull up resistor may be electrically removed (*i.e.*, set to a high impedance or "tri-stated") from the D+ line," and this is nothing more than creating an SE0 electrical state that the host controller interprets as a disconnect as required by the USB specification, even though the USB cable is still connected to the hub. Ex. 1003 ¶56. Cohen also discloses the use of a sideband signal, H8USBON, which signals the hub to reconnect to the USB host. Ex. 1005, [0020].

Cohen is not the only prior-art reference to make use of an artificially created USB disconnect state such as described and claimed in the '766 Patent. This technique was used in multiple other prior-art references including Maemura discussed below, demonstrating that it was well within the knowledge of a POSITA.

B. Maemura

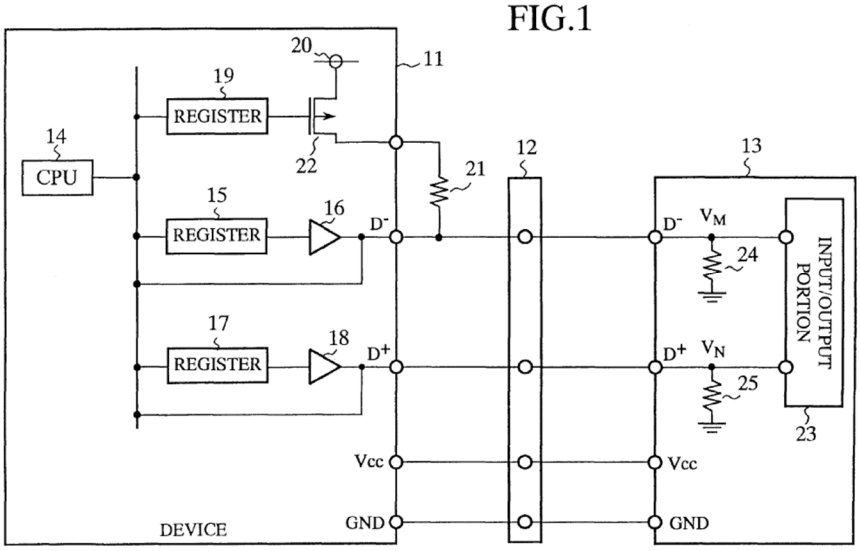
Maemura discloses a USB system wherein "inoperative" devices are electrically disconnected from the USB host controller in order to save power. Ex. 1006, Abstract. Maemura explains that, in a conventional system, "even if the [USB peripheral] device 1 is inoperative in actuality, the host computer 5 must continue a communication processing like that carried out while the device 1 is operative as long as the device 1 is physically connected." *Id*., 2:2-8. That is, even when a USB

peripheral device is not being used, its physical connection to the USB host controller causes power to be wasted by the processor of the host system.

To overcome this problem, Maemura discloses that, "when the [USB peripheral device 11 is physically connected to the host computer 13, but is actually inoperative," a switching circuit is used to disconnect the pull-up resistor on the D+ or D- line from its power source. *Id*., 5:12-18, 7:64-67. As a result, the voltage on both of the data lines falls below a threshold voltage "V_{TH2}" that the host controller uses to determine if a device has been physically disconnected (*id*., 1:51-2:2, 5:19-25, Fig. 10B), creating the "SE0" condition that is defined as a disconnect in the USB standards. Ex. 1007, 149; Ex. 1003 ¶59. Per the USB standards, this causes the host controller to perceive the USB peripheral device as having been physically disconnected from it. *Id*. This in turn permits the processor in the host computer to enter a low power state. As a result, power is saved by reducing the processing load of the processor of the host system. Ex. 1006, 5:40-50.

Maemura's Figure 1, below, depicts peripheral device 11, USB connection 12, and host computer 13:

FIG.1



Id., Fig. 1.

C. USB 2.0

USB 2.0 was published on April 27, 2000 and is prior art under §102(b). Ex. 1007, Cover; Ex. 1009 ¶¶3-5. USB 2.0 sets forth various requirements of a USB system, including the bus attributes, protocol definition, types of transactions, bus management, and programming interface required to design and build systems and peripherals that are compliant with this standard. Ex. 1007, 1.

D. USB 1.0

USB 1.0 was published on January 15, 1996 and is prior art under §102(b). Ex. 1016, Cover; Ex. 1018 ¶¶7-9. USB 1.0 is the original version of the USB standard.

E. Tornai

Tornai relates to power management in computer systems, and more specifically to removing power from inactive peripherals. Of particular relevance to certain dependent claims, Tornai discloses using a timer to make sure an inactive peripheral is truly inactive before disconnecting it from power. Ex. 1008, 3:19-35.

VII. SPECIFIC GROUNDS FOR PETITION

A. Ground I

Claims 1, 3, 6, 8, 10-11, 13-14, 16, 21, 25-26, 28, 39, 45, 47, 50, 54-55, and 57-58 are rendered obvious by Cohen, alone or in combination with the USB 2.0 standard.

A POSITA would have been motivated to combine the disclosures of Cohen with those of USB 2.0 because Cohen is specifically directed to a USB system (Ex. 1005, Abstract, [0001]-[0006]), and USB 2.0 was the operative version of the USB standard as of Cohen's 2001 filing date, and also the '766 Patent's January 2004 priority date. Ex. 1003 ¶64. Furthermore, a POSITA would have been motivated to look to USB 2.0 to better understand implementation details of the USB system described by Cohen, as it is an industry standard with which such a system would need to comply. *Id*. Moreover, a POSITA would have had a reasonable expectation of success in combining these complementary disclosures as doing so would have been well within the abilities of a POSITA and would have yielded predictable results without undue experimentation, given that Cohen discloses a USB system,

USB 2.0 discloses the requirements for such a system, and USB was a well-known and common standardized interconnect technology at the time. *Id*.

1. Claim 1

a) 1[pre]: "A system, comprising:"

To the extent a limitation, Cohen discloses this preamble, as it discloses various examples of a USB "computer ***system***" in Figures 1 through 4. Ex. 1005, [0007]-[0009], [0015], [0018], [0020], Figs. 2-4; Ex. 1003 ¶66.

b) 1[a]: "a processor"

Cohen discloses a USB host that includes at least one processor: "A conventional computer system may include a host, a USB hub and multiple USB connectors integrated into a single unit. The host typically includes one or more integrated circuits, ***including at least one processor***, that run an operating system ("OS") for the conventional computer system." Ex. 1005, [0012]. Cohen also discloses processors in the embodiments of Figures 2-4. *Id*., [0017], [0019], [0020]; Ex. 1003 ¶67.

c) 1[b]: "a host controller coupled to the processor"

Cohen renders this element obvious in view of USB 2.0. First, Cohen discloses a USB system, and a POSITA would understand and find obvious that Cohen's USB system contains a host controller. Ex. 1003 ¶¶68-69. For example, USB 2.0 explains that a USB system is ***required*** to have a host and a host controller, where the host is "[t]he host computer system where the USB Host Controller is

installed. This includes the host hardware platform (CPU, bus, etc.) and the operating system in use[,]" and the host controller is "[t]he host's USB interface." Ex. 1007, 6; *see also id*., 15-84, 275-96. USB 2.0 further explains that "[t]here is only one host in any USB system. The USB interface to the host computer system is referred to as the Host Controller." *Id*., 16.

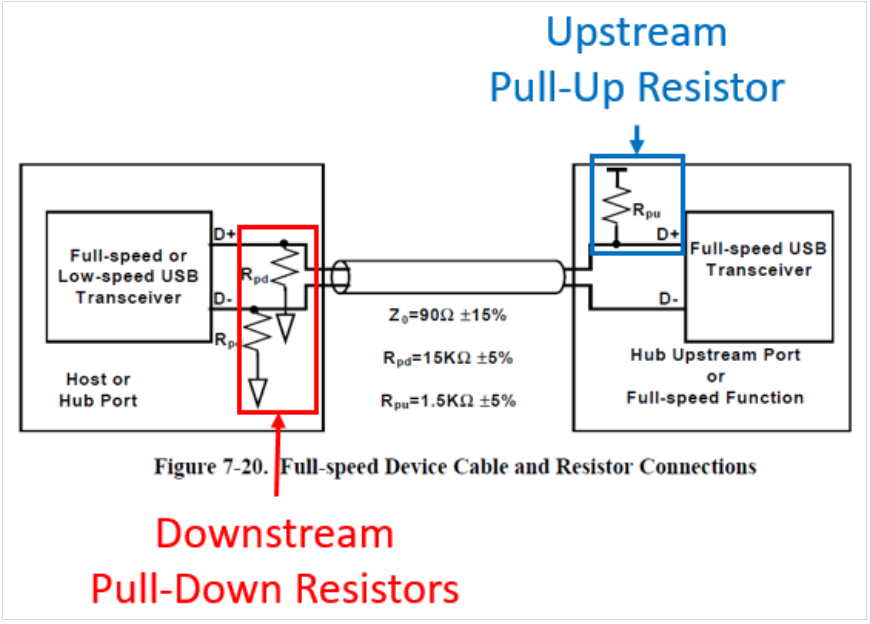
Second, a POSITA would understand that the host controller in Cohen is coupled to the processor in the host computer, where the term "coupled" is defined in the '766 Patent as directly or indirectly connected (Ex. 1001, 4:14-15), since the host controller is the interface to the host computer, and the host computer is controlled by its processor(s). Ex. 1003 ¶¶70-71. Indeed, the entire purpose of Cohen is to control power to the processor(s) in the host computer by disconnecting inactive USB devices, and this information must be reported to the processor through the USB host controller. A POSITA would thus understand and find obvious that there is at least an indirect connection between the host controller and the processor(s) in the host computer. Ex. 1003 ¶¶70-71.

d) 1[c]: "a device coupled to the host controller"

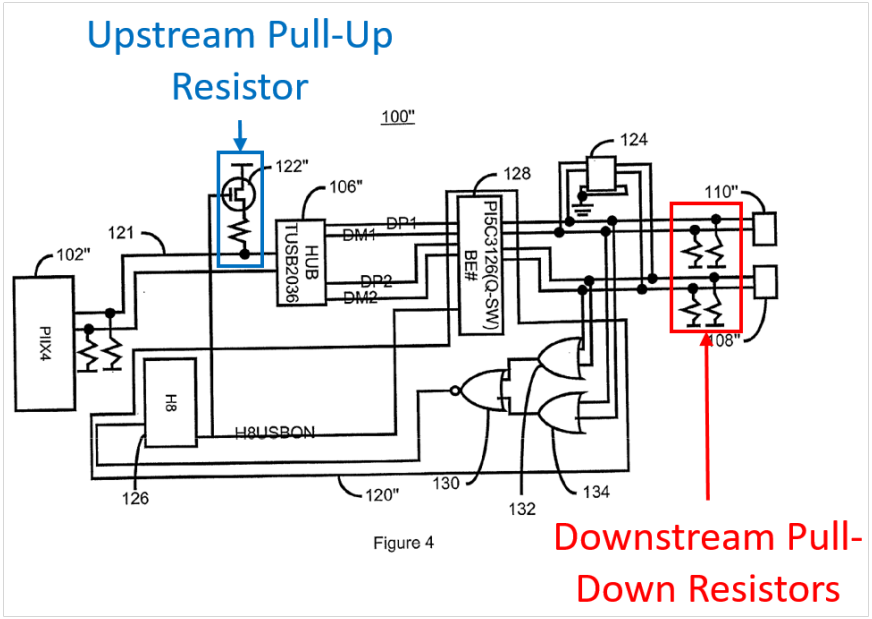
Cohen discloses this element or renders it obvious in view of USB 2.0. Ex. 1003 ¶72. First, Cohen discloses a device in the form of a USB hub connected to a host computer, as shown in Figures 2 (hub 106 connected to host 102), 3 (hub 106′ connected to host 102′), and 4 (hub 106″ connected to host processor 102″). Ex.

1005, [0007]-[0009], [0015], [0018], [0020], Figs. 2-4. And as explained with respect to element 1[b], a POSITA would understand and find obvious that the USB hub is coupled to a host controller because, per USB 2.0, "[t]he USB host interacts with USB devices through the Host Controller." Ex. 1007, 24; *see also, e.g.*, *id*., 15-84, 275-96, Figs. 4-1, 5-1, 5-5, 5-7.

Additionally, while Cohen refers to elements 106, 106', and 106" as "the USB hub," a POSITA would recognize that other elements disclosed by Cohen are part of the same device as the hub. As Dr. Baker explains, USB 2.0 requires that hubs have both upstream and downstream ports. Ex. 1003 ¶73; Ex. 1007, 22-23, 297. While the upstream ports are not labeled with an element number in Cohen, a POSITA would recognize USB connectors 108, 110, 108', 110', 108″, and 110″ as the hub's downstream ports. *Id*.; Ex. 1005, [0016], [0018], [0020], Figs. 2-4. Additionally, Dr. Baker explains that USB 2.0 requires that hubs include pull-down resistors on the downstream ports and a pull-up resistor on the upstream port. Ex. 1003 ¶74; Ex. 1007, 123, 141, Figs. 7-20, 7-21. These resistors can be seen in Figure 7-20 from USB 2.0 and Cohen's Figure 4, both of which are annotated below:



Ex. 1007, Figs. 7-20 (annotated).



Ex. 1005, Fig. 4 (annotated). A POSITA would thus understand that all of these elements are part of the same device as the hub. Ex. 1003 ¶74. Dr. Baker further explains that, based on the circuit diagram in Figure 4, a POSITA would have also

have recognized that connector 122″ to be part of the hub device because it is in between the pull-up resistor and the port through which the resistor connects to power. *Id*.

Additionally, to the extent Complainant argues that the upstream ports, downstream ports, pull-up and pull-down resistors, or connecters 122, 122′, and 122″ are located outside of the hub, that argument is incorrect and beside the point. As Dr. Baker explains, a POSITA would find it obvious that all of these elements can be included in the hub device. Ex. 1003 ¶75. Indeed, there are only two possible locations for this circuitry, inside the hub or outside the hub. And as Dr. Baker explains, it would have been obvious to include these elements inside the hub device because it would simplify the implementation and allow all of the necessary connections to be made to a single device, rather than require multiple components to be assembled and connected. *Id*. Such an implementation would also have been well within the skill of a POSITA, who would have had a reasonable expectation of success implementing such a design with undue experimentation given that it is merely a routine issue of packaging known components. *Id*.

e) 1[d]: "wherein the device is electrically disconnected from the host controller if the device is not in an active state"

Cohen discloses this element or renders it obvious in view of USB 2.0. Ex. 1003 ¶¶76-80. For example, Cohen's embodiment of Figures 3 and 4 utilizes ***the very same method of electrical disconnection described in the '766 Patent*** by

creating an SE0 state as specified in USB 2.0—electrically removing the pull-up resistor from the D+ line. *See* Ex. 1001, 6:5-9. As Dr. Baker explains, in this embodiment, when no USB devices are connected to ports 108″ and 110″ of hub 106″ via USB line 121, the hub is inactive because it is not performing any functions (the hub serves an attachment point for other USB devices and is inactive when no devices are connected; this is an example of inactivity provided in the '766 specification). Ex. 1003 ¶77. Attach/removal detection logic 120″ causes FET 122″ to disconnect the attached pull-up resistor from power, resulting in the hub 106″ being electrically disconnected from the host controller. *Id*. On the other hand, when a device is connected to one of the ports of hub 106″, the hub is performing its connection function, and the resistor is connected to power and pulled high, connecting the hub to the host controller. *Id*. Cohen explains as follows:

> When a USB device is connected to a USB connector 108″ or 110″, the attach/removal detection logic 120″ provides a signal (H8USBON) that is on. When this signal is on, the FET 122″ is turned on. Thus, the line 121 between the processors 102″ and the USB hub 106″ is driven high when a USB device is connected to one of the connectors 108″ or 110″. As a result, the USB hub 106″ is connected to the processors 102″ only when the USB connector 108″ or 110″ is in use. Thus, the processors 102″ only recognize the USB hub 106″ as a USB device when the USB connector 108″ or 110″ is being used. At other times, the processors 102″ behave as though the USB hub 106″ is not present in the computer system 100″.

Ex. 1005, [0020]; *see also id*., [0018]-[0019]. Because Cohen's device is a USB hub and is disconnected by creating an SE0 state, a POSITA would understand that it is

a full-speed USB device with the pull-up resistor connected to the D+ line, because USB hubs cannot be low-speed which would have the pull-up resistor connected to D-. Ex. 1007, 139, 141, 297, 318, Figs. 7-20, 7-21; Ex. 1003 ¶ 108.

As Dr. Baker explains, this constitutes an electrical disconnection in USB because the hub and host controller cannot communicate over the bus given that the host controller does not know the hub is there, even though they remain physically connected. Ex. 1003 ¶78. As Dr. Baker further explains, this is simply a consequence of the disconnect states defined in Section 7.1.7.3 of USB 2.0, and is precisely what happens in the USB embodiments disclosed in the '766 Patent. *Id*. By electrically removing the pull-up resistor from the D+ line, such that it no longer drives the data line to a high voltage, the host controller is unable to recognize the attached device, and this is deemed an electrical disconnection by the '766 Patent. This embodiment is essentially identical to an embodiment disclosed in the '766 Patent where a hub is "not in an active state" if no devices are attached to it. *See, e.g.*, Ex. 1001, 2:60-65, 7:46-61, 9:7-36, Fig. 8, claims 3, 16, 47.

Similarly, in connection with its Figure 2 embodiment, Cohen discloses that hub 106 will be electrically disconnected from the host controller when no devices are attached to hub ports 108 and 110, *i.e.*, when hub 106 is inactive. Ex. 1005, [0016]-[0017]; Ex. 1003 ¶80.

f) 1[e]: "wherein the device being electrically disconnected from the host controller causes an appearance to the host controller that the device is not

coupled to the host controller"

Cohen discloses this element or renders it obvious in view of USB 2.0. As Dr. Baker explains, both Cohen and the '766 Patent artificially create a USB disconnect state defined in Section 7.1.7.3 of USB 2.0 by manipulating the state of the interface between the USB device—a hub in the case of Cohen—and the host controller to create an electrical state that the host controller interprets as the device being physically unplugged, but ***without physically uncoupling*** them from each other. Ex. 1003 ¶¶81-82. This appearance of physical de-coupling is not an inventive feature of the '766 Patent, but merely the consequence of electrically creating a USB disconnect state. In other words, as Dr. Baker explains, a USB host controller by definition interprets a disconnect state as a physical de-coupling, because that is what the USB standard requires of it. *Id*., ¶44; Ex. 1007, 149. This is confirmed by Cohen itself, which explains that in a USB disconnected state, the hub is considered not to be present in the system, even though it remains physically attached to the host: "Thus, the processors 102″ only recognize the USB hub 106″ as a USB device when the USB connector 108″ or 110″ is being used. ***At other times, the processors 102" behave as though the USB hub 106" is not present*** in the computer system 100″." Ex. 1005, [0020]; *see also id*., [0016]-[0017] (discussing hub being unrecognized in Figure 2 embodiment). Indeed, the only support in the

'766 specification for this element is the references to the USB disconnect states. Ex. 1001, 5:39-56, 6:5-11.

g) 1[f]: "wherein a sideband signal is used to signal the device to electrically reconnect after the device has been electrically disconnected"

This element is disclosed or rendered obvious by Cohen. Cohen discloses a signal from the attach/removal detection logic—element 120, 120, or 120″, depending on the embodiment—which causes the hub to electrically reconnect to the host controller when a USB device is connected to either of the USB hub's downstream facing ports. Ex. 1005, [0016], [0018], [0020], Figs. 2-4. This signal is referred to as an H8USBON signal. As Cohen explains, this signal is used to connect Cohen's hub to the host when a device is plugged into one of its ports:

> When a USB device is connected to a USB connector 108″ or 110″, the attach/removal detection logic 120″ provides a signal (H8USBON) that is on. When this signal is on, the FET 122″ is turned on. Thus, the line 121 between the processors 102″ and the USB hub 106″ is driven high when a USB device is connected to one of the connectors 108″ or 110″. As a result, the USB hub 106″ is connected to the processors 102″ only when the USB connector 108″ or 110″ is in use."

Ex. 1005, [0020]; *see also id*., [0016]-[0019]. By driving the data line to a high voltage, Cohen's hub electrically reconnects to the host controller. A POSITA would also understand and find obvious based on this disclosure that a device could be connected to one of the downstream ports of Cohen's hub after the hub had been electrically disconnected, thus causing it to reconnect. Ex. 1003 ¶83. The output from the attach/removal detection logic signals Cohen's hub because it causes the

hub to electrically reconnect by causing it to raise the voltage on the D+ line via the pull-up resistor in the Figure 3 and 4 embodiment, or causes the hub to re-connect to power in the Figure 2 embodiment. As discussed in Section VII.A.1.d) above, connectors 122, 122′, and 122″ that receive this signal are part of the same device as the hub. It is also obvious to a POSITA to include them in the same device, for the reasons discussed in Section VII.A.1.d).

Further, as Dr. Baker explains, in all of the embodiments, the signal from the attach/removal detection logic is a "sideband signal" because it is transmitted over an electrical pathway that is separate from the USB connection between the host controller and the USB hub. Ex. 1003 ¶86; Ex. 1005, Figs. 2-4. This can be seen in Figure 4 of Cohen, where H8USBON is transmitted over a connection other than the USB connection 121 between the hub and host. *Id*.

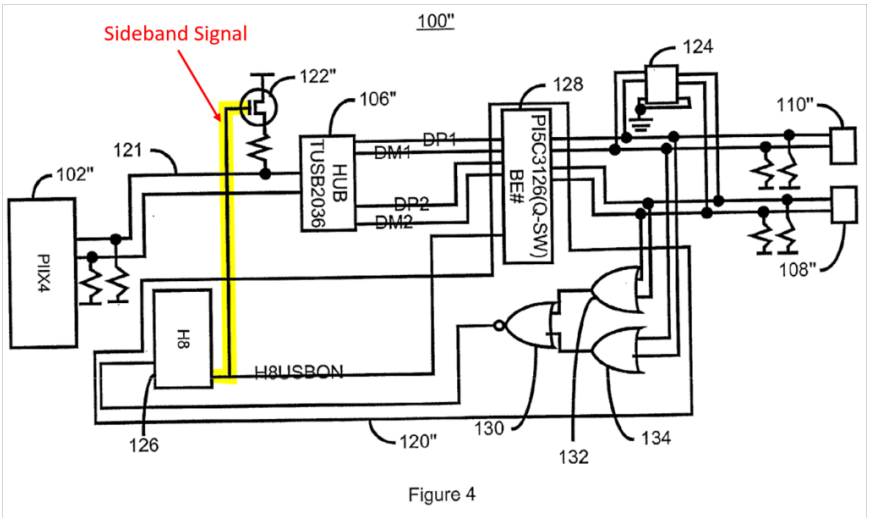


Figure 4

Ex. 1005, Fig. 4 (annotated).

2. Claim 3: "The system of claim 1, wherein the device is a hub and the active state comprises a second device attached to the hub"

Claim 1 is obvious as discussed above and Cohen further discloses this element. As explained with regard to elements 1[c] and 1[d], Cohen discloses a USB hub that is "in an active state" when a device is attached to one of its downstream ports. Ex. 1005, Abstract, [0001], [0005], [0008]-[0010], [0012]-[0013], [0015]-[0020], Figs. 2-4; Ex. 1003 ¶101.

3. Claim 6: "The system of claim 1, wherein when the device is electrically disconnected from the host controller, the device does not cause bus activity"

Claim 1 is obvious as discussed above. Cohen further discloses this element or renders it obvious in view of USB 2.0. As explained with regard to elements 1[d] and 1[e], when Cohen's hub is electrically disconnected from the host controller, it does not cause bus activity because it is "logically decoupled" from and not recognized by the host, in which state it cannot communicate over the USB bus. Ex. 1005, Abstract, [0005], [0013], [0016]-[0020]; Ex. 1003 ¶102.

4. Claim 8: "The system of claim 1, wherein if the processor is in a low power state, the processor exits the low power state if an electrical disconnect is discontinued"

Claim 1 is obvious as discussed above. Cohen further discloses this element or renders it obvious in view of USB 2.0. Ex. 1003 ¶¶103-106. As Cohen describes and teaches, when a device is connected to one of Cohen's hub ports, the processor cannot be in a low power state. As discussed above, Cohen discloses discontinuing

an electrical connection by connecting the pull-up resistor on the data lines to connect to the pull-up power supply, electrically connecting the hub to the host controller. Ex. 1005, [0020]. From the perspective of the host controller, this is equivalent to connecting Cohen's hub to a USB port on the host computer, and would cause the processor in the host computer to exit a low power state. Ex. 1003 ¶¶104. Indeed, Cohen explains that "the processors 102" only recognize the USB hub 106" as a USB device when the USB connector 108" or 110" is being used." Ex. 1005, [0020]. A POSITA would understand that the processors in Cohen's system must exit the low power state in order to recognize the USB hub, and that when devices are plugged into Cohen's hub, the processor will not maintain a low power state. Ex. 1003 ¶105.

In addition, a POSITA would have recognized that, pursuant to USB 2.0, the connection of a device to a USB port may generate "a resume signal" that causes the processor in a host system to exit a low power state. Ex. 1007, 156, 280, 282; Ex. 1003 ¶106. As Dr. Baker describes, it would have been obvious to a POSITA to use such a resume signal with Cohen, because enabling device initiated wake-up signaling provides added convenience for users of USB systems. *Id*. A POSITA would have had reasonable success in implementing a resume signal with Cohen because this was a well-understood functionality common in USB systems and with which a POSITA would have been familiar. *Id*.; Ex. 1007, 156, 308.

5. Claim 10: "The system of claim 1, wherein the host controller provides a peripheral bus interface for the device"

Claim 1 is obvious as discussed above. Also as discussed with regard to element 1[b], a USB host controller is an interface to the host, and Cohen's hub connects to the host through the host controller via the USB bus. Ex. 1003 ¶107; Ex. 1007, 16; *see also id*., 15-84, 275-96.

6. Claim 11: "The system of claim 1, wherein electrically disconnecting the device comprises electrically removing a pull up resistor from a D+ line"

Claim 1 is obvious as discussed above. Cohen further discloses this element or renders it obvious in view of USB 2.0. Cohen discloses the use of FET 122" to electrically remove the pull-up resistor shown in Figure 4 from the D+ line. Ex. 1005, [0020], Fig. 4; Ex. 1003 ¶108. This is done by removing the connection between the resistor and power, which has the effect of rendering the resistor electrically disconnected, because it has no electrical influence on the D+ line. To the extent Patent Owner contends that Cohen does not explicitly refer to a D+ line, a POSITA would have found it obvious in view of USB 2.0. Ex. 1003 ¶108. Cable 121 is a USB cable (*see* Ex. 1005, [0012], [0020]) and, as discussed in the background section above, a POSITA would understand that a USB cable includes a D+ line. Ex. 1007, 17-18, Fig. 4-2. Further, in USB 2.0 (as in earlier versions), the upstream port of a hub ***must*** include a pull-up resistor on the D+ line, and not on the D- line. *Id*., 139, 141, 297, 318, Figs. 7-20, 7-21; Ex. 1003 ¶108.

7. Claim 13: "The system of claim 1, wherein the device being electrically disconnected from the host controller allows the processor to enter a low power state or remain in a low power state"

Claim 1 is obvious as discussed above. Cohen further discloses this element or renders it obvious: "At other times, the processors 102″ behave as though the USB hub 106″ is not present in the computer system 100″. Therefore, the processors 102″ can enter a lowest power state when the USB connectors 108″ and 110″ are not in use." Ex. 1005, [0020]; *see also id*., [0003], [0017], [0019]. Furthermore, as Dr. Baker explains, allowing the processor to enter or remain in a low power state is not a separate inventive element or step described in the '766 Patent specification. Ex. 1003 ¶109. Rather, it is simply a consequence of causing an appearance to the host controller that the device is no longer coupled, as claimed in the independent claim. *See* Ex. 1001, 2:36-42.

8. Claim 14

a) 14[pre]: "A method:"

As discussed with regard to claim 1, Cohen discloses a system and method for electrically disconnecting and reconnecting a USB hub to a USB host based on whether there are any devices attached to the host. *See, e.g.*, Ex. 1005, Title, Abstract, [0001], [0005]-[0006]; Ex. 1003 ¶87.

b) 14[a]: "detecting whether a device coupled to a host controller is in an

active state"

Cohen discloses detecting whether the USB hub device—which, as explained with respect to element 1[c], is coupled to a host controller—is an active state by determining whether there are any USB devices attached to its downstream ports. Ex. 1005, [0005]; *see also id*., Abstract, [0013], [0016], [0018], [0020], Figs. 2-4; Ex. 1001, 9:7-36, Fig. 8, claims 3, 16, 47; Ex. 1003 ¶88.

c) 14[b]: "if the device is not in an active state, electrically disconnecting the device from a host controller, wherein electrically disconnecting the device from the host controller causes an appearance to the host controller that the device is not coupled to the host controller"

See element 1[d] above.

d) 14[c]: "wherein electrically disconnecting the device from the host controller causes an appearance to the host controller that the device is not coupled to the host controller"

See element 1[e] above.

e) 14[d]: "if the device is in an active state, maintaining an electrical connection between the device and the host controller"

Cohen discloses that, if a device is attached to one of the USB hub's downstream ports, *i.e.*, the hub is in an active state, then the electrical connection between the hub and host controller will be maintained, *i.e.*, there will be no electrical disconnection. Ex. 1005, [0017]; *see also id*., Abstract, [0005], [0013], [0016], [0018]-[0020]. As explained with respect to element 1[c], a POSITA would recognize and find obvious that Cohen's hub is coupled to the host through a USB host controller. Ex. 1003 ¶¶72, 91.

f) 14[e]: "electrically reconnecting the device using a sideband signal after the device has been electrically disconnected"

See element 1[f] above.

9. Claim 16: "The method of claim 14, wherein the device is a hub, and the active state comprises a second device coupled to the hub"

See claim 3.

10. Claim 21: "The method of claim 14, wherein if no devices are coupled to the host controller the host controller does not create bus activity"

Claim 14 is obvious as discussed above. In addition, a POSITA would have found the additional element of claim 21 obvious because, if there are no devices coupled to the host controller, there are no devices with which the host controller can communicate over the bus. Ex. 1003 ¶110.

11. Claim 25: "The method of claim 14, wherein the host controller provides a peripheral bus interface for the device"

See claim 10.

12. Claim 26: "The method of claim 14, wherein electrically disconnecting the device comprises electrically removing a pull up resistor from a D+ line"

See claim 11.

13. Claim 28

Claim 28 is obvious over Cohen and USB 2.0. Ex. 1003 ¶¶93-95. Claim 28 is very similar to claim 1, and the analysis of claim 1 is incorporated herein by reference. Claim 28 specifically requires device detect logic and auto detach logic,

which are disclosed by Cohen in the form of attach/removal detection logic. Ex. 1005, Abstract, [0005], [0013], [0015]-[0020], Figs. 2-4. Cohen also discloses the additional hub requirement, as explained with regard to claim 3. *Id*.; *see also id*., [0001], [0008]-[0010], [0012].

14. Claim 39

Claim 39 is obvious. Ex. 1003 ¶96. Claim 39 is a method claim that tracks claim 14, except that it specifies the device as a hub, the active state as a device being connected to the hub, and the inactive state as no device connected to the hub. These elements are all disclosed by Cohen. Ex. 1005, Abstract, [0001], [0005], [0008]-[0010], [0012]-[0013], [0015]-[0020], Figs. 2-4.

15. Claim 45

Claim 45 is a "computer accessible memory medium" claim whose elements are mirrored in method claim 14, and is obvious for the same reasons claim 14 is obvious. Ex. 1003 ¶97. In addition, to the extent the preamble is limiting, it would have been obvious to a POSITA that Cohen's invention could be implemented using processor executable program instructions stored in a computer accessible memory medium—which the '766 Patent broadly defines to include many different types of memory mediums and combinations of those mediums. Ex. 1001, 10:13-46. As Dr. Baker explains, it would have been obvious to a POSITA that the attach/removal detection logic could be implemented in processor executable program instructions,

for example firmware on Cohen's integrated circuits 126 and 128, which would be stored in a computer accessible memory medium. Ex. 1005, [0020]. Such processor executable implementations were common, well-known, and well within the capabilities of a POSITA. Ex. 1003 ¶¶98-99. Furthermore, such implementations had benefits in the form of simplicity and reconfigurability, as changes could be implemented without removing or replacing hardware. *Id*.

16. Claim 47: "The memory medium of claim 45, wherein the device is a hub, and the active state comprises a second device coupled to the hub"

See claim 3.

17. Claim 50: "The memory medium of claim 45, wherein if no devices are coupled to the host controller the host controller does not create bus activity"

See claim 21.

18. Claim 54: "The memory medium of claim 45, wherein the host controller provides a peripheral bus interface for the device"

See claim 10.

19. Claim 55: "The memory medium of claim 45, wherein electrically disconnecting the device comprises electrically removing a pull up resistor from a D+ line"

See claim 11.

20. Claims 57 and 58

Claim 57 is the same as claim 1, minus the "causes an appearance" limitation, and dependent claim 58 includes that additional limitation. Both claims are obvious for the same reasons as claim 1. Ex. 1003 ¶¶ 100, 111.

B. Ground 2

Claims 4-5, 19, 20, 48-49, and 60 are rendered obvious by Cohen in combination with the USB 2.0 standard and Tornai.

1. Claims 5, 20, and 49

Claim 5, 20, and 49 are all invalid as obvious over Cohen, USB 2.0, and Tornai. Ex. 1003 ¶¶117-119. These claims depend from claims 1, 14 and 45, respectively, which are obvious for the reasons explained in Ground 1. These claims all recite the additional element "wherein if the device is not in an active state, the device is electrically disconnected after a wait period, wherein if the device becomes active during the wait period, the device is not electrically disconnected." This element is obvious in view of Tornai.

Like Cohen, Tornai relates to power management in computer systems, and more specifically to removing power from an inactive peripheral device "when it is not needed in order to minimize the power consumed by the peripheral." Ex. 1008, Abstract. Tornai discloses the common-sense notion of using a timer to make sure an inactive peripheral is truly inactive before disconnecting it from power. As Tornai explains:

> [P]rocessor 14 continues to process the various input signals received on input port 12 to determine whether any of the peripherals are no longer needed, and thus, should be deactivated. ***If processor 14 determines that a particular peripheral is no longer being used, it starts a timer having a selected time limit***. After starting the timer, processor 14 monitors the input signals for input signal activity, and if signal activity is detected, the timer is reset and the peripheral remains on. However, ***if no input signal activity is detected before the expiration of the time limit, processor 14 generates and sends a deactivation signal to the connection circuit 16 to cause the circuit 16 to disconnect the appropriate peripheral from the power source***. Hence, the apparatus 10 automatically and efficiently deactivates idle peripherals to prevent the unnecessary consumption of energy.

Ex. 1008, 3:19-35; *see also id*, Abstract, 2:22-39.

As Dr. Baker explains, a POSITA would be motivated to combine this teaching from Tornai with Cohen, as they disclose complementary methods of accomplishing the same goal. Ex. 1003 ¶¶113. First, a POSITA would have found it obvious to utilize the timers described by Tornai to ensure that Cohen's hub is actually inactive (*i.e.*, that a user has not removed the devices from the downstream ports and immediately replaced them with other devices) before it is electrically disconnected, so that the hub does not need to be unnecessarily re-enumerated (*i.e.*, identified and allocated resources by the host controller) seconds after it has been disconnected. *Id*., ¶114.

Second, while Cohen describes a solution to the problem of power that is wasted when no devices are coupled to a hub, a POSITA would have recognized that just as much, if not more, power is wasted when completely inactive devices are

coupled to the hub. Ex. 1003 ¶115. A POSITA would have recognized that electrically disconnecting a hub from the host controller when there are no devices attached to its downstream ports ***and*** when devices attached to the downstream ports are inactive would enable the processor in the host to enter its lowest power state more often, which is Cohen's stated goal, saving even more power than Cohen's solution alone. *Id*.; Ex. 1005, [0003]-[0006]. In addition, a POSITA would have recognized the benefits of Tornai's timer feature, which prevents the disconnection of devices that are not actually inactive, minimizing disruptions to the system and the user. Ex. 1003 ¶113.

Further, a POSITA would have had a reasonable expectation of success in combining these complementary disclosures as doing so would have been well within the abilities of a POSITA—the trivial implementation of a timer—and would have yielded predictable results without undue experimentation. *Id*., ¶116. As Dr. Baker explains, all of the necessary hardware is already provided by Cohen as the USB standard requires that hubs implement timers on their downstream facing ports, and Cohen's design includes circuitry to monitor the activity on the downstream data lines. *Id*. (citing Ex. 1007, 316; Ex. 1005, Fig. 4). A POSITA would only need to modify some programming to start the timers when the downstream data lines are in an idle state or disconnected (SE0) state, which would have been well within the capabilities of a POSITA. *Id*.

2. Claim 60

Claim 60 depends from claim 57, which was shown to be obvious above. Claim 60 adds a limitation that requires "wherein the device is not in an active state if the device has not been used in a specified amount of time." This element is obvious for the same reasons as Claims 5, 20, and 49. Ex. 1003 ¶¶120-121.

3. Claims 4, 19, and 48

Claims 4, 19, 48, and 60 are all invalid as obvious over Cohen, USB 2.0, and Tornai. Ex. 1003 ¶122. These claims depend from claims 1, 14 and 45, respectively, which are obvious for the reasons explained in Ground 1. These claims are similar to claim 60, and all require "wherein the device is not in an active state if the device has not been used in a second specified amount of time." In the parallel ITC investigation, Sonrai has taken the position that use of the word "second" in this limitation is a typographical error, because there is no "first" period of time specified in these claims or the claims from which they depend. Under this view, these claims are invalid as obvious for the same reasons as claim 60.

C. Ground 3

Claims 1, 6, 8, 10-14, 21, 25-27, 45, 50, and 54-58 are rendered obvious by Maemura in view of USB 2.0 and/or USB 1.0.

A POSITA would have found been motivated to combine the disclosures of Maemura with those of USB 2.0 and/or USB 1.0 because Maemura states explicitly that its invention operates "according to the USB (Universal Serial Bus Specification

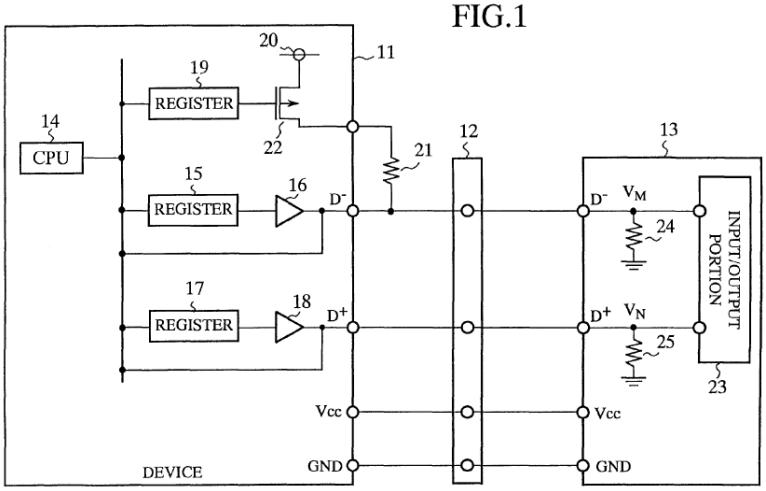
Revision 1.0, Jan. 15, 1996) standard." Ex. 1006, 1:5-11. Thus, a POSITA would have been motivated to look to USB 1.0 to better understand certain implementation details of the USB system described by Maemura. Ex. 1003 ¶124. Because USB 2.0 was the operative version of the USB standard as of the '766 Patent's January 2004 priority date, and because there are no differences between USB 1.0 and USB 2.0 that are material to the disclosures in Maemura, a POSITA would also have looked to the disclosures of USB 2.0 for the same reasons. *Id*. Moreover, a POSITA would have had a reasonable expectation of success in combining these complementary disclosures as doing so would have been well within the abilities of a POSITA and would have yielded predictable results without undue experimentation, given that Maemura discloses a USB system, USB 2.0 and USB 1.0 disclose the requirements for such a system, and USB was a well-known and common standardized interconnect technology at the time. *Id*.

1. Claim 1

a) 1[pre]

To the extent a limitation, Maemura discloses a system comprised of a USB peripheral device such as "a mouse, a keyboard, a data tablet, or a game pad" coupled to a host computer via USB connection. Ex. 1006, 3:48-54; *see also id*., 4:25-28; Ex. 1003 ¶¶125-126. One embodiment is depicted in Figure 1, below, with peripheral device 11, USB connection 12, and host computer 13:

FIG.1



Id., Fig. 1; *see also, e.g.*, *id*., Figs. 3-4, 6-7.

b) 1[a]

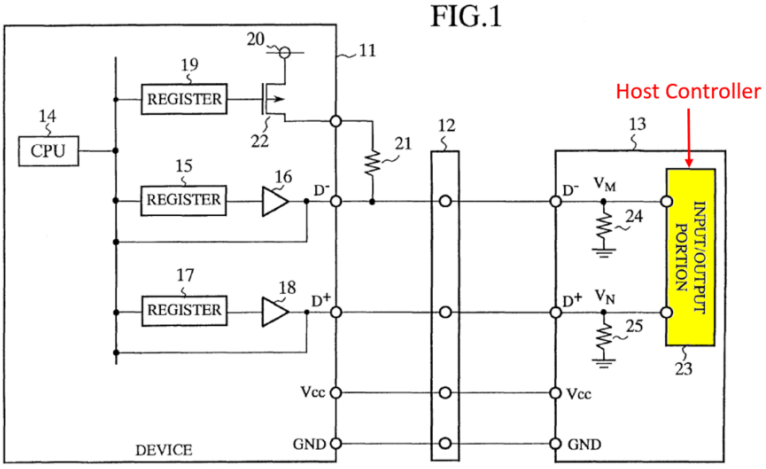
Maemura discloses that the host computer of its system includes a "CPU," which is a processor. Ex. 1006, 4:33-36; *see also id*., 1:34-50. Indeed, because Maemura's host computer is described as "a personal computer or the like" (*id*., 3:48-54; *see also id*., 1:14-27), a POSITA would have recognized that it necessarily includes a processor. Ex. 1003 ¶127.

c) 1[b]

Maemura and USB 2.0 and/or USB 1.0 render this element obvious. First, Maemura discloses a USB system, and a POSITA would understand and find obvious that a USB system must contain a host controller, as required by both USB 1.0 and USB 2.0. Ex. 1003 ¶129. For example, both USB 1.0 and USB 2.0 explain that a USB system is required to have a host and a host controller, where the host is "The host computer system where the USB Host Controller is installed. This

includes the host hardware platform (CPU, bus, etc.) and the operating system in use[,]" and the host controller is "[t]he host's USB interface." Ex. 1007, 6; *see also id*., 15-84, 275-96; Ex. 1016, 16, 27-28. Maemura specifically describes that the host computer of its USB system includes "an input/output portion of the host computer 13 for receiving and transmitting data…." Ex. 1006, 4:16-22. As Dr. Baker explains, a POSITA would understand and find obvious that Maemura's input/output portion 23, shown in Figure 1, is a host controller. Ex. 1003 ¶129.

FIG.1



Ex. 1006, Fig. 1 (annotated); *see also id*., Figs. 3-4, 6-7.

Second, a POSITA would understand that the host controller in Maemura is coupled to the processor in the host computer, where the term "coupled" is defined in the '766 Patent as directly or indirectly connected. Ex. 1001, 4:14-15. Maemura describes that the input/output portion of its host computer is coupled to the CPU of the host computer, as Maemura describes that the CPU "analyzes the contents of the data" received via the input/output portion. Ex. 1006, 4:29-36. The input/output

portion and CPU must be coupled in order for data to move between the two. Ex. 1003 ¶130.

d) 1[c]

Maemura discloses a device coupled to the host controller. In particular, Maemura describes that a USB peripheral device such as "a mouse, a keyboard, a data tablet, or a game pad" is connected to the input/output portion of the host computer "through the signal lines D- and D+." Ex. 1006, 3:48-54, 4:16-22; *see also id*., 4:25-36. Further, a POSITA would understand and find obvious that all devices in a USB system must be coupled to the host controller. Ex. 1007, 24; *see also, e.g.*, *id*., 15-84, 275-96, Figs. 4-1, 5-1, 5-5, 5-7; Ex. 1003 ¶¶131-132.

e) 1[d]

Maemura discloses that the device is electrically disconnected from the host controller if the device is not in an active state. Maemura describes that, when the USB peripheral device—in Maemura's primary embodiments a low-speed USB device—is "inoperative," *i.e.*, not in an active state because it is not performing any functions, a pull-up resistor on the data lines is disconnected from pull-up power supply, electrically disconnecting the USB peripheral device from the host controller:

> [W]hen the device 11 is physically connected to the host computer 13, but is actually inoperative, the CPU 14 stores the H level signal into the register 19. This brings the gate 22 into nonconducting state, thereby

> disconnecting the pullup resistor 21 from the pullup power supply 20. Thus, the potential V_M of the signal line D- is not pulled up.

Ex. 1006, 5:12-25; *see also id*., Abstract, 2:23-35, 2:50-63, 4:1-15, 5:40-43. As a result, the voltage on both of the data lines falls below a threshold voltage "VTH2" that the host controller uses to determine if a device has been physically disconnected (*id*., 1:51-2:2, 5:19-25, Fig. 10B), creating the "SE0" condition that is defined as a disconnect in the USB standards. Ex. 1007, 149; Ex. 1003 ¶¶133-134. This is exactly the same method of electrical disconnection described in the '766 Patent. *See* Ex. 1001, 6:5-9. And, as Dr. Baker explains, this constitutes an electrical disconnection in USB because, as a consequence of the disconnect states defined in Section 7.1.7.3 of USB 2.0 and Section 7.1.4.1 of USB 1.0, there is no way for the USB peripheral device and the host controller to communicate over the USB bus, even though they remain physically connected. Ex. 1003 ¶133.

f) 1[e]

Maemura discloses this element or renders it obvious in view of USB 2.0. and/or USB 1.0. As explained with respect to element 1[d], Maemura describes "electrically disconnecting" from the host controller the same way that is described in the '766 Patent, by artificially generating a USB "disconnect condition," as defined in Section 7.1.7.3 of USB 2.0 and Section 7.1.4.1 of USB 1.0, ***without physically uncoupling*** the peripheral device from the host controller. Ex. 1006, 5:12-25; Ex. 1003 ¶136. And as Dr. Baker explains, this causes an appearance to

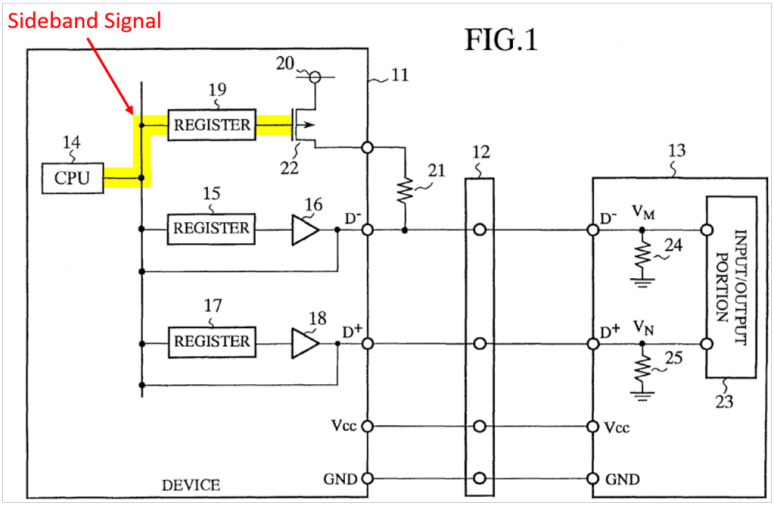
the host controller that the peripheral device is no longer coupled to the host controller for the same reason described by the '766 Patent—because, per the USB standard, USB host controllers interpret a "disconnect condition" as a physical disconnection. Ex. 1003 ¶136; Ex. 1001, 6:5-9. In other words, this appearance of physical de-coupling is not an inventive feature of the '766 Patent, but merely the consequence of creating an electrical state that corresponds to the disconnect condition defined in the USB standard. Ex. 1003 ¶136; Ex. 1007, 149; Ex. 1016, 116. Indeed, Maemura confirms that a USB host determines whether a USB device "is physically connected or not" based on the voltage levels of the D+ and D- lines. Ex. 1006, 1:52-2:2, Figs 10A-B.

g) 1[f]

This element is disclosed by Maemura in the form of an L signal received by register 19 from the USB peripheral device's CPU when the USB device is in an operative mode. Maemura explains that this signal causes the gate connecting the pull-up resistor on the data lines to connect to the pull-up power supply, electrically connecting the USB peripheral device to the host controller. Ex. 1006, 4:1-15, 4:44-54; *see also id*., Abstract, 2:23-35, 2:50-63, 5:40-43. A POSITA would understand and find it obvious that the USB peripheral device of Maemura's system is placed in an "operative" mode and connected to the host controller when it is needed, and placed into an "inoperative" mode and disconnected when it is not, such that the

device could be placed in an "operative" mode and electrically reconnected to the host controller after it had been electrically disconnected, and *vice versa*. Ex. 1003 ¶¶137-138.

Further, as Dr. Baker explains, and as shown in Figure 1 of Maemura, the signal received from the USB peripheral device's CPU and stored in register 14 is a sideband signal because it is transmitted over a connection other than the USB connection between the peripheral device and host. *Id.*, 139.



Ex. 1006, Fig. 1 (annotated).

1. Claim 6

Claim 1 is obvious as discussed above. Maemura further discloses this element. Because Maemura's USB peripheral device is electrically disconnected from the host when it is inoperative, it does not transmit information on the USB bus when in that state. Ex. 1003 ¶149. Indeed, Maemura explains that "when the device 11 is inoperative, since no data is input to the device 11, … the potential V_M of the

signal line D- and the potential V_N of the signal line D+ become zero[.]" Ex. 1006, 5:19-25.

2. Claim 8

Claim 1 is obvious as discussed above. Maemura further discloses this element or renders it obvious in view of USB 2.0 and/or USB 1.0. As discussed above, Maemura discloses discontinuing an electrical connection by connecting the pull-up resistor on the data lines to connect to the pull-up power supply, electrically connecting the USB peripheral device to the host controller. Ex. 1006, Abstract, 2:23-35, 2:50-63, 4:1-15, 4:44-54, 5:40-43. From the perspective of the host controller, this is equivalent to connecting Maemura's USB peripheral device to a USB port on the host computer, and would cause the processor in the host computer to exit a low power state. Ex. 1003 ¶151. Indeed, as Dr. Baker explains, causing the processor to exit a low power state is not described anywhere in the '766 Patent specification. *Id*. Rather, a POSITA would understand and find obvious that this is simply a consequence of connecting a device to a USB port, which is how the host controller interprets electrically reconnecting a device that has been electrically disconnected. *Id*.

In addition, a POSITA would have recognized that, pursuant to USB 1.0 and USB 2.0, the connection of a device to a USB port may generate "a resume signal" that causes the processor in a host system to exit a low power state. Ex. 1007, 156,

280, 282; Ex. 1016, 120-21, 200; Ex. 1003 ¶152. As Dr. Baker describes, it would have been obvious to a POSITA to use such a resume signal with Maemura, because enabling device initiated wake-up signaling provides added convenience for users of USB systems. Ex. 1003 ¶152. A POSITA would have had reasonable success in implementing a resume signal with Maemura because this was a well understood functionality common in USB systems and with which a POSITA would have been familiar. *Id*.; Ex. 1007, 156, 308.

3. Claim 10

Claim 1 is obvious as discussed above. Also as discussed above, Maemura's host controller—"input/output portion of the host computer 13"—provides a peripheral bus interface through which the USB peripheral device is connected to the host computer. Ex. 1006, 3:48-54, 4:16-22; *see also id*., 4:25-36; Ex. 1003 ¶153.

4. Claim 11

Claim 1 is obvious as discussed above. Maemura further discloses this element or renders it obvious in view of USB 2.0 and/or USB 1.0. As discussed above, Maemura discloses electrically disconnecting the inoperative USB peripheral device from the host controller by electrically removing a pull-up resistor from the data lines, *i.e.*, by removing the connection between the resistor and a power source such that it no longer drives the data line to a high voltage. Ex. 1006, Abstract, 2:23-35, 2:50-63, 4:1-15, 5:12-18, 5:40-43. And as Dr. Baker explains, disconnecting the

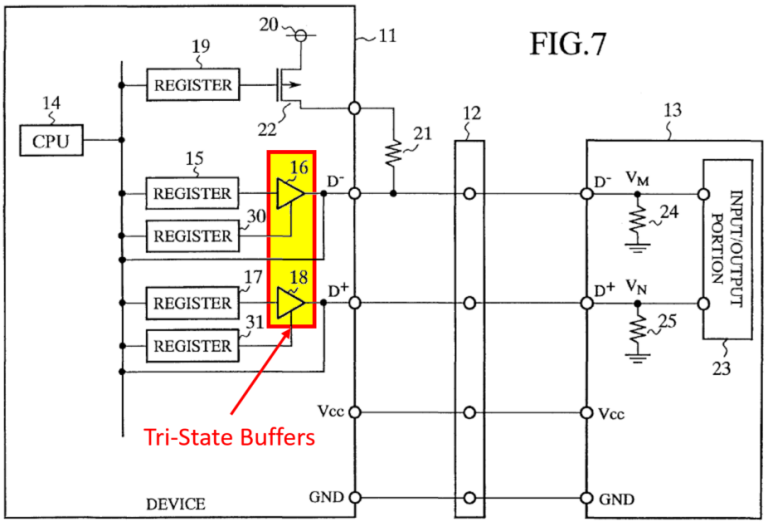
resistor from its power source is equivalent, from an electrical perspective, to removing it altogether. Ex. 1003 ¶154.

Maemura further describes that the pull-up resistor may be on, and electrically removed from, the D+ line. Ex. 1006, 7:64-67. This would also have been obvious to a POSITA, who would have understood that, pursuant to USB 2.0 and USB 1.0, the pull-up resistor must be on the D+ line if the USB peripheral device is a "full-speed device." Ex. 1003 ¶154; Ex. 1007, 141; Ex. 1016, 114.

5. Claim 12: "The system of claim 1, wherein electrically disconnecting the device comprises tri-stating a D+ line and a D− line"

Claim 1 is obvious as discussed above. In addition, Maemura discloses this element or renders it obvious in view of USB 2.0 and/or USB 1.0. Ex. 1003 ¶155. Maemura discloses tri-stating both the D+ and D- lines when electrically disconnecting the inoperative USB peripheral device. Maemura describes "a tri-state buffer connected to the signal line" that is set to "a high-impedance state" when the device is in an inoperative mode. Ex. 1006, 2:45-49. Maemura further explains that, "[t]o switch the device 11 into the inoperative mode, the CPU 14 sets the L level signal in the registers 30 and 31 so that the buffers 16 and 18 are placed at the high-impedance states as shown in FIG. 8. This will prevent a current that flows to the ground through the buffer 16 or 18 even when the device 11 is inoperative in the foregoing embodiments, thereby further reducing the consumed current." Ex. 1006,

8:9-23, Fig. 8. As shown in Figure 7 below, Maemura's tri-state buffers are connected to the D+ and D- lines:



Ex. 1006, Fig. 7 (annotated).

6. Claim 13

Claim 1 is obvious as discussed above. Maemura further discloses this element or renders it obvious in view of USB 2.0 and/or USB 1.0. In particular, Maemura discloses that "when the device 11 is inoperative, the host computer 13 need not carry out the communication processing with the device 11, which presents an advantage of reducing the processing load of the host computer 13." Ex. 1006, 5:47-50; *see also id*., Abstract, 1:65-8, 7:41-55. A POSITA would have understood that the reduced processing load enables the processor to enter or remain in a low power state. Ex. 1003 ¶156. Indeed, as Dr. Baker explains, allowing the processor to enter or remain in a low power state is not a separate inventive element or step described in the '766 Patent specification. *Id*. Rather, it is simply a consequence of

causing an appearance to the host controller that the device is no longer coupled, as claimed in the independent claim. *See* Ex. 1001, 2:36-42.

7. Claim 14

a) 14[pre]

As discussed with regard to claim 1, Maemura discloses a system and method for electrically disconnecting a USB peripheral device from a USB host controller when the device is inoperative, and reconnecting the device when it is operative. Ex. 1003 ¶140.

b) 14[a]

As explained with regard to elements 1[d] and 1[f], Maemura discloses detecting whether the USB peripheral device that is connected to the host controller is in an "operative" mode, *i.e.*, whether it is an active state. Ex. 1006, 4:1-15; Ex. 1003 ¶141.

c) 14[b]

See element 1[d] above.

d) 14[c]

See element 1[e] above.

e) 14[d]

Maemura discloses maintaining an electrical connection between the device and the host controller if the device is in an active state. Specifically, Maemura describes that, when the USB peripheral device is "operative"—*i.e.*, in an active

state—the pull-up resistor on the data lines remains connected to the pull-up power supply and, thus, the USB peripheral device remains electrically connected to the host controller. Ex. 1006, 2:23-35, 4:1-15, 4:44-54, 5:40-43; Ex. 1003 ¶144.

f) 14[e]

See element 1[f] above.

8. Claim 21

Claim 14 is obvious as discussed above. In addition, a POSITA would have found the additional element of claim 21 obvious because, if there are no devices coupled to the host controller, there are no devices with which the host controller can communicate over the bus. Ex. 1003 ¶157.

9. Claim 25

See claim 10.

10. Claim 26

See claim 11.

11. Claim 27

See claim 12.

12. Claim 45

Claim 45 is a "computer accessible memory medium" claim whose elements are mirrored in method claim 14, and is obvious for the same reasons claim 14 is obvious. In addition, to the extent the preamble is limiting, it would have been obvious to a POSITA that Maemura's invention could be implemented using

processor executable program instructions stored in a computer accessible memory medium—which the '766 Patent broadly defines to include many different types of memory mediums and combinations of those mediums. Ex. 1001, 10:13-46. Indeed, Maemura describes that the process of electrically disconnecting and reconnecting the USB peripheral device is implemented by the CPU—or processor—of the USB peripheral device, which determines whether the USB peripheral device is "operative" or "inoperative" and sets the value of register 19 accordingly. Ex. 1006, 4:1-15, 4:44-49, 5:12-18. A POSITA would have understood that such a processor would operate based on executable program instructions stored in a computer accessible memory medium. Ex. 1003 ¶147.

13. Claim 50

See claim 21.

14. Claim 54

See claim 10.

15. Claim 55

See claim 11.

16. Claim 56

See claim 12.

17. Claims 57 and 58

Claim 57 is the same as claim 1, minus the "causes an appearance" limitation, and dependent claim 58 includes that additional limitation. Both claims are obvious for the same reasons as claim 1. Ex. 1003 ¶¶148, 158.

VIII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any evidence of secondary considerations that would support a finding of non-obviousness. *See Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1311–12 (Fed. Cir. 2006); Ex. 1003 ¶159. The asserted prior art demonstrates there is no evidence of failure by others and that the features recited in the Challenged Claims were readily available in the prior art. Even if secondary considerations did exist (and they do not), they cannot overcome the strong prima facie case of obviousness shown in this Petition. *See Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010). While in the parallel ITC investigation Patent Owner contended a confidential discovery response that there are secondary considerations that are relevant to the analysis here, Patent Owner has failed to show the requisite nexus between any alleged secondary consideration and the allegedly novel aspects of the claimed subject matter of the Challenged Claims, and none exist. *See In re Huai-Hung Kao*, 639 F.3d 1057, 1068 (Fed. Cir. 2011) (secondary considerations must have a nexus to "what is both claimed and ***novel*** in the claim") (emphasis in original).

Should Patent Owner attempt to meet its burden to show secondary considerations, Petitioner reserves the right to respond.

IX. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. Institution Is Appropriate Under 35 U.S.C. §325(d)

The *Advanced Bionics* and *Becton, Dickinson* factors weigh in favor of institution under 35 U.S.C. §325(d). *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, Case IPR2019-01469, Paper 6 (P.T.A.B. Feb. 13, 2020); *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017).

First, there are significant and material differences between the prior art and arguments asserted in this Petition and the prior art and arguments previously presented to the Patent Office. In the first instance, Maemura, Tornai, USB 2.0, and USB 1.0 were not "made of record by the Examiner" nor were they provided by the applicant in an information disclosure statement. Ex. 1002; *Advanced Bionics*, Paper 6 at 7-9. In addition, while the patent that issued from the Cohen application (US 6,928,562) was made of record by the Examiner, it was only considered as part of three-reference combinations with US 6,460,143 ("Howard") and US 2004/0027879 ("Chang") or US 2003/0167345 ("Knight"), and then only for the limitations of certain claims that required a "hub." Ex. 1002, 169-71. The Examiner never evaluated or considered Cohen's disclosures with respect to the "electrically

disconnect," "causes an appearance…," or "sideband signal" limitations of the independent claims. *See* Ex. 1002. Further, Petitioner is not relying upon Cohen by itself, but in combination with other references not considered by the Examiner. "Petitioner need not explain how the Examiner erred in consideration of the references at issue, because the Examiner did not consider the combinations of the references asserted in the Petition at all, let alone for the challenged claims." *Bowtech, Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5 (P.T.A.B. Aug. 6, 2019).

Second, the Examiner relied on non-analogous arguments and disclosures during the original prosecution. For instance, and as the Applicant noted during prosecution, for the "electrically disconnect" limitations, the Examiner relied on disclosure from Howard that pertained to shutting down a USB bus, rather than electrically disconnecting a USB device from a host controller when the device is not in an active state. Ex 1002, 169-170. Cohen and Maemura, however, do not concern shutting off a USB bus. Likewise, with respect to the "causes an appearance …" limitations, the Examiner relied on disclosure from US 6,405,362, ("Shih") that pertained to "changing of appearance on the host system by not displaying the icons." *Id*., 153. By contrast, the grounds presented above rely on the disconnect states from USB 2.0 and USB 1.0, which were not considered by the Examiner. Thus, not only was the art considered by the Examiner different, the arguments in

this Petition are also materially different than the arguments presented during prosecution. *Bowtech,* Paper 14 at 14.

B. Institution Is Appropriate Under *Fintiv*

Evaluation of the six factors under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) favors institution.

Most fundamentally, as demonstrated in Section VII, the Petition presents overwhelming arguments for unpatentability of the Challenged Claims based on exactly the same features and functionality described in the specification of the '766 Patent. *Samsung Elecs. Co., Ltd. v. Dynamics, Inc.*, No. IPR2020-00504, 2020 WL 6050685, at *14 (P.T.A.B. Oct. 13, 2020) (finding the "merits of the case weigh in favor" of institution). Thus, institution is consistent with the significant public interest against "leaving bad patents enforceable." *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

The need for this IPR is further bolstered by the fact that the ITC cannot invalidate a patent. *Samsung Elecs. Co., Ltd. v. BitMicro, LLC*, IPR2018-01410, Paper 14 at 18 (P.T.A.B. Jan. 23, 2019) (the ITC applies "differen[t]…evidentiary standards and burdens" and "does not have the authority to invalidate a patent"); *Tech. Gen. Corp. v. Genentech, Inc.*, 80 F.3d 1553, 1564 (Fed. Cir. 1996) (the ITC cannot "set aside a patent as being invalid [and/or] render it unenforceable"). Thus, the ITC proceeding will not resolve the validity of the Challenged Claims. Indeed,

even if the ITC invalidated the '766 Patent's claims, there is nothing preventing Sonrai from pursuing its claims in the district court.

In addition, this Petition challenges the validity of claims that are not at issue in the ITC investigation—claims 12, 20, 21, 27, 28, 39, 50, and 56—two of which are independent claims. Ex. 1010; Ex. 1012. "[T]he ITC proceeding will not resolve the parties' dispute concerning patentability of [these] claims …, which recite different and additional elements than the claims in the ITC proceeding." *Dynamics* 2020 WL 6050685, at *3 (finding "the non-overlapping claims were sufficient to weigh in favor of institution"). For instance, there are no claims at issue in the ITC investigation that recite or otherwise implicate "a device detect logic" or "an auto detach logic coupled to the hub," as recited in independent claim 28. Nor are there any claims at issue in the ITC that recite or otherwise implicate "tri-stating a D+ line and a D− line," as recited in claims 12, 27, and 56. Ex. 1012.

To further avoid overlap, Petitioner also stipulates that, if this IPR is instituted, it will not pursue the same primary references or grounds presented in this Petition in the ITC. Ex. 1019. Thus, there will not be any overlap between this Petition and potential invalidity grounds in the co-pending investigation, weighing in favor of institution. *MED-EL Elektromedizinische Geräte Ges.m.b.h. v. Advanced Bionics AG*, IPR2021-00044, 2021 WL 1287684, at *13 (P.T.A.B. Apr. 6, 2021) (finding that factor four "weighs against exercising discretion to deny" where "the Board and

the Delaware District Court would consider the disclosures of [] different asserted prior art references in the context of certain overlapping claims").

Furthermore, although the target February 7, 2023 completion date of the ITC Investigation will likely pre-date the Board's final written decision, the target date is not set in stone and could easily change. Indeed, the ALJ has expressly warned that the ITC schedule is not fixed or guaranteed, and is "subject to change because of restrictions and uncertainty due to the COVID-19 pandemic" (Ex. 1014, 2; Ex. 1015, 2). Thus, it is certainly possible that the ultimate completion of the investigation will occur closer to and possibly after the Board's final written decision (per typical Commission extensions). The district court proceedings are stayed, and any final determination there will post-date the Board's final written decision.

Finally, the ITC investigation is in its early stages and thus the Commission and parties have not yet invested substantial resources. Ex. 1013, 2. While activity in the investigation will subsequently increase at a pace typical of ITC actions, Samsung's diligence in filing this Petition—mere weeks after submitting its invalidity contentions (Ex. 1010; Ex. 1011)—weighs against discretionary denial. *See Philip Morris Prods., S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 at 10 (P.T.A.B. Nov. 16, 2020); *Fintiv*, Paper 11 at 11. Concluding otherwise would mean that this factor would always weigh against institution when

there is a parallel ITC investigation because such investigations always require a rapid investment of resources at the outset.

Accordingly, based on a "holistic view of whether efficiency and integrity of the system are best served," the facts here weigh against exercising discretion under § 314(a) to deny institution. *Dynamics*, Paper No. 11 at 15.

X. MANDATORY NOTICES

A. Real Party-In-Interest

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. are the real parties-in-interest.

B. Related Matters

The '766 Patent is the subject of an active ITC investigation, *Certain Laptops, Desktops, Servers, Mobile Phones, Tablets, And Components Thereof*, Inv. No. 337-TA-1280, as well as multiple parallel proceedings in the Western District of Texas, *Sonrai Memory Limited v. Amazon.com, Inc.*, 6:21-cv-00787 (W.D.Tex.); *Sonrai Memory Limited v. Dell Technologies, Inc. et al.*, 6:21-cv-00788 (W.D.Tex.); *Sonrai Memory Limited v. Lenovo Group Ltd. et al.*, 6:21-cv-00790 (W.D.Tex.); *Sonrai Memory Limited v. LG Electronics Inc. et al.*, 6:21-cv-00791 (W.D.Tex.); *Sonrai Memory Limited v. Motorola Mobility LLC*, 6:21-cv-00792 (W.D.Tex.); and *Sonrai Memory Limited v. Samsung Electronics Co., Ltd. et al.*, 6:21-cv-00793 (W.D.Tex.), all of which have been stayed pending the outcome of the ITC investigation. These actions may affect, or be affected by, decisions in this proceeding. Nothing herein

should be taken as an endorsement of Sonrai's positions in the co-pending litigations.

C. Counsel Information

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D. Service Information

Samsung concurrently submits a Power of Attorney, 37 C.F.R. § 42.10(b), and consents to electronic service directed to the following email address: Samsung_Sonrai_IPR@kirkland.com.

XI. PAYMENT OF FEES

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. § 42.15(a)(1) any additional fees that may be due in connection with this Petition to

Deposit Account No. 506092, including the fees required for the 11 excess claims above twenty 20 that are challenged in this Petition.

XII. CERTIFICATION

Petitioner certifies, pursuant to Rule 42.104(a), that the '766 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR of the Challenged Claims on the grounds identified in this Petition. Petitioner certifies: (1) Petitioner is not the owner of the '766 Patent; (2) Petitioner (or any real party-in-interest) has not filed a civil action challenging the validity of any claim of the '766 Patent; (3) this Petition is being filed within one year of service of a complaint against Petitioner asserting the '766 Patent; (4) estoppel provisions of 35 U.S.C. §315(e)(1) do not prohibit this IPR; and (5) this Petition is filed after the '766 Patent was granted.

XIII. CONCLUSION

Petitioner requests institution of an IPR and cancellation of the Challenged Claims.

Date: December 10, 2021

Respectfully submitted,

/s/ James E. Marina, P.C.

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CERTIFICATE OF COMPLIANCE

This Petition complies with the type-volume limitations as mandated in 37 C.F.R. § 42.24, totaling 13,903 words. Counsel has relied upon the word count feature provided by Microsoft Word.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing document with accompanying Exhibits 1001 – 1020 as listed in Petitioner's Exhibit List on page ix of this document, was served on December 10, 2021, via overnight delivery, upon agreement under 37 CFR §42.105, directed to the attorney/agent of record for the patent as identified on USPTO PAIR at the following address:

Meyertons, Hood, Kivlin, Kowert & Goetzel
P.O. Box 398
Austin TX 78767

A courtesy copy was also served by electronic mail on the Patent Owner's designated lead counsel for service for the related matter: *In the Matter of Certain Laptop, Desktop, Servers, Mobile Phones, Tablets, and Components Thereof,* Inv. No. 337-TA-1280

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