UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KIOXIA AMERICA, INC and KIOXIA CORPORATION,

Petitioners,

v.

BiTMICRO LLC,

Patent Owner.

Case No.: IPR2023-00741
U.S. Patent No. 9,135,190

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,135,190

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Challenged Claims of U.S. Patent No. 9,135,190

Claim element	Claim 1
[Claim 1Pre]	A method of performing transactions on a set of memory locations that includes a first memory location and a second memory location, the method comprising:
[Claim 1a]	performing a memory transaction comprising addressing a first memory location in a first memory device in a memory store,
[Claim 1b]	said first memory location and a second memory location respectively associated with a first device profile and a second device profile,
[Claim 1c]	wherein said second memory location is in a second memory device in the memory store,
[Claim 1d]	wherein a memory read transaction or a memory write transaction is performed on at least one of the first memory location or second memory location,
[Claim 1e]	wherein data is transferred to the first memory location or second memory location from a host for a memory write transaction, wherein data is transferred from the first memory location or second memory location to the host for a memory read transaction;
[Claim 1f]	wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 1g]	said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
[Claim 1h]	said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first

	and second device profiles;
[Claim 1i]	after identifying the command details, obtaining the first set of attributes;
[Claim 1j]	wherein each attribute in the first set of attributes and second set of attributes is associated with a respective attribute qualifier that qualifies a respective memory location;
[Claim 1k]	wherein the memory store is directly coupled to at least one memory bus and wherein the at least one memory bus is directly coupled to a controller, and wherein the controller performs the memory read transaction and memory write transaction on the memory store;
[Claim 1l]	wherein the host is directly coupled to the controller by a communication path as the controller performs the memory read transaction or memory write transaction;
[Claim 1m]	wherein the first device profile and second device profile are each stored in the memory store;
[Claim 1n]	and using attributes from said first and second device profiles; and
[Claim 1o]	selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.
Claim element	**Claim 5**
[Claim 5]	The method of claim 1, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
Claim element	**Claim 6**
[Claim 6]	The method of claim 5, wherein said different attribute qualifiers include different attribute values.
Claim element	**Claim 29**
[Claim 29Pre]	A non-transitory computer readable medium comprising computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location, said method

	comprising:
[Claim 29a]	performing a memory transaction comprising addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;
[Claim 29b]	wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 29c]	said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
[Claim 29d]	said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;
[Claim 29e]	after identifying the command details, obtaining the first set of attributes;
[Claim 29f]	and using attributes from said first and second device profiles; and
[Claim 29g]	selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.
Claim element	**Claim 36**
[Claim 36]	The computer readable medium of claim 29, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
Claim element	**Claim 37**
[Claim 37]	The computer readable medium of claim 36, wherein said different attribute qualifiers include different attribute values.
Claim element	**Claim 45**

[Claim 45Pre]	A memory controller for performing memory transactions, said memory controller comprising:
[Claim 45a]	means for performing a memory transaction comprising a means for addressing a first memory location, said first memory location and a second memory location are respectively associated with a first device profile and a second device profile;
[Claim 45b]	said means for addressing is directly coupled to the first memory location and second memory location;
[Claim 45c]	wherein said means for addressing includes an interface controller means for processing memory transaction requests;
[Claim 45d]	said means for addressing is directly coupled to a host as said means for addressing addresses the first memory location or second memory location;
[Claim 45e]	wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 45f]	said performing the memory transaction further comprising identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
[Claim 45g]	said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;
[Claim 45h]	said means for addressing obtains the first set of attributes after identifying the command details;
[Claim 45i]	and said means for addressing uses attributes from said first and second device profiles and selects a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

Claim element	Claim 51
[Claim 51]	The memory controller of claim 45, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
Claim element	**Claim 52**
[Claim 52]	The memory controller of claim 51, wherein said different attribute qualifiers include different attribute values.
Claim element	**Claim 59**
[Claim 59Pre]	A memory controller comprising:
[Claim 59a]	an interface controller coupled to a memory device interface and an input/output (IO) device interface;
[Claim 59b]	a memory store;
[Claim 59c]	wherein the memory device interface is directly coupled to the memory store;
[Claim 59d]	said interface controller disposed to perform a memory transaction by addressing a first memory location in the memory store,
[Claim 59e]	said first memory location and a second memory location respectively associated with a first device profile and a second device profile;
[Claim 59f]	wherein said first device profile is optimal for a data type subject to the memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 59g]	said interface controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
[Claim 59h]	said device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first and second device profiles;
[Claim 59i]	said interface controller obtaining the first set of attributes

	after identifying the command details;
[Claim 59j]	and said addressing of said first memory location includes using said attributes from said first device profile; and
[Claim 59k]	said addressing of said first memory location includes selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.
Claim element	**Claim 71**
[Claim 71]	The memory controller of claim 59, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
Claim element	**Claim 76**
[Claim 76]	The memory controller of claim 71, wherein said different attribute qualifiers include different attribute values.
Claim element	**Claim 80**
[Claim 80Pre]	An electronic storage device, comprising:
[Claim 80a]	a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;
[Claim 80b]	said memory controller directly coupled to a host as said memory controller addresses the first memory location or second memory location;
[Claim 80c]	wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 80d]	said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;
[Claim 80e]	said first device profile representing a first set of attributes of said first memory location, and said second device profile representing a second set of attributes of said second memory location, and a difference exists between said first

	and second device profiles;
[Claim 80f]	said memory controller obtaining the first set of attributes after identifying the command details;
[Claim 80g]	and said memory controller using attributes from said first and second device profiles; and
[Claim 80h]	said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.
Claim element	**Claim 84**
[Claim 84]	The electronic storage device of claim 80, wherein said difference includes different attribute qualifiers for at least one set of shared attributes from said first and second device profiles.
Claim element	**Claim 85**
[Claim 85]	The electronic storage device of claim 84, wherein said different attribute qualifiers include different attribute values.
Claim element	**Claim 98**
[Claim 98Pre]	An electronic storage device, comprising:
[Claim 98a]	a memory controller directly coupled to and disposed to address a first memory location and a second memory location which are respectively associated with a first device profile and a second device profile;
[Claim 98b]	wherein the memory controller is directly coupled to a host as the memory controller addresses the first memory location or the second memory location;
[Claim 98c]	wherein said first device profile is optimal for a data type subject to a memory transaction, wherein said data type comprises one of a random data type or a sequential data type;
[Claim 98d]	said memory controller identifies command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device;

[Claim 98e]	the first device profile representing a first set of attributes of the first memory location, and the second device profile representing a second set of attributes of the second memory location;
[Claim 98f]	said memory controller obtaining the first set of attributes after identifying the command details;
[Claim 98g]	and wherein said memory controller uses attributes from the first and second device profiles;
[Claim 98h]	wherein said memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes.

I. INTRODUCTION

KIOXIA Corporation and KIOXIA America, Inc. ("Petitioners") petition for institution of inter partes review ("IPR") of claims 1, 5-6, 29, 36-37, 45, 51-52, 59, 71, 76, 80, 84-85, 98 ("challenged claims") of U.S. Patent No. 9,135,190 ("the '190 patent"). Ex-1001.

II. GROUNDS FOR STANDING

Petitioners certify that the '190 patent is available for review under 35 U.S.C. § 311(c) and that Petitioners are not estopped from requesting *inter partes* review of the challenged claims on the grounds identified in this Petition.

III. FEES

The Commissioner is hereby authorized to charge or credit the fee specified by 37 C.F.R. § 42.15(a), and any other additional fees, to Bracewell LLP Deposit Account No. 50-0259.

IV. PRECISE RELIEF REQUESTED

Petitioners request review of the challenged claims under 35 U.S.C. § 311 and cancellation of the challenged claims under pre-AIA 35 U.S.C. § 103(a) in view of the prior art and grounds described herein.

A. Prior Art

1. Cornwell

Petitioners rely on U.S. App. Pub. No. 2007/0180186 ("Cornwell"). Ex-1005. Cornwell was published on August 2, 2007, more than a year before the alleged priority date for the '190 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

2. Ware

Petitioners also rely on U.S. Patent No. 7,269,708 ("Ware"). Ex-1006. Ware was issued on September 11, 2007, more than a year before the alleged priority date for the '190 patent, and qualifies as a prior art printed publication under at least pre-AIA 35 U.S.C. § 102(b).

B. IPR Grounds

Ground	Claims	Statutory Basis
1	1, 5-6, 29, 36-37, 45, 51-52, 59, 71, 76, 80, 84-85, 98	Obviousness under pre-AIA § 103(a) in view of Cornwell and a POSITA's knowledge
2	1, 5-6, 29, 36-37, 45, 51-52, 59, 71, 76, 80, 84-85, 98	Obviousness under pre-AIA § 103(a) in view of Ware and a POSITA's knowledge

V. THE '190 PATENT

A. Overview of the '190 Patent

The '190 patent relates to solid-state storage devices utilizing multi-profile memory controllers, but does not purport to invent a new type of memory, multi-profile memory controller, or communication protocol for memory devices and controllers. Ex-1001, 1:17-19. Instead, the patent confirms that the memory devices discussed in the specification, such as Flash memory, SRAM, or DRAM, were well-known at the time of filing. *Id*., 1:21-37, 4:47-5:20. The patent further discloses that multi-profile memory controllers for use with these memory devices were well-known at the time of filing, having "been traditionally designed to operate with memory stores or modules that comprise of memory devices that use the same memory device characteristics," *id*., 1:21-24, and explains that the recited methods and systems can simply utilize known standards and protocols, such as the Open NAND Flash Interface Specification ("ONFI"), which is a "known device interface standard created by a consortium of technology companies." *Id*., 4:47-5:3.

Instead, the '190 patent purports to identify a need for a multi-profile memory controller that can operate with memory devices having different memory attributes, *id*. at 1:43-48, and describes a "multi-profile memory controller disposed to perform memory transactions using different device profiles," to address this purported need. *Id*., 2:44-47. The'190 patent discloses a memory store, which may include multiple

memory locations, each of which is associated with at least one memory "attribute" or "characteristic of a memory location that is related to accessing or addressing the memory location." *Id*., 2:63-3:15. According to the patent, a multi-profile memory controller can perform memory transactions using the different profiles for these memory devices, *id.* at 3:61-63, 2:44-47. The '190 patent alleges that information can then be mapped to a memory location that is associated with a device profile that is optimal for the type of data subject to the memory transaction request. *Id*., 9:7-16.

B. Prosecution History of the '190 Patent

The application underlying the '190 patent was filed on September 4, 2010. In response to multiple rejections asserting that the applied-for claims were anticipated or rendered obvious by the prior art, the applicant made numerous substantive amendments to the claims. Ultimately, the Examiner issued a Notice of Allowance on June 22, 2015. Importantly, neither Cornwell nor Ware was before the Examiner during prosecution; however, as discussed below, both references disclose the particular claim elements on which the Examiner based the Notice of Allowance. *See* Ex-1003, ¶¶ 25-40.

VI. LEVEL OF ORDINARY SKILL IN THE ART

As of the priority date, a person of ordinary skill in the art ("POSITA") would have had at least a Bachelor's degree in electrical or computer engineering, or a similar field, and at least two years of work experience in the computer memory or

data storage industry. Ex-1003, ¶¶ 66-69. A POSITA could have substituted less formal education with additional relevant work experience, and vice versa. *Id.*

VII. CLAIM CONSTRUCTION

In an IPR, claim terms should be construed according to the *Phillips* standard. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *see also* 37 C.F.R. § 42.100(b). The Board need only construe terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A patent claim that uses the term "means for" invokes a rebuttable presumption that the term is a means-plus-function term that should be construed pursuant to 35 U.S.C. § 112. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). Construing a means-plus-function term is a two-step process. *Id*. at 1351. First, the claimed function must be identified. *Id*. Second, the structure disclosed in the specification for performing the claimed function must be determined. *Id*.

For purposes of this proceeding only, Petitioners submit constructions for the following terms.[1] Petitioners do not believe that construction of any other term is

[1] While Petitioners propose these constructions for purposes of this proceeding, Petitioners reserve their right to revise or amend these constructions in any other

necessary.[2]

A. Claim 45: "means for performing a memory transaction"

This term should be construed as a means-plus-function term, with a recited function of "performing a memory transaction." Further, the corresponding structure should be construed as a "multi-profile memory controller or similar structure configured to perform a memory transaction." This is confirmed by the specification, which states that the invention is directed to a "***multi-profile memory***

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action or forum. *Western Digital Corp. v. Spex Techs., Inc.*, IPR2018-00084, Paper 14 at 11 (PTAB April 25, 2018) ("37 C.F.R. § 104(b)(3) does not require [a p]etitioner to express its subjective agreement regarding correctness of its proffered claim constructions or to take ownership of those constructions"). Petitioners also reserve the right to challenge the validity of the challenged claims under 35 U.S.C. § 112 in another other action or forum. *See Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12-13 (PTAB Nov. 10, 2020) (instituting IPR despite indefiniteness arguments in parallel lawsuit, explaining that this kind of "alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review").

[2] In the co-pending litigation, the Court held that the term "optimal" had a plain and ordinary meaning. Ex-1007 at 42-45.

controller disposed to ***perform a memory transaction***." Ex-1001 at 2:44-47 (emphasis added); 3:61-63; 7:50-53; Figure 1; Ex-1003, ¶¶ 71-75.

B. Claim 45: "interface controller means for processing memory transaction requests"

This term should be construed as a means-plus-function term, with a recited function of "processing memory transaction requests." The corresponding structure should be construed as an "interface controller or similar structure configured to process memory transaction requests." This construction is established by the specification, which explains that the "***[i]nterface controller*** 52 ***processes memory transaction request[s]*** 6 by interpreting the memory transaction request and performing a memory transaction on a memory location." Ex-1001 at 7:21-24; 5:21-42; Figure 1; Ex-1003, ¶¶ 76-80.

C. Claim 45: "means for addressing a first memory location"

This term should be construed as a means-plus-function term, with a recited function of "addressing a first memory location." The corresponding structure should be construed as a "a memory device interface, a host interface, an interface controller or similar structure configured to process memory transaction requests, and associated communication pathways."

This construction is confirmed by both claim 45 and the specification. For example, claim 45 recites four requirements for the "means for addressing"

structure:

1. "means for performing a memory transaction"—i.e., the memory controller—"comprises" means for addressing, confirming that the means for addressing is a portion of the memory controller.
2. means for addressing "is directly coupled to the first memory location and second memory location," confirming that the means for addressing must include the memory device interface as that component is "directly coupled" to the memory. Ex-1001, Figure 1.
3. means for addressing is "directly coupled to a host as said means for addressing addresses the first memory location or second memory location," confirming that the means for addressing must include a host interface as that component is directly coupled to the host. *Id*.
4. means for addressing "includes an interface controller means for processing memory transaction requests." Thus, means for addressing must include an "interface controller or similar structure configured to process memory transaction requests" as explained above.

The specification of the '190 patent confirms this construction, describing these components and demonstrating that they involved in addressing a memory location. *Id*. at 5:21-42; Figure 1; Ex-1003, ¶¶ 81-86. Petitioner's construction should thus be adopted.

VIII. OVERVIEW OF THE PRIOR ART

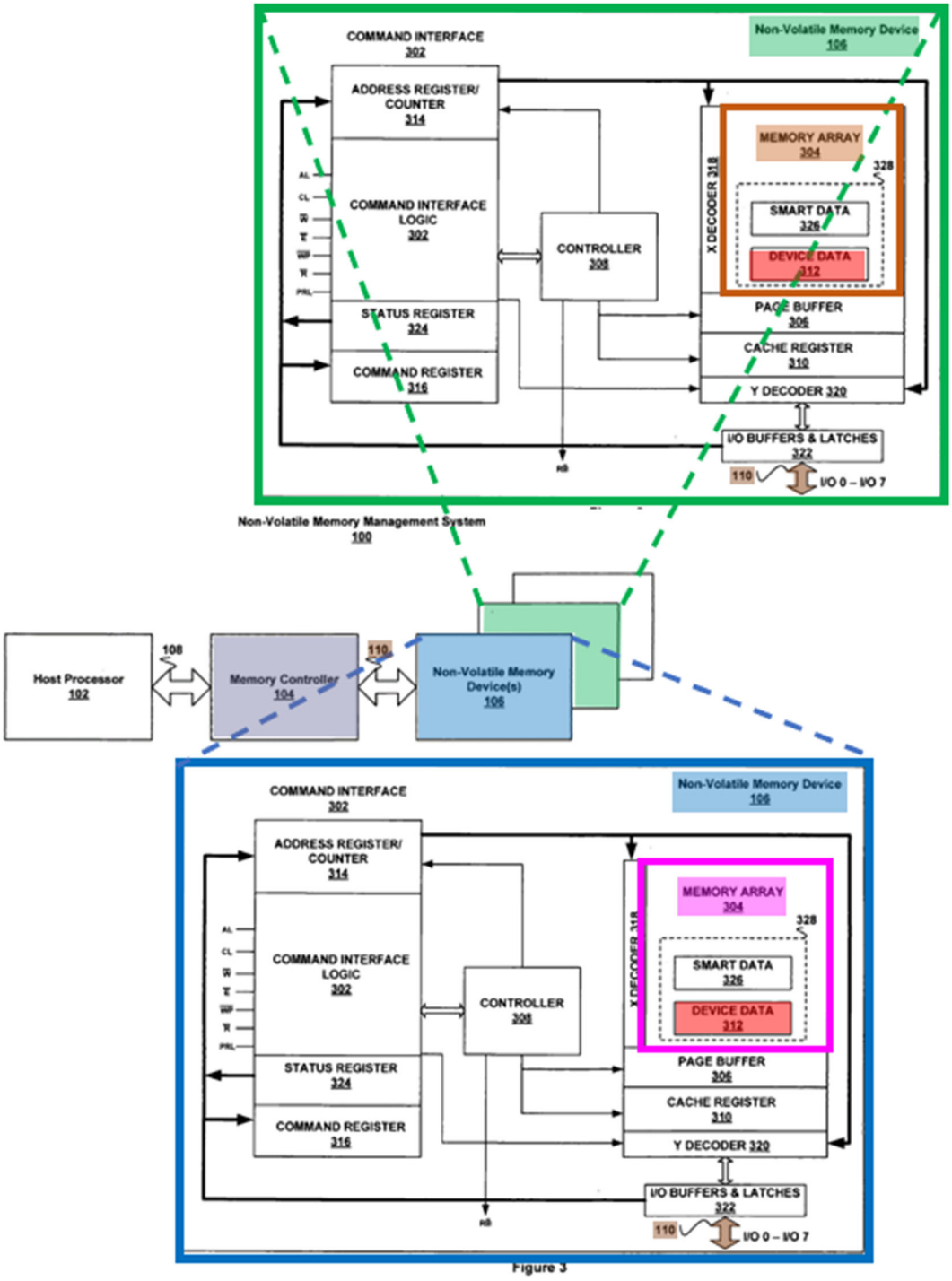
A. Cornwell

Cornwell teaches a memory management system comprising a memory controller that is coupled to—and utilizes device profiles for—multiple non-volatile memory devices. Ex-1005, ¶¶ [0007]-[0008]. These device profiles, also referred to as "device data," are used to identify each memory device and include a variety of information such as device serial number, device type, device density, device operating voltage, page size, spare area size, sequential access time, block size, bus width, bad block identification, and "any other information that is associated with attributes, properties or characteristics of the memory device." *Id.*, ¶ [0042].

Cornwell teaches that these attribute values may differ between the memory devices. For example, because the memory controller can support "single-level cell (SLC) and/or multi-level cell (MLC) flash media," Cornwell teaches that "syncing with memory devices 106 that include multi-level (MLC) technology can be performed at a different frequency than with memory devices 106 that include single-level cell technology (SLC)." *Id.*, ¶¶ [0019]; [0078]. Cornwell teaches that numerous other attribute values, such as device type and device density, may also vary between the memory devices. *Id.*, ¶ [0042].

Annotated Figures 1 and 3 illustrate Cornwell's **memory controller** coupled to a **first memory device** and **second memory device**, each of which contain **device**

data or profiles.



B. Ware

Ware teaches a memory controller for a "non-homogenous memory system" in which the main memory is comprised of two or more memory "portions" or device types, such as DRAM and Flash. Ex-1006 at 2:18-25; 3:57-4:11. Each of the memory devices has a device profile comprising sets of attributes, such as a write-to-read access time ratio, volatility, and endurance. *Id*. at 4:6-11.

Ware teaches that each of these memory devices have "different attributes." *Id*. at 2:21-26. For example, the write-to-read access time ratio differs substantially between DRAM and flash memory. *Id*. at 4:22-37. Similarly, the endurance attribute differs between memory devices. *Id*. at 2:41-48. Accordingly, the memory controller of Ware utilizes these different attributes to distribute data among the different memory devices "in a manner designed to provide fast access to the data and programs that are most frequently used." *Id.*, 3:64-67.

Annotated Figures 1 illustrates Wares **memory controller** coupled to a **first memory device** and **second memory device**.

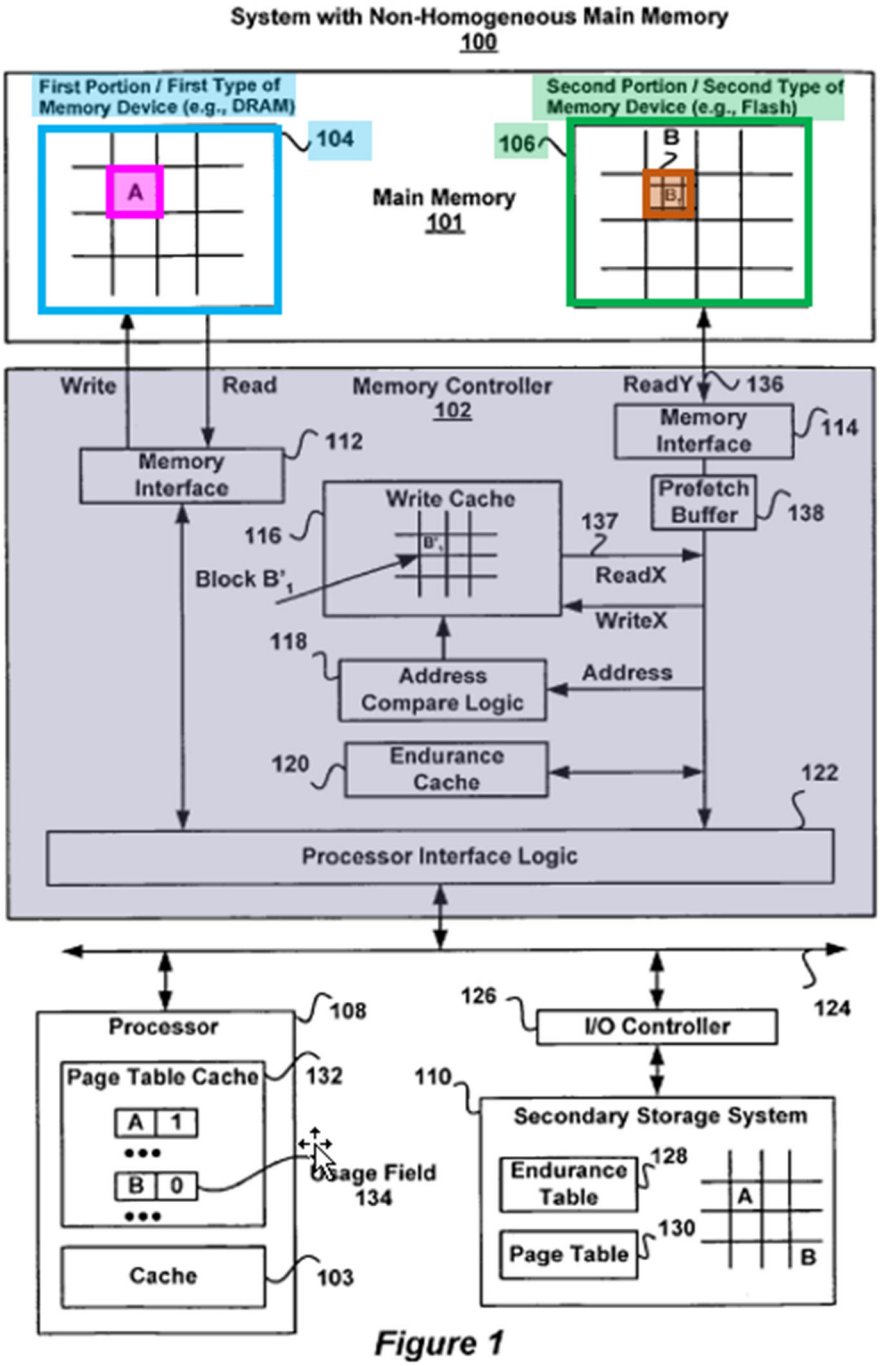

System with Non-Homogeneous Main Memory
100
First Portion / First Type of Memory Device (e.g., DRAM)
104
A
Main Memory
101
Second Portion / Second Type of Memory Device (e.g., Flash)
106
B
B'1
Write
Read
Memory Controller
102
ReadY
136
Memory Interface
112
Memory Interface
114
Write Cache
116
Block B'1
Prefetch Buffer
138
137
ReadX
WriteX
118
Address Compare Logic
Address
120
Endurance Cache
122
Processor Interface Logic
124
126
I/O Controller
Processor
108
Page Table Cache
132
A 1
B 0
Usage Field
134
110
Secondary Storage System
Endurance Table
128
Page Table
130
Cache
103

Figure 1

IX. THE CHALLENGED CLAIMS ARE UNPATENTABLE AND SHOULD BE CANCELLED

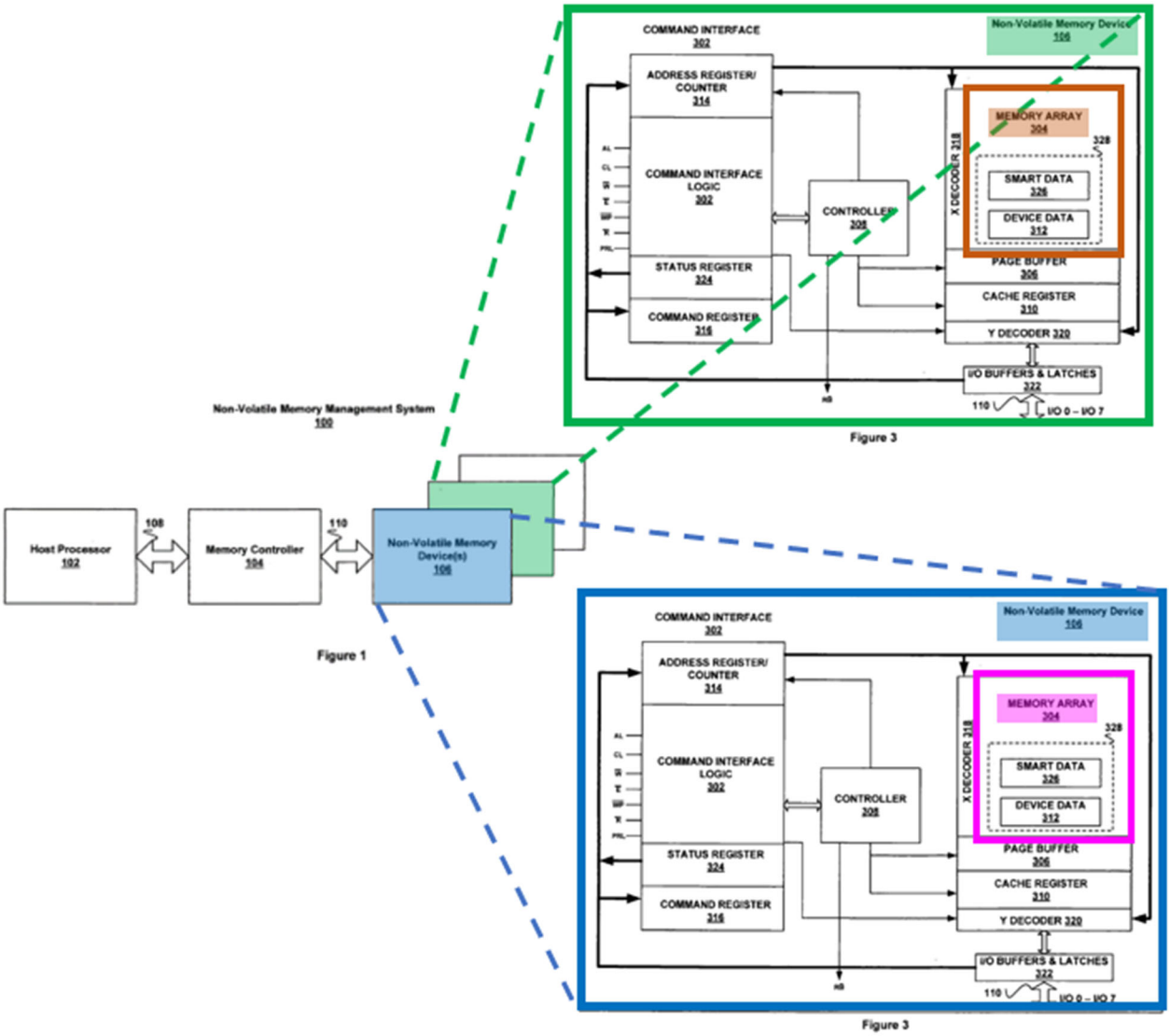
A. Ground 1: Each of the Challenged Claims is Rendered Obvious by Cornwell in View of a POSITA's Knowledge

1. Claim 1 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 1Pre]

To the extent the preamble is limiting, Cornwell discloses this element by teaching "systems, methods and devices for managing non-volatile memory," as well as memory transactions in the form of "read or write requests . . . [that] are mapped to physical memory addresses that can span two or more memory devices." Ex-1005, ¶¶ [0006]; [0008]; [0024]; [0038]; [0040]; [0046]. Each of the "one or more non-volatile memory devices 106" can be "discrete chips, chipsets and or memory modules." *Id.*, [0018]; [0020]; Ex-1003, ¶¶ 98-102.

The **first memory location** in a **first memory device 106** and **second memory location** in a **second memory device 106** disclosed by Cornwell are shown in annotated Figures 1 and 3 below:


Non-Volatile Memory Management System
100
Host Processor
102
Memory Controller
104
Non-Volatile Memory Device(s)
106
108
110
Figure 1
COMMAND INTERFACE
302
ADDRESS REGISTER/ COUNTER
314
COMMAND INTERFACE LOGIC
302
STATUS REGISTER
324
COMMAND REGISTER
316
CONTROLLER
308
Non-Volatile Memory Device
106
MEMORY ARRAY
304
328
SMART DATA
326
DEVICE DATA
312
X DECODER 318
PAGE BUFFER
306
CACHE REGISTER
310
Y DECODER 320
I/O BUFFERS & LATCHES
322
I/O 0 – I/O 7
Figure 3
Figure 3

Ex-1003, ¶ 100.

b. [Claim 1a]

Cornwell discloses a memory store comprising "one or more non-volatile memory devices 106." Ex-1005, ¶¶ [0018]; [0020]; Ex-1003, ¶ 103. The **memory store**, which includes a **first memory device 106** and a **second memory device 106**, is illustrated in annotated Figure 1 below:

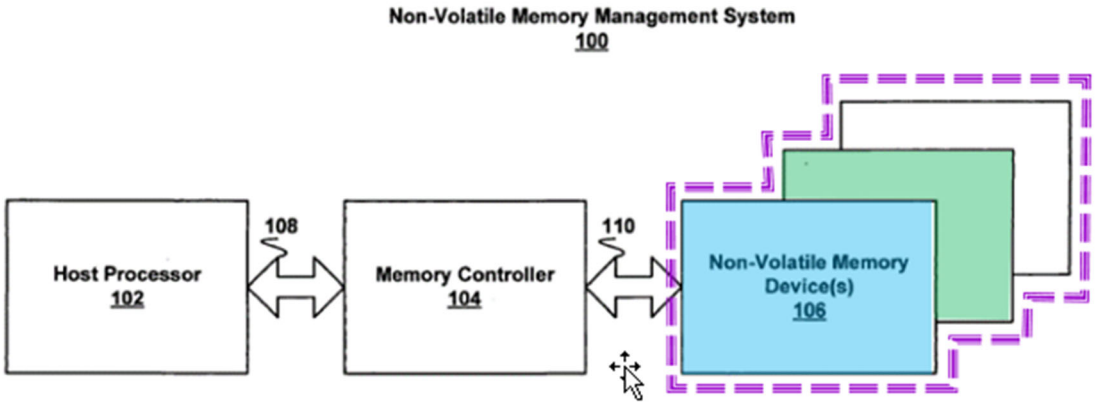
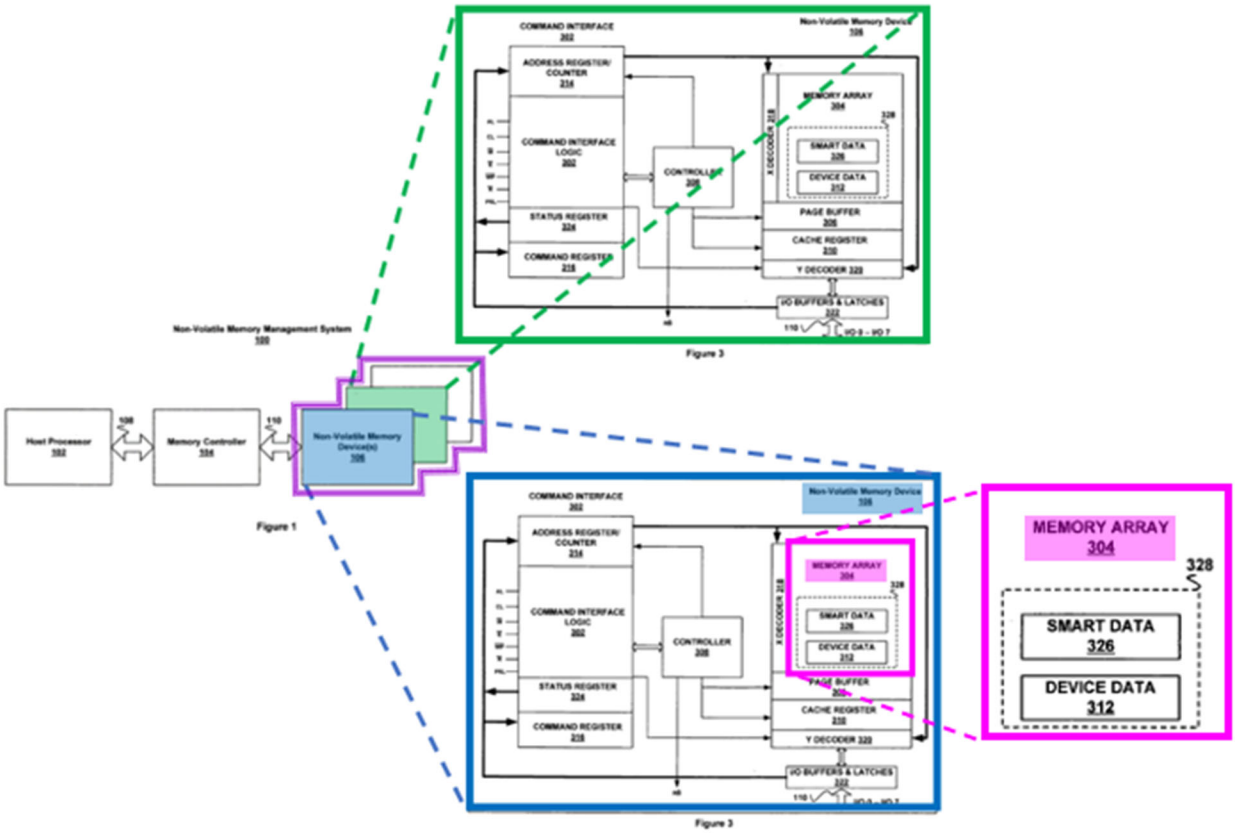


Figure 1

Ex-1003, ¶ 104.

Cornwell further discloses addressing a first memory location in a memory store, teaching that "the memory controller 104 recognizes control, ***address***, and data signals transmitted . . . by the host processor 102" and "translates the control, ***address*** and data ***signals into*** memory ***access requests on memory devices 106***." Ex-1005, ¶¶ [0021] (emphasis added); [0035]; [0037]. A POSITA would understand that the address for accessing data in Cornwell's memory device would include information addressing the location in the memory device where the data is located, including in

the **first memory location** in a **first memory device 106** in the **memory store,** as illustrated below:



See Ex-1003, ¶¶ 104-107.

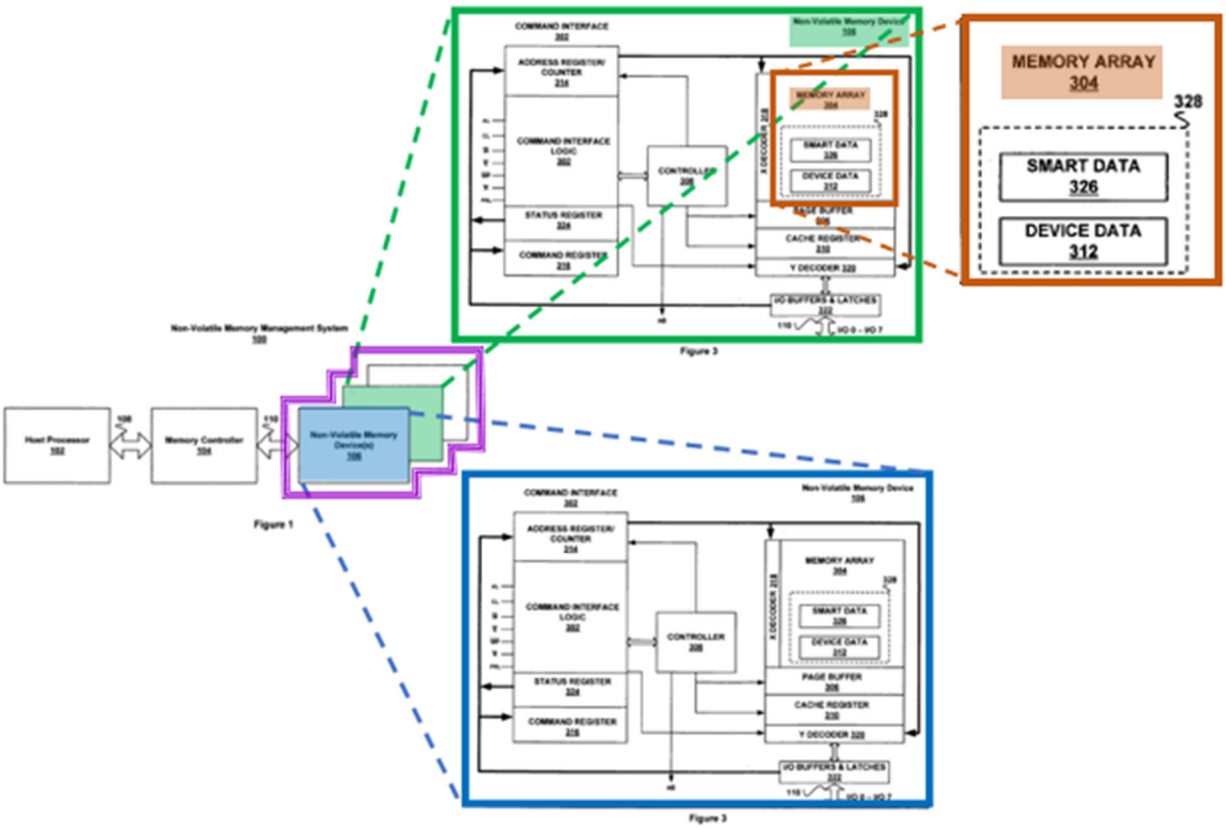
c. [Claim 1b]

Cornwell discloses that each memory device 106 includes a device profile in the form of "device data 312 [that] can be used to identify the memory device 106 and its manufacturer." Ex-1005, ¶ [0042]; Ex-1003, ¶ 108. The device profile (device data) "can include an electronic signature or serial number that includes a manufacturer code and/or device code," as well as attributes such as "device type

(e.g., NAND, NOR, etc.), device density (e.g., 512 Mb, 1 Gb, 2 Gb, etc.), device operating voltage (e.g., 3.3 volts), page size (1 k, 2K, etc.), spare area size (e.g., 8, 16 bytes, etc.), sequential access time (e.g., 30, 50 nanoseconds, etc.), block size (e.g., 64 k, 128 k, etc.), bus width (e.g., ×8, ×16, etc.), bad block identification, and any other information that is associated with attributes, properties or characteristics of the memory device 106 (collectively, referred to herein as 'attributes')." Ex-1005, ¶ [0042]; Ex-1003, ¶¶ 108-110.

d. [Claim 1c]

As illustrated below in annotated Figures 1 and 3, the **second memory location** disclosed by Cornwell is in the **second memory device** in the **memory store**. *See also supra*, §§ IX.A.1.b, IX.A.1.c; Ex-1003, ¶¶ 111-112.



e. [Claim 1d]

Cornwell discloses that a memory read or write transaction is performed on at least one memory location, teaching that "[d]uring operation, one or more memory devices 106 receive signals from the memory controller 104 over Input/Output (I/O) bus 110, which enables the ***memory devices 106 to perform*** memory access requests (e.g., ***read or write operations***)." Ex-1005, ¶¶ [0024] (emphasis added); [0031]; [0034]; [0039]; [0040]; Ex-1003, ¶¶ 113-114.

f. [Claim 1e]

Cornwell discloses that data is transferred between the host and the first or

second memory locations, explaining that "***a host system performs reads and writes*** to logical block addresses (LBAs) which are mapped or translated to ***physical block addresses of flash memory***." Ex-1005, ¶¶ [0004] (emphasis added); [0007]; [0021]; [0029]; Ex-1003, ¶ 115. Annotated Figure 1, below, illustrates that data is transferred by **the host processor** over **bus 108** and **bus 110** to and from memory locations in the **first memory device** and the **second memory device**:

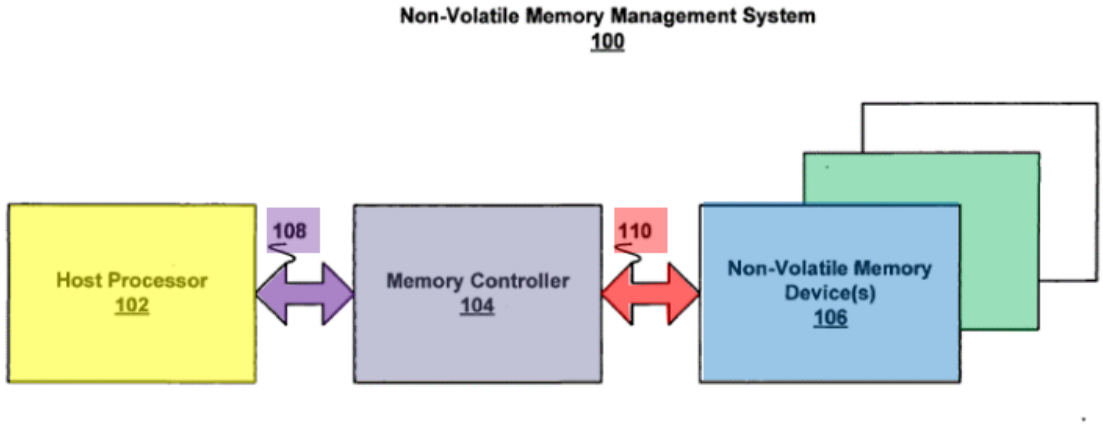
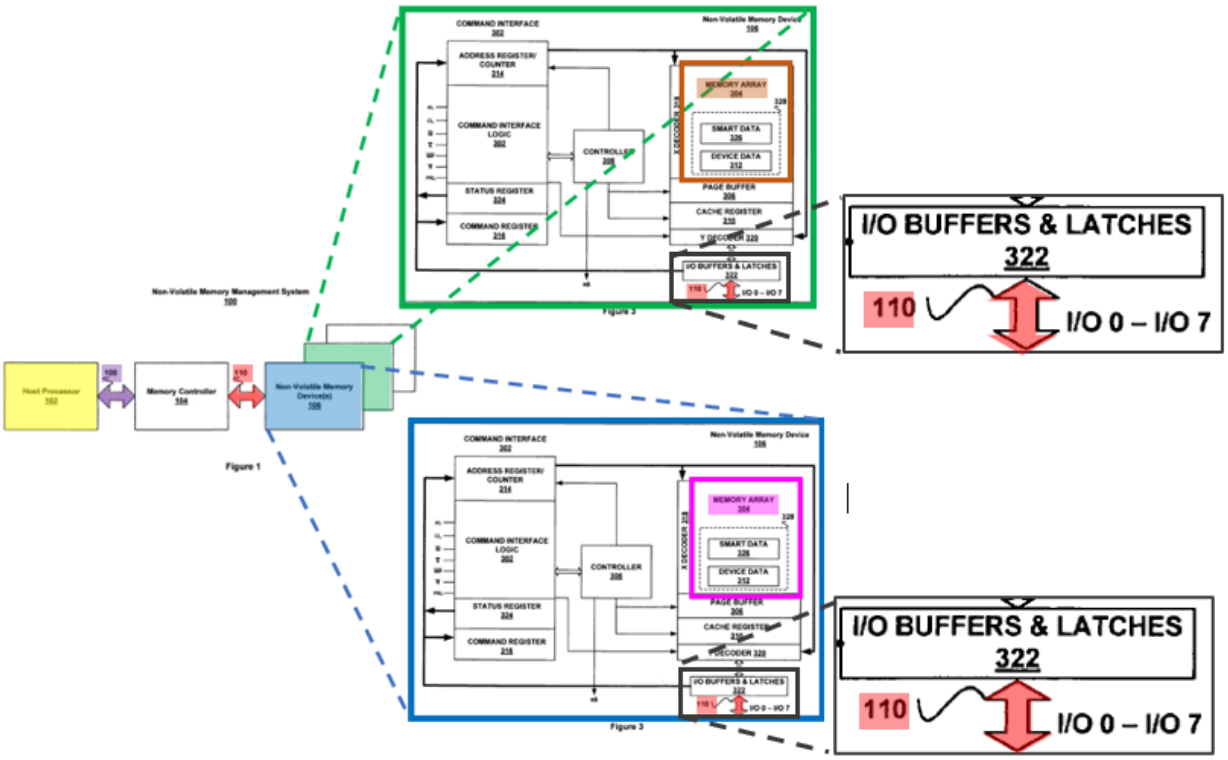


Figure 1

Annotated Figures 1 and 3 below further illustrate this process:



Ex-1003, ¶¶ 116-118.

g. [Claim 1f]

The device profile disclosed by Cornwell "can be used to identify the memory device 106 and its manufacturer" and may be comprised of a variety of information. Ex-1005, ¶ [0042]; *supra* § VI.A.1.c; Ex-1003, ¶ 119. This information includes identifying the "device type (e.g., NAND, NOR, etc.)." Ex-1005, ¶ [0042]. A POSITA would have understood that NOR flash provides access to, and is therefore optimal for, a random data type. Ex-1003, ¶ 120. Likewise, a POSITA would have understood that NAND flash provides access to, and thus is optimal for, a sequential type. *Id*.

Cornwell also discloses that the device profile may comprise information regarding "block size (e.g., 64 k, 128 k, etc.)," Ex-1005, ¶ [0042], and teaches that a device profile can be optimized for a particular data type subject to the memory transactions through "block defining," wherein "[m]emory access efficiency can be improved by matching the average size of files to be stored in the flash media to the block size of the flash media." *Id.*, ¶¶ [0048]-[0050] (emphasis added). Cornwell further discloses that "[i]n some implementations a ***random* [*data type*] *read command*** may be issued first, followed by a page [***sequential data type***] read command." *Id*., ¶ [0040] (emphasis added). By matching block size to file size, and teaching that files contain random or sequential data types, Cornwell teaches that a first device profile is optimal for a data type subject to the memory transaction. Ex-1003, ¶ 122.

Accordingly, because a POSITA would have understood from Cornwell that a device profile would be optimal for a data type subject to the transaction, this claim element is rendered obvious by Cornwell in view of a POSITA's knowledge. *Id.*, ¶¶ 119-123.

h. [Claim 1g]

The memory device disclosed by Cornwell "includes a command interface 302, a memory array 304 and a controller 308." Ex-1005, ¶ [0034]. Cornwell further discloses a variety of commands that are "translated into signals which can be used

by a controller and decoding logic in the memory device 106 to access a memory array." *Id*., ¶ [0027]. "For example, when the host processor 102 makes a read request, the 'Read Sectors' opcode (20 h) is transmitted to the memory controller 104, together with address and control signals for accessing the sector(s)." *Id*., ¶¶ [0027]; [0035]; [0038]. A POSITA would thus understand that Cornwell discloses identifying command details for causing the memory transaction to be performed, wherein the command details comprise the first memory device. Ex-1003, ¶ 124.

Examples of commands, including read and write commands, are shown in Table 1:

TABLE I

Examples of Standard ATA-6 Commands

Opcode	Command
10h	Recalibrate
20h	Read Sectors
30h	Write Sectors
40h	Read Verify
B0h	SMART
C8h	Read DMA
CAh	Write DMA
E0h	Standby Immediate
E2h	Standby
E7h	Flush Cache
ECh	Identify
EFh	Set Features

Ex-1005, ¶ [0026]; Ex-1003, ¶¶ 125-127.

i. [Claim 1h]

Cornwell discloses that each device profile (device data 312) includes a variety of information "associated with ***attributes***, ***properties or characteristics*** of

the memory device 106 (***collectively, referred to herein as 'attributes'***)." Ex-1005, ¶ [0042] (emphasis added); *supra* § IX.A.1.c. The memory profiles taught by Cornwell may also be different, including by having different densities for single-layer cell or multi-layer cell technology. Ex-1005, ¶ [0078]; Ex-1003, ¶ 129. Similarly, Cornwell identifies many other potential differences in device attributes, including device type, device density, spare area, block size, bad block identification, etc. Ex-1005, ¶¶ [0042]; [0054]-[0056]; Ex-1003, ¶ 130.

Accordingly, because a POSITA would have understood from Cornwell that differences could exist between device profiles, this claim element is rendered obvious by Cornwell in view of a POSITA's knowledge. Ex-1003, ¶¶ 128-133.

j. [Claim 1i]

Cornwell discloses that attributes comprising device data 312 can be obtained or "transmitted to the memory controller 104 via the I/O bus 110 ***in response to a read command*** issued by the memory controller." Ex-1005, ¶ [0043] (emphasis added). This teaching confirms that the attributes are obtained after the command details are identified. Ex-1003, ¶¶ 134-135.

k. [Claim 1j]

Cornwell teaches that each of the attributes, as described above, is associated with a respective attribute qualifier. Ex-1005, ¶ [0042]; *supra*, § IX.A.1.i. For example, the "device type" attribute is associated with the qualifiers "NAND" or

"NOR," the "device density" attribute is associated with the qualifiers "512 Mb," "1Gb," and "2Gb," etc. Ex-1005, ¶ [0042]; Ex-1003 ¶ 136. Cornwell also discloses that the device profile (device data 312) comprising these qualifiers "can be used to identify the memory device 106 and its manufacturer," thereby qualifying each memory location. Ex-1005, ¶ [0042]; Ex-1003, ¶¶ 137-138.

l. [Claim 1k]

Cornwell discloses that the memory store is directly coupled to at least one memory bus that is also coupled to a controller, noting "one or more memory devices 106 receive[s] signals ***from the memory controller 104 over Input/Output (I/O) bus 110***, which enables the memory devices 106 to perform memory access requests (e.g., read or write operations)." Ex-1005, ¶¶ [0024] (emphasis added); [0042]. Annotated Figure 1 further illustrates that the **memory store** is directly coupled to **bus 110**, which is directly coupled to the **memory controller 104**:

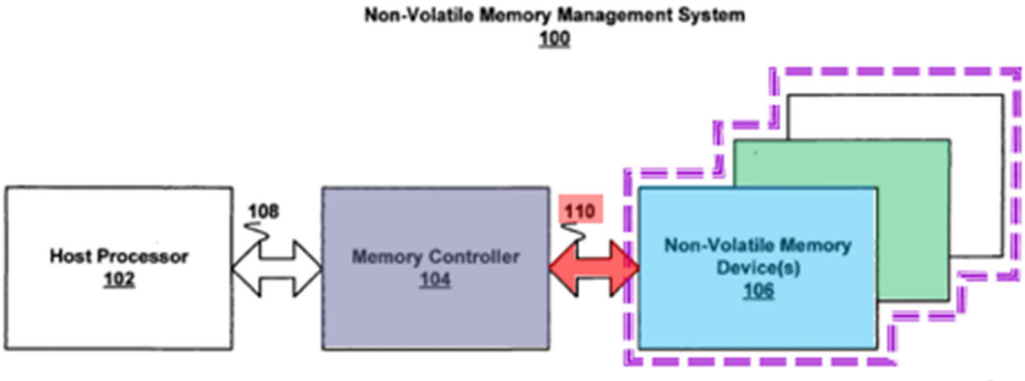


Figure 1

Ex-1003, ¶ 140.

Cornwell further discloses that the controller performs read and write transactions on the memory store, explaining that the memory devices "receive signals from the memory controller 104," which "enables the memory devices 106 to perform memory access requests (e.g., read or write operations)." Ex-1005, ¶¶ [0024]; [0029]; Ex-1003, ¶¶ 139-142.

m. [Claim 1l]

As shown in annotated Figure 1, Cornwell discloses that the **host processor** is directly coupled to the **memory controller 104** via **bus 108**, explaining that data requests "are transmitted to the memory controller 104 on the IDE/ATA ***bus 108*** by the host processor 102." Ex-1005, ¶¶ [0025] (emphasis added); [0021]; Ex-1003, ¶¶ 143-145:

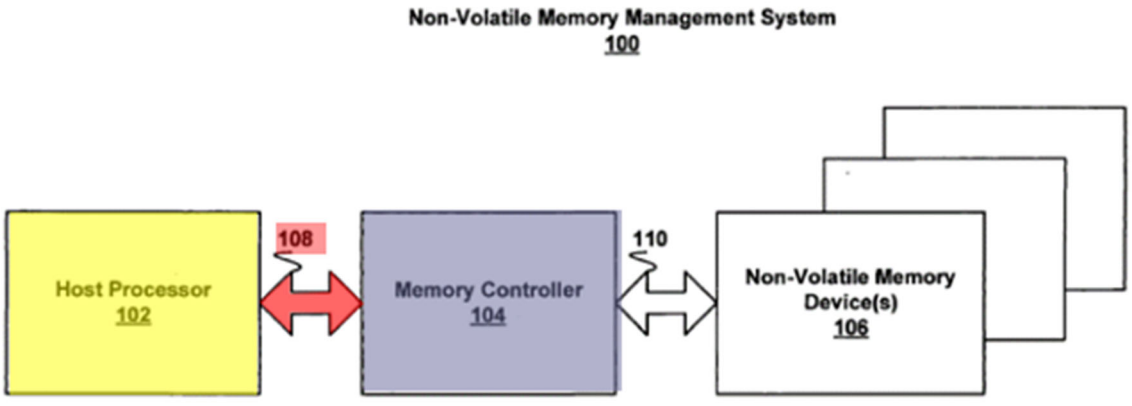
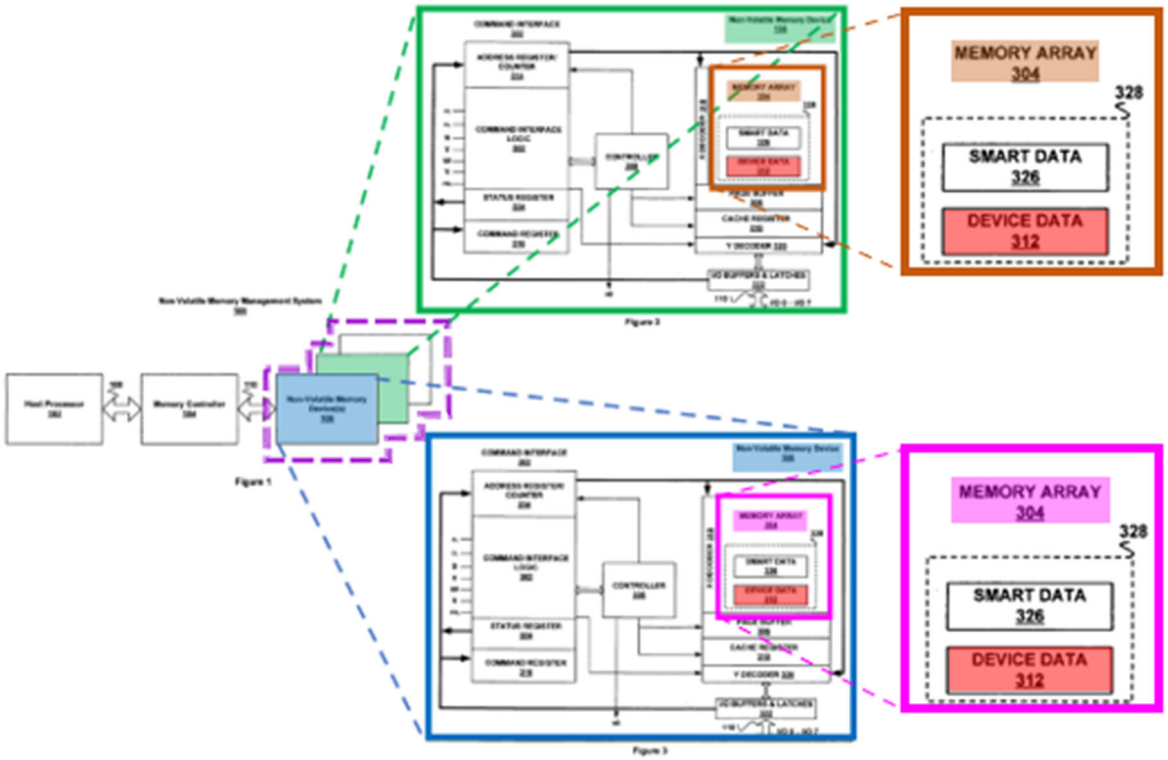


Figure 1

n. [Claim 1m]

Cornwell discloses that each device profile (device data 312) may be "stored in a spare area 328 of the memory array 304" and "can be used to identify the memory device 106 and its manufacturer." Ex-1005, [0042]; *supra* §§ IX.A.1.c, IX.A.1.i; Ex-1003, ¶¶ 146-148. Annotated Figures 1 and 3 illustrate that **device profiles** for both the **first memory location** (memory array 304) and the **second memory location (memory array 304)** are stored in **the memory store**:



Ex-1003, ¶ 147.

o. [Claim 1n]

Cornwell teaches that attributes from each device profile are used, i.e., device data 312 is transmitted "***in response to a read command*** issued by the by the

memory controller" and "***used by the memory controller 104 and/or host system*** to perform various memory management tasks." Ex-1005, ¶¶ [0043] (emphasis added); [0042]; [0046], [0058]; Ex-1003, ¶¶ 149-150.

p. [Claim 1o]

Cornwell teaches that "the controller 308, ***programs the page*** into the memory array 304 . . . ." Ex-1005, ¶ [0039] (emphasis added). Each page has a specific "page size (1k, 2k, etc.)." *Id*., ¶¶ [0042]; [0048]; [0050]. Cornwell therefore teaches selecting a transfer size for the memory transaction. Ex-1003, ¶ 151.

Cornwell also discloses that page size is a function of device density, which may vary, and the IDE/ATA bus standard, which is used as the communication between the host and the command interface 302. Ex-1005, [0042]; *supra*, §§ IX.A.1.i-IX.A.1.k. Further, a POSITA would have understood that page size is the length of a row (i.e., the number of columns) in the memory, which varies with the device density, and that the data size information (e.g., the number of logical sectors to be transferred), which is referred by the controller for the communication between the controller and the memory store, is included in the ATA command from the host. Ex-1003, ¶¶ 151-152. Cornwell thus teaches that the transfer size is also a function of the first set of attributes, such as the device density. *Id.* Cornwell also teaches that the transfer size is selected by the controller. *Id.*, ¶¶ 153-155.

2. Claim 5 is Obvious in View of Cornwell and a POSITA's Knowledge

Cornwell teaches that the first and second device profiles (device data 312) have shared attributes. Ex-1005, ¶ [0042]; *supra*, §§ IX.A.1.k, IX.A.1.i. It would also have been obvious to a POSITA that these shared attributes could have different attribute qualifiers. *Supra*, § IX.A.1.k; Ex-1003, ¶ 158. For example, it would have been obvious to a POSITA, based on their knowledge in view of Cornwell, that the first memory location using NAND would have a "NAND" qualifier for the "device type" attribute, while a second memory location using NOR would have a "NOR" qualifier for the "device type" attribute. Ex-1005, ¶ [0042]; Ex-1003, ¶ 158.

3. Claim 6 is Obvious in View of Cornwell and a POSITA's Knowledge

It would have been obvious to a POSITA that the shared attributes disclosed by Cornwell could have different attribute qualifiers. *Supra*, §§ IX.A.1.i; Ex-1003, ¶ 162. Cornwell also discloses that each attribute qualifier has an attribute value, which can be different for different attribute qualifiers. *Supra*, §§ IX.A.1.i, IX.A.2. It therefore would have been obvious to a POSITA, based on their knowledge in view of Cornwell, to include different attribute values for different attribute qualifiers. Ex-1003, ¶¶ 162-164.

4. Claim 29 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 29 pre]

To the extent the preamble is limiting, Cornwell discloses the recited method for the reasons discussed above with respect to element [1 pre]. *Supra*, § IX.A.1.a; Ex-1003, ¶ 166. Cornwell further discloses that "memory device information is stored on a ***computer-readable medium*** in the host system (e.g., memory, hard disk, CDROM, etc.)," which constitute non-transitory computer readable media. Ex-1005, ¶ [0047] (emphasis added). Further, "the host system can include pre-stored information for multiple memory devices that are known to be compatible with the host system and the memory controller." *Id*. Thus, the non-transitory computer readable medium comprises computer executable instructions adapted to cause a method of performing memory transactions on a first memory location and a second memory location. *Id.*, ¶¶ [0083]-[0084]; Ex-1003, ¶¶ 167-171.

b. [Claim 29a]

The recited features of element [29a] are substantially identical to those of elements [1a] and [1b]. Cornwell discloses this element for the reasons discussed above. *Supra* §§ IX.A.1.b, IX.A.1.c; Ex-1003, ¶¶ 172-178.

c. [Claim 29b]

Element [29b] is identical to element [1f] and is rendered obvious by Cornwell for the reasons discussed above. *Supra* § IX.A.1.g; Ex-1003, ¶¶ 179-184.

d. [Claim 29c]

Element [29c] is identical to element [1g] and is disclosed by Cornwell for the

reasons discussed above. *Supra* § IX.A.1.h; Ex-1003, ¶¶ 185-188.

e. [Claim 29d]

Element [29d] is identical to element [1h] and is rendered obvious for the reasons discussed above. *Supra* § IX.A.1.i; Ex-1003, ¶¶ 189-194.

f. [Claim 29e]

Element [29e] is identical to element [1i] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.1.j; Ex-1003, ¶¶ 195-196.

g. [Claim 29f]

Element [29f] is identical to element [1n] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.1.o; Ex-1003, ¶¶ 197-198.

h. [Claim 29g]

Element [29g] is identical to element [1o] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.1.p; Ex-1003, ¶¶ 199-203.

5. Claim 36

Claim 36 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.A.2; Ex-1003, ¶¶ 205-207.

6. Claim 37

Claim 37 is substantially identical to claim 6 and is rendered obvious for the reasons discussed above. *Supra* § IX.A.3; Ex-1003, ¶¶ 209-212.

7. Claim 45 is Obvious in View of Cornwell and a POSITA's

Knowledge

a. [Claim 45 pre]

To the extent the preamble is limiting, Cornwell discloses "[a] memory controller [that] is operatively coupled to the one or more non-volatile memory devices and configurable to access the one or more non-volatile memory devices." Ex-1005, ¶ [0007]; Ex-1003, ¶¶ 214-215.

b. [Claim 45a]

Cornwell discloses the first recited function of "performing a memory transaction" as well as a "memory controller" for performing that function pursuant to Petitioner's proposed construction. Specifically, Cornwell discloses "***[a] memory controller*** [that] is operatively coupled to the one or more non-volatile memory devices and ***configurable to access the one or more non-volatile memory devices***." Ex-1005, ¶¶ [0007] (emphasis added); [0021] (explaining that "memory controller 104 translates control, address and data signals into memory access requests on memory devices 106"); [0024]-[0025]; Ex-1003, ¶¶ 218-219.

Cornwell also discloses the second recited function of "addressing a first memory location." Cornwell explains that the memory controller "translates control, ***address*** and data signals into memory access requests on memory devices 106." *Id*. ¶¶ [0021]; [0035]. Cornwell also discloses Petitioner's proposed structure of "a **memory device interface**, a **host interface**, an **interface controller**, and **associated**

communication pathways," *supra* § VII.C, as shown in annotated Figures 1 and 2:

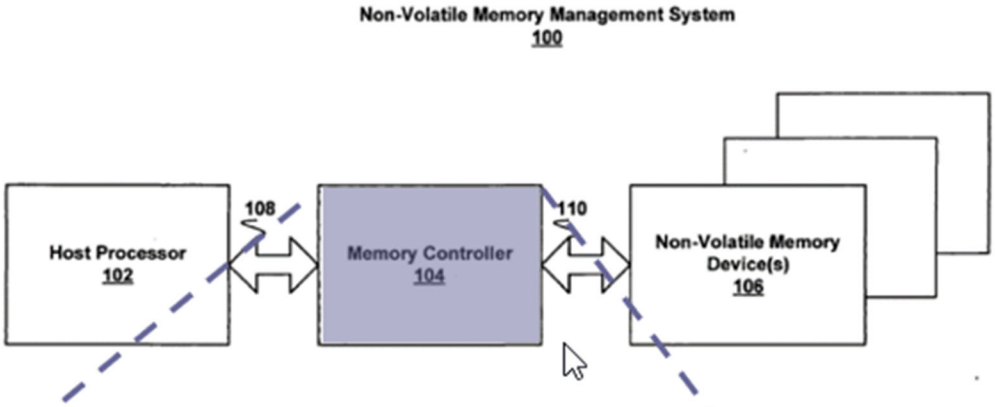


Figure 1

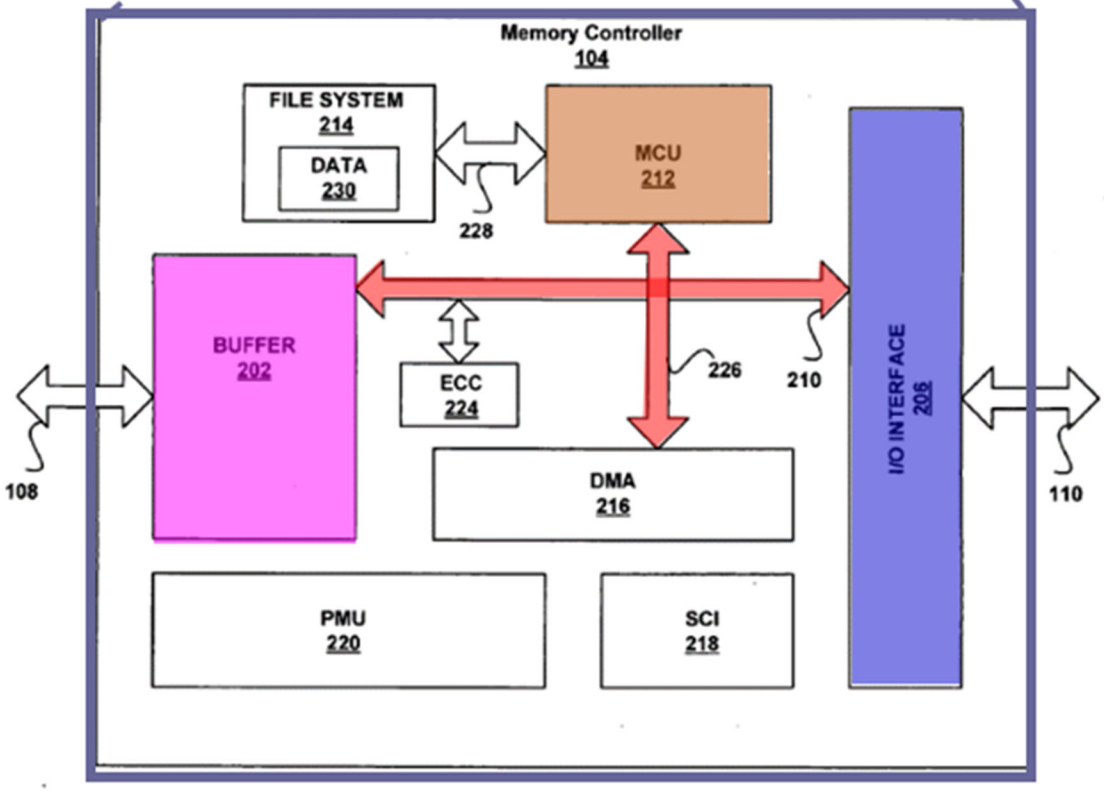


Figure 2

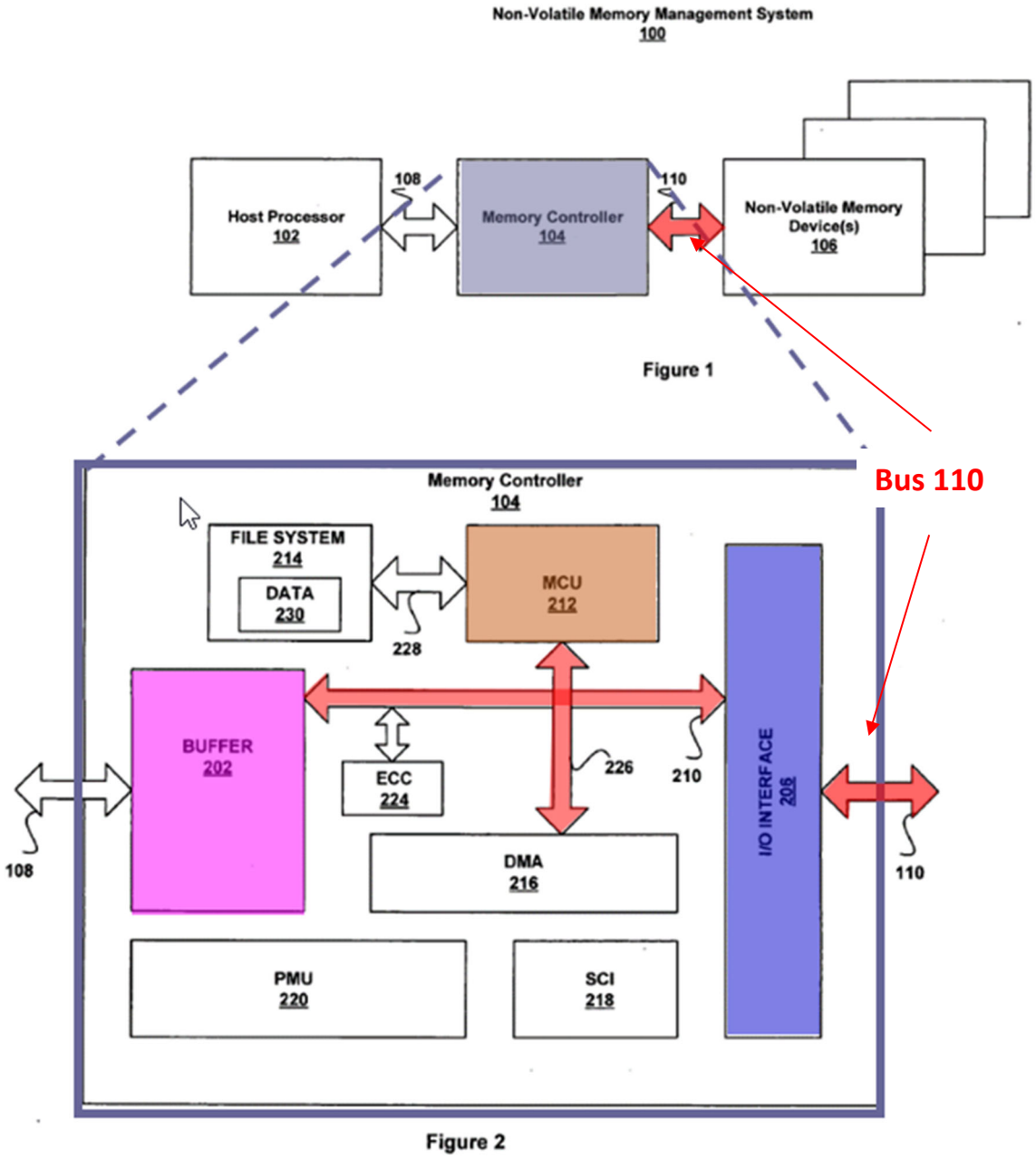
Ex-1003, ¶¶ 221-225.

Cornwell also teaches that the first and second memory locations are

respectively associated with a first device profile and second device profile as explained above for element [1b]. *Id.*, ¶ 226; *supra* § IX.A.1.c.

c. [Claim 45b]

Cornwell discloses that the memory device interface (I/O interface 206), which is part of the means for addressing, is directly coupled to the memory and "provides connectivity to the memory devices 106 through I/O bus 110, and includes circuitry for enabling read, program and erase operations to one or more memory devices 106." Ex-1005, ¶ [0031]. This memory device interface "allows concurrent read, program, and erase operations to multiple memory devices." *Id.*; Ex-1003, ¶ 228. Annotated Figures 1 and 2 below show that **I/O interface** is directly connected to the memory devices via **bus 110**:



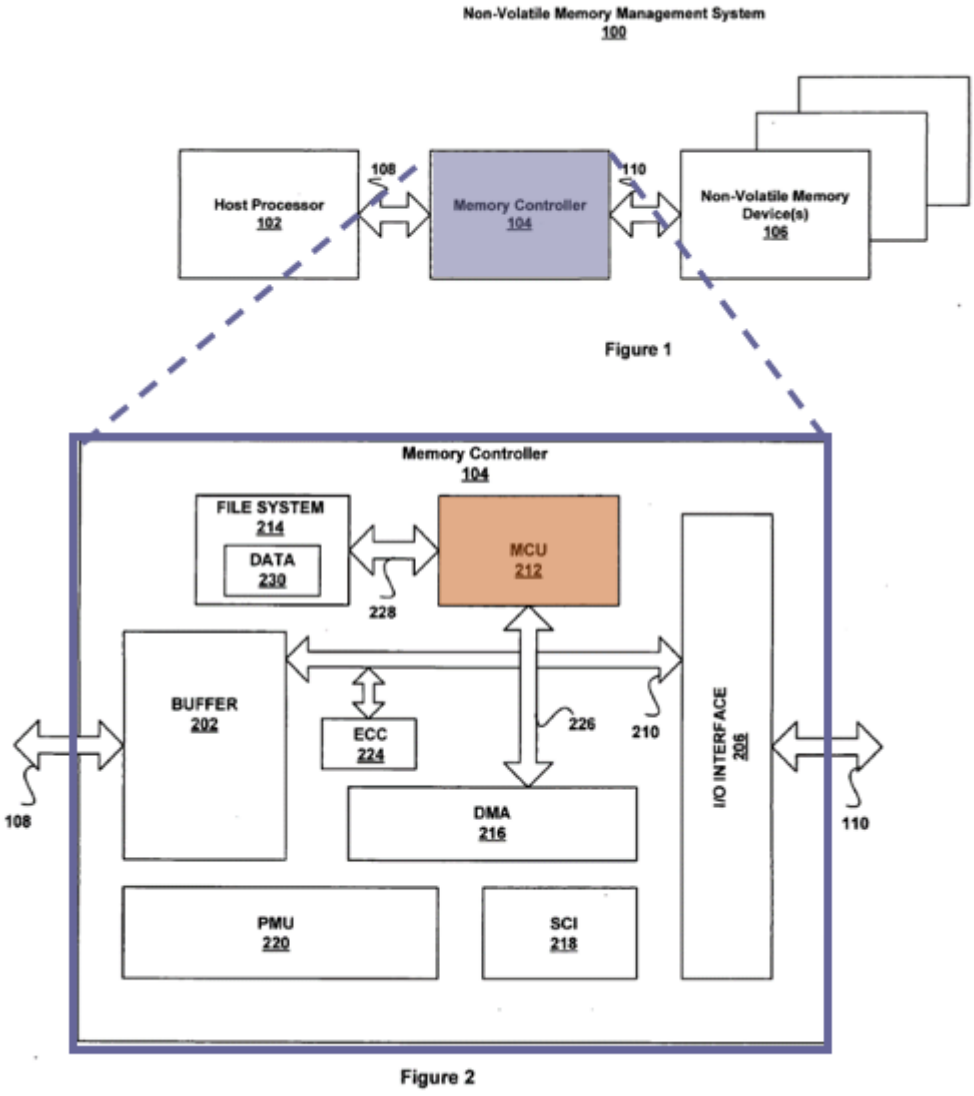
Ex-1003, ¶ 229.

d. [Claim 45c]

Cornwell discloses the recited function of "processing memory transaction requests," as well as Petitioner's proposed structure of an interface controller.

Cornwell discloses a micro-controller unit 212 ("MCU") that "translates IDE/ATA commands into data and control signals required for memory operations." Ex-1005, ¶¶ [0028]-[0029]. The MCU is also coupled to a file system 214, which contains firmware for performing tasks such "translat[ing] signals from the host processor 102 into memory read and write operations." *Id*., ¶ [0029]. Accordingly, the MCU (and related firmware) is an interface controller that performs the function of processing memory transaction requests per Petitioner's proposed construction. *Supra* § VII.B;Ex-1003, ¶¶ 231-232.

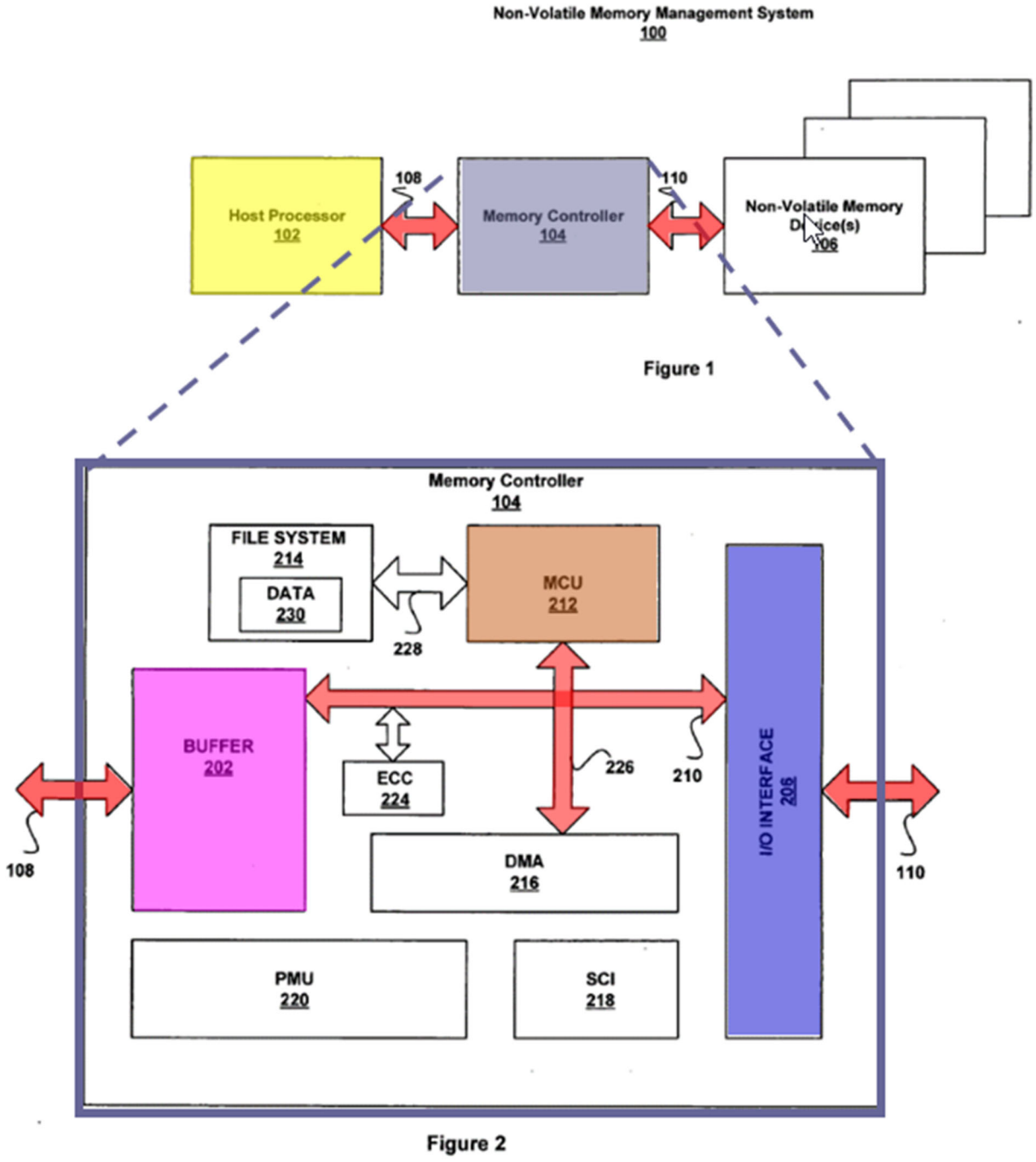
The **interface controller** (MCU) is illustrated in annotated Figures 1 and 2 below:



Ex-1003, ¶ 233.

e. [Claim 45d]

As illustrated below, Cornwell discloses that the means for addressing—i.e., the **memory device interface**, a **host interface**, an **interface controller**, and **associated communication pathways**—is directly coupled to the **host processor** as the first or second memory location are addressed:



Ex-1003, ¶¶ 235-237.

f. [Claim 45e]

Element [45e] is identical to element [1f] and is rendered obvious by Cornwell for the reasons discussed above. *Supra* § IX.A.1.g; Ex-1003, ¶¶ 239-243.

g. [Claim 45f]

Element [45f] is identical to element [1g] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.1.h; Ex-1003, ¶¶ 244-247.

h. [Claim 45g]

Element [45g] is identical to element [1h] and is rendered obvious for the reasons discussed above. *Supra* § IX.A.1.i; Ex-1003, ¶¶ 248-253.

i. [Claim 45h]

Cornwell discloses that the MCU, part of the means for addressing, obtains the first set of attributes after identifying the command details, explaining that the attributes are transmitted to the memory controller "***in response to a read command*** issued by the memory controller." Ex-1005, ¶¶ [0043] (emphasis added); [0029] (explaining the function of the MCU); Ex-1003, ¶¶ 254-256.

j. [Claim 45i]

Cornwell discloses using attributes from the first and second device profiles, and selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes. *Supra* § IX.A.7.b; Ex-1003, ¶¶ 257-261.

Cornwell also discloses that these functions are performed by the MCU, which is part of the means for addressing. Ex-1005, ¶ [0029]; Ex-1003, ¶ 262.

8. Claim 51 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 51 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.A.2; Ex-1003, ¶¶ 265-267.

9. Claim 52 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 52 is substantially identical to claim 6 and is rendered obvious for the reasons discussed above. *Supra* § IX.A.3; Ex-1003, ¶¶ 269-272.

10. Claim 59 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 59 pre]

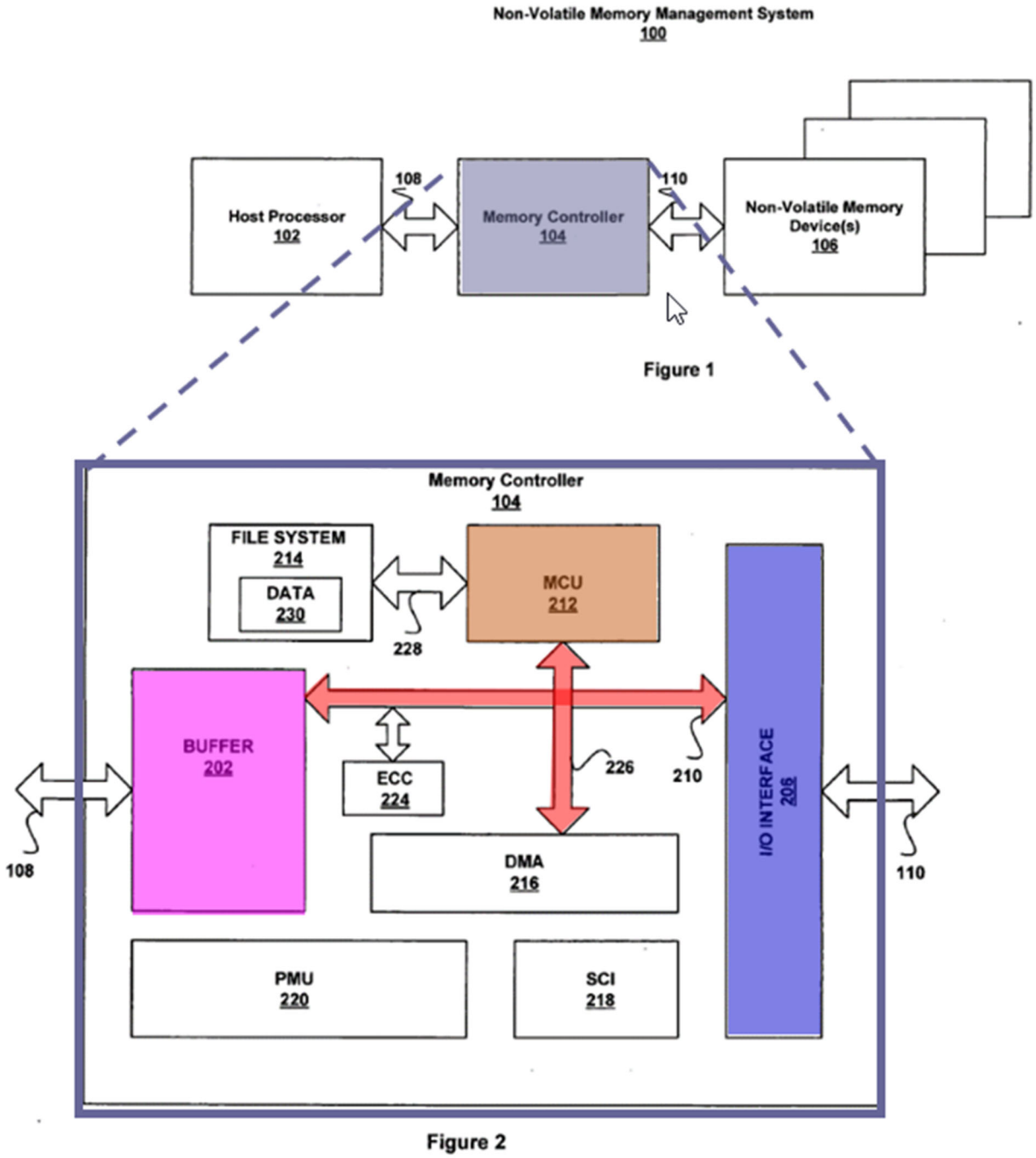
To the extent the preamble is limiting, Cornwell discloses a memory controller. *Supra*, § IX.A.7.a; Ex-1005, ¶¶ [0007]; [0019]; [0028]-[0033]; Ex-1003, ¶¶ 274-276.

b. [Claim 59a]

Cornwell discloses an interface controller in the form of a MCU, *supra* § IX.A.7.d, which is coupled to the host interface (I/O interface) and memory device interface. Cornwell explains that the MCU "translates IDE/ATA commands" from the host "into data and control signals required for memory operations" on the memory device. Ex-1005, ¶ [0029]; *id*. ("MCU firmware can translate signals from

the host processor into memory read and write operations").

Annotated Figures 1 and 2 below show that **MCU** is directly connected to the **memory devices interface** and a **host** (I/O interface) via **communication pathways**:



Ex-1003, ¶¶ 277-281.

c. [Claim 59b]

Cornwell discloses a memory store that comprises "one or more non-volatile

memory devices 106," which "can be discrete chips, chipsets and or memory modules." Ex-1005, ¶¶ [0018], [0020]; *supra* § IX.A.1.b; Ex-1003, ¶¶ 282-284.

d. [Claim 59c]

As shown in Annotated Figures 1 and 2 below, Cornwell discloses that the **memory device interface** (IO Interface 206) is directly coupled to the **memory store**, explaining that the "I/O interface provides connectivity to the memory devices 106 through I/O bus 110." Ex-1005, ¶¶ [0031], [0024]-[0025]; Ex-1003, ¶¶ 285-287.

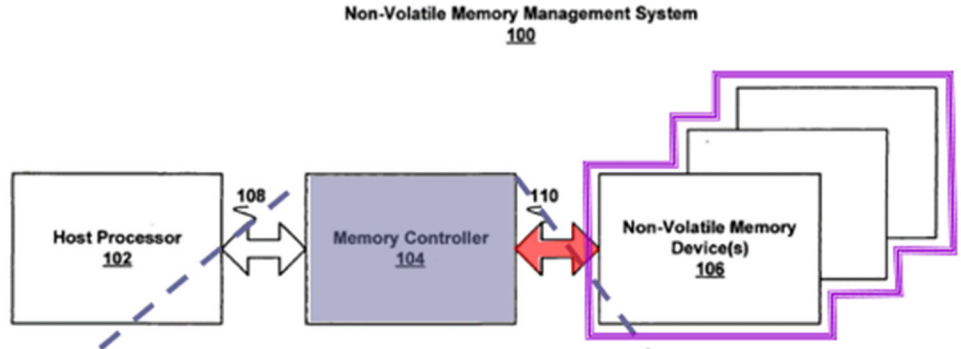


Figure 1

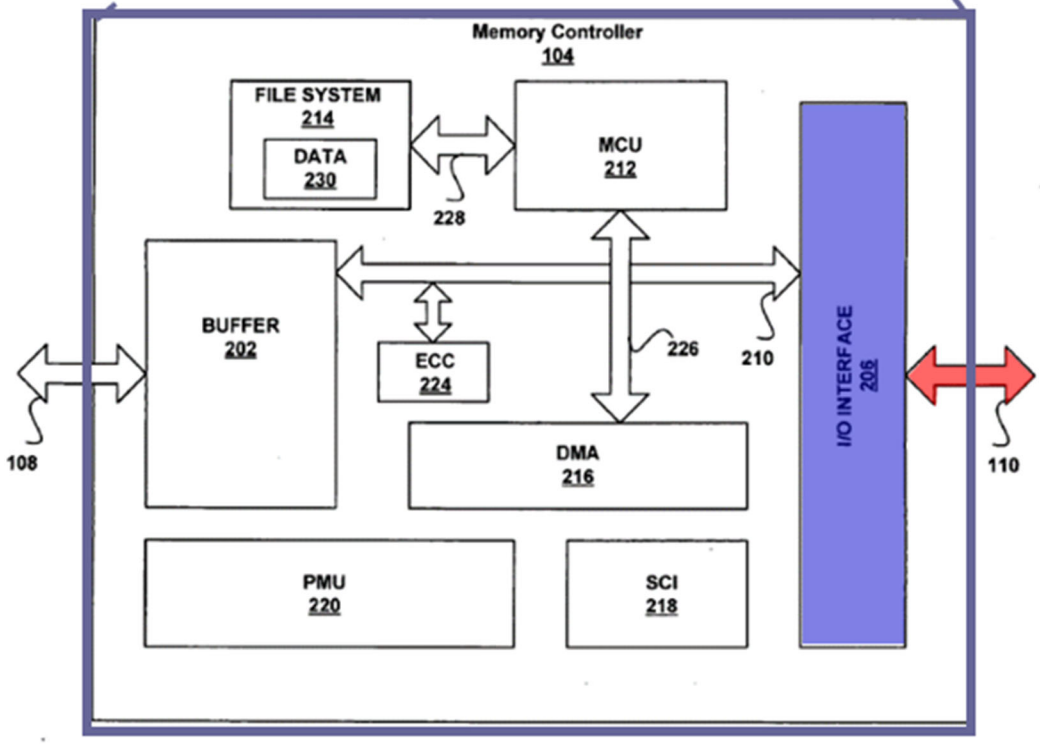


Figure 2

e. [Claim 59d]

Cornwell teaches that the MCU (interface controller) performs memory transactions by addressing a first memory location in a memory store. *Supra* § IX.A.7.d; Ex-1005, ¶ [0029] (the MCU "translates IDE/ATA commands into data

and control signals required for memory operations" and the "MCU firmware can translate signals from the host processor 102 into memory read and write operations"); Ex-1003, ¶¶ 288-293.

f. [Claim 59e]

Element [59e] is identical to element [1b] and is disclosed by Cornwell as discussed above. *Supra* § IX.A.1.c; Ex-1003, ¶¶ 294-296.

g. [Claim 59f]

Element [59f] is identical to element [1f] and is rendered obvious by Cornwell as discussed above. *Supra* § IX.A.1.g; Ex-1003, ¶¶ 297-301.

h. [Claim 59g]

Cornwell discloses identifying command details for causing the memory transaction to be performed, wherein said command details comprise the first memory device. *Supra* § IX.A.1.h; Ex-1003, ¶¶ 302-304. Cornwell further discloses that the interface controller (MCU 212) performs these functions. Ex-1005, ¶ [0029]; Ex-1003, ¶ 305.

i. [Claim 59h]

Element [59h] is substantially identical to element [1h] and is rendered obvious for the reasons discussed above. *Supra* § IX.A.1.i; Ex-1003, ¶¶ 307-312.

j. [Claim 59i]

Cornwell discloses obtaining the first set of attributes after identifying the

command details. *Supra* § IX.A.1.j; Ex-1003, ¶ 313. Cornwell also discloses that the interface controller (MCU 212) performs these functions. Ex-1005, ¶ [0029]; Ex-1003, ¶ 314.

k. [Claim 59j]

Cornwell discloses using attributes from a first device profile. *Supra* § IX.A.1.o; Ex-1003, ¶ 316. A POSITA would thus understand that Cornwell discloses this claim element. Ex-1003, ¶¶ 316-317.

l. [Claim 59k]

Element [59k] is identical to elements [1o] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.1.p; Ex-1003, ¶¶ 318-322.

11. Claim 71 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 71 is substantially identical to claim 5 and is obvious for the reasons discussed above. *Supra* § IX.A.2; Ex-1003, ¶¶ 324-326.

12. Claim 76 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 76 is substantially identical to claim 6 and is obvious for the reasons discussed above. *Supra* § IX.A.3; Ex-1003, ¶¶ 328-331.

13. Claim 80 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 80 pre]

To the extent the preamble is limiting, Cornwell discloses an electronic device

by teaching a memory management system in a "host system," which "can be ***any electronic or computing device*** that uses non-volatile memory, including but not limited to: flash drives, portable and desktop computers . . . ." Ex-1005, ¶¶ [0018] (emphasis added), [0081]-[0088]; Ex-1003, ¶¶ 333-335.

b. [Claim 80a]

Cornwell discloses a memory controller. *Supra* § IX.A.7.a. As illustrated below, Cornwell also explains that the **memory controller** is **coupled** (via bus 110) to the **first memory location** and a **second memory location**, explaining that "***one or more memory devices 106 receive signals from the memory controller 104 over Input/Output (I/O) bus 110***, which enables the memory devices 106 to perform memory access requests (e.g., read or write operations)." Ex-1005, ¶ [0024] (emphasis added); ¶ [0031]; Ex-1003, ¶¶ 336-339. Each of the memory locations also includes a **device profile** (device data 312). *Supra* § IX.A.1.c; Ex-1003, ¶ 340.

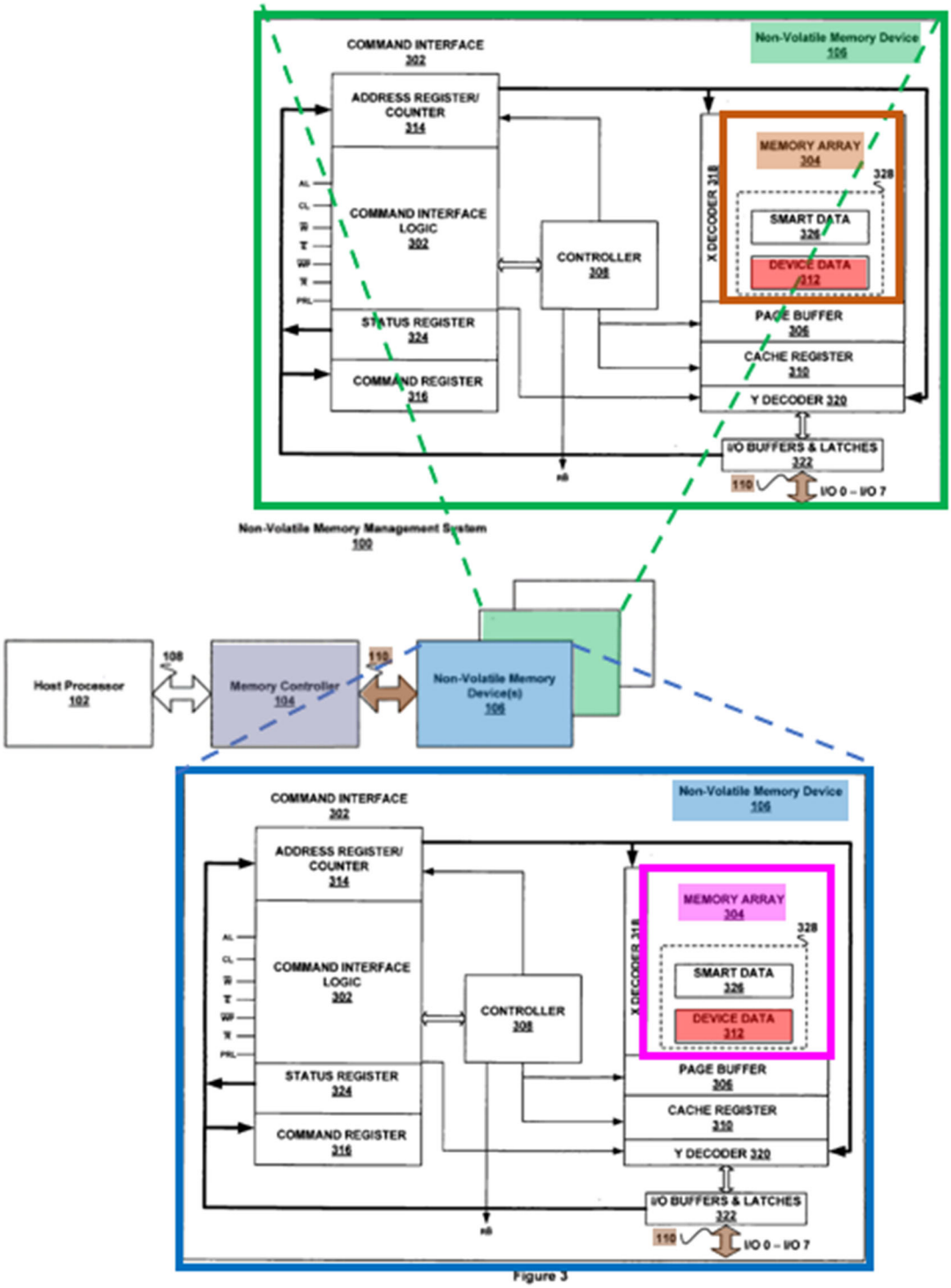


Figure 3

Ex-1003, ¶ 341.

c. [Claim 80b]

As illustrated below, Cornwell discloses the memory controller is directly coupled to the **host processor** while it addresses the **first memory location** or the **second memory location**, explaining that "the memory controller 104 recognizes control, address, and data signals transmitted on bus 108 by the host processor 102" and "translates the control, address and data signals into memory access requests on memory devices 106." Ex-1005, ¶¶ [0021], [0025]; Ex-1003, ¶¶ 343-345.

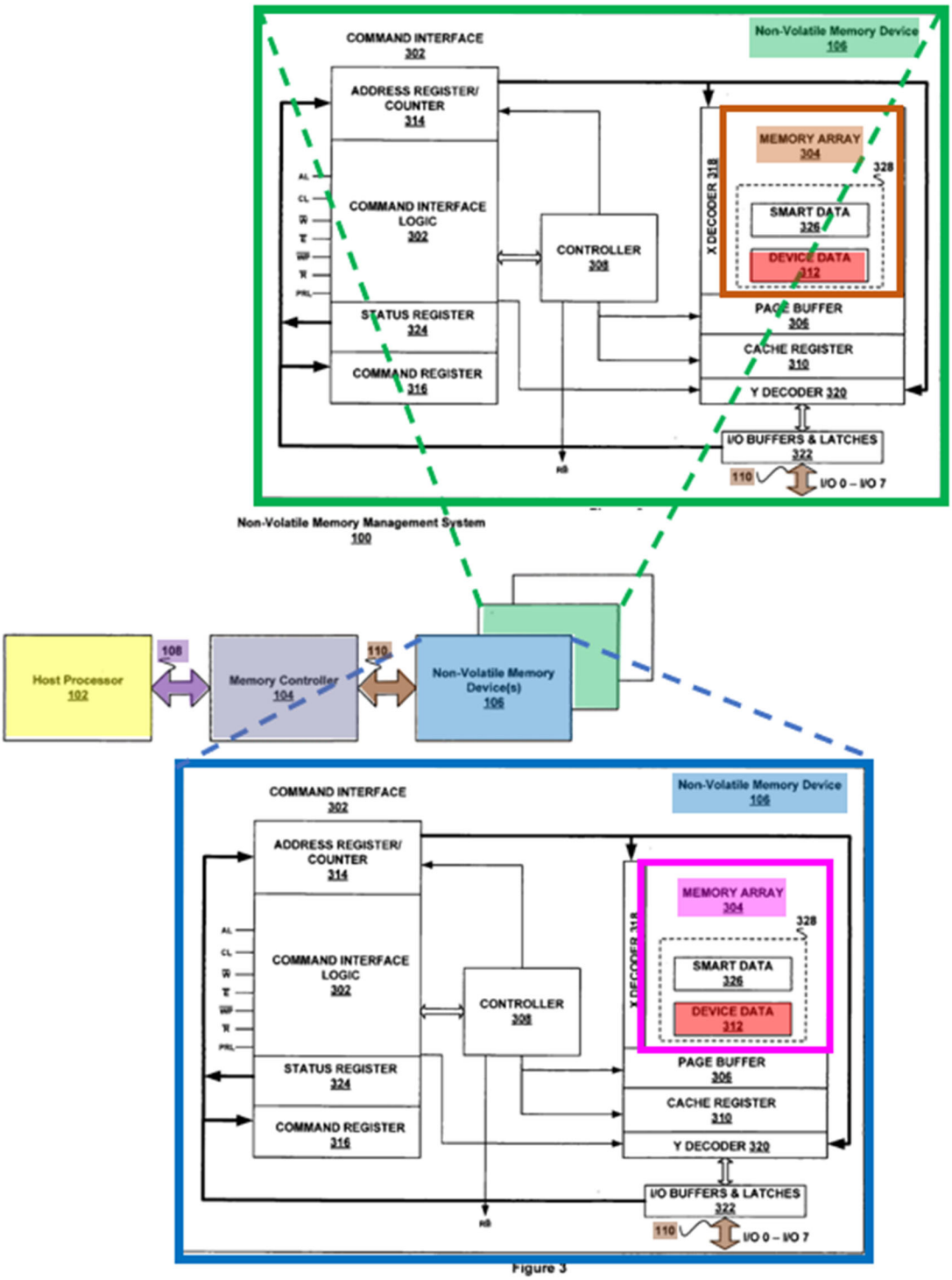


Figure 3

d. [Claim 80c]

Element [80c] is identical to element [1f] and is rendered obvious by Cornwell

as discussed above. *Supra* § IX.A.1.g; Ex-1003, ¶¶ 346-350.

e. [Claim 80d]

Cornwell discloses identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device. *Supra*, §§ IX.A.1.h; Ex-1003, ¶ 351. Cornwell further discloses that the interface controller (MCU 212) in the memory controller performs these functions. *Supra*, § IX.A.10.h; Ex-1003, ¶ 352.

f. [Claim 80e]

Element [80e] is substantially identical to elements [1h] and is obvious for the reasons discussed above. *Supra* § IX.A.1.i; Ex-1003, ¶¶ 354-359.

g. [Claim 80f]

Element [80f] is substantially identical to element [59i] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.10.j; Ex-1003, ¶¶ 360-361.

h. [Claim 80g]

Cornwell discloses using attributes from first and second device profiles. *Supra* § IX.A.1.o; Ex-1003, ¶ 362. Cornwell further discloses that these functions are performed by a memory controller: "device data 312 can be transmitted to the memory controller 104 . . . ***in response to a read command*** issued by the by the memory controller" and "***used by the memory controller 104 and/or host system*** to perform various memory management tasks." Ex-1005, ¶ [0043] (emphasis added);

[0042], [0046], [0058]; Ex-1003, ¶ 362.

i. [Claim 80h]

Cornwell discloses a memory controller selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes. *Supra* §§ IX.A.1.p; Ex-1003, ¶¶ 364-368.

14. Claim 84 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 84 is substantially identical to claim 5 and is obvious for the reasons discussed above. *Supra* § IX.A.2; Ex-1003, ¶¶ 370-372.

15. Claim 85 is Obvious in View of Cornwell and a POSITA's Knowledge

Claim 85 is substantially identical to claim 6 and is obvious for the reasons discussed above. *Supra* § IX.A.3; Ex-1003, ¶¶ 374-377.

16. Claim 98 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 98 pre]

Element [98 pre] is identical to element [80 pre] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.a; Ex-1003, ¶¶ 379-381.

b. [Claim 98a]

Element [98a] is identical to element [80a] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.b; Ex-1003, ¶¶ 382-388.

c. [Claim 98b]

Element [98b] is substantially identical to element [80b] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.c; Ex-1003, ¶¶ 389-391.

d. [Claim 98c]

Element [98c] is identical to element [80c] and is rendered obvious by Cornwell for the reasons discussed above. *Supra* § IX.A.13.d; Ex-1003, ¶¶ 392-396.

e. [Claim 98d]

Element [98d] is identical to element [80d] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.e; Ex-1003, ¶¶ 397-399.

f. [Claim 98e]

Element [98e] is substantially identical to element [80e] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.f; Ex-1003, ¶¶ 400-402.

g. [Claim 98f]

Element [98f] is identical to element [80f] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.g; Ex-1003, ¶¶ 403-404.

h. [Claim 98g]

Element [98g] is substantially identical to element [80g] and is disclosed by Cornwell for the reasons discussed above. *Supra* § IX.A.13.h; Ex-1003, ¶¶ 405-406.

i. [Claim 98h]

Element [98h] is substantially identical to element [80h] and is disclosed by

Cornwell discloses for the reasons discussed above. *Supra* § IX.A.13.i; Ex-1003, ¶¶ 407-411.

B. Ground 2: Each of the Challenged Claims is Rendered Obvious by Ware in View of a POSITA's Knowledge

1. Claim 1 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 1Pre]

To the extent the preamble is limiting, Ware discloses "memory systems and methods" utilizing "a memory controller for a non-homogeneous memory system." Ex-1006 at 1:6-8. Ware's method is depicted in the "a non-homogeneous memory management process" of Figure 3 below. *Id*. at 11:62-63; Ex-1003, ¶ 414.

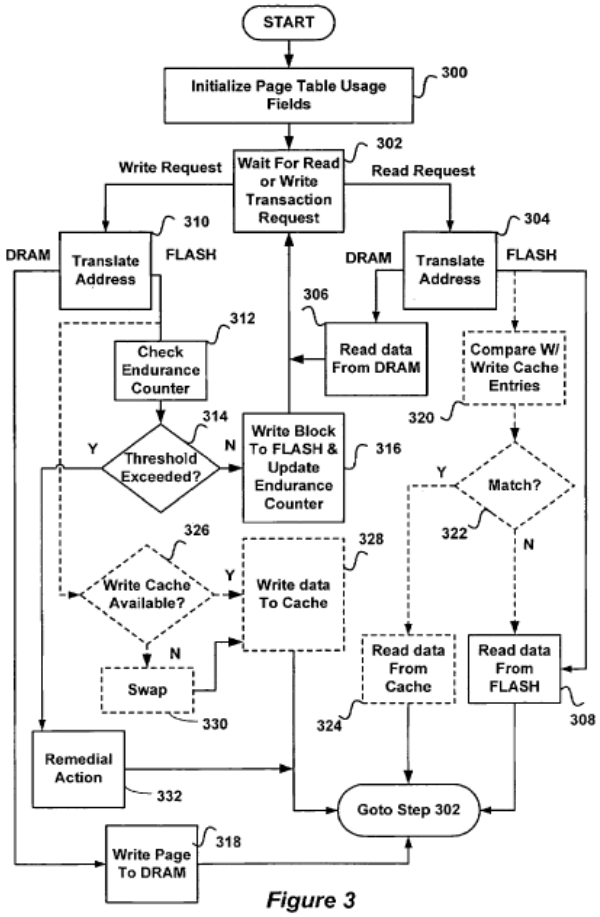


Figure 3

Ware further discloses that the memory may comprise multiple portions, including a "first portion 104 implemented with one or more memory devices of a first type (e.g., DRAM), and a second portion 106 implemented with one or more memory devices of a second type (e.g., NOR Flash, often simply called Flash memory)." Ex-1006 at 3:56-61, 5:57-61; Ex-1003, ¶ 415. As shown below in Annotated Figure 1, Ware also discloses performing a memory transaction on a **first memory location** (field value A in a **first memory portion 104**) and a **second memory location** (field value B in a **second memory portion 106**):

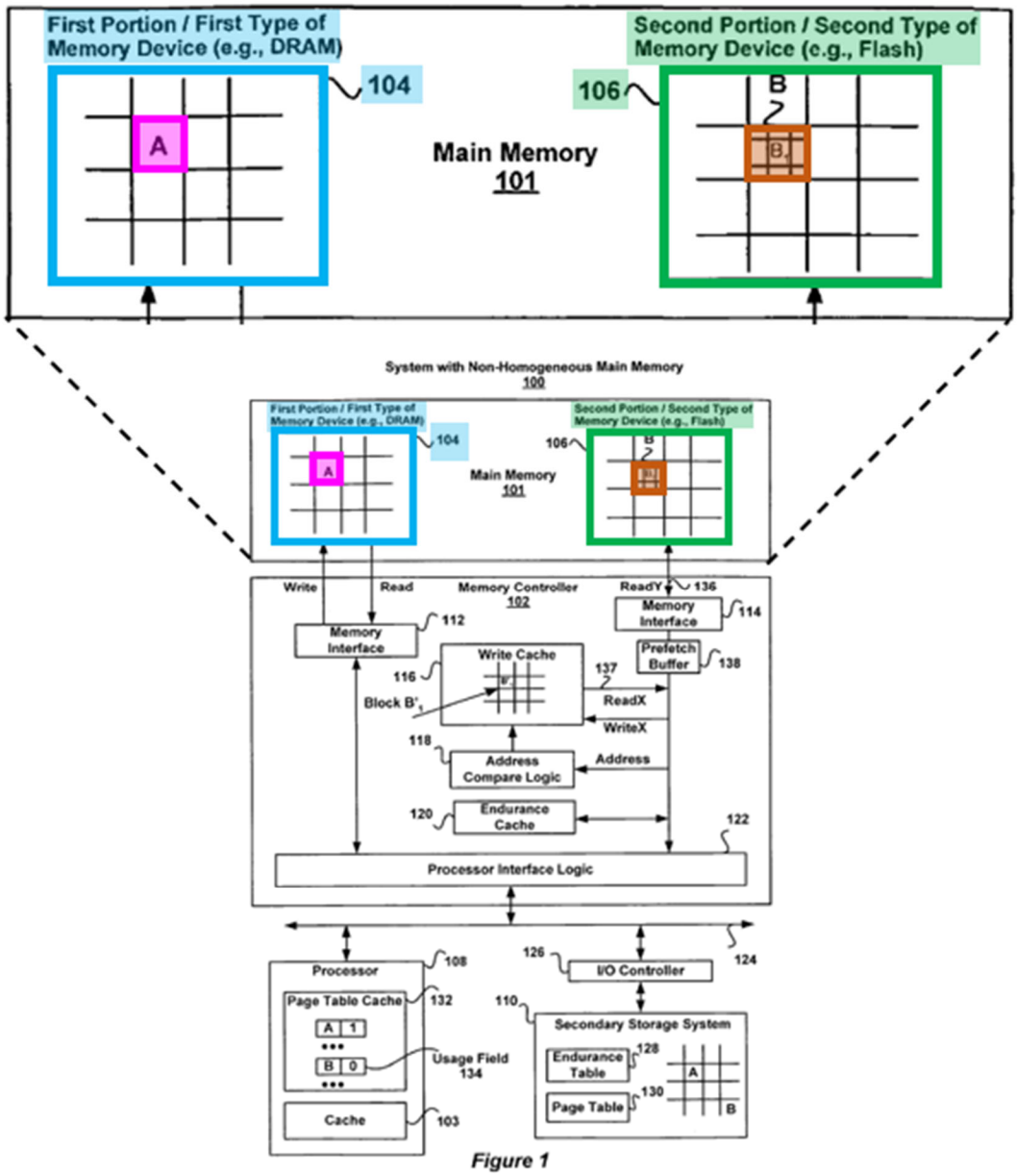


Figure 1

Ex-1003, ¶ 416.

b. [Claim 1a]

Ware discloses performing a memory transaction on the first (and second) memory location, explaining that "[d]ata can be distributed among the first and second portions 104, 106 of main memory 101." Ex-1006 at 3:64-67. The memory

transaction includes reading and writing information to and from a location characterized by a "usage field value of 'A,'" which "represents a page mapped to the first portion 104 of main memory"—i.e., the first memory location. *Id.*, 5:57-61. A POSITA would understand that performing such read and write transactions to the first memory location in the first memory device requires addressing that location. *Id.* at 7:22-25, 7:46-49; Ex-1003, ¶¶ 418-419.

Annotated Figure 1 depicts Ware's **memory store**, which comprises a **first memory location** (field value A in a **first memory portion 104**) addressed in a read or write transaction:

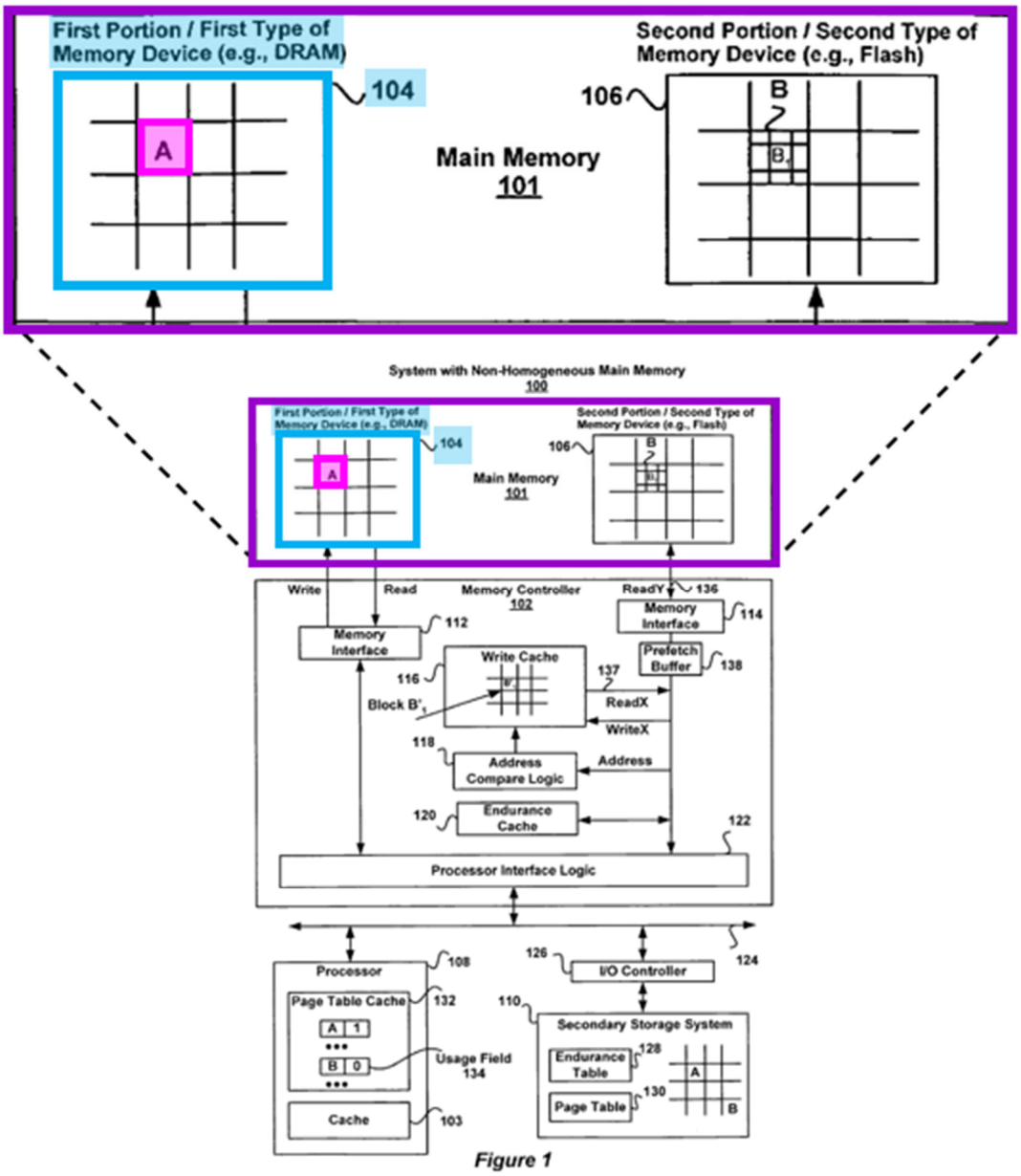


Figure 1

Ex-1003, ¶ 420.

c. [Claim 1b]

Ware discloses that each memory location is associated with a device profile consisting of a set of attributes, explaining that the first memory location is in a memory device of "a first memory type having a ***first set of attributes***," while the

second memory location is in a second memory device "of a second memory type having a ***second set of attributes***." Ex-1006, Abstract (emphasis added). Ware also discloses a "usage field 208" that "stores data indicative of the usage model of the page, which can be used by processor 210 to exploit the ***unique attributes of a physical memory device associated with the main memory address space 212***." *Id.* at 11:1-4 (emphasis added); 11:19-23, Fig. 2; Ex-1003, ¶ 422.

Ware's **device profile** (i.e., the usage field used to store a first and second sets of attributes), which is associated with both the **first memory location** (in the first memory device) and the **second memory location** (in the second memory device), is shown below in annotated Figure 2:

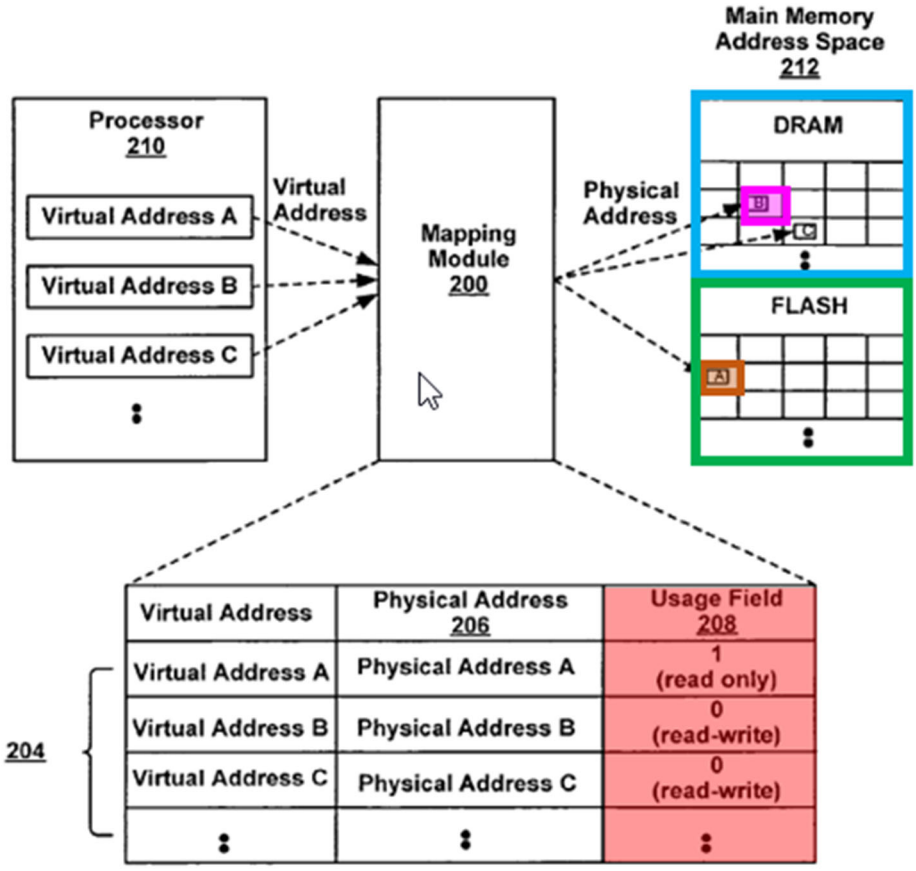


Figure 2

Ex-1003, ¶ 423.

d. [Claim 1c]

As described above and shown below in annotated Figure 1, the **second memory location** (usage field "B") is in the **second memory device** (second portion 106) in the **memory store**. *Supra*, § IX.B.1.c; Ex-1003, ¶ 425.

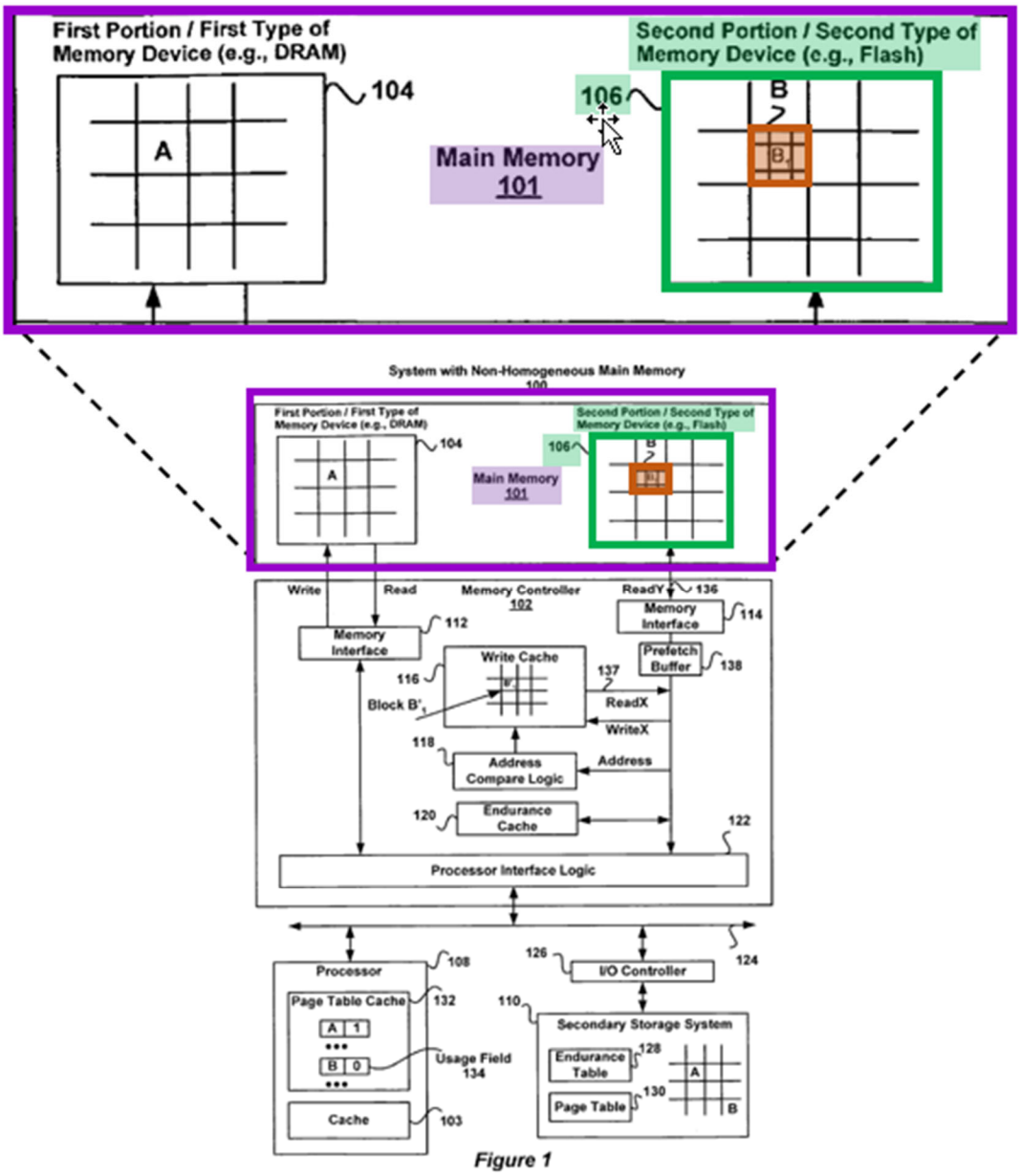


Figure 1

e. [Claim 1d]

Ware discloses that "the memory controller waits 302 for a read or write transaction request." Ex-1006 at 12:13-14. For example, if the request indicates that the data should be read from the first memory location ("first portion" or DRAM), "then the data . . . ***is read at step 306 from DRAM*** and returned to the requestor."

Id. at 12:20-22. If the request indicates that data should be written to first memory location, "then ***the write data is written to DRAM*** at step 318." *id*. at 12:43-44 (emphasis added), 2:30-36. Accordingly, Ware teaches that a memory read transaction (read request) and memory write transaction (write request) are performed on a first memory. Ware also teaches reading and writing to the second location in flash memory. *Id*. at 7:55-67; 8:24-28; 9:48-57; Ex-1003, ¶¶ 427-428.

Annotated Figure 1 illustrates read and write transactions being performed on either a **first memory location** (in DRAM) or a **second memory location** (in Flash memory):

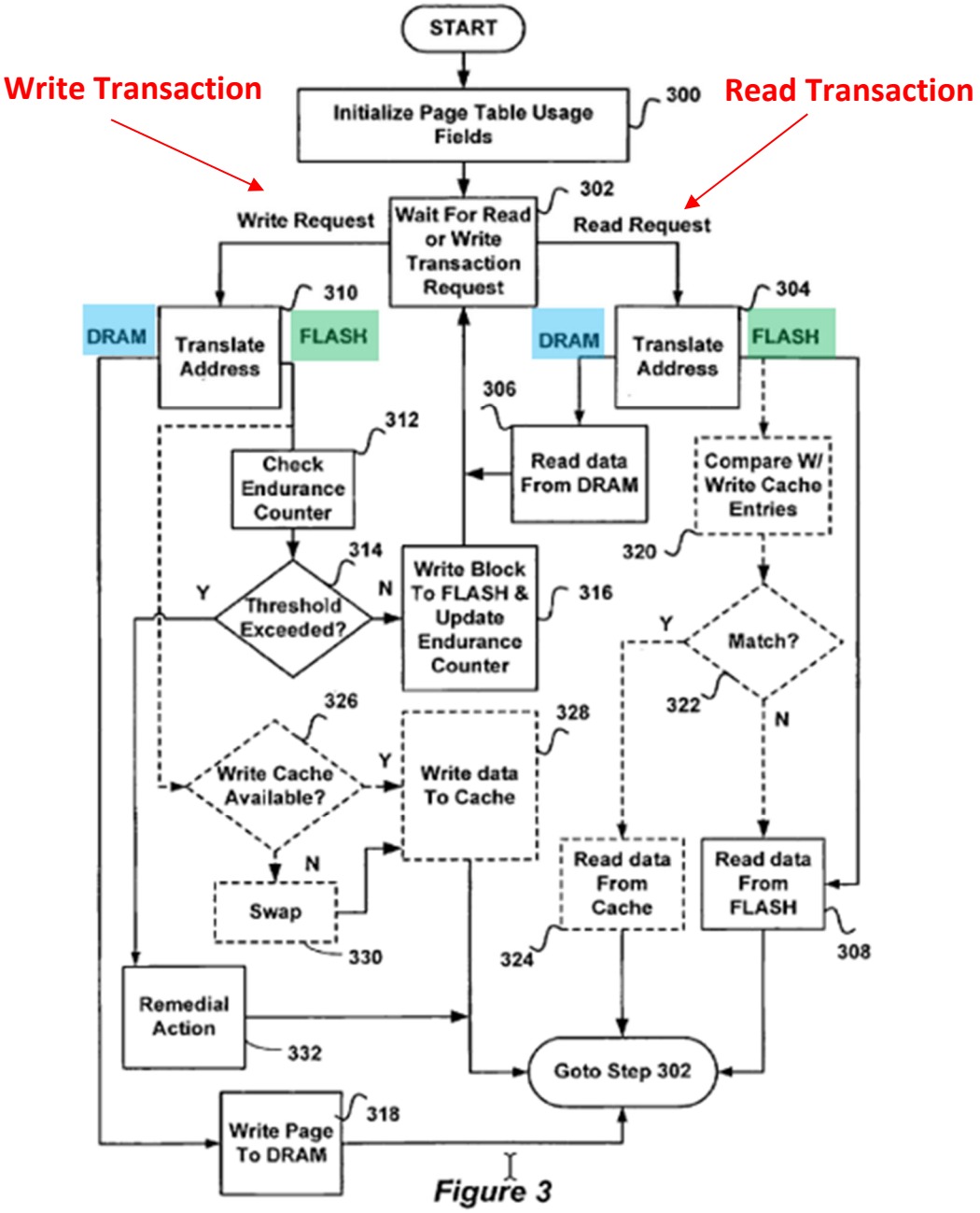


Figure 3

Ex-1003, ¶ 429.

f. [Claim 1e]

As explained above, Ware discloses that data is read from a first or second memory location in a read transaction and is written to a first or second memory

location in a write transaction. *Supra* § IX.B.1.e. Ware further discloses that data is transferred to and from the host and first/second memory locations during read/write transactions, explaining that "programs and data used by [host] processor 108" are stored in the main memory, comprised of the first/second memory locations. Ex-1006 at 3:61-63; 3:39-44 7:9-10; Ex-1003, ¶ 431.

Annotated Figure 1 below illustrates the data transfer to and from the **host processor** (processor 108) over bi-directional **bus 124** and **communication paths** to and from the **first memory location** (usage field "A") and **second memory location** (usage field "B"):

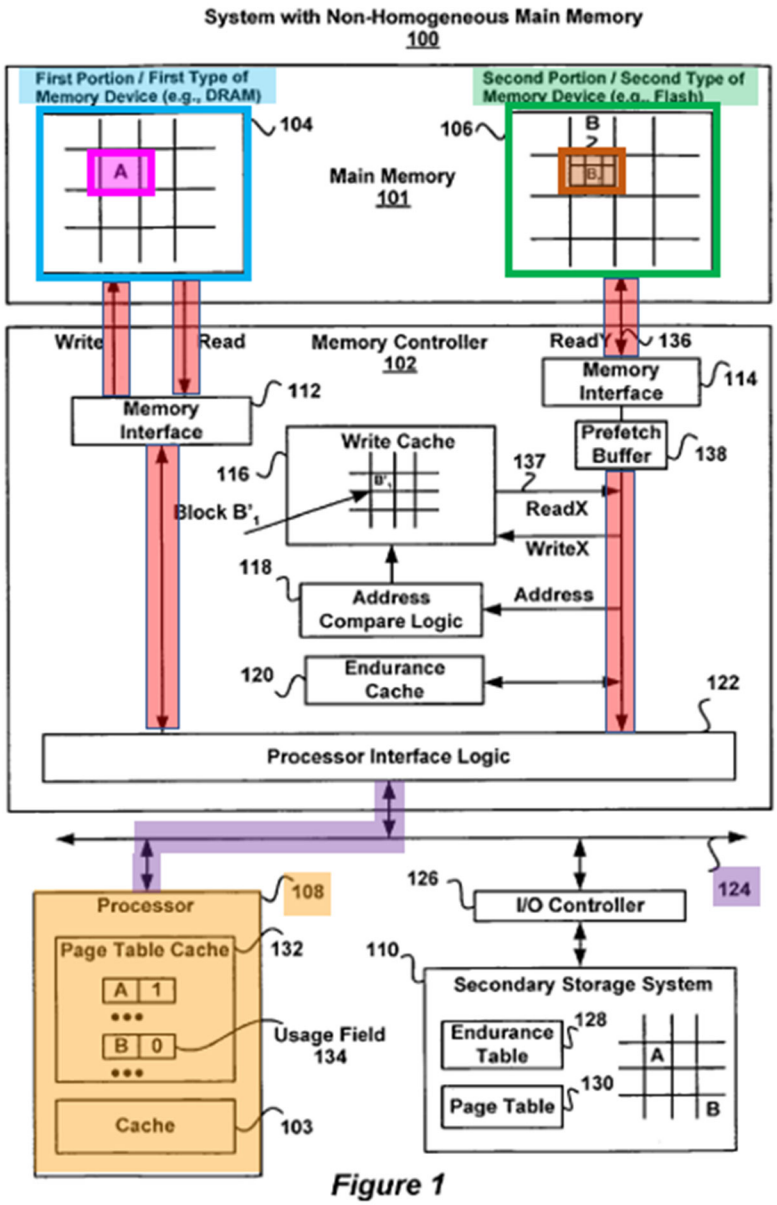


Figure 1

Ex-1003, ¶ 432.

g. [Claim 1f]

Ware discloses a first memory location comprising DRAM having a device profile and a second memory location comprising a flash device with a device profile. *Supra*, § IX.B.1.c. Ware also teaches that DRAM "has a near-***optimal***

combination of operational attributes"—or device profile—"for implementing main memory." Ex-1006 at 1:65-2:6 (emphasis added); 11:1-4. For example, a POSITA would understand that a random read command results in accessing a byte of data at some random location in the memory, and that a device profile for DRAM would be optimal for this random data type. Ex-1003, ¶ 434. A POSITA would similarly understand that flash memory utilizes page read commands that result in sequentially accessing bytes of data located in a row location (page) of the memory and that, as a result flash memory would have a device that is optimal for a sequential data type. *Id*., ¶ 434 & n.34.

h. [Claim 1g]

As explained above, Ware teaches read/write transactions. *Supra* § IX.B.1.e*; see also* Ex-1006 at 12:12-14. Ware further teaches that performing read/write transactions requires "translating" addresses, "reading the usage field" for the page, and determining from the usage field whether the data should be read/written from or to DRAM or flash. Ex-1006 at 12:17-22; 12:38-45. A POSITA would thus understand that command details would be required for executing these steps of a read or write request, and further that Ware requires identifying command details that identify or comprise the first memory location. Ex-1003, ¶¶ 436-440.

i. [Claim 1h]

Ware discloses that both the first memory location (field value A in a first

memory portion 104) and second memory location (field value B second memory portion 106) have sets of attributes comprising a device profile. *Supra* § IX.B.1.c. Ware further teaches that "[t]he memory devices in portion 104 have one or more ***attributes that differ*** from the attributes of the memory devices in portion 106." Ex-1006, 4:4-9 (emphasis added), Abstract, 2:21-25, 4:19-29, claim 15; Ex-1003, ¶¶ 441-442. Accordingly, Ware teaches that a "difference exists" between the first/second device profiles.

j. [Claim 1i]

Ware discloses identifying command details for causing a memory transaction. *Supra*, §§ IX.B.1.h. Ware further discloses that the first set of attributes are obtained after the command details are identified. As shown below, Ware teaches that once it has been determined that a transaction request is a write request at step 302 (which requires identifying command details), ***then*** a virtual address is "translated into a physical address at step 310, which once again includes reading the usage field for the page containing the specified address." Ex-1006 at 12:38-41, 12:41-45; 11:1-4. As a result, a POSITA would understand that after the **command details are identified** in step 302—the address is translated in step 310, which requires **obtaining the set of attributes**:

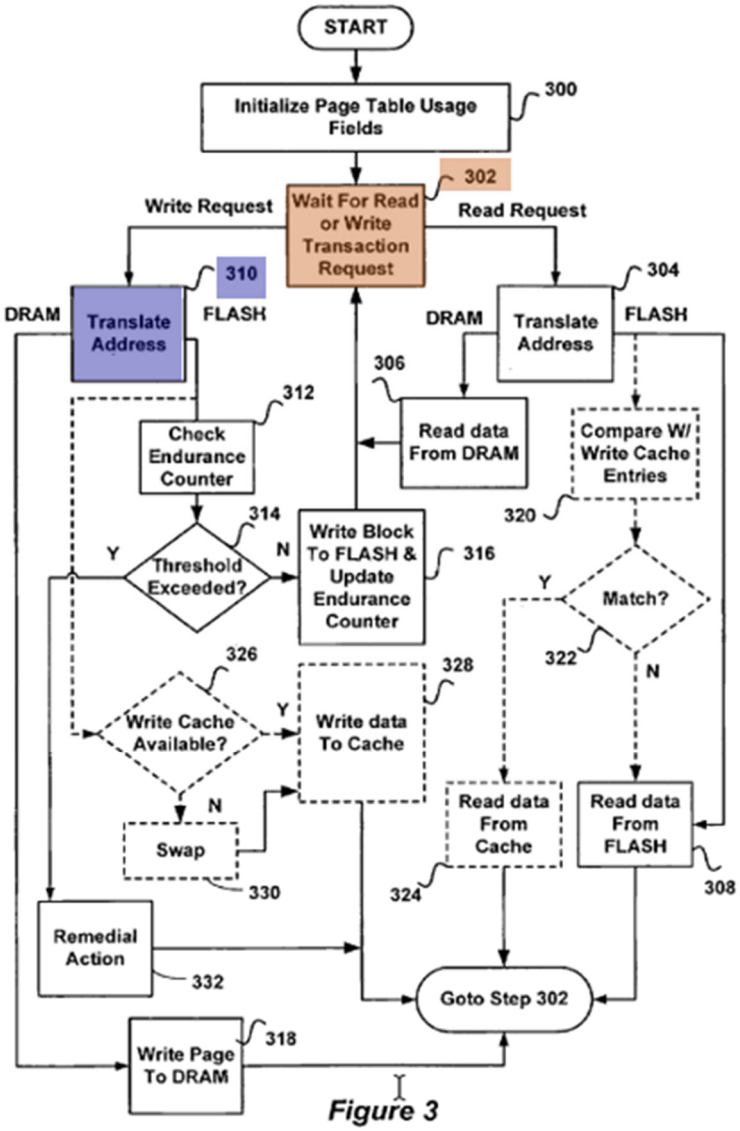


Figure 3

Ex-1003, ¶¶ 443-445.

k. [Claim 1j]

Ware discloses that "[t]he memory devices in portion 104 have one or more attributes that differ from the attributes of the memory devices in portion 106," such as "the ratio of write access time to read access time, volatility, and endurance." Ex-1006 at 4:6-11. Ware also discloses attribute qualifiers for such attributes by, for

example, teaching that in a NOR flash device "the ratio of write access time to read access time may exceed 10,000 to 1, and will typically be greater than 100 to 1." *Id*. at 4:19-24. This attribute differs from DRAM, in which the ratio of write access time to read access time "is generally less than 4 to 1, and is typically less than 2 to 1." *Id*. at 4:29-31. These numerical ratios are qualifiers for the write-to-read access time attribute of each memory location. Ex-1003, ¶ 446.

A POSITA would also have known that memory attributes, like those described in Ware, comprise a "qualifier" to describe the attribute, such as the value of the attribute or the type of the attribute. *Id.* A POSITA would also understand that attribute qualifiers for the "volatility" attribute would be yes/no (1/0 indicating whether the memory is volatile or non-volatile), while the attribute qualifier for endurance would be a numerical representation of program/erase cycles the memory could endure before the memory becomes unreliable. *Id*., ¶ 447.

As a result, "attribute qualifiers," including values representing the ratio of write time to speed time, volatility, and endurance, would have been well known and readily available—and thus obvious—to a POSITA based on Ware in view of a POSITA's knowledge. *Id.*, ¶ 448.

l. [Claim 1k]

Ware discloses that at least one memory bus is directly coupled to both the memory store and controller, explaining "[t]he memory controller 102 includes

memory interfaces 112, 114 for ***coupling the memory controller 102 to the memory devices*** in two or more distinct portions (104, 106) of main memory 101." Ex-1006 at 7:21-29; Abstract; claim 1. Ware further teaches that the controller performs read/write transactions by "transmitting addresses, data, and control signals to and from the memory devices in main memory portions 104 and 106." *Id*., 7:21-29; Abstract; 12:12-64; claim 1; Ex-1003, ¶¶ 450-452.

Annotated Figure 1 illustrates that the **memory store** (main memory 101) is directly coupled to the **memory controller** (memory controller 102) via **communication paths**, which a POSITA would understand as encompassing a memory bus:

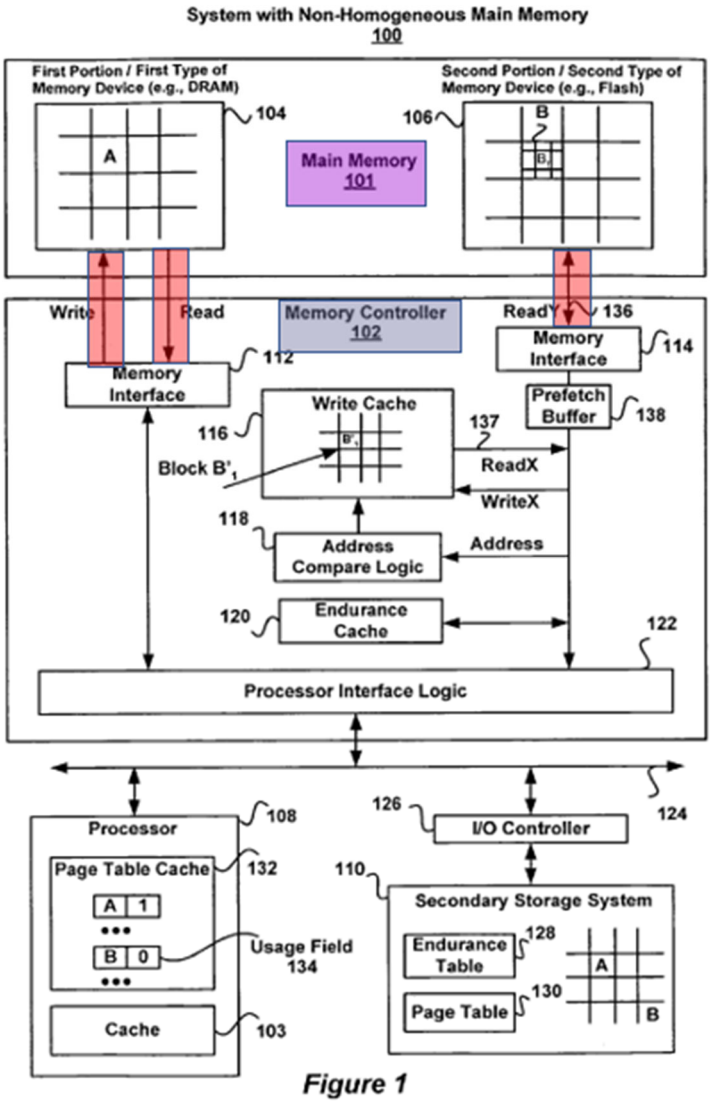


Figure 1

Ex-1003, ¶ 451.

m. [Claim 1l]

Ware teaches that a host "***processor 108 is coupled to the memory controller*** 102 via bus 124 and processor interface logic 122." Ex-1006 at 7:9-10 (emphasis added). Ware further demonstrates that the host processer is coupled to the memory controller during a read/write transaction since the "main memory 101 stores

programs and data used by processor 108 during execution of those programs." *Id.*, 3:61-63, 7:46-49; *supra* § IX.B.1.l; Ex-1003, ¶¶ 454-455. Annotated Figure 1 further illustrates the **host processor** (processor 108) directly coupled to the **memory controller** (memory controller 102) via **bus 124** during read/write transactions:

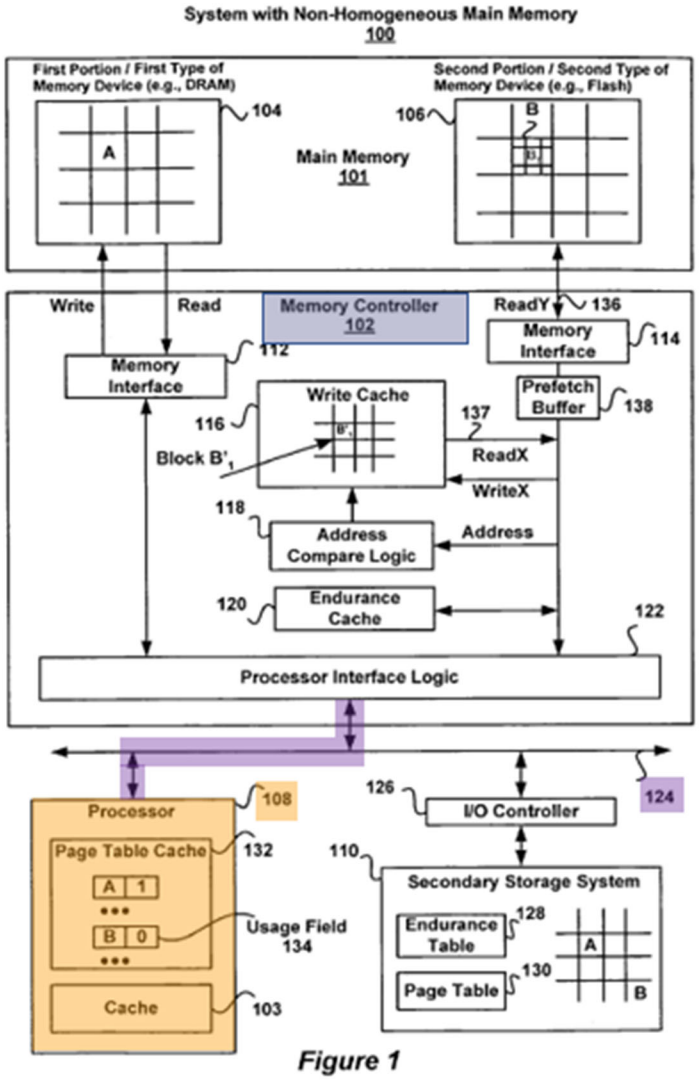


Figure 1

Ex-1003, ¶ 455.

n. [Claim 1m]

Ware teaches device profiles in the form of "usage fields." *Supra* § IX.B.1.c. Ware further discloses that these fields may be stored in the memory store, explaining that usage data may be kept "in the first portion 104 of main memory" and that the usage field "of each page in a main memory 101 can be set based on the accumulated usage data." Ex-1006 at 11:50-55. Thus, Ware teaches that the usage fields (e.g., first device profile and second device profile) in step 300 in Figure 3 are transferred from secondary storage to the memory store (main memory 101) during initialization. Ex-1003, ¶ 457.

o. [Claim 1n]

Ware teaches that the first and second device profiles (i.e., usage fields) include a number of attributes. *Supra* § IX.B.1.i; Ex-1006 at 5:65-6:7. Ware also teaches using these attributes. Ex-1003, ¶ 458. As described above, for example, Ware teaches using the write-to-read access time attribute. *Id.*; *supra* § IX.B.1.k. Ware also teaches using the endurance attribute, noting that certain devices have limited endurance while other have unlimited endurance. Ex-1006 at 2:41-48. Accordingly, Ware's system "keep[s] track of the number of write operations" and checks the write count prior to performing a write transaction "to ensure that the endurance limit of the device is not exceeded." *Id*. at 6:15-20, 28-41. Ware teaches that other measures can also be "employed to ensure that the endurance limitation[s]

of the memory devices . . . are not exceeded," including through remapping. *Id*. at 6:59-66; Ex-1003, ¶ 459.

Ware also teaches a device granularity attribute, noting that different devices have "different granularity for read and write operations." Ex-1006 at 5:65-66. A POSITA would have understood that granularity is the minimum unit for read and write operations, thus resulting in the need to use the device granularity attribute in a memory transaction. Ex-1003, ¶¶ 460-461. As a result, Ware in view of a POSITA's knowledge renders obvious using attributes from the first and second device profiles. *Id*.

p. [Claim 1o]

As explained above, Ware teaches that different devices have different granularity, resulting in the need to select a transfer size for read/write transactions. *Supra* § IX.B.1.o. For example, a POSITA would have understood that flash memory can be written in pages, Ex-1006 at 6:9-12, and that a page is the number of bits in a row of data in flash memory that can be transferred during a memory transaction, and that page size is an attribute. Ex-1003, ¶¶ 463-464. Ware further teaches that a page may be "of a different size than a block in a Flash memory device" and thus may be stored in a plurality of blocks, or one block could store multiple pages, or each page could be stored in a single block." Ex-1006 at 6:9-14 (emphasis added). As a result, a POSITA would understand that the transfer size

(granularity) would be a function of the data size of the transaction and the first set of attributes. Ex-1003, ¶ 464.

2. Claim 5 is Obvious in View of Ware and a POSITA's Knowledge

As explained above, Ware teaches that shared attributes for the first and second device profiles—which include write-to-read access time ratio, volatility, and endurance—are different. *Supra* § IX.B.1.k; Ex-1006 at 4:6-11; 3:19-30; Ex-1003, ¶ 468. For example, a POSITA would have understood that the volatility attribute qualifier for DRAM (memory portion 104) is "volatile," while the qualifier for Flash (memory portion 106) is "non-volatile." Ex-1003, ¶ 469; Ex-1006 at 3:10-12; 30-33; 3:18:30. Likewise, a POSITA would understand the attribute "endurance" would have an attribute qualifier of "unlimited" for DRAM and "limited" for Flash. Ex-1006, 3:18-30; Ex-1003, ¶ 469; *supra* §§ IX.B.1.k, IX.B.1.o. Ware also teaches that qualifiers for the write-to-read access time ratio are different, noting that the ratio will "typically be greater than 100 to 1" for NOR flash, but will "is generally less than 4 to 1, and is typically less than 2 to 1" for DRAM. Ex-1006 at 4:19-24; 4:29-31; Ex-1003, ¶ 469.

As a result, different attribute qualifiers for at least one set of shared attributes, would have been well known and readily available—and thus obvious—to a POSITA based on Ware in view of a POSITA's knowledge. Ex-1003, ¶¶ 467-470.

3. Claim 6 is Obvious in View of Ware and a POSITA's Knowledge

It would have been obvious to a POSITA that the "volatility" attribute would have different values for "volatile" and "non-volatile" memory. For example, a POSITA would have recognized that volatility would be represented by either a 1 or 0, demonstrating that the memory is either volatile or non-volatile. *Supra* §§ IX.B.2, IX.B.1.k; Ex-1003, ¶ 473. Likewise, as explained above, "endurance" attribute would have different attribute values, such as the number of read/write cycles. *Supra* § IX.B.2; Ex-1003, ¶ 473.

As a result, different attribute values for attribute qualifiers would have been well known and readily available—and thus obvious—to a POSITA based on Ware in view of a POSITA's knowledge. Ex-1003, ¶¶ 472-474.

4. Claim 29 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 29 pre]

To the extent the preamble is limiting, Ware teaches this claim element. As discussed above, Ware discloses a method of performing memory transactions on a first and second memory location. *Supra* § IX.B.1.a; Ex-1003, ¶¶ 476-478. A POSITA would readily understand that the executable instructions for performing this method would be stored on a computer readable medium. Ex-1003, ¶¶ 479-481.

For example, Ware teaches that the system in which the method is performed

comprises storage that can be "any type of file storage device" such as "hard disk units, optical disks, Universal Serial Bus (USB) Flash . . . and any other file storage device." Ex-1006 at 4:61-5:1. A POSITA would have readily understood that these devices comprise a non-transitory computer readable medium. Ex-1003, ¶ 479. Indeed, Ware discloses that such non-transitory computer readable medium is used for "storing various forms of programs (e.g., source, object, ***executable***)…." Ex-1006 at 5:3-6 (emphasis added); 1:25-26; 5:9-12. The secondary storage can also "store[] computer programs and data, including an operating system 410." *Id*. at 10:33-37. A POSITA would have also understood that the operating system would comprise computer readable instruction adapted to perform the recited method. Ex-1003, ¶ 480.

b. [Claim 29a]

The recited features of element [29a] are substantially identical to those of elements [1a] and [1b] and are disclosed by Ware for the reasons discussed above. *Supra* §§ IX.B.1.b, IX.B.1.c; Ex-1003, ¶¶ 483-488.

c. [Claim 29b]

Element [29b] is identical to element [1f] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.g; Ex-1003, ¶¶ 489-490.

d. [Claim 29c]

Element [29c] is identical to element [1g] and is disclosed by Ware for the

reasons discussed above. *Supra* § IX.B.1.h; Ex-1003, ¶¶ 491-495.

e. [Claim 29d]

Element [29d] is identical to element [1h] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.i; Ex-1003, ¶¶ 496-497.

f. [Claim 29e]

Element [29e] is identical to element [1i] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.j; Ex-1003, ¶¶ 498-500.

g. [Claim 29f]

Element [29f] is identical to element [1n] and is rendered obvious for the reasons discussed above. *Supra* § IX.B.1.o; Ex-1003, ¶¶ 501-504.

h. [Claim 29g]

Element [29g] is identical to element [1o] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.p; Ex-1003, ¶¶ 505-507.

5. Claim 36 is Obvious in View of Ware and a POSITA's Knowledge

Claim 36 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.B.2; Ex-1003, ¶¶ 509-512.

6. Claim 37 is Obvious in View of Ware and a POSITA's Knowledge

Claim 37 is substantially identical to claim 6 and is obvious for the reasons discussed above. *Supra* § IX.B.3; Ex-1003, ¶¶ 514-516.

7. Claim 45 is Obvious in View of Cornwell and a POSITA's Knowledge

a. [Claim 45 pre]

To the extent that the preamble is limiting, Ware discloses "a memory controller for a non-homogenous memory." Ex-1006 at 1:7-8; 2:18-21; 7:21-25; claim 1. The memory controller performs memory transactions, such as read/write transactions, and "can be configured to exploit the different attributes of the memory device types in the respective portions of main memory so as to improve one or more aspects of memory system performance." *Id*., 2:47-52; 12:4-64; claim 1; claim 7; Ex-1003, ¶¶ 518-521.

b. [Claim 45a]

Ware discloses the first recited function of "performing a memory transaction" as well as a "memory controller" for performing the function pursuant to Petitioner's proposed construction. For example, Ware discloses "a memory controller for a non-homogenous memory," which "direct[s] memory transactions" to first and second memory interfaces. Ex-1006, Abstract; 1:7-8; 7:49-54; Ex-1003, ¶¶ 522-525.

Ware also discloses the second recited function of "addressing a first memory location," teaching components and functionality "for transmitting ***addresses, data, and control signals to and from the memory devices*** in main memory portions 104

and 106." Ex-1006 at 7:25-29 (emphasis added); 7:46-54; 12:3-64. Ware further demonstrates that this function is performed by Petitioner's proposed structure of "a memory device interface, a host interface, an interface controller or similar structure configured to process memory transaction requests, and associated communication pathways." *Supra* § VII.C. In particular, Ware states that processor interface logic (an interface controller, as explained below) "include[s] signal conditioning circuitry and other devices for transmitting data, ***addresses*** and control signals to and from bus 124." *Id*. at 7:46-49 (emphasis added). Likewise, memory interfaces 112 and 114 "include signal conditioning circuitry and other devices for transmitting addresses, data, and control signals to and from memory devices." *Id*. at 7:25-29; Ex-1003, ¶¶ 526-530.

Petitioner's proposed structure of a **memory device interface**, a host interface that is part of an **interface controller** (processor interface logic, as explained below), and **associated communication pathways** are shown in annotated Figure 1:

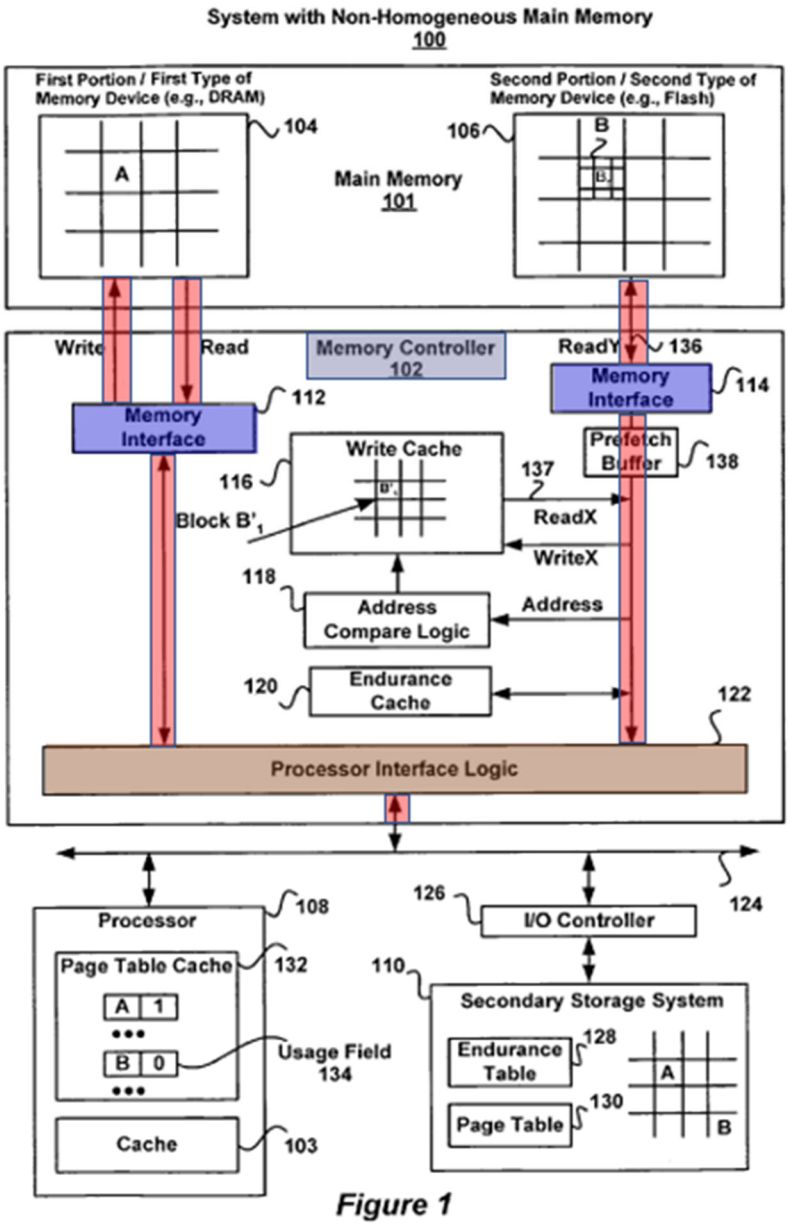


Figure 1

Ex-1003, ¶ 529.

c. [Claim 45b]

Ware discloses that the means for addressing is directly coupled to the first and second memory locations: "The memory devices in the first and second portions 104, 106 of main memory are coupled to the memory controller 102 via memory

interfaces 112 and 114, respectively." Ex-1006 at 4:4-6. Ware also discloses that memory is coupled through path 136 "to the bus 124 via the processor interface logic 122." *Id*. at 7:9-10, 45-46; Ex-1003, ¶¶ 532-533. Annotated Figure 1 demonstrates that the **memory interfaces** (which are part of the means for addressing) are **directly coupled** to the **first memory location** (in first memory device 104) and the **second memory location** (in second memory device 106):

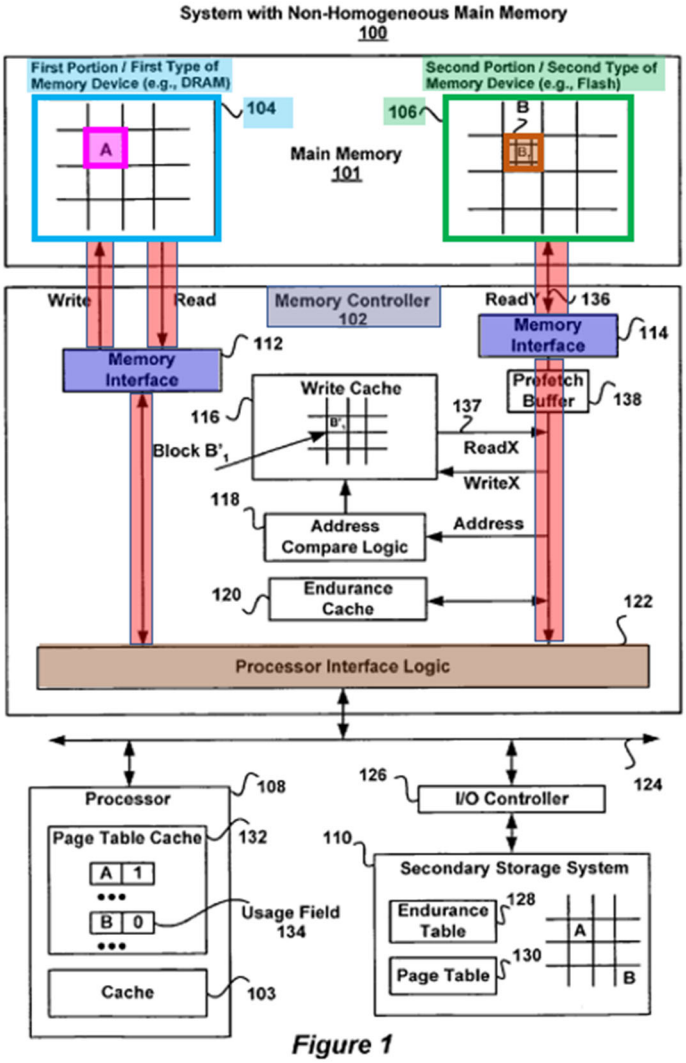


Figure 1

Ex-1003, ¶ 533.

d. [Claim 45c]

Ware discloses the recited function of "processing memory transaction requests," as well as Petitioner's proposed structure of an interface controller or equivalent structure for processing memory transaction requests. Ware discloses "processor interface logic 122" that "may include signal conditioning circuitry and other components for transmitting data, addresses and control signals to and from the bus 124." Ex-1006 at 7:46-49. The processor interface logic also "may include decoding logic for decoding one or more bits of a physical address to determine whether the first or second portion of main memory will receive a memory access transaction." *Id*. at 7:49-54. Accordingly, as illustrated in Annotated Figure 1, "**processor interface logic 122**," which is part of the addressing means, is an interface controller or equivalent structure for processing memory transaction requests. Ex-1003, ¶¶ 535-538.

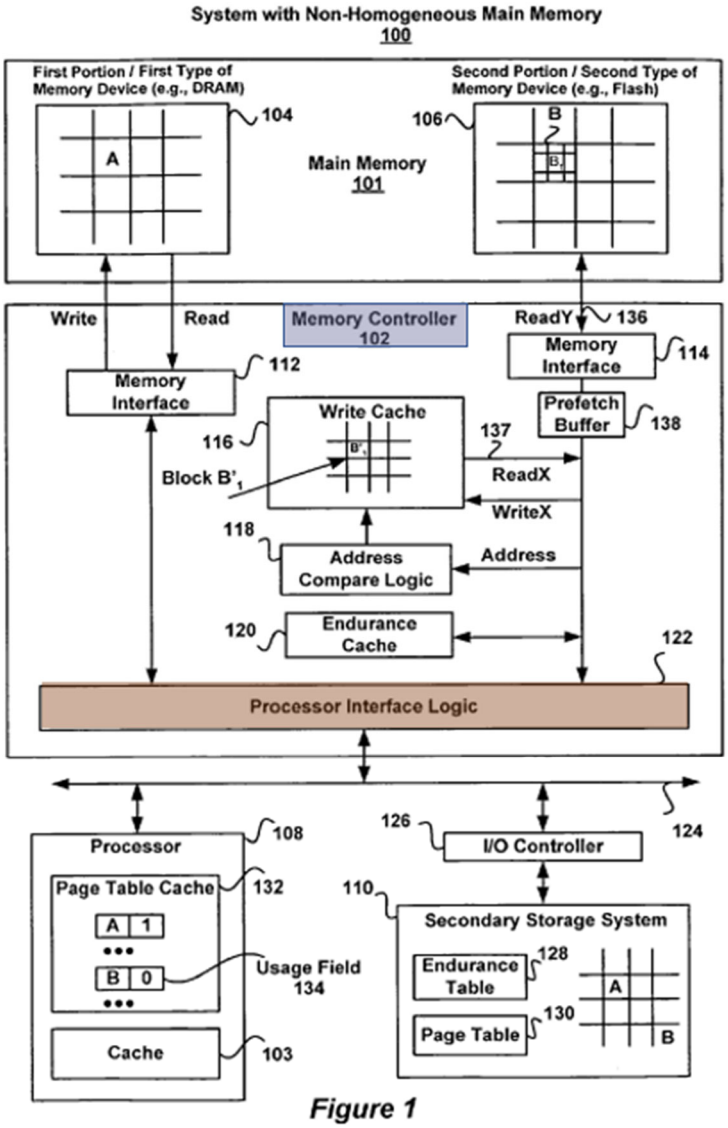


Figure 1

e. [Claim 45d]

As illustrated below, Ware demonstrates the means for addressing—i.e., the **memory device interfaces**, a host interface that is part of an **interface controller** (processor interface logic), and **associated communication pathways**—is **directly coupled** (via bus 124) to the **host processor** as the **first** or **second** memory location are addressed:

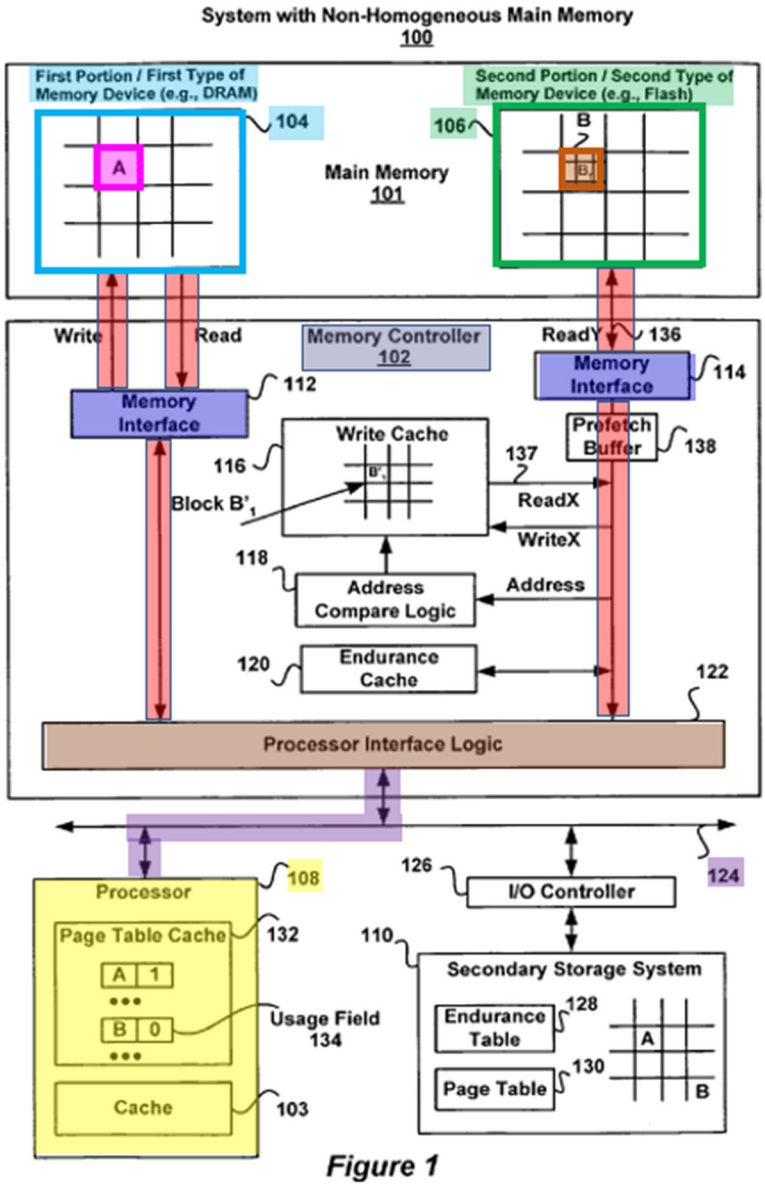


Figure 1

See also Ex-1006 at 7:9-10 (disclosing that the host "processor 108 is coupled to the memory controller 102 via bus 124 and processor interface logic 122"); Ex-1003, ¶¶ 539-542.

f. [Claim 45e]

Element [45e] is identical to element [1f] and is disclosed by Ware for the

reasons discussed above. *Supra* § IX.B.1.g; Ex-1003, ¶¶ 543-544.

g. [Claim 45f]

Element [45f] is identical to element [1g] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.h; Ex-1003, ¶¶ 545-549.

h. [Claim 45g]

Element [45g] is identical to element [1h] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.i; Ex-1003, ¶¶ 550-551.

i. [Claim 45h]

Ware discloses obtaining the first set of attributes after identifying the command details. *Supra* §§ IX.B.1.j; Ex-1003, ¶ 552. Ware also teaches that this operation is performed by the interface controller (processor interface logic 122)—which is part of the means for addressing—explaining, for example, that the processor interface logic 122 "may include signal conditioning circuitry and other devices for transmitting data, addresses and control signals to and from the bus 124." Ex-1006 at 7:46-49; 7:49-54; Ex-1003, ¶¶ 553-555.

j. [Claim 45i]

Ware discloses using attributes from first and second device profiles, and selecting a transfer size that is function of the data size and the first set of attributes. *Supra* §§ IX.B.1.o, IX.B.1.p; Ex-1003, ¶ Ex-1003, ¶¶ 556. Ware also teaches that this operation is performed by the interface controller (processor interface logic

122), which is part of the means for addressing. For example, Ware teaches that the processor interface logic 122 "may include signal conditioning circuitry and other devices for transmitting data, addresses and control signals to and from the bus 124," as well as "decoding logic for decoding one or more bits of a physical address ***to determine whether the first or second portion of main memory will receive a memory access transaction***, as described below with respect to FIG. 2." Ex-1006 at 7:46-49; 7:49-54; Ex-1003, ¶¶ 557-560. A POSITA would understand that, by decoding bits of a physical address to "determine whether the first or second portion of main memory will receive a memory access transaction," the processor interface logic uses attributes from the first and second device profiles and selects a transfer size for the memory transaction as a function of the data size of the memory transaction and the first set of attributes. Ex-1003, ¶ 561.

Accordingly, Ware in view of a POSITA's knowledge renders obvious this claim element. Ex-1003, ¶¶ 556-562.

8. Claim 51 is Obvious in View of Ware and a POSITA's Knowledge

Claim 51 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.B.2; Ex-1003, ¶¶ 564-567.

9. Claim 52 is Obvious in View of Ware and a POSITA's Knowledge

Claim 52 is substantially identical to claim 6 and is rendered obvious for the

reasons discussed above. *Supra* § IX.B.3; Ex-1003, ¶¶ 569-571.

10. Claim 59 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 59 pre]

Ware discloses "***a memory controller*** for a non-homogenous memory." Ex-1006 at 1:7-8 (emphasis added); *supra* § IX.B.7.a; Ex-1003, ¶¶ 573-575.

b. [Claim 59a]

Ware discloses an interface controller in the form of "processor interface logic 122" that "may include signal conditioning circuitry and other devices for transmitting data, addresses and control signals to and from the bus 124." Ex-1006 at 7:46-54; *supra* § IX.B.7.d. Ware discloses that the processor interface logic is directly coupled to the memory device interfaces. *Id*. at 7:22-39; Figure 1. Ware further discloses that the processor interface logic is directly coupled to the host device through a bus. *Id*. at 7:9-10; Figure 1. A POSITA would understand that Ware's processor interface logic includes an input/output (IO) device interface coupling to the host. Ex-1003, ¶¶ 576-578.

Annotated Figure 1 illustrates the **interface controller**—which would include an I/O interface coupled to a host **via bus 124**—coupled to the **memory device interfaces**:

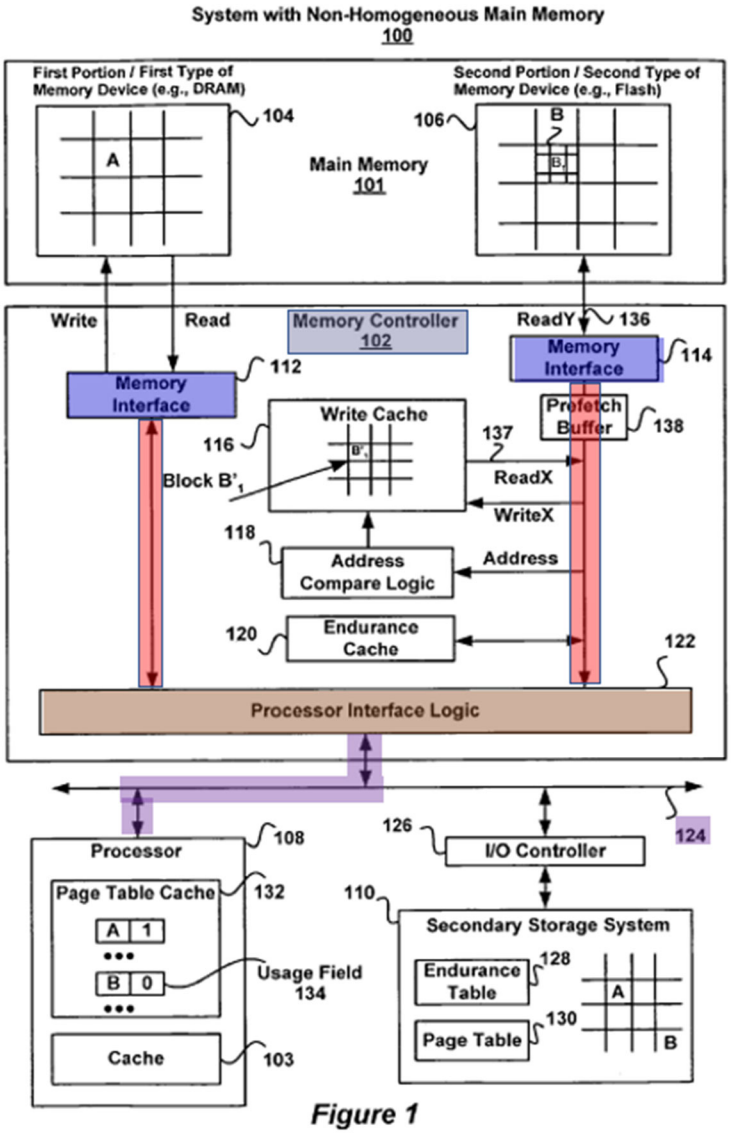


Figure 1

Id.

c. [Claim 59b]

Ware discloses a **memory store** (main memory 101) as explained above, *supra* § IX.B.1.b, and illustrated below:

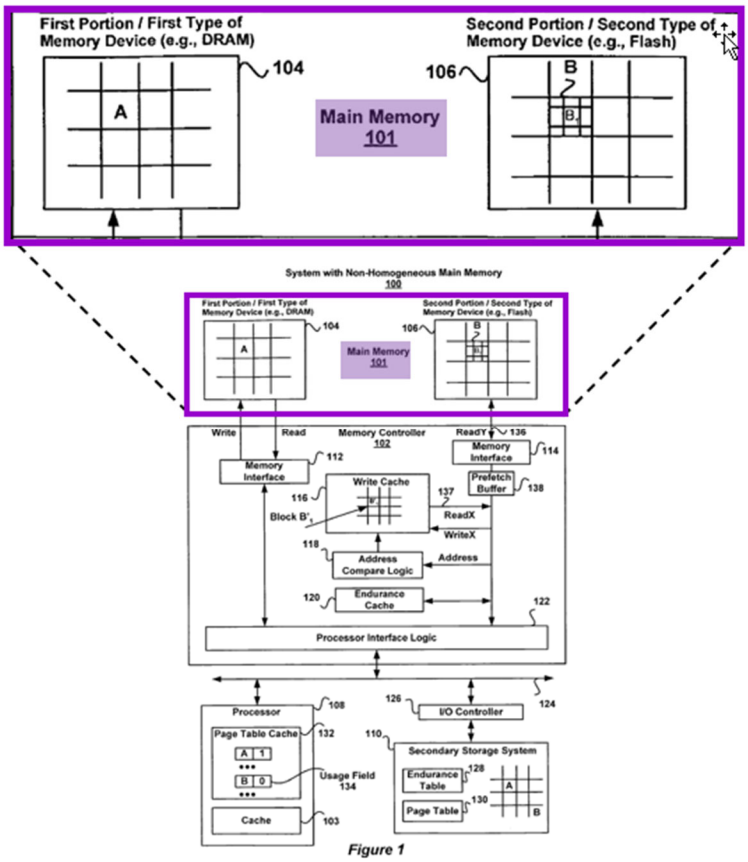


Figure 1

See Ex-1003, ¶¶ 579-581.

d. [Claim 59c]

As illustrated in Annotated Figure 1 below, Ware teaches that that the **memory device interfaces** are directly **coupled** to the **memory store**, explaining that "memory controller 102 includes memory interfaces 112, 114 for coupling the memory controller 102 to the memory devices in two or more distinct portions (104, 106) of main memory 101." Ex-1006 at 7:21-25; 4:4-6; Ex-1003 ¶¶ 582-584.

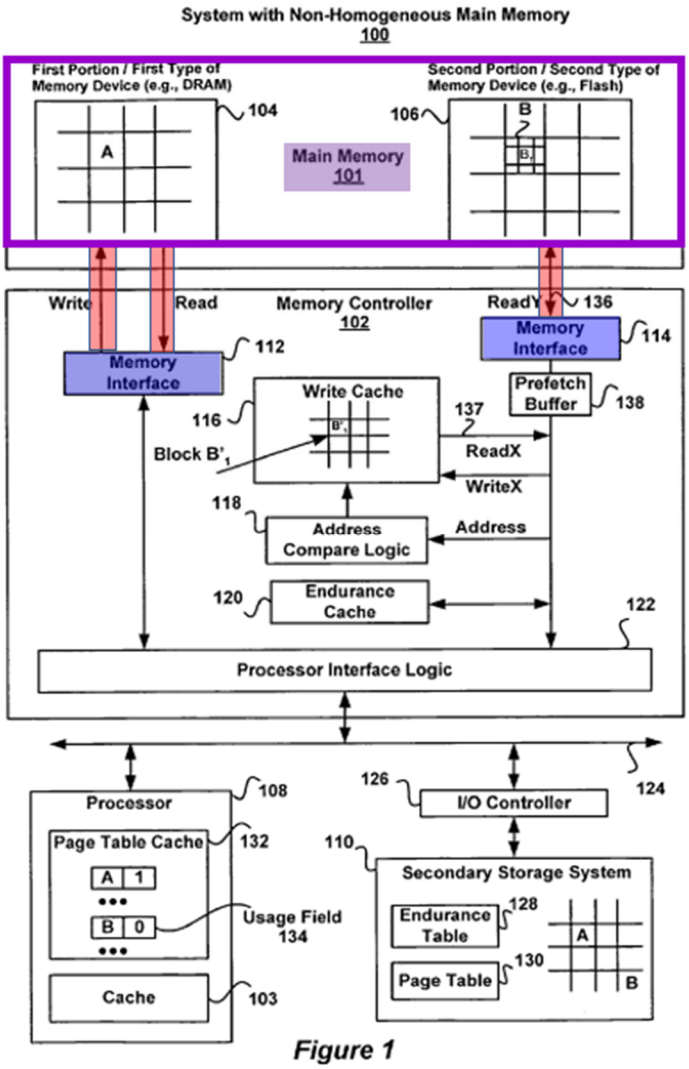


Figure 1

e. [Claim 59d]

Ware discloses performing a memory transaction comprising addressing a first memory location in a first memory device within a memory store. *Supra* § IX.B.1.b. Ware further teaches that the interface controller (processor interface logic) performs this memory transaction by addressing a first memory location, explaining that the interface controller includes "signal conditioning circuitry and other devices for ***transmitting data, addresses and control signals*** to and from the

bus 124," and also "decoding logic for decoding one or more bits of a physical address ***to determine whether the first or second portion of main memory will receive a memory access transaction***." Ex-1006 at 7:46-54; Ex-1003, ¶¶ 585-588. Annotated Figure 1 illustrates the **interface controller** performing a memory transaction by addressing a **first memory location** (field value A) in the **memory store**:

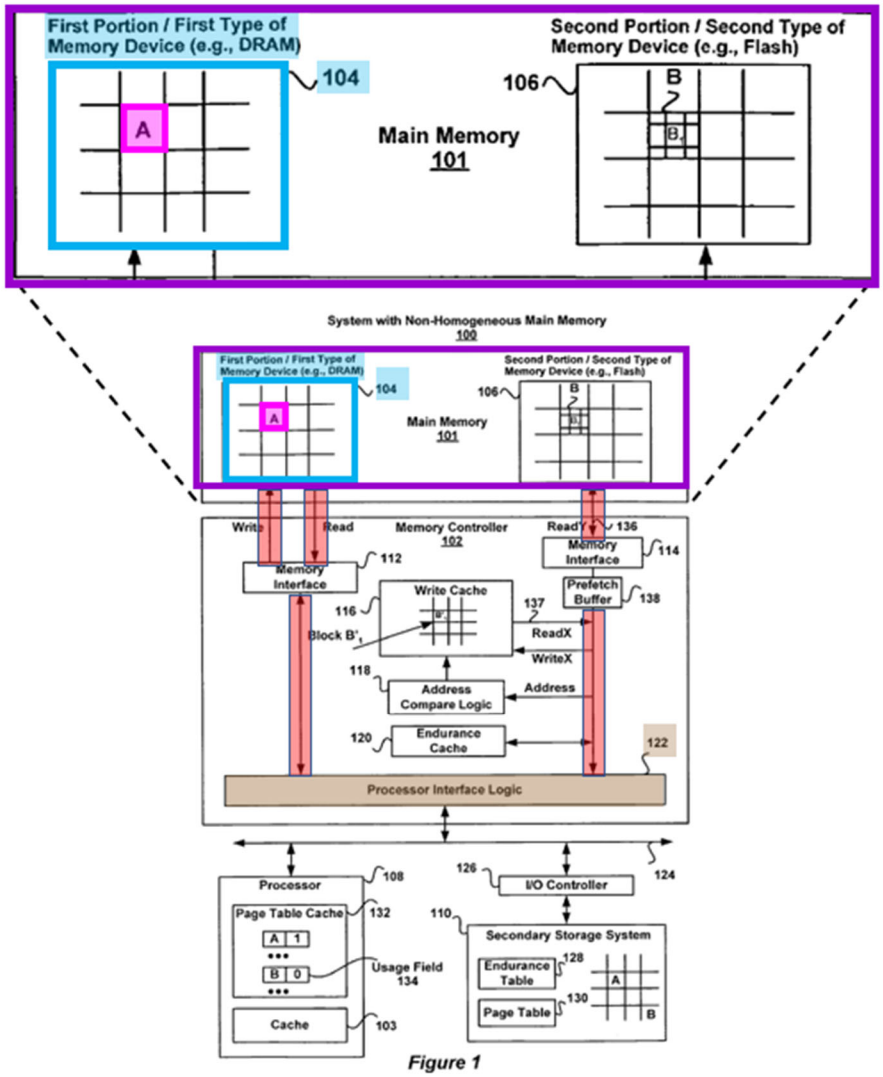


Figure 1

Ex-1003, ¶ 588.

f. [Claim 59e]

Element [59e] is identical to element [1b] and is disclosed by Ware as discussed above. *Supra* § IX.B.1.c; Ex-1003, ¶¶ 590-594.

g. [Claim 59f]

Element [59f] is identical to element [1f] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.g; Ex-1003, ¶¶ 595-596.

h. [Claim 59g]

Ware discloses identifying command details for causing the memory transaction to be performed, wherein said command details comprising the first memory device. *Supra* § IX.B.1.h; Ex-1003, ¶¶ 597-600. Ware further discloses that the interface controller (processor interface logic 122) performs these functions, explaining that interface controller includes "signal conditioning circuitry and other devices for ***transmitting data, addresses and control signals*** to and from the bus 124," and also "decoding logic for decoding one or more bits of a physical address ***to determine whether the first or second portion of main memory will receive a memory access transaction***." Ex-1006 at 7:46-54; Ex-1003, ¶ 601.

i. [Claim 59h]

Element [59h] is substantially identical to element [1h] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.i; Ex-1003, ¶¶ 603-604.

j. [Claim 59i]

Ware discloses that the interface controller obtains the first set of attributes after identifying the command details. *Supra* § IX.B.1.j; Ex-1003, ¶¶ 605-608.

k. [Claim 59j]

Ware renders obvious using attributes from a first device profile. *Supra* § IX.B.1.o; Ex-1003, ¶¶ 609-614.

l. [Claim 59k]

Ware discloses selecting a transfer size for the memory transaction, wherein the transfer size is a function of a data size of the memory transaction and the first set of attributes. *Supra* § IX.B.1.p; Ex-1003, ¶¶ 615-617.

11. Claim 71 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 71]

Claim 71 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.B.2; Ex-1003, ¶¶ 619-622.

12. Claim 76 is Obvious in View of Ware and a POSITA's Knowledge

Claim 76 is substantially identical to claim 6 and is rendered obvious for the reasons discussed above. *Supra* § IX.B.3; Ex-1003, ¶¶ 624-626.

13. Claim 80 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 80 pre]

Ware discloses an electronic storage device in the form of "a computer system 100" that "includes a memory controller 102, main memory 101, one or more processors 108 and secondary storage 100 (e.g., a hard disk unit)." Ex-1006 at 3:38-43 (emphasis added); claim 15; Ex-1003, ¶¶ 628-631.

b. [Claim 80a]

Ware discloses a memory controller. *Supra* § IX.B.7.a; Ex-1003, ¶ 632. Ware further teaches that the memory controller comprises an interface "coupled to one or more first memory devices of a first memory type" and an interface "coupled to one more second memory devices of a second memory type." Ex-1006, Abstract; 4:4-6; 7:22-25; claim 1.

Ware discloses that the memory store "includes a first portion 104 implemented with one or more memory devices of a first type (e.g., DRAM), and a second portion 106 implemented with one or more memory devices of a second type (e.g., NOR Flash, often simply called Flash memory)." Ex-1006 at 3:56-61; Ex-1003, ¶ 632. Ware also teaches addressing locations within each memory device, explaining that "a usage field value of 'A' represents a page mapped to the first portion 104 of main memory 101, while a value of 'B' represents a page mapped to the second portion 106 of main memory 101." *Id*. at 5:57-61; 7:46-54 (explaining that processor interface logic contains circuitry "for transmitting data, addresses and control signals" and "determining whether the first or second portion of main

memory will receive a memory access transaction"); Ex-1003, ¶ 632.

Annotated Figure 1 illustrates the memory controller **directly coupled** via communication pathways to, and disposed to address, a **first memory location** (field value A in a **first memory portion 104**) and a **second memory location** (field value B in a **second memory portion 106**):

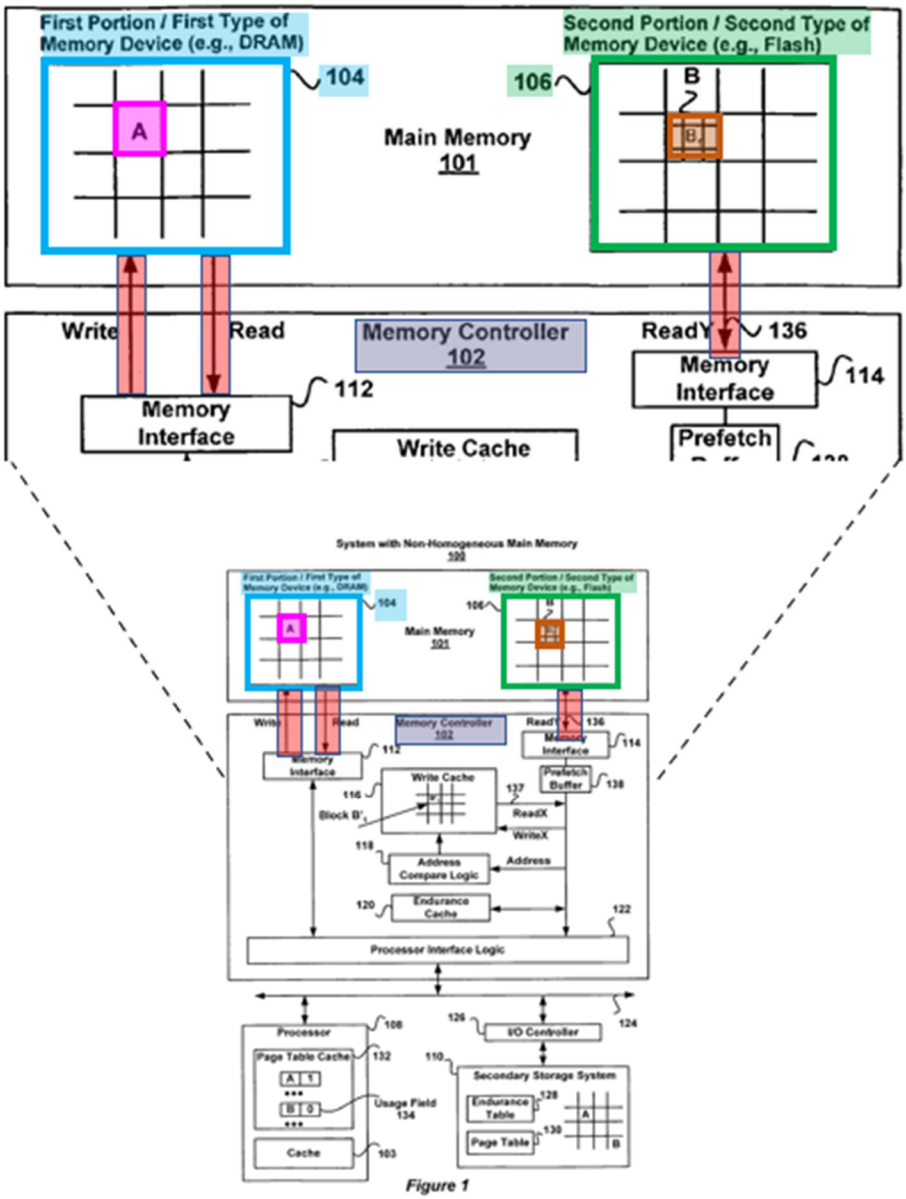


Figure 1

Ex-1003, ¶¶ 633-634.

Ware also teaches that the first memory location and second memory location are respectively associated with a first device profile and a second device profile. *Supra* § IX.B.1.c; Ex-1003, ¶¶ 635-636.

c. [Claim 80b]

As explained above, *supra* §§ IX.B.1.m, IX.B.7.e, and illustrated in Annotated Figure 1 below, Ware teaches that the **memory controller** is **directly coupled** (via bus 124) to the **host processor** as it performs memory address the **first** or **second** memory locations:

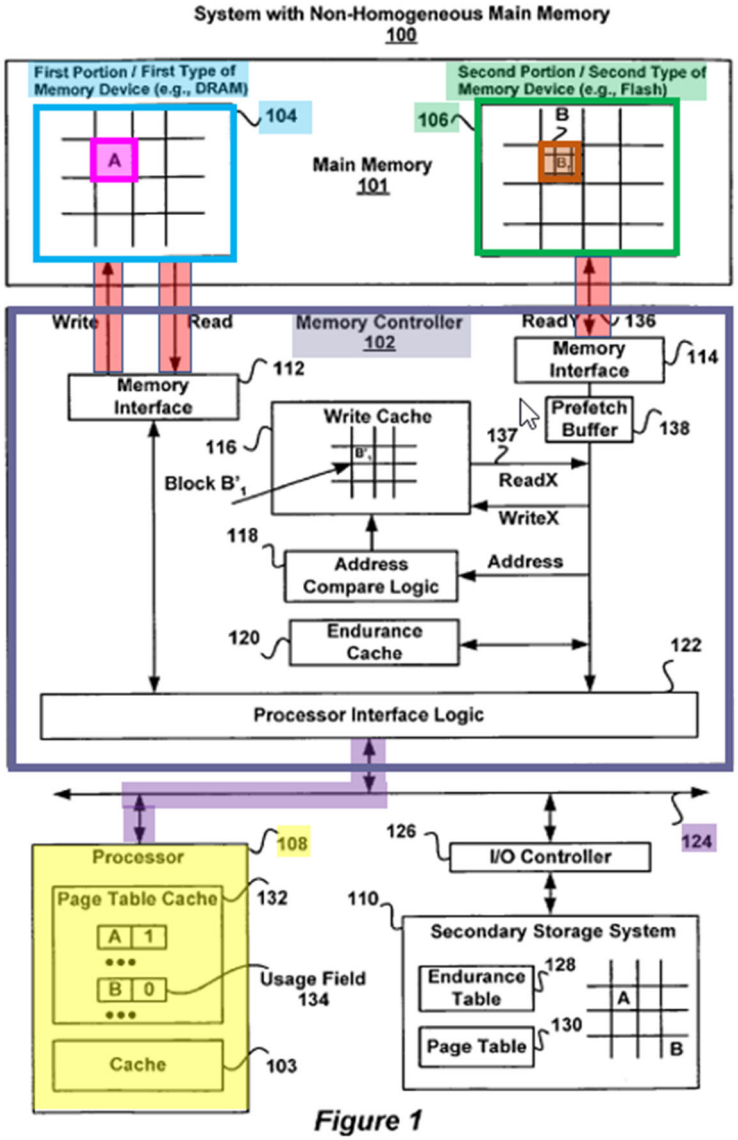


Figure 1

See Ex-1003, ¶¶ 638-640.

d. [Claim 80c]

Element [80c] is identical to element [1f] and is disclosed by Ware for the reasons discussed above. *Supra* § IX.B.1.g; Ex-1003, ¶¶ 641-642.

e. [Claim 80d]

Processor interface logic in the memory controller identifies command details

for causing the memory transaction to be performed, wherein said command details comprising the first memory device. *Supra* § IX.B.1.h; Ex-1003, ¶¶ 643-647.

f. [Claim 80e]

Element [80e] is substantially identical to element [1h] and is rendered obvious for the reasons discussed above. *Supra* § IX.B.1.i; Ex-1003, ¶¶ 648-649.

g. [Claim 80f]

Processor interface logic in the memory controller obtains the first set of attributes after identifying the command details. *Supra* § IX.B.10.j; Ex-1003, ¶¶ 650-653.

h. [Claim 80g]

Ware renders obvious using attributes from said first and second device profiles. *Supra* § IX.B.1.o; Ex-1003, ¶ 654. Ware, in view of a POSITA's knowledge, also renders obvious that these functions are performed by a memory controller. Ex-1003, ¶ 654. For example, Ware teaches that "[t]he processor interface logic 122 may include signal conditioning circuitry and other devices for transmitting data, addresses and control signals to and from the bus 124," as well as "decoding logic for decoding one or more bits of a physical address to determine whether the first or second portion of main memory will receive a memory access transaction." Ex-1006 at 7:46-59. A POSITA would have understood that, by decoding bits of a physical address to "determine whether the first or second portion

of main memory will receive a memory access transaction," the processor interface logic in the memory controller uses attributes from the first and second device profiles. Ex-1003, ¶¶ 655-658.

i. [Claim 80h]

Ware discloses that processor interface logic in the memory controller selects a transfer size for a transaction, wherein the transfer size is a function of a data size of the transaction and the first set of attributes. *Supra* § IX.B.1.p; Ex-1003, ¶¶ 659-662.

14. Claim 84 is Obvious in View of Ware and a POSITA's Knowledge

Claim 84 is substantially identical to claim 5 and is rendered obvious for the reasons discussed above. *Supra* § IX.B.2; Ex-1003, ¶¶ 664-667.

15. Claim 85 is Obvious in View of Ware and a POSITA's Knowledge

Claim 85 is substantially identical to claim 6. Accordingly, Ware, in view of a POSITA's knowledge, renders obvious this claim for the reasons discussed above. *Supra* § IX.B.3; Ex-1003, ¶¶ 669-671.

16. Claim 98 is Obvious in View of Ware and a POSITA's Knowledge

a. [Claim 98 pre]

Element [98 pre] is identical to element [80 pre] and is disclosed by Ware as discussed above. *Supra* § IX.B.13.a; Ex-1003, ¶¶ 673-676.

b. [Claim 98a]

Element [98a] is identical to element [80a] and is disclosed by Ware as discussed above. *Supra* § IX.B.13.b; Ex-1003, ¶¶ 677-683.

c. [Claim 98b]

Element [98b] is substantially identical to element [80b] and is disclosed by Ware as discussed above. *Supra* § IX.B.13.c; Ex-1003, ¶¶ 684-686.

d. [Claim 98c]

Element [98c] is identical to element [80c] and is disclosed by Ware as discussed above. *Supra* § IX.B.13.d; Ex-1003, ¶¶ 687-688.

e. [Claim 98d]

Element [98d] is identical to element [80d] and is disclosed by Ware as discussed above. *Supra* § IX.B.13.e; Ex-1003, ¶¶ 689-693.

f. [Claim 98e]

Element [98e] is substantially identical to element [80e] and is rendered obvious for the reasons discussed above. *Supra* § IX.B.13.f; Ex-1003, ¶¶ 694-696.

g. [Claim 98f]

Element [98f] is identical to element [80f] and is rendered obvious for the reasons discussed above. *Supra* § IX.B.13.g; Ex-1003, ¶¶ 697-700.

h. [Claim 98g]

Element [98g] is substantially identical to element [80g] and is rendered

obvious for the reasons discussed above. *Supra* § IX.B.13.h; Ex-1003, ¶¶ 701-704.

i. [Claim 98h]

Element [98h] is substantially identical to element [80h] and is rendered obvious for the reasons discussed above. *Supra* § IX.B.13.i; Ex-1003, ¶¶ 705-708.

X. INSTITUTION SHOULD NOT BE DISCRETIONARILY DENIED

A. The Board Should Not Exercise Its Discretion Under 35 U.S.C. § 314(a)

Petitioners hereby stipulate that, should the Petition be granted, they will not pursue in the district court the same grounds that are raised or could have reasonably been raised in this Petition pursuant to *Sotera Wireless, Inc., v. Masimo Corp.* IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A). Under the June 21, 2022, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, the Director has stated "the PTAB will not discretionarily deny institution of on an IPR" in view of such a stipulation. Interim Procedures at 7; *id*. at 3 and n.3 (discussing *Sotera*).

Accordingly, Petitioners' stipulation is dispositive in establishing that institution should not be discretionarily denied pursuant to 35 U.S.C. § 314(a).

B. The Board Should Not Exercise Its Discretion under 35 U.S.C. § 325(d)

"In evaluating arguments under § 325(d), [the PTAB] use[s] a two-part framework: (1) whether the same or substantially the same art previously was

presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petition has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *The Data Co. Techs., Inc. v. Bright Data Ltd.*, IPR2022-00135, Paper 12 at 15 (PTAB June 1, 2022) (citing *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020).

Here, neither Cornwell nor Ware was presented to the Office during examination of the application that led to the '190 patent. Nor were any other prior art or arguments substantially similar to those presented in this Petition presented to the Office. Thus, the *Advanced Bionics* framework does not apply because the first part is not satisfied. *Id.* at 17 (Where "the first part of the *Advanced Bionics* framework is not satisfied, [the Board] need not consider the second part of the framework.").

XI. MANDATORY NOTICES

A. Real Parties in Interest—37 C.F.R. § 42.8(b)(1)

The following entities are real parties in interest to this proceeding: KIOXIA Corporation and KIOXIA America, Inc. No other parties had access to or control over this Petition, and no other parties funded this Petition.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

To the best of Petitioner's knowledge, the '190 patent has been or is involved in the following cases:

- *Certain Solid State Storage Drives, Stacked Electronics Components, and Products Containing Same*, Inv. No. 337-TA-1097 (Int'l Trade Comm'n). This case is no longer ongoing.
- *SK Hynix Inc., et al. v. BiTMICRO, LLC*, Case No. 3:18-cv-03505 (N.D. Cal.). This case is no longer ongoing.
- *Samsung Semiconductor, Inc. et al v. BiTMICRO, LLC et al.*, Case No. 3:18-cv-03502 (N.D. Cal.). This case is no longer ongoing.
- *BiTMICRO LLC v. KIOXIA Am. Inc., et al.*, Case NO. 6:22-cv-00331 (W.D. Tex. 2022). This case is ongoing.
- *BiTMICRO LLC v. Intel Corp.*, Case No. 5:23-cv-00625 (N.D. Cal.), which was transferred from the District Court for the Western District of Texas, Case No. 6-22-cv-00335. This case is ongoing.

Petitioners are not aware of any other matters involving the '190 patent.

C. Lead and Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioners provide the following designation of counsel.

Lead Counsel	Backup Counsel
Douglas F. Stewart, Reg. No. 51,060 Bracewell, LLP 701 Fifth Avenue, Suite 3420 Seattle, WA 98104-7018 (206) 204-6200 (t) (800) 404-3970 (f) doug.stewart@bracewell.com	Jared D. Schuettenhelm, Reg. No. 59,539 Bracewell, LLP 701 Fifth Avenue, Suite 3420 Seattle, WA 98104-7018 (206) 204-6200 (t) (800) 404-3970 (f) jared.schuettenhelm@bracewell.com Patrick Connolly, Reg. No. 69,570 Bracewell, LLP 701 Fifth Avenue, Suite 3420 Seattle, WA 98104-7018 (206) 204-6200 (t) (800) 404-3970 (f) patrick.connolly@bracewell.com

D. Service Information—37 C.F.R. § 42.8(b)(4)

Please address all correspondence and service to the address listed above. Petitioners consent to electronic service by email at Bracewell-IP@bracewell.com.

XII. CONCLUSION

The prior art references cited herein demonstrate that the challenged claims of the '190 patent are obvious. Petitioners thus request that the PTAB grant this Petition, institute *inter partes* review, and cancel the challenged claims.

Respectfully Submitted,

Dated: March 23, 2023

/s/ Douglas F. Stewart
Douglas F. Stewart
doug.stewart@bracewell.com
(Reg. No. 51,060)
Jared D. Schuettenhelm
Jared.schuettenhelm@bracewell.com
(Reg. No. 59,539)
Patrick Connolly
patrick.connolly@bracewell.com
(Reg. No. 69,570)
Bracewell LLP
701 Fifth Avenue, Suite 3420
Seattle, WA 98104-7018
(206) 204-6200 (t)
(800) 404-3970 (f)

Counsel for Petitioners

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24, the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,140 words excluding the caption, table of contents, table of authorities, table of exhibits, claim listing, mandatory notices, certificate of service, and certificate of word count. Petitioner has relied on the word count feature of the word processing system used to create this paper in making this certification.

Dated: March 23, 2023

/s/ Douglas F. Stewart

doug.stewart@bracewell.com
(Reg. No. 51,060)
Bracewell LLP
701 Fifth Avenue, Suite 3420
Seattle, WA 98104-7018
(206) 204-6200 (t)
(800) 404-3970 (f)

Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on March 23, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review, associated exhibits, and power of attorney to be served via overnight courier upon the following counsel of record for Patent Owner per 37 CFR §§ 42.105(a) and 42.205(a).

Patent Office Counsel of Record	**Litigation Counsel of Record**
Joseph P. Lally Jackson Walker LLP 100 Congress Ave. Ste 1100 Austin, TX	Michael Flynn-O'Brien Bunsow De Mory LLP 701 El Camino Real Redwood City, CA 94063

I further certify that I served courtesy copies of the foregoing documents via electronic mail on March 23, 2023, upon Patent Owner's counsel of record as follows:

Patent Office Counsel of Record	**Litigation Counsel of Record**
Joseph P. Lally jlally@jw.com	Michael Flynn-O'Brien Corey Johanningmeier Richard C. Lin Denise M. De Mory Li Guo BDIP-BiTMicro-KIOXIA@bdiplaw.com B. Russell Horton rhorton@gbkh.com

Dated: March 23, 2023 */s/Andrea Kato*
Andrea Kato, Bracewell LLP