UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC.

Petitioner

v.

BELL SEMICONDUCTOR, LLC

Patent Owner

Patent No. 7,646,091

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,646,091

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I. INTRODUCTION

NXP USA, Inc. ("Petitioner" or "NXP") requests *inter partes* review of claims 1-14 ("the challenged claims") of U.S. Patent No. 7,646,091 ("the '091 Patent") (Ex. 1001), which, according to PTO records, is assigned to Bell Semiconductor, LLC ("Patent Owner" or "PO"). For the reasons discussed below, the challenged claims should be found unpatentable and cancelled.

II. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: NXP USA, Inc. ("Petitioner"), NXP Semiconductors N.V., NXP B.V., and Freescale Semiconductor Holdings V, Inc.

Related Matters

The '091 Patent is at issue in *Bell Semiconductor, LLC v. NXP USA, Inc. et al* Case No. 8:22-cv-02133-HDV-ADS, pending in Federal District Court in the Central District of California.

Counsel and Service Information

Lead counsel is Timothy Taylor (Reg. No. 76,643), and Backup counsel are (1) Bruce Garlick (Reg. No. 36,520), (2) Timothy Markison (Reg. No. 33,534), and (3) Patricia Healy (Reg. No. 73,072). Service information is: Garlick & Markison, 2025 Guadalupe Street, Suite 260, Austin, TX 78705; Tel.: 512-751-5682; Fax: 888-

456-7824; email: GM-NXP-Bell-IPR@texaspatents.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

Fees under 37 C.F.R. § 42.15(a) will be paid at the time of filing. When necessary to further the proceeding or in the case of overages, the PTO is authorized to charge and deposit funds to and from Deposit Account No. 50-2126.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '091 Patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein. 37 C.F.R. § 42.104(a)

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-14 should be canceled as unpatentable based on the following grounds:

Ground 1: Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 102 as being anticipated by *Okabe* (Ex. 1005).

Ground 2: Claim 1 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Hashemi* (Ex. 1006) and in view of *Okabe* (Ex. 1005).

Ground 3: Claims 1 and 12 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe* (Ex. 1005) in view of *Applicant's Admitted Prior Art* (*AAPA*) from within the '091 Patent (Ex. 1001).

Ground 4: Claims 2, 5, 6, and 9 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, and *Sutardja* (Ex. 1012).

Ground 5: Claims 3, 4, and 7 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, *Sutardja*, and *Taggart* (Ex. 1009).

Ground 6: Claims 8 and 11 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, *Sutardja,* and *Choi* (Ex. 1011).

Ground 7: Claim 10 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, *Sutardja*, *Choi*, and *Digital Design* (Ex. 1010).

Ground 8: Claim 13 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, *Kramer* (Ex. 1007), and Sutardja.

Ground 9: Claim 14 is unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Okabe*, in view of *AAPA*, *Conn* (Ex. 1013), *Kramer*, and *Sutardja*.[1] Note that none of the above references were considered by the Examiner during prosecution.

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[1] For each Ground, Petitioner does not rely on any reference other than those listed. Other references are to show the state of the art at the time of the invention. *See Ariosa Diagnostics v. Verinata Health, Inc*., 805 F.3d 1359, 1365 (Fed. Cir. 2015).

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '091 Patent would have had a bachelor's degree in a field relating to the integrated circuit package manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication and packaging of integrated circuits. (Ex. 1002, ¶20)[2] More education can supplement practical experience and vice versa. (*Id.*)

VII. THE '091 PATENT AND PRIOR ART

A. The '091 Patent

The '091 Patent is entitled "Semiconductor Package and Method using Isolated Vss Plane to Accommodate High Speed Circuitry Ground Isolation". (Ex. 1001, Title) (Ex. 1002, ¶26)

The '091 Patent discloses an example of a prior art integrated circuit package in Figure 1 below, which includes a single ground plane 111 utilized for the IC die 101. (Ex. 1001, 1:64-66) (Ex. 1002, ¶27)

[2] Petitioner submits the declaration of Dr. Jacob Baker (Ex. 1002), an expert in the field of the '091 patent. (*See generally* Ex. 1003)

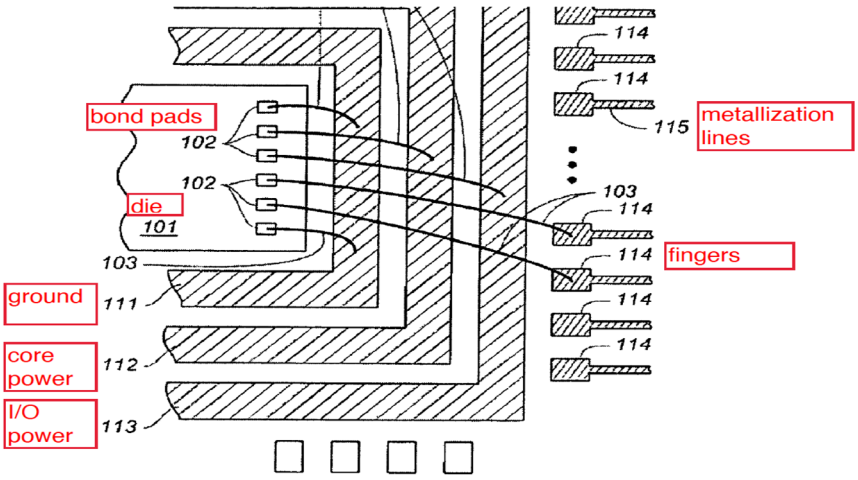


FIG. 1 (PRIOR ART)

(Ex. 1001., FIG. 1 (annotated).)

The ’091 Patent also discloses that prior art packaging substrates include various metallization and solder mask layers to form the substrate. (*Id.*, 1:30-32) The ’091 Patent further discloses that the prior art taught a series of bond pads of the die that are connected with the fingers, the ground layer, the core power layer, and the I/O power layer. (*Id.*, 1:62-64) The ’091 Patent further discloses that the fingers are typically connected to the ground plane and that metallization lines electrically connect the fingers to vias that connect with solder balls on the bottom of the substrate. (*Id.*, 1:58-62) (Ex. 1002, ¶28)

According to the ’091 patent, when the high speed portions and low speed portions of the IC are electrically connected to the same ground plane 111, excessive noise generated by the high speed circuitry interferes with the operation of the low-speed circuitry. (*Id.*, 1:64 – 2:13) (Ex. 1002, ¶¶29-30)

The '091 Patent admits that the prior art had already addressed this interference issue by using individual pins for separately grounding each high-speed connection. However, this solution used up a limited amount of pins to accommodate the grounding of the high-speed circuitry. (Ex. 1001, 2:23-31) (Ex. 1002, ¶30)

Thus, the '091 Patent purports to solve the interference resulting from having high and low speed circuitry sharing the same ground plane by utilizing a separate ground plane for the high speed circuitry. (Ex. 1001, 2:45-48) (Ex. 1002, ¶31) This is shown below in Figure 4 of the '091 Patent as high speed ground plane 331 and low speed ground plane 311.

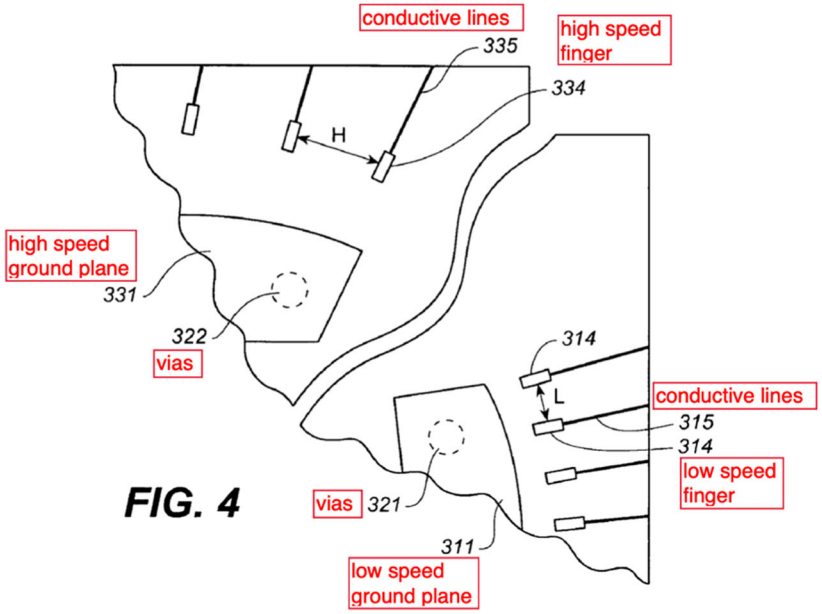


FIG. 4

(*Id.*, FIG. 4 (annotated).)

Notably, the '091 Patent does not disclose *any* physical or otherwise structural difference (e.g., size, materials, shape, etc.) in a ground plane enabled for use with

high speed circuitry as opposed to a ground plane enabled for use with low speed circuitry. (Ex. 1002, ¶31)

The ’091 Patent also purports to address interconnection crosstalk issues by increasing the spacing (H, shown above in Figure 4) between high speed conductive lines. (*Id*., ¶¶33-34)

As explained below (*infra* Section IX), the above features (e.g., separate ground planes and spacing between interconnections) were all well known in the prior art. (*See Id.*, ¶25; ¶¶61-215; see also *Id.*, ¶¶36-59 (describing the state of the art).)

B. The Prior Art

1. *Okabe* (Ex. 1005)

Okabe is analogous to the ’091 Patent as they are both in the same field of integrated circuit packages. *Okabe* discloses a radio frequency (RF) module comprising a module substrate that has reduced interference between its electronic circuit blocks, where the electronic circuits operate at different speeds (e.g., frequencies (e.g., 3.8 megahertz (MHz), 1.9 gigahertz (GHz), 2.1 GHz, 200 kilohertz (kHz), etc.)). (Ex. 1005, 2:66 – 3:3, 3:10-18, 7:36-43, 14:5-13)

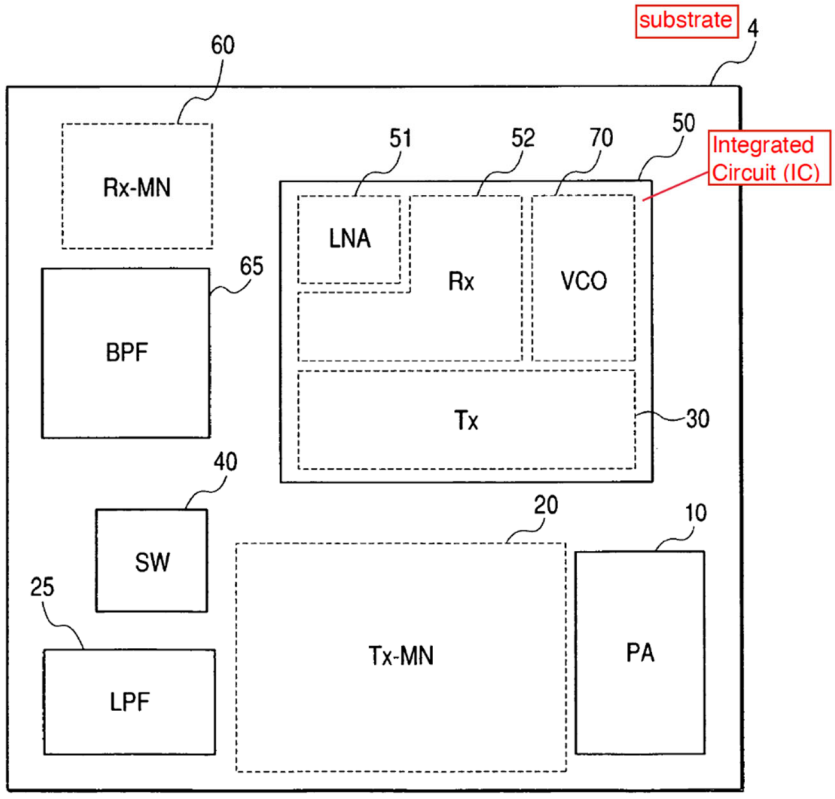
Okabe discloses the reduced interference results from separate ground planes that are separated and electronically isolated. (*Id.* 5:39-46; Abstract.) *Okabe* teaches it was well known in the art to separate ground planes to reduce interference between

a first and second active circuit chip on a single interconnect substrate. (*Id.*, 2:24-41) (Ex. 1002, ¶36)

Okabe further discloses that the separate ground planes can be extended to individual circuits. (Ex. 1005, 2:42-49) (Ex. 1002, ¶37) *Okabe* also teaches a common ground plane (e.g., a reference plane) to which all separate ground planes are connected, fixes reference potential for the individual circuits for stable performance that is not dependent on the ground land on a motherboard (Ex. 1005, 11:14-19)

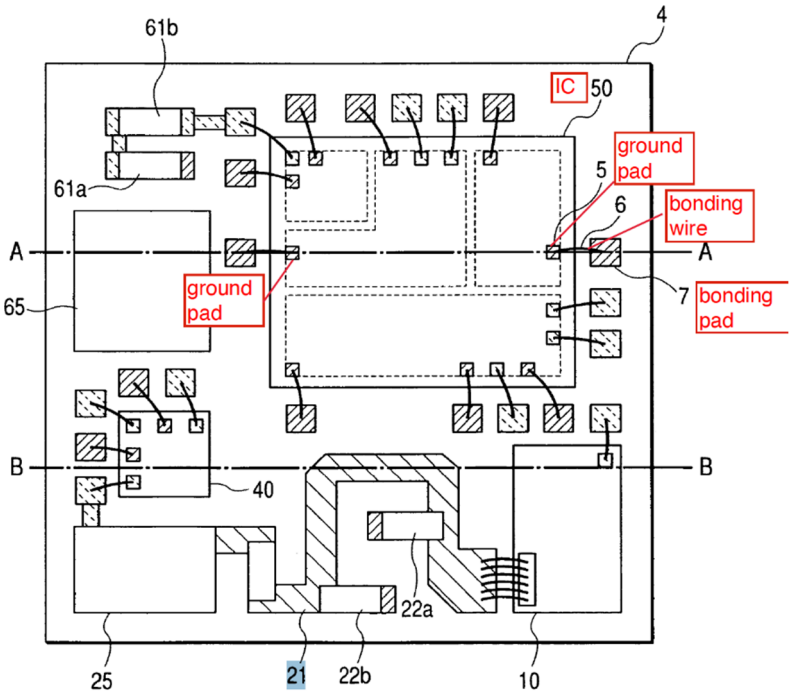
As shown below in Figure 3, *Okabe* discloses an IC 50 on a substrate 4, wherein the IC includes lower speed components and higher speed components. For example, IC 50 includes a low noise amplifier (LNA) 51, a receive (Rx) circuit 52, a transmitter (Tx) circuit 30, and a voltage controlled oscillator (VCO) 50. (*Id.*, 9:10-16) (Ex. 1002, ¶¶38-39)

FIG. 3



(Ex. 1005, FIG. 3 (annotated).)

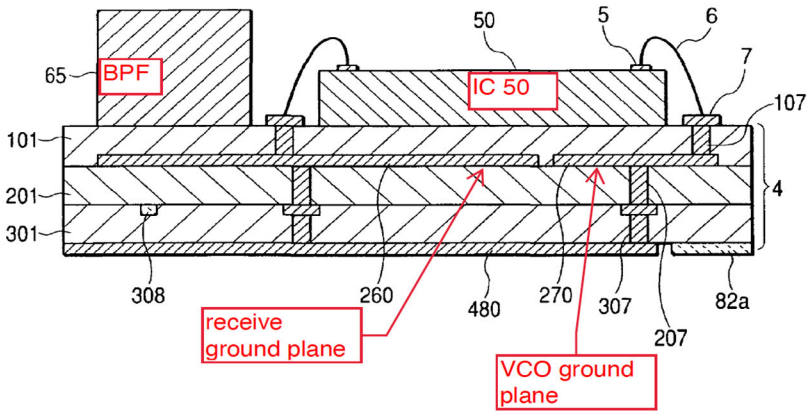
As shown below in Figure 4, *Okabe* shows how different components of the same IC are connected to bonding pads of the substrate 4 via bonding wire 6 and ground pad 5. (Ex. 1002, ¶40)



(Ex. 1005, FIG. 4 (annotated).)

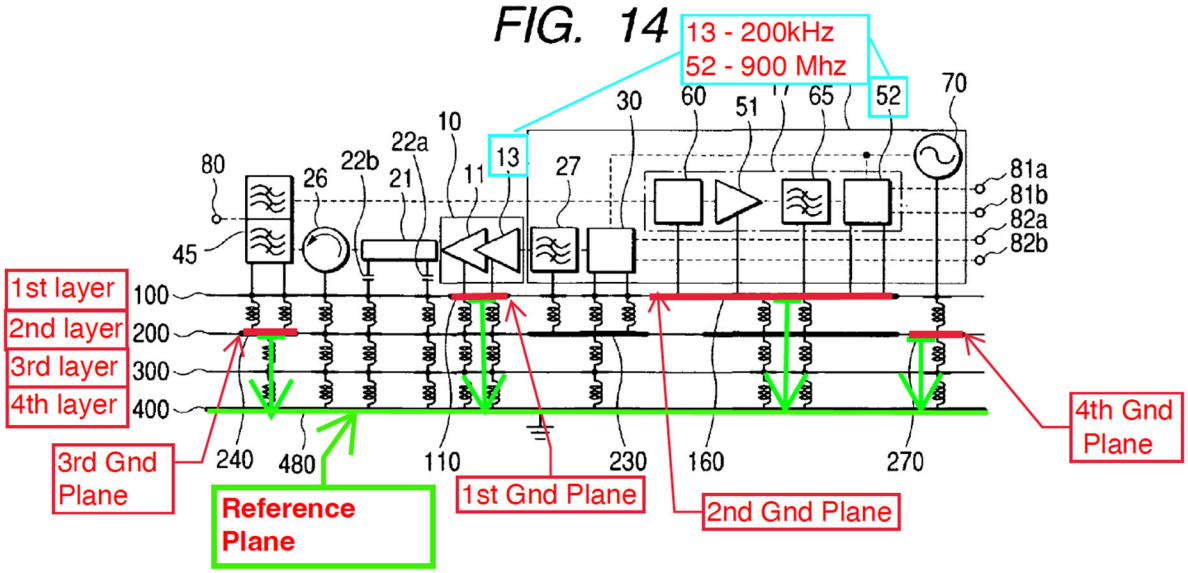
Cross section A of Figure 4 above, is then shown in Figure 9, shown below, which shows the connection of different components (having different speeds) of the same IC 50 to different ground planes of the substrate 4. (Ex. 1002, ¶40)

FIG. 9



(Ex. 1005, FIG. 9 (annotated).)

Okabe further discloses in Figure 14, shown below, a substrate that includes four layers 100-400, where layer 100 includes separate ground planes 110 and 160, and layer 200 includes separate ground planes 240, 230, and 270. (*Id.*, 14:26 – 15:3)



(*Id.*, FIG. 14 (annotated).)

Okabe provides an example where the frequency of the circuit 13 is operating at 200 kilohertz (kHz), and the circuit 52 is operating at 900 megahertz (MHz). (*Id.*, 7:36-43) Thus, *Okabe* teaches a first layer 100 includes a first ground plane 110 connected with lower speed circuitry, and a second ground plane 160 connected with higher speed circuitry, where the first and second ground planes are separated and electrically isolated. (Ex. 1002, ¶42)

Okabe further discloses a second layer 200 that includes a third ground plane 240 and a fourth ground plane 270 that are separated and electrically isolated. (*Id.*)

(Ex. 1005, 14:13-25) With further reference to Figure 14 above, a reference plane (e.g., common ground 480) is disclosed that is associated with each layer of the substrate (e.g., layers 100-400) and the ground planes 110, 160, 230, 240, and 270. (Ex. 1002, ¶43)

2. *Hashemi* (Ex. 1006)

Hashemi is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. *Hashemi* discloses "a multiple chip module (MCM) for use with baseband, RF or IF applications" that includes a number of active circuit chips mounted on a substrate. (Ex. 1006, Abstract) (Ex. 1002, ¶44) *Hashemi* teaches the MCM is capable of concurrent operation at different speeds, with examples ranging from 45 Megahertz (MHz) to 2.4 Gigahertz (GHz). (*Id.*) (Ex. 1006, 3:5-10, 43-51)

Hashemi teaches that the MCM can include physically separated split ground planes to achieve electronic isolation between different active circuit chips (e.g., RF and IF) and the physically separated or split ground planes can reside at different metal layers or at the same metal layer. (Ex. 1006, Abstract, Claims 15-16, 7:9-26) (Ex. 1002, ¶45)

Hashemi teaches in Figure 1, shown below, a first ground plane 122 being used for a first active chip 104, and a second ground plane 124 being used for a second active chip 104, which reduces unwanted interference (e.g., noise). (Ex. 1006, 7:16-21) (Ex. 1002, ¶46)

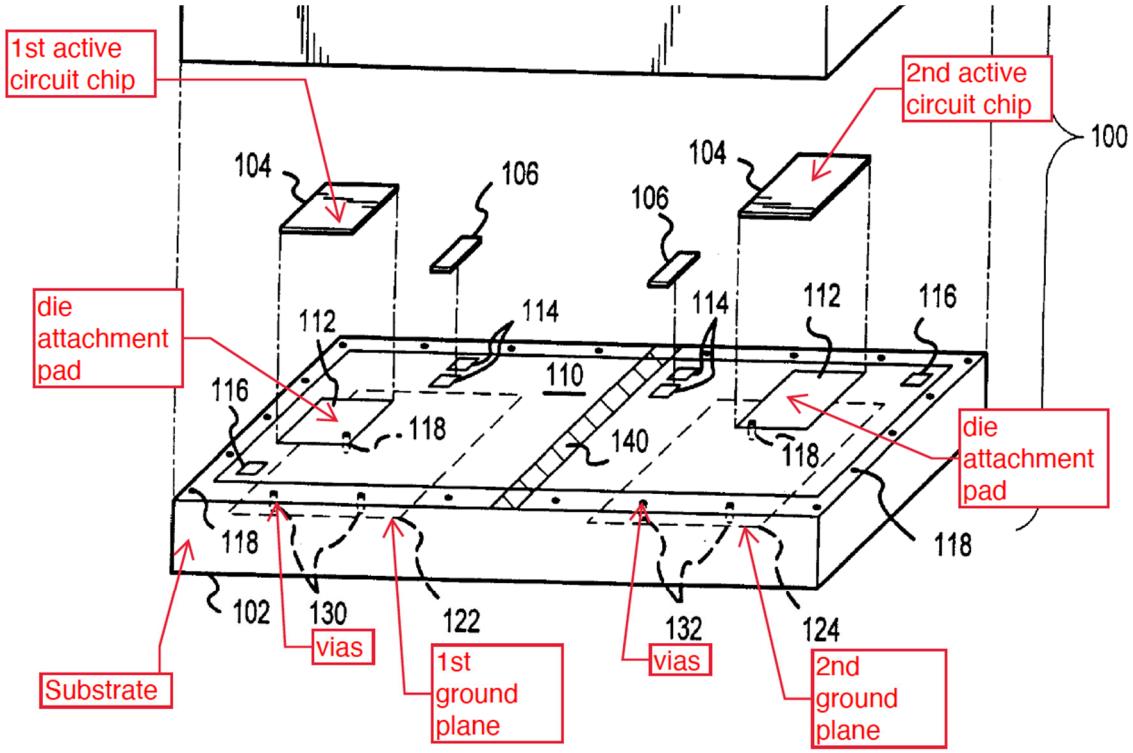


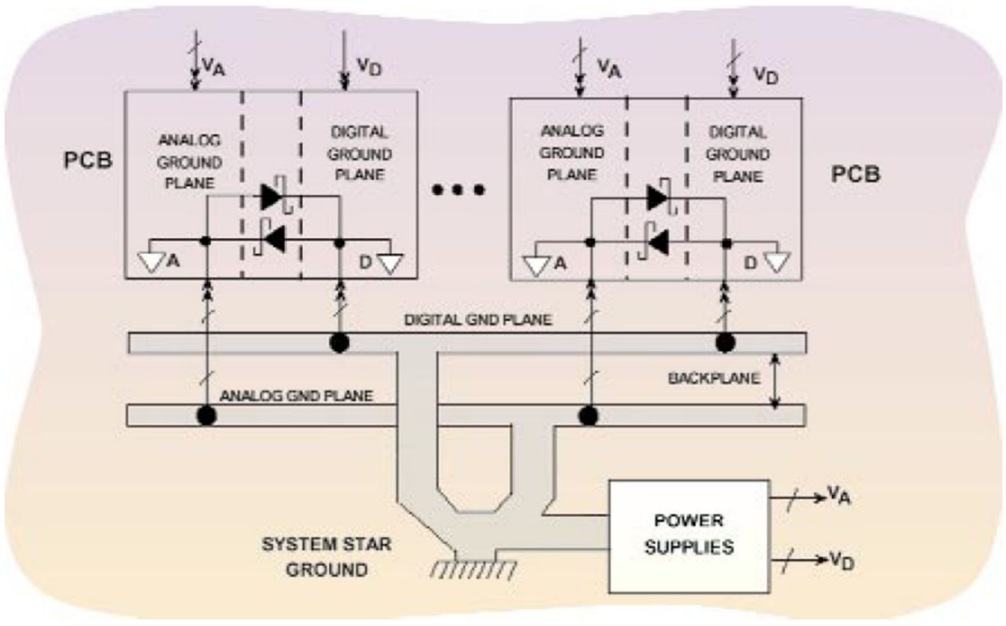
FIG.1

(Ex. 1006, FIG. 1 (annotated).)

3. *Kester* (Ex. 1015)

Kester is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. *Kester* is entitled "Proper Grounding is Critical for High-Speed Systems" and was published in Wireless Systems Design in May of 2000.

(Ex. 1015, p. 42) *Kester* teaches in high-speed systems that "it is highly desirable to physically separate sensitive analog components from noisy digital components". (*Id.*, p. 40) (Ex. 1002, ¶48) *Kester* further teaches, as shown below in Figure 1, that to minimize noise in high speed circuits, it is "essential" to separate ground planes for the analog and digital circuitry. (Ex. 1015, p. 40) (Ex. 1002, ¶48)



1. *In order to minimize noise in high-frequency, high-speed circuits, it is essential to separate analog and digital grounds.*

WIRELESS SYSTEMS DESIGN / MAY 2000

(Ex. 1015, FIG. 1 (emphasis added).)

4. *Kramer* (Ex. 1007)

Kramer is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. *Kramer* discloses isolating grounds for separate portions of an integrated circuit. (Ex. 1007, 5:38-41) As shown in Figure 3 below, *Kramer*

discloses an integrated circuit 30 attached to BGA package 28 includes an analog circuit 31. Kramer states that "IC 30 comprises an analog circuit 31, such as a serial transceiver, that requires isolated power and ground connections to reduce noise on analog circuit 31 from other circuits of IC 30". (*Id.*) (Ex. 1002, ¶49)

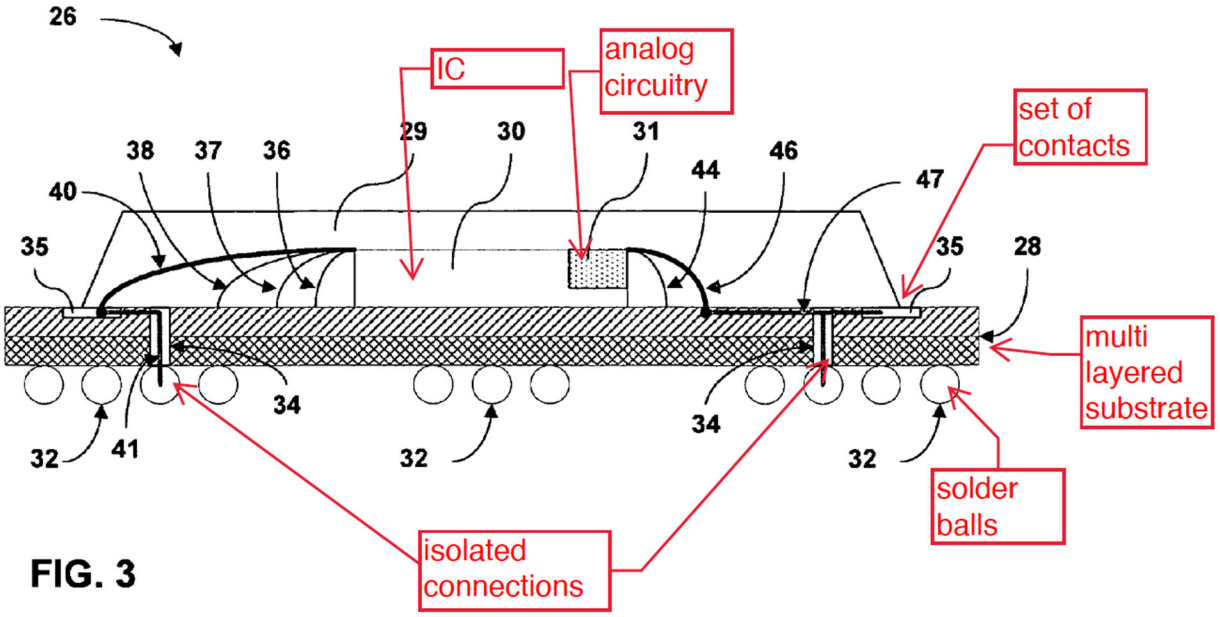


FIG. 3

(Ex. 1007, FIG. 3, (annotated).)

5. *Taggart* (Ex. 1009)

Taggart is analogous to the '091 Patent as they are both in the same field of integrated circuit packages. *Taggart* discloses a spacing or "pitch" for aligning bond fingers with die pads in as shown below in Figure 9. (Ex. 1009, ¶27) (Ex. 1002 ¶51) *Taggart* discloses specific values for the spacing ranging from "about 10 um

[micrometers] to about 200 um", with specific examples of the pitch being 135 um and 200 um. (Ex. 1009, ¶27) (Ex. 1002, ¶50)

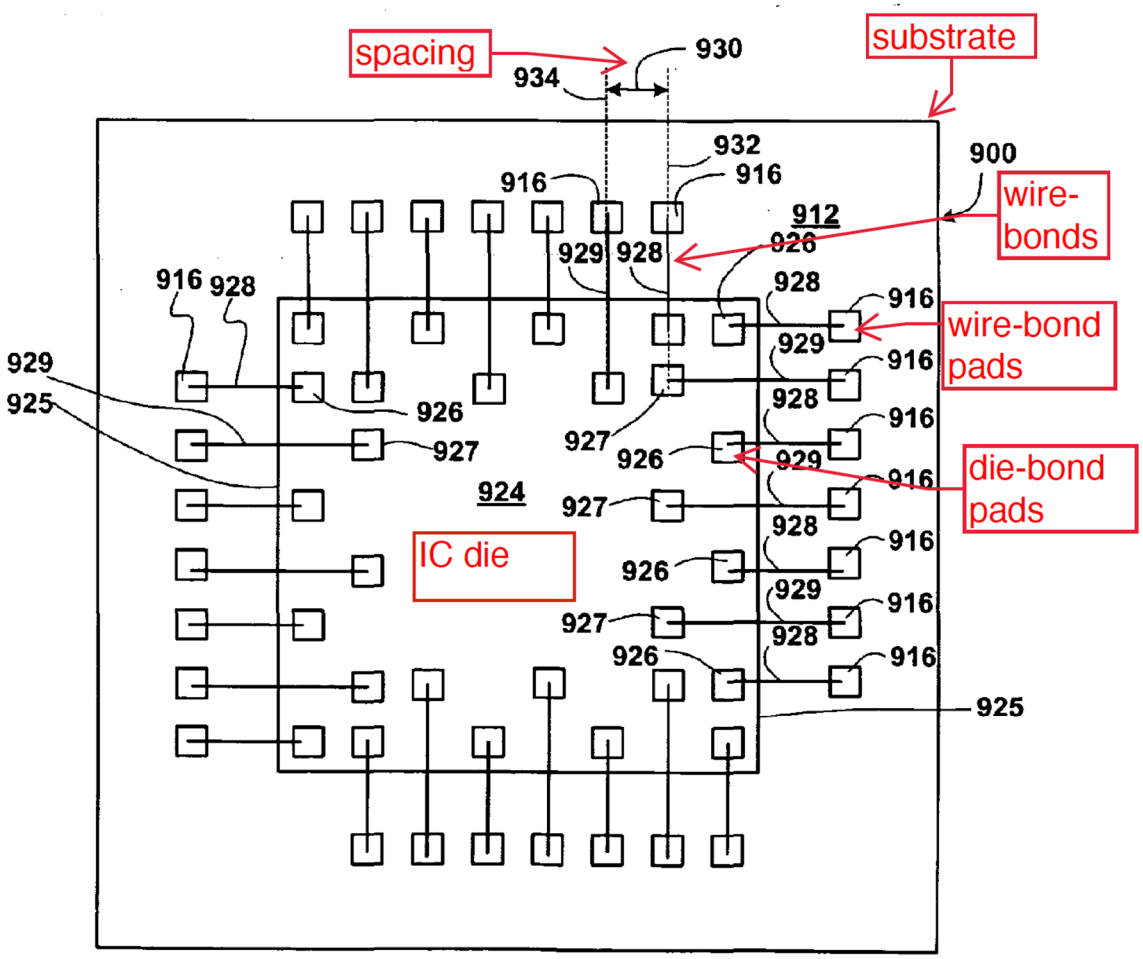


FIG. 9

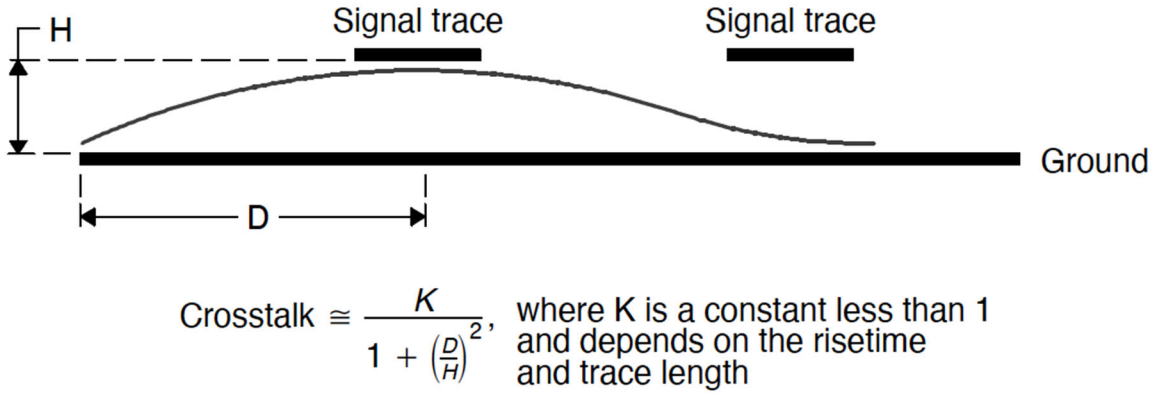
(Ex. 1009, FIG. 9, (annotated).)

6. *High-Speed DSP Systems Design* (hereinafter *High-Speed DSP*") (Ex. 1014)

High-Speed DSP discloses crosstalk is when noise interferes with other circuits. (Ex. 1014, p. 31) *High-Speed DSP* discloses in Figure 3-3, shown below,

that the spacing or distance, D, between the traces affects the amount of crosstalk. (*Id.*, p. 32) (Ex. 1002, ¶52)

Figure 3-3. Crosstalk Estimation (1)



(Ex. 1014, FIG. 3-3)

Thus, *High-Speed DSP* teaches that a "higher D yields lower crosstalk." (Ex. 1002, ¶35) To further emphasize this point, *High-Speed DSP* states "Obviously, moving the traces further from each other will reduce the crosstalk." (*Ex*. 1014, p. 32) (Ex. 1002, ¶52)

7. *High-Speed Digital Design* (hereinafter "*Digital Design*") (Ex. 1010)

Digital Design discloses design guidelines for various circuits to control crosstalk for high and low speed signals by determining how far to separate traces. (Ex. 1010, p. 189) (Ex. 1002, ¶¶53-54) *Digital Design* shows in Figure 5.4, shown below, that crosstalk for signal traces is based on in part on the distance, D, between

signal traces (Ex. 1010, p. 192) (Ex. 1002, ¶54). As one example, *Digital Design* discloses that "more closely spaced traces yield more crosstalk". (Ex. 1010, p. 215)

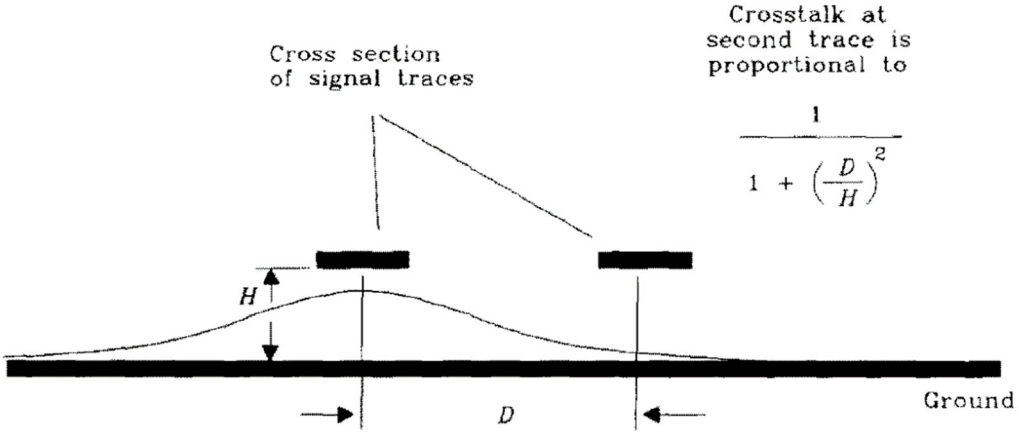
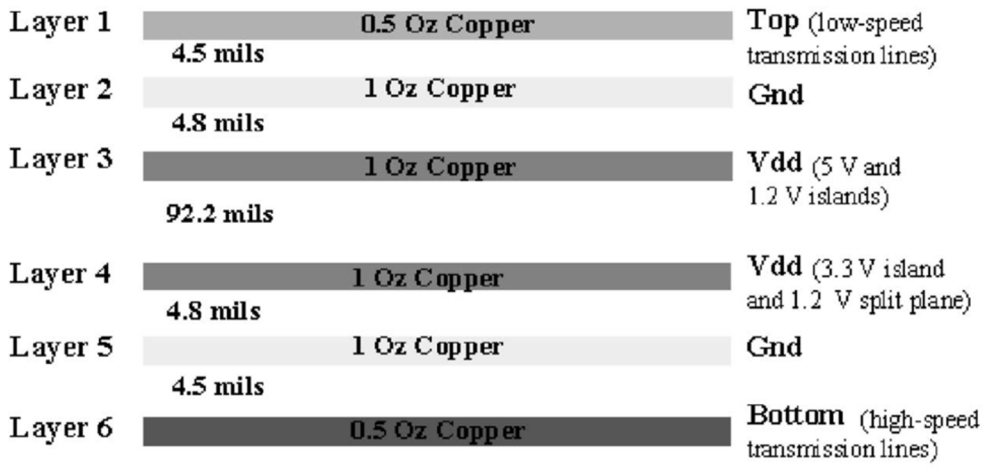


Figure 5.4 Cross section of two traces showing crosstalk.

(*Id.*, FIG 5.4)

8. *Choi* (Ex. 1011)

Choi teaches in Figure 6, shown below, a multi-layered PCB that has low-speed interconnects on layer 1 and high-speed interconnects on layer 6. (Ex. 1011, p. 304) (Ex. 1002, ¶55) *Choi* further teaches that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms) and the high-speed signal transmission lines are designed to provide 100 Ohm differential impedance. (*Id.*)



(Ex. 1011, FIG. 6)

9. *Sutardja* (Ex. 1012)

Sutardja teaches in Figure 10A, shown below, that the spacing between the low speed leads (d1, annotated in green) is different from the spacing between the pairs of high speed leads (d4, annotated in yellow), and further that the spacing (d1, d2, d3, and d4) "may be irregular to increase or decrease coupling." (Ex. 1012, ¶0139) (Ex. 1002, ¶57)

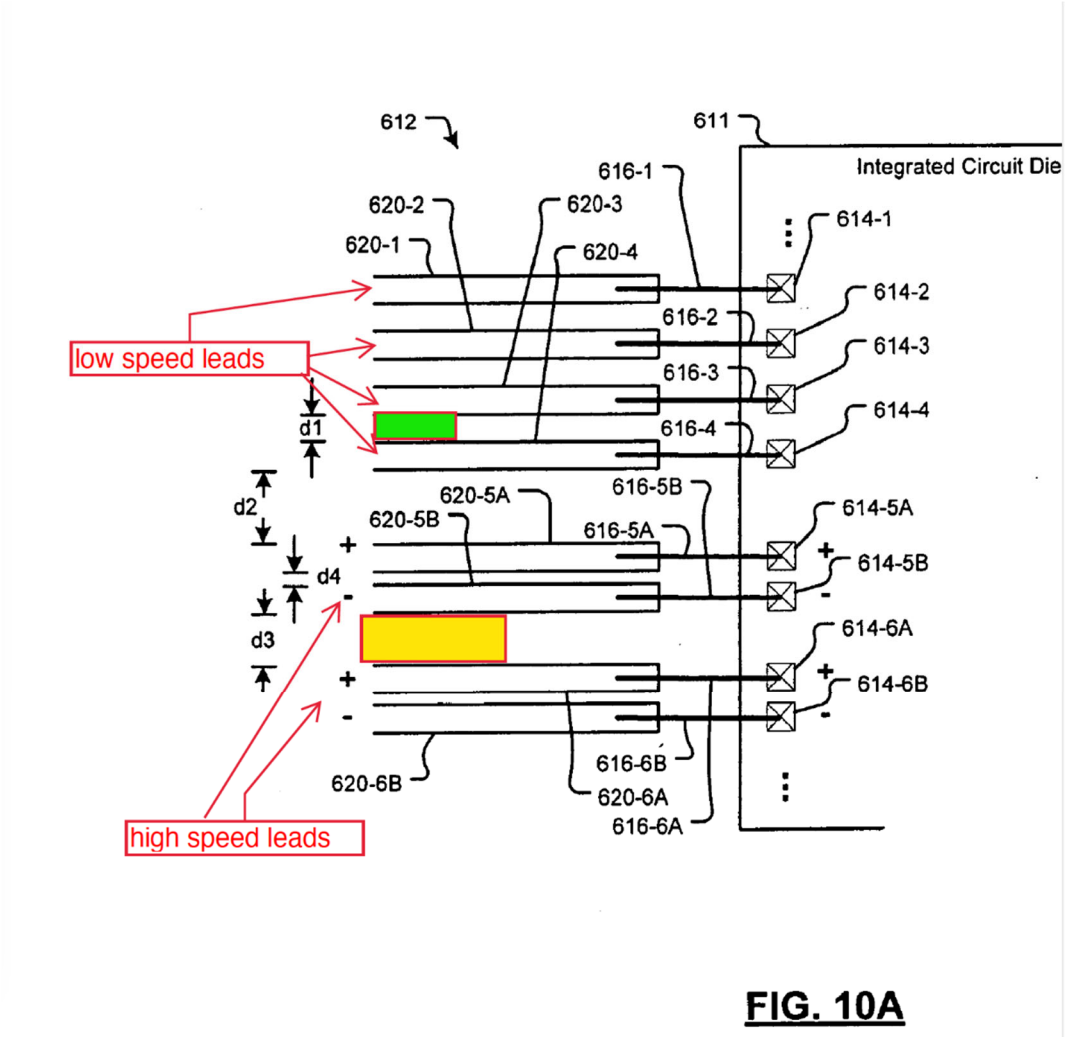


FIG. 10A

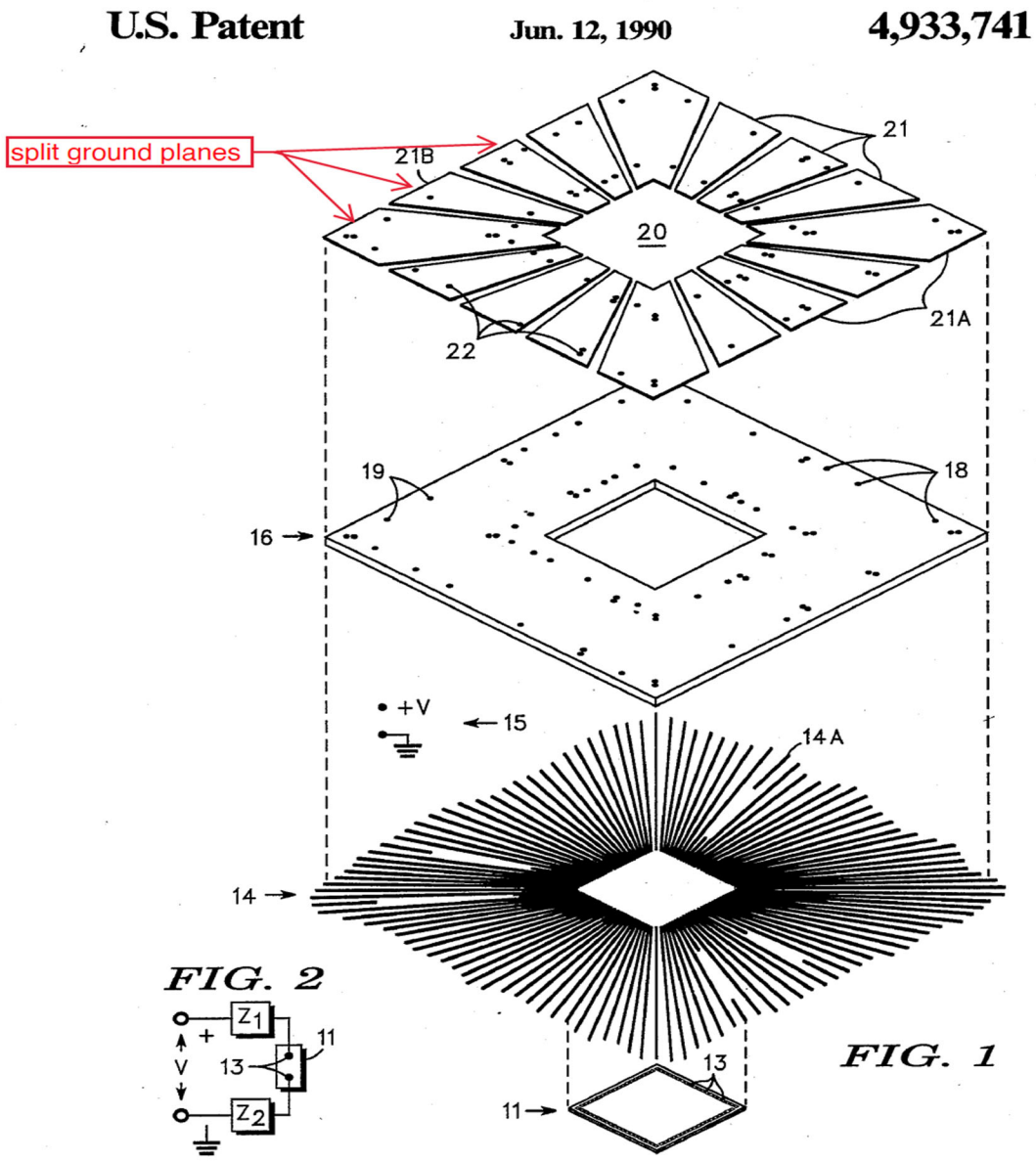
(Ex. 1012, FIG. 10A, (annotated).)

10. *Conn* (Ex. 1013)

Conn discloses a stacked die arrangement for different IC die. (Ex. 1013, Abstract) In an example, one die can be operable at frequencies much higher than another die. (*Id.*, 6:40-50) (Ex. 1002, ¶58)

11. *Schroeder* (Ex. 1008)

Schroeder discloses split ground planes 21 to reduce cross talk between conductors 14 of an integrated circuit. (Ex. 1008, 4:25-40) (Ex. 1002, ¶59)



(Ex. 1008, FIG.1 (annotated).)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; *see also Id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶35)

IX. DETAILED EXPLANATION OF UNPATENTABILITY

A. Ground 1 – *Okabe* Anticipates Claim 1.

1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

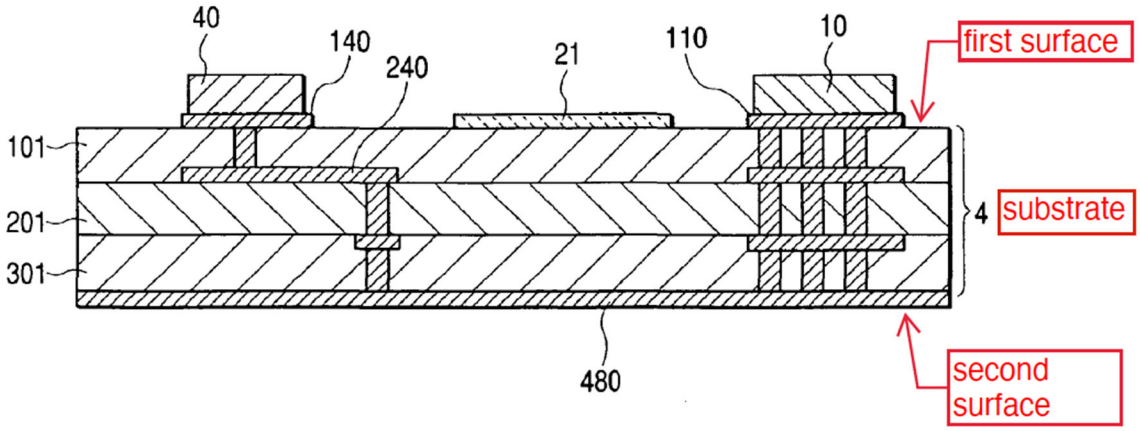
Okabe teaches this element. (Ex. 1002, ¶63) *Okabe* discloses various "circuits and chips are mounted onto a substrate of the module 1" (Ex. 1005, 13:66-67) *Okabe* further discloses prior art multi-chip modules that include integrated circuit chips

bonded to a single interconnect substrate. (*Id.*, 2:24-36) A POSITA would understand the above to be an IC package. (Ex. 1002, ¶64)

b) "a substrate having a first surface and a second surface wherein;"

Okabe teaches this element. (*Id.*, ¶65) As shown in Figure 10 below, *Okabe* discloses a substrate 4 having a first surface and a second surface.

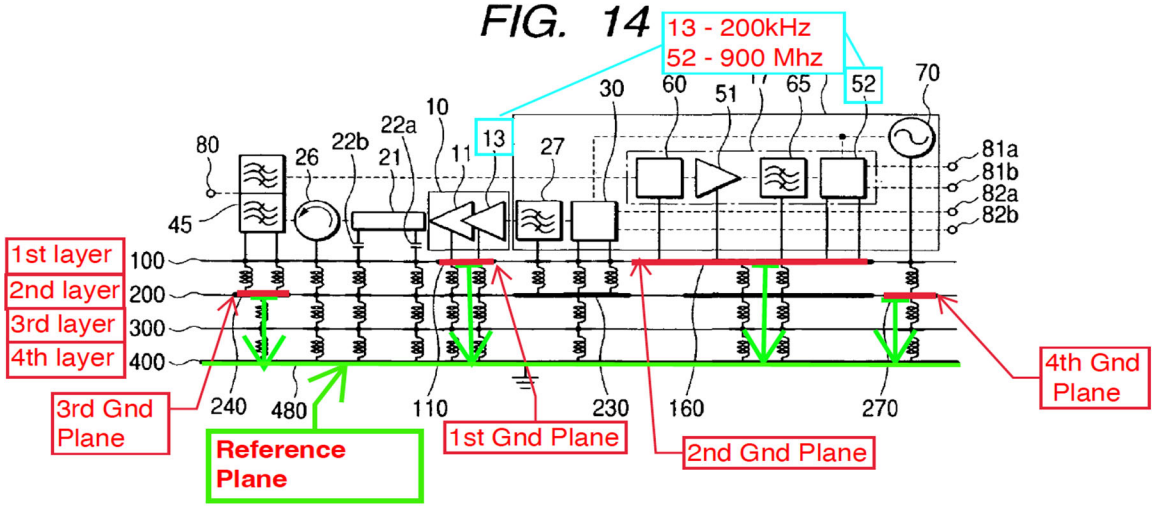
FIG. 10



(Ex. 1005, FIG. 10, (annotated).)

c) "a first layer of the substrate includes,"

Okabe teaches this element. (Ex. 1002, ¶66) *Okabe* discloses in Figure 14, shown below, a first layer 100 of the substrate 4. (Ex. 1005, 8:18-20, 9:20-22)



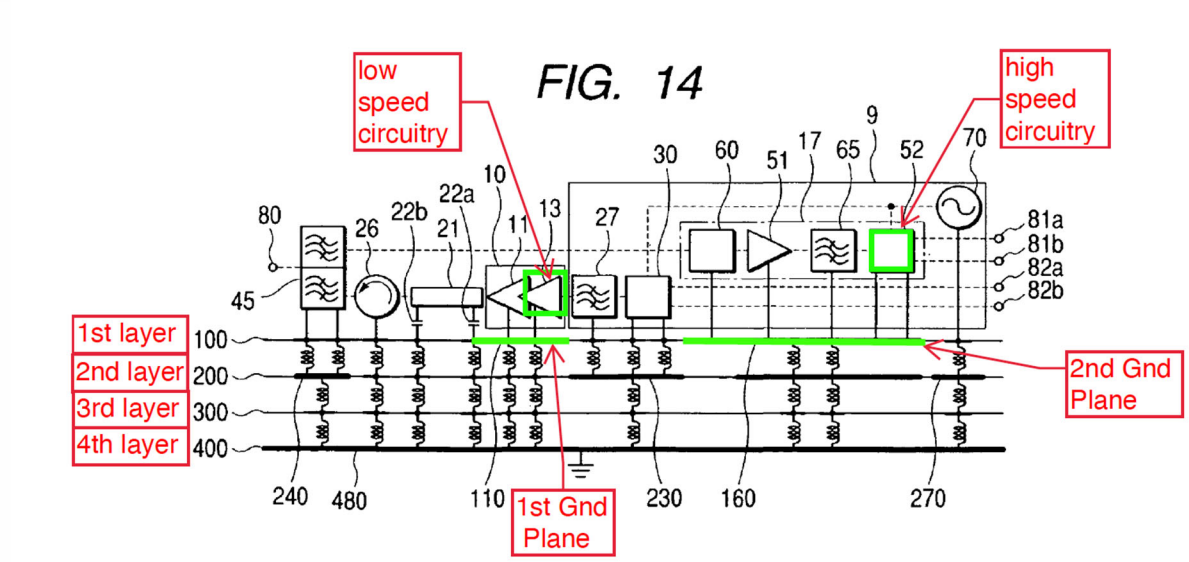
(*Id.*, FIG. 14, (annotated).)

d) "a first ground plane enabling electrical connection with low speed electronic circuitry, and"

Okabe teaches this element. (Ex. 1002, ¶67) As shown in Figure 14 above, *Okabe* discloses a first ground plane 110 on the first layer 100 of the substrate 4 (Ex. 1005, 8:8-28) (Ex. 1002, ¶67) In an example, *Okabe* teaches that circuit 13 operates in a frequency band of 200 kilohertz (kHz), while circuit 52 operates in a frequency band of 900 megahertz (MHz). (Ex. 1005, 7:36-41) Based on these frequencies, a POSITA would have understood circuit 13 is "low speed electronic circuitry". (Ex. 1002, ¶67) *Okabe* also shows circuit 13 is connected to ground plane 110 (e.g., a first ground plane). (*Id.*) (Ex. 1005, 7:52-55; 8:25-27) A POSITA would have understood that connection of the circuit 13 to the ground plane 110 would be an "electrical connection". (Ex. 1002, ¶67)

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

Okabe teaches this element. (Ex. 1002, ¶68) As shown in Figure 14, shown below, *Okabe* discloses a second ground plane 160 that is separated from and electrically isolated from the first ground plane 110. (Ex. 1005, 14:13-25, 14:64 – 15:3)



(*Id.*, FIG. 14 (annotated).)

As discussed supra in Section IX.A.1(d), *Okabe* teaches circuit 52 operates at higher speeds than circuit 52 and as such a POSITA would understand circuit 52 to be "high speed electronic circuitry". (Ex. 1002, ¶69) *Okabe* teaches the circuit 52 is electrically connected to the second ground plane 160 (*Id.*)

f) "a second layer of the substrate includes,"

Okabe teaches this element. (Ex. 1002, ¶70) As shown in Figure 14, shown above, *Okabe* discloses a second layer 200 of the substrate 4 (Ex. 1005, 8:18-21, 9:28-31)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"

Okabe teaches this element. (Ex. 1002, ¶71) Figure 14, shown above, discloses duplexer 45 connected to a third ground plane 240 on the second layer 200 of the substrate 4. (Ex. 1005, 8:27-35) A POSITA would understand duplexer 45 could operate at a lower speed than VCO 70 and thus the third ground plane 240 would be "configured for" electrical connection with "low speed electronic circuitry". (Ex. 1002, ¶71)

h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"

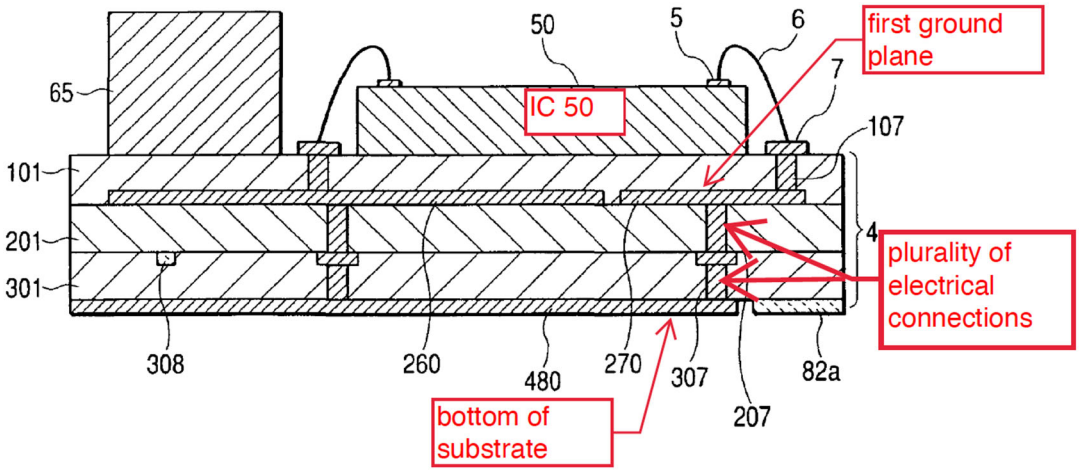
Okabe teaches this element. (Ex. 1002, ¶72) *Okabe* shows in Figure 14, shown above, a fourth ground plane 270 separated and electrically isolated from the third ground plane 240 on the same layer 200 of the substrate 4 (Ex. 1005, 14:13-33). As discussed above, a POSITA would understand that VCO 70 would be capable of operating at a higher frequency than duplexer 45, thus the fourth ground plane 270

would be "configured for" electrical connection with "high speed electronic circuitry". (Ex. 1002, ¶73)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Okabe teaches this element (Ex. 1002, ¶74). *Okabe* in figure 9, shown below, discloses a first ground plane 270 electrically connected to a bottom of a substrate 4 by way of vias 207 and 307 (a plurality of electrical connections). (Ex. 1005, 8:38-44)

FIG. 9



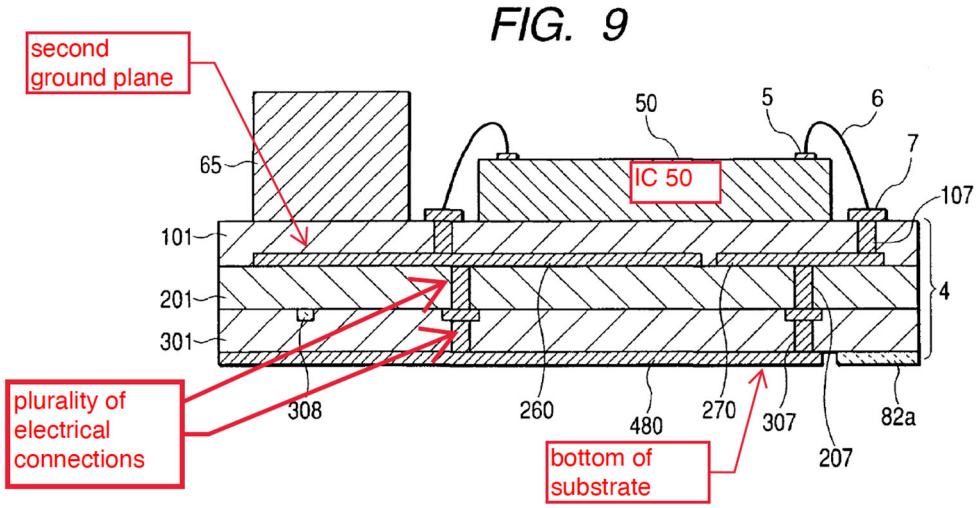
(*Id.*, FIG. 9 (annotated).)

Okabe also discloses that solder bumping may be used in a flip chip connection process. (*Id.*, 9:32-38) A POSITA would have understood that "solder bumping" when used in the context of a flip chip connection process is analogous to

solder balls, which were known to be placed on the bottom of a substrate in a flip chip process. Thus, a POSITA would have understood this to mean the solder balls could be electrically connected to ground plane 270 by way of vias 207, and 307 (e.g., a plurality of electrical connections). (Ex. 1002, ¶75)

j) "a plurality of additional electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Okabe teaches this element. (Ex. 1002, ¶76) As shown below in Figure 9, *Okabe* shows ground plane 260 (second ground plane) connected to bottom of substrate 4 by way of another set of vias (plurality of additional electrical connections). (Ex. 1002, ¶72)



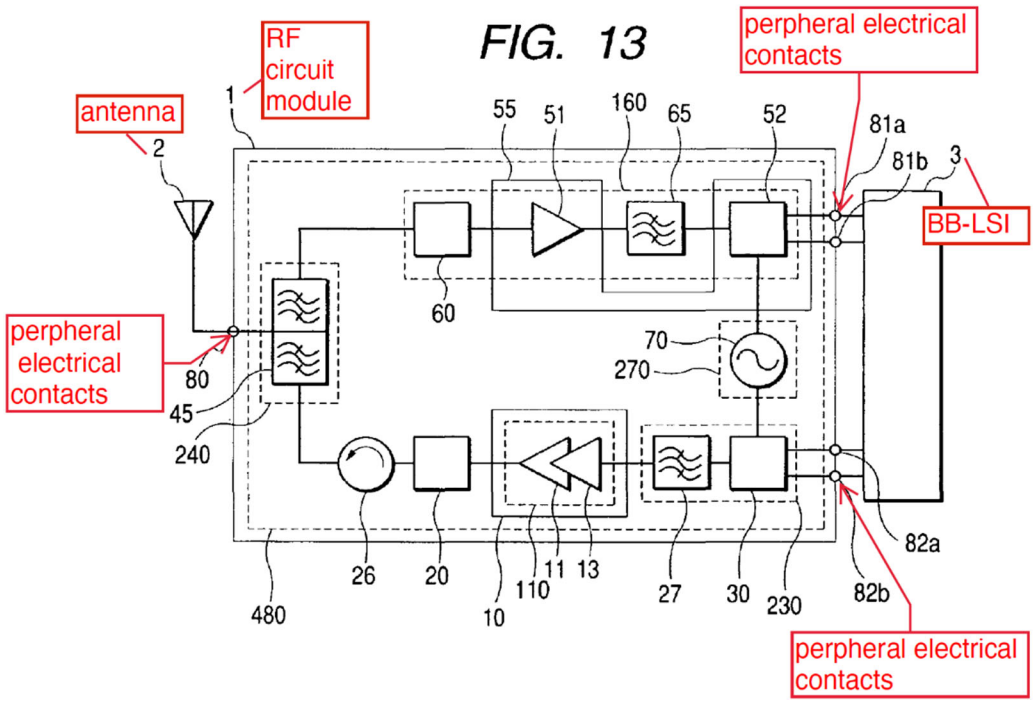
(*Id.*, FIG. 9 (annotated).)

As discussed supra in Section IX.A.1(i), *Okabe* discloses solder balls are a well-known element in IC packaging. (Ex. 1002, ¶75) As such, a POSITA would

have understood the second ground plane could also be electrically connected with the solder balls in a similar fashion to the first ground plane. (*Id.*, ¶77)

k) "peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and"

Okabe teaches this element. (*Id.*, ¶78) *Okabe* teaches in Figure 13, shown below, an antenna 2 and an BB-LSI 3 external to RF circuit module 1. A peripheral connection 80 connects switch 40 with the external antenna 2 and peripheral connections 81a-82b connect the RF module 1 with the external BB-LSI 3. (*Id.*) (Ex. 1005, 7:23-35, 13:40-45)

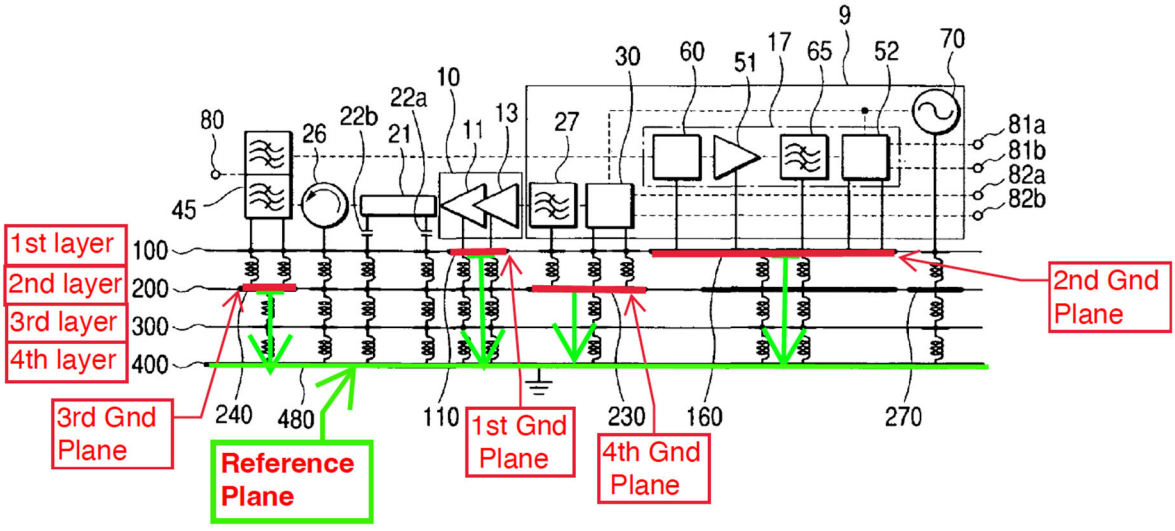


(*Id.*, FIG. 13, (annotated).)

l) "At least one reference plane associated with each layer of the substrate and the ground planes included thereon"

Okabe teaches this element. (Ex. 1002, ¶79) *Okabe* discloses in Figure 14, shown below, a common ground plane 480 associated with a first layer 100, a second layer 200, a third layer 300, and a fourth layer 400 (e.g., each layer of substrate 4) and each ground plane included on each of the four layers 100-400 (Ex. 1005, 14:13-25) *Okabe* further discloses that "by providing the module with the common ground plane 480 to which all ground planes are connected, **reference potential** for all RF circuits can be fixed, not dependent on the ground land on the motherboard." (*Id.,* 11:14-18 (emphasis added).)

FIG. 14



(*Id.*, FIG. 14 (annotated).)

As such, a POSITA would have understood the common ground plane would be "a reference plane". (Ex. 1002, ¶79)

B. Ground 2*:* Claim 1 is unpatentable as obvious over *Hashemi* in view of *Okabe*.

1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

Hashemi teaches this element. (Ex. 1002, ¶80) *Hashemi* discloses integrated circuit packages that may contain a number of bare and/or packaged integrated circuit (IC) chips. (Ex. 1006, 1:14-18, 12:9-12) (Ex. 1002, ¶81)

b) "a substrate having a first surface and a second surface wherein;"

Hashemi teaches this element. (*Id.*, ¶82) *Hashemi* shows in Figure 7 below, a substrate having an upper surface and a lower surface. (Ex. 1006, Claim 35)

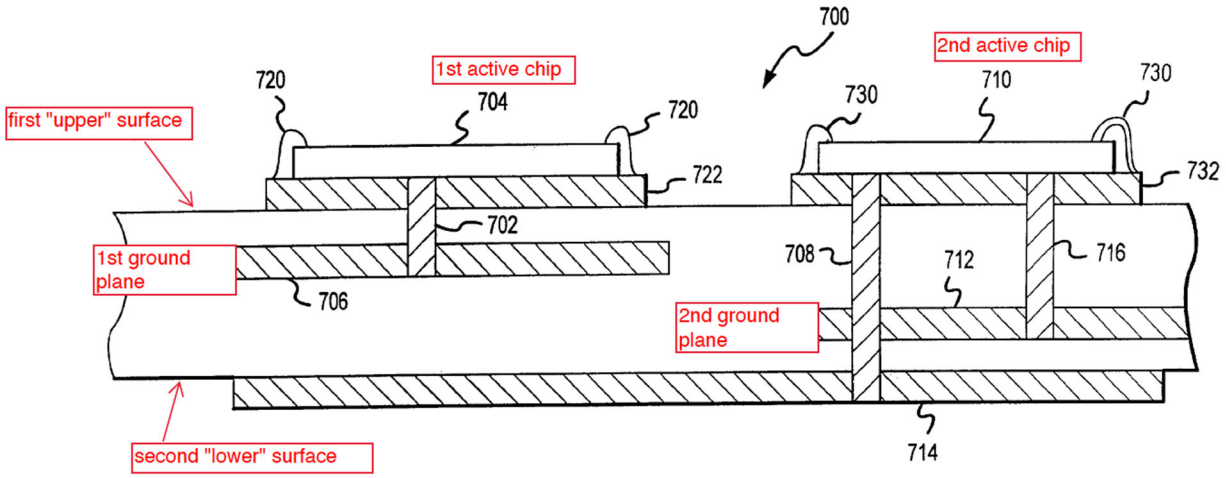


FIG.7

(*Id.*, FIG. 7 (annotated).)

c) "a first layer of the substrate includes,"

Hashemi teaches this element. (Ex. 1002, ¶83) *Hashemi* discloses the substrate may include any number of metal layers. (Ex. 1006, 4:21-34)

d) "a first ground plane enabling electrical connection with low speed electronic circuitry, and"

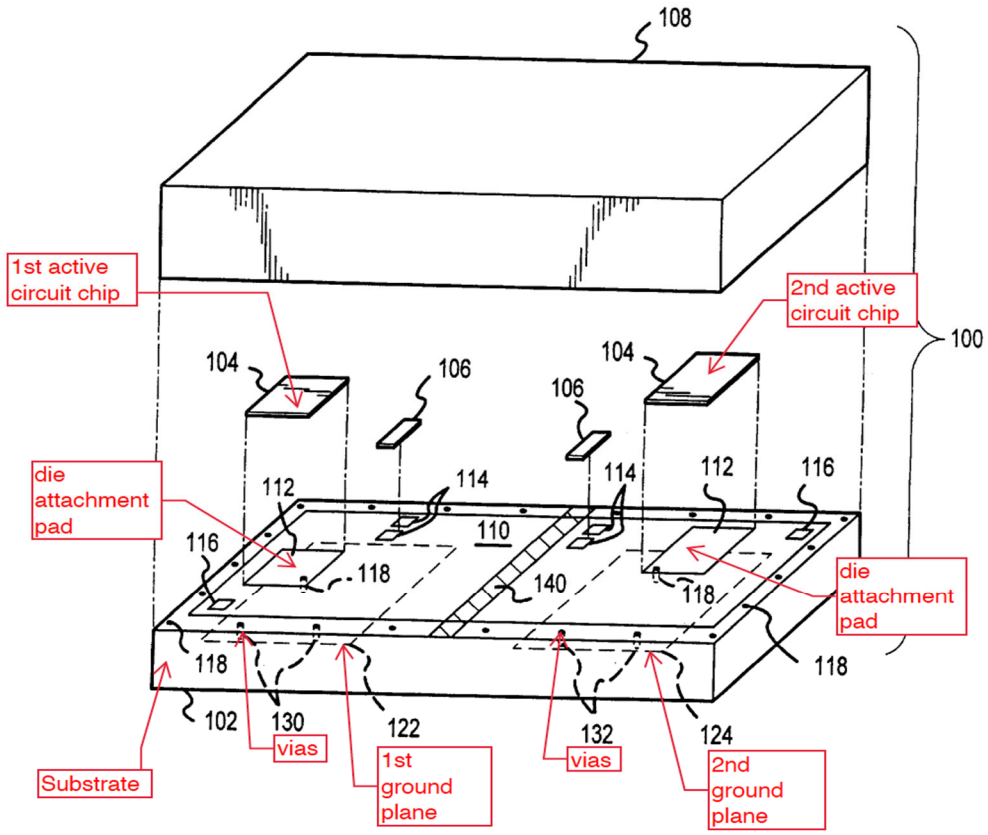


FIG.1

(*Id.*, FIG. 1 (annotated).)

Hashemi teaches this element. (Ex. 1002, ¶84) *Hashemi* discloses in Figure 1 above, vias 130 connect a first ground plane 122 to a first active chip 104. *Hashemi* further discloses the first circuit chip 104 operates at different frequencies than a second circuit chip 104 (Ex. 1006, Claim 3) (Ex. 1002, ¶84).

As such, a POSITA would have understood the first circuit chip 104 operating at lower frequencies would be "low speed electronic circuitry". (*Id*.)

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

Hashemi teaches this element. (*Id*., ¶85) As shown above in Figure 1, *Hashemi* discloses vias 132 connect second ground plane 124 with second circuit chip 104. *Hashemi* discloses that the second ground plane is physically distinct and electrically isolated from the first ground plane. (Ex. 1006, 8:4-9, Claims 15-16) (Ex. 1002, ¶85)

As discussed supra in Section IX.B.1(d), a POSTIA would have understood that the circuits 104 operating at different speeds would include the second active circuit chip 104 operating at a higher frequencies and therefore would be "high speed electronic circuitry". (*Id*., ¶86)

f) "a second layer of the substrate includes,"

Hashemi teaches this element. (*Id*., ¶87) *Hashemi* discloses a preferred embodiment where the substrate includes 2-4 metal layers (Ex. 1006, 4:28-34)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"

Hashemi teaches this element. (Ex. 1002, ¶88) As discussed supra in Section IX.B.1(d), *Hashemi* discloses electrically connecting low speed circuity with a separate ground plane. *Hashemi* also discloses "the MCM may employ split RF

ground planes, located at indeterminate metal layers or at the lower exposed metal layer". (Ex. 1006, 11:11-14) A POSITA would have understood that the split ground planes were not limited to a single layer, and as such, would include a third and fourth ground plane on another layer. (Ex. 1002, ¶88)

In the event the Patent Owner argues that Hashemi does not disclose this feature, Okabe discloses a third ground plane as discussed above. (*See supra* Section IX.A.1(g) regarding claim 1)

> **h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"**

Hashemi teaches this element. (Ex. 1002, ¶89) As discussed above in Sections IX.B.1(g) and IX.B.1(e), *Hashemi* teaches the split ground planes are not limited one layer and teaches the split ground planes are electrically isolated and physically distinct. As such, it would have been clear to a POSITA that the split ground planes feature could be implemented at a different layer, and thus would include a third and fourth ground plane on a second layer of a multi-layered substrate. (*Id.*) A POSITA would take note that '091 Patent does not disclose any difference between a third and fourth ground plane on a second layer versus a first and second ground plane on a first layer. (*Id.*)

In fact, the Patent Owner admitted this by stating "the third and fourth ground planes **are analogous to** the first and second ground planes recited in claim 1, where

the first ground plane enables 'electrical connection with low speed electronic circuitry' and the second ground plane enables 'electrical connection with high speed electronic circuitry'". (Ex. 1004, p. 251 (emphasis added).)

In the event the Patent Owner argues that Hashemi does not disclose this feature, Okabe discloses third and fourth ground planes as discussed above. (*See supra* Section IX.A.1(g-h) regarding claim 1)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Hashemi teaches this element. (Ex. 1002, ¶90) *Hashemi* discloses that MCMs may employ a ball grid array and that solder balls may be used as a termination device at the bottom of the MCM. (Ex. 1006, 12:21-25) *Hashemi* further discloses in the description of Figure 7, shown below, an internal ground plane may be "connected to a suitable ground termination". (*Id.*, 6:61-63) A POSITA would have understood that being "connected to" solder balls would include a plurality of electrical connections and that the bottom of the MCM would be the second surface of the substrate. (Ex. 1002, ¶90)

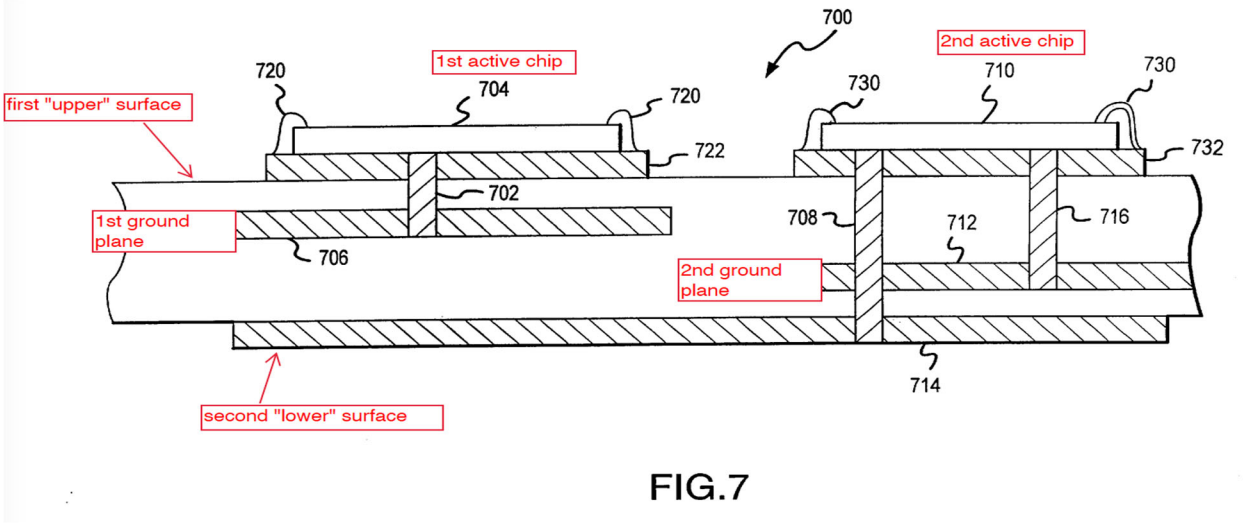


FIG.7

(Ex. 1006, FIG. 7 (annotated).)

j) "a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Hashemi teaches this element. (Ex. 1002, ¶91) *Hashemi* discloses that solder balls may be used as a termination device at the bottom of the MCM. (Ex. 1006, 12:21-25) Hashemi further discloses that an internal ground plane may be "connected to a suitable ground termination" (*Id.*, 6:61-63), and discloses any of the split ground planes may be electrically connected using vias to die attach pads. (*Id.* 7:13-27)

k) "peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and"

Hashemi teaches this element. (Ex. 1002, ¶92) *Hashemi* teaches solder balls are used as a termination device. (*Id.*) (Ex. 1006, 12:21-25) A POSITA would understand this to be peripheral electrical contacts for connection with electronic

circuitry external to the package. (Ex. 1002, ¶92) However, in the event the Patent Owner argues that *Hashemi* does not disclose this limitation, *Okabe* discloses this limitation (*See supra* Section IX.A.1(k) regarding claim 1) (Ex. 1002, ¶93)

l) "At least one reference plane associated with each layer of the substrate and the ground planes included thereon"

The *Hashemi-Okabe* combination teaches this element. (Ex. 1002, ¶94) *Okabe* discloses this limitation (*See supra* Section IX.A.1(l) regarding claim 1) (Ex. 1002, ¶94) A POSITA implementing the MCM package of *Hashemi* would have good reason to look to *Okabe* to provide a common reference plane to remove variance of the potential of the separate grounds of *Hashemi*, as they are both in the same field of integrated circuits packages. (Ex. 1002, ¶95) Moreover, such a POSITA implementing the IC package of Hashemi would be motivated to include the reference plane of Okabe to provide stable performance by fixing reference potentials for the integrated circuit which are not dependent on ground lands of a motherboard as disclosed by Okabe (Ex. 1005, 11:14-19) (Ex. 1002, ¶95)

C. Ground 3: Claims 1 and 12 are unpatentable as obvious over *Okabe* in view of *Applicant's Admitted Prior Art* (*AAPA).*

1. Claim 1

a) "A semiconductor integrated circuit (IC) package which comprises:"

Okabe teaches this element. (*See supra* Section IX.A.1(a) regarding claim 1) (Ex. 1002, ¶¶97-98)

AAPA also teaches this element. (*Id*., ¶¶99-100) The '091 Patent discloses "the semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate." (Ex. 1001, 1:15-17); (Ex. 1002, ¶¶99-100)

b) "a substrate having a first surface and a second surface wherein;"

Okabe teaches this element. (*See supra* Section IX.A.1(b) regarding claim 1) (Ex. 1002, ¶101)

APPA also teaches this element. (*Id*., ¶102) The '091 Patent discloses it was widely known to use packaging substrates for ICs. (Ex. 1001, 1:16-20) (Ex. 1002, ¶102)

c) "a first layer of the substrate includes,"

Okabe teaches this element. (*See supra* Section IX.A.1(c) regarding claim 1) (*Id*., ¶103)

AAPA also teaches this element. (*Id*., ¶103) The '091 Patent discloses as *AAPA* an IC package includes layers. (Ex. 1001, 1:30-32; 5:1-2) (Ex. 1002, ¶103)

d) "a first ground plane enabling electrical connection with low speed electronic circuitry, and"

Okabe teaches this element. (*See supra* Section IX.A.1(d) regarding claim 1) (Ex. 1002, ¶¶104-106)

AAPA teaches this element. (*Id*., ¶106) The '091 Patent discloses as *AAPA* that high and low speed circuitry were commonly known in the art and could be electrically connected to a ground plane (Ex. 1001, 1:64-67 ["in the depicted die 101 the **high speed portions** of the die and **low speed portions** of the die are electrically connected to the same ground plane Vss 111." emphasis added)]) (Ex. 1002, ¶106)

e) "a second ground plane that is spatially separated and electrically isolated from the first ground plane, the second ground plane enabling electrical connection with high speed electronic circuitry;"

Okabe teaches this element. (*See supra* Section IX.A.1(e) regarding claim 1) (Ex. 1002, ¶¶107-108)

f) "a second layer of the substrate includes,"

Okabe teaches this element. (*See supra* Section IX.A.1(f) regarding claim 1) (Ex. 1002, ¶109)

AAPA also teaches this element. (*Id*., ¶109) The '091 Patent discloses as *AAPA* an IC package includes **layers**. (Ex. 1001, 1:30-32, 5:1-2 (emphasis added).)

g) "a third ground plane configured for electrical connection with low speed electronic circuitry, and"

Okabe teaches this element. (*See supra* Section IX.A.1(g) regarding claim 1) (Ex. 1002, ¶110)

h) "a fourth ground plane that is spatially separated and electrically isolated from the third ground plane, the fourth ground plane configured for electrical connection with high speed electronic circuitry, and"

Okabe teaches this element. (*See supra* Section IX.A.1(h) regarding claim 1) (Ex. 1002, ¶111)

i) "a plurality of electrical connections that electrically connect the first ground plane with solder balls mounted on the second surface of the substrate"

Okabe teaches this element. (*See supra* Section IX.A.1(i) regarding claim 1) (Ex. 1002, ¶112)

AAPA also teaches this element. (*Id*., ¶113) The '091 Patent discloses that the prior art teaches solder balls on a bottom of a substrate are electrically connected to a ground layer, either via fingers to vias or directly via interlayer vias. (Ex. 1001, 1:51-67; 4:37-42 ["when the principles of the invention are applied to ball grid array (BGA) type packages, these contacts are typically facilitate[d] by conductive vias that pass through the substrate and are electrically connected to both, a ground plane and an underlying solder pad. Solder balls are then used to make the external ground connections to other grounds".]) The '091 Patent further discloses as *AAPA* that the

packaging substrate 600 can be "an ordinary multi-layer BGA substrate 600" (*Id.*, 7:34-35) (Ex. 1002, ¶113)

As such, a POSITA would have understood that a normal (ordinary) BGA substrate would provide a plurality of electrical connections to connect a ground plane with solder balls mounted on a second surface (e.g., bottom) of the BGA substrate. As such, a POSITA would understand that solder balls could be mounted on the bottom of *Okabe's* substrate 4 (see annotated Fig. 9 of *Okabe* above at pg. 34 of this petition) and that *Okabe's* vias 207 and 307 would be a "plurality of electrical connections" to electrically connect *Okabe's* ground plane 270 with the solder balls. (*Id*., ¶114)

j) "a plurality of electrical connections that electrically connect the second ground plane with solder balls mounted on the second surface of the substrate"

Okabe teaches this element. (*See supra* Section IX.A.1(j)) (Ex. 1002, ¶115) However, if Patent Owners contend that *Okabe* does not teach solder balls mounted on the second surface electrically connected to a ground plane via a plurality of electrical connections, *AAPA* teaches this element. (*Id.*)

The '091 Patent discloses that the prior art taught solder balls mounted on a bottom surface of a BGA package. The '091 Patent further discloses that "typically, metallization lines 115 electrically connects the fingers to vias (not shown) that connect with solder balls on the bottom of the substrate. In some configurations the

fingers 114 are typically connected to the ground plane". (Ex. 1001, 1:50-61) (Ex. 1002, ¶115)

k) "peripheral electrical contacts arranged on the substrate and configured for connection with electronic circuitry external to the package; and"

Okabe teaches this element. (*See supra* Section IX.A.1(k) regarding claim 1) (Ex. 1002, ¶116)

AAPA also teaches this element. (*Id*., ¶117) The '091 Patent discloses as *AAPA* that "the semiconductor industry makes wide use of packaging substrates to hold and electrically interconnect integrated circuit (IC) die mounted within the packaging substrate. In some implementations the packaging substrates are configured to protect and secure the delicate IC die while enabling electrical connections with known **external** electrical interconnection socket formats." (Ex. 1001, 1:16-22) A POSITA would have understood that external electrical interconnection socket formats would include peripheral electrical contacts arranged on the substrate configured for connection with circuitry external to an IC package. (Ex. 1002, ¶117)

l) "At least one reference plane associated with each layer of the substrate and the ground planes included thereon"

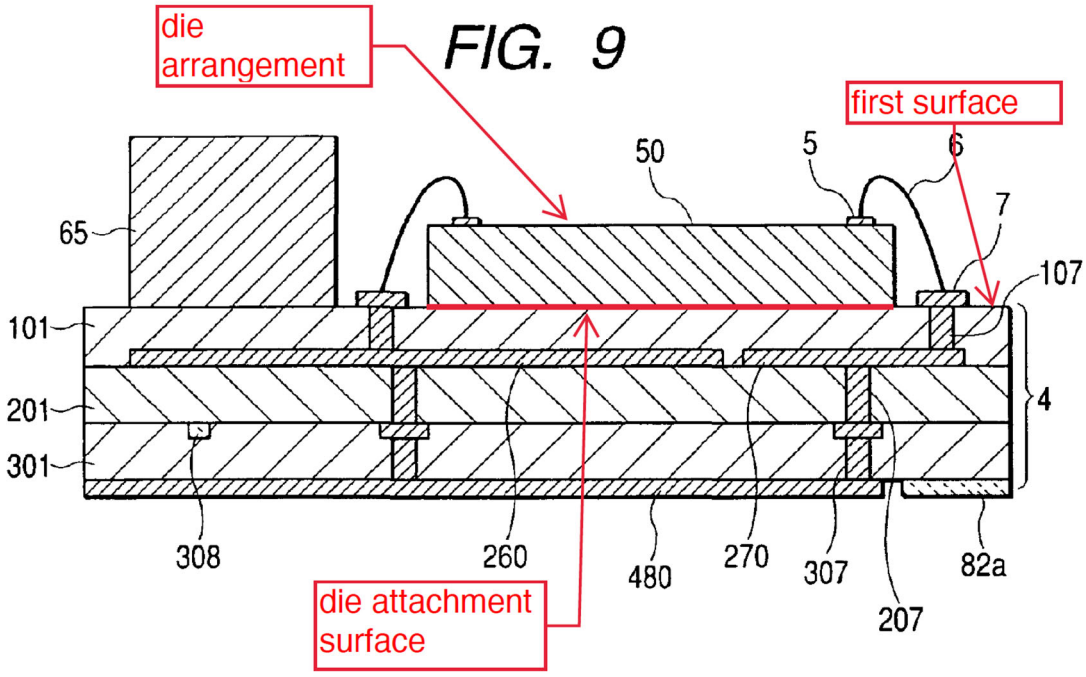
Okabe teaches this element. (*See supra* Section IX.A.1(l) regarding claim 1) (*Id.*, ¶118).

2. Claim 12

a) "An IC package as recited in claim 1, wherein the first surface includes a die attachment surface with a die arrangement attached thereto"

Okabe teaches this element (*Id.*, ¶121)

Okabe discloses in Figure 9, shown below, an IC 50 is attached to a first surface of substrate 4 at a particular area of the substrate (die attachment surface). (Ex. 1005, 9:9-14)



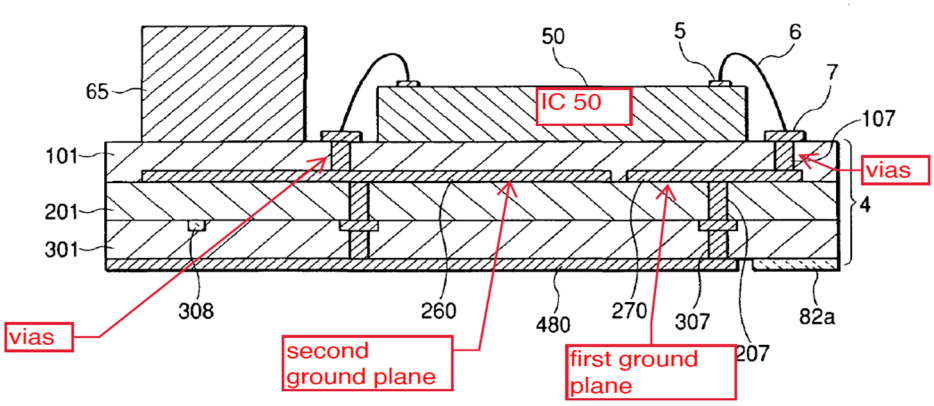
(*Id.*, FIG 9 (annotated).)

However, if Patent Owners contend that *Okabe* does not teach a "die attachment surface", *AAPA* teaches this element. (Ex. 1002, ¶122)

The '091 Patent discloses as *AAPA* "in one common implementation semiconductor die is attached to the substrate …. such packages and the methods of their construction are well known to persons having ordinary skill in the semiconductor packaging arts." (Ex. 1001, 1:35-42) As such, a POSITA would have known that the top of *Okabe's* substrate where the IC is mounted, would be a "die attachment surface". (Ex. 1002, ¶122)

b) "the die arrangement being electrically connected to the first ground plane, the second ground plane, and the peripheral electrical contacts of the substrate"

Okabe teaches this element (Ex. 1002, ¶123). *Okabe* discloses an IC being electrically connected to a first ground plane and a second ground plane on a substrate. For example, Figure 9, shown below, shows an integrated circuit 50 connected (e.g., by way of ground pad 5, bond wire 6, bonding pad 7, and via 107) to a first ground plane 270 and a second ground plane 260. (Ex. 1005, 9:24-31)



(*Id.*, FIG. 9 (annotated).)

Okabe further discloses the IC being electrically connected to terminals 81a-82b, which are on the peripheral of the substrate module (*Id.*, 7:4-15, 23-35, 8:29-40)

In the event the Patent Owner argues *Okabe* does not disclose a die arrangement electrically connected to peripheral contacts, *AAPA* also teaches this element. (Ex. 1002, ¶¶125-126)

The '091 Patent discloses peripheral contacts in Figure 1, shown below, as fingers 114 and metallization lines 115 that are electrically connected to die 101 via bond pads 102 and wires 103. (*Id.*, ¶125)

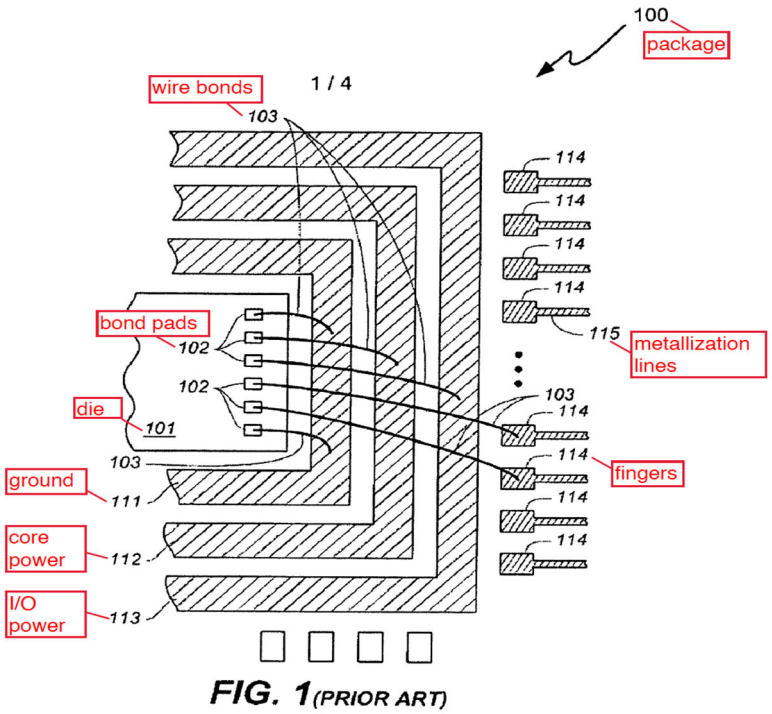


FIG. 1 (PRIOR ART)

(Ex.1001, FIG. 1 (annotated).)

As such, even in a scenario where *Okabe* did not disclose a die electrically connected to peripheral contacts, it would have been obvious to a POSITA to modify *Okabe* substrate to provide electrical connections from an IC die arrangement to peripheral contacts. (Ex. 1002, ¶126) The modification of *Okabe* with the teachings of *AAPA* would have amounted to nothing more than the use of a known technique to improve a similar device, and the results of the modification would have been predictable. (*Id.*) This is because at the time of the invention, a POSITA would have had the requisite skill level to readily modify the IC package disclosed by *Okabe* to implement the teachings of electrical connections to peripheral contacts disclosed by *AAPA* in order to route power and signals from an IC to a PCB. (*Id.*) Moreover, such modification of Okabe would have been routine for the POSITA as they would be using well-known elements with no change in their respective functions. (*Id.*)

D. Ground 4: Claims 2, 5, 6, and 9 are unpatentable as obvious over *Okabe*, in view of *Applicant's Admitted Prior Art* (*AAPA)* and *Sutardja*.

1. Claim 2

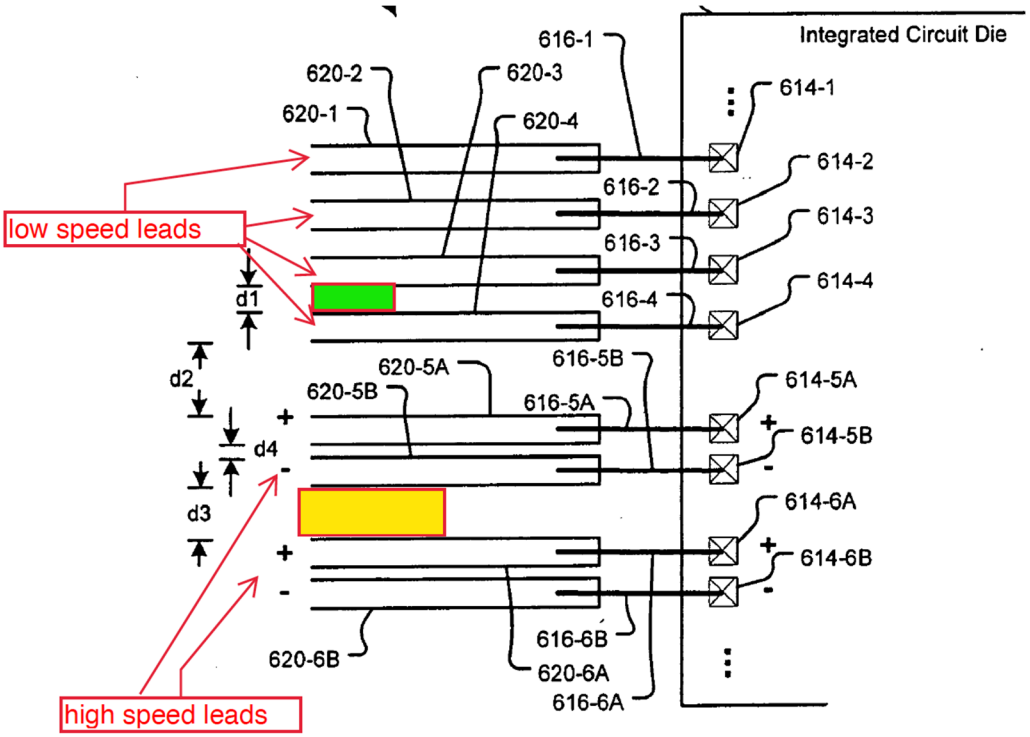
a) "An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with the low speed circuitry, and"

b) "a second set of electrical contacts for electrical connection with the high speed electronic circuitry; and"

Okabe-AAPA-Sutardja teaches these elements. (Ex. 1002 ¶128) The Okabe-AAPA combination teaches an IC package with peripheral electrical contacts for electrical connection with low speed and high speed circuitry. (See supra Section IX.C.1(a-f) regarding claim 1)

As shown below in Figure 10A below, Sutardja also discloses this claim limitation by disclosing an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through

620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (*Id.* ¶139)



(*Id.*, FIG. 10A (annotated).)

A POSITA would have understood that the leads operating at a lower speed would be a first set of electrical contacts for electrical connection with low speed circuitry and the leads operating at a higher speed would be a second set of electrical contacts for electrical connection with high speed circuitry. (Ex. 1002, ¶129)

c) "wherein the second set of electrical contacts are spaced apart at a distance that is at least twice as far apart as the spacing for the first set of electrical contacts."

Sutardja shows in Figure 10A above, that the second set of leads appear to be twice as far apart as the first set of leads, but does not explicitly state this. However,

Sutardja does state that the distances between the high and low speed leads "may be irregular to increase or decrease coupling" (Ex. 1012, ¶0139)

It would be obvious to a POSITA to modify the distances of a first and second set of electrical contacts to "increase or decrease coupling" as disclosed by Sutardja and a spacing for the second set of at least twice as far apart as the first set, as inherently disclosed by Sutardja, would be obvious to try for a POSITA. (Ex. 1002, ¶131)

A POSITA would have known that spacing between the leads (electrical contacts) affects the coupling. Thus, such a person would have been motivated to modify the spacing of the leads to minimize cross talk and/or maintain impedance accuracy of such low and high speed leads. (Ex. 1002, ¶132)

A POSITA implementing an IC package like that of the Okabe-AAPA combination would have had good reason to look to Sutardja, particularly because all of these references are in the same field of integrated circuit packages. Having looked to Sutardja, such a POSITA would have been motivated to utilize the spacing of the electrical contacts with characteristics suitable for connection with low speed circuitry as disclosed by Sutardja for the peripheral electrical contacts of the IC package of Okabe-AAPA to ensure impedance accuracy and minimize cross-talk (increase or decrease coupling). (Ex. 1002, ¶133)

Moreover, a POSITA would have found it straightforward to space the high and low speed leads as disclosed by Sutardja. Such an implementation would have simply been the application of a known device (IC with low speed contacts) to a similar device (IC) and would have produce predictable results (increase or decrease coupling). As such, the *Okabe-AAPA-Sutardja* combination discloses or suggests this claim limitation. (Ex. 1002, ¶134)

2. Claim 5

a) "An IC package as recited in claim 1, wherein the low speed electronic circuitry is defined as circuity having serial transfer rates of less than about 1 Gigabits per second (Gb/s); and"

The *Okabe-AAPA* combination discloses an IC package with low speed electronic circuitry, but does not explicitly state low speed is defined as less than 1 Gb/s. (*See supra* Section IX.C.1(d) regarding claim 1) (Ex. 1002, ¶¶104-105, 136) However, *Sutardja* discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, ¶139) *Sutardja* further discloses that the high speed leads are operable to for high speed signals that are "greater than or equal to 1 Gigabit per second". (*Id.*, ¶75) A POSITA would have understood that if high speed is greater than or equal to 1 Gb/s, than low speed would be less than 1 Gb/s. (Ex. 1002, ¶136)

b) "wherein the high speed electronic circuitry is defined as circuity having serial transfer rates of greater than about 1 Gb/s."

As discussed above, *Sutardja* discloses an integrated circuit die connected to low speed leads and high speed leads. (Ex. 1012, ¶139) *Sutardja* further discloses that the high speed leads are operable to for high speed signals that are "greater than or equal to 1 Gigabit per second". (*Id.*, ¶75)

A POSITA would take note that the '091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of "greater than about 1 Gb/s [gigabits per second]" recited in claim 5. (Ex. 1002, ¶138)

3. Claim 6

a) "An IC package as recited in claim 1 wherein the high speed electronic circuitry is defined as circuity having serial transfer rates of greater than about 8.5 Gb/s."

The *Okabe-AAPA* combination teaches an IC package having high speed circuitry, but does not explicitly state high speed is defined by 8.5 Gb/s. (*See supra* Section X.C.1(e) regarding claim 1) (Ex. 1002, ¶140) However, *Sutardja* discloses high speed leads are operable to for high speed signals that are "greater than or equal to 1 Gigabit per second". (Ex. 1012, ¶75) A POSITA would have understood that if high speed is greater than or equal to 1 Gb/s, that would include speeds of 8.5 Gb/s. (Ex. 1002, ¶140)

A POSITA would take note that the '091 Patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the specific speed of "greater than about 8.5 Gb/s" recited in claim 6. (Ex. 1002, ¶141) A POSITA would also take note that the '091 Patent does not provide any structural difference to the IC package or the high speed electronic circuitry in claims 5 and 6 when differentiating between purported high speed thresholds of 1 Gb/s in claim 5 and 8.5 Gb/s in claim 6. As has been shown in numerous contemporaneous reference mentioned above, speeds of 1 Gb/s and 8.5 Gb/s were well known in the art. (*Id.*)

4. Claim 9

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with the low speed circuitry, and"

Okabe-AAPA-Sutardja teach this element. (*See supra* Section IX.D.1(a-b) regarding claim 2) (Ex. 1002, ¶142)

b) "a second set of electrical contacts for electrical connection with the high speed circuitry; and"

Okabe-AAPA-Sutardja teach this element. (*See supra* Section IX.D.1(a-b) regarding claim 2) (Ex. 1002, 143).

c) "wherein the electrical contacts are arranged such that, a first spacing between the contacts of the first set of electrical contacts is smaller than a second spacing between the contact of the second set of electrical contacts, thereby enabling greater contact density for the first set of electrical contacts."

Sutardja discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads. This spacing "may be irregular to increase or decrease coupling". (Ex. 1012, ¶139) *Sutardja* shows in Figure 10A that the spacing (d1) between the first set of electrical contacts is smaller than the spacing (d3) between the second set of electrical contacts. Thus, it would have been obvious to a POSITA that the smaller spacing of the first set of electrical contacts (low speed leads) would be "enabling greater contact density for the first set of electrical contacts". (Ex. 1002, ¶145)

A POSITA implementing an IC package that of Okabe-AAPA would have had good reason to look to *Sutardja* as these references are in the same field of IC packages. Having looked to Sutardja, such a POSITA would have been motivated to use the decreased spacing of *Sutardja* in order to enable more contacts for the Okabe-AAPA IC package. (Ex. 1002, ¶146)

Moreover, a POSITA would have found it straightforward to decrease spacing to enable more contact density for the low speed signals where spacing is generally not an issue due to less crosstalk issues with low speed signals. (Ex. 1002, ¶147)

E. Ground 5: Claims 3, 4 and 7 are unpatentable as obvious over *Okabe*, in view of Applicant's Admitted Prior Art (*AAPA)*, *Sutardja* and *Taggart*.

1. Claim 3

a) "An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 um (micrometers)"

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (Ex. 1002, ¶149) *Okabe-AAPA-Sutardja* teaches an IC package with a first set of electrical contacts spaced to minimize cross talk and/or maintain impedance accuracy (increase or decrease coupling), but does not explicitly use 70 um. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶149)

However, *Taggart* discloses a distance (pitch or spacing) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers. (Ex. 1009, ¶27) A POSITA working with the *Okabe-AAPA-Sutardja* IC package would look to *Taggart* as they are all in the integrated circuit packaging fields. Moreover, a POSITA would have understood that any sets of wire-bond pads, wire-bonds, and die bond pads would be "electrical contacts" and the 70 micrometers would be in the range of about 10-200 micrometers. Such a person would have been motivated to space electrical contacts of the IC package of Okabe-AAPA-Sutardja with the ranges of Taggart to increase or decrease coupling which

would minimize cross talk and/or maintain impedance accuracy for the electrical contacts as was very well known in the art. (Ex. 1002, ¶150)

b) "and wherein the second set of electrical contacts are spaced apart a distance of at least 140 um (micrometers)"

Okabe-AAPA-Sutardja teaches an IC package with a second set of electrical contacts spaced to increase or decrease coupling, but does not explicitly disclose a spacing of 140 micrometers. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶151)

However, *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers, (Ex. 1009, ¶27), with a specific embodiment where the pitch is about 135 micrometers (*Id.*, Claim 13). A POSITA would have understood that any other of the sets of wire-bond pads, wire-bonds, and die bond pads would be second "electrical contacts" and the 140 micrometers would be in the range of about 10-200 micrometers and specifically "about 135 micrometers" as disclosed by *Taggart*. (Ex. 1002, ¶139)

2. Claim 4

a) "An IC package as recited in claim 2, wherein the first set of electrical contacts are spaced apart a distance of at least 70 um (micrometers)"

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (*See supra* Section IX.E.1(a) regarding claim 3) (Ex. 1002, ¶¶154-155)

b) "and wherein the second set of electrical contacts are spaced apart a distance of at least 200 um (micrometers)"

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (Ex. 1002, ¶156) *Taggart* discloses a distance (pitch) between wire-bond pads, wire-bonds, and die bond pads within a range from about 10 micrometers to about 200 micrometers, and gives a specific example of the wire-bond pads, the die bond pads, and the wire-bonds "spaced on 200 um centers". (Ex. 1009, ¶27) (Ex. 1002, ¶156)

3. Claim 7

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with the low speed circuitry; and"

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (Ex. 1002, ¶151) The *Okabe-AAPA* combination teaches an IC package with peripheral electrical contacts for electrical connection with low speed circuitry (*See supra* Section IX.C.1(a-d), Ex. 1002, ¶158) As shown below in Figure 10A, *Sutardja* discloses an integrated circuit (IC) package that includes an IC die having die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (*Id.* ¶139)

A POSITA would have understood that the leads operating at a lower speed would be a first set of electrical contacts for electrical connection with low speed circuitry. (Ex. 1002, ¶159)

b) "a second set of electrical contacts for electrical connection with the high speed circuitry, and"

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (Ex. 1002, ¶160) As shown below in Figure 10A, *Sutardja* discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (Ex. 1012, ¶139) A POSITA would have understood that die pads 614-5A through 614-6B, bondwires 616-5A through 616-6B, and "high speed leads" 620-5A through 620-6B would be equivalent to "a second set of electrical contacts for electrical connection with high speed circuitry". (Ex. 1002, ¶153) A POSITA would have understood that die pads 614-1 through 614-4, bondwires 616-1 through 616-4, and "low speed leads" 620-1 through 620-4 would be equivalent to "a first set of electrical contacts for electrical connection with low speed circuitry". (*Id.*)

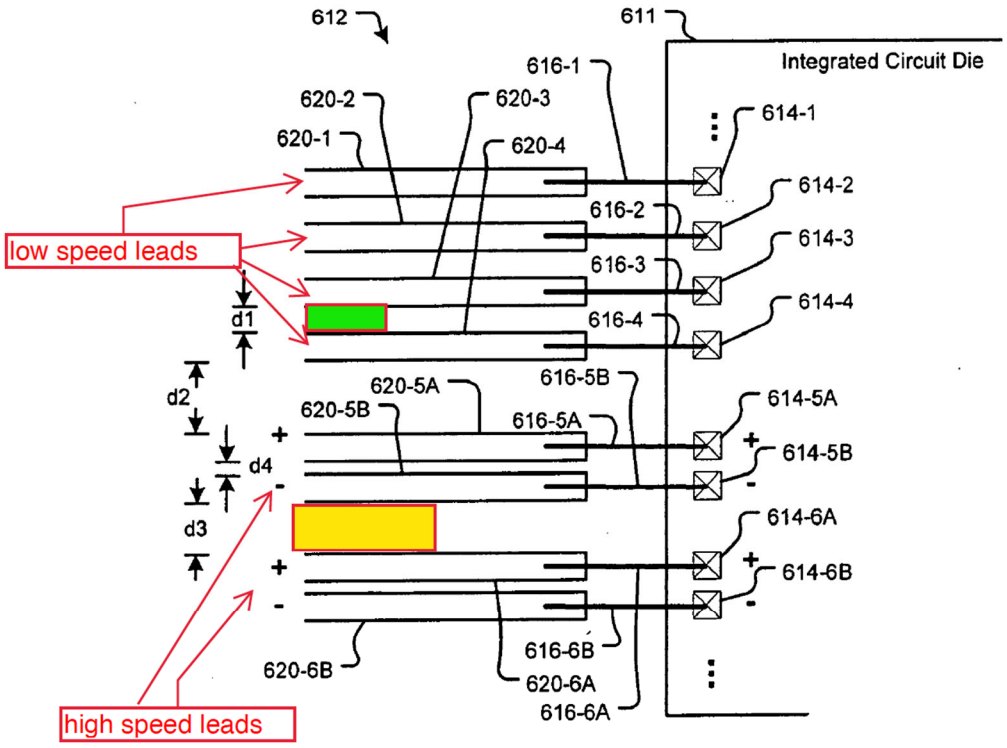


FIG. 10A

(Ex. 1012, FIG. 10A (annotated).)

c) wherein the second set of electrical contacts are spaced apart at a distance that is at least three times as far apart as the spacing for the first set of electrical contacts."

The *Okabe-AAPA-Sutardja-Taggart* combination teaches this element. (Ex. 1002, ¶161) *Sutardja* discloses various spacing between the low speed leads, the high speed leads, and between the low and high speed leads and explicitly states that "this spacing "may be irregular to increase or decrease coupling" (*Id.,* ¶139). Although *Sutardja* shows in Figure 10A above that the spacing (d3) between the second set of electrical contacts is larger than the spacing (d1) between the first set

of electrical contacts, *Sutardja* does not explicitly state the d3 spacing is "at least three times as far apart" as the d1 spacing. (*Id*., ¶161)

Taggart discloses an integrated circuit (IC) package that includes an IC die having die bond pads connected to wire-bond pads via bond wires. *Taggart* further discloses spacing any of the die bond pads, wire-bond pads, and bond wires in accordance with a pitch that ranges from "about 10 um [micrometers] to 200 um". (Ex. 1009, ¶27) A POSITA would have understood that this range would include many pitch values that would be 3x greater than other pitch values in the ranges. (Ex. 1002, ¶155) For example, a first pitch value of 10 um would leave 30 um – 200 um values that would all be at least three times greater than 10 um. (*Id.*)

A POSITA would have good reason to look to *Taggart* to modify the *Okabe-AAPA-Sutardja* IC package with spaced electrical contacts to select values within 10 um - 200 um to increase or decrease coupling between the high or low speed leads as needed. (*Id.*, ¶163) Because *Taggart* and *Sutardja* both disclose integrated circuit packages very similar to the *Okabe-AAPA* combination, a POSITA implementing the IC package of *Okabe-AAPA* would have good reason to look to *Taggart* and *Sutardja*. (*Id.*)

A POSITA would have understood that particular spacing between the leads for high speed and low speed would modify the coupling of signals as disclosed by *Sutardja*. Such a person would have a reasonable expectation of success in

implementing spacing as they were well-known and widely-implemented features of signal traces in integrated circuit packages. (*Id.*, ¶164)

F. Ground 6: Claims 8 and 11 are unpatentable as obvious over *Okabe*, in view of *Applicant's Admitted Prior Art* (*AAPA*), *Sutardja*, and *Choi*.

1. Claim 8

a) "An IC package as recited in claim 1, wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with the low speed circuitry, and"

The *Okabe-AAPA* combination teaches this element. (Ex. 1002, ¶166) In the event the Patent Owner argues that *Okabe-AAPA* does not disclose a first set of electrical contacts, Sutardja does. (*Id.*) As discussed above with in Section IX.D.1 regarding claim 2, Sutardja discloses leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (Ex. 1012 ¶139) A POSITA would have understood that "low speed leads" 620-1 through 620-4 would be "a first set of electrical contacts for electrical connection with the low speed circuitry". (Ex. 1002, ¶167)

b) "a second set of electrical contacts for electrical connection with the high speed circuitry"

Sutardja teaches this element. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶168)

c) "wherein the second set of electrical contacts are spaced apart at a distance sufficient to establish a differential impedance of at least 100 ohms between the contacts of the second set"

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling", but does not explicitly state "a differential impedance of 100 Ohms". (Ex. 1012, ¶139) (Ex. 1002, ¶169)

However, *Choi* discloses a PBGA package having high speed differential traces designed to provide a 100 ohm differential impedance. (Ex. 1011, p. 304) A POSITA implementing the IC package of *Okabe-AAPA* would have looked to *Sutardja* and *Choi* as they are all in the same field of IC packages. Such a POSITA would have been motivated to modify the IC package of Okabe-AAPA with the spacing of *Sutardja* to achieve the 100 ohm differential impedance for high speed traces as taught by *Choi*. (Ex. 1002, ¶170)

2. Claim 11

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with the low speed circuitry; and"

The *Okabe-AAPA-Sutardja* combination teaches this element. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶172)

b) "a second set of electrical contacts for electrical connection with the high speed circuitry; and"

Sutardja teaches this element. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶173)

c) "wherein the electrical contacts are arranged as part of I/O lines such that,"

Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B (Ex. 1012, ¶138) and that the leads 620-1 through 620-4 "operate at a speed that is lower than the leads 620-5A and 620-5B and 620-6A and 620-6B". (*Id.*, ¶139) A POSITA would have understood that 620-1 through 620-6B would be equivalent to input/output lines. (Ex. 1002, ¶174)

d) "a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts; and"

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling", but does not explicitly state a differential impedance of 50 ohms (Ex. 1012, ¶139) (Ex. 1002, ¶175).

However, *Choi* discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms). (Ex. 1011, p. 304) A POSITA

implementing the *Okabe-AAPA-Sutardja* IC package with spacing of a first set of electrical contacts would have good reason to *Choi's* low-speed transmission lines having characteristic impedances of 50 Ohms to avoid impedance mismatch, which was known to cause degradation of a signal. (Ex. 1002, ¶176)

e) "a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts"

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling" (Ex. 1012, ¶139). However, *Sutardja* does not explicitly discloses "a differential impedance of at least 100 Ohms between the contacts of the second set of electrical contacts". (Ex. 1002, ¶177)

However, *Choi* discloses a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for 100 Ω (Ohms). (Ex. 1011, p. 304) (Ex. 1002, ¶178) A POSITA would have good reason to modify the IC package of *Okabe-AAPA* with the spacing of *Sutardja* and the characteristic impedance of *Choi*. Such a person would have been motivated to set the spacing and impedance of the electrical contacts "to decrease or increase coupling" as needed. (Ex. 1002, ¶179)

G. Ground 7: Claim 10 is unpatentable as obvious over *Okabe*, in view of *Applicant's Admitted Prior Art* (*AAPA*), *Sutardja*, *Choi*, and *Digital Design*.

1. Claim 10

a) "An IC package as recited in claim 1 wherein the peripheral electrical contacts include "a first set of electrical contacts for electrical connection with the low speed circuitry, and"

Okabe-AAPA-Sutardja teach this element (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶181).

b) "a second set of electrical contacts for electrical connection with the high speed circuitry, and"

Okabe-AAPA-Sutardja teach this element. (*See supra* Section IX.D.1 regarding claim 2) (Ex. 1002, ¶182)

c) "wherein the electrical contacts are arranged as part of I/O lines such that,"

Okabe-AAPA-Sutardja teach this element Sutardja discloses die pads 614-1 through 614-6B connected, via bondwires 616-1 through 616-6B, to leads 620-1 through 620-6B for transmitting and receiving signals. (Ex. 1012, ¶¶4, 138) (Ex. 1002, ¶183)

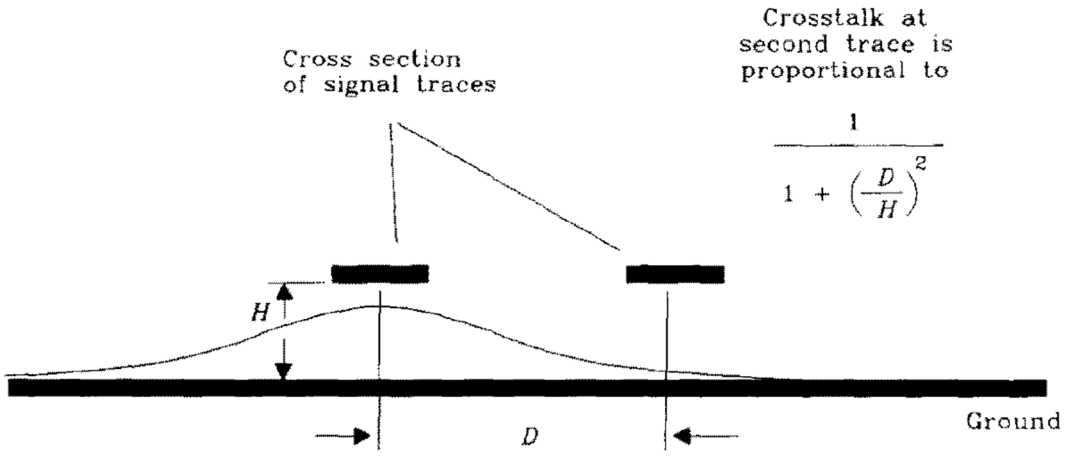
d) "a first spacing between the contacts of the first set of electrical contacts is sufficient to establish a control differential impedance of at least 50Ω between the contacts of the first set of electrical contacts to substantially eliminate cross-talk between I/O lines for the low speed electronic circuitry; and"

Sutardja discloses spacing d1 between the low speed leads (first set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling". (Ex. 1012, ¶139) (Ex. 1002, ¶176)

Choi discloses, a multi-layered PCB that has a low-speed interconnects on layer 1 and that the low-speed signal transmission lines have characteristic impedances designed for 50 Ω (Ohms). (Ex. 1011, p. 304) (Ex. 1002, ¶185)

Digital Design discloses in Figure 5.4, shown below, that the spacing of signal traces affects crosstalk. (Ex. 1010, p. 192) (Ex. 1002, ¶186)

$$\text{Crosstalk} \approx \frac{K}{1+(D/H)^2} \qquad [5.2]$$



(Ex. 1010, FIG. 5.4)

Digital Design further shows in Figure 5.20, shown below, measuring cross talk for lines having a 50 Ohm characteristic impedance.

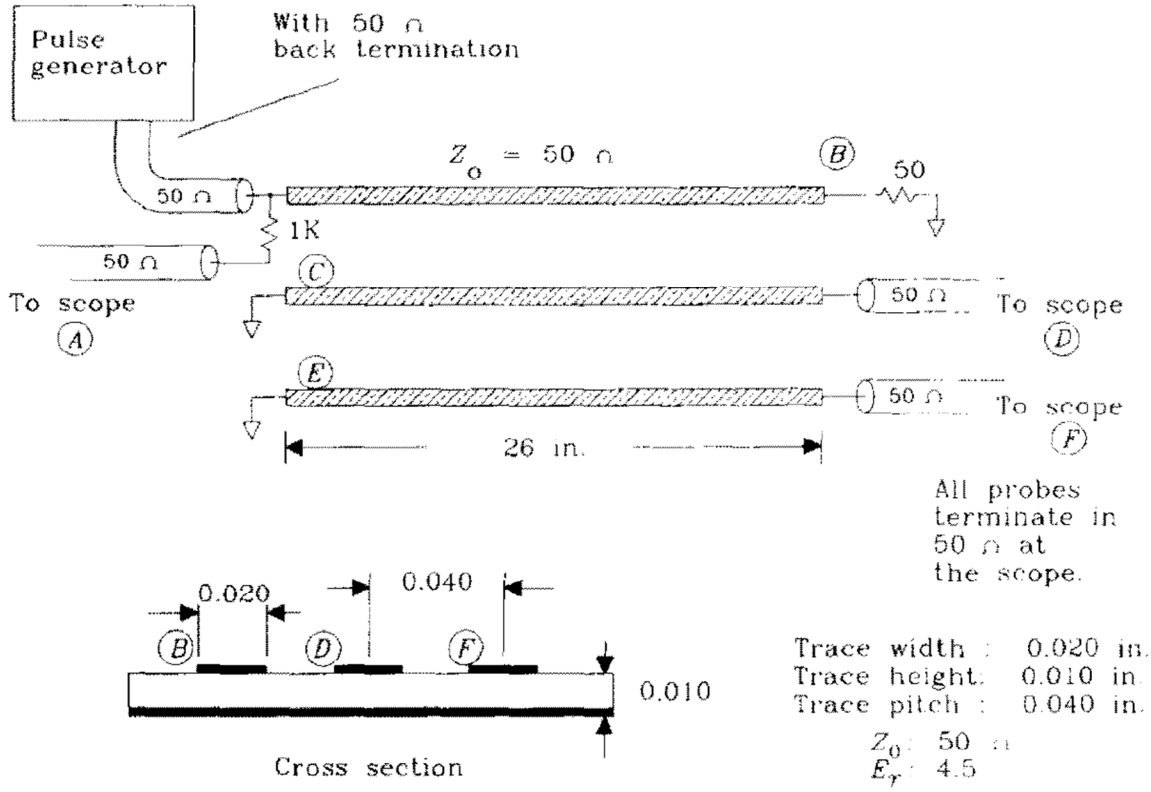


Figure 5.20 Setup for reflected reverse crosstalk measurement.

(*Id.*, FIG. 5.20)

A POSITA implementing the IC package of *Okabe-AAPA* would have good reason to look at *Choi*, *Digital Design*, and *Sutardja* for modifying the spacing of signal lines of *Sutardja* to achieve a 50 Ohm impedance as taught by *Choi* and *Digital Design* as they are all related to IC packages and/or signal characteristics. Such a person would have been motivated to optimize the spacing as it was widely

known in the art that spacing would affect the cross talk as disclosed by *Digital Design*. (Ex. 1002, ¶188)

e) "a second spacing between the contacts of the second set of electrical contacts is sufficient to establish a control differential impedance of at least 100Ω between the contacts of the second set of electrical contacts to substantially eliminate cross-talk between I/O lines for the high speed electronic circuitry."

Sutardja discloses spacing d4 between the high speed leads (second set of electrical contacts), and that the spacing can be changed to "increase or decrease coupling" (Ex. 1012, ¶139) (Ex. 1002, ¶189)

Choi discloses, a multi-layered PCB that has a high-speed interconnects on layer 6 and that the high-speed signal transmission lines have characteristic impedances designed for 100 Ω (Ohms). (Ex. 1011, p. 304)

As discussed above with reference to Section IX.G.1(d) regarding claim 7, *Digital Design* discloses it was well known that spacing of signal traces affects crosstalk. (Ex. 1010, p. 192) As such, a POSITA would have been motivated to implement Choi's 100 Ohm characteristic impedance for high speed transmission lines, and the spacing of *Digital Design* and *Sutardja* to optimize coupling in order to substantially eliminate cross-talk as was widely known in the art. Such a person implementing the IC package of *Okabe-AAPA* would have good reason to look to *Sutardja*, *Choi*, and *Digital Design* as they all relate to IC packaging and/or signal trace spacing optimization. (Ex. 1002, ¶191)

H. Ground 8: Claim 13 is unpatentable as obvious over *Okabe*, in view of *Applicant's Admitted Prior Art* (*AAPA*), *Kramer,* and *Sutardja*.

1. Claim 13

a) "An IC package as recited in claim 12, wherein the die arrangement comprises a die having both the high-speed electronic circuitry and the low-speed electronic circuitry; and"

The *Okabe-AAPA* combination teaches an IC package as discussed above with reference to Section IX.C.2 regarding claim 12. *Kramer* shows in Figure 3 below, an integrated circuit (IC) 30 having a portion of the IC being analog circuitry 31. (Ex. 1007, 2:47-57) (Ex. 1002, ¶193) The analog circuitry transmits high-speed differential signals (speeds over 4.25 Gb/s) via wire bond 46, while wire bond 40 transmits signals from the other portions of the IC 30. (Ex. 1007, 11:14-23)

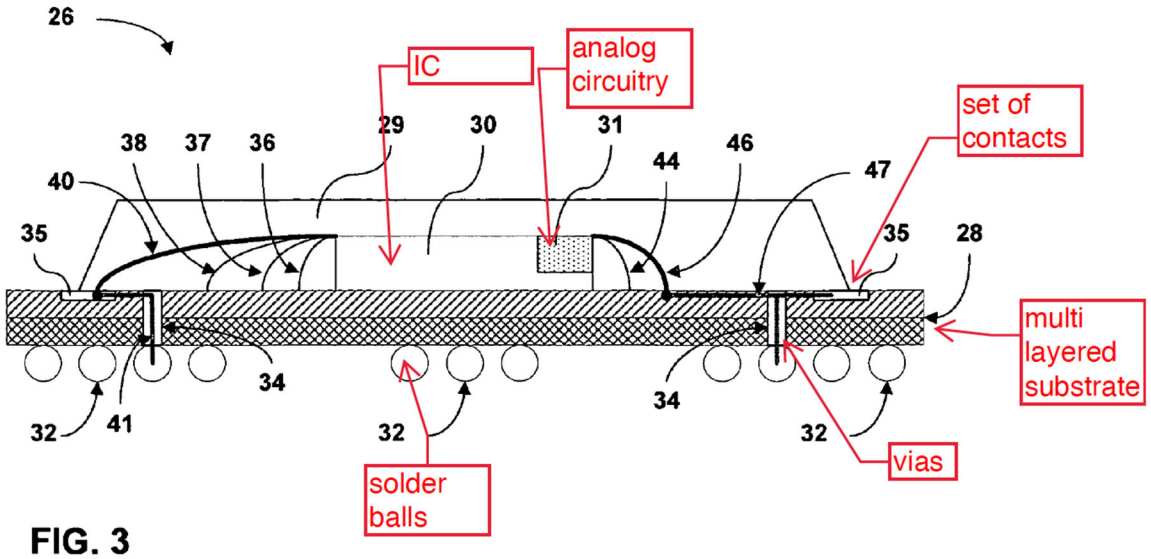


FIG. 3

(*Id.*, FIG. 3 (annotated).)

A POSITA would have understood that analog circuitry operating at speeds of 4.25 Gb/s and above with specific isolated routing of these signals via separate wirebonds, would indicate that the other portions of the IC would not operate at those speeds and thus either the analog or the other portions (whichever has lower speeds), would include "low speed circuitry". (Ex. 1002, ¶194)

b) "wherein the peripheral electrical contacts include, a first set of electrical contacts for electrical connection with low speed circuitry; and a second set of electrical contacts for electrical connection with high speed circuitry; and"

Sutardja discloses peripheral electrical contacts including high speed leads and low speed leads, shown below, where a first set of electrical contacts (620-1 – 620-4) are utilized for electrical connection with low speed circuitry, and a second

set of electrical contacts (620-5A – 620-6B) are utilized for electrical connection with high speed circuitry. (Ex. 1012, ¶0139) (Ex. 1002, ¶195)

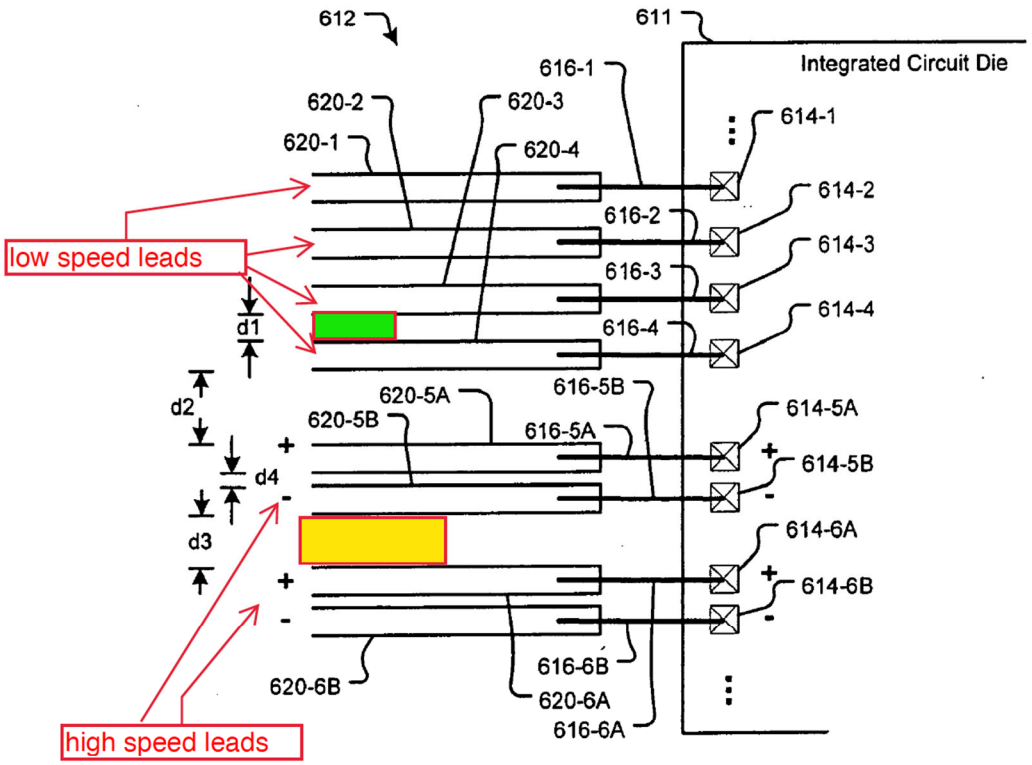


FIG. 10A

(Ex. 1012, FIG. 10A (annotated).)

c) "wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low speed electronic circuitry; and"

Kramer discloses in Figure 6, shown below, that an IC circuit 72 includes an analog circuit 73 that is connected with a first portion of ground plane that is separated from the remaining portion of ground plane 74 outside the analog area.

Kramer also discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). *Kramer* also discloses the non-analog portions of the IC 72 re connected to electrical contacts 77 outside the analog area. "Although not shown in FIG. 6, wire bonds outside of the analog area of the BGA package couple IC 72 to ground ring 74, power stripes 75 and 76, and the set of contacts 77. Analog circuit 73 of IC 72 requires isolated power and ground connections to avoid introducing noise from other circuits". (Ex. 1007, 8:60-66) (Ex. 1002, ¶196)

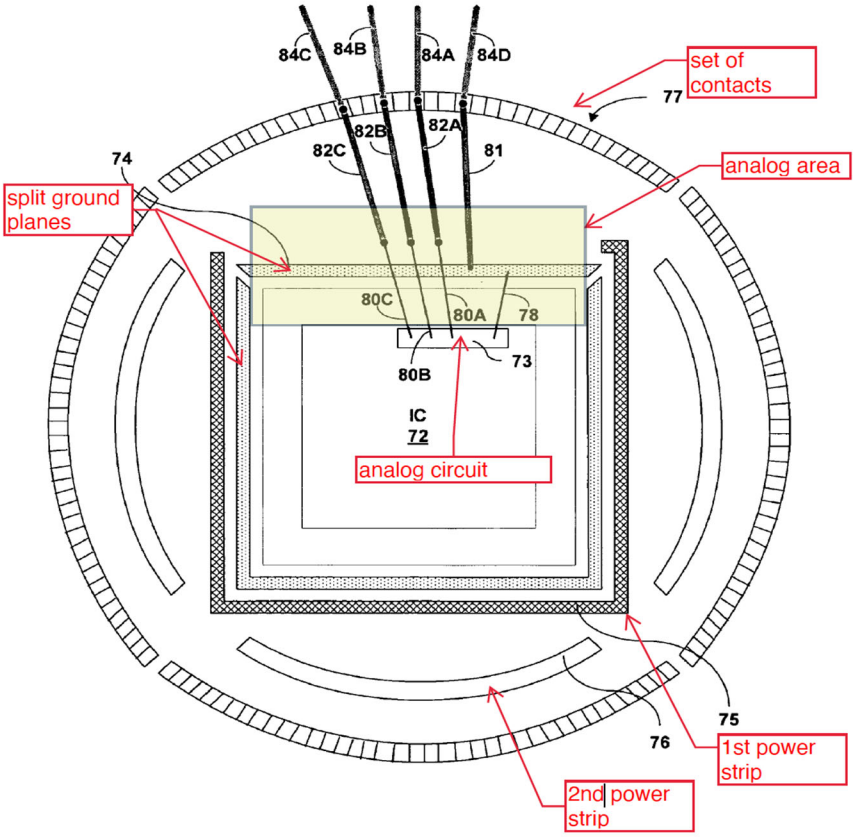


FIG. 6

(Ex. 1007, FIG. 6 (annotated).)

A POSITA would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuity, and that the IC 72 being connected to the portion of the ground plane 74 outside the analog area would be a first ground plane. (Ex. 1002, ¶197) *Kramer* does not explicitly disclose the contacts 77 are "spaced for connection with low speed electronic circuitry". (*Id.*)

However, *Sutardja* clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. *Sutardja* further discloses that spacing between the leads may be changed to "increase or decrease coupling. (Ex. 1012, ¶139) (Ex. 1002, ¶198)

As such, a POSITA would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts. (Ex. 1002, ¶199)

d) "wherein the high-speed electronic circuitry is connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry."

Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. (Ex. 1007, FIG. 6)

Kramer discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). (*Id.*, 1:35-42) However, *Kramer* does not explicitly disclose "the second set of electrical contacts that are spaced for connection with the high speed circuitry". (Ex. 1002, ¶200)

However, *Sutardja* shows in Figure 10A, shown above, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). *Sutardja* further discloses spacing may be irregular to "increase or decrease coupling". (Ex. 1012, ¶0139) (Ex. 1002, ¶201)

As such, a POSITA implementing the IC package of *Okabe-AAPA* would have good reason to look to *Kramer* and *Sutardja* as they are all in the field of IC packaging. Moreover, a POSITA would have understood that a particular spacing for *Kramer's* high speed contacts would affect a particular impedance and minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by *Sutardja*. (Ex. 1002, ¶202)

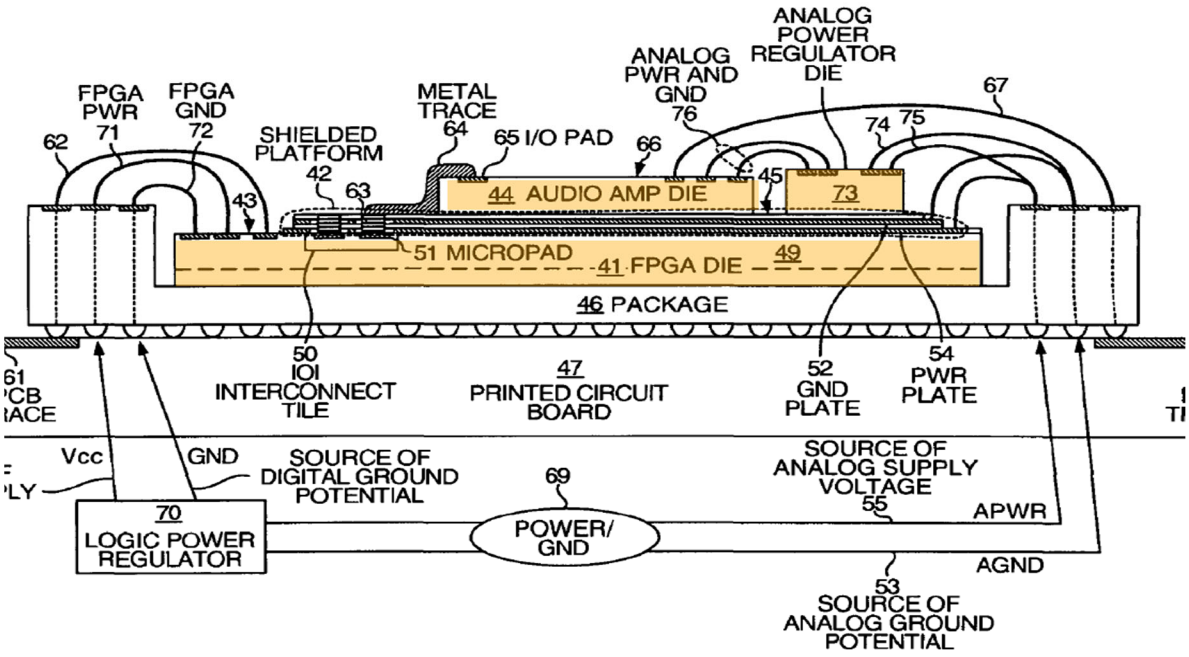
I. Ground 9: Claim 14 is unpatentable as obvious over *Okabe,* in view of *Applicant's Admitted Prior Art* (*AAPA*), *Conn*, *Kramer,* and *Sutardja*.

1. Claim 14

a) "An IC package as recited in claim 12, wherein the die arrangement comprises a stacked die arrangement"

As discussed in Section IX.C.2(a) above, *Okabe-AAPA* discloses an IC package with an IC die. However, *Okabe-AAPA* does not explicitly disclose "a stacked die arrangement". (Ex. 1002, ¶204)

However, *Conn* illustrates a stacked die arrangement in Figure 2 shown below. For example, analog power regulator die 73 is stacked on FPGA die 49. (Ex. 1013, 1:35-54) (Ex. 1002, ¶205)



(Ex. 1013, FIG. 2 (annotated).)

b) "wherein at least one die has the high-speed electronic circuitry and wherein at least one die has the low-speed electronic circuitry;"

Conn discloses in an example that the analog power regulator die 73 operates at a lower frequency than the underlying FPGA die 49 (*Id.*, 6:30-50) As such, a POSITA would have understood that a die being capable of operating at a higher frequency than the other would indicate one die having high-speed electronic circuitry and the other die having low speed electronic circuitry. (Ex. 1002, ¶206)

c) "wherein the low-speed electronic circuitry is connected with the first ground plane and is electrically connected with the first set of electrical contacts that are spaced for connection with the low-speed connection with the low speed electronic circuitry; and"

Kramer discloses in Figure 6, shown below, an IC 72 is connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. *Kramer* further discloses the analog circuitry operates at higher speeds (e.g., 4.25 Gb/s and above). (Ex. 1007, 1:35-42) *Kramer* also discloses the IC 72 is connected to electrical contacts 77 outside the analog area. (Ex. 1002, ¶207)

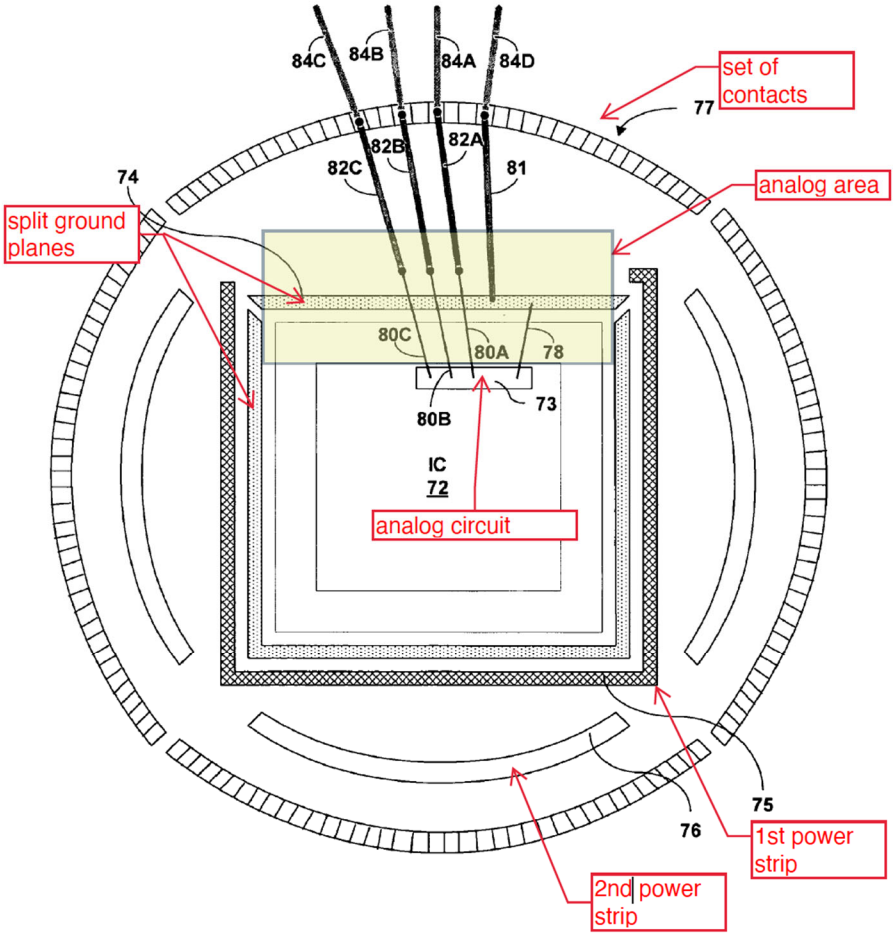


FIG. 6

(Ex. 1007, FIG. 6 (annotated).)

A POSITA would have understood the IC operating at lower speeds than the analog circuit 73 would be low speed circuity, and that the IC 72 being connected to the portion of the ground plane 74 outside the analog area would be a first ground plane. *Kramer* does not explicitly disclose the contacts 77 are "spaced for connection with low speed electronic circuitry". (Ex. 1002, ¶207)

However, *Sutardja* clearly shows in Figure 10A that low speed leads are spaced closer together than high speed leads. *Sutardja* further discloses that spacing between the leads may be changed to "increase or decrease coupling. (Ex. 1012, ¶139)

As such, a POSITA would have understood spacing of lines and contacts affects coupling, and would have been motivated to space such low speed leads in order to minimize cross-talk and/or maintain impedance accuracy of the contacts. (Ex. 1002, ¶210)

d) "wherein the high-speed electronic circuitry is electronic connected with the second ground plane and is electrically connected with the second set of electrical contacts that are spaced for connection with the high speed electronic circuitry."

Kramer discloses in Figure 6, shown above, analog circuitry 73 connected with a first portion of ground plane 74 that is separated from the remaining ground plane 74 outside the analog area. *Kramer* discloses the analog circuitry 73 operates at higher speeds (e.g., 4.25 Gb/s and above). However, *Kramer* does not explicitly disclose "the second set of electrical contacts that are spaced for connection with the high speed circuitry". (Ex. 1002, ¶211)

However, *Sutardja* shows in Figure 10A, shown below, that the spacing for the high speed leads (second set of electrical contacts) is greater than spacing for low speed leads (first set of electrical contacts). *Sutardja* further discloses spacing

may be irregular to "increase or decrease coupling". (Ex. 1012, ¶139) (Ex. 1002, ¶212)

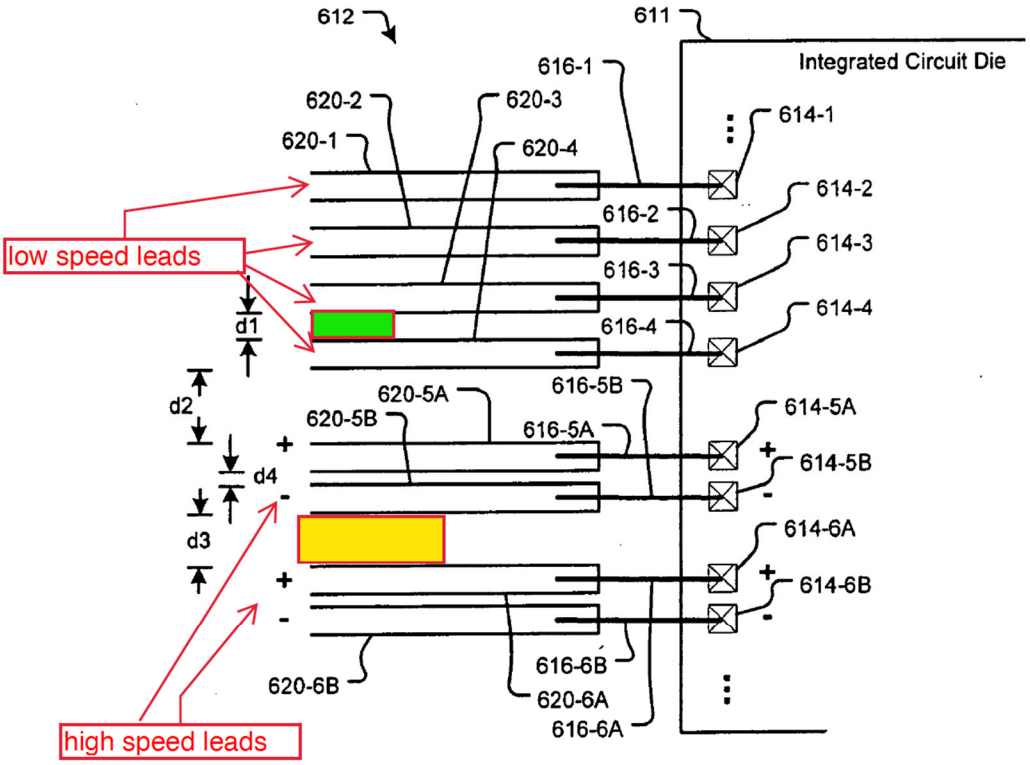


FIG. 10A

(Ex. 1012, Fig. 10A (annotated).)

As such, a POSITA implementing the IC package of *Okabe-AAPA* would have good reason to look to *Conn*, *Kramer* and *Sutardja* as they are all in the field of IC packaging. Moreover, a POSITA would have understood that a particular spacing for *Kramer's* high speed contacts would affect a particular impedance and minimize cross talk, and thus it would have been straightforward to modify spacing of the high speed contacts as taught by *Sutardja*. (Ex. 1002, ¶213)

A POSITA implementing the IC package of *Okabe-AAPA*, would have good reason to look at *Conn*, *Sutardja*, and *Kramer* as they all are in the similar fields of IC packaging, having multi-layered substrates and/or spacing of signal lines. (Ex. 1002, ¶214)

Such an implementation would have simply been the application of a known device (IC package with multiple IC dies) to a similar device (stacked IC dies) and would have produce predictable results. Therefore, in my opinion, the Ok*abe-AAPA-Conn-Sutardja-Kramer* combination discloses or suggests this claim limitation. (Ex. 1002, ¶215)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. The Board Should Not Deny Institution Under § 325(d)

The Board should not deny institution under §325(d) because the art asserted herein was not before the Examiner and is not cumulative of art that was considered. (*See generally* Ex. 1004, Ex. 1001, References Cited) As set forth below, the Examiner either (1) was not presented with the same or substantially the same art or arguments as Petitioner's, or (2) materially erred in allowing the challenged claims. (*Advanced Bionics, LLC v. Med-El Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (citing *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017)).

Becton, Dickinson Factors (a), (b), and (d). Neither "the same [nor] substantially the same" art or arguments were previously presented to the Office during prosecution of the challenged claims. *Okabe*, *Hashemi*, *Kramer*, *Taggart*, *Digital Design*, *Choi*, *Sutardja*, *Conn*, *High-Speed DSP*, *Kester*, and *Schroeder* were never cited during prosecution of the '091 patent, let alone considered by the Examiner or made the subject of a rejection. (*See generally* Ex. 1004) These references are also not substantially the same or cumulative of references considered during examination. During Examination, the pending claims were rejected under sections 102 and 103 over combinations of U.S. Patent Pub. No. 2004/0238939 ("Wu") and U.S. Pub. No. 2005/0173807 ("Zhu"). The Patent Owner argued that the cited references failed to disclose "two separate and electrically isolated ground planes" (Ex. 1004, p. 349) As explained above, at least *Okabe*, *Hashemi*, *Kester*, *Kramer*, and *Schroeder* disclose such isolated ground planes. (*See supra* Section VII.B.1, Section VII.B.2, Section VII.B.3, Section VII.B.4, and Section VII.B.11)

The Patent Owner further argued that the cited art fails to disclose that "the spacing arrangements between the high speed and low speed contacts are different". (Ex. 1004, p. 350) As explained above, at least *High-Speed DSP*, *Digital Design* and *Sutardja* disclose such spacing arrangements. (*See supra* Section VII.B.6, Section VII.B.7, and Section VII.B.9)

Becton, Dickinson Factors (c), (e), and (f). As explained above, the answer to the first inquiry of Advanced Bionics—whether the same or substantially the same art or arguments were previously presented to the Office—is a definitive "no." Accordingly, analysis of Examiner error is unnecessary. Nevertheless, to the extent the Board disagrees and determines *Becton, Dickinson* factors (a), (b), and (d) do not favor institution, discretionary denial still is not warranted because the Examiner must have necessarily overlooked anticipatory disclosures of the art that was examined, constituting material error. Advanced Bionics, IPR2019-01469, Paper 6, 10 (listing silence as evidence of error). As stated above in detail, *Okabe*, *Okabe-AAPA*, and *Hashemi-Okabe* teaches every element of at least claim 1. To the extent any reference that was Examined could be considered cumulative of *Okabe* and *Hashemi*, the Examiner should have rejected the challenged claims under section 102, or at least under section 103, and maintained the rejection(s). Under these circumstances, Petitioner respectfully submit that denial of institution under § 325(d) would not be appropriate.

B. Institution is Proper Under Section 314(a) and *Fintiv*

The merits of Petitioner's arguments are compelling and the evidence in support is substantial. This "alone demonstrates that the PTAB should not

discretionarily deny institution under *Fintiv*." (Ex. 1020 at 4-5[3]) Nevertheless, the six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because NXP has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** weighs against denial. Jury Trial is set for August 20, 2024 (Ex. 1017). However, on June 23, 2023, the co-pending Central District of California lawsuit was reassigned to the Honorable Hernan D. Vera, which more than likely will result in delay of the Jury trial (Ex. 1017). Therefore, it is likely that the trial will occur after the FWD in this IPR, which is expected prior to the end of November 2024. And even if the trial proceeds in August 2024, which it likely will not, the above timing does not tip in favor of denying the petition in this case. *See also, e.g., Apple Inc. v. Aire Tech. Ltd.*, IPR2022-01135, Paper 11 at 5-6 (PTAB Jan. 4, 2023).

The **third factor** weighs strongly against denial. Defendant served its initial infringement contentions on May 17, 2023. Petitioner's diligence in pursuing this petition less than 6 months after receiving the infringement contentions weighs in

[3] Citations are to page numbers of Memorandum from Director Vidal (dated June 21, 2022) that are on the bottom of each page.

favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions).

The **fourth factor** weighs against denial because this Petition challenges claims 1-14 of the '091 patent. Only claims 1, 5, 6, 8, and 10-13 of the '091 Patent are asserted against Petitioner in district court. (Ex. 1019) This IPR petition is thus the only venue in which invalidity challenges of claims 2, 3, 4, 7, 9 and 14 will be adjudicated, which promotes system efficiency. See *Fintiv*, Paper 11 at 4. Accordingly, this factor weighs strongly against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and Patent Owner are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial. None of the above references were considered by the Examiner. There is also a significant public interest against "leaving bad patents enforceable," and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

XI. CONCLUSION

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1-14 of the ’091 patent.

Respectfully Submitted,

Dated: November 9, 2023 By: /Timothy D. Taylor/

Timothy D. Taylor (Reg. No. 76,643)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,646,091 contains, as measured by the word processing system used to prepare this paper, 13,312 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully Submitted,

Dated: November 9, 2023 By: /Timothy D. Taylor/

Timothy D. Taylor (Reg. No. 76,643)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on November 9, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,646,091 and supporting exhibits filed November 9, 2023, to be served via Priority Mail Express on the Patent Owner at the following correspondence addresses of record:

Mendelsohn Dunleavy, P.C.
1500 John F. Kennedy Blvd., Ste. 910
Philadelphia, PA 19102

Bell Semiconductor, LLC
401 N. Michigan Ave., Suite 1630
Chicago, IL 60611

Respectfully Submitted,

Dated: November 9, 2023 By: /Timothy D. Taylor/

Timothy D. Taylor (Reg. No. 76,643)
Counsel for Petitioner