

# Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation

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**Abstract**—The voltage-time domain (VT) characteristics of the CMOS NOR logic circuit are investigated using a switch matrix technique (SMT). VT performance is analyzed following gate oxide wearout in a pMOSFET, induced by applying a constant voltage stress (CVS) at  $-4.0$  V. Results for the NOR VT characteristics show approximately 30% increase in rise time ( $t_r$ ), a considerable digression from nominal operation.

## I. INTRODUCTION

THE effects of gate dielectric breakdown (BD) on digital circuit operation is becoming progressively more important as gate oxide thicknesses ( $t_{ox}$ ) are scaled below 2.0 nm [1], due in part to increased gate leakage current. Therefore, better understanding of BD and its effect on circuit function may lead to more accurate reliability projections [2]. Through simulation performed on digital circuits, such as NAND and NOR gates, it has been reported that BD leads to considerable timing delays [1], [3]. However, the physical characteristics pertaining to the effects of oxide degradation in both the devices and circuits have received less attention.

A recent study by Ogas *et al.* examined the effects of single degraded pMOSFET devices on the voltage-time response (VT) of the NAND logic circuit [4]. Using a SMT developed by several of the co-authors [5]-[6], they were able to conclude that a substantial increase in rise time ( $t_r$ ) was attributed to an increase in channel resistance of the degraded pMOSFET [4].

In this preliminary study, the same wearout degradation regime and circuit reliability technique reported by Ogas *et al.* [4] is targeted to examine the VT response of the NOR logic circuit.

## II. EXPERIMENTAL

The MOSFET devices used in this study are fabricated using a 0.1  $\mu\text{m}$  CMOS process with a  $t_{ox}$  of 2.0 nm. The device width is 10  $\mu\text{m}$  and the length is 0.1  $\mu\text{m}$ . Measurements are obtained using an integrated semiconductor characterization system described elsewhere [6]. SMT involves wafer level measurements using two probe stations, each with eight micropositioners necessary to connect the NOR circuit (Fig. 1). This technique permits the measurement of NOR circuit performance, as well as, the isolation of four

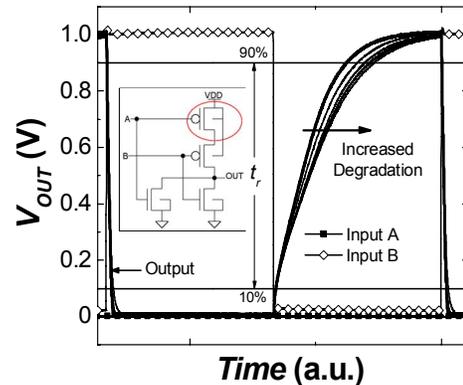


Fig. 1. NOR Voltage-Time measurement with Input A held at ground and Input B swept from 0V to 1V (configuration 2). Inset: NOR circuit with degraded pMOSFET circled.

separate MOSFET devices to obtain individual MOSFET characteristics [6].

Gate oxide wearout in one pMOSFET of the NOR gate is induced by applying constant voltage stress (CVS) at  $-4.0$  V in periods of 600 seconds (Fig. 2). This approach has been used in similar studies involving pMOSFET devices [7]. The remaining three MOSFETs in the NOR circuit are not stressed. Wearout is the cumulative effects of oxide degradation over five CVS periods, as defined by Ogas *et al.* [4]. After each stress period, NOR circuit VT and device characteristics were measured which include gate leakage current ( $I_G$ - $V_G$ ) and maximum drain current ( $I_{DRIVE,MAX}$ ).

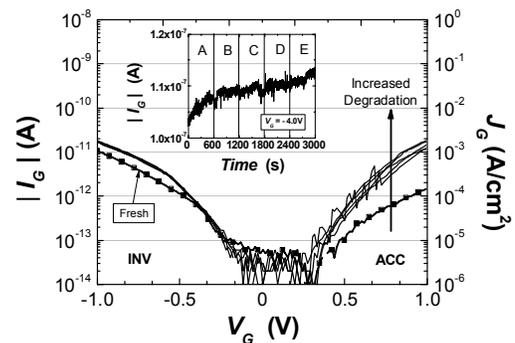


Fig. 2. Pre- and post-CVS  $I_G$ - $V_G$  data showing the effects of wearout in a pMOSFET. Inset:  $I_G$  vs. time, in intervals of 600s, during CVS.

TABLE I  
NOR GATE INPUT CONFIGURATIONS INDICATING I/O STATE

Configuration	Input/Output			
	1	2	3	4
Input A	VDD	GND	Pulse	Pulse
Input B	Pulse	Pulse	VDD	GND
Output	0	0,1	0	0,1

Grey = positions affected by wearout. 0,1 = output transition

Table I illustrates the NOR gate response examined for the pMOSFET position highlighted in Fig. 1. It is observed that the circuit response is affected by only configurations 2 and 4. For this preliminary study, only configuration 2 is presented. The data for configuration 4 is currently being analyzed. However, initial measurements suggest configuration 4 yields similar results to configuration 2.

### III. RESULTS AND DISCUSSION

**NOR Circuit:** The VT characteristics for the NOR circuit in configuration 2 are shown in Fig. 1. It was observed that  $t_r$  of the circuit increases by  $27\% \pm 5\%$  for configuration 2. Rise time is defined as the time it takes for the output signal to increase from 10% to 90% of the final voltage, as indicated in Fig. 1 [8]. It should be noted that previous studies on inverter and NAND logic circuits have indicated that changes in  $t_r$  are indicative of pMOSFET degradation, while changes in fall time ( $t_f$ ) are associated with the nMOSFET [4]-[6]. Moreover, Carter *et al.* suggests that an increased  $t_r$  could potentially cause logic errors in a high speed digital circuit when introduced into a large scale design.

**MOSFETs:** The increased  $t_r$  of the NOR circuit response warrants investigation of the characteristics of the degraded pMOSFET. The CVS graph coupled with the gate leakage (Fig. 2) suggests the pMOSFET has not endured a traditional dielectric breakdown (i.e. hard breakdown) [9]. Moreover, as indicated by Ogas *et al.*, the pMOSFET device appears to be operating in the wearout regime [4]. Further analysis of the data indicates a dramatic change in the performance of the pMOSFET device attributed to dielectric wearout (Fig. 3), despite the minimal change in gate leakage current (Fig. 2). Additionally, the  $I_{DRIVE,MAX}$  is decreased by  $41.0 \pm 5.4\%$ , (Fig. 3).

Similar pMOSFET degradation was observed by Ogas *et al.* in [4]. They found the degradation produced an increase of  $t_r$

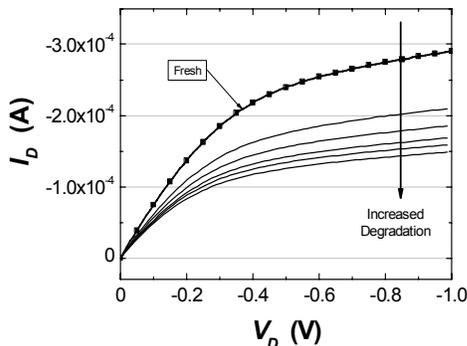


Fig. 3. Drain current vs. drain voltage characteristics of degraded pMOSFET from Fresh to Test E.

in NAND gates. The  $t_r$  increase was correlated to an increase in channel resistance by relating the degradation in pMOSFET parameters to channel resistance. The results of Ogas *et al.* suggests the increase in  $t_r$  of the NOR circuit as observed in this study correlates to an increase in channel resistance of the degraded pMOSFET. Particularly interesting is the observation that  $t_r$  degradation from the NOR VT characteristics is approximately half that of the  $t_r$  degradation as compared to NAND circuit operation [4]. The difference in VT response may be due to the stacking nature of the pMOSFET devices in the NOR circuit compared to the pMOSFET configuration in the NAND circuit, justifying further examination [10].

### IV. CONCLUSION

The preliminary results reported for wearout in one pMOSFET of a NOR gate circuit indicate a substantial increase in  $t_r$  attributed to an increase in channel resistance. This preliminary study suggests that the NOR circuit configuration is less sensitive to single pMOSFET wearout than the NAND circuit, potentially due to the stacking effect in digital circuits. Future goals include investigation of the stacking effect in digital circuits relative to the wearout regime, as well as examination of correlations between increased  $t_r$  and variations in threshold voltage.

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