Indirect Compensation Technique for Low-Voltage CMOS Op-amps

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***Abstract*—Two and three-stage indirect-compensated op-amps employing split-length composite devices are presented. By incorporating split-length devices the right-half plane zero which hampers op-amp performance can be eliminated. Chip test results indicate significant enhancements in op-amp speed while reducing power consumption and layout area. Moreover, these techniques can be used to compensate three-stage op-amps operating at low supply voltage (V_{DD}).**

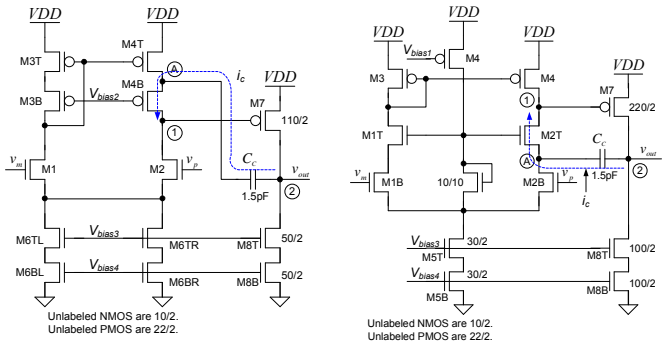
I. Introduction

Two-stage op-amps have been the amplifier topologies of choice in analog system design due to their simple frequency compensation and relaxed stability criterions. The two-stage op-amps have traditionally been compensated using the Miller (or Direct) compensation technique [1][2]. Miller compensation achieves dominant pole compensation by pole splitting due to capacitance multiplication effect. However, the compensation capacitance (C_c) connected between the outputs of the first and second gain stages, leads to a right-half plane (RHP) zero. The RHP zero, located at $z_1=g_{m2}/C_C$ in the s-plane, pulls down the phase margin of the op-amp and requires a larger capacitance to compensate the op-amp. This in turn results in a reduced unity gain frequency of the op-amp given by $f_{un}=g_{m1}/2\pi C_c$ [1].

The RHP zero can be eliminated by blocking the feed-forward compensation current, while allowing the feedback component of the compensation current to attain pole splitting. This can be achieved by several methods including a zero nulling resistor (R_Z) or a voltage buffer in series with the compensation capacitor in the feedback path [1][4]. A common-gate stage can also be employed to block the feed-forward component of the compensation current while achieving pole-splitting [3]. Such techniques where the compensation current is indirectly fed-back are categorized as indirect compensation. This paper presents a brief description of indirect feedback compensation and presents the use of split-length devices for op-amp compensation while operating at low-V_{DD}.

II. Indirect Feedback Compensation Of Op-Amps

The class of amplifier compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is defined as *Indirect Feedback Frequency Compensation* or simply, indirect compensation [1], [5]. Here, the compensation capacitor is connected to an internal low impedance node in the first stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node i.e. the output of the first stage. The dominant pole location for the indirect compensated op-amp is same as in Miller compensation. However, instead of a RHP zero we now have a LHP zero located at $z_1=g_{mc}/(C_C+C_A)$, where g_{mc} is the transconductance of the common-gate device and C_A is the capacitance attached to the low-impedance node A. The non-dominant pole location is given by $p_2=-g_{m2}C_C/(C_1C_L)$. Also there exists a third parasitic pole arising due to the loading of the low impedance node-A [4].



(a) Cascoded current mirror load

(b) Cascoded Diff-pair

Figure 1. Indirect compensated two-stage op-amps using cascode common gate device. The compensation capacitor, C_c, in each of the op-amps is connected to the the low impedance node A [1][4].

We can discern that when using indirect compensation, the second pole, p_2, is pushed further away from the dominant pole, p_1, by a factor of approximately C_C/C_1. Hence, pole splitting can be achieved with a lower value of the compensation capacitor C_C and/or with a lower value of g_{m2}.

This results in a significantly higher unity-gain frequency attainable by the op-amp. Also the LHP zero adds to the phase in the vicinity of the unity gain frequency, f_{un}, and improves the phase margin [1][2]. Figure 1 shows two-stage op-amp topologies where indirect compensation is achieved by using the "embedded' common-gate device in the cascode structure [4].

III. Indirect Compensation using Split-Length Composite Transistors

Indirect-compensated two-stage op-amps can be designed by employing the internal low impedance nodes available in a cascode topology to feedback the compensation current [1]. However, with continual scaling of supply voltage (V_{DD}) cascoding may no longer be an option in the sub-100nm CMOS processes [6]. A suitable technique for low V_{DD} design which employs a split-length composite transistor for indirect compensation, proposed in [1]&[5], is analyzed in this section.

Figure 2 illustrates splitting of an NMOS or a PMOS to create a low impedance node-A. For a composite NMOS, the lower device, M1B, operates either in cut-off or triode region but never in saturation. Since a triode device offers a low channel resistance and also that node-A is connected to the source of M1T, the node-A is a low impedance node. Similar argument holds for the PMOS composite device [1].

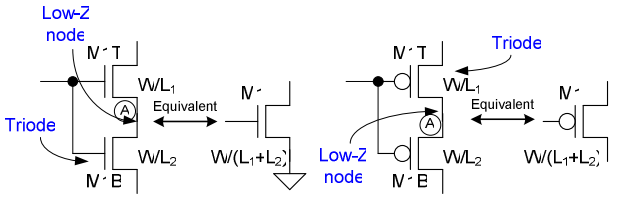


Figure 2. Illustration of the split-length composite NMOS and PMOS devices [1].

A. *Split length current mirror load (SLCL)*

Figure 3 exhibits a two-stage op-amp with a split-length current mirror load (SLCL) topology. The compensation capacitor is connected to the internal low impedance node-A to achieve indirect compensation.

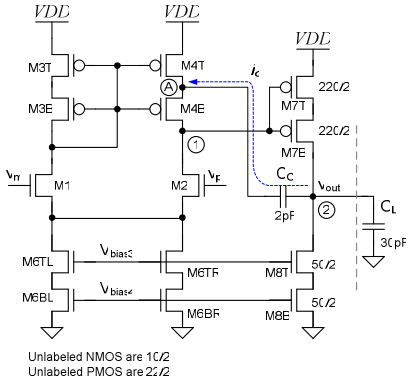


Figure 3. A two-stage op-amp with indirect feedback compensation using split-length load composite devices [1][5].

In order to simplify the small signal analysis of this op-amp topology, few assumptions have been made. The transconductance of each of the split PMOS devices is denoted as g_{mp}. The resistance, R_A, can be approximated to be equal to the channel resistance of the trioded PMOS, which is close to $1/g_{mp}$. Also, here if the current mirror load is designed with the same g_m as the diff-pair, we have $g_{mp} = \sqrt{2}\,g_{m1}$. The simplified small-signal model for SLCL op-amp is shown in figure 4 [7].

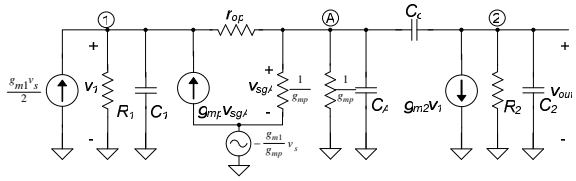


Figure 4. Small signal model for analysis of the two-stage op-amp employing split length load devices [7].

On applying nodal analysis on the small signal model shown in figure 4, we obtain a dc gain of $-g_{m1}R_1 g_{m2}R_2$ and a unity gain frequency equal to

$$f_{un} = \frac{g_{m1}}{2\pi(2C_C)} \tag{1}$$

The dominant pole is given as

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_C} \tag{2}$$

The LHP zero is located at

$$z_1 \approx -\frac{4g_{mp}}{3(C_C+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C+C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un} \tag{3}$$

The non-dominant poles are approximated by

$$p_2 \approx -\frac{g_{m2}C_C}{2C_1C_L} \tag{4}$$

$$p_3 \approx -\left[2g_{mp}/C_2 \| C_C + 1/\left(R_1 \| r_{op}\right)C_1\right] \tag{5}$$

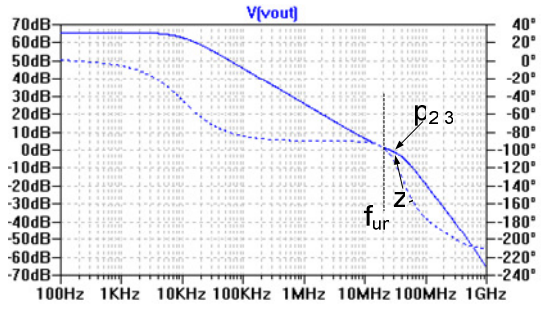


Figure 5. Simulated frequency response of the indirect compensated opamp with split-length current mirror load (SLCL). Here f_{un}=20MHz and PM=80°.

SPICE simulated frequency response for this op-amp is shown in figure 5. This op-amp exhibits a unity gain frequency of 20MHz, a phase margin of 75° and a transient settling of 60ns.

B. *Split length differential pair (SLDP)*

Figure 6 shows the proposed two-stage op-amp topology where a split-length diff-pair (SLDP) is used for indirect compensation. This topology exhibits better power supply rejection ratio (PSRR) since the node used for compensation (node A) is isolated from the supply rails and lesser supply noise is leaked to the output.

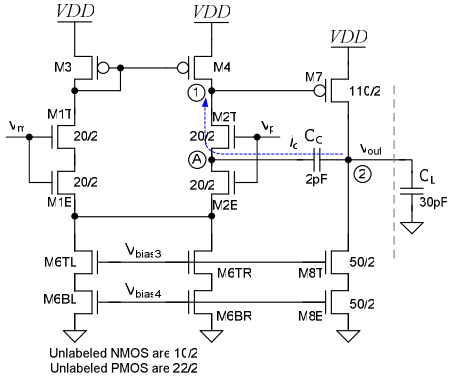


Figure 6. An indirect compensated two-stage op-amp employing split-length diff-pair.

Small signal analysis of this topology again yields the same non-dominant poles and zero locations as in the split-length current mirror load case. However, the unity gain frequency is now estimated by

$$f_{un} = \frac{2g_{m1}}{2\pi C_C} \tag{6}$$

Thus the LHP zero can now be expressed as

$$z_1 \approx -\frac{4g_{mn}}{3(C_C + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C + C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un} \tag{7}$$

which implies that the LHP zero is located at a lower frequency than the unity gain frequency. This has the effect of flattening the gain magnitude response which may degrade the phase margin of the op-amp. The SPICE simulated frequency response for this op-amp is shown in figure 7. This op-amp exhibits a unity gain frequency of 35MHz, a phase margin of 62° and a transient settling of 75ns [7].

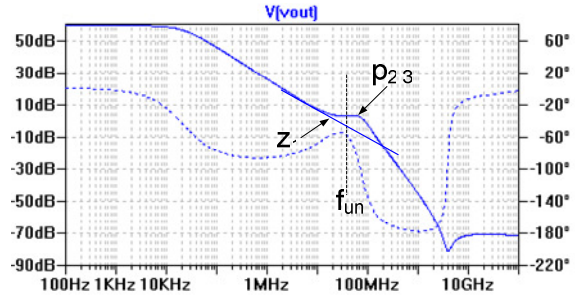


Figure 7. Simulated frequency response of the indirect compensated opamp with split-length diff-pair (SLDP). Here f_{un}=35MHz and PM=60°.

In the case of SLCL indirect compensation, we have the flexibility of varying g_{mp} independent of g_{m1} in order to control the location of the LHP zero and hence the phase margin of the op-amp. However, in the case of SLDP we do not have such convenience and it might be hard to obtain desirable phase margins with the SLDP topology. But the SLDP indirect compensation topology is of great utility when designing multi-stage indirect compensated op-amps described in [6].

IV. INDIRECT COMPENSATION OF THREE STAGE OP-AMPS

The SLCL and SLDP indirect compensation techniques shown in the last section form the basis for low-voltage op-amp compensation. However, one may argue that the op-amp gain is sacrificed by avoiding cascoding. But, since cascoding may no longer be viable due to supply voltage (V_{DD}) scaling and relatively fixed threshold voltages (V_{TH}). Thus the paradigm of cascoding needs to be traded with cascading of low-voltage stages to design high-gain op-amps in nano-CMOS. Also since the intrinsic gain of the transistors ($g_m r_o$) has been dropping with continued scaling, use of at least three stages is inevitable for op-amp design in nano-CMOS.

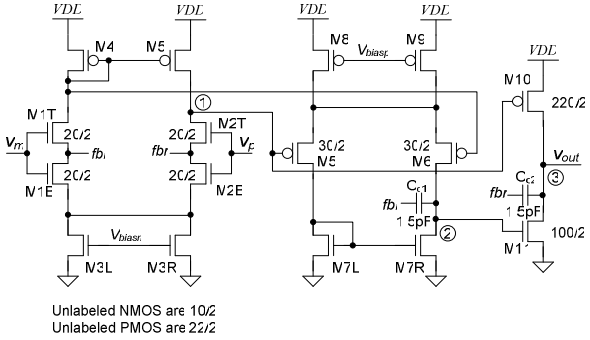


Figure 8. A low-V_{DD} class-AB three-stage op-amp employing reversed nested indirect compensation (RNIC).

Figure 8 presents a three-stage op-amp operating at a supply voltage of 2.5V, designed by cascading three low-V_{DD} gain stages. A PMOS diff-amp is used in the second stage to precisely set the bias level for the third common-source stage and also for providing higher CMRR. The third stage is biased in a class-AB fashion such that the gates of M10 and M11 move together and one of the devices is shut-off while driving the load. Note the way in which the compensation currents are indirectly fed-back to node-1 from nodes 2 and 3.

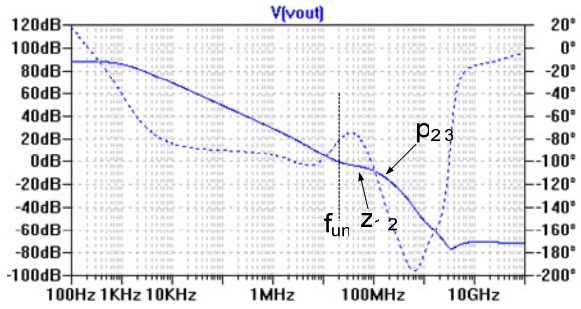


Figure 9. Simulated frequency response of the indirect compensated three-stage opamp (RNIC). Here f_{un}=20MHz and PM=76°.

This compensation scheme leads to two LHP zeros besides a dominant pole and two non-dominant poles. The two LHP zeros counter the two non-dominant poles and help improve the phase margin. The low impedance internal nodes fbl and fbr also lead to two parasitic poles at higher frequencies, which are close to the f_T limited poles (or mirror poles) and can be ignored. Detailed analysis for this three-stage topology is provided in [6]. Thus incorporation of indirect-compensation in three-stage op-amps leads to lower power, simple and manufacturable topologies as shown in figure 8.

V. CHIP TEST RESULTS AND PERFORMANCE COMPARISON

The test chip, designed using AMI's C5N (0.5µm) process, includes Miller compensated op-amps with and without the zero nulling resistor and the SLCL, SLDP & RNIC indirect compensated op-amp topologies (see figure 10).

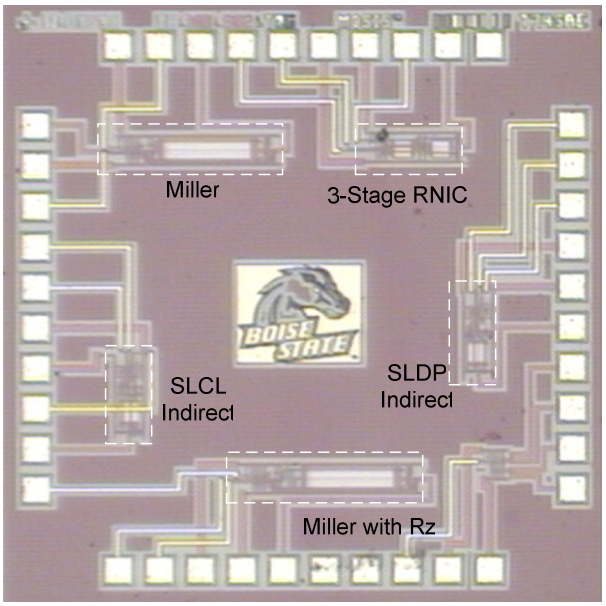


Figure 10. Microphotograph of the test chip showing the fabricated two and three stage op-amps.

A performance comparison of the op-amp topologies fabricated on the test chip is presented in Table 1. The chip test results exhibit that the indirect-compensated two-stage op-amps exhibit nearly ten times improvement in the gain bandwidth (f_{un}) and four times faster transient settling when compared to the Miller compensated op-amps. Also the indirect compensation results in 40% reduction in power and 50% reduction in the layout area of the two-stage op-amps.

Further, the proposed three-stage topology leads to around 26 dB higher gain with almost the same unity-gain frequency (as SLCL op-amp) by consuming only 20% more power while operating at 50% of the supply voltage and occupying the same layout area as the corresponding two-stage op-amps.

TABLE I. PERFORMANCE COMPARISON OF THE OPAMPS FOR CL=30PF.

Op-amp Topology	A_{DC} (dB)	f_{un} (MHz)	C_C (pF)	PM	t_s (ns)	Power (mW)	Layout area (mm^2)
Miller	57	2.5	10	74°	270	1.2	0.031
Miller with R_Z	57	2.7	10	85°	250	1.2	0.034
SLCL (this work)	66	20	2	80°	60	0.7	0.015
SLDP (this work)	60	35	2	60°	75	0.7	0.015
RNIC (this work)	89	20	1.5, 1.5	76°	60	1.4	0.017

VI. CONCLUSION

Indirect feedback compensation technique applied to two-stage and three-stage op-amps using split-length transistors has been presented. The chip test results demonstrate that the indirect feedback compensation employing split-length devices leads significantly faster, lower power op-amps with smaller layout footprint when compared to the traditional Miller compensation. These indirect compensated topologies are suitable for op-amp design in nano-CMOS processes.

ACKNOWLEDGMENT

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