CMOS Image Sensor using Delta-Sigma Modulation

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Abstract – A CMOS image sensor ADC using delta-sigma modulation is presented and discussed. Experimental results from a test chip are presented. The experimental results show that the proposed ADC has several benefits over the use of pipeline ADCs including noise reduction, fast design times, ease with which to maximize ADC output based on a varying input range, and simple symmetric analog routing for large arrays. A clock frequency of 100 MHz, and a 20 mus row sense time results in resolutions of 10-bits. A 2000 column imager using the proposed topology can output data continuously every 10 ns after an initial one row latency.

I. INTRODUCTION

CMOS image sensors typically use a pipeline ADC to convert an analog voltage, produced by the Active Pixel Sensor (APS), into a digital value. In commercial imaging chips, multiple columns share a single pipeline ADC. This could be in the form of an ADC per color, multiple colors, or a subset of a color for large arrays. The advantage of a pipeline ADC is that offsets are common to all columns sharing the ADC. Routing differences between the analog signals of columns to the shared ADC are a big concern. The use of a pipeline ADC requires large capacitors to minimize the effects of thermal noise. Since they are precision circuits, the design times will be long.

In this paper, an ADC per column using delta-sigma modulation (DSM) is proposed. The proposed ADC offers advantages over pipeline ADCs including increased SNR, fast design time, fast frame rates, easy APS signal amplification to maximize dynamic range, and the elimination of issues with routing analog signals for large arrays. These circuits will also compete with pipeline ADCs in terms of layout space and power consumption. The drawback of the design is that using an ADC per column can result in additional column fixed pattern noise (FPN). This paper identifies and addresses these drawbacks, which are also the topic of future work.

II. IMAGE SENSOR ADC USING DSM

Illustrated in Fig. 1 is the sensing scheme for the image sensor. The image capture begins with the reset voltage sampling onto one of the hold capacitors, C_H, through the SHR switch. After a fixed integration time, the other hold capacitor samples the image signal voltage through the SHI switch. Sampling of these two voltages, referred to as correlated double sampling, removes variation from offsets in the APS [1] producing a differential voltage to apply as the input to the DSM ADC. At this point, the differential voltage is applied onto a high impedance gate making the hold capacitance variation a lot less critical than in the pipeline ADC topology.

There is one DSM sensing circuit per column. The DSM produces a modulated output based on the differential input signal from reset and signal voltages held on hold capacitors C_H. (The size of these capacitors set the thermal noise floor in this topology.) The modulated output is sent to a counter that is used as a low pass filter produces a digital code [2].

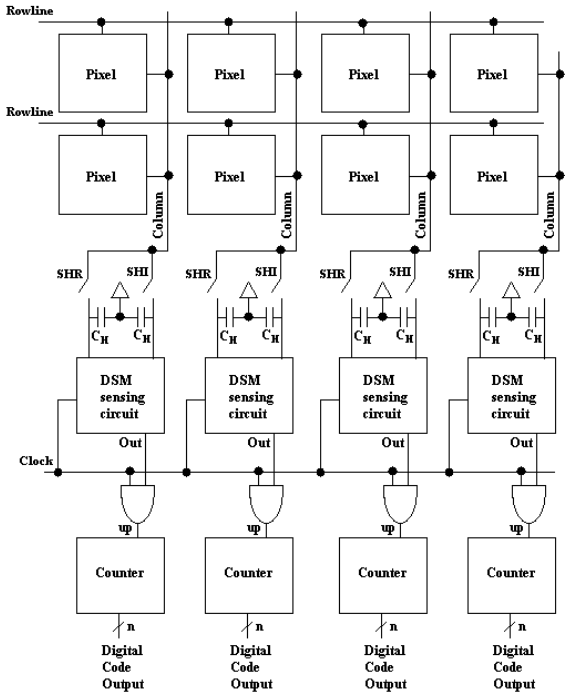

Fig 1. A 2x4 pixel diagram of DSM sensing in an imager.

The DSM sensing circuit, illustrated in Fig. 2, is clocked N times to produce a digital code related to the analog input signal V_{SIGNAL} with respect to the V_{RESET} signal. The phi1 and phi2 signals are out of phase nonoverlapping clocks with a frequency at half the rate of the master clock denoted as f_{phi}.

In order to minimize the effects of device mismatch in the reset and signal paths the sense is broken up into two parts switching the signal and reset paths midway through the sense. For the first half of the sensing period (N/2 clock cycles), the SL_TRU and SL_BAR will be set to V_{DD} and V_{SS}, respectively. During this period, the magnitude of the $I_{BUCKI,t=1}$ and $I_{BUCK,t=1}$ currents are

$$I_{BUCKI,t=1} = C_2 f_{phi}\left(V_{RESET} - V_{TH,M6}\right) \quad (1)$$

$$I_{BUCK,t=1} = C_1 f_{phi}\left(V_{SIGNAL} - V_{TH,M5}\right) \quad (2)$$

During the first half of the sensing period, the positive

terminal of the comparator connects to the V_{BUCKI} terminal, and the negative terminal of the comparator connects to the V_{BUCK} terminal. If the voltage on the V_{BUCKI} terminal is lower than the V_{BUCK} terminal, the comparator turns off transistor M_{14}. However, if the voltage on the V_{BUCKI} terminal is higher than the V_{BUCK} terminal, the comparator turns on transistor M_{14} and a current, I_{DIFF}, flows. The comparator senses N/2 times and turns on the M_{14} transistor $M_{t=1}$ times during this first half of the sensing period. The average magnitude of the $I_{DIFF,t=1}$ current during this first half of the sensing period is

$$I_{DIFF,t=1} = \frac{M_{t=1}}{N} 2C_3 f_{phi}\left(V_{REF} - V_{TH,M13}\right) \qquad (3)$$

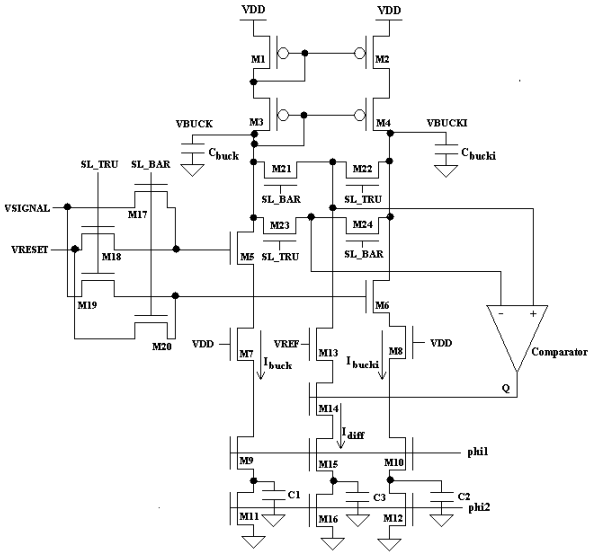

Fig. 2. The DSM used for an ADC in a CMOS imager [3].

The sum of $I_{DIFF,t=1}$ and $I_{BUCKI,t=1}$ along with the current flow in or out of capacitor C_{BUCKI} is a current mirror of I_{BUCK} set by transistors, M_1 and M_3. The sum of current into the C_{BUCKI} capacitor over N/2 clock cycles, ideally, is zero. With this said, the digital relationship of the analog input signals during the first half of the sensing period is

$$M_{t=1} = \frac{C_2(V_{RESET} - V_{TH,M6}) - C_1(V_{SIGNAL} - V_{TH,M5})}{\frac{2}{N}C_3(V_{REF} - V_{TH,M13})} \qquad (4)$$

For the second half of the sense (also over N/2 clock cycles), the SL_TRU and SL_BAR signals are set to V_{SS} and V_{DD}, respectively. Using the same approach to calculate M in the first half of the sense when applied to the second half results in the following

$$M_{t=2} = \frac{C_1(V_{RESET} - V_{TH,M5}) - C_2(V_{SIGNAL} - V_{TH,M6})}{\frac{2}{N}C_3(V_{REF} - V_{TH,M13})} \qquad (5)$$

If the digital code values $M_{t=1}$ and $M_{t=2}$ are added together at the end of the sensing period, the true digital code representation of the analog input signals, V_{SIGNAL} and V_{RESET} over N clock cycles, is

$$M_{t=1} + M_{t=2} = N\frac{(C_1+C_2)}{2\times C_3}\frac{(V_{RESET} - V_{SIGNAL})}{(V_{REF} - V_{TH,M13})} \qquad (6)$$

From Eq. 6, the digital code representation is free from any threshold voltage mismatch from transistor M_5 and M_6 that might cause fixed pattern noise [3]. However, FPN can result from column to column threshold differences in the difference path threshold of M_{13} [4]. A methodology to reduce or eliminate the threshold voltage dependency is the subject of ongoing work. Another benefit of this DSM sensing circuit is that the gain of the transfer function adjusts by altering the V_{REF} voltage. This is very beneficial when a user would like to capture an image in a low-light environment.

The least significant bit voltage, V_{LSB} for this DSM sensing scheme can be approximated using

$$V_{LSB} = \frac{2\times C_3}{(C_1+C_2)}\frac{(V_{REF} - V_{TH,M13})}{N} \qquad (7)$$

The bit accuracy of the DSM sensing circuit increases with the number of clock cycles, N. Using a clock multiplier is a simple way to increase accuracy.

III. THERMAL NOISE

The main advantage of using this ADC is its robustness to noise. As the sense time increases, the averaging filters out random noise. The input-referred thermal noise, set by the capacitors, has an RMS value for this ADC related to the square root of kT/NC and not the square root of kT/C. This gives the ADC superior SNR performance and allows the use of smaller capacitors in the ADC design. The signal and reset capacitors C_H still have an RMS value related to kT/C since they get sampled only one time onto the input of the ADC.

IV. TEST CHIP RESULTS

A test chip design consisting of multiple DSM ADCs used to obtain experimental results is shown in Fig. 3 [4].

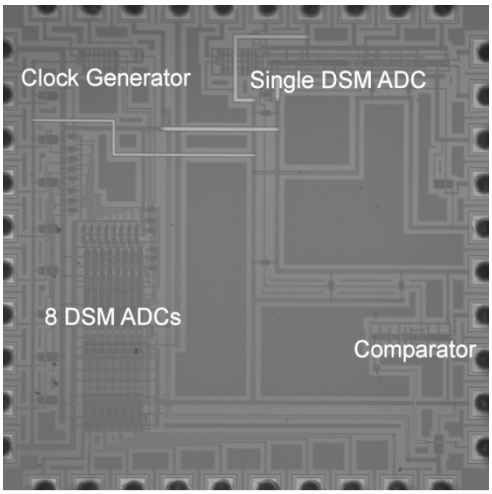

Fig. 3. Image of test chip fabricated through MOSIS.

Test chip data compared to the calculated values from Eq. 1, in Fig. 4, show that the test results match closely with theory.

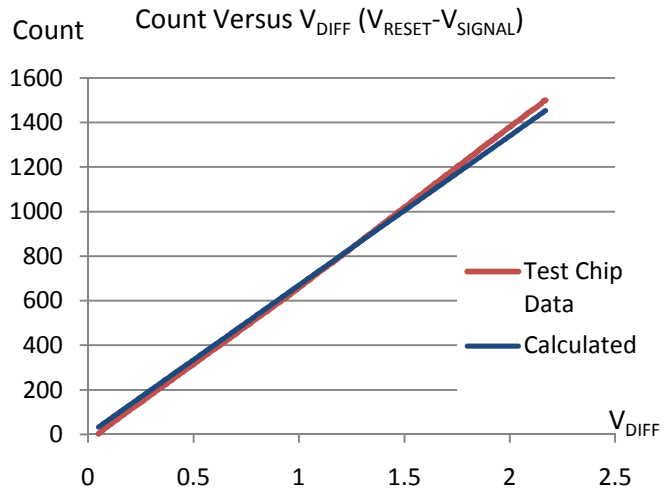

Fig. 4. Comparison of calculated results versus test chip data.

At an increment of 10 mV, the average step size is seven counts. In order to get an idea of the differential nonlinearity on the test chip, the count for every 10 mV increment is compared to the average count per 10 mV increment. Results are shown in Fig. 5. The minimum step size of the input voltage supply used was 10 mV. This limited the data collection to an approximate step size of seven counts.

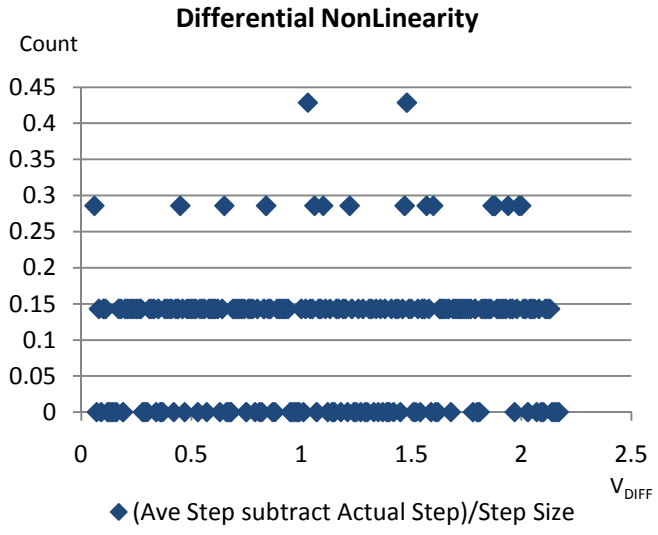

Fig. 5. DNL of the test chip based on the lowest step size being 7 counts.

The integral nonlinearity for the test chip, although not as critical as DNL, has a variation around 1.6 counts on the test chip, as shown in Fig. 6.

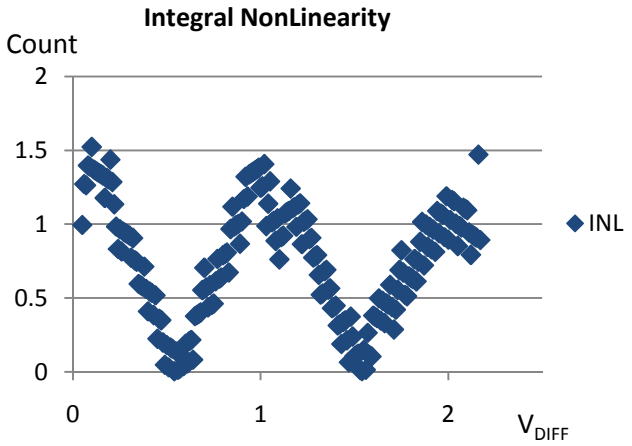

Fig. 6. Integral nonlinearity. The actual count at each point compared to a best fit line through the data points.

The output range of the APS of a CMOS imager is dependent on the intensity of light, integration time, and conversion gain of the pixel. Ideally, the output of the pixel should match the input range required to utilize the full range of the ADC for the scene of interest. Adjusting the integration time based on the scene can achieve this. However, lengthy integration times will result in additional noise and allow the image to move during capture (slower frame rate). In order to optimize integration time tradeoff, sensor designs will include an amplification stage to adjust the range of input to the imager ADCs. For the ADC using delta-sigma modulation, maximizing the output range for a particular input requires only varying the V_{REF} voltage. V_{REF} control by color, illustrated in Fig. 7, is necessary for functions such as white balancing.

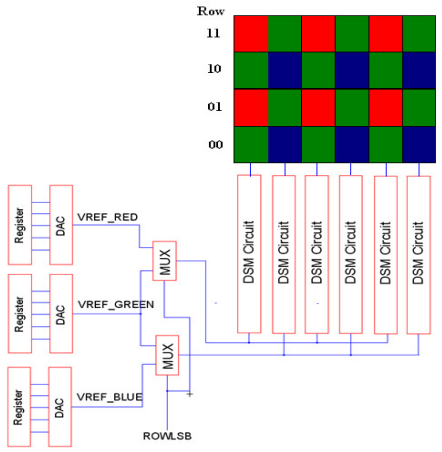

Fig. 7. Diagram showing the implementation of V_{REF} control to maximize the dynamic range.

Results from the test chip, shown in Fig. 8, illustrate the output count versus input voltage change with varying V_{REF}. Maximizing the dynamic range based on an input, which varies with the image, consists of a simple register and DAC taking up a very small amount of silicon.

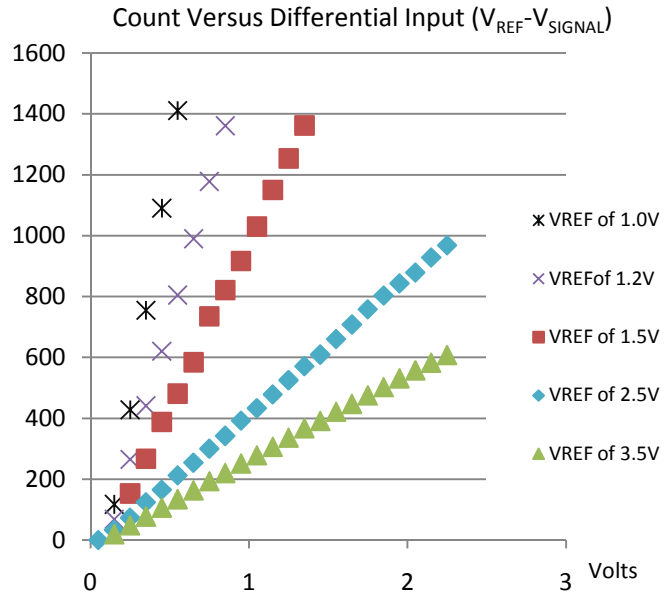

Fig. 8. Count versus input voltage for different V_{REF} values.

Data taken from six different ADCs on the test chip, shown in Fig. 9, illustrate the variation between ADCs due to device mismatch. (Minimum size devices were used which is ideal to show a larger mismatch.) The data was taken with SL_TRU at V_{DD} and SL_BAR at V_{SS} throughout the sense time preventing V_T cancellation due to path switching.

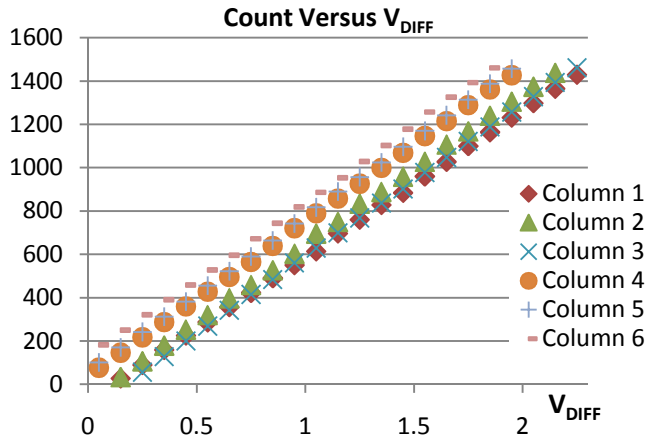

Fig. 9. Data from six ADCs taken without path switching.

Data taken from the same six ADCs, switching paths midway through the sense, illustrates device mismatch cancellation. The columns line up very well, as shown in Fig. 10, with the exception of column 1. The variation in column 1 is most likely the result of a V_T variation in M_{13} of the difference path.

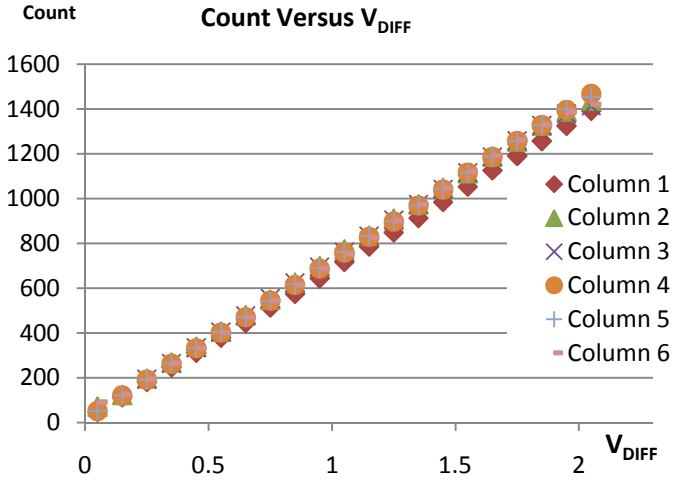

Fig. 10. Data from the same six ADCs, as in Fig. 9, taken with path switching enabled.

V. Summary and Conclusions

This research looked at a CMOS imager ADC design using delta-sigma modulation, which would be very robust in a production design. Data from a test chip illustrated the linearity of the design. The major benefits were explored and FPN issues from using an ADC per column were closely examined. With increasing array size and speed requirements, these types of designs are likely to become a standard in imager design.

Special Thanks

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