

Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process

Paper Authors:

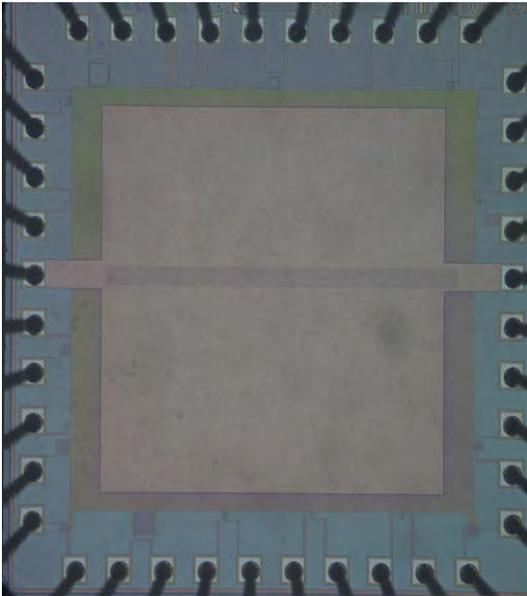
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Benefits From using Standard Process

- Low cost solution
 - No extra specialized steps
 - Reduced Size, Weight, and Power



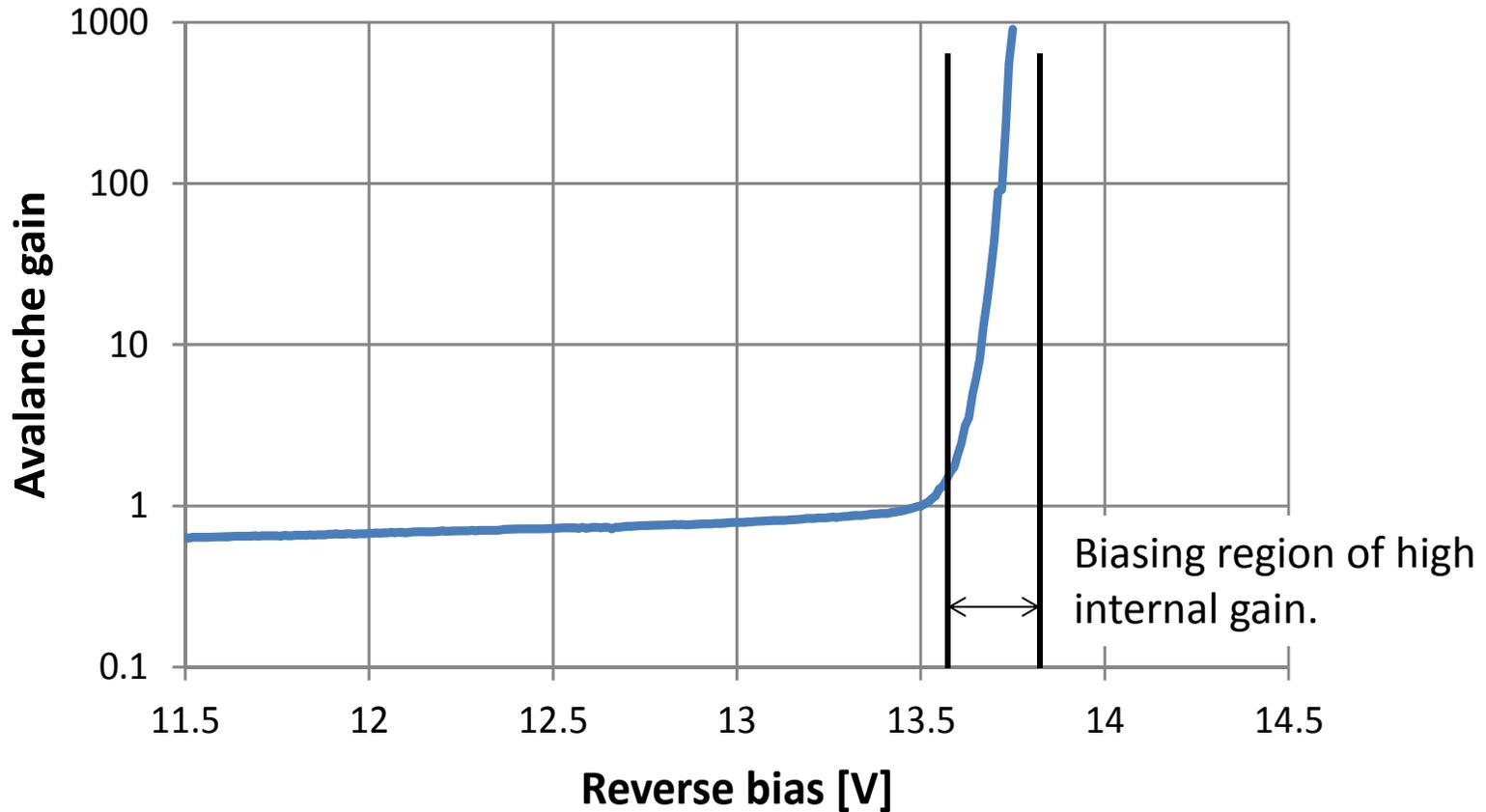
ROIC circuits can be built on same die as APD using a standard CMOS process

APD Benefits

- APD's are very sensitive due to high internal gain
- Fast Response Times

Photodetector Comparison (Typical values)	Gain	Response Time(s)
Avalanche Photodiode	10^2-10^4	10^{-10}
p-n junction	1	10^{-11}
p-i-n junction	1	$10^{-8}-10^{-10}$
Metal Semiconductor Diode	1	10^{-11}
Bipolar phototransistor	10^2	10^{-8}
Field Effect phototransistor	10^2	10^{-7}

APD PhotoDetectors

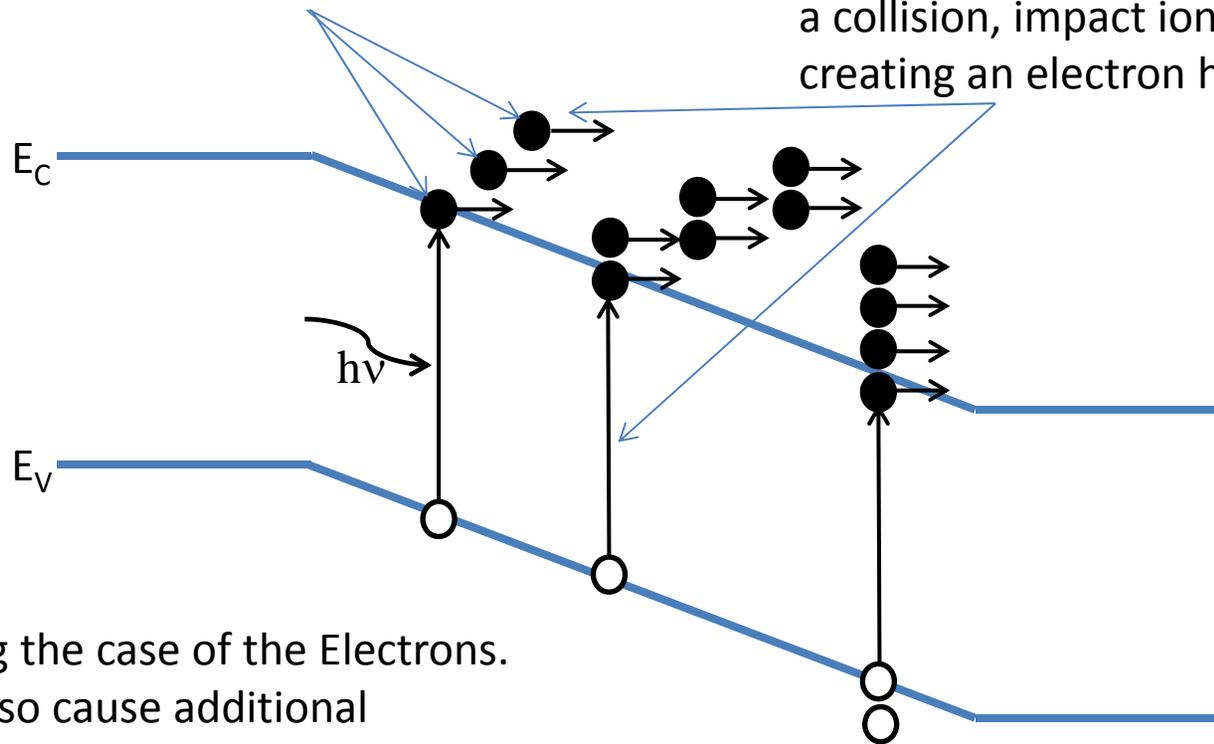


Impact ionization occurs at high reverse-bias conditions because a large Electric Field is required.

Avalanche Multiplication

Electron Gains K.E. because of E-Field

If electron gains enough K.E. before a collision, impact ionization occurs creating an electron hole pair.



Showing the case of the Electrons.
Holes also cause additional
electron/hole pairs.

MULTIPLICATION RESULTS IN A HIGH INTERNAL GAIN!

Application Examples

LADAR – Light Detection and Ranging

- ❑ Automotive
 - Blind Spot Detection
 - Collision Avoidance Systems
 - Etc.
- ❑ Military
 - Range Finders
- ❑ Traffic Safety
 - Traffic Lights
 - i.e. Delay Green Light for cars based on no stop on red

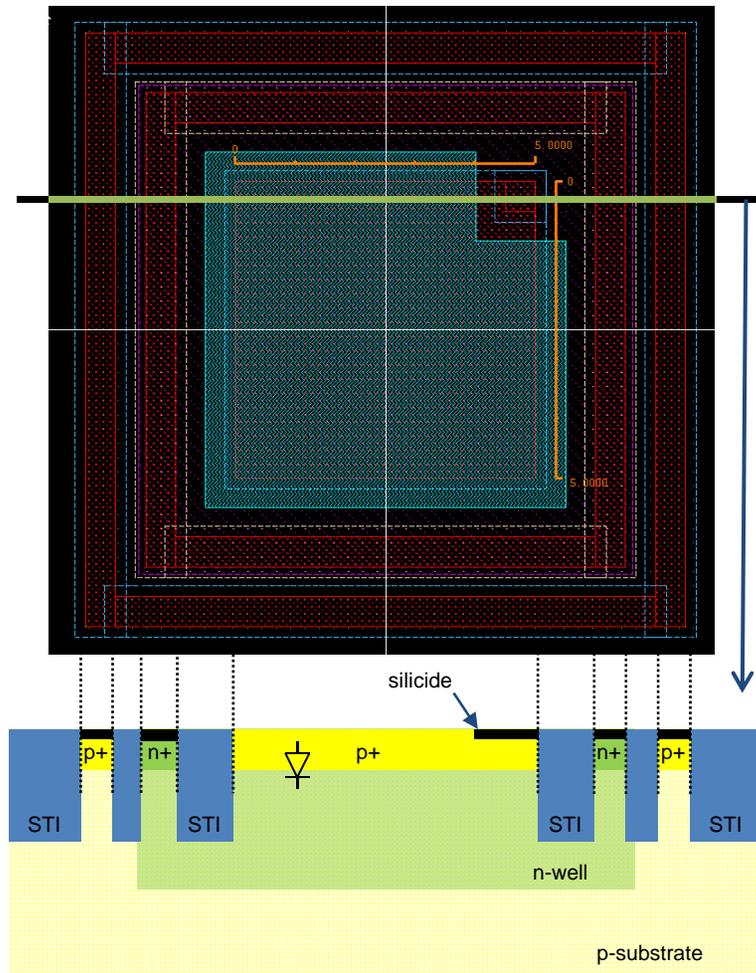
Communications

- ❑ Optical Fiber Communications

Test Chip Objectives

- Fabricate APD's in a standard CMOS Process
- Investigate Layout Considerations
 - Avoid bending E-Fields.
 - Look at various active area sizes.
 - Reduced Guard Ring Layout.
 - Maximum Fill Factor versus Substrate Leakage.
- APD Electrical Measurements
 - Dark and Light Anode, Cathode, and Substrate currents.
 - Light measurement is broadband microscope illuminator. Detailed spectral response is left for future work.
 - APD Gain.

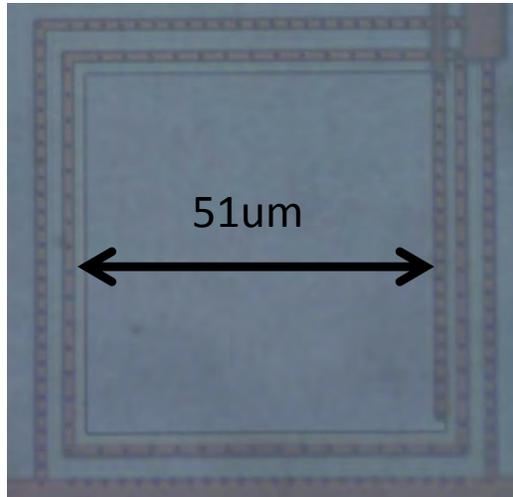
Layout Considerations



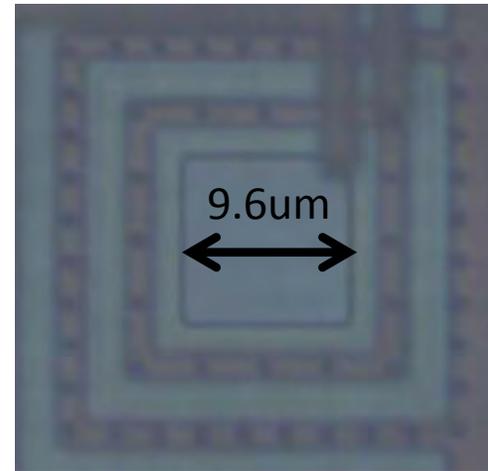
- ❑ Avalanche PhotoDetector (APD) is formed with p+ and the n-well
- ❑ Active area is p+ in the n-well
- ❑ Impact ionization (depletion) region is normal to the surface of the wafer, avoid “bending E fields”
 - ❑ STI is used to ensure a planar p+ to n-well transition (Guard against Junction Curvature Effect)
 - ❑ Important for reliable performance
- ❑ Various Active Area Sizes
- ❑ Reduced Guard Ring Layouts
 - ❑ Larger Fill Factor
 - ❑ Increase in Substrate Current?

Various Active Area Sizes

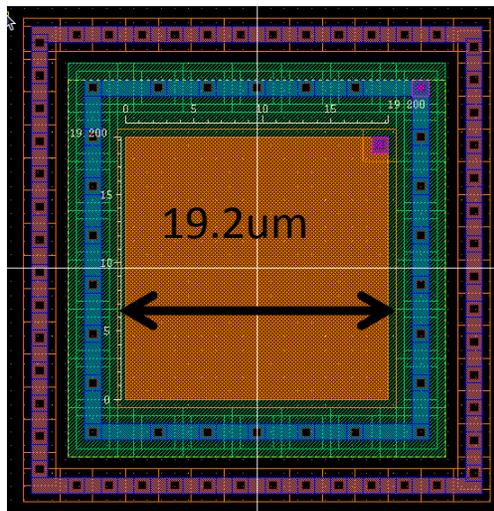
51um²



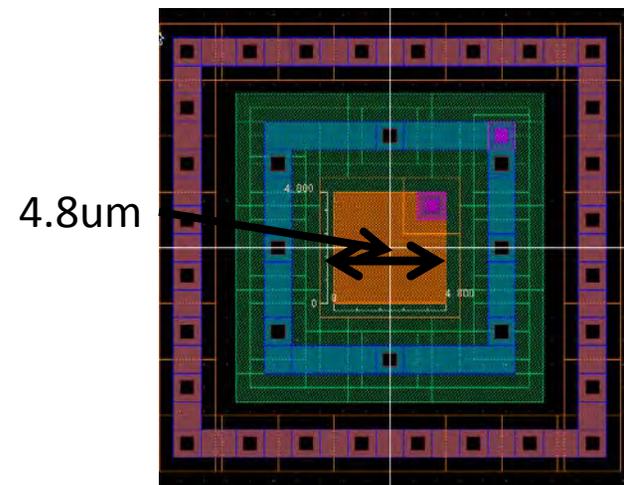
9.6um²



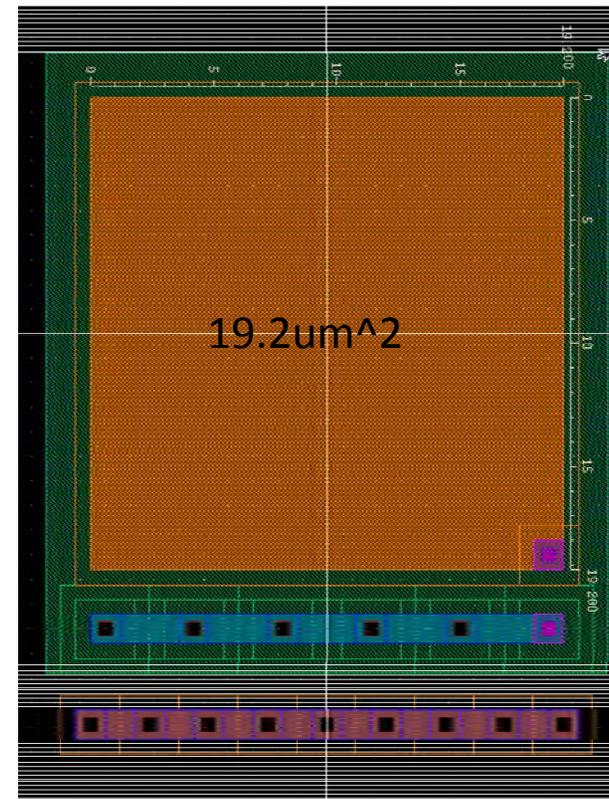
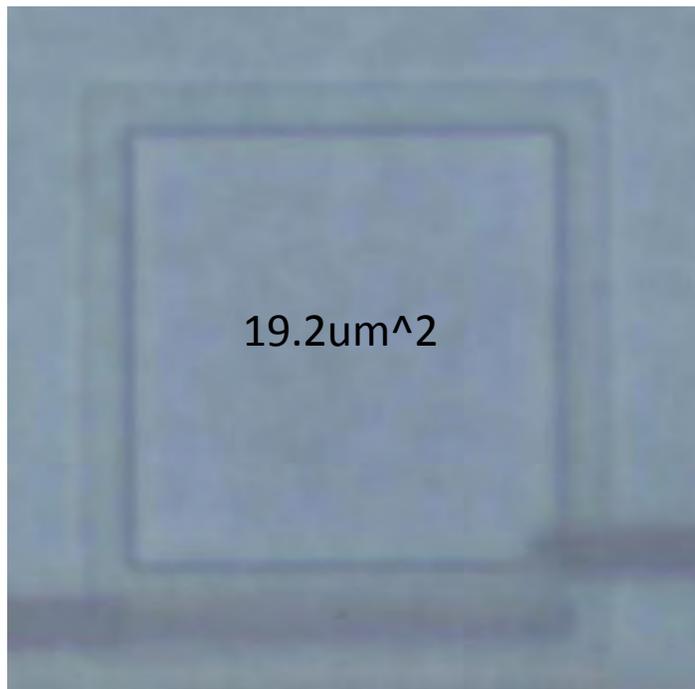
19.2um²



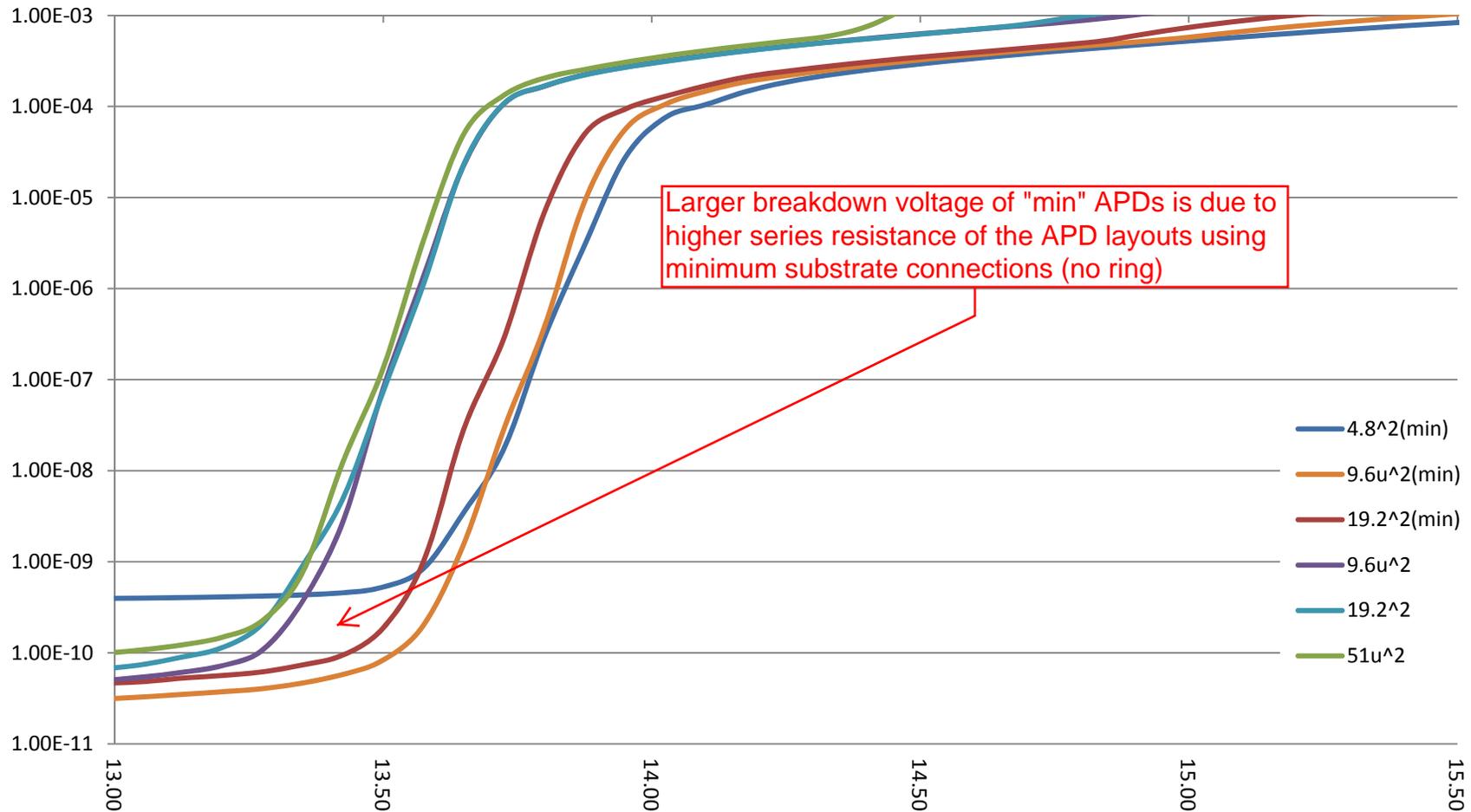
4.8um²



Minimum Guard Rings

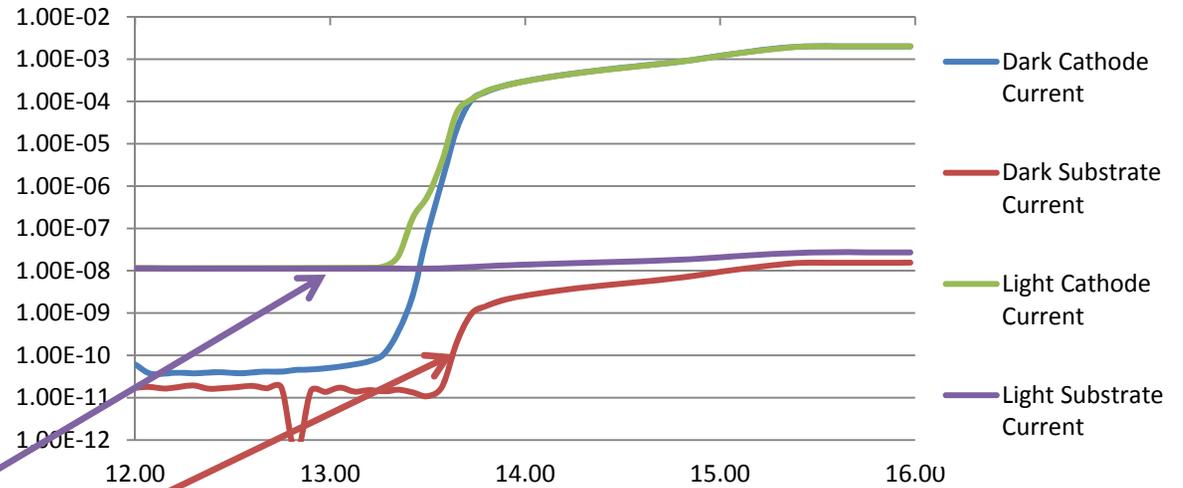
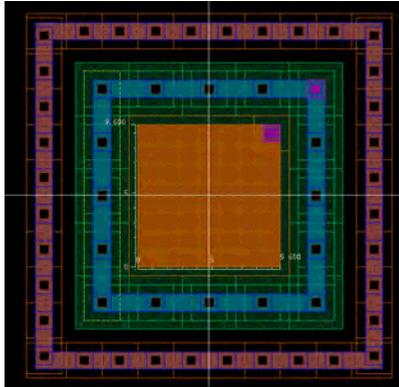


Various APD IV Curves (No Light)

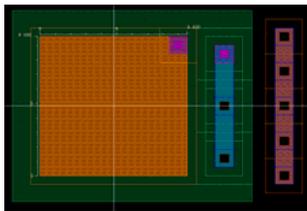


Reduced Guard Ring Layout

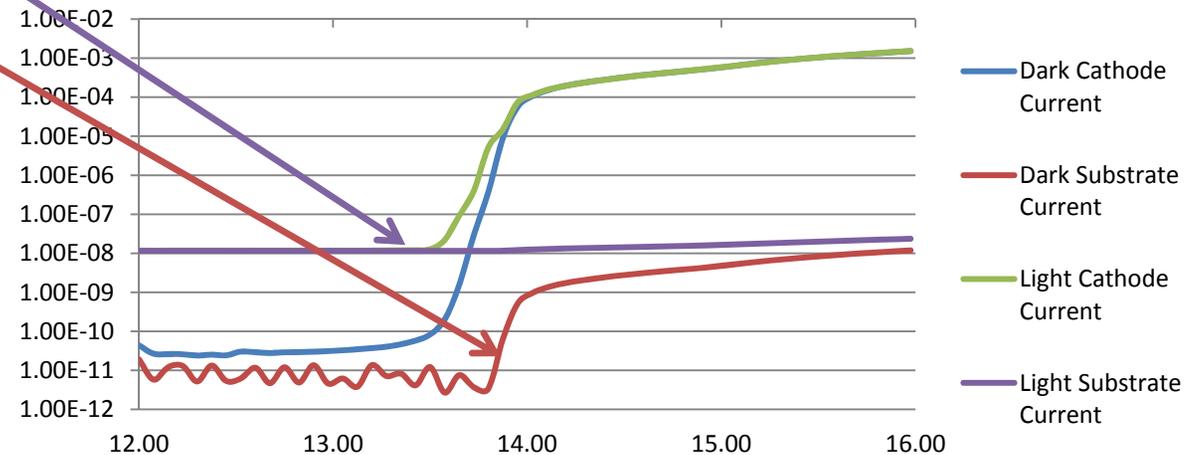
9.6 μ m² Active Area APD with Maximum Guard Rings



No Measureable Substrate Current Differences!



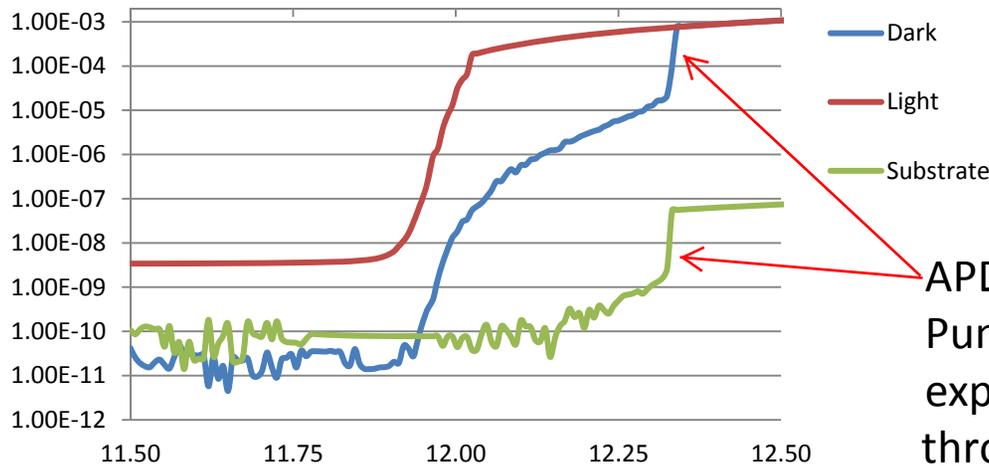
9.6 μ m² Active Area APD with Minimum Guard Rings



Note: Current measurements of 1.00E-11 are a stretch for the equipment used.

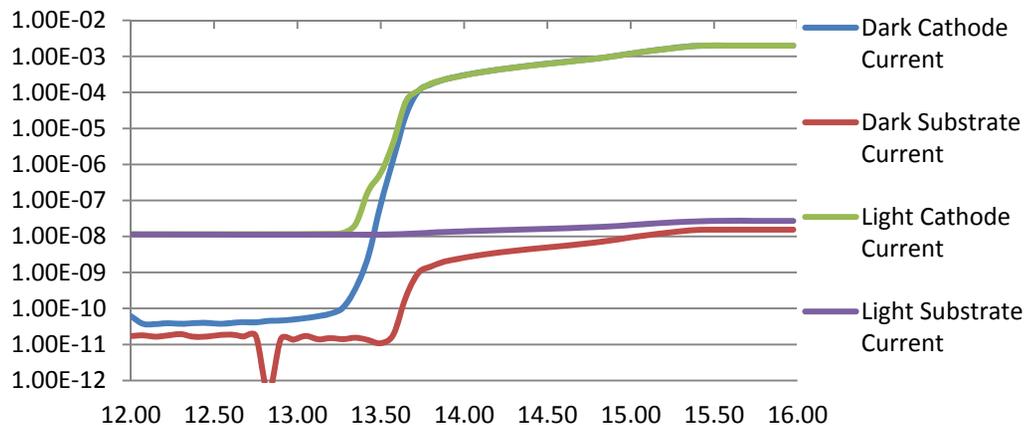
Punch-Through

Cathode and Substrate Current



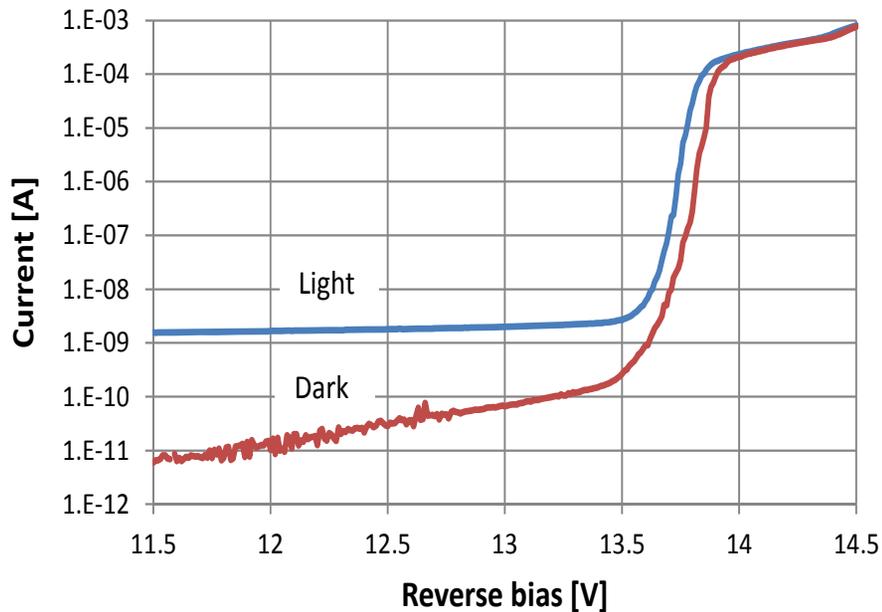
APD's Built using 180nm process. Punch-Through was an issue for these experimental APD's, E field punched through n-well shorting p+ to substrate.

9.6u² Active Area APD with Maximum Guard Rings



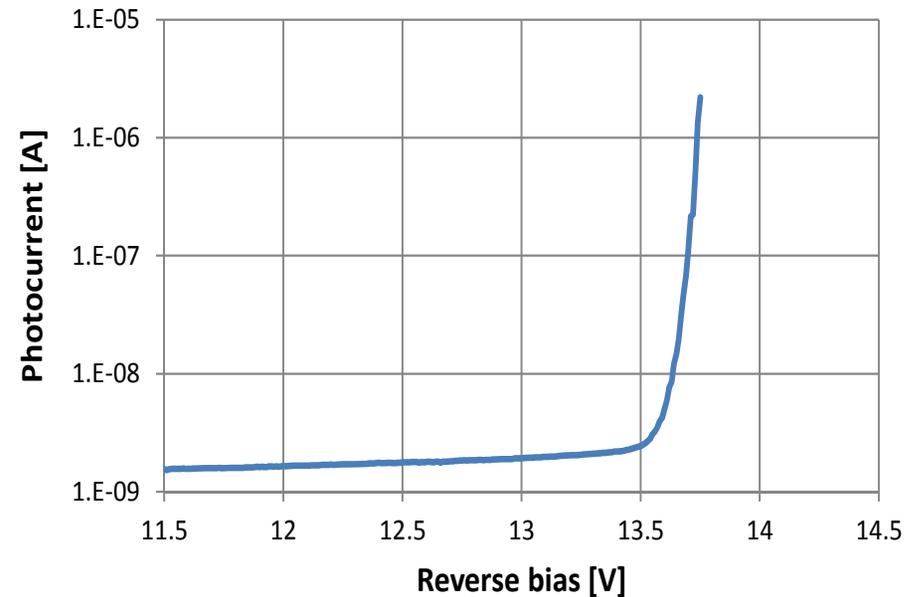
This issue was not observed for the APD's fabricated in ON's 500nm C5 process.

APD Current Measurements



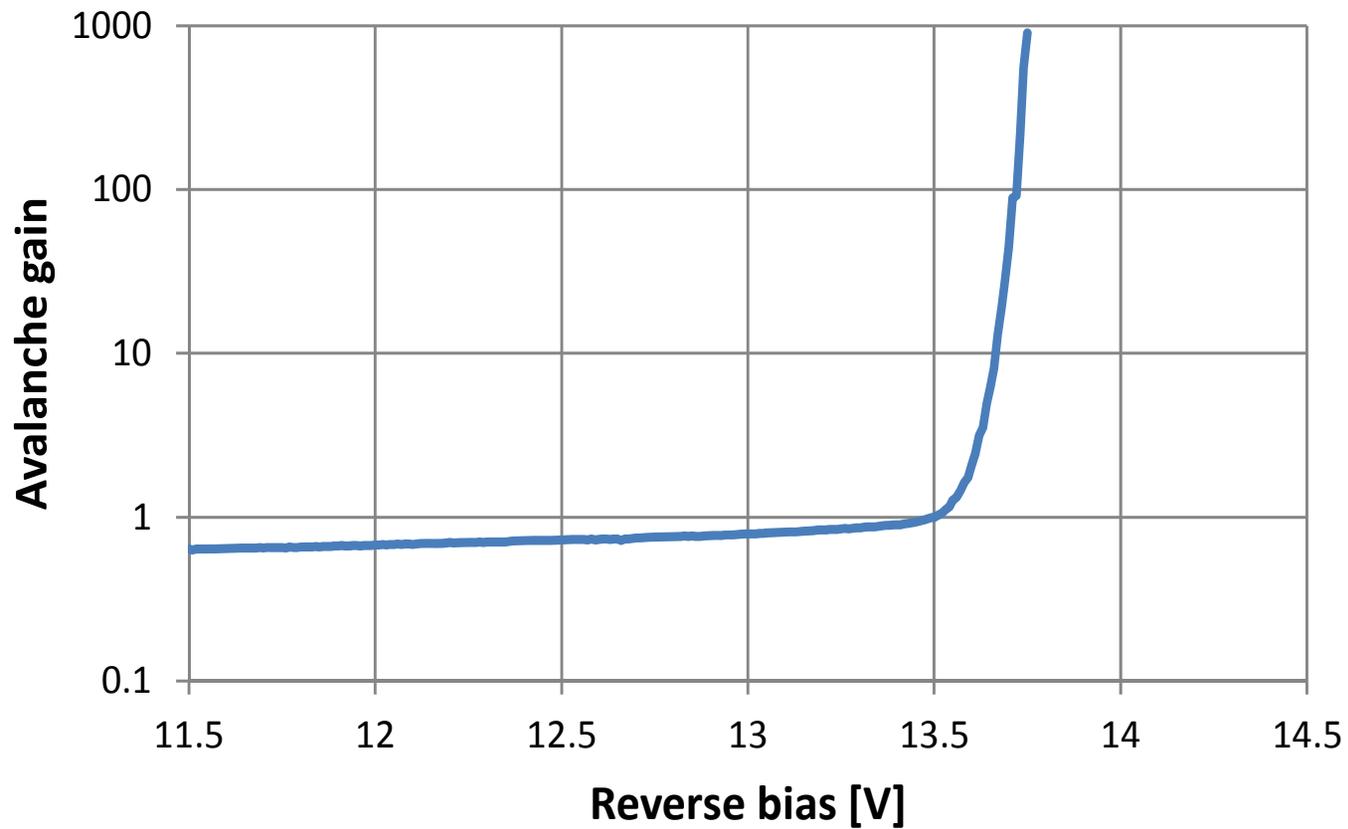
Light conditions produced with an uncalibrated broad-band microscope illuminator.

Dark Measurements produced by using a light-proof enclosure



Photocurrent Versus Reverse Bias. For the next slide, a gain of 1 will be defined at 13.5V just before the knee of the photocurrent.

APD Gain



Gains in excess of 1000 achievable at photocurrents of 10 μ A.

Future Work

- In depth APD Electrical Characteristics
 - Spectral Response, noise response, pulse characterization, etc.
- Using APD's along with on-die readout circuitry in a standard CMOS process.