A Linear High Gain Time Difference Amplifier Using Feedback Gain Control

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***Abstract*—This paper describes a feedback time difference amplifier (FTDA) with good linearity and high gain for coarse-fine time-to-digital converters. The symmetrical FTDA has two identical output generators. Each one consists of one SR-latch, one XOR gate, one buffer and two feedback P-type keepers. The improvement in linearity and time difference gain is achieved with two feedback paths based on meta-stability of the SR-latch. Its validity was demonstrated using 130nm CMOS technology. The power consumption is 91.54uW for the highest gain at 2MHz input signals. The gain can be controlled from 25.06 to 734.9 with a ±20ps input time interval.**

Keywords—Feedback; Time difference amplifier; Linearity; Gain control

I. INTRODUCTION

As CMOS process technology moves down towards the single-digital nanometer regime, decreasing intrinsic gain brings challenges to the design of mixed-signal blocks. However, the desire for smaller area and faster switching speed keeps on pushing the process dimensions going smaller and smaller. It results in continuously decreasing gate delay and further improvement in time-domain processing, while advanced small processes make the design of amplitude domain mixed-signal circuits more difficult.

The time-to-digital converters (TDCs), as the front-end block in time-domain processing, plays a significant role in quantizing time intervals between two rising edges. It has been widely employed in a variety of applications, such as time-of-flight (ToF) measurement, jitter measurement, all-digital phase-locked loop (ADPLL), particle physics, etc. The resolution offered by the TDC and its dynamic range of operation are among important factors in these applications.

Typically, the TDC is realized with a chain of inverters, but its resolution is limited to the propagation delay of a single inverter. A wide input range, high resolution TDC implementation spans a large area and consumes a great deal of power. Another method is to employ two buffer chains with different delays instead of one, which is called the Vernier delay line method [1],[2]. With its fine time resolution, it achieves sub-gate delays, but still suffers from large power dissipation and requires a large area for a wide dynamic range. Even worse, reaching high resolution requires that the two delay line be well-matched in layout design.

To improve the resolution and dynamic range of TDCs, several studies have focused on exploiting the time difference amplifier (TDA). Compared to Vernier delay-line TDCs, the TDA-based architecture enables coarse-fine conversion to improve these two parameters. Similar to voltage-type operational amplifiers, the TDA conceptually amplifies time differences. The large gain offered by a TDA enables a high resolution of two-step TDC yet with less components.

Various attempts [3]-[8] have been made to improve the performance of TDAs, including such variations as pulse-train TDA[3], closed-loop TDA[4], and meta-stability TDA with time offset[5]. However, all these methods can offer only a limited gain with poor linearity.

This paper proposed a new approach to increase the time difference gain by introducing a feedback technique with two mirrored output generators. Each one has two feedback paths, two inputs and one output. The proposed FTDA converts time intervals between two inputs into a voltage difference on a capacitor and manipulates the discharging current of the capacitor by using feedback keepers. Smaller discharging current results in longer output regeneration time. Therefore, the TDA gain can be enlarged and controlled.

The rest of the paper is organized as follows. Section II briefly introduces the principle of the conventional meta-stability TDA with two mutual exclusive circuits and an improved version using inverters as a time offset. Section III motivates and describes the feedback output generator and discusses the FTDA topology. Section IV presents the simulation results followed by conclusions in Section V.

II. CONVENTIONAL TDA

The conventional TDA with two mutual exclusive circuits (MUTEX) was first reported in [9]. It exploits the meta-stability of the SR-latch. As shown in Fig.1, the MUTEX consists of one SR-latch and one XOR gate. Two clock signals are connected to S and R nodes in the SR-latch.

The output regeneration time ΔT_{out} is a logarithmic function of the time difference between two rising edges ΔT_{SR}, which can be represented by the following equation

$$\Delta T_{out}=\tau*(\log V_{TH} - \log|\alpha*\Delta T_{SR}|) \quad (1)$$

where α is a proportional factor, $\tau=C/g_m$, g_m is the NAND gate transconductance, C is the SR-latch output capacitance and V_{TH} is the threshold voltage of the XOR gate.

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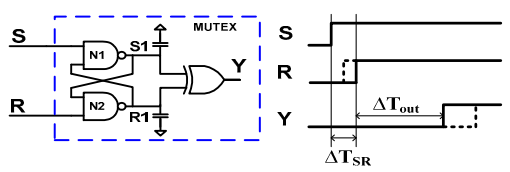

Fig. 1. MUTEX block with timing diagram

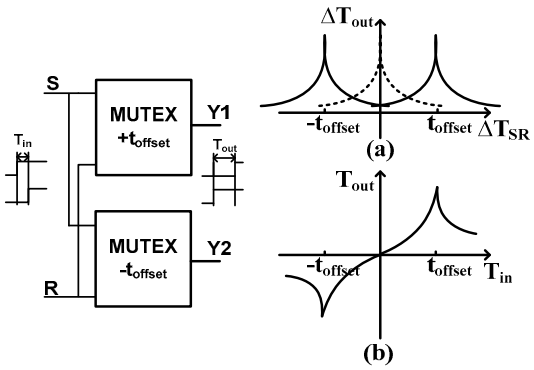

Fig. 2. Conventional TDA and (a) output regeneration time curve for each MUTEX; (b) input and output transfer charasteristic

The conventional TDA is shown in Fig.2. By using two MUTEX circuits with opposite time offsets, the meta-stability point of the SR-latch is shifted to realize the time difference amplification. The gain is equal to output time difference divided by input time difference, Δ_{out}/Δ_{in} , and is proportional to τ/t_{offset}. Thus, the time difference gain is achieved by adjusting the offset. However, not only is the gain small and easily affected by process/voltage/temperature (PVT) variations but also its linearity is constrained by a small input time range.

In [5], the method was proposed to use two inverters at each input to improve the conventional architecture. However, the gain is still small and the linearity range is constrained by the inverters.

III. Proposed Feedback TDA

To achieve high time difference gain, we proposed the feedback topology. The output regeneration time is amplified and controlled by two feedback paths in the output generator.

A. Output generator

The proposed output generator is shown in Fig.3. It offers the same functionality as a MUTEX circuit and differs by inserting a buffer and adding two feedback P-type keepers [10] at SR-latch outputs. Time difference amplification is thus realized by taking advantage of meta-stability of the SR-latch and the use of feedback. The keepers' gates are connected to the same node S1. Two clock signals are given to IN1 and IN2 and time difference T_{in} between their rising edges is regarded as the FTDA's input. If IN1 is assumed to rise to VDD earlier than IN2, T_{in} becomes positive. Otherwise, T_{in} is negative. The four steps of the process are described in detail below.

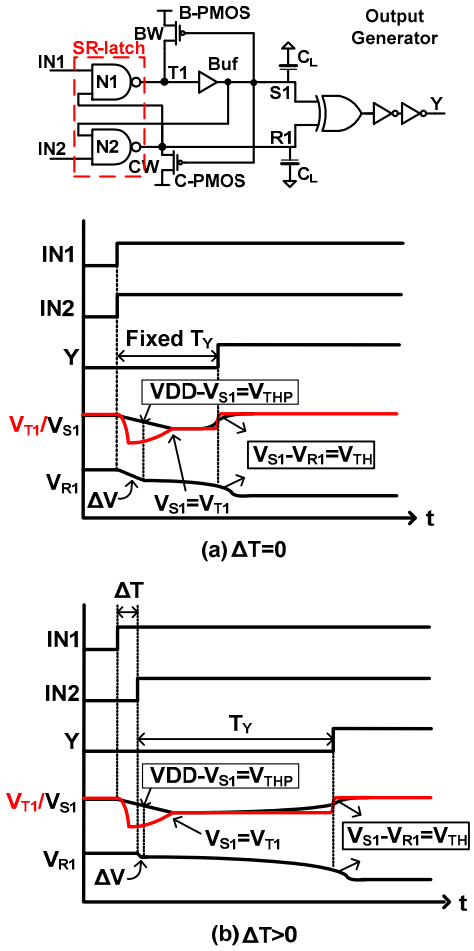

Fig. 3. Output generator block and timing diagram

As shown in Fig.3, the voltages at S1, T1 and R1 are initially equal to *VDD*. The feedback keepers (B-PMOS and C-PMOS) are turned off. Take the positive T_{in} as an example and assume IN1 rising up to *VDD* at t0.

The first step is when IN1 rises to *VDD* V_{T1} is pulled down to *GND* with a NAND gate delay. V_{S1} is also decreasing but slower than V_{T1} because of capacitor C_L. V_{R1} remains at *VDD* without change.

The second step occurs at the time t1 when B-PMOS and C-PMOS are turned on when V_{S1} becomes equal to $VDD-|V_{THP}|$. Meanwhile, V_{T1} is pulled up by turned-on B-PMOS.

The status of V_{R1} depends on the rising edge of IN2. If IN2 rises before t1, V_{R1} gets a ΔV reduction before C-PMOS is turned on. Otherwise, if IN2 rises after t1, V_{R1} stays at *VDD*. Comparing the timing diagram in Fig.3 (a) and (b), the smaller T_{in} becomes, the larger the ΔV. The rising edge of IN2 causes to start discharging V_{R1}. For a larger ΔV the capacitor will be discharged more quickly, otherwise, the time will be longer. Hence, output regeneration time is negatively proportional to $|\Delta V|$.

The third step is when B-PMOS becomes diode-connected, which means gate voltage V_{S1} is equal to drain voltage V_{T1}.

The discharging process of two load capacitors is used to further determine output regeneration time as depicted in Fig.4. The size of B-PMOS is set to keep the currents balanced for keeping V_{T1} equal to V_{S1}. The drain current I_{CP} of C-PMOS is made smaller than I_{BP} by using a smaller width of device, which makes V_{R1} reduce more slowly. Thereby, reduction speed of V_{R1} is controlled by current difference

$$I_C = I_{CP} + I_{P2} - I_{N2} \quad (2)$$

The output regeneration time control is thus achieved. In other words, a wide C-PMOS enables decreasing the discharge current I_C and increasing the output regeneration time.

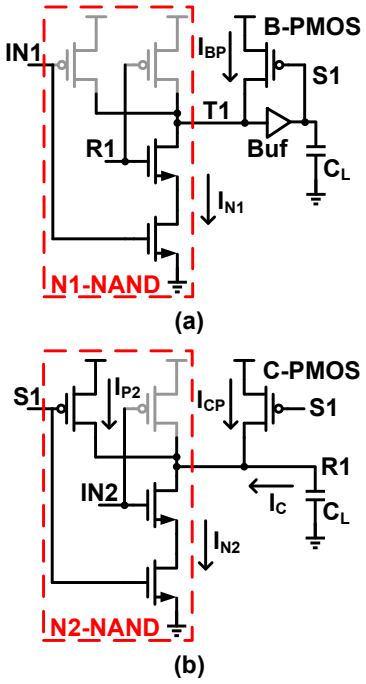

Fig. 4. (a) Current balance model and (b) capacitor discharging model

The size of C-PMOS controls the reduction speed of V_{R1}. A properly-sized buffer inserted between B-PMOS gate and drain is used to maintain the V_{R1} reduction situation. If the buffer has less delay, the faster-decreasing V_{S1} will pull V_{R1} up. Otherwise, the slowly-decreasing V_{S1} will speed up V_{R1} reduction and make output regeneration time shorter.

In addition, for a larger T_{in}, the V_{R1} reduction curve becomes longer. The input time interval is positively proportional to the beginning value of V_{R1} when both keepers are turned on. The discharging time of a capacitor is calculated based on the following equations. It is reasonable to achieve positive time amplification by making the C/I_C larger than one.

$$\left.\begin{array}{c} V_{R1} \propto T_{in} \\ I_C * \Delta t = C * (V_{R1} - 0) = C * V_{R1} \end{array}\right\} \rightarrow \Delta t = \frac{C * V_{R1}}{I_C} \propto \frac{C * T_{in}}{I_C} \quad (3)$$

The final step is logic generation. As V_{R1} continues to reduce, it turns on the PMOS of N1 in Fig.4(a). The unbalanced current between B-PMOS and NAND gate therefore causes both V_{T1} and V_{S1} to increase. When the difference between V_{S1} and V_{R1} is equal to the threshold voltage of the XOR gate, the XOR gate's output Y toggles to *VDD*.

In this context, the output generation time T_Y, which is the difference between the rising edge of output and the later rising edge of the two input signals, is amplified and controlled by feedback P-type keepers.

A special case happens at $T_{in}=0$. The rising edges of IN1 and IN2 are at the same time. The proposed feedback output generator still goes through four steps and the feedback technique slows down the V_{S1} and V_{R1} reduction speed to make the output regeneration time a constant value $T_Y(0)$ as shown in Fig.3(a).

B. Proposed time difference amplifier

As shown in Fig.5, the proposed FTDA consists of two mirrored output generators and their inputs are cross-coupled to get opposite input time differences. For example, if IN1 rises earlier than IN2, the up-side generator has a positive input interval but the down-side generator has a negative input interval. Both generation times, Y1 and Y2, are linearly proportional to the input time difference T_{in} but have the opposite slope in the input range. The input-output transfer characteristic of each generator and the entire FTDA are depicted in Fig.5. The FTDA's output T_{out} is derived by subtracting T_{Y2} from T_{Y1} as in (4). Therefore, the FTDA's final gain becomes twice the slope gradient and the constant value $T_Y(0)$ theoretically could be removed.

$$\left.\begin{array}{l} T_{Y1} = gain * T_{in} + T_Y(0) \\ T_{Y2} = -gain * T_{in} + T_Y(0) \end{array}\right\}$$

$$\rightarrow T_{out} = T_{Y1} - T_{Y2} = 2 * gain * T_{in} \quad (4)$$

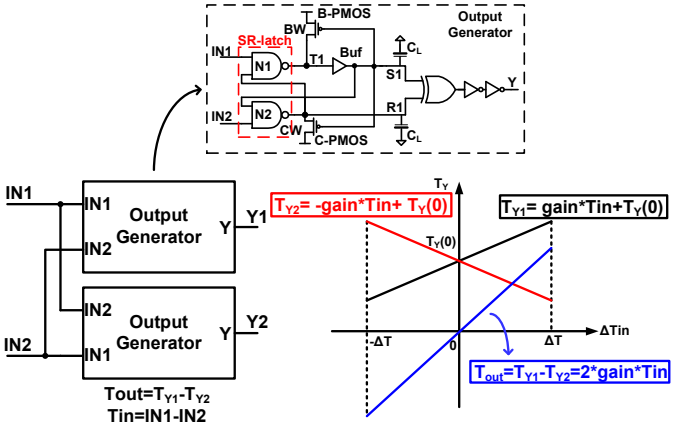

Fig. 5. Proposed FTDA with input-output transfer charastersitics

IV. Simulation

The proposed FTDA with feedback keepers is demonstrated to provide a high gain time difference amplification by using 130nm CMOS technology with 1.2V supply voltage. In the feedback output generators, the larger B-PMOS is used to achieve the current balance situation. The size of C-PMOS varies from 280nm to 500nm. The capacitor in each input nodes of the XOR gates is 500fF. The simulation results illustrated in

Fig.6-7 demonstrates the time difference amplification and that the FTDA's gain is controllable by changing the width of the C-PMOS.

The time difference amplification can be as high as 734 in the input time ranging from -20ps to 20ps. The FTDA with the highest gain needs to set the input frequency smaller than 2MHz. When reducing the gain, the requirement of input clock frequency can be relaxed. Moreover, the time difference gain provided by FTDA is linear for the entire input time range. The maximum standard deviation is 6.18 for gain equal to 734.

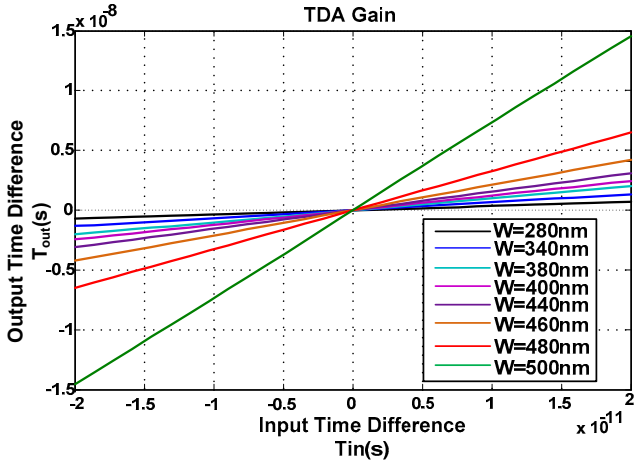

Fig. 6. Transfer characteristic of different C-PMOS width

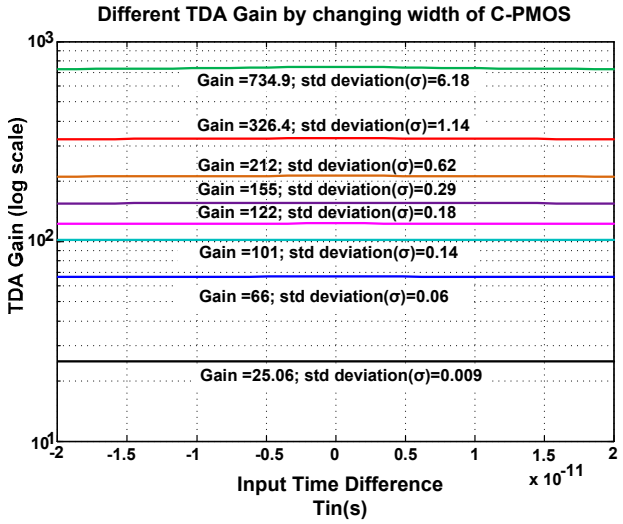

Fig. 7. Time difference gain with standard deviation for different C-PMOS width width

V. Conclusions and Future Work

In this paper, a feedback TDA was proposed as an improvement to the gain and linearity. The FTDA comprises a mirrored architecture consisting of two identical proposed feedback output generators. Two P-type keepers are inserted to provide feedback. The concept of time amplification is achieved and expanded. It also provides a controllable time difference gain feature. The capacitor discharging model has been used to analyze the feedback gain control procedure. As a result, the proposed FTDA achieves the highest linear time difference gain as depicted in Table I. However, it suffers from excessive PVT variation.

Future work will focus on using compensation technique to solving the PVT issue and applying the FTDA to high-resolution two-step TDCs.

TABLE I. Comparison of Different TDAs

Methods	Gain	Input Range(ps)	Process(nm)
Ref[3]	2-8	0-200	65
Ref[4]	4	±300	180
Ref[5]	20	±40	90
Ref[6]	10-120	±2000	130
Ref[7]	4-117	±300	90
Ref[8]	27-150	±20	110
This work	25-734	±20	130

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