Design of Bandpass Delta-Sigma Modulators: Avoiding Common Mistakes

R. Jacob Baker and Vishal Saxena
Department of Electrical and Computer Engineering
Boise State University
1910 University Dr., ET 201
Boise, ID 83725
jbaker@boisestate.edu

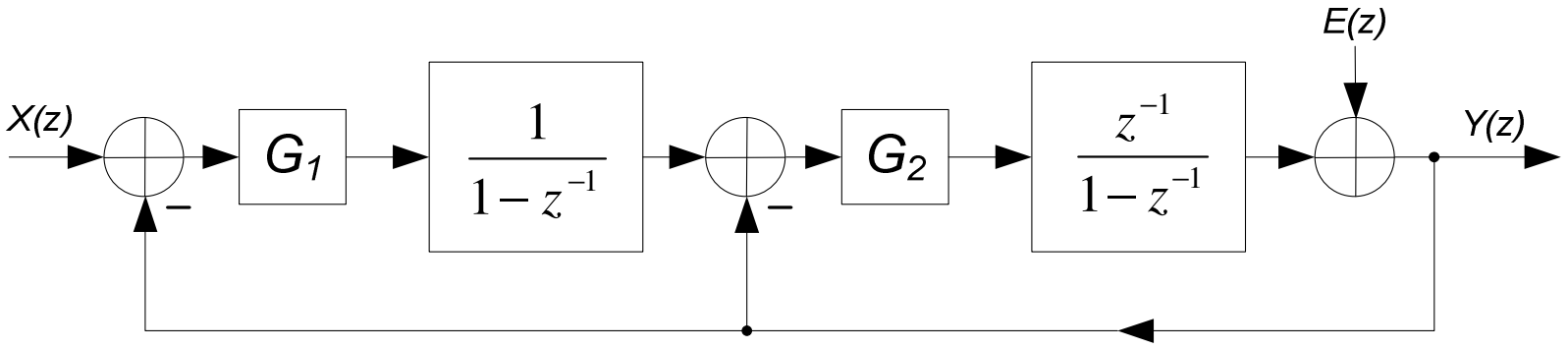
Abstract –Implementation of analog-to-digital converters in the IF stage of a communication receiver can employ bandpass delta-sigma modulation (BPDSM). The benefit of using BPDSM is the ease with which in-phase (I) and quadrature (Q) components of the information can be extracted and translated to DC (to minimize both power and the required operating speeds). BPDSM topologies are commonly based on a cascade of resonators with transfer functions of $z^{-2}/(1 + z^{-2})$. This talk will show that these topologies, seen frequently in the literature, are always unstable. Discussions concerning the design of BPDSM-based analog-to-digital converters, in the IF stage, will be presented including why two or more paths are required and the details of implementing I/Q demodulation. Finally, examples will be given that show how the design topologies are applied.

Low Pass Delta-Sigma Modulation (DSM)

- A low pass second order delta sigma modulator is described by the following transfer function

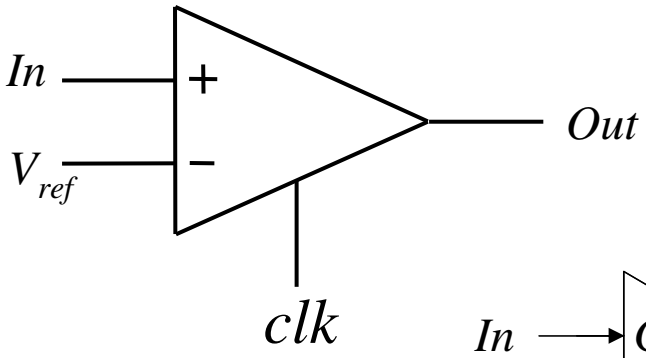
$$Y(z) = X(z) \cdot \overbrace{z^{-1}}^{STF} + E(z) \cdot \overbrace{\left(1 - z^{-1}\right)^2}^{NTF}$$

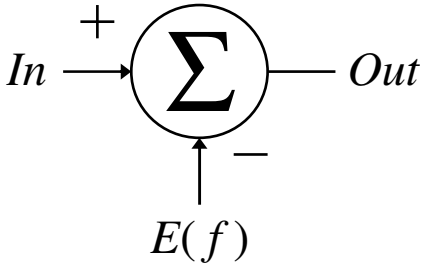
- This equation is implemented using



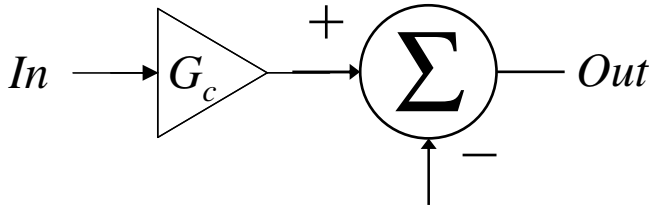
A Common Mistake

- Modeling the comparator with **only** an additive noise source doesn't accurately model the performance of the modulator
  - ✓ Still useful for estimating performance and describing mathematically
  - ✓ Assumes the added noise source is white (it isn't)
  - ✓ Better to add both additive and multiplicative noise sources
  - ✓ Careful! While SPICE will show accurate performance (for a particular input signal) other methods of simulating DSM may not





Additive noise only



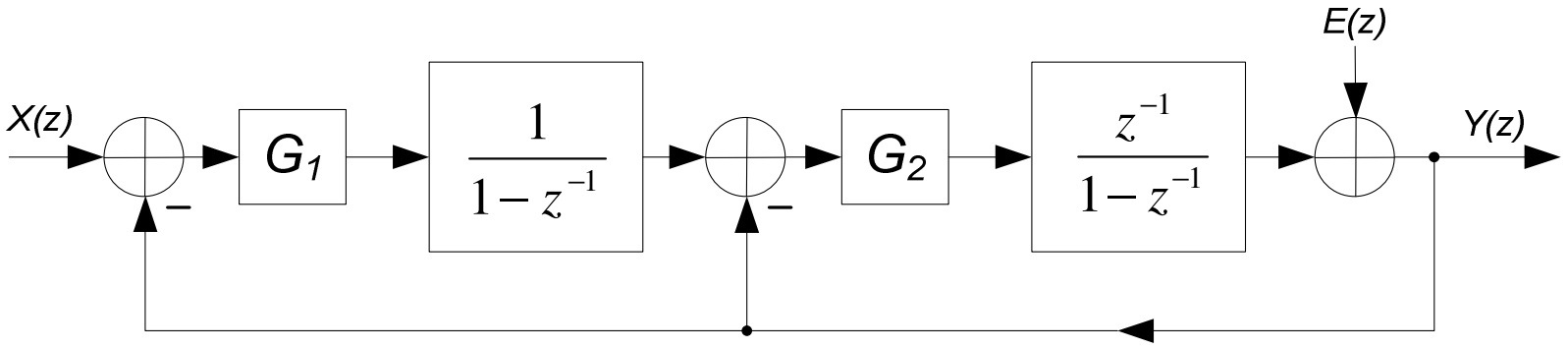
Adding gain and a white noise source

Comments on low pass DSM transfer function

- Notice that this equation was derived assuming G_1 and G_2 are unity (and they are likely < 1 to keep the integrators from saturating)

$$Y(z) = X(z) \cdot \overbrace{z^{-1}}^{STF} + E(z) \cdot \overbrace{\left(1 - z^{-1}\right)^2}^{NTF}$$

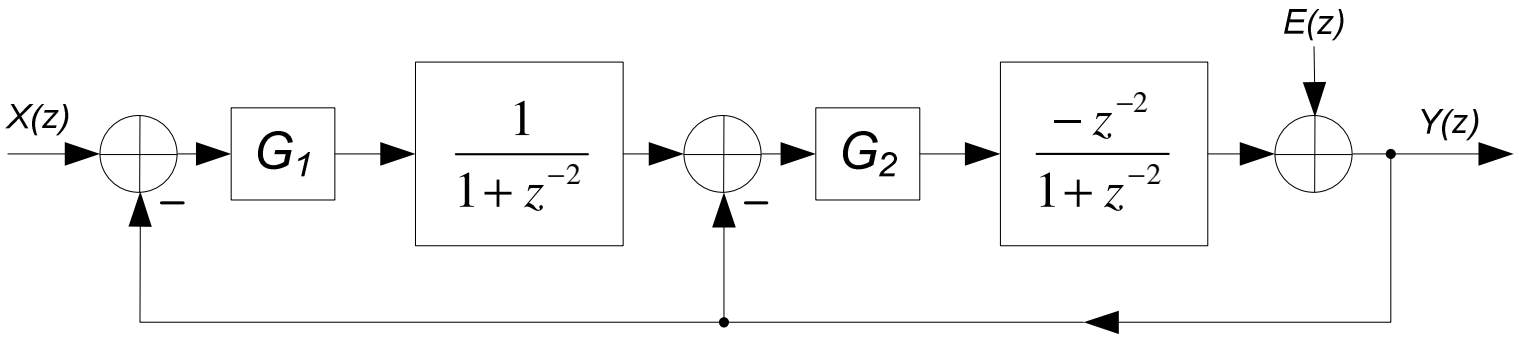
- Re-derive the transfer function adding a comparator gain and see that forward (STF) gain goes to 1 and this equation is valid



Band Pass Delta-Sigma Modulation (BPDSM)

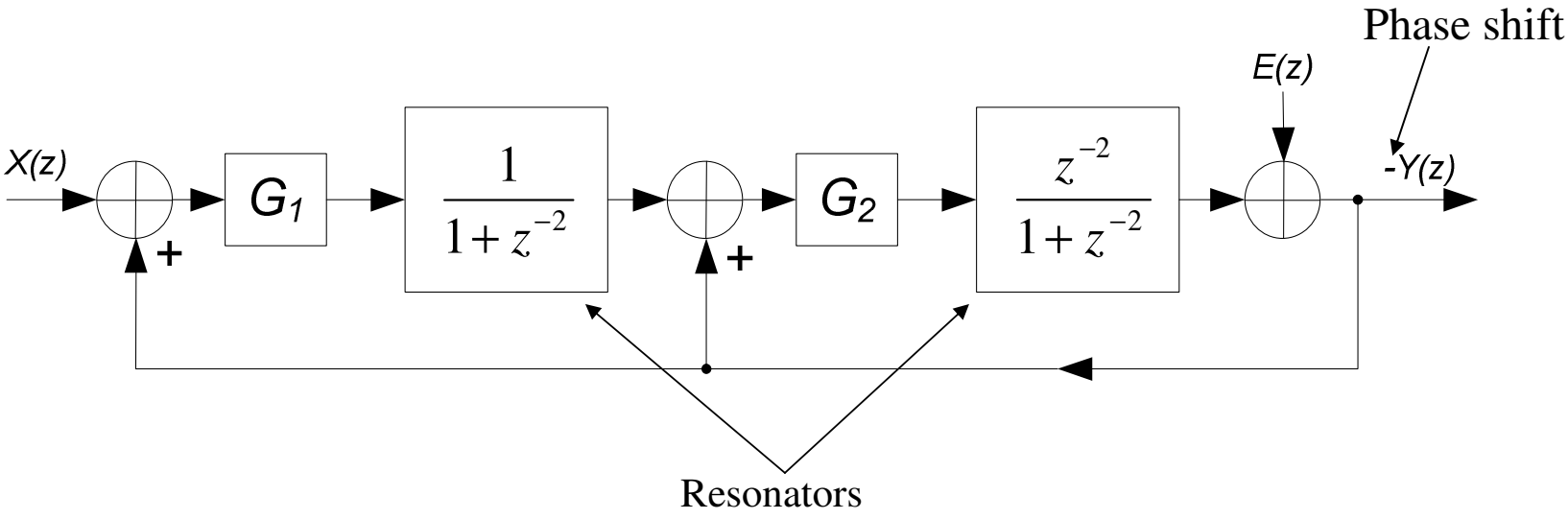
- A fourth order $f_s/4$ band pass delta sigma modulator (BPDSM) can be easily obtained by substituting $-z^{-2}$ for z^{-1} in the low pass second order DSM. The transfer function of the resulting band pass modulator is given as (assuming $G_1 = G_2 = 1$),

$$Y(z) = X(z)\cdot\overbrace{\left(-z^{-2}\right)}^{STF} + E(z)\cdot\overbrace{\left(1+z^{-2}\right)^{2}}^{NTF}$$



Redrawing the BPDSM topology

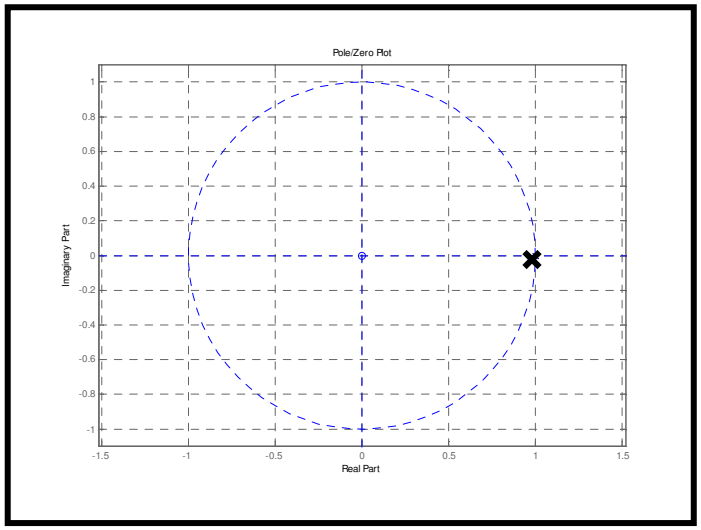
- Implementation of the BPDSM
- The next question we need to answer is how do we implement the resonators?
  - ✓ The problem is getting two delays for the feedback paths



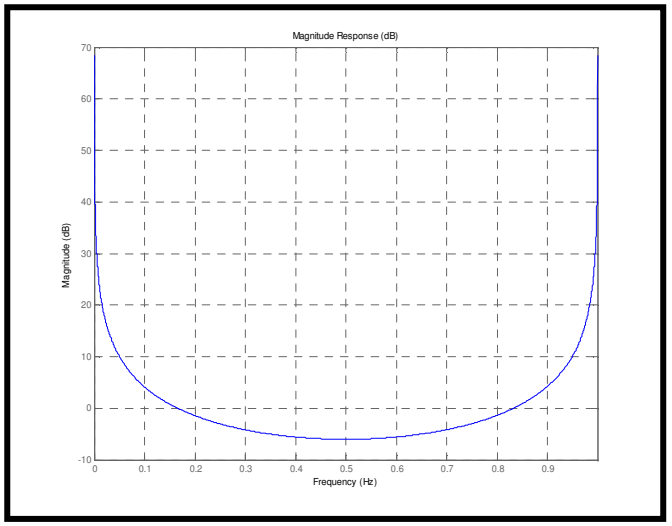
Changing z^{-1} to z^{-2}

- The integrator block in the low pass modulator becomes a resonator in the equivalent band pass modulator topology. The low pass to band pass modulator transformation can be understood as moving the pole at 1 to +/– j. The modulation noise for the bandpass modulator can now be written as

$$\left|NTF(f)\right|^2 . \left|V_{Qe}(f)\right|^2 = \frac{V_{LSB}^2}{12 f_s} . \left(2\cos\left(2\pi \frac{f}{f_s}\right)\right)^4$$



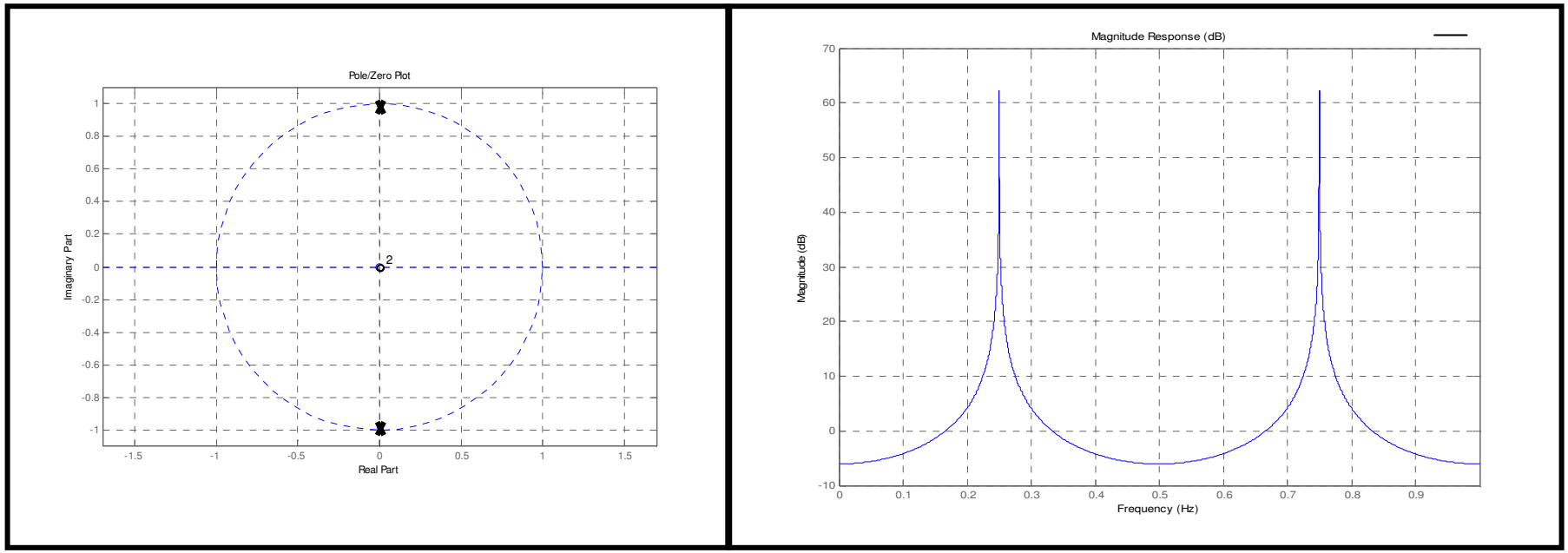
z-plane for discrete integrator



Magnitude response for the integrator

Changing z^{-1} to z^{-2}, continued

- Below is the z-plane plot and magnitude response for $z^2/(z^2 + 1)$



z-plane for the resonators

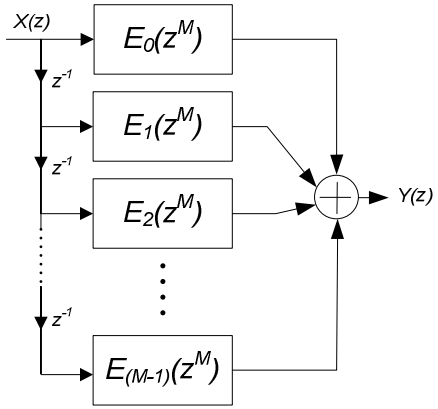
Magnitude response of the resonator

Polyphase Decomposition and Two-Path Implementation

- Polyphase decomposition is a standard DSP technique which results in simpler implementation of filters. A filter $H(z)$ can be decomposed*

$$H(z) = \sum_{k=0}^{M-1} E_k\left(z^M\right) z^{-k} \qquad e_k[n] = h[nM + k] = h_k[nM]$$

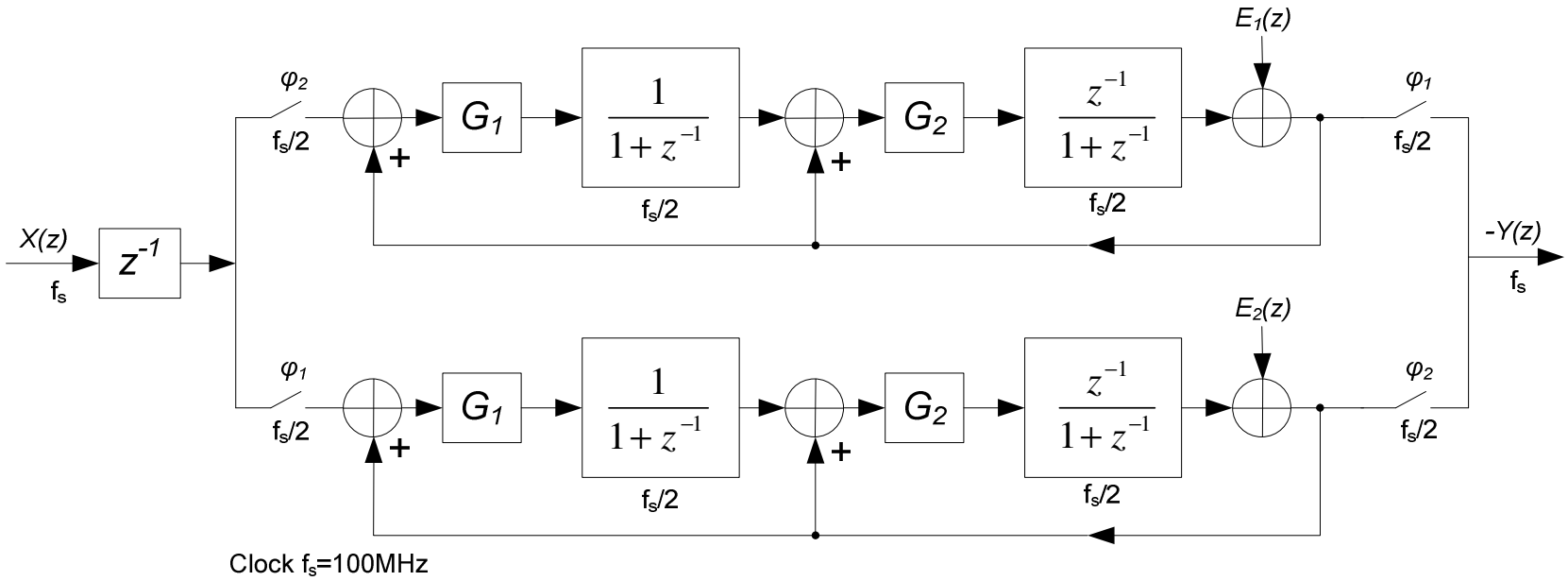
where $h_k[n] = h[n+k]$ for n=integer multiple of M, otherwise = 0.



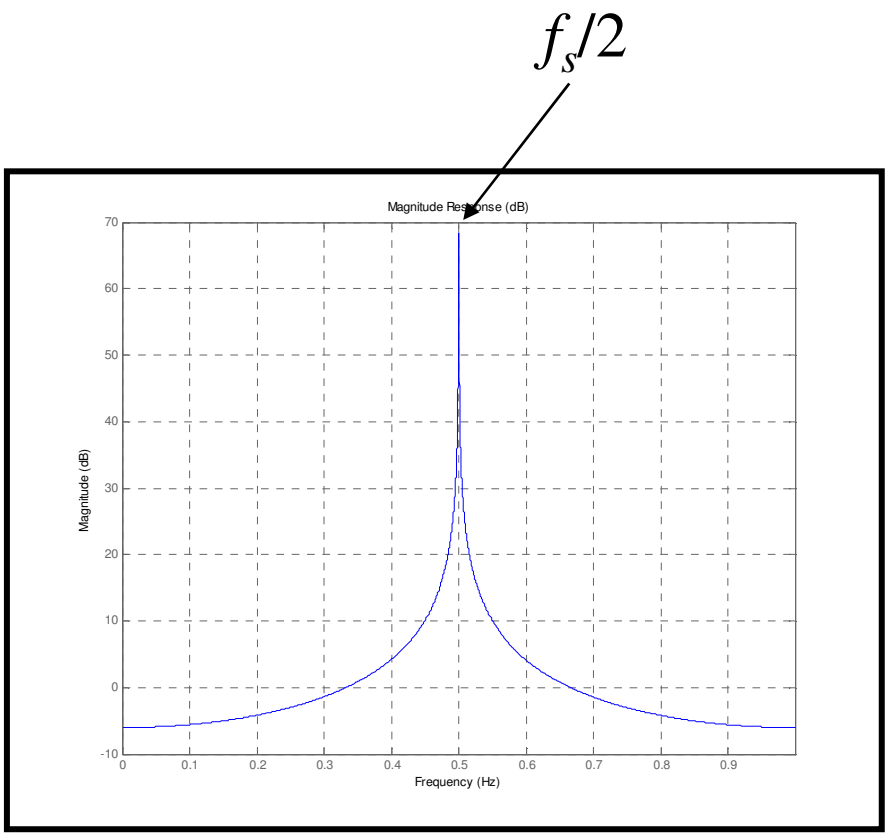
* A. V. Oppenheim, R. W. Schafer, *Discrete-Time Signal Processing, 2nd ed.*, pgs.180-183 : Prentice Hall, 1999.

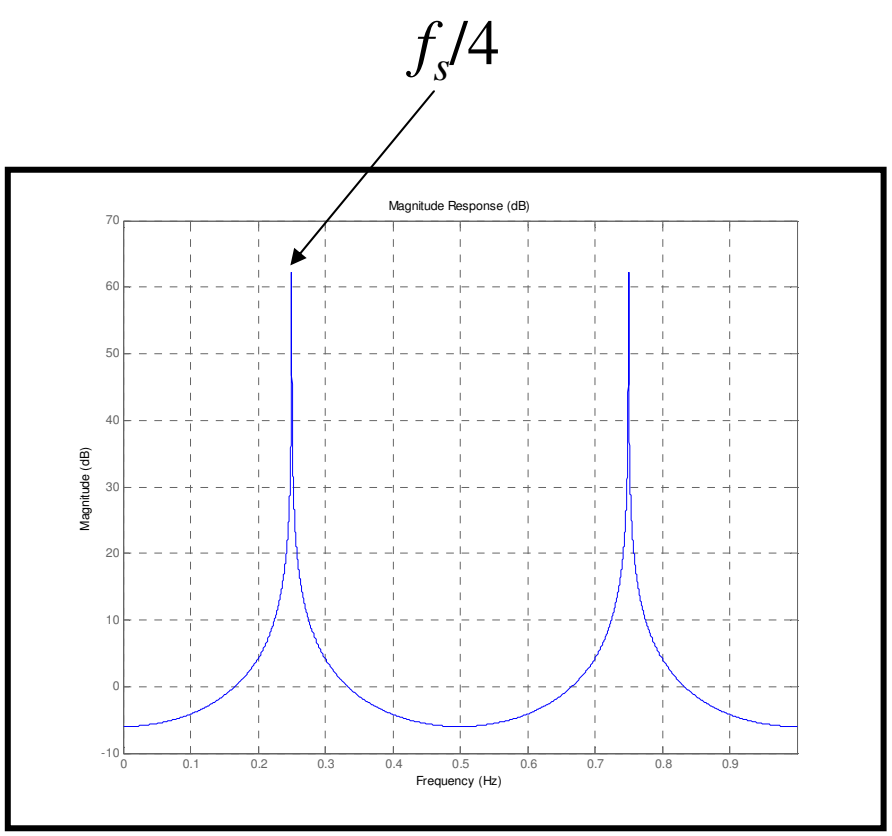
Changing z^{-1} to z^{-2}, continued

- By using two paths we essentially double the sampling frequency.
  - ✓ This changes z^{-1} to z^{-2}
  - ✓ Note that we are actually using $f_s/2$ resonators!



Frequency response of the sections



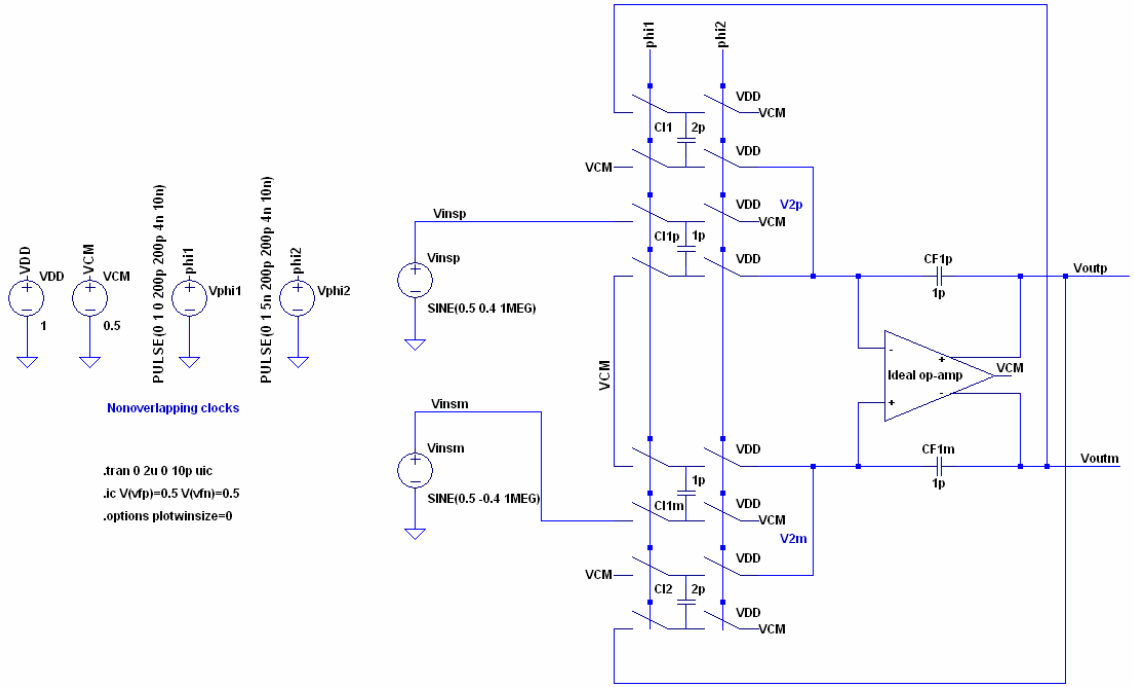


Frequency response of $1/(1 + z^{-1})$, note this is a high-pass response.

Using two paths, $1/(1 + z^{-2})$, note that this is a band pass response.

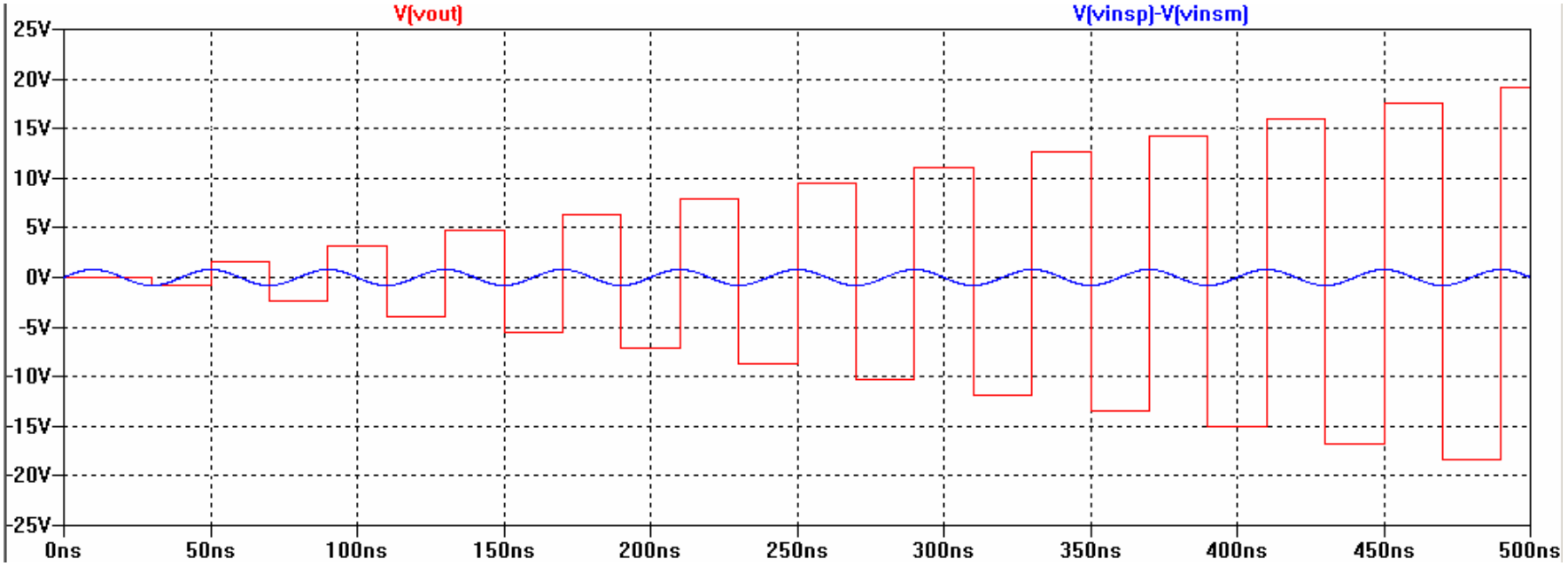
Switched-Capacitor Implementation of $1/(1 + z^{-1})$, an $f_s/2$ resonator

- A basic building block for $1/(1 + z^{-1})$
  - ✓ Well (!) actually the transfer function is $z^{-1/2}/(1 + z^{-1})$
  - ✓ This is why we can't have a non-delaying second stage in our BPDSM
  - ✓ It's also why we added a delay to the input in our two-path topology seen on page 10

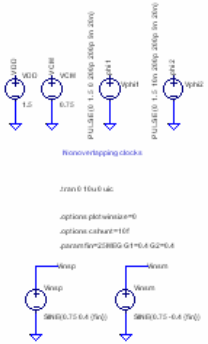


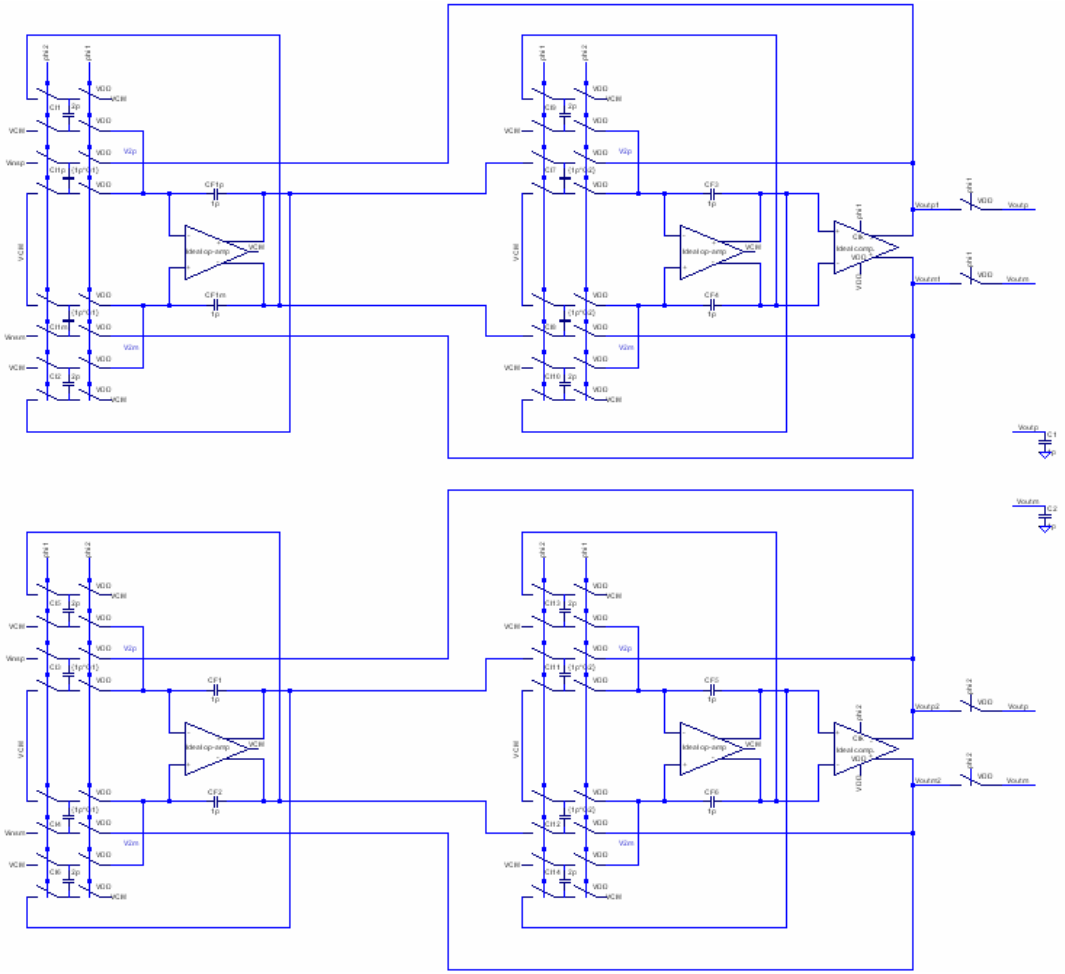
Simulating an $f_s/2$ resonator

- Poles are right on the unit circle (so we see instability of course)
  - ✓ All of the simulations in this presentation are found at:
    - o http://cmosedu.com/cmos1/LTspice/LTspice.htm
    - o Install LTspice, unzip the simulations in LTspice_cmosedu.zip to the desktop and go to \Extras_LTspice\Ch8_MSD_LTspice



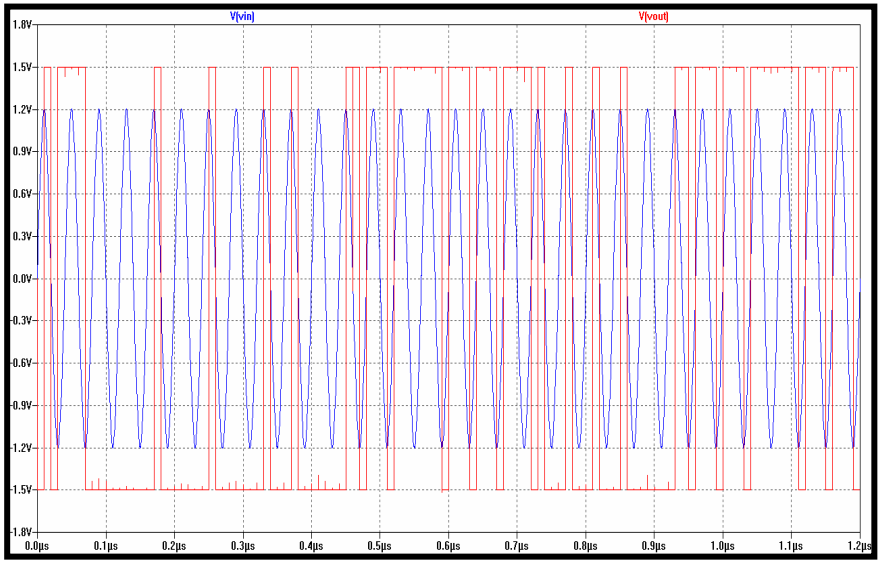
Implementation of a BPDSM at $f_s/4$

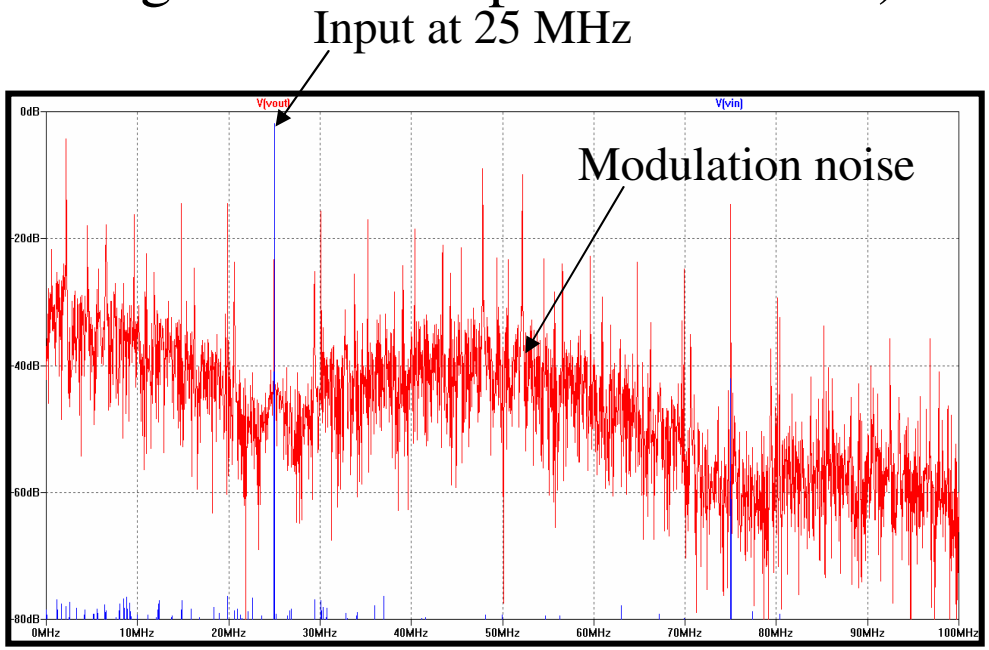




Simulating Operation

- The band pass modulator shapes and moves the quantization noise away from the IF at 25MHz. We can observe spurious tones for an input of 25MHz. These tones are due to the limit cycle oscillations in the system (just like applying a DC signal to a low pass modulator).



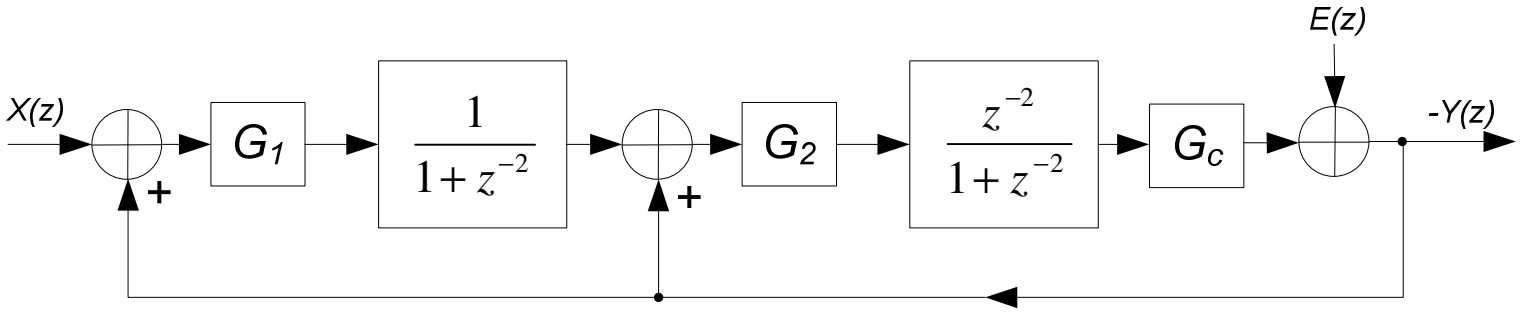


Modulator Stability and Parameters Selection

- The transfer function for BPDSM is (including comparator gain, G_C), where the forward gain, G_F, = $G_1G_2G_C$, is

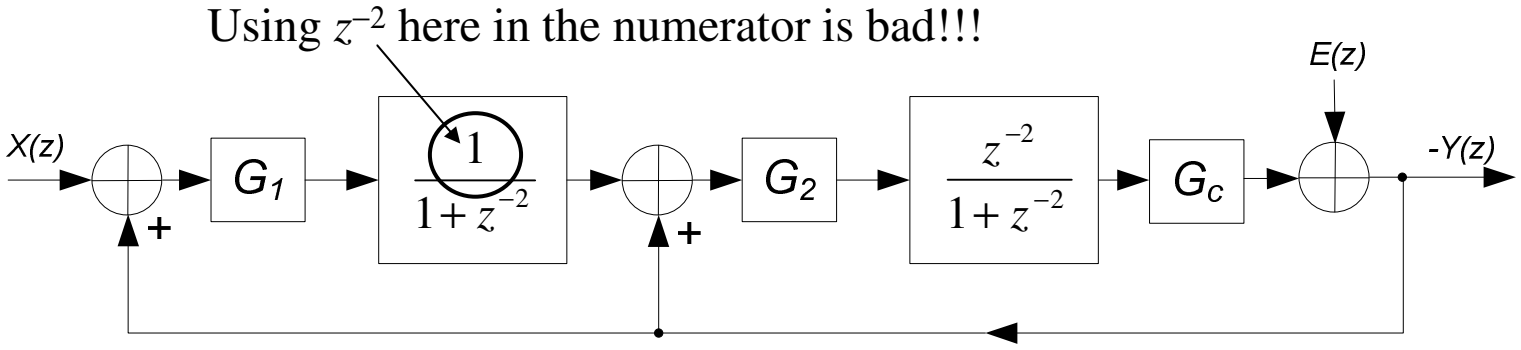
$$Y(z) = X(z)\cdot \overbrace{\frac{G_F z^{-2}}{\left((G_2G_c-1)z^{-4}+(G_F+G_2G_c-2)z^{-2}-1\right)}}^{STF} + E(z)\cdot \overbrace{\frac{-\left(1+z^{-2}\right)^2}{\left((G_2G_c-1)z^{-4}+(G_F+G_2G_c-2)z^{-2}-1\right)}}^{NTF}$$

- By using low pass filters in the simulations the gain values can be determined
  - ✓ Note that a common mistake is to exclude the comparator's gain when determining the transfer function and thus the stability



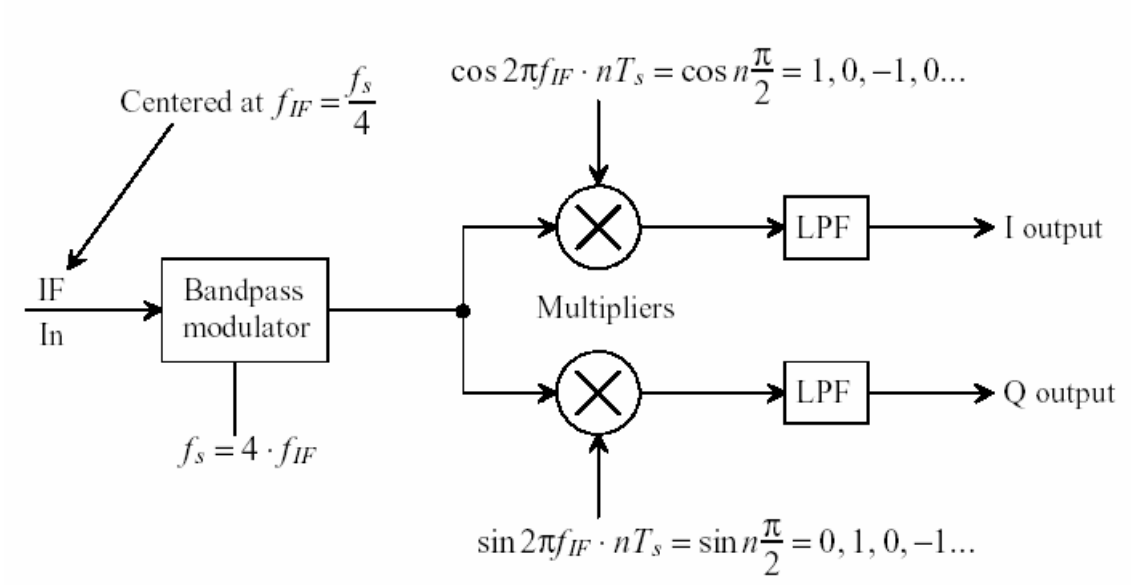
A Common Mistake

- Using two delaying resonators is a common mistake found in the literature!
  - ✓ Adding gratuitous delay in the forward or feedback paths of a feedback system makes the system move towards instability
  - ✓ The difference between a delaying and non-delaying resonator is simply a switch in the clock phases (swap the clock connections in the stage)
  - ✓ This, using a delaying first stage, is also a common mistake found in the literature covering the design of low pass delta-sigma modulators
  - ✓ Note that it can be shown, both mathematically and with SPICE simulations, that a modulator using a cascade of two delaying resonators is impossible to make stable (so be careful when looking at the published literature!)



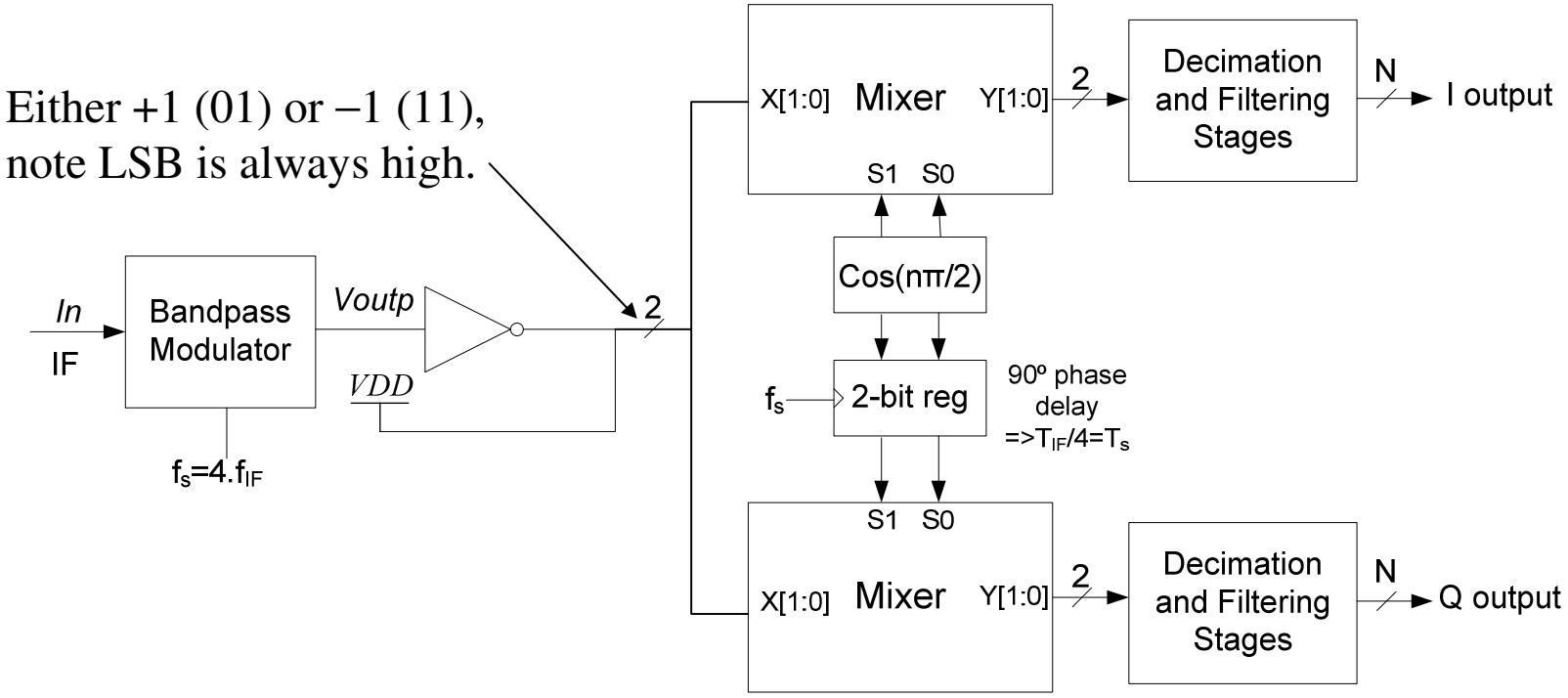
Digital I/Q Demodulation

- The band pass modulator can be used for fully digital I/Q demodulation in a heterodyne receiver
  - ✓ In the examples here the intermediate frequency, IF,= $f_s/4$, is 25Mhz
  - ✓ For this case, the mixing operation is very simple and can be accomplished using some simple digital logic



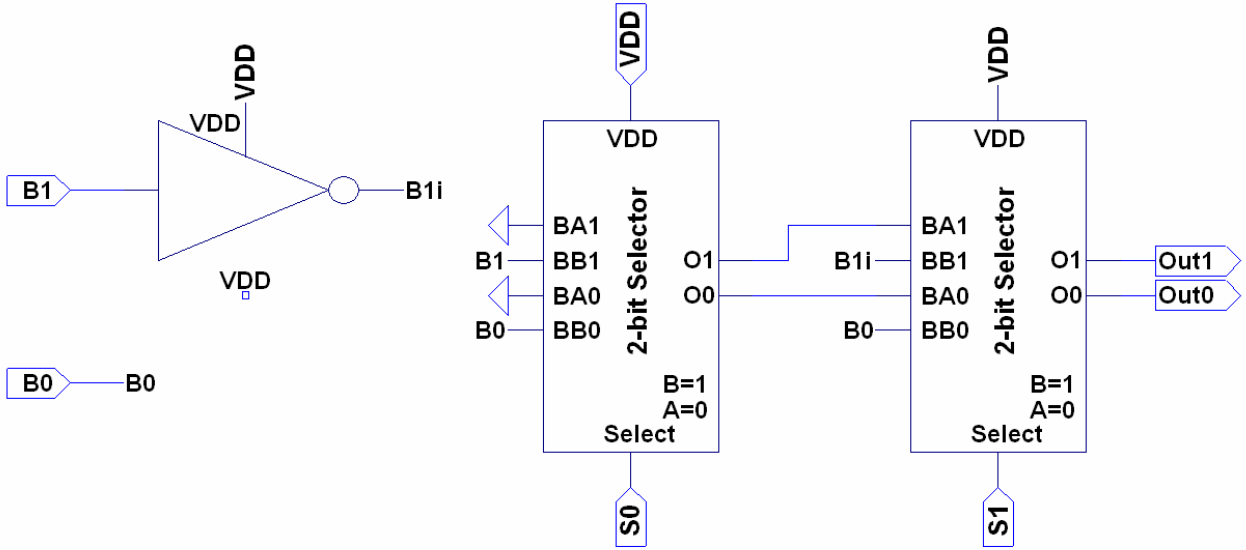
Fully digital Implementation of I/Q demodulation

- The output of the bandpass modulator (i.e. +1,–1) is converted to 2-bit two's complement format. The modulator output is then digitally mixed using MUXes as seen below.



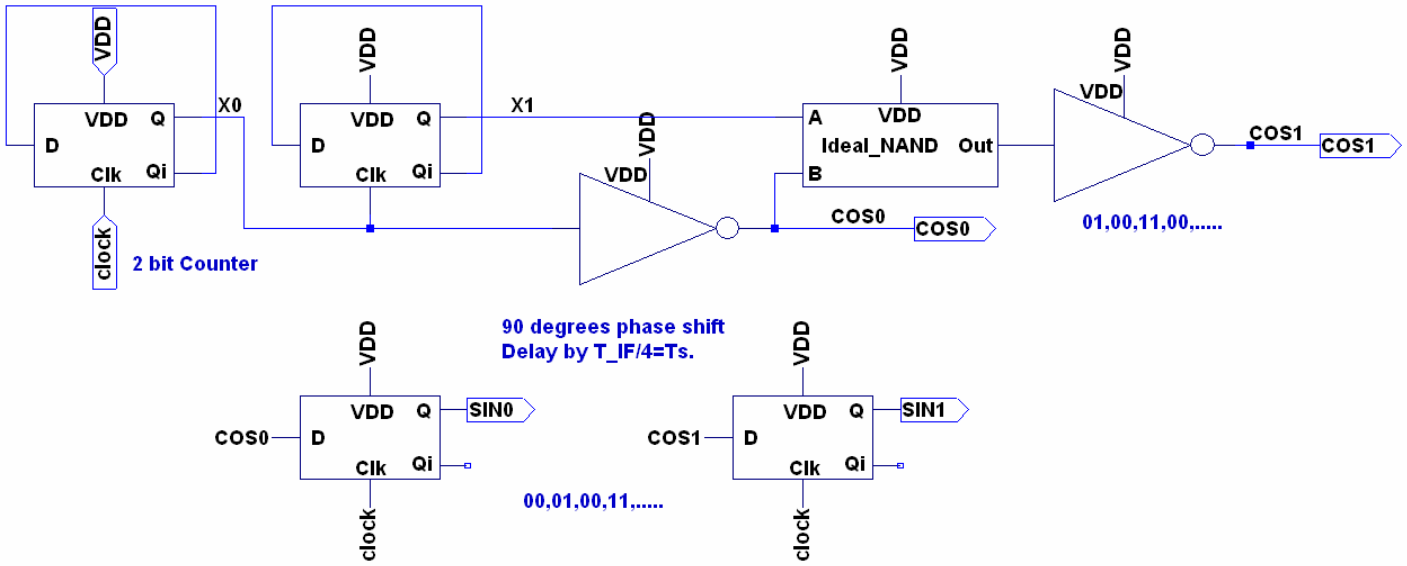
Digital Mixer Implementation using Selectors (aka MUXes)

- The output of the reference generator is, $\cos(2\pi f_{IF} n T_s) = \cos(n\pi/2) = 1, 0, -1, 0, \ldots$ sequence, which in 2's complement format is 01, 00, 11, 00, …sequence.
- Note that the point of doing digital I/Q demodulation is that we move the digital data down to a low frequency (for a general communication system, like transmission of voice, this may be in the kHz range)
- Low power can thus be obtained and DSP can be used



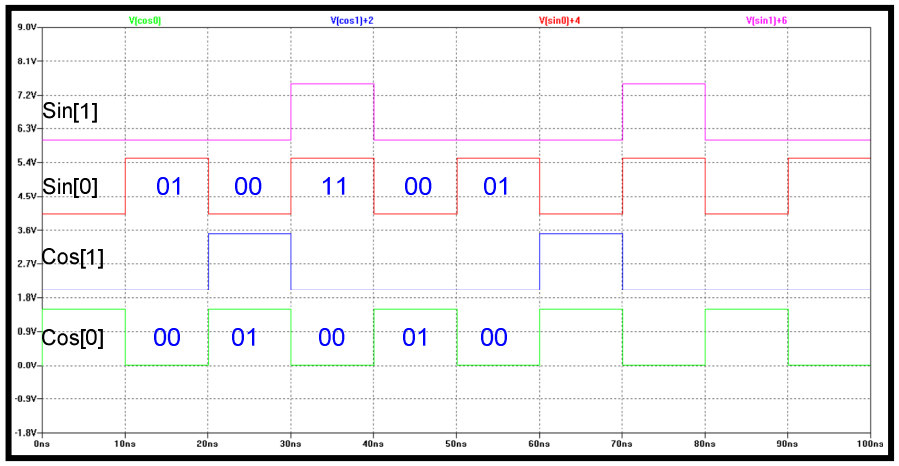
Digital I/Q Demodulation, cont'd

- A 2 bit counter with combinatorial logic is employed to generate the cos(nπ/2) sequence as shown below. The sin(nπ/2) sequence (=00,01,00,11,…) is generated by delaying the cos(nπ/2) sequence by 90º, which is same as delaying it by one Ts period ($T_s = T_{IF}/4$ => 90º delay).

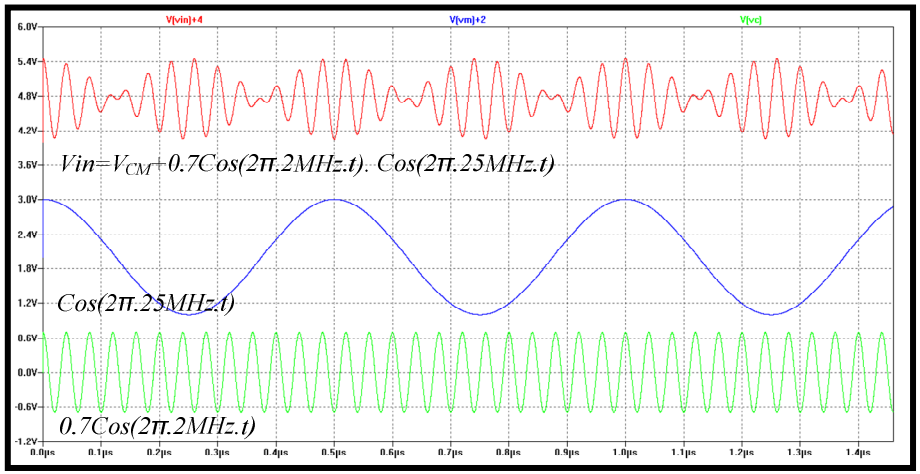


Example

- An AM modulated cosinusoidal carrier at 25MHz is used as the input to the system in order to demonstrate the *I*/*Q* demodulation.
- A cosinusoidal modulating signal with 2MHz frequency is employed. Thus the modulated signal is given as,
  - ✓ $V_{in} = V_{CM} + 0.7 \cdot cos(2\pi \cdot 2\text{MHz} \cdot t) \cdot cos(2\pi \cdot 25\text{MHz} \cdot t)$



Plot showing the COS and SIN sequences.



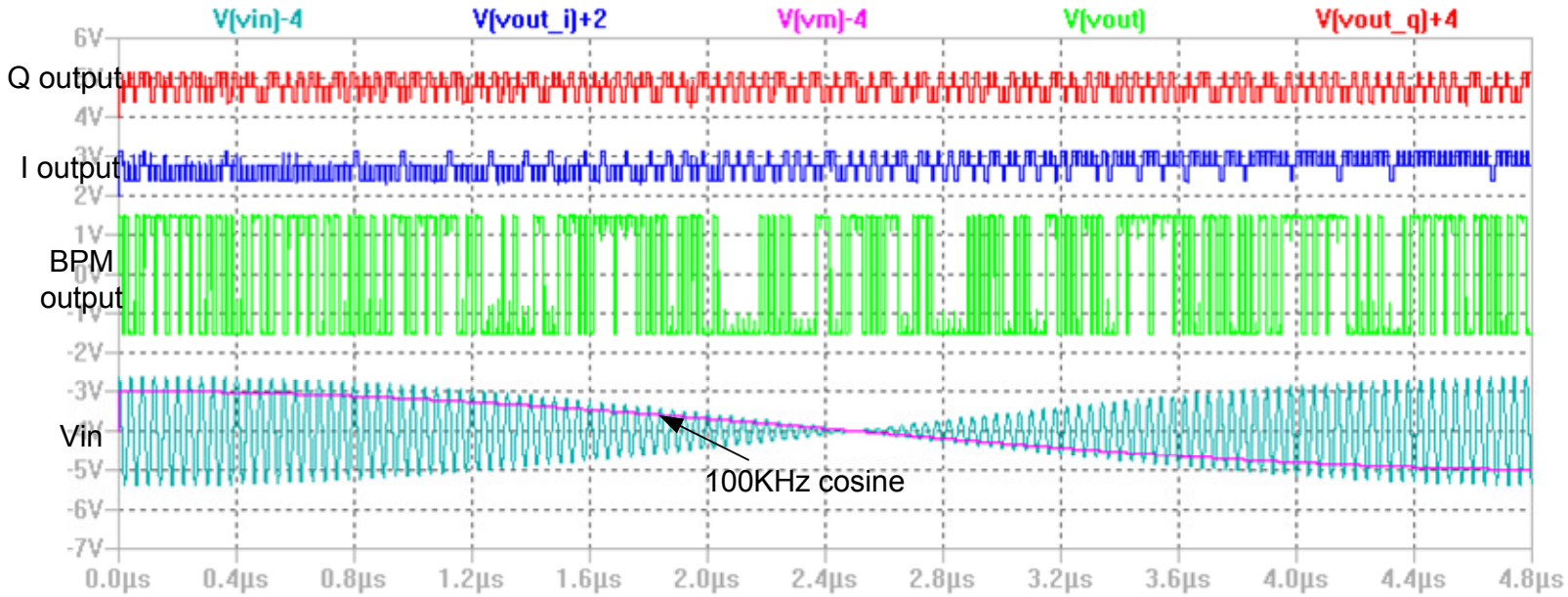
Plot showing the AM modulated input used for testing the I/Q demodulator.

Example, cont'd

- An *I*/*Q* modulated signal is described as

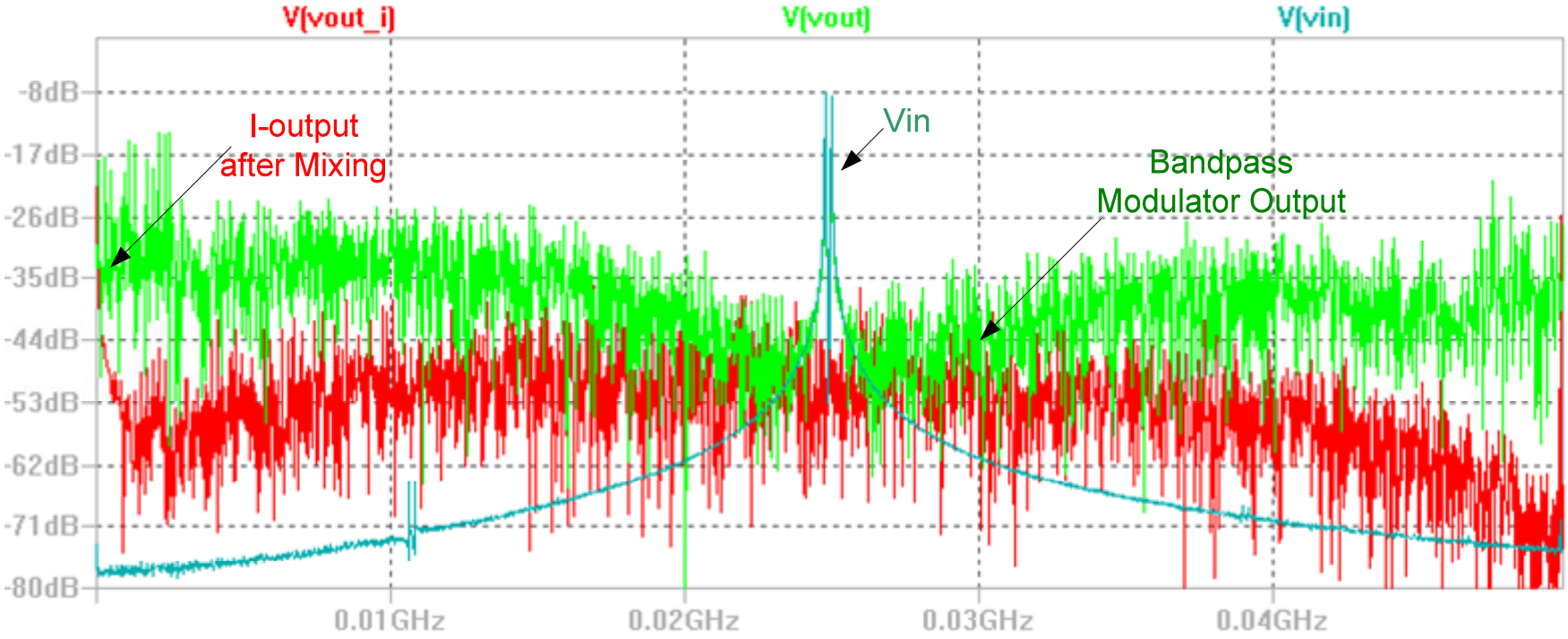
$$s(t) = A_c \cdot [m_I(t) \cdot cos(2\pi f_c t) + m_Q(t) \cdot sin(2\pi f_c t)]$$

- Here the *I* component is $m_I(t)$= 0.7·cos(2π·2MHz·t) and the *Q* component, $m_Q(t)$, is 0 (a DC voltage of V_{CM}=0.75V).
- Below is an example where we've used a modulating signal of 100 kHz (instead of 2 MHz)
  - ✓ The bottom trace, the *I* component, shows both the modulated carrier and the final 100 kHz output after filtering (the *Q* component output is a DC voltage of 0.75 V)



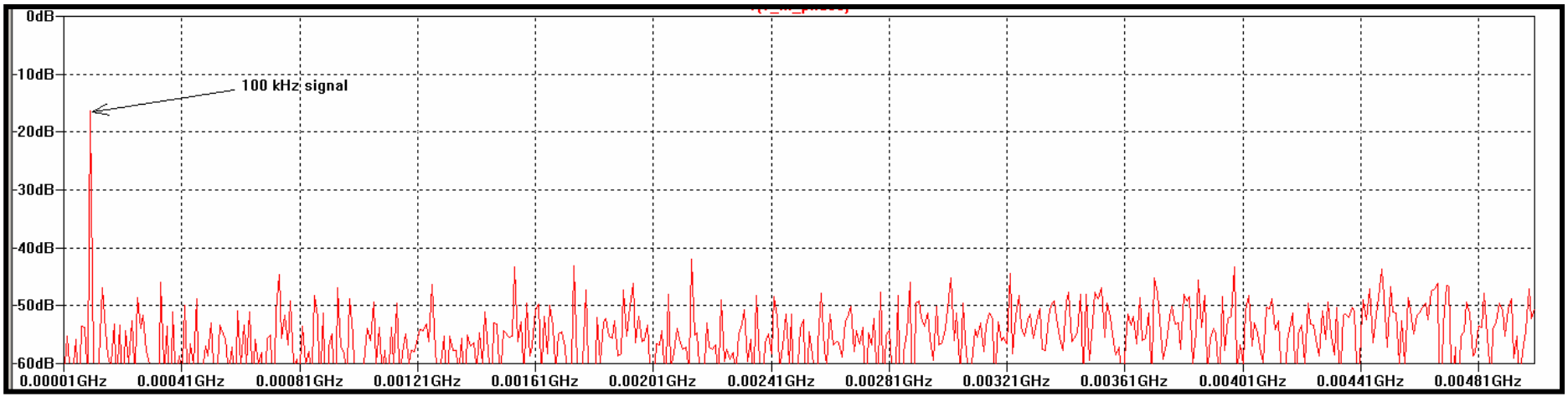
Example, cont'd

- Showing the spectrums of the signals at various points in our receiver.
  - ✓ Note the carrier is 25 MHz and the information is offset from the carrier by 100 kHz (here 24.9 and 25.1 MHz)
- Note how the in-phase component is shifted down to DC.



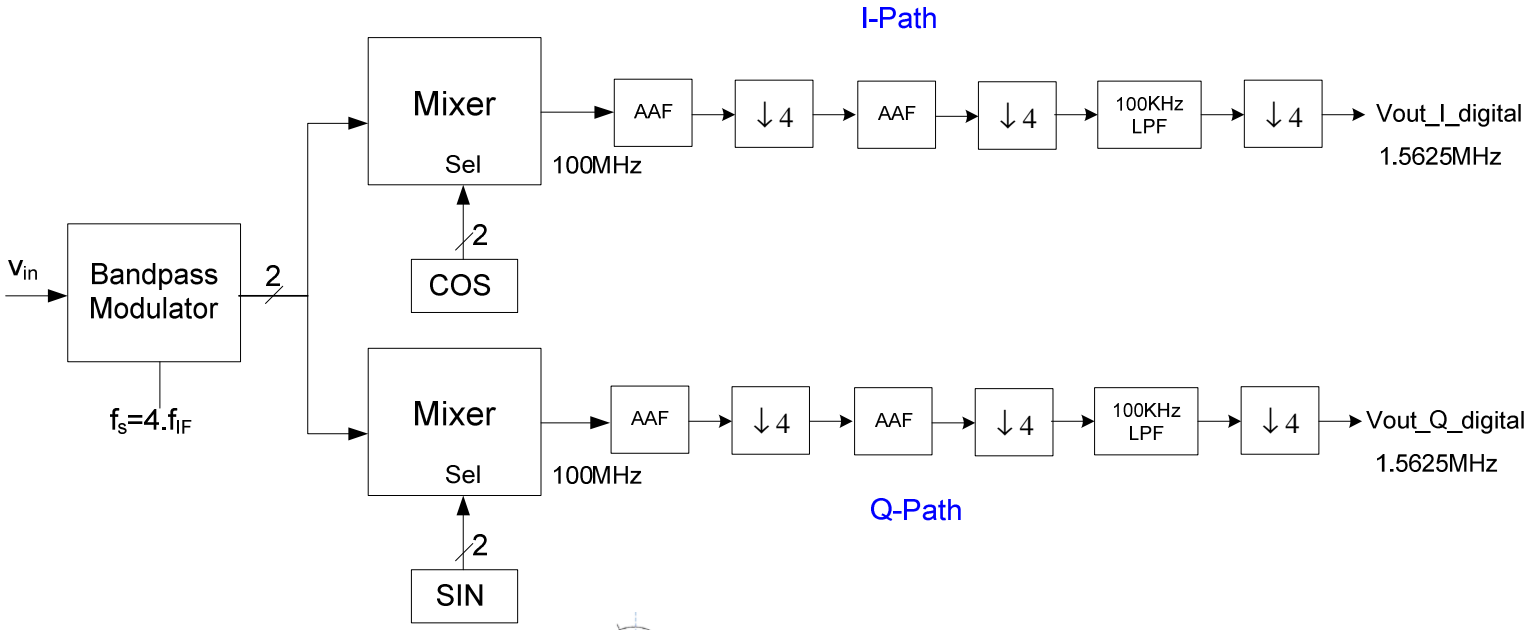
Showing the Signal in the Baseband

- Seen below is a close up view of the *I* output component seen on the previous slide
- Note that the digital data is still moving at full speed!
  - ✓ Still need to decimate (reduce the digital clocking frequency)
  - ✓ Prior to decimating we need to pass the data through digital anti-aliasing filters
    - o It's important for low power operation to keep things as simple as possible



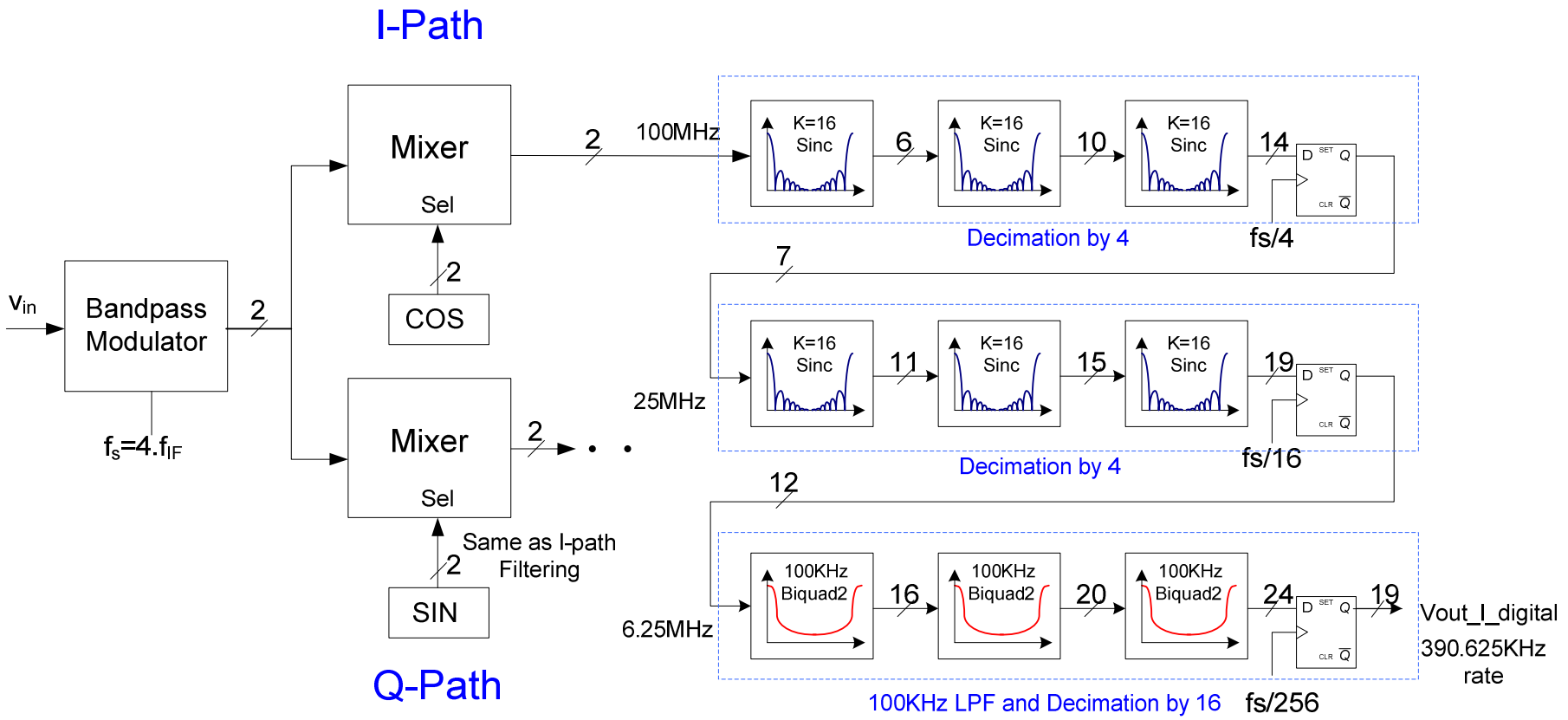
Decimation and Low-pass Filtering

- A straightforward approach to decimation would be to directly use a cascade of biquad low pass filters operating at 100MHz followed by re-sampling at a lower clocking frequency
  - ✓ The cut-off frequency of this LPF will be 100 kHz which leads to a sensitivity (f_0/f_s) of 0.1% which will require very high precision implementation of the biquads (not simple digital coefficients).
- A better approach would be to decimate the mixer output down to a slower clock using simple sinc filters which will relax the precision required for the coefficients of the final biquad LPF
- However we can't be too aggressive on decimation to reduce the data rates as we need to be very careful of aliasing of filtered noise into the baseband. A possible decimation and filtering approach is shown below



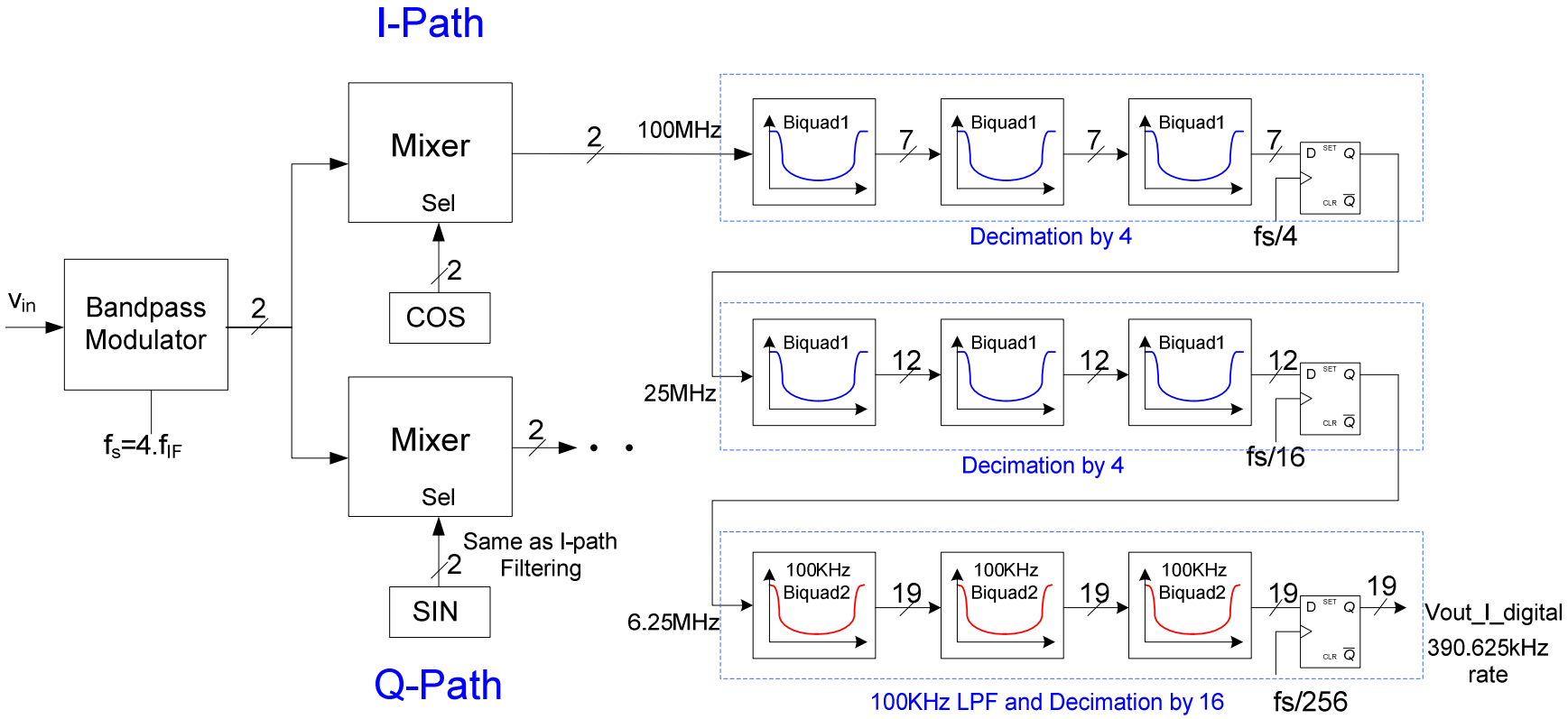
Digital Filtering: One Possibility

- Seen below is a block diagram of the system employing sinc filters as the decimation anti-aliasing filters.



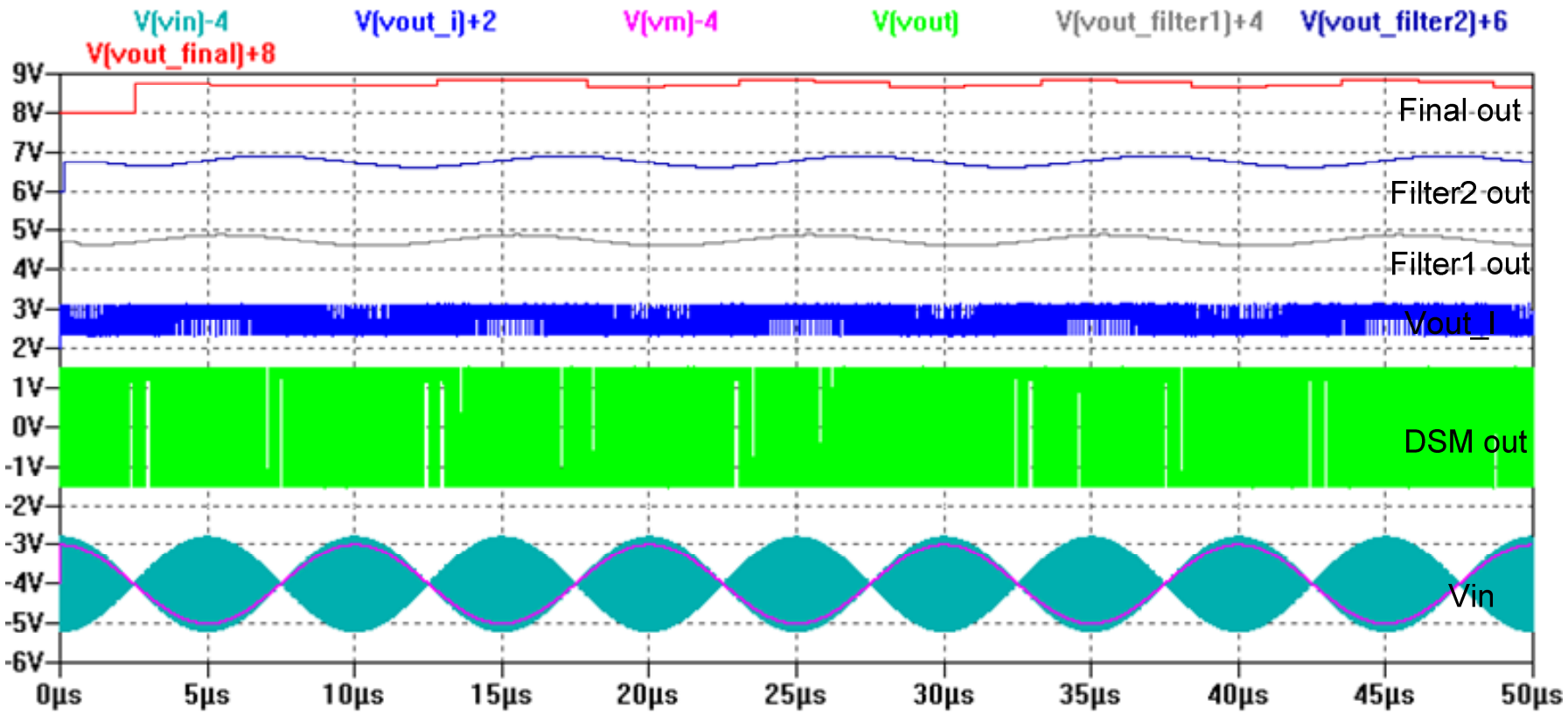
Digital Filtering: Another Possibility

- Using simple, imprecise, biquads earlier in the decimation process reduces hardware and power
  - ✓ Final *SNR* is > 100 dB



Signals at Various Points in the Receiver

- Ideal DACs were used to display the digital filter outputs



Conclusions and Research Directions

- We've talked about the implementation of band pass delta-sigma modulators (BPDSM) for use in heterodyne receivers
- Some common mistakes made when designing BPDSM were presented and discussed
- Concerns for implementing the digital filtering were discussed
- Research directions include:
  - ✓ Low power using passive implementations
    - o Continuous-time circuits using both passive and simple active implementations are clearly of future importance
  - ✓ Parallel paths (> 2) to effectively increase SNR
    - o Reduces the effects of clock jitter
- Of course the digital filtering is important for both power and size