The Baker ADC – An Overview

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- An ADC made using the K-Delta-1-Sigma modulator, invented by R. Jacob Baker in 2008, and a digital filter is called a Baker ADC or Baker data converter.
  - Potential for > 100 GHz sampling in standard sub-100-nm CMOS technologies
  - Uses noise-shaping so precise components are not required
- This talk gives an overview and discussion of the operation and design of the Baker ADC
  - Assumes the audience understands noise-shaping (e.g., delta-sigma) techniques and the operation of data converters
  - Figures taken from CMOS Mixed-Signal Circuit Design, Second Edition, Copyright Wiley-IEEE 2009 (source for the content of this presentation), see: http://cmosedu.com/cmos2/book2.htm
  - Background, theory, and experimental results are presented

Towards High-Speed Data Conversion: Double-Sampling

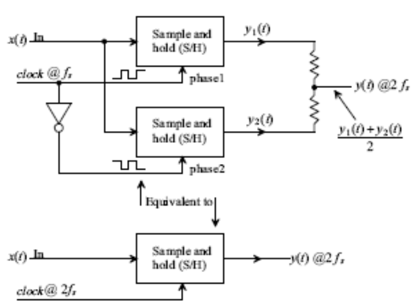


Figure 2.34 Using two S/H paths.

- One simple way to increase sampling rate is to "double-sample"
- Circuits are clocked on the rising and falling edges of a clock
- Simple and widely employed
  - See Ch. 8 covering Bandpass data converters

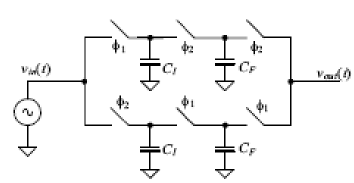


Figure 2.36 Switched-capacitor 2-path lowpass filter.

Limitations of Double-Sampling

- Can't sample any faster than the clock signal
  - 1 GHz clock, 1-ns period, results in clocking at 2 GHz
- In the K-Delta-1-Sigma (KD1S) topology, however, the sampling is determined by the delay between clock edges
  - This delay can be as small as an inverter delay
    - A 10 ps inverter delay results in a 100 GHz sampling rate
  - The number of sampling paths, *K*, is determined by the clock frequency and set by the requirement that each path settle before it's clocked again
  - Design problems are in the digital domain

Double-Sampling, Additional Reading

- H.-K. Yang, E. I. El-Masry, "Double Sampling Delta-Sigma Modulators," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 43, No. 7, pp. 524-529, July 1996
- D. Senderowicz, Germano Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavalle "Low-Voltage ΔΣ Double-Sampled Converters," *IEEE J. Solid-State Circuits*, Vol. 32, No. 12, pp. 1907-1919, Dec. 1997
- P. Rombouts, J. Raman, and L. Weyten, "Approach to Tackle Quantization Noise Folding in Double-Sampling Modulation A/D Converters," *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 50, No. 4, pp. 157-163, April 2003
- G. Ahn, D. Chang, M. Brown, N. Ozaki, H. Youra, K. Yamamura, K. Hamashita, K. Takasuka, G. Temes, and U. Moon, "A 0.6V 82-dB delta-sigma audio ADC using switched-RC integrators," *IEEE J. Solid-State Circuits*, pp. 2398-2407, Dec. 2005
- M. G. Kim, G.-C. Ahn, P. K. Hanumolu, S.-H. Lee, S.-H. Kim, S.-B. You, J.-W. Kim, G. C. Temes, and U.-K. Moon, "A 0.9V 92-dB Double-Sampled Switched-RC Delta-Sigma Audio ADC," *IEEE J. Solid-State Circuits*, Vol. 43, No. 5, pp. 1195-1206, May 2008

Using K-Paths (Poly-phase, or Multi-Rate Signal Processing)

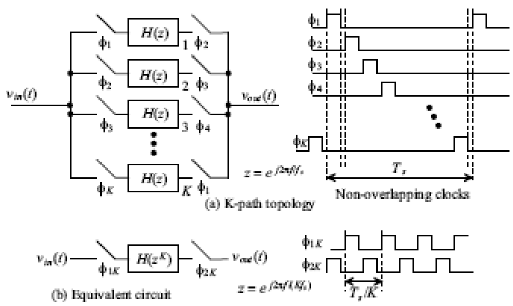


Figure 2.37 A K-path topology and its equivalent circuit.

- Replicates a system for time-interleaved operation.
- Changes z^{-1} to z^{-K}
- Output signal changes at Kf_s rate
- Practical problems
  - Analog paths have to settle in T_s/K
  - If this is possible why not use a single path clocked at the faster rate (or better yet use double sampling)?

Using K-Paths with Delta-Sigma Modulators (DSM), Time-Interleaved DSM

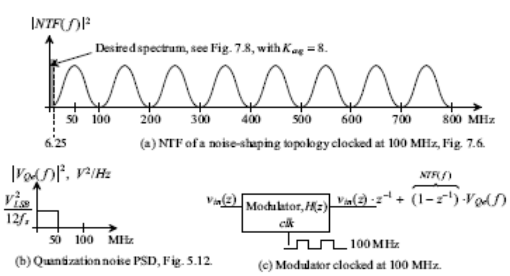
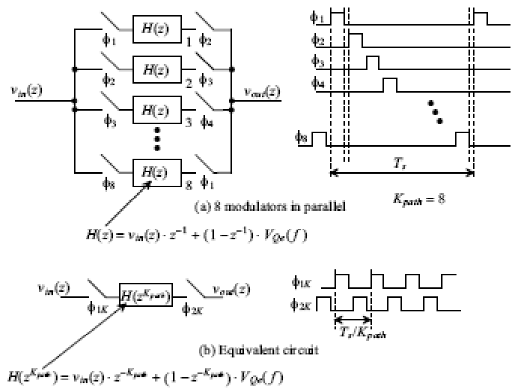


Figure 9.19 NTF and quantization noise spectrums of a first-order NS modulator clocked at 100 MHz with $K_{osr} = 8$.

- To the left is a single path DSM showing the output modulation noise
- What happens when we put K of these in parallel?

Using *K*-Paths with Delta-Sigma Modulators, Time-Interleaved DSM, Continued.



- At first glance we might think this will result in high-speed data conversion
- Large area

Using *K*-Paths with Delta-Sigma Modulators, Time-Interleaved DSM, Continued.

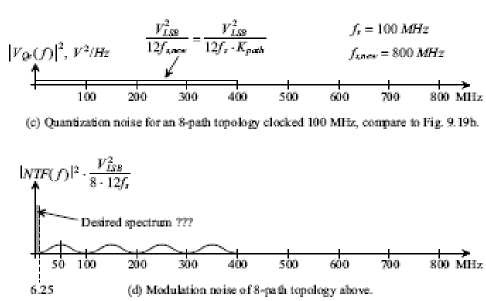


Figure 9.20 Eight modulators in parallel (a time-interleaved topology).

- Using *K*-paths of DSM won't lead to a high-speed topology

- Using *K*-paths spreads the quantization noise out over a wider frequency range
- Doesn't further shape the noise, that is, it doesn't move the modulation noise to a portion of the spectrum where it can be removed with a digital filter
- Note how noise is reduced in the low frequency spectrum
  - For every doubling in *K* we get 3 dB increase in SNR

Time-Interleaved Delta-Sigma, Additional Reading

- R. Schreier, G. C. Temes, A. G. Yesilyurt, Z. X. Zhang, Z. Czarnul and A. Hairapetian, “Multibit Bandpass Delta-Sigma Modulators using N-path Structures,” *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 593-596, May 10-13 1992
- I. Galton and H. T. Jensen, “Oversampling Parallel Delta-Sigma Modulator A/D Conversion,” *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 43, No. 12, pp. 801-810, Dec. 1996
- R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, “Time-Interleaved Oversampling A/D Converters: Theory and Practice,” *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 45, No. 8, pp. 634-645, August 1997
- E. T. King, A. Eshraghi, Ian Galton, and Terri S. Fiez, “A Nyquist-Rate Delta–Sigma A/D Converter,” *IEEE J. Solid-State Circuits*, Vol. 33, No. 1, pp. 45-52, Jan. 1998
- M. Kozak, and I. Kale, “Novel Topologies for Time-Interleaved Delta–Sigma Modulators,” *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 47, No. 7, pp. 639-654, July 2000
- V.-T. Nguyen, P. Loumeau, and J. F. Naviner, “Advantages of High-Pass DS Modulators in Interleaved DS Analog-to-Digital Converter,” *Proceedings of the 45th Mid-West Symposium on Circuits and Systems*, August 4-7, Tulsa, OK, pp. I-136-I-139, 2002
- A. Eshraghi and T. S. Fiez, “A Time-Interleaved Parallel DS A/D Converter,” *IEEE Trans. on Circuits and Systems - II: Analog and Digital Signal Processing*, Vol. 50, No. 3, pp. 118-129, March 2003
- A. Eshraghi and T. S. Fiez, “A Comparative Analysis of Parallel Delta–Sigma ADC Architectures,” *IEEE Trans. on Circuits and Systems - I: Regular Papers*, Vol. 51, No. 3, pp. 450-458, March 2004
- F. Borghetti, C.D. Fiore, P. Malcovati, and F. Maloberti, “Synthesis of the Noise Transfer Function in N-path Sigma-Delta Modulators,” *5th IEE International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, Limerick, Ireland, pp. 171-176, July 25-27, 2005.

Moving Towards the K-Delta-1-Sigma (KD1S) Modulator

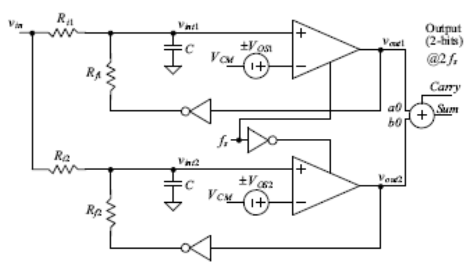


Figure 6.23 Two-path, time-interleaved, passive modulator with mismatch and offsets.

- Consider putting two passive DSMs in parallel (double-sampling)
- Practical problem is the path mismatch
- What happens if we share the integrator?
- Note how the output bits are combined forming a filter, we’ll call the path filter

$$H(z) = 1 + z^{-1} = \frac{1 - z^{-2}}{1 - z^{-1}}$$

- Sampling frequency is $2f_s$

Simple KD1S Modulator Topology

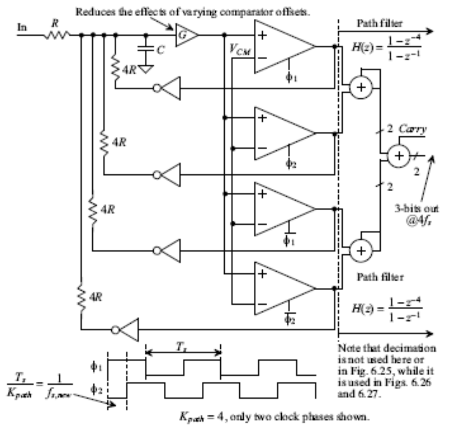


Figure 6.24 Four-path passive modulator. No longer time-interleaved since the integrator is common to all feedback paths (we'll call this the K-Delta-1-Sigma topology).

- Sampling frequency is 4*fs*

- We get high-speed sampling by using *K* feedback paths (*K*-Deltas)
- Quantization noise is pushed to a high frequency by using 1 integrator (1-Sigma)
- While a passive integrator is used here we get better performance using an active integrator
- Bandpass conversion can be accomplished by replacing the integrator with a resonator (e.g. an LC tank)
- Note how well this works for high-speed conversion if R is 50 ohms
- Also note the lack of precise analog components, and the possibility for very low power operation

Simple Baker ADC

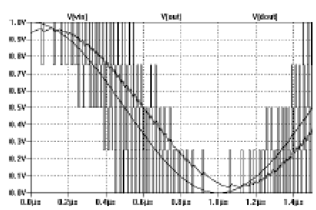


Figure 6.25 Simulating the operation of the 4-path modulator in Fig. 6.24.

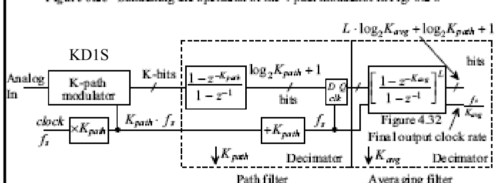


Figure 6.26 Performing decimation on the output of the modulator.

- If the KD1S topology is ideal it behaves, when using a single integrator, like a first-order modulator clocked at Kf_s
  - The built-in instability is a concern (more later)
- Theory developed for first-order modulator can be used to determine SNR, bandwidth, etc.
- Further research includes looking at passive second-order modulators, using current feedback DACs, design of fast comparators (more on this later), bandpass topologies, etc.
- Note also that filters can be implemented using these techniques (many, many research ideas)

Design Example from Ch. 9

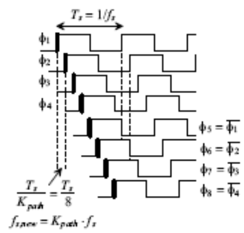


Figure 9.1 Showing the clock signals used for time-interleaved sampling and the high-speed topologies discussed in this chapter.

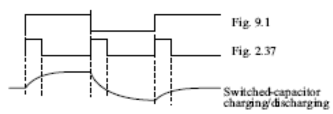


Figure 9.2 Charging discharging a switched-capacitor.

- Effective sampling rate is set by the spacing between edges of clock signals
- Path settling must be within in T_s
- Note that while the path settling time can be slow (T_s) the input signal must still be sampled at T_s/K (for switched-capacitors) or filtered using the RC seen in slide 11 (50 ohm R and 1 pF C form a circuit with a time constant of 50 ps)
- There is a built-in instability which must be controlled by minimizing the forward and feedback delays
  - Oscillations removed with the digital filter

Path Filtering and Decimation

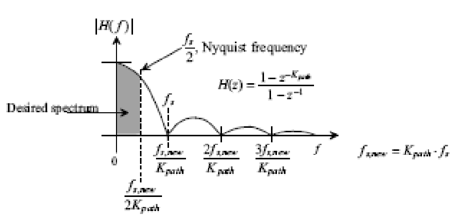


Figure 9.3 Frequency response of the summing circuit (path filter) seen in Fig. 9.4.

- Adding the K outputs together and clocking out at f_s results in a response that is exactly like a Sample-and-Hold clocked at f_s
- Avoiding decimation, discussed in the book, can be used for higher-speed operation
- For the experimental results presented later, with 8 paths, the filter output is then 0000 (all path outputs are 0s) to 1000 (decimal 8 where all outputs are high)

Switched-Capacitor KD1S

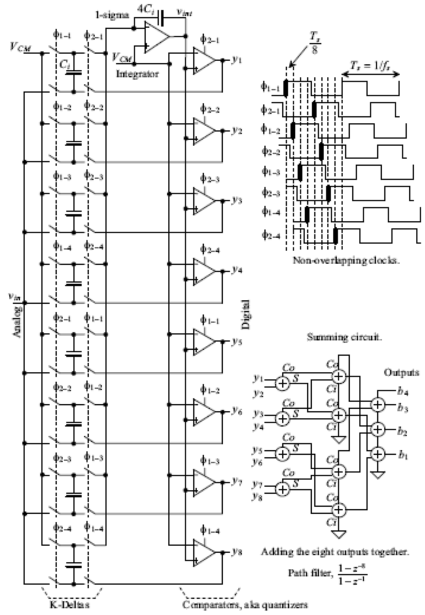
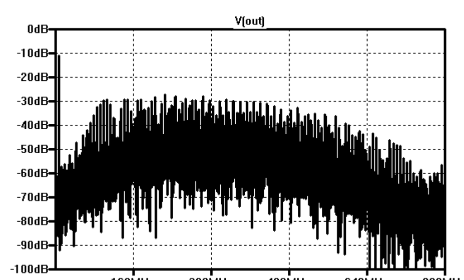


Figure 9.4 A topology for high-speed data conversion using mixed-signal techniques, the K-delta-1-sigma topology.

Showing Modulation Noise Spectrum of the KD1S with K = 8 and clocked at 100 MHz



- Again the KD1S has an effective sampling rate of 800 MHz even though the clock frequency is 100 MHz since 8 paths are used
- Spectrum shown at the left is the output of the KD1S if the outputs are sequentially fed to a 1-bit output at the 800 MHz rate, no Path filter
- Verifies the topology behaves like a first-order delta-sigma with a clock frequency of 800 MHz
- Since effectively a first-order topology we need two Sinc filters (path filter and one more). If K=8 then the conversion BW is 50 MHz and the output resolution is 7-bits (roughly 42 dB SNR)

Example Filter and Output

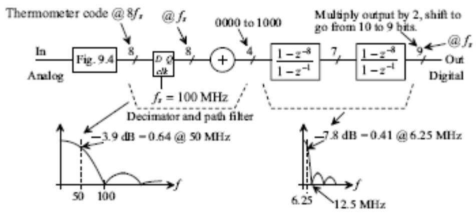


Figure 9.10 Decimating and filtering the output of the K-path modulator, an approach that won't work for Nyquist-rate conversion.

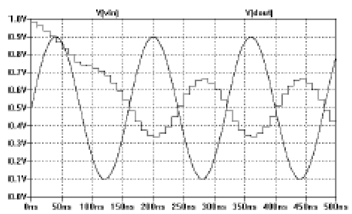


Figure 9.11 Simulating Fig. 9.10 with a 6.25 MHz input signal.

- The KD1S has an effective sampling rate of 800 MHz even though the clock frequency is 100 MHz since 8 paths are used
- As discussed in the book the early-stage decimation limits the conversion bandwidth using simple moving-average filters

Built-In Instability

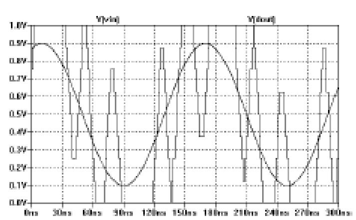
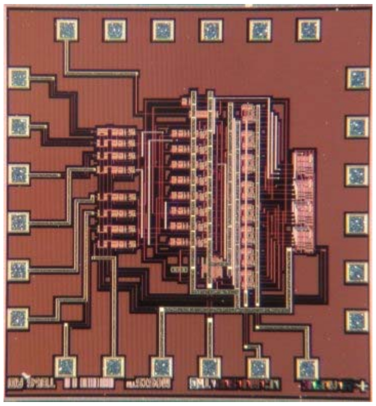


Figure 9.22 Showing built-in instability with a sinewave input signal.

- The delay through the comparator and integrator feedback to the input results in a built-in instability
  - Always at a multiple of the clock frequency so it is removed with the digital filter
  - Can result in integrator saturation if not careful
  - Limits the use of higher-order topologies
- Qualitatively the instability comes from the information always trying to "keep-up" with the input signal.

Test Chip Results (See Design Details in Sec. 9.2)



- The data converter designed using a 500 nm process in Sec. 9.2 was fabricated
  - Large part of the chip photo at the left is output buffers since the KD1S topology is so simple
  - Used Matlab for the filtering
  - 8 outputs where latched with one clock so the output was decimated from 800 MHz down to 100 MHz (see slide 17)
- Design behaved just like predicted in the book
- Again, 800 MHz sampling in 500 nm CMOS!

Design Example Continued - Clock Generation

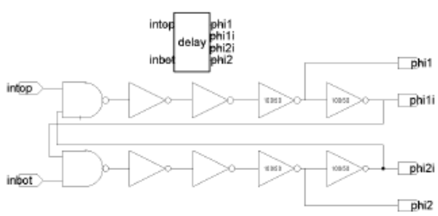


Figure 9.23 Delay stage used in the ring oscillator, schematic and icon.

- Schematic simulations without parasitics showed an oscillation frequency of 1600 MHz
- Experimental results resulted in a clock frequency of 800 MHz
- Used asynchronous internal clock

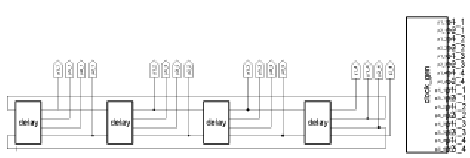


Figure 9.24 Ring oscillator, schematic and icon, for use with the data converter.

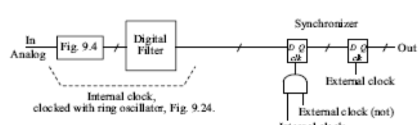


Figure 9.26 Synchronizing the external and internal clock signals.

Design Example Continued – Building Blocks

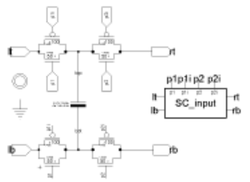


Figure 9.27 Schematic and icon of the switched-capacitors used in the modulator.

- Used 100 fF capacitors
  - Thermal noise is set by *K* times C and then further reduced by the oversampling factor
- Need fast comparator and integrator for most ideal behavior

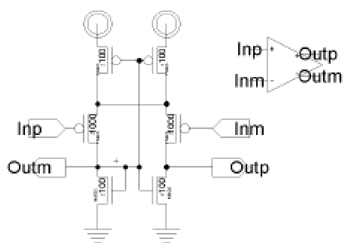


Figure 9.28 Self-biased amplifier and icon.

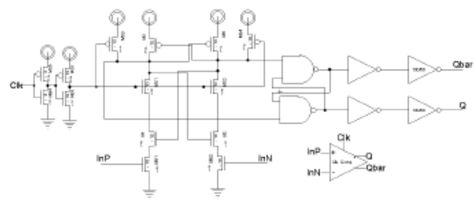


Figure 9.30 Clocked comparator and icon.

Design Example Continued – Final Schematic

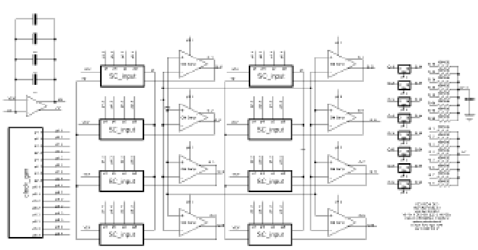


Figure 9.32 K-delta-1-sigma modulator.

- The resistors seen are a simple way to plot digital data (by summing the data into an analog signal) in SPICE but they are not used in the chip.
- Latches re-sample digital data at 100 MHz (decimate) as seen below

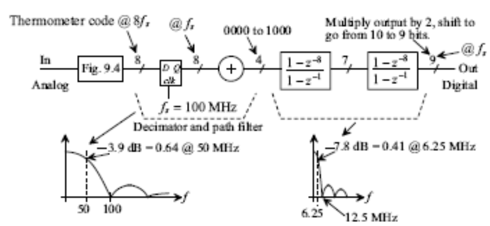
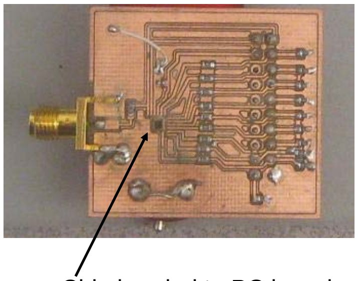
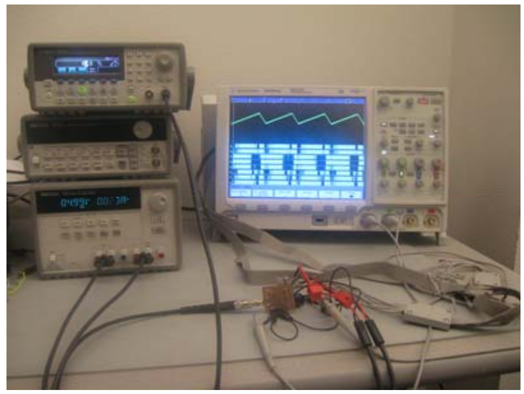


Figure 9.10 Decimating and filtering the output of the K-path modulator, an approach that won't work for Nyquist-rate conversion.

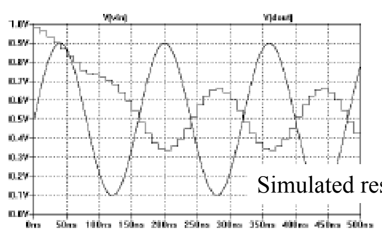
Design Example Continued – Harvesting Data

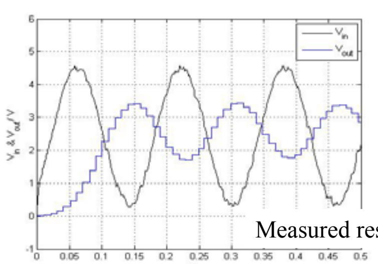


- The bare die was bonded to PC board to minimize the parasitics
- Agilent MSO7104A used to capture analog input and digital outputs



Design Example Continued – Data Results

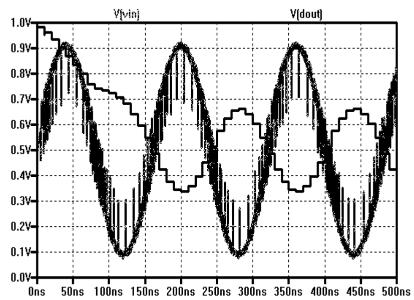




Also with a 6.25 MHz input that is swinging from 0 to VDD

- The simulation example in Figure 9.11, seen at the left, was generated using ideal components with a VDD of 1 V.
- The data seen below this is the experimentally measured output of our data converter designed in a half-micron process with a VDD of 5 V.
  - Since the design is basically digital it's predictable
  - Note the start-up transient is the delay through the digital filter
  - Small differences are due to the sampling frequencies being different between the two sets of data

Design Example Continued – Data Results



- Notice how the measured input signal on the previous slide looked noisy
- Simulations were generated with an ideal input voltage
- In the test setup our input voltage source is supplied through a co-axial cable so the source has a 50 ohm output resistance
- The figure seen at the left is the result of regenerating Fig. 9.11 with a 50 source resistance
- When we place the scope probe, around 15 pF loading, to measure the signal we get a waveform that appears to be noisy as seen on the previous slide
- Continuous-time designs don't have this clock feed through noise

Design Example Continued – Data Results

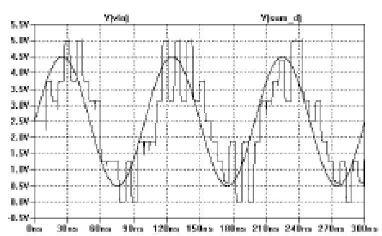
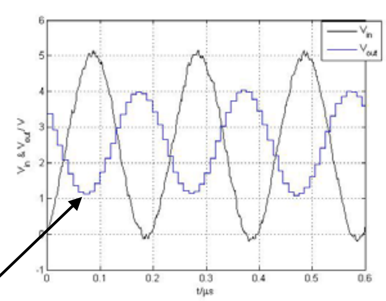
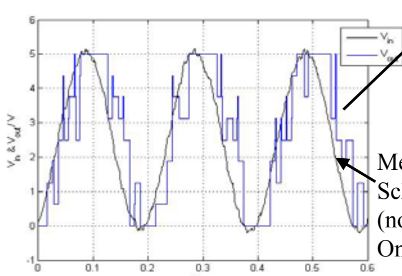


Figure 9.33 Simulating the ADC in Fig. 9.32 with a 10 MHz input signal.



Measured data with a 5 MHz input after two more Sinc filters, Fig. 9.10 (slide 22)



Measured data with a 5 MHz input.
Schematic simulations in Ch. 9 showed a 1.6 GHz clock (no parasitics) while actual silicon gave 800 MHz.
Only the path filter is applied to the data (see slide 22).

Design Example Continued – Data Results

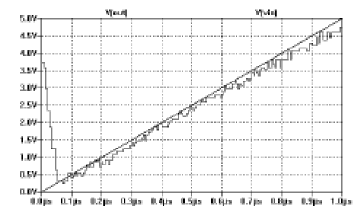
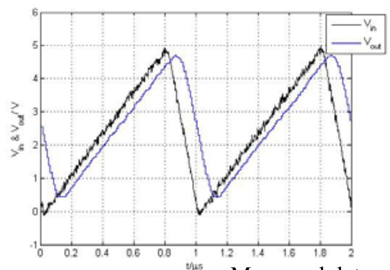


Figure 9.35 Simulating the modulator with a ramp input signal. Shift input later in time by 50 ns to compare to output.



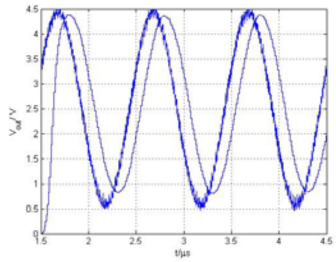
Measured data, rail-to-rail ramp input

- Large signal behavior, note compression close to the power supply rails
- Looking at time-domain data is useful but frequency domain data, as discussed in Ch. 5, can be much more telling about the performance of the converter
- Using ideal components what SNR should we expect using the filter seen in Fig. 9.10 on slide 22?
- Ideally the KD1S modulator behaves like a first-order modulator (continued on the next slide)

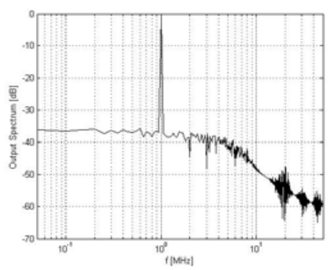
Design Example Continued – Data Results

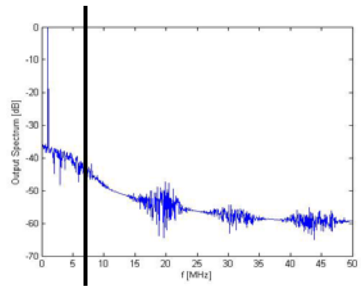
- The output of the KD1S modulator and path filter ranges from 0 (0000) to 8 (1000) or essentially 3-bits
- If we pass this output through two Sinc filters with *K* = 8 we expect the resolution to go up by 3-bits in each filter for a total output word size, as seen in Fig. 9.10 on slide 22, of 9-bits (oversampling of 64, going from 800 MHz to 12.5 MHz).
- Ideally then our SNR is roughly 54 dB
- Conversion bandwidth limited by the decimation of 800 MHz down to 100 MHz in the path filter, is 6.25 MHz
  - Without decimation and *K* = 8 the conversion bandwidth is 50 MHz with a final output clock frequency of 800 MHz (again this is a half-micron process!) and an output word size of 6-bits (SNR of 36 dB)

Design Example Continued – Data Results



- Normalized spectrums (log-log and log-linear) of the data converter's time-domain output (left) with a 1 MHz input tone (also left) are seen below
- Doesn't remove the start-up transient's influence on the spectrums
- Detailed results will be published in a journal paper





The Baker ADC: Comments and Conclusions

- We've discussed:
  - How a K-Delta-1-Sigma modulator uses time-interleaved sampling (K-Delta or K-feedback paths) for high speed sampling
  - How a K-Delta-1-Sigma modulator uses a single integrator (1-Sigma) to push the quantization noise to higher frequencies (shape the noise)
- Experimental results verified the design presented in Ch. 9 of CMOS Mixed-Signal Circuit Design, Second Edition
  - Design of an ADC in a 500 nm process with a sampling frequency of 800 MHz
- A likely topology for high-speed data conversion in nanometer CMOS technology nodes
  - Rich area for research and development
  - Uses in products ranging from ultra-wideband radar to mm-wave signal processing

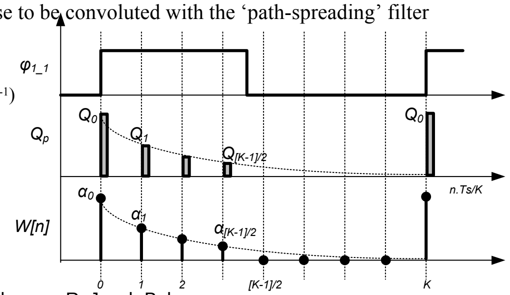
Integrator Speed Requirements for KD1S

- The unity gain frequency (f_{un}) of the shared integrator in the KD1S topology can be as low as f_S.
  - A true first-order DSM operating at K*fs will need integrator f_{un} equal to at least K*fs (67% settling).
  - Integrator is allowed to settle in Ts/2 time by spreading the differential-charge ($=C_I(v_{in}[n]-v_{out}[n-1])$) over K/2 paths.
- The charge spreading is described as:

  $\alpha_p=(C_I/C_F).\Delta V.\alpha_0^p(1-\alpha_0)$, p=0,….,[K/2]-1, where $\alpha_0=e^{-\beta.fun/K.fs}$
  - Charge $C_I\Delta V.\alpha_{(p1-p2)mod\ K}$ is injected from path p_1 to path p_2 during the operation of the integrator.
  - The leads to the integrator's response to be convoluted with the 'path-spreading' filter

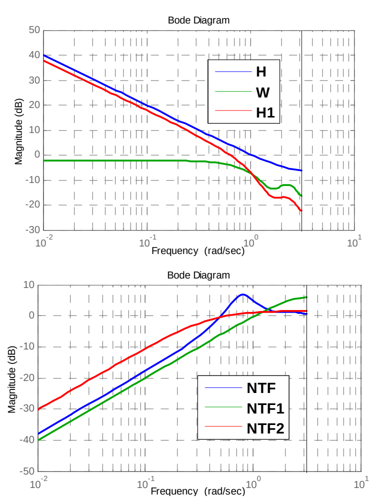
    $W(z)=\sum_{n=0\ to\ [K/2]-1}\alpha_n z^{-n}$
  - The integrator's response is now

    $H1(z)=W(z)H(z)$, where $H(z)=z^{-1}/(1+z^{-1})$



- NTF(z)=1/(1+W(z).H(z))
- STF(z)=W(z).H(z)/(1+W(z).H(z))

Noise Shaping with KD1S



- The transfer function of $H_1(z)$ looks close to an integrators response.
  - W(z) acts like a LPF shaping integrator's response.
- The Noise shaping response, NTF(z), is also close to the ideal NTF for a true first order DSM (NTF1 here for β=1, $f_{un}=f_s$).
  - 10dB loss (1.37 bits) if the slow integrator ($f_{un}=f_s$) is clocked for $T_{s,new}/K$ time (NTF2 here). Similar to the double-sampling case.
- Only 2dB more in-band noise (0.04 bits less) in KD1S, as opposed to 10dB for NTF2.
- Analyze carefully for stability with higher noise magnitude in KD1S.
  - Poles are within the unit circle.
- Noise shaping is very close to an ideal first-order DSM with a slow integrator operation at the clock speed!
  - The design effectively runs at the comparator speed.
  - Multi-GHz's of sampling speed possible!!