Delta-Sigma Modulation For Sensing

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Abstract – This talk will give an overview of the use of Delta-Sigma modulation (DSM) for sensing. This robust technique can be used to improve the signal-to-noise ratio in CMOS integrated sensing circuits. Example applications of DSM will be discussed in the areas of resistive and flash memory, and in CMOS image sensors. The talk will conclude with a discussion of practical circuit design techniques to implement DSM sensing circuits.

Talk Outline

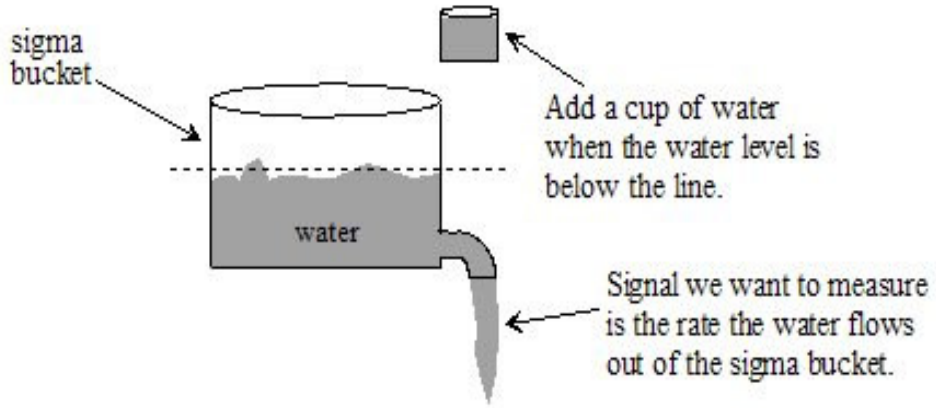
- Introduction to DSM Technique
  - ✓ Precise sensing of a signal corrupted with noise
  - ✓ Qualitative explanation
  - ✓ Resolution and Precision
- DSM for sensing in Flash Memory
  - ✓ DSM to sense the state of the cell
- Sensing Resistive Memory

Talk Outline (cont'd)

- Sensing in CMOS imagers
  - ✓ Qualitative explanation
  - ✓ Sampling reference and intensity
  - ✓ Offset, noise
  - ✓ Sense Amplifier Design
  - ✓ Problems: clock feed through, kickback noise
- Conclusions
- Ongoing research

Using a bucket-water analogy to illustrate DSM

- A robust sensing scheme using simple signal processing (averaging) for measuring an analog quantity.
- Averaging can be thought of as reducing the noise in the signal (the variations in water level because of sloshing).
- Averaging how often we add the cup of water gives a digital representation of the signal we are trying to measure.



Qualitative Explanation

- The size of the cup that adds water is important.
  - ✓ Using too small of a cup results in the water draining out of the bucket. (We can't add the water fast enough).
  - ✓ Using a small cup for adding water increases the resolution.
- As long as the water level is at a constant value the actual level is unimportant (offset doesn't matter).
- If the sigma bucket is "leaky" and the water it holds leaks out the quality of the sense will be affected.
- What limits the resolution of this scheme? 1) A leaky bucket, and 2) filling the cup imperfectly.

Qualitative Example

- Example: Assume that the rate of water flowing into the sigma bucket, is 1 cup every 40 seconds. (0.25 cups per 10 seconds).We remove a cup of water from the bucket every time the water level is > 5 cups
  - ✓ Say that the height of the water in the bucket is checked every 10 seconds. We can write (assuming we want to keep, water height at 5 cups our reference line):

Time (secs)	Water level in sigma bucket (cups).	Remove cup? (Water level >5)	Average # cups
0	5	No, don't remove	0
10	5.25	Yes	1
20	4.5	No	0.5
30	4.75	No	0.33
40	5	No	0.25
50	5.25	Yes	0.4
60	4.5	No	0.33
70	4.75	No	0.29

Qualitative Example (cont'd)

- Continuing, we can write:

Time (secs)	Water level in sigma bucket (cups).	Remove cup? (Water level >5)	Average # cups
80	5	No	0.25
90	5.25	Yes	0.33
100	4.5	No	0.3
110	4.75	No	0.27
120	5	No	0.25
130	5.25	Yes	0.31
140	4.5	No	0.29
150	4.75	No	0.26
160	5	No	0.25

Qualitative Example

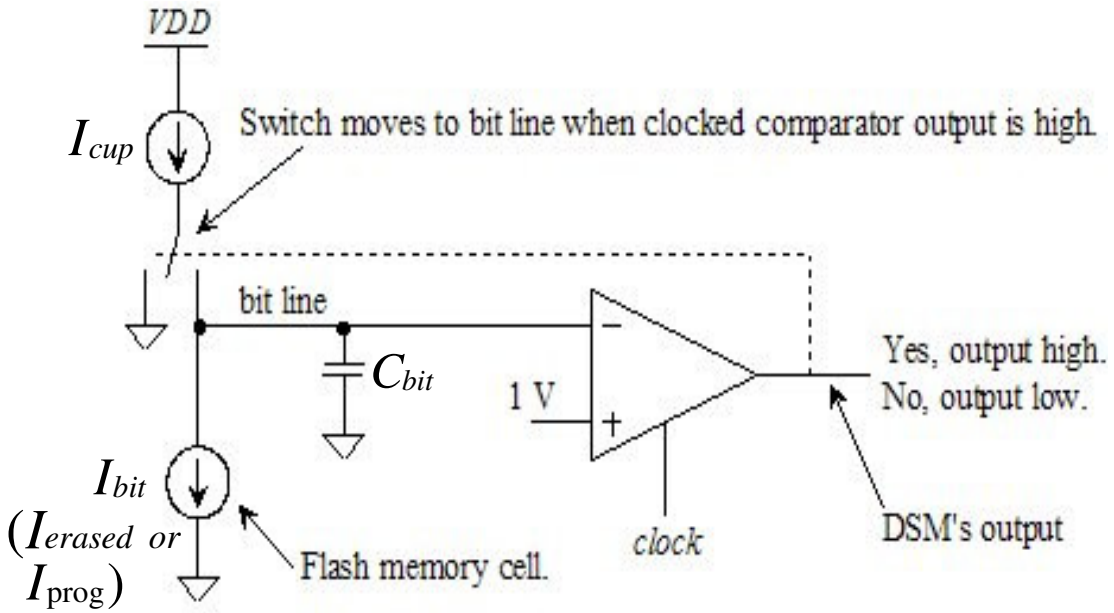
- Note how, as we increase the number of samples, the average bounces around 0.25 cups/10 seconds.
  - ✓ The longer we average the closer the output converges on 0.25 .
- The input signal is the product of the output number (average) and the feedback signal size (cup size) or here 0.25*10 .
- Note that if we make a wrong decision it doesn't really matter.
  - ✓ If we do not determine the level of water correctly it really doesn't matter! The error will average out over time.
  - ✓ A counter is used for averaging (count the number of times we remove water from the bucket).

Resolution and Precision

- Again, the resolution is set by the size of the cup we use to remove water from the bucket.
  - ✓ Smaller cup, faster, more accurate sense.
  - ✓ If the cup is too small we can't remove water fast enough from the bucket and it will overfill.
- The precision is set by how accurately we remove the water from the bucket.
  - ✓ Spilling water out of the cup or not filling it up all the way reduces the sensing accuracy.
- The ultimate resolution is determined by how leaky the bucket is.
- Note that the longer we sense the better the sense.

Sensing a Flash Memory using DSM

- State of the flash cell *erased* or *programmed* can be determined precisely by DSM.
- Comparator makes a decision based on the bit line voltage.
- I_{bit} can be determined very precisely by looking at the number of times the output of the DSM sensing circuit goes high.
- DSM programs the cell as well as sets the programmed current flow this will allow us to make a memory cell out of a single transistor that can be used to store several logic levels.



C_{bit} = sigma bucket

$I_{bit}(I_{erased}\ or\ I_{prog})$ = the signal we are trying to measure, rate current flows out of the bucket.

Equations

The rate of charge removed from the bit line is

$$\frac{I_{bit}}{C_{bit}} = \frac{\Delta V_{bit}}{T}$$

The amount of charge removed from the bit line in one clock cycle is

$$Q_{bit} = I_{bit} \cdot T = C_{bit} \cdot \Delta V_{bit}$$

The amount of charge we add from I_{cup} is

$$Q_{bit} = I_{bit} \cdot T = C_{bit} \cdot \Delta V_{bit}$$

Equating the amount of charge leaving the bucket (Q_{bit}) and the amount of charge entering the bucket (Q_{cup})

$$Q_{bit} = I_{bit} \cdot T = Q_{cup} = I_{cup} \cdot \frac{M}{N} \cdot T$$

Equations (cont'd)

We get

$$\frac{I_{bit}}{I_{cup}} = \frac{M}{N}$$ which gives the resolution

where

M=Total number of clock cycles.

N=Number of times the output of the comparator goes high.

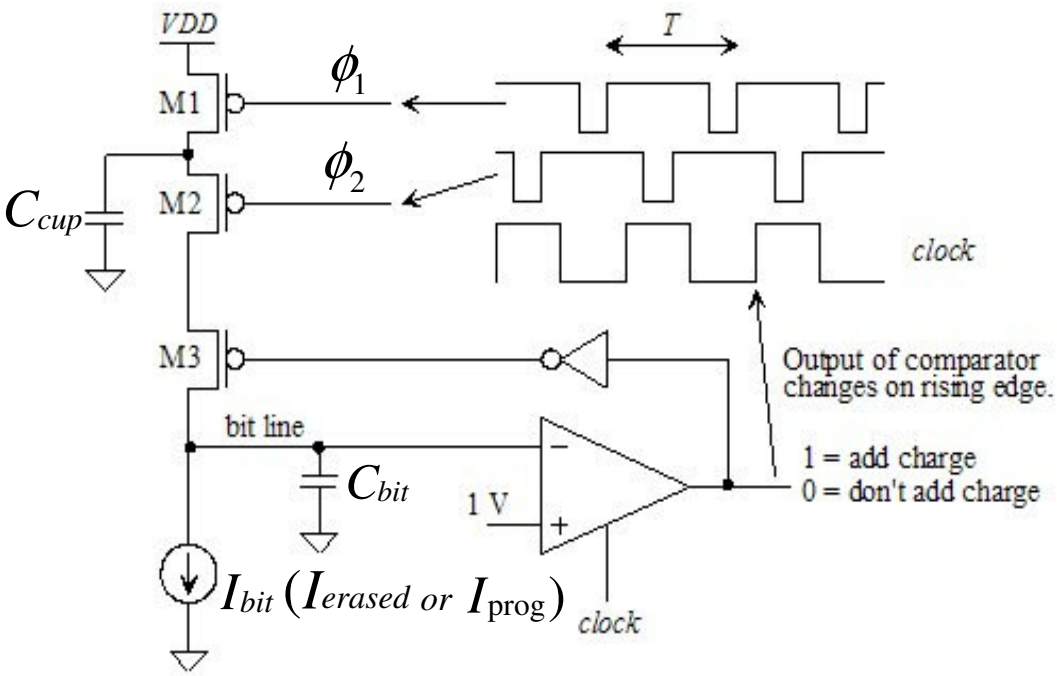
Assuming $I_{cup} \geq I_{bit}$

$$\Delta V_{bit,\max} = \frac{I_{cup} \cdot T}{C_{bit}}$$

where $\Delta V_{bit,\max}$ is the maximum deviation on the bit line.

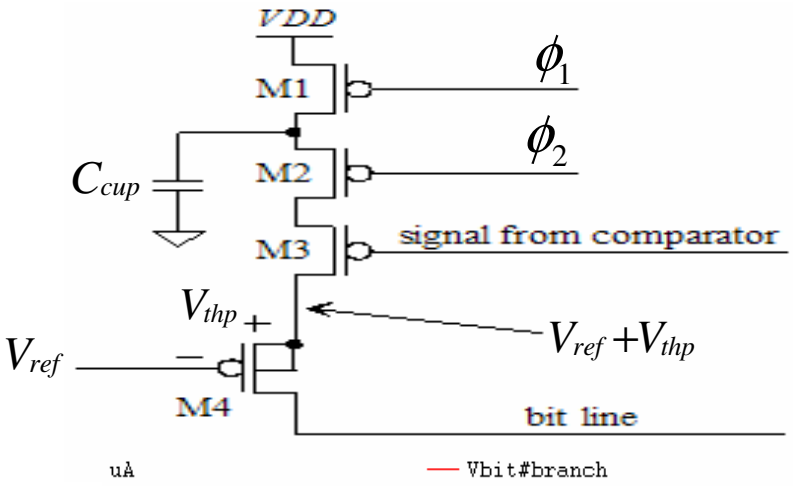
Switched-Capacitor Circuit

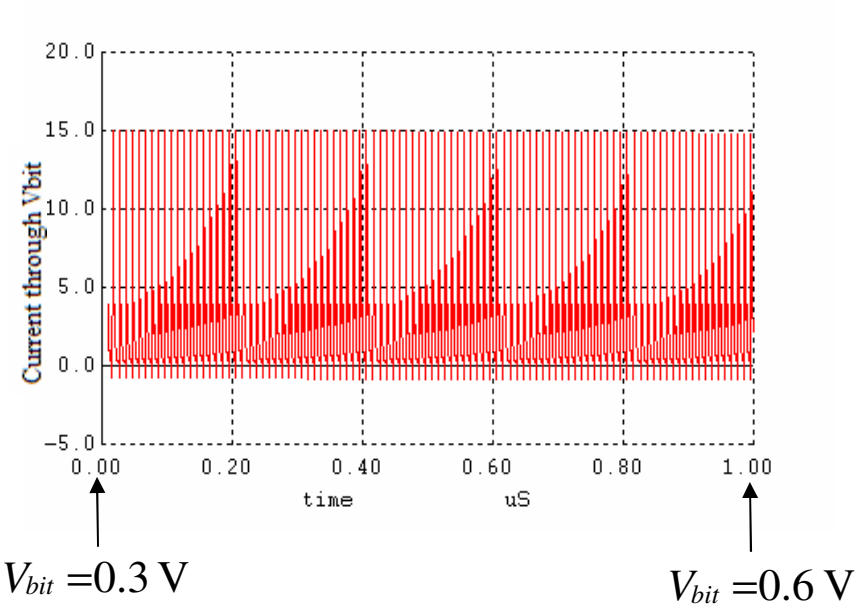
- Parasitic capacitance on the output of the current source limits how precisely the current can be guided in to or out of bit line capacitance.
- A switched capacitor circuit is used to minimize power consumption and the effects of parasitic capacitance.
- ϕ_1 and ϕ_2 are never low at the same time.



Switched-Capacitor Circuit(cont'd)

- With an added PMOS the charge added to bit line is independent of variations in V_{bit} .
- Figure below shows how the charge applied to V_{bit} becomes linear with the added PMOS.
- PMOS is used instead of an NMOS since drain of an NMOS device is a high impedance node and can't be controlled.
- C_{bit} should not be too large as it won't discharge V_{ref}.



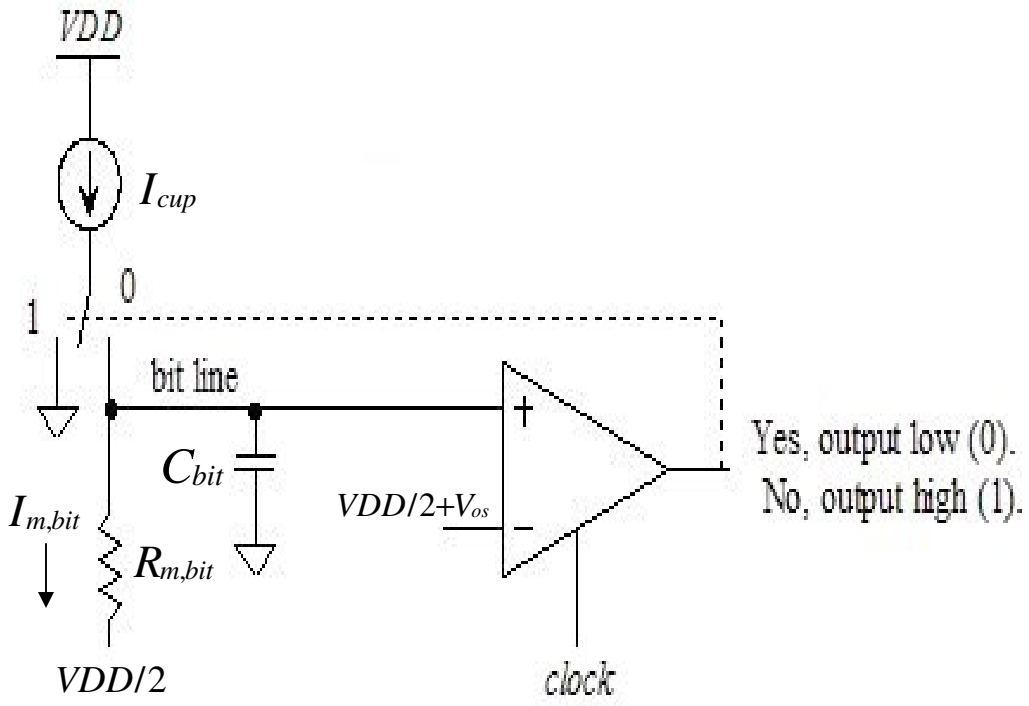


V_{bit} =0.3 V

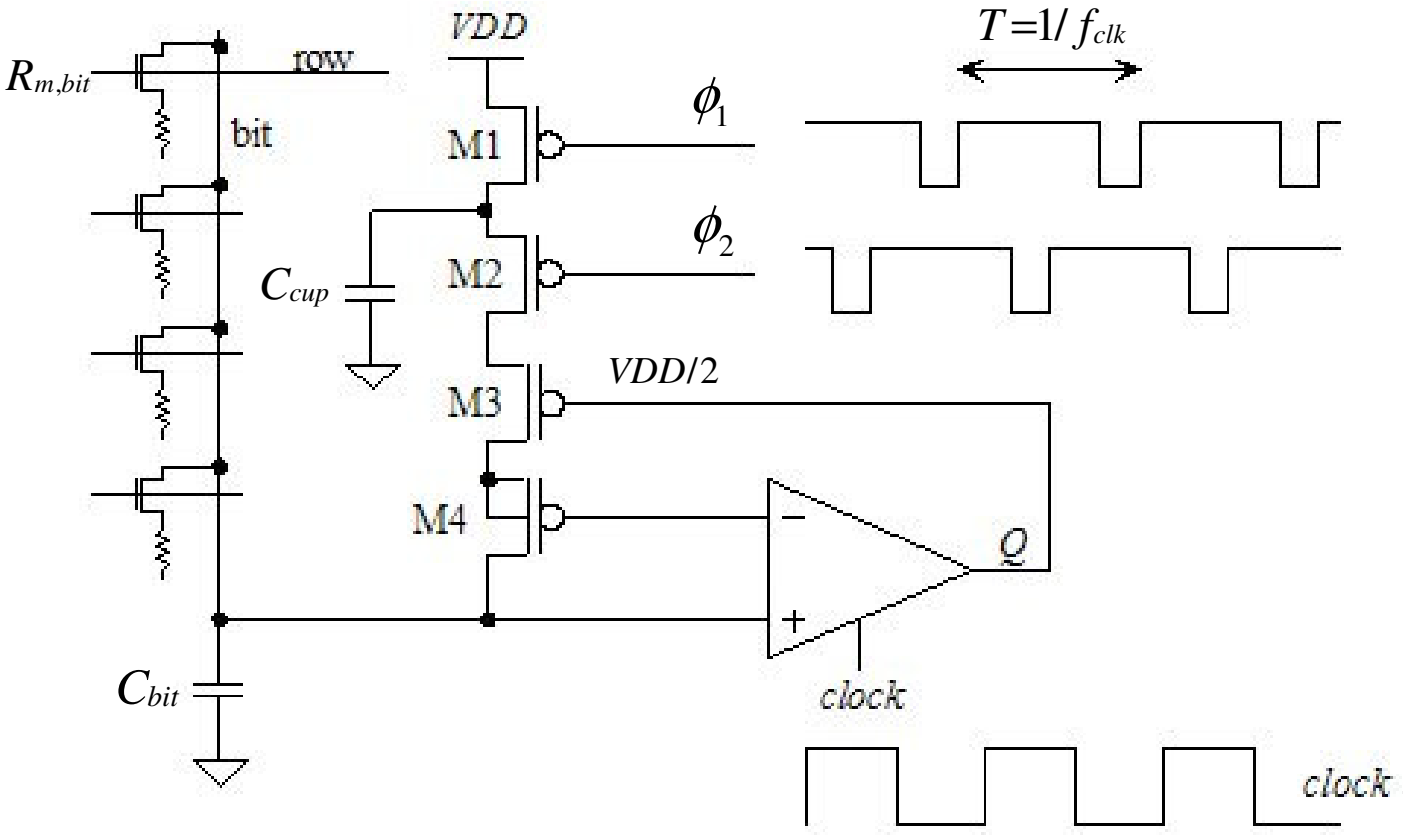
V_{bit} =0.6 V

Sensing Resistive Memory

- *Ideally* the resistor is either zero ohms (the *programmed state*) or infinite (the *erased state*).
- In the *erased state* the output of the DSM is a string of 0's and we need not add charge to the bit line.
- In the *programmed state* bit line is pulled to VDD/2 and the DSM's output is a string of 1's.
- Number of reference voltages in the sense scheme can be reduced by designing the comparator with a built in offset.



DSM Sensing Circuit for Resistive Memories



Equations

Current through the cell is given by

$$I_{m,bit} = \frac{V_{os}}{R_{m,bit}}$$

We can write

$$\frac{V_{os}}{R_{m,bit}} = Q_{cup} \cdot \frac{M}{N} \cdot T = (V_{DD} - V_{DD}/2 - V_{thp}) \cdot C_{cup} \cdot \frac{M}{N} \cdot \frac{1}{T}$$

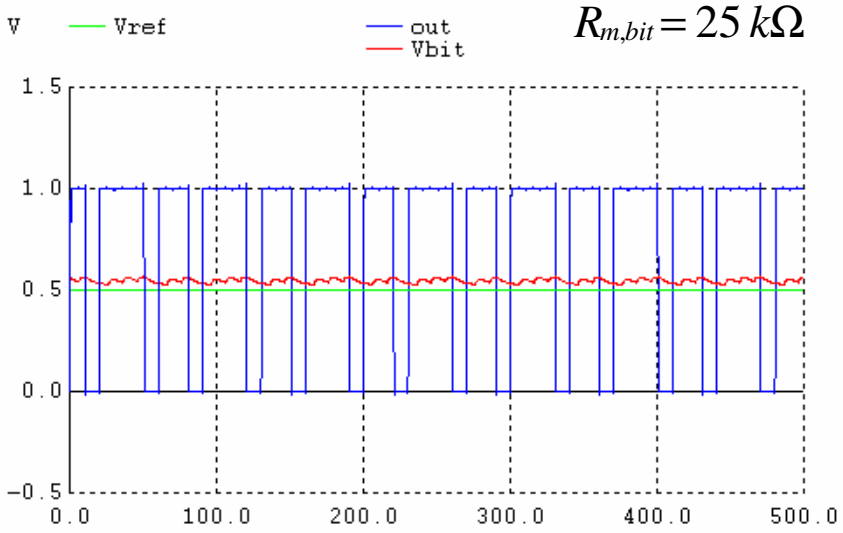
The bit line resistance can be estimated as

$$R_{m,bit} = \frac{V_{os} \cdot T}{(V_{DD}/2 - V_{thp}) \cdot C_{cup} \cdot \frac{M}{N}} \qquad \textit{Equation } 1$$

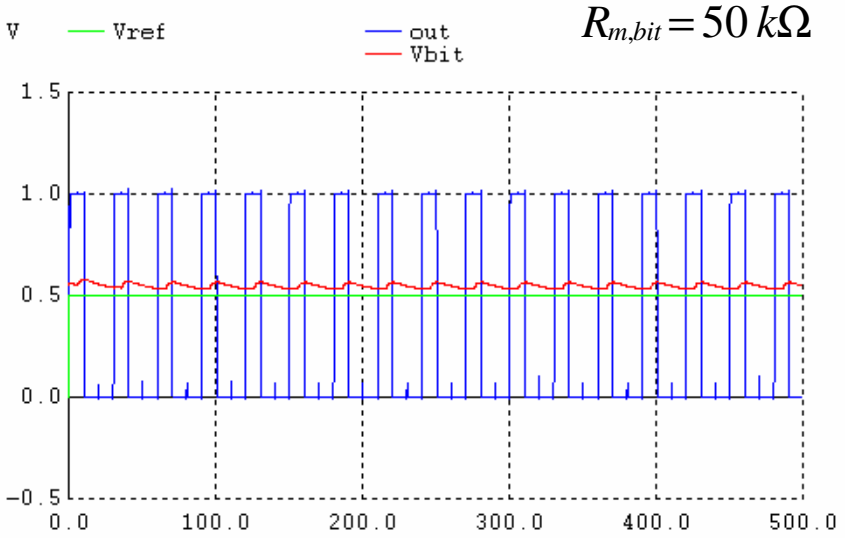
Maximum change in bit line voltage is

$$\Delta V_{bit} = \frac{C_{cup}}{C_{cup} + C_{bit}} \cdot (VDD/2 - V_{thp})$$

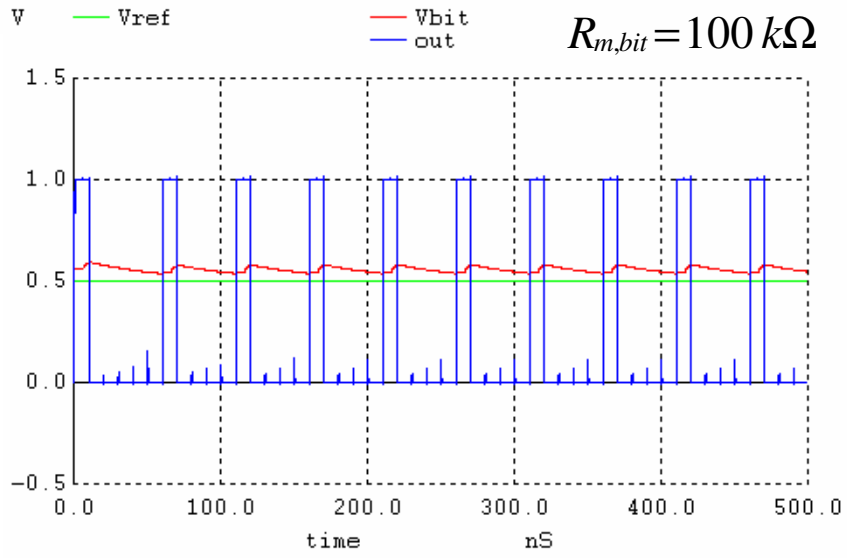
Simulations



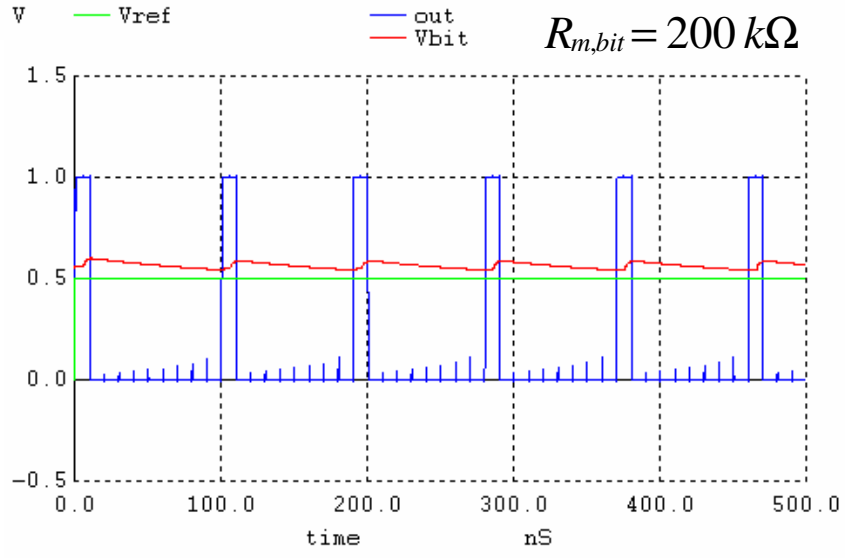
$R_{m,bit} = 25\ k\Omega$



$R_{m,bit} = 50\ k\Omega$



$R_{m,bit} = 100\ k\Omega$



$R_{m,bit} = 200\ k\Omega$

Example

❑ For $V_{os}=50\,mV, C_{cup}=100f,\ V_{DD}=1V, Vthp=280\,mV,\ f_{clk}=100\,MHz$

From Equation 1 we can write

$$R_{m,bit}=25\ k\cdot\frac{N}{M}$$

In (a) $R_{m,bit}=25k$, we get an output of 14 zeroes and 36 ones (=M)

$$R_{m,bit}=25k\cdot\frac{50}{36}=35k$$ (actual value from simulations 25k)

For (b) we see M = 17 so

$$R_{m,bit}=25k\cdot\frac{50}{17}=73k$$ (actual value 50k)

and for (c) and (d)

$$R_{m,bit}=25k\cdot\frac{50}{10}=125k$$ (actual value 100k)

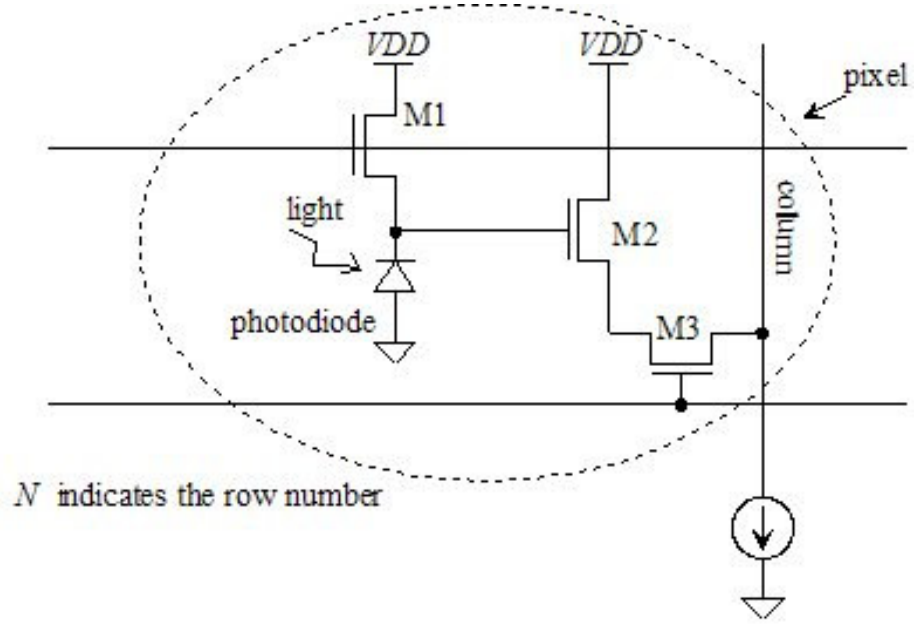
$$R_{m,bit}=25k\cdot\frac{50}{6}=208k$$ (actual value 200k)

Comments

- Simulated values are different from the calculated values due to the incomplete settling time (making C_{cup} smaller than it actually is) and the offset voltage not being precisely 50mV.
  - ✓ By clocking the circuit slower the incomplete settling time problem can be solved.
  - ✓ Generating a precise voltage reference for the comparator could solve the offset voltage problem.
- Noise on VDD/2 feeds evenly into the comparator circuit and doesn't affect the operation.
- We can get a good linearity with resistance values ranging from 25k to 75k.
- Note that we have to sense longer to estimate larger values of resistances.

Sensing in CMOS imagers

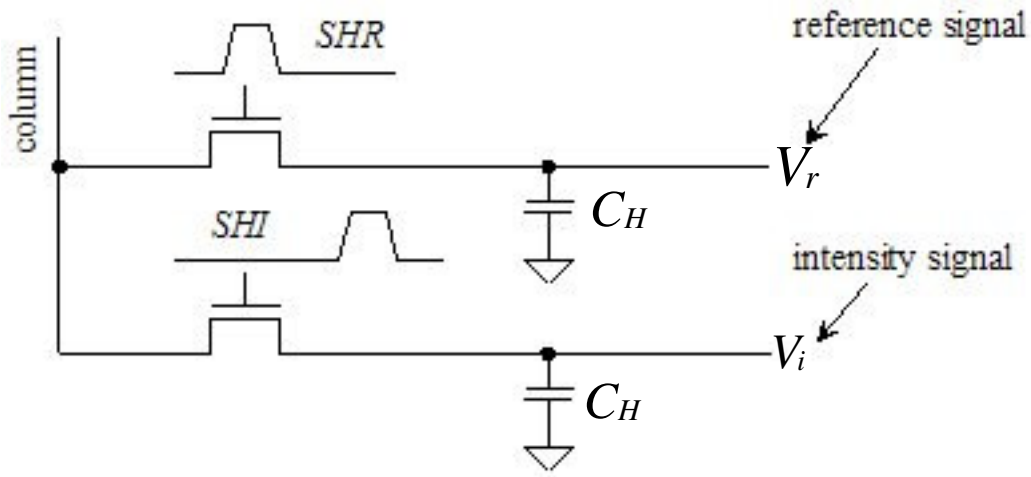
- DSM (delta-sigma modulation) can be used for sensing CMOS imaging chips used to acquire images in cameras or video recording.



- The photodiode converts light into charge which is converted into a voltage and passed to the column line.

Sampling reference and intensity signals

- *SHR* goes high and the reference or dark signal V_r from the column line is first sampled on to the hold capacitor.
- Next, *SHI* goes high and the required intensity of light V_i is sampled.
- DSM circuit takes the difference in V_r and V_i and generates a digital number.



Noise

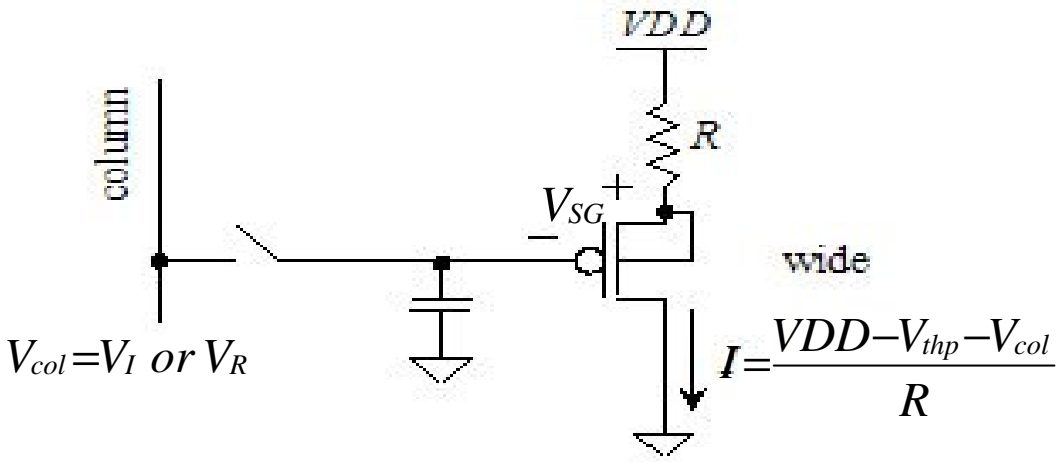
- Circuit noise limits dynamic range of sense resulting in blurring of images.
- Input sampling capacitor size set by kT/C noise considerations. This limits thermal noise in the sample.
- Output current of the pixel also contains flicker noise, using a large hold capacitance will result in lower thermal noise but will cause flicker noise to be integrated.
- Minimizing the amount of time SHR and SHI are high and the time difference between both the signals achieves a low noise sample onto C_H.
- Noise variance in the remaining part of the circuit may be reduced by N (the number of samples averaged).

Comments

- Reference and desired signals are subtracted to minimize pixel variations.
- If the comparator makes an error and switches states too earlier or too late the sense circuitry adds noise to the measured signal (digital code isn't constant but moves around).
- Counter can be thought of as a low pass digital filter.
- Increasing the clock frequency lowers the band-width of the digital filter and increases the resolution of the sense.
- Using DSM the sense operation can be run indefinitely.

Subtracting reference and intensity

- These voltages are converted into currents and then subtracted in order not to change these values with the sensing circuit.
- Voltage to current converter is used for this.
- Having the PMOS device in its own well eliminates body effect.
- Current mirror is used for subtracting V_r and V_i .



Equations

Current corresponding to reference voltage is

$$I_R = \frac{VDD - V_{thp} - V_R}{R_R} = \frac{V_{R,shift}}{R_R}$$

Current corresponding to intensity of light is

$$I_I = \frac{VDD - V_{thp} - V_I}{R_I} = \frac{V_{I,shift}}{R_I}$$

Equating the currents we get

$$V_{I,shift} = \frac{R_I}{R_R} \cdot V_{R,shift}$$

- Intensity of light on the pixel can be determined by the ratio of resistances.

Equations (cont'd)

- Resistors can be implemented using switched capacitor resistors.

We know

$$V_{I,shift} \geq V_{R,shift}$$

We can write

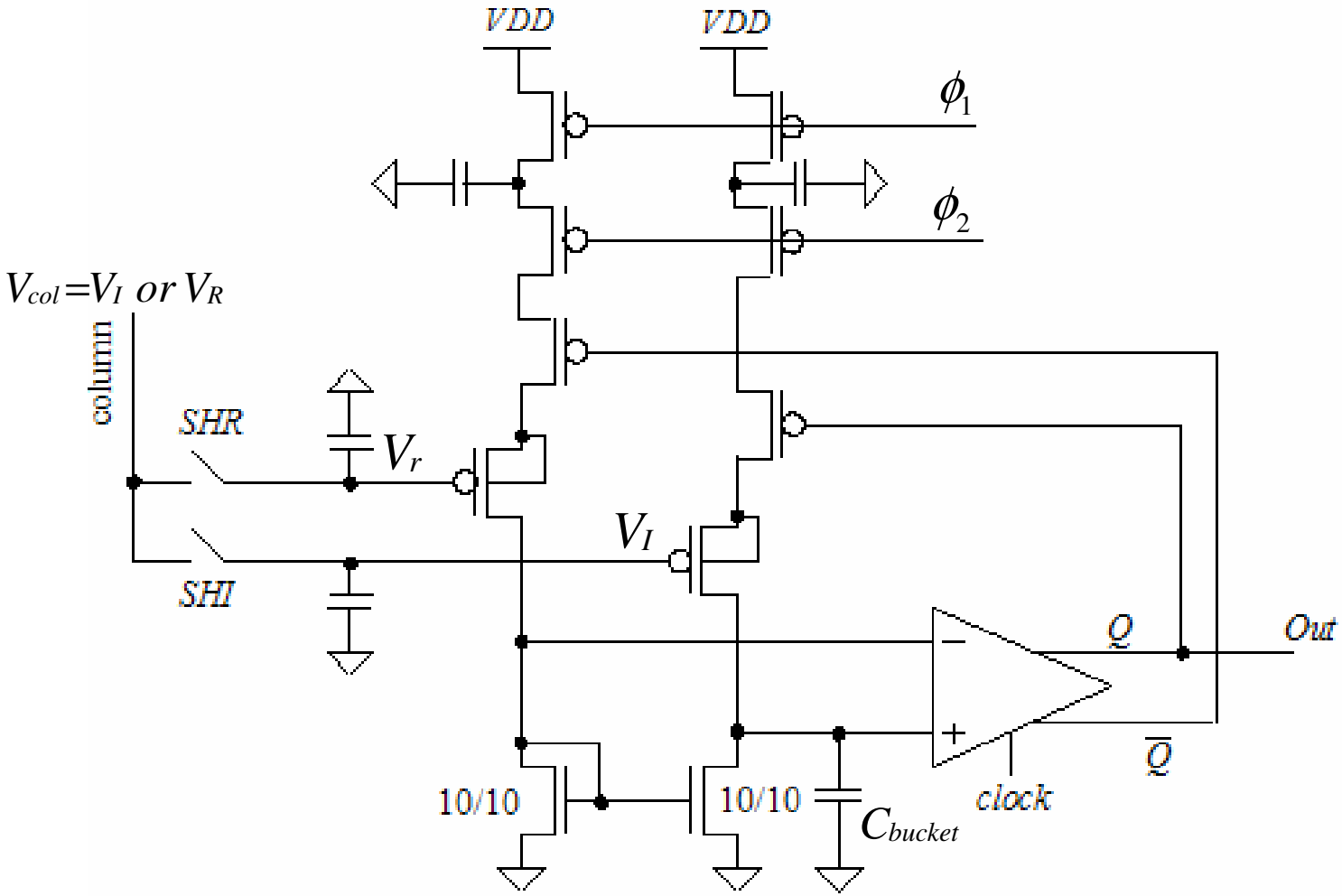
$$R_R = \frac{1}{f \cdot C_{cup} \cdot \frac{M}{N}} \qquad R_I = \frac{1}{f \cdot C_{cup} \cdot \frac{N-M}{N}}$$

then

$$V_{I,shift} = V_{R,shift} \cdot \frac{M}{N-M}$$

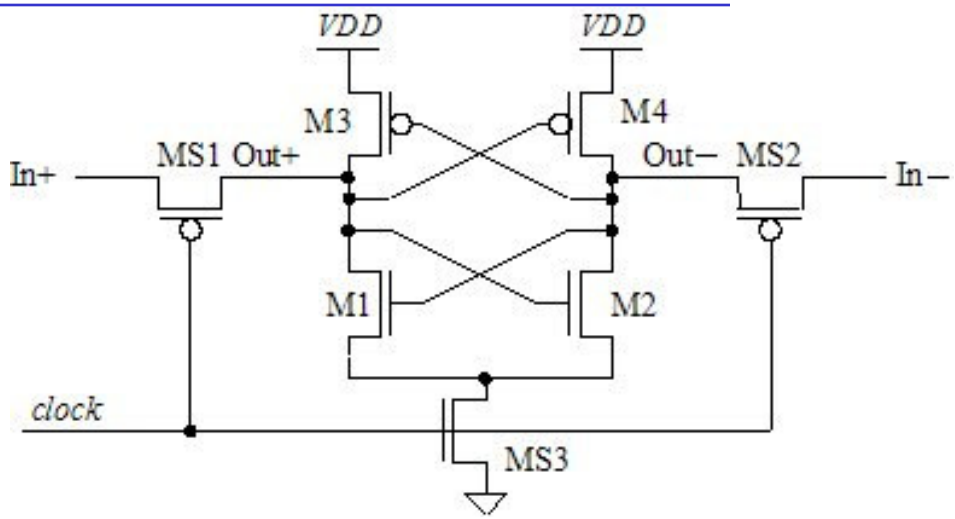
- Desired intensity of light can thus be measured.

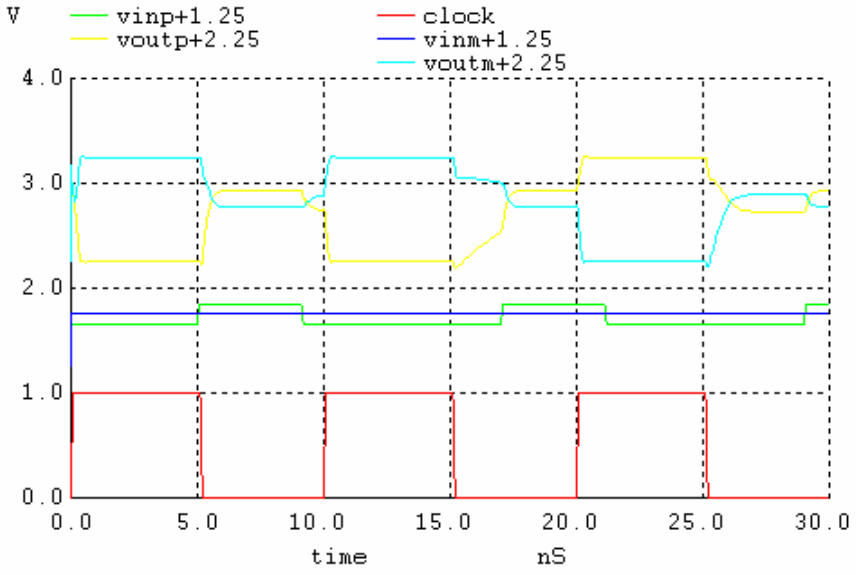
Schematic of a DSM



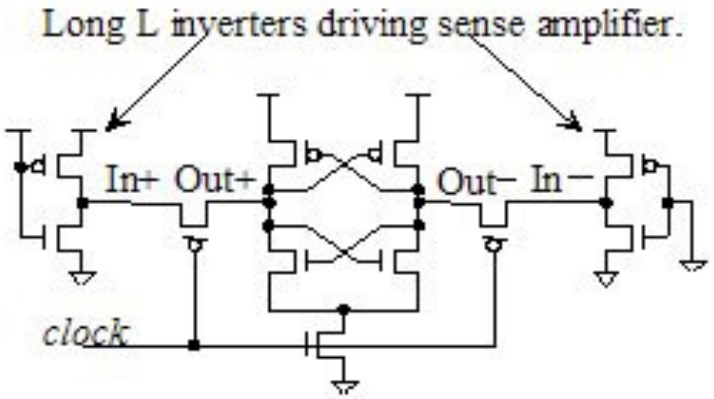
Sense-Amplifier

- When clock goes high the imbalance causes circuit to latch high or low depending on the state of inputs.
- From the simulation we can see that as clock goes low the outputs ideally track the input signal levels.
- The circuit has problems with kickback noise, memory and significant contention current.

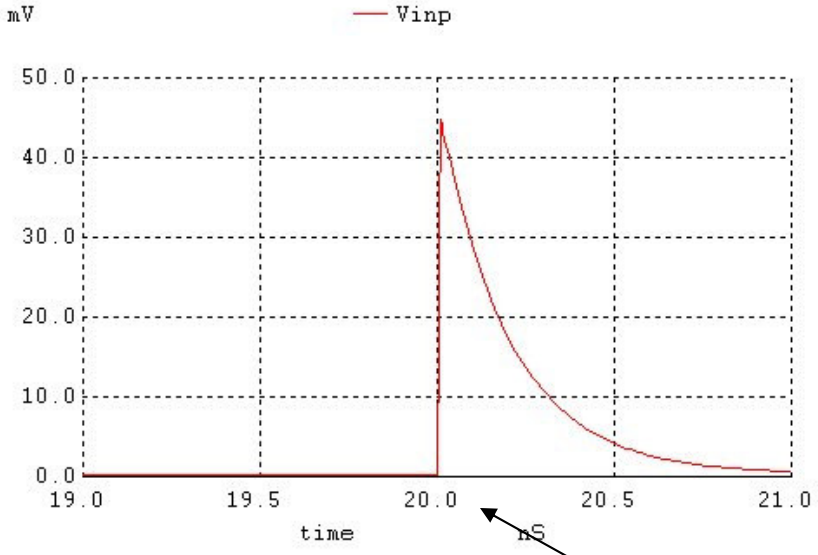


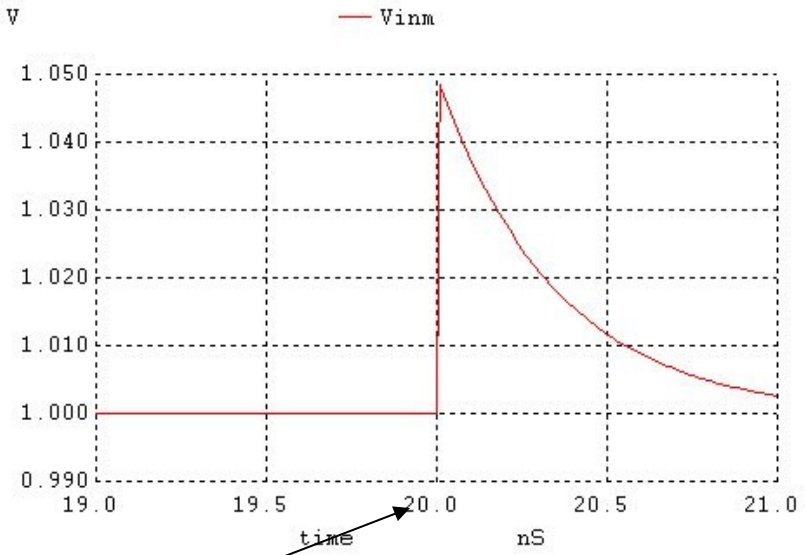


Illustrating problems with Sense-Amp



Showing clock feedthrough noise

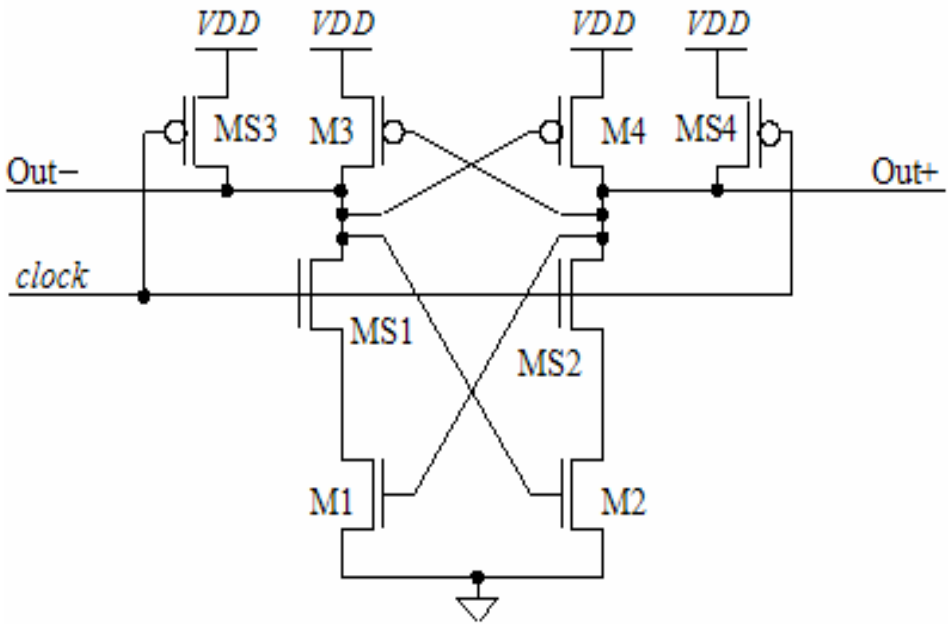




clock goes high at 20ns

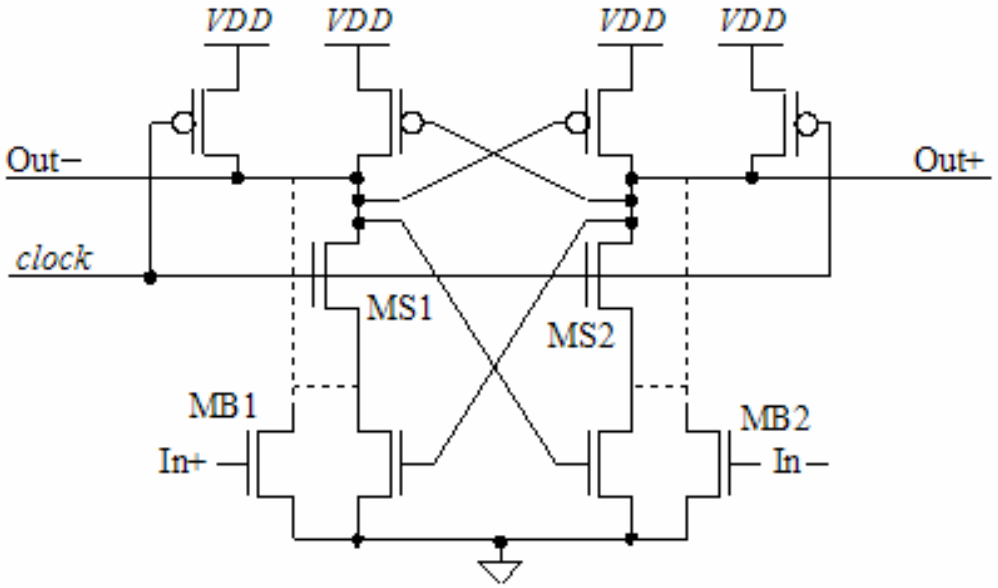
Removing Sense Amp memory

- For precision sense operation all nodes must be equilibrated to a known voltage.
- Note that here there is no direct path from VDD to ground.
- All nodes are driven high to VDD or pulled low to ground.



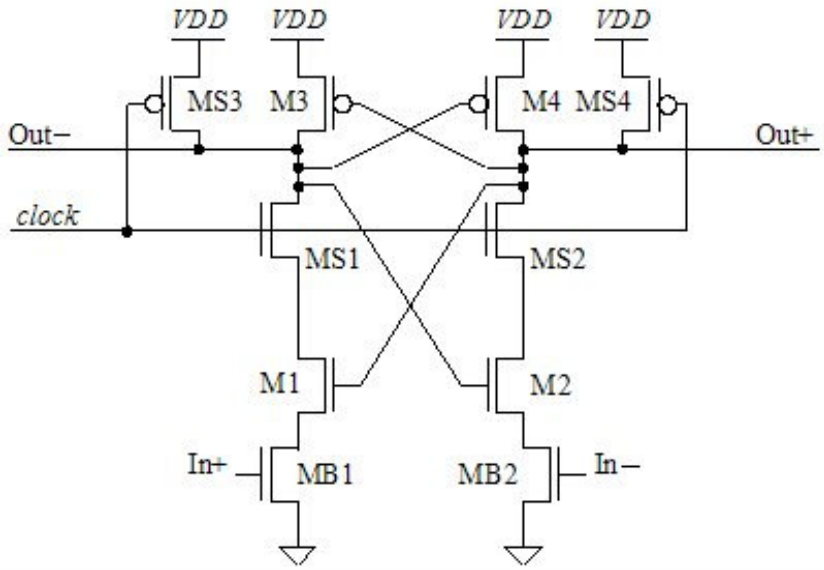
Creating an imbalance in the sense-amp

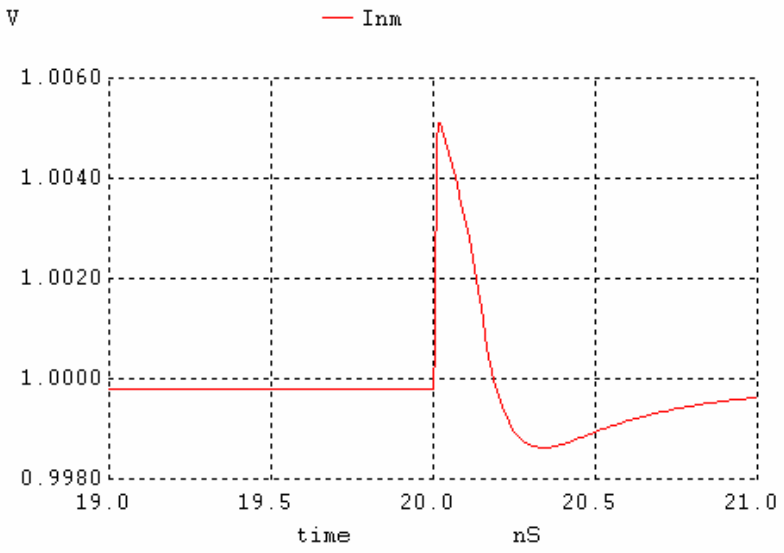
- Connecting MB1/MB2 to the drains of MS1/MS2 gives a high gain.
- Very small voltage differences can cause quick sensing.
- Long L devices can be used for MB1 and MB2 so that they don't draw significant amount of current.

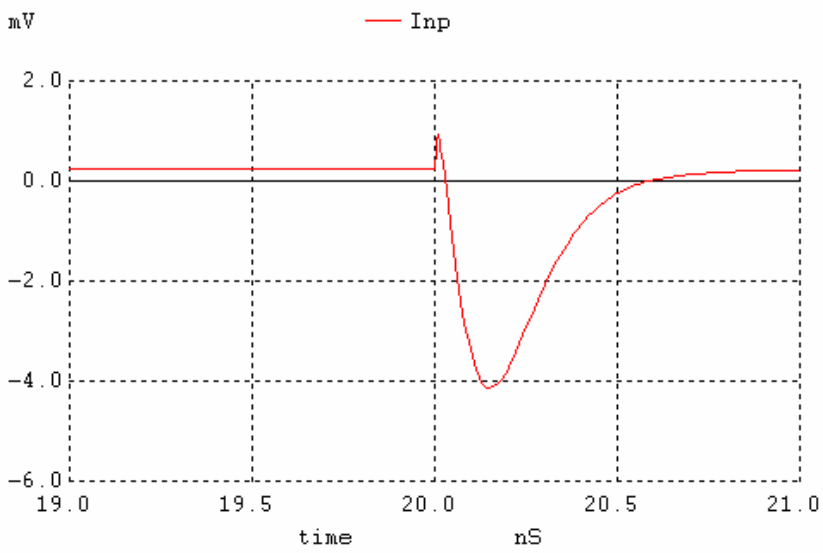


Reducing power in the sense-amp

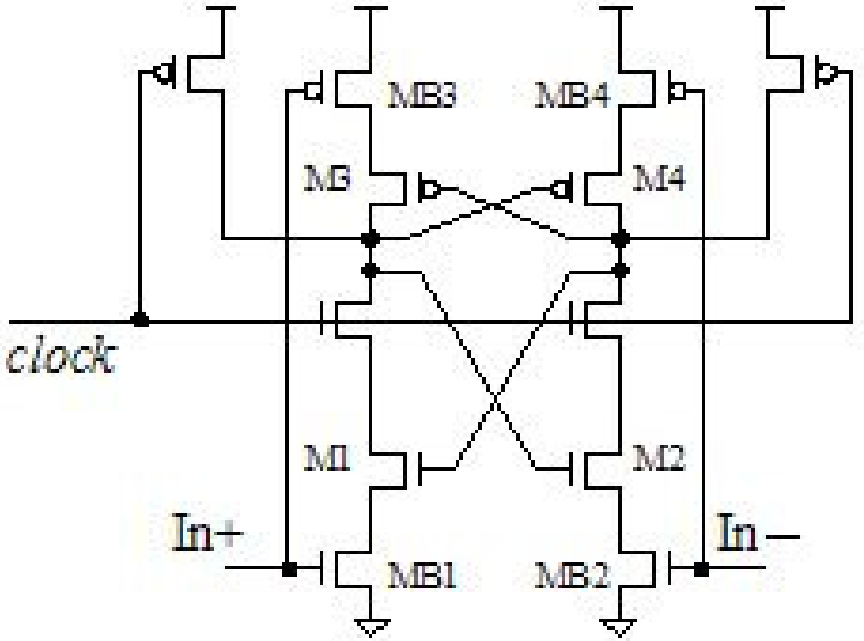
- Figure shows one idea of reducing amount of current drawn.
- Kickback noise is reduced as inputs are isolated from latch.







Showing how not to get a wide swing operation



A bad design.

Comments for this Scheme

- Robust sensing scheme
- Comparator gain and offset are not important.If the comparator makes a mistake it is averaged out.
- Any noise coupled into the sense amplifier will be averaged out.
- Sensing operation can be indefinite.
- Better resolution with increased clocked frequency.
- Less power consumption.
- Low noise (only concerned with averaged thermal noise).

On Going Research

- Circuit topologies that simplify the circuit design while at the same time provide sensitive sensing.
- Fabricating and testing the simulated designs.