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(54) **INTEGRATED CIRCUIT MEMORY WITH OFFSET CAPACITOR**

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(51) **Int. Cl.**
H01L 21/8242 (2006.01)

(52) **U.S. Cl.** **257/306**; 257/309; 257/308

(58) **Field of Classification Search** 257/306–309, 257/303, 905, 666, 777, 202–205, 723, 725, 257/668–671, 295, 296–302; 438/123, 587, 438/598, 129, 139, 107–110, 396–399, 240–254
See application file for complete search history.

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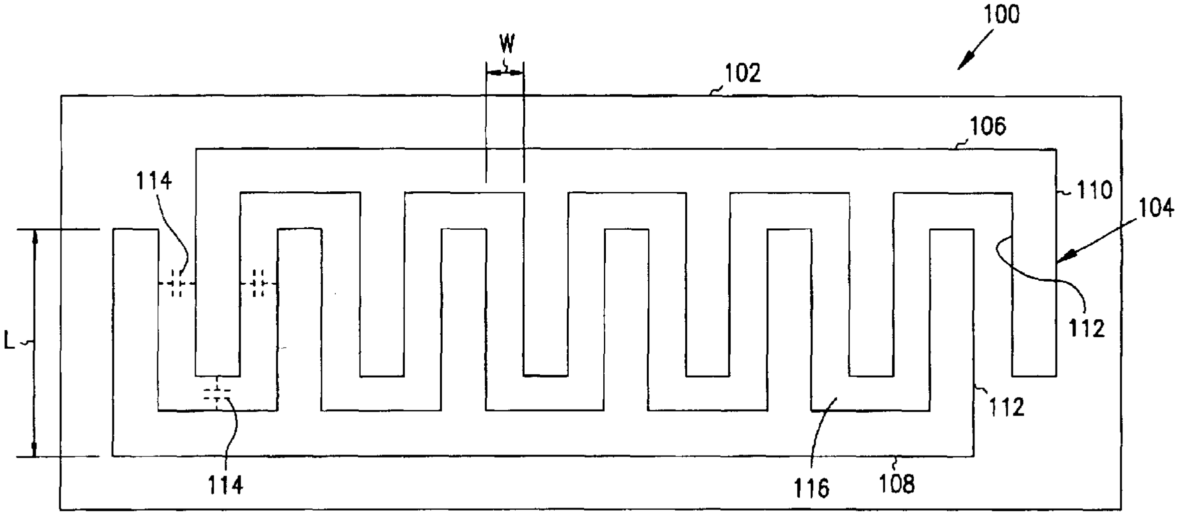
(57) **ABSTRACT**

A capacitor for use in integrated circuits comprises a layer of conductive material. The layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of capacitance per semiconductor die area.

34 Claims, 9 Drawing Sheets



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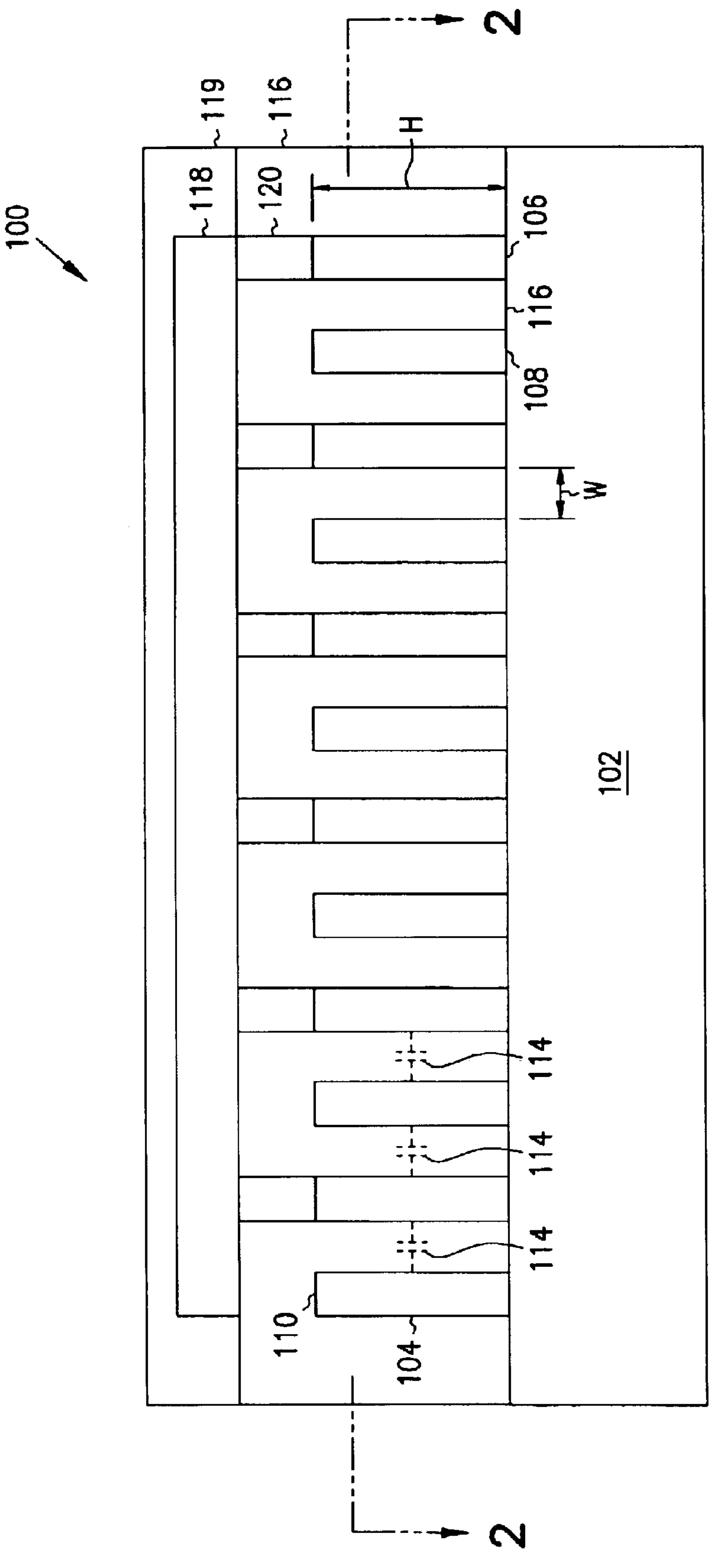


FIG. 1

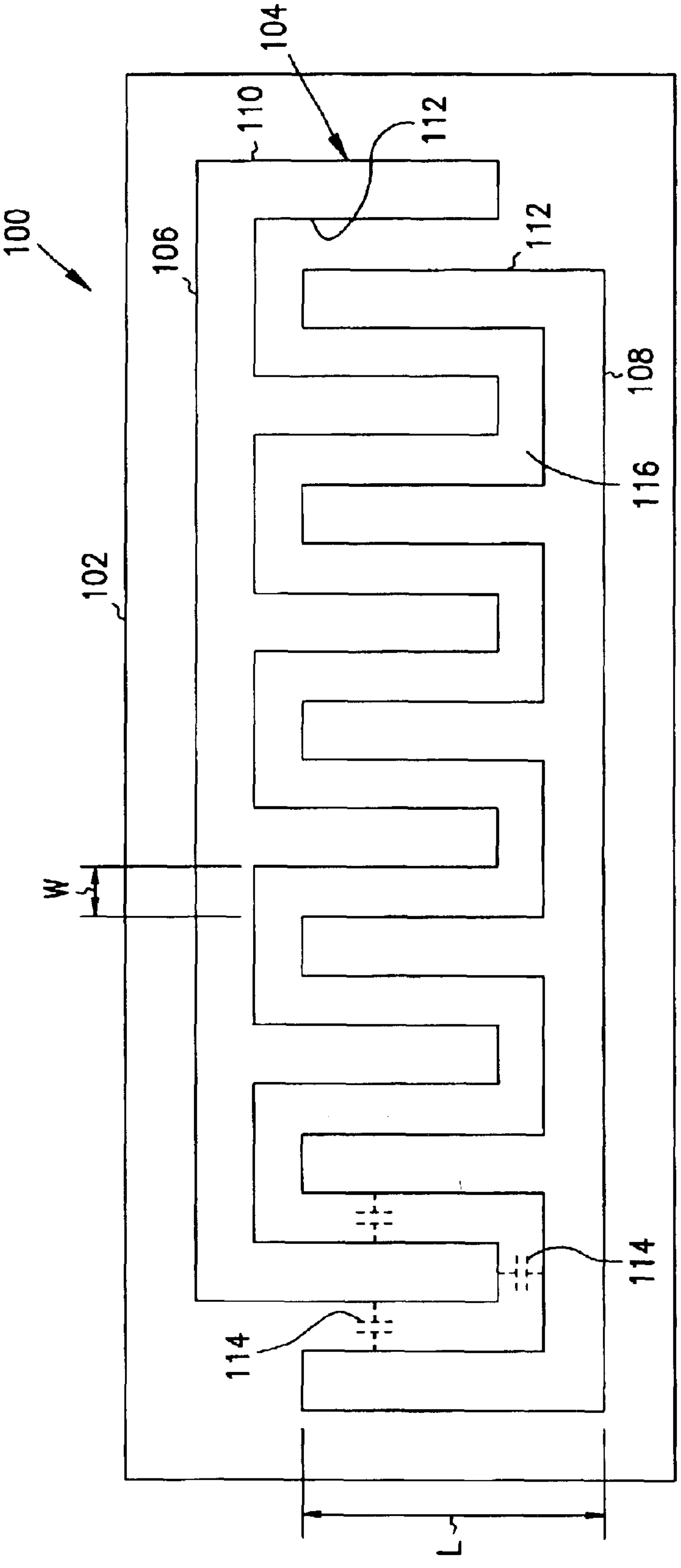
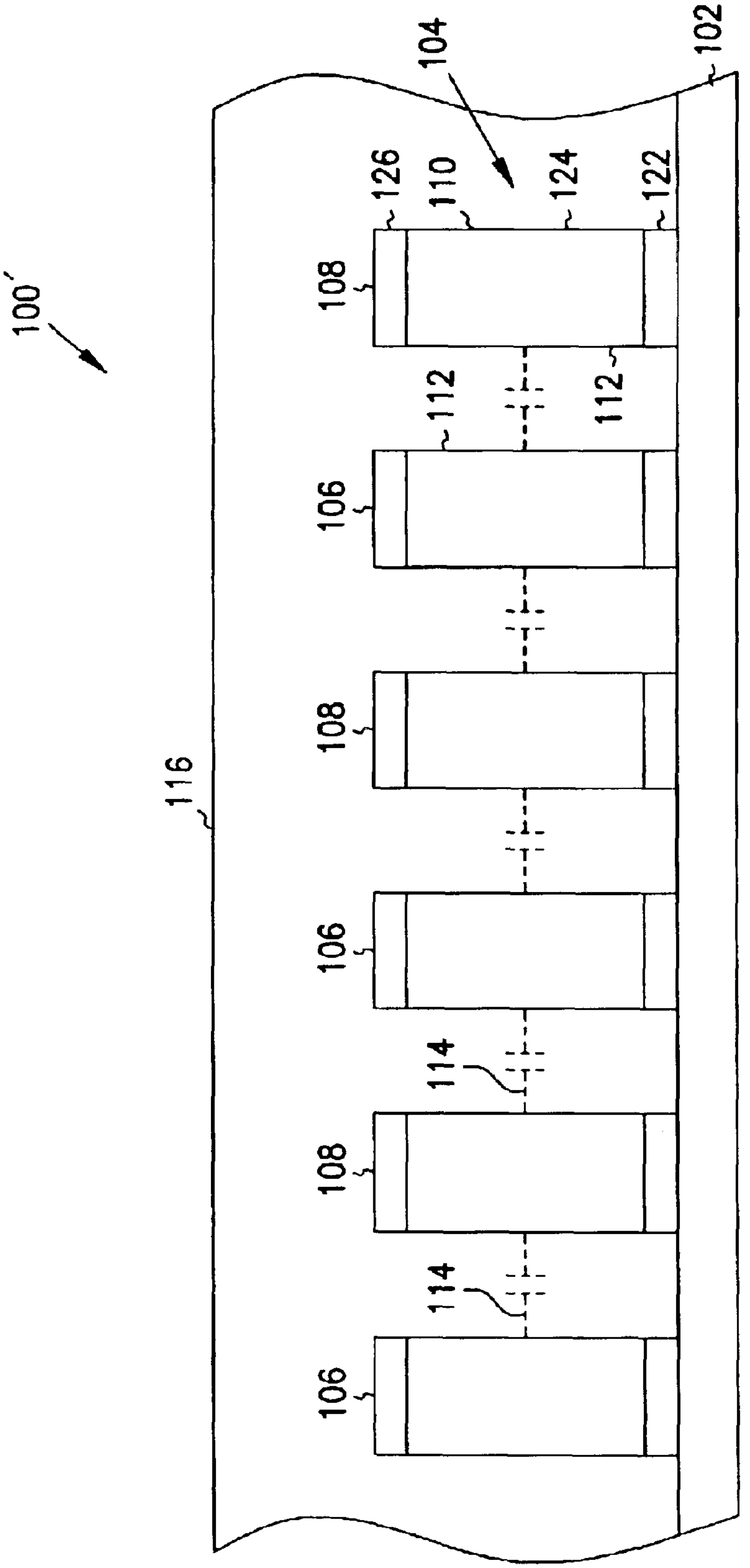


FIG. 2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102
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106
116

FIG. 3

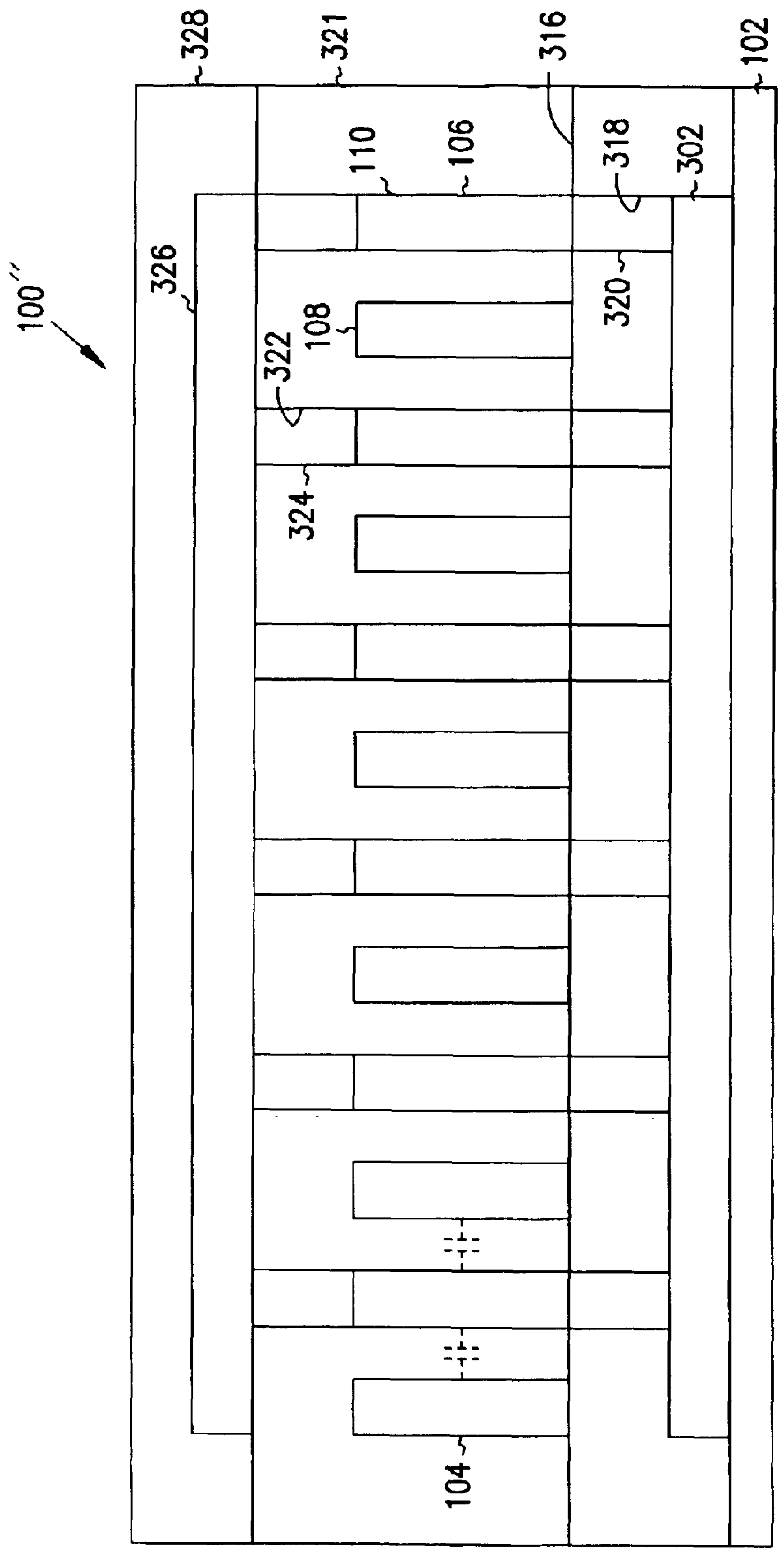
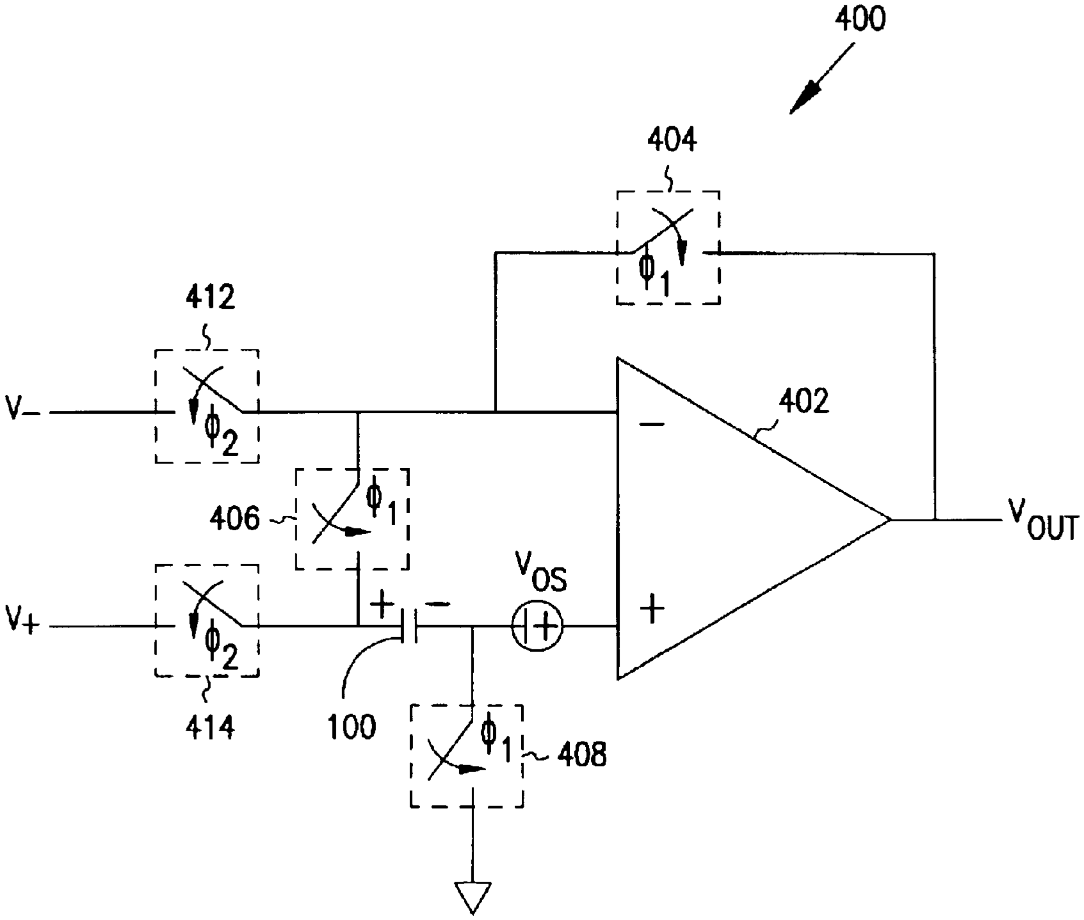


FIG. 4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404
ϕ_1
412
V−
ϕ_2
402
−
406
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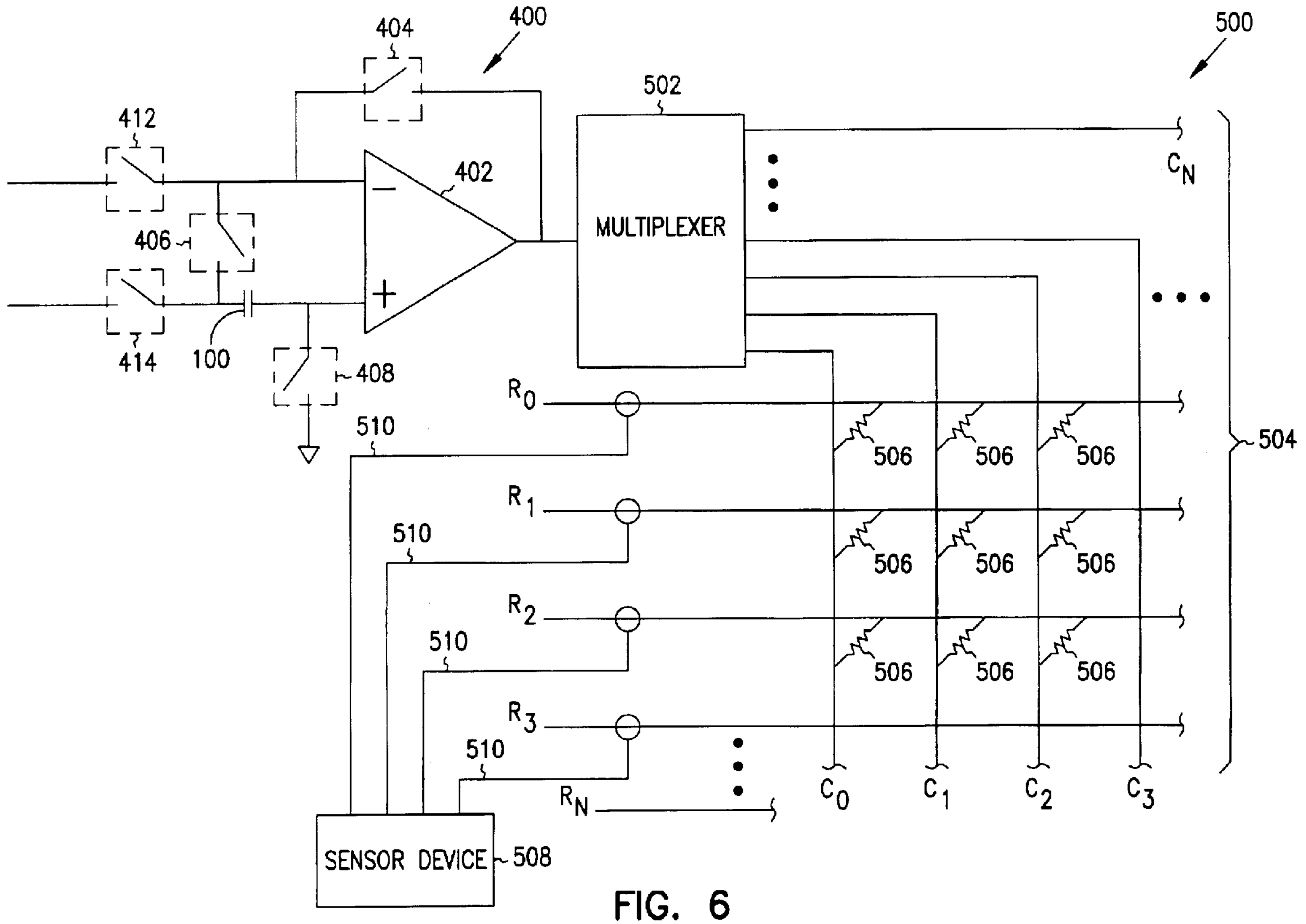
V+
ϕ_2
+
−
V_{OS}
+
414
100
ϕ_1
408

FIG. 5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100
408
MULTIPLEXER
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500
C_N
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C_1
C_2
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504
R_0
R_1
R_2
R_3
R_N
506
506
506
506
506
506
506
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506
510
510
510
510
SENSOR DEVICE
508

FIG. 6

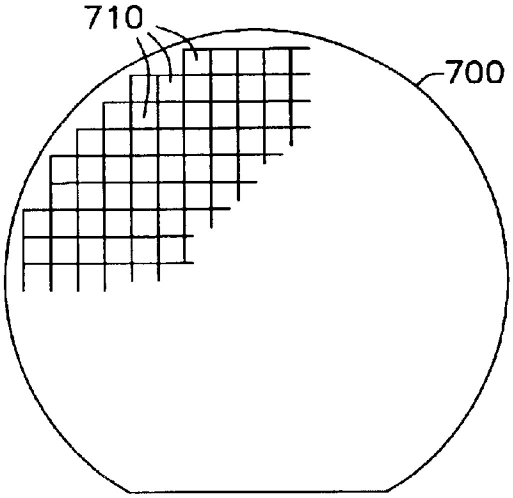


FIG. 7

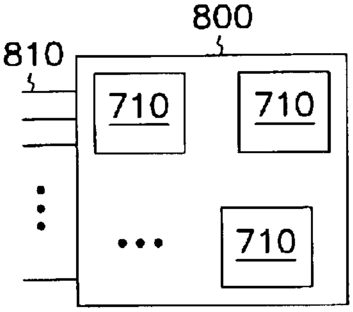


FIG. 8

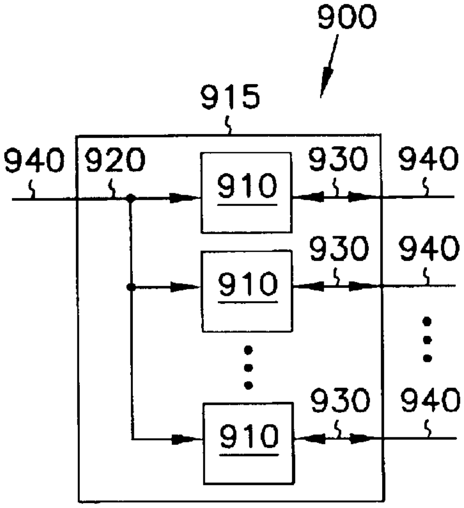


FIG. 9

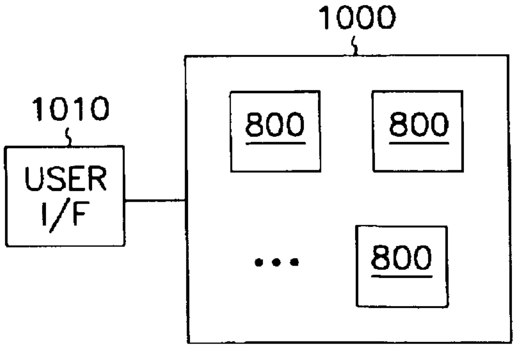
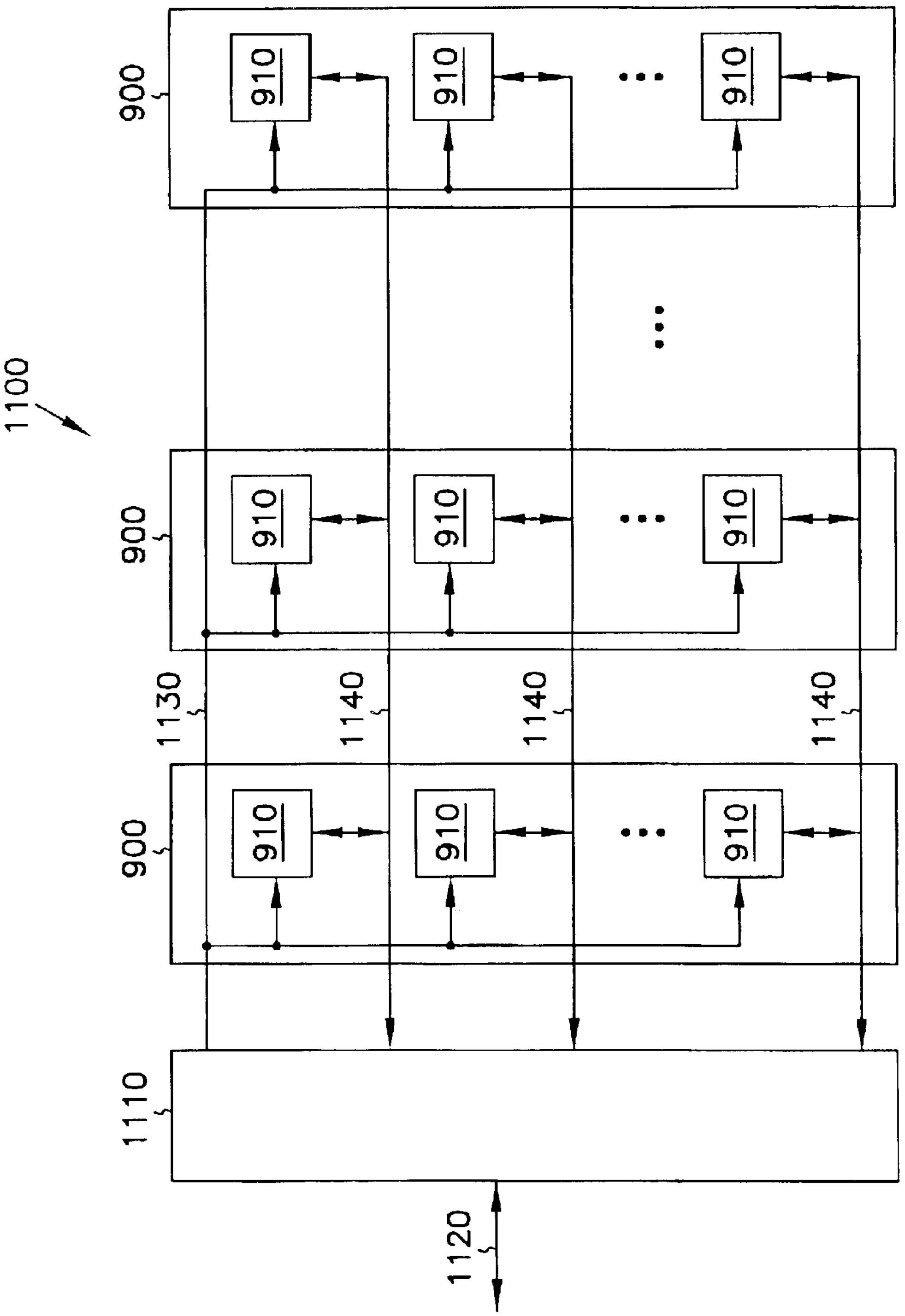


FIG. 10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900
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1110
1120

FIG. 11

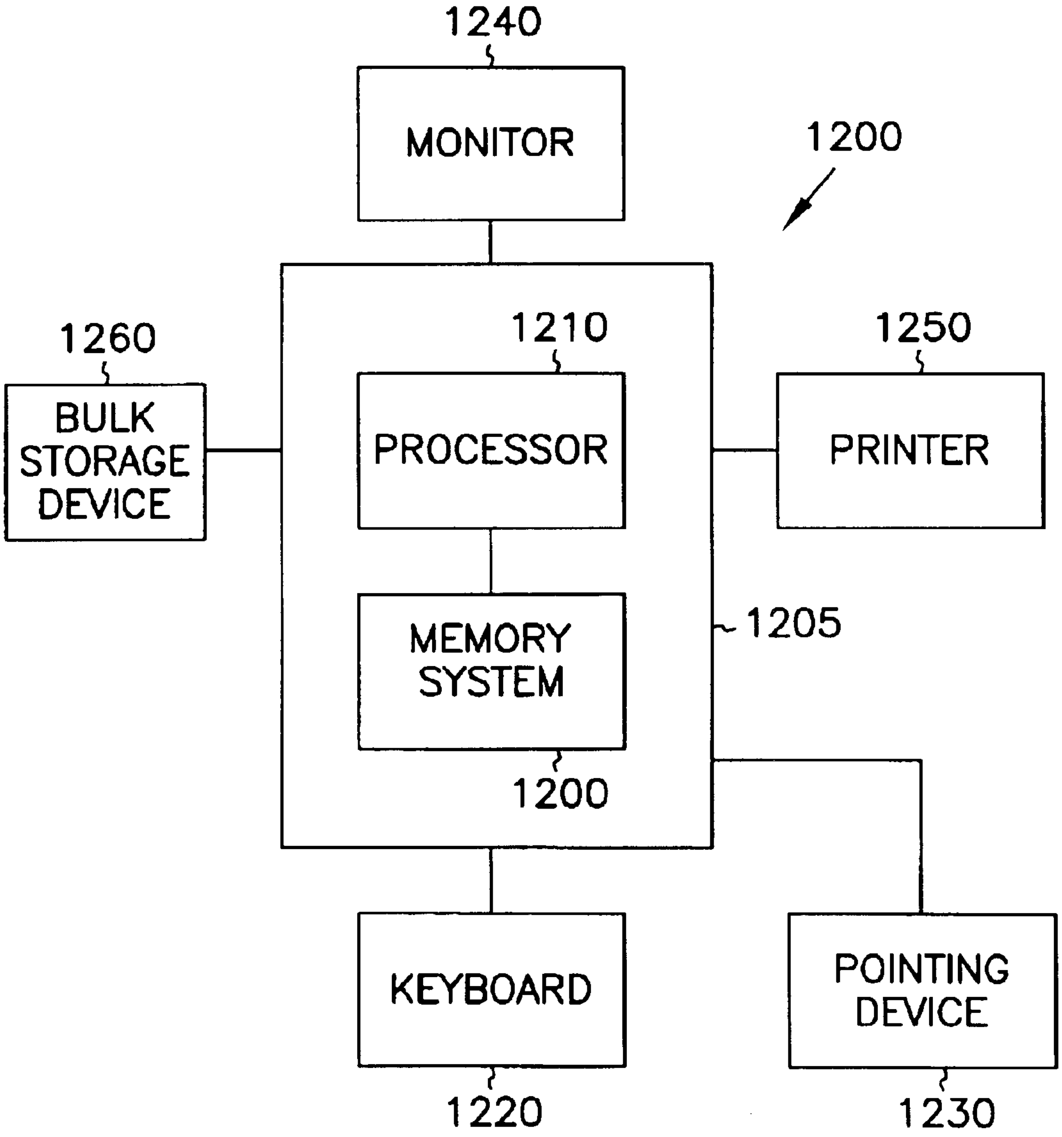
1240
MONITOR
1200
1260
BULK STORAGE DEVICE
1210
PROCESSOR
1250
PRINTER
MEMORY SYSTEM
1205
1200
KEYBOARD
POINTING DEVICE
1220
1230

FIG. 12

INTEGRATED CIRCUIT MEMORY WITH OFFSET CAPACITOR

This application is a Continuation of U.S. application Ser. No. 09/940,328, filed Aug. 27, 2001 now U.S. Pat. No. 6,509,245, which is a Divisional of U.S. application Ser. No. 09/838,526, filed Apr. 19, 2001, now U.S. Pat. No. 6,410,955.

FIELD OF THE INVENTION

The present invention relates generally to electronic circuits, and more particularly to a capacitor for use in integrated circuits.

BACKGROUND INFORMATION

There is a continuing demand for integrated circuits to perform more functions or operations in shorter periods of time. This typically requires additional components to perform the additional functions, store more data and operate more efficiently. At the same time packaging requirements are decreasing. Consumers want smaller, lighter weight products that do more and are more mobile or portable. Accordingly, circuit designers are challenged to provide more components or greater capacity per unit of area on a semiconductor die. Most electronic circuits include basic electrical components such as transistors, resistors, inductors, capacitors and the like. Capacitors are one component that can occupy a lot of area on a semiconductor die depending upon the size of the capacitor. Capacitors are typically made by depositing a first metal plate, depositing a layer of insulation material over the first metal plate and then depositing a second metal plate over the layer of insulation material and parallel to the first metal plate. The size of the capacitance will be a function of the surface area of the two facing parallel plates and other parameters such as the dielectric constant of the insulation material and the spacing between the plates. Accordingly, one primary means of increasing the capacitance, is to increase the size of each of the parallel plates but this will consume more area on the semiconductor die.

Additionally, in some circuits it may be desirable for the capacitor to be independent of voltage and frequency applied across the capacitor once it is charged to a predetermined level. For example, a capacitor may be connected to the non-inverting input of an operational amplifier to reduce or cancel the offset voltage inherent in the operational amplifier. The capacitor may be pre-charged to the opposite polarity of the offset voltage of the amplifier so that the offset voltage is canceled during normal operation of the amplifier. When an input voltage signal is applied to the input of the operational amplifier, the output voltage signal will be stable and uninfluenced by the offset voltage if the capacitor is voltage and frequency independent.

Accordingly, for the reason stated above, and for other reasons that will become apparent upon reading and understanding the present specification, there is a need for a capacitor that maximizes the amount of capacitance per unit of area of a semiconductor die and that is independent of voltage and frequency.

SUMMARY OF THE INVENTION

In accordance with the present invention, a capacitor includes a layer of conductive material formed on a substrate or semiconductor die. The layer of conductive material includes a first portion and a second portion. The first and

second portions are arranged in a predetermined pattern relative to one another to provide a maximum amount of capacitance per unit of area on the substrate or semiconductor die.

In accordance with one embodiment of the present invention, the first portion and the second portion of the layer of conductive material each have a substantially comb-like structure with a plurality of teeth. The teeth of the first portion and the teeth of the second portion are interleaved and each tooth includes a pair of sidewalls. Each sidewall, except an outside sidewall of an end tooth, faces a sidewall of a tooth of the other portion to provide a maximum of juxtaposed surface area.

In accordance with another embodiment of the present invention, an integrated circuit includes an amplifier formed on a substrate or semiconductor die and a capacitor formed on the substrate and connected to an input of the amplifier. The capacitor includes a first substantially comb-like structure of conductive material with a plurality of teeth and a second substantially comb-like structure of conductive material also with a plurality of teeth. The teeth of the second substantially comb-like structure are interleaved with the teeth of the first substantially comb-like structure and each tooth of the first and second comb-like structures have a pair of sidewalls. Each sidewall has a selected surface area and each of the teeth of the first and second comb-like structures are separated by a gap of a chosen width to provide a predetermined capacitance.

In accordance with another embodiment of the present invention, a memory system includes an array of memory elements. Each memory element is connected by one of plurality of row lines and by one of a plurality of column lines. An amplifier is connected to at least one of each of the plurality of column lines or each of the plurality of row lines. A capacitor is connected to an input of each amplifier to cancel the offset voltage of the amplifier. The capacitor includes a layer of conductive material having a first portion and a second portion. The first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of capacitance per given area of the substrate or semiconductor die.

In accordance with a further embodiment of the present invention, a electronic system includes a processor and a memory device coupled to the processor. The memory device includes an array of memory elements and each memory element is connected by one of a plurality of row lines and by one of a plurality of column lines. An amplifier is connected to at least one of each of the plurality of row lines or to each of the plurality of column lines. A capacitor is connected to an input of each amplifier to cancel the offset voltage. Each capacitor includes a layer of conductive material divided into a first portion and a second portion. The first and second portions are arranged in a predetermined pattern relative to one another to provide a maximum amount of capacitance per given area of a substrate or semiconductor die.

In accordance with a further embodiment of the present invention, a method for making a capacitor includes depositing at least one layer of conductive material on a substrate; removing material from the layer of conductive material to form a first and second portion arranged in a predetermined pattern relative to one another to provide a maximum amount of capacitance per area of the substrate or wafer.

In accordance with another embodiment of the present invention, a method for correcting for offset voltage in an amplifier includes: connecting an output of the amplifier to an inverting input of the amplifier; connecting a capacitor between the inverting input and a positive or non-inverting input of the amplifier, wherein the capacitor comprises a layer of conductive material including at least a first portion and a second portion and wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum capacitance per area; and connecting the positive input of the amplifier to ground to cause the capacitor to charge to the offset voltage.

In accordance with a further embodiment of the present invention, a method for applying a stable voltage to a column or a row line of a memory device includes forming an amplifier and connecting an output of the amplifier to one of the row line or the column line; forming a capacitor connected to an input of the amplifier, wherein the capacitor is formed by depositing at least one layer of conductive material and removing material from the at least one layer of conductive material to form a first portion and a second portion that are arranged in a predetermined pattern relative to one another to provide a maximum capacitance per area of a semiconductor wafer or die; and forming circuitry to charge the capacitor to an opposite polarity of the offset voltage to nullify the offset voltage of the amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings like reference numerals describe substantially similar components throughout the several views. Like numerals having different letter suffixes represent different instances of substantially similar components.

FIG. **1** is a side elevation view of a capacitor in accordance with one embodiment of the present invention.

FIG. **2** is a cross-section view of the capacitor of FIG. **1** taken along lines **2**—**2**.

FIG. **3** is a partial side elevation view of a capacitor in accordance with another embodiment of the present invention.

FIG. **4** is a side elevation view of a capacitor in accordance with a further embodiment of the present invention.

FIG. **5** is a schematic diagram of an offset or operational amplifier and offset capacitor in accordance with an embodiment of the present invention.

FIG. **6** is schematic diagram of a portion of a memory device or system including an operational amplifier and offset capacitor in accordance with an embodiment of the present invention.

FIG. **7** is a top view of a wafer or substrate containing semiconductor dies in accordance with an embodiment of the present invention.

FIG. **8** is a block diagram of an exemplary circuit module in accordance with an embodiment of the present invention.

FIG. **9** is a block diagram of an exemplary memory module in accordance with an embodiment of the present invention.

FIG. **10** is a block diagram of an exemplary electronic system in accordance with the present invention.

FIG. **11** is a block diagram of an exemplary memory system in accordance with the present invention.

FIG. **12** is a block diagram of an exemplary computer system in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that process or mechanical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor, as well as other semiconductor support structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Referring to FIGS. **1** and **2**, FIG. **1** is a side elevation of a capacitor **100** in accordance with the present invention. The capacitor **100** may be formed on a substrate **102** or semiconductor wafer. A layer **104** of conductive material is deposited on the substrate **102** by chemical vapor deposition (CVD) or similar techniques to a selected height “H.” The conductive layer **104** may be tungsten. The conductive layer **104** is then etched by photo resistive techniques, mechanical etching or the like to form a first portion **106** and a second portion **108** arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area between the first and second portions **106** and **108** and accordingly a maximum amount of capacitance per unit of area of the substrate **102** or semiconductor wafer on which the capacitor **100** is formed. In accordance with one embodiment of the invention, the predetermined pattern of the first portion **106** and the second portion **108** may be substantially comb-like structures as shown in FIG. **2**. Each of the first and second portions **106** and **108** include a plurality of teeth **110**. Each tooth **110** has a sidewall **112** with a selected height “H” corresponding to the height of the conductive layer **104** and length “L” to provide a selected surface area facing a juxtaposed surface area of the other portion **106** or **108**. The capacitor **100** is then formed by the juxtaposed sidewalls **112** of the teeth **110** of the first and second portions **106** and **108** corresponding to parallel plates of a capacitor as illustrated by the standard capacitor symbols **114** shown by broken lines between the sidewalls **112** in FIGS. **1** and **2**. The interleaved teeth **110** of the comb-like structures of first and second portions **106** and **108** provide a maximum amount of capacitance per unit of area of the substrate **102**.

In the predetermined pattern, the first and second portions **106** and **108** are separated by a substantially serpentine-shaped gap of a selected width “W.” A layer of insulation material **116** is deposited over and between the first and second portions **106** and **108**. The value or amount of the capacitance formed by the first and second portions **106** and **108** will be a function of the surface area of the juxtaposed sidewalls **112**, the width W of the gap between the first and second portions **106** and **108** and the dielectric constant of the insulation layer **116**. Accordingly, the value or amount of the capacitance may be predetermined by selecting the length L and height H of the juxtaposed sidewalls **112** to provide a selected surface area, choosing the width of the gap W and selecting the dielectric constant of the insulation layer **116**.

While the predetermined pattern of the first and second portions **106** and **108** have been described an a substantially comb-like structure, it should be noted that other patterns may be used as well to provide a predetermined or desired capacitance. Interconnected strips of material of a selected height and width that are interleaved with other interconnected strips of material may be used to provide the desired capacitance value.

In accordance with one embodiment of the present invention shown in FIG. **1**, a reference plate **118** of conductive or semiconductive material may be disposed on the insulation layer **116** and over the first and second portions **106** and **108**. The reference plate **118** is electrically connected to one of the first or second portions **106** or **108** by at least one contact or plug **120**. The plugs may be formed by creating vias or holes through the insulation layer **116** and then depositing a conductive material in the via in contact with the first portion **106** or the second portion **108**. The plugs **120** may be formed from tungsten, copper, aluminum or the like. The reference plate **118** will provide further capacitance between itself and the one of the first or second portions **106** or **108** that is not electrically connected to the reference plate **118**. The reference plate **118** is then preferably covered by another insulation layer **119**. While the reference plate **118** is shown in FIG. **1** and being disposed over the first and second portions **106** and **108**, the reference plate **118** could have also been formed on the substrate **102** first and then the first and second portions **106** and **108** could have been formed over the reference plate **118**.

In another embodiment of the present invention shown in FIG. **3**, the layer of conductive material **104** may include a first layer of metalization, semiconductor material or polysilicon **122**, a second layer of tungsten **124** disposed over the first layer of metalization **122** and a third layer of metalization, semiconductor material or polysilicon **126** or polysilicon disposed over the second layer of tungsten **124**. All three layers **122**, **124** and **126** are then etched to form the teeth **110** of the first and second portions **106** and **108**. The capacitance **100'** is therefore created between the sidewalls **112** as illustrated by the capacitor symbols **114** in broken lines and between the metalization layers **122** and **126**. The metalizations layers **122** and **126** may be much thinner than the tungsten layer **124**.

In another embodiment of the present invention shown in FIG. **4**, a capacitor **100"** is similar to the capacitor **100** in FIGS. **1** and **2** and includes a first reference plate or layer **302** of conductive or semiconductive material formed on the substrate **102** or silicon wafer. A layer of insulation material **316** is disposed over the first reference plate **302**. At least one hole or via **318** is formed in the insulation layer **316** and contacts or plugs **320** are formed in the vias **318** to electrically connect the first reference plate **302** to the teeth **110** of one of the first or second portions **106** or **108**. A layer of conductive material **104** is deposited on the insulation layer **316** and is etched to form the first portion **106** and the second portion **108**. The first and second portions **106** and **108** will preferably be formed in a predetermined pattern to provide the maximum amount of juxtaposed surface area and therefore the maximum amount of capacitance per unit of area of the substrate **102** similar to that described with respect the capacitor **100** in FIGS. **1** and **2**. Accordingly, the first and second portions **106** and **108** may also be comb-like structures similar to those in FIGS. **1** and **2**; although other patterns may be used as well to provide a predetermined capacitance value. A further layer of insulation material **321** is deposited over the first and second portions **106** and **108**.

At least one hole or via **322** is formed through the insulation material **321** exposing whichever of the first or second portions **106** or **108** that is contacted by the first reference plate **302**. A plug or contact **324** of conductive material is deposited in the hole **322** in contact with the first or second portion **106** or **108**. A second reference plate **326** of conductive or semiconductive material is then deposited on the insulation material layer **321** and in contact with the at least one plug **324**. Accordingly, the reference plates **302** and **326** form additional capacitance with whichever of the first and second portions **106** or **108** that is not connected by the plugs **320** and **324** to the first and second reference plates **302** and **326**. The plugs **320** and **324** may be made from tungsten. The first portion **106** and the second portion **108** may also be made from tungsten or may be two metalization layers separated by a thicker layer of tungsten similar to the teeth **110** shown in FIG. **3**.

One application of the capacitor **100** is as an offset capacitor **100** in an operational amplifier circuit **400** to reduce or cancel the offset voltage (Vos) of an operational amplifier **402** as shown in FIG. **5**. The offset capacitor **100** may be connected to the non-inverting or positive input of the operational amplifier **402**. A first switch **404** is connected between an output (Vout) of the amplifier **402** and an inverting or negative input of the amplifier **400**. A second switch **406** is connected between the inverting input of the amplifier **402** and one side of the capacitor **100**. The other side of the capacitor **100** is connected to the non-inverting input of the amplifier **402**, and a third switch **408** is connected between the other side of the capacitor **100** at a node **410** and ground. Another pair of switches **412** and **414** respectively connect or disconnect any input signals V− or V+ from the inverting and non-inverting inputs of the amplifier **402**.

In operation, a timing signal ϕ_1 may be generated by a controller or processor (not shown in FIG. **5**) to close switches **404**, **406** and **408**. The capacitor **100** will then be charged to the level of the offset voltage Vos but with the opposite polarity of the offset voltage to nullify or cancel the offset voltage during normal operation of the amplifier **402**. After a predetermined time delay to fully charge the capacitor **100** to the offset voltage, switches **404**, **406** and **408** are opened or another signal may be generated to open switches **404**, **406** and **408**, and a timing signal ϕ_2 is generated to connect any input signals to the operational amplifier **402**. The offset capacitor **100** will then cancel the offset voltage Vos to provide a stable output voltage Vout that is independent of the input voltage and frequency.

Referring to FIG. **6**, one application of the operational amplifier circuit **400** of FIG. **5** is to drive the column lines of a magnetic random access memory (MRAM) device or system **500**. A simplified schematic diagram of a portion of an MRAM system **500** is shown in FIG. **6**. The amplifier **402** is preferably connected to a multiplexer **502** and the multiplexer **502** is connected to a plurality of column lines C_0–C_n. A plurality of amplifier circuits **400** could be used rather than the multiplexer **502** with an amplifier circuit **400** being connected to each column line; however, the plurality of amplifier circuits **400** would occupy much more area on a substrate or semiconductor die (not shown in FIG. **6**) that is better used for other components such a memory array **504** or matrix. The memory array **504** includes a plurality of resistive elements or memory elements **506**. Each memory element **506** is connected between each column line C_0–C_n and row line R_0–R_n. A sensor device **508** is connected by leads **510** to each of the row lines to sense the current when a row line is active to retrieve or read information from the

MRAM system **500**. The current in an active row line should be precise for sensing to function correctly. Accordingly, to provide an accurate current level and proper sensing, the associated column lines must be held at a stable, constant reference voltage level. A variation of one or two millivolts could provide erroneous sensing of the row lines. Accordingly, the reference output voltage Vout from the amplifier circuit **400** that is applied to the column lines must be very stable and not influenced by the offset voltage of the operational amplifier **402**. The capacitor **100** must therefore accurately nullify the offset voltage and not be influenced or vary as a result of voltage or frequency changes associated with the input signals; in other words, the capacitor **100** should be independent of voltage and frequency.

The present invention provides a relatively large bipolar capacitor in terms of the number of microfarads per unit of die area compared to other uses of capacitors in memory circuits which have capacitances on the order of nanofarads or femtofarads per unit of area. As described above, the large capacitance values are required in the MRAM amplifier circuit to provide the very stable line voltage for sensing and reading of the row lines for proper operation of the MRAM system. The three dimensional capacitor structures of the present invention pack the largest surface area between capacitor plates in the smallest footprint or die area (IC real estate) to provide additional die area for memory elements.

While the memory device **500** has been described with respect to the amplifier circuit **400** being connected to the column lines, the memory array **504** is substantially symmetrical and the row and column lines could be interchanged such that the amplifier circuit **400** could just as well be connected to the row lines and the column lines could be read or sensed by the sensor device **508**.

With reference to FIG. **7**, in one embodiment, a semiconductor die **710** is produced from a silicon wafer **700**. The die **710** is an individual pattern, typically rectangular, on a substrate that contains circuitry to perform a specific function. A semiconductor wafer **700** will typically contain a repeated pattern of such dies **710** containing the same functionality. Die **710** may contain circuitry for the capacitor **100**, operational amplifier circuit **400** and memory device **500** or other device with which the capacitor **100** may be utilized, as discussed above. Die **710** may further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die **710** is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die **710** for unilateral or bilateral communication and control.

As shown in FIG. **8**, two or more dies **710** may be combined, with or without protective casing, into a circuit module **800** to enhance or extend the functionality of an individual die **710**. Circuit module **800** may be a combination of dies **710** representing a variety of functions, or a combination of dies **710** containing the same functionality. Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules and application-specific modules, multiple voltage supply switches **100** and control circuits **200** and may include multi-layer, multi-chip modules. Circuit module **800** may be a sub-component of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft and others. Circuit module **800** will have a variety of leads **810** extending therefrom providing unilateral or bilateral communication and control.

FIG. **9** shows one embodiment of a circuit module as a memory module **900**. Memory module **900** generally depicts a Single In-line Memory Module (SIMM) or Dual In-line Memory Module (DIAM). A SIMM or DIAM is generally a printed circuit board (PCB) or other support containing a series of memory devices. While a SIMM will have a single in-line set of contacts or leads, a DIAM will have a set of leads on each side of the support with each set representing separate I/O signals. Memory module **900** contains multiple memory devices **910** contained on support **915**, the number depending upon the desired bus width and the desire for parity. Memory module **900** may contain memory devices **910** on both sides of support **915**. Memory module **900** accepts a command signal from an external controller (not shown) on a command link **920** and provides for data input and data output on data links **930**. The command link **920** and data links **930** are connected to leads **940** extending from the support **915**. Leads **940** are shown for conceptual purposes and are not limited to the positions shown in FIG. **9**. The memory module **900** or memory devices **910** may also include the multiple voltage switch **100** and control circuit **200** to provide application of different voltages to the memory devices **910** to enable the memory devices to perform different functions or operations or to place the memory devices **910** in different modes as previously described.

FIG. **10** shows an electronic system **1000** containing one or more circuit modules **800**. Electronic system **1000** generally contains a user interface **1010**. User interface **1010** provides a user of the electronic system **1000** with some form of control or observation of the results of the electronic system **1000**. Some examples of user interface **1010** include the keyboard, pointing device, monitor and printer of a personal computer; the tuning dial, display and speakers of a radio; the ignition switch and gas pedal of an automobile; and the card reader, keypad, display and currency dispenser of an automated teller machine. User interface **1010** may further describe access ports provided to electronic system **1000**. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules **800** may be a processor providing some form of manipulation, control or direction of inputs from or outputs to user interface **1010**, or of other information either preprogrammed into, or otherwise provided to, electronic system **1000**. One or more of the circuit modules **800** may also include a multiple voltage switch **100** and control circuit **200** to facilitate the application of different voltage levels to other components in the circuit module **800** or to other circuit modules **800** in the electronic system **1000**. As will be apparent from the lists of examples previously given, electronic system **1000** will often contain certain mechanical components (not shown) in addition to circuit modules **800** and user interface **1010**. It will be appreciated that the one or more circuit modules **800** in electronic system **1000** can be replaced by a single integrated circuit. Furthermore, electronic system **1000** may be a sub-component of a larger electronic system.

FIG. **11** shows one embodiment of an electronic system as a memory system **1100**. Memory system **1100** contains one or more memory modules **900** and a memory controller **1110**. Memory controller **1110** provides and controls a bidirectional interface between memory system **1100** and an external system bus **1120**. Memory system **1100** accepts a command signal from the external bus **1120** and relays it to the one or more memory modules **900** on a command link **1130**. Memory system **1100** provides for data input and data output between the one or more memory modules **900** and external system bus **1120** on data links **1140**. Memory system **1100** may include memory devices such as the MRAM device **500** of FIG. **6**.

FIG. **12** shows a further embodiment of an electronic system as a computer system **1200**. Computer system **1200** contains a processor **1210** and a memory system **1100** housed in a computer unit **1205**. Computer system **1200** is but one example of an electronic system containing another electronic system, i.e. memory system **1100**, as a subcomponent. Computer system **1200** optionally contains user interface components. Depicted in FIG. **12** are a keyboard **1220**, a pointing device **1230**, a monitor **1240**, a printer **1250** and a bulk storage device **1260**. It will be appreciated that other components are often associated with computer system **1200** such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor **1210** and memory system **1100** of computer system **1200** can be incorporated on a single integrated circuit. Such single package processing units reduce the communication time between the processor **1210** and the memory system **1100**.

While the three dimensional capacitor structures of the present invention have been described with respect to use in an amplifier circuit and memory circuits, it should be noted that the three dimensional capacitor structures may be used in any circuit where a relatively large capacitance value is needed but design constraints or available die area necessitate that the capacitor occupies the smallest possible footprint on the die or wafer. The present invention packs the largest surface area between capacitor plates into the smallest footprint on a semiconductor die or wafer.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area between the first and second portions; and

a layer of insulation material disposed at least between the first and second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

2. The integrated circuit memory device of claim **1**, wherein the predetermined pattern is a substantially comb-like structure wherein the teeth of the combs of the first portion and the second portion are interleaved.

3. The integrated circuit memory device of claim **2**, wherein the teeth of each of the combs of the first and second portions have a selected height and length to provide a selected capacitance.

4. The integrated circuit memory device of claim **1**, wherein the predetermined pattern forms a substantially serpentine gap of a selected width between the first and second portions to provide a selected capacitance between the first and second portions.

5. The integrated circuit memory device of claim **1**, wherein the multi-resistive memory array includes a magnetic random access memory (MRAM) device.

6. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion each have a structure arranged relative to one another to provide a maximum amount of juxtaposed surface area between the first and second portions; and

a layer of insulation material disposed at least between the first and second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

7. An integrated memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor and an amplifier operably connected to the capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area between the first and second portions; and

a layer of insulation material disposed at least between the first and second portions;

the amplifier includes:

an output;

an inverting input;

a first switch between the output to the inverting input;

a non-inverting input connected to the capacitor;

a second switch between the non-inverting input and ground; and

a switch between the non-inverting input and the capacitor; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

8. The integrated circuit memory device of claim **7**, wherein the multi-resistive memory array includes a plurality of column lines and a plurality of row lines, and wherein the circuit includes a multiplexor connected to the output of the amplifier and one of the plurality of column lines and the plurality of row lines to provide the stable voltage.

9. The integrated circuit memory device of claim **7**, wherein the multi-resistive memory array includes a plurality of column lines and a plurality of row lines, one of the plurality of column lines and the plurality of row lines being operatively connected to the sensor device.

10. The integrated circuit memory device of claim **7**, wherein the capacitor nullifies an offset voltage of the amplifier and is independent of voltage and frequency changes in an input signal applied to the non-inverting input and the inverting input.

11. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area;

a layer of insulation material disposed between and over the first and second portions;

a reference plate disposed on the layer of insulation material and over the first and second portions; and

at least one contact electronically connecting the reference plate to one of the first or second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

12. The integrated circuit memory device of claim **11**, wherein the at least one contact is a plug of conductive material disposed in a opening through the layer of insulation.

13. The integrated circuit memory device of claim **12**, wherein the plug is formed from one of tungsten, copper, aluminum or an alloy of tungsten, copper and aluminum.

14. The integrated circuit memory device of claim **11**, wherein the circuit includes and amplifier the comprises:

an output;

an inverting input;

a first switch between the output to the inverting input;

a non-inverting input connected to the capacitor;

a second switch between the non-inverting input and ground; and

a third switch between the non-inverting input and the capacitor.

15. The integrated circuit memory device of claim **14**, wherein the multi-resistive memory array includes a plurality of column lines, and wherein the circuit includes a multiplexor connected to the output of the amplifier and the plurality of column line s to provide the stable voltage.

16. The integrated circuit memory device of claim **14**, wherein the multi-resistive memory array includes a plurality of column lines and a plurality of row lines, one of the plurality of column lines and the plurality of row lines being operatively connected to the sensor device.

17. The integrated circuit memory device of claim **14**, wherein the multi-resistive memory array includes a magnetic random access memory (MRAM) device.

18. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion each have a substantially comb-like structure with a plurality of teeth, the teeth of the first portion and the second portion being interleaved and each tooth including a pair of sidewalks, each sidewall except an outside sidewall of an end tooth facing a sidewall of a tooth of the other portion to provide a maximum amount of juxtaposed surface areas;

a layer of insulation material disposed between and over the first and second portions;

a reference plate disposed on the layer of insulation material and over the first and second portions; and

at least one contact electrically connecting the reference plate to one of the first or second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

19. The integrated circuit memory device of claim **18**, wherein the sidewall of each tooth has a selected height and length to provide a selected capacitance.

20. The integrated circuit memory device of claim **18**, further comprising a substantially serpentine gap of a selected width between the first and second portions to provide a selected capacitance between the first and second portions.

21. The integrated circuit memory device of claim **18**, wherein the circuit includes an amplifier that comprises:

an output;

an inverting input;

a first switch between the output to the inverting input;

a non-inverting input connected to the capacitor;

a second switch between the non-inverting input and ground; and

a third switch between the non-inverting input and the capacitor.

22. The integrated circuit memory device of claim **21**, wherein the multi-resistive memory array includes a plurality of column lines and a plurality of rows lines, and wherein the circuit includes a multiplexor connected to the output of the amplifier and one of the plurality of column lines and the plurality of row lines to provide the stable voltage.

23. The integrated circuit memory device of claim **21**, wherein the multi-resistive memory array includes a plurality of column lines and a plurality of row lines, one of the plurality of column lines and the plurality of row lines being operatively connected to the sensor device.

24. The integrated circuit memory device of claim **18**, wherein the multi-resistive memory array includes a magnetic random access memory (MRAM) device.

25. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a first reference plate of conductive material disposed on the substrate;

a first layer of insulation material covering the first reference plate;

a layer of conductive material formed on the first layer of insulation material, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area;

a second layer of insulation material disposed between and over the first and second portions;

a second reference plate disposed on the second layer of insulation material and over the first and second portions; and

at least one contact electrically connecting at least one of the first and second reference plates to at least one of the first or second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

26. The integrated circuit memory device of claim **25**, wherein the at least one contact is a plug of conductive material disposed in a opening through at least one of the first or second layers of insulation.

27. The integrated circuit memory device of claim **26**, wherein the plug is formed one of tungsten, copper, aluminum or an alloy of tungsten, copper and aluminum.

28. The integrated circuit memory device of claim **25**, wherein the circuit includes an amplifier connected to the capacitor and a multiplexor connected to the amplifier and the multi-resistive memory array.

29. The integrated circuit memory device of claim **28**, wherein the multi-resistive memory array includes a magnetic random access memory device.

30. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a circuit connected to the multi-resistive memory array and adapted to provide a stable voltage to the multi-resistive memory array, the circuit including a capacitor, the capacitor includes:

a substrate;

a first reference plate of conductive material disposed on the substrate;

a first layer of insulation material covering the first reference plate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion each have a substantially comb-like structure with a plurality of teeth, the teeth of the first portion and the second portion being interleaved and each tooth including a pair of sidewalls, each sidewall except an outside sidewall of an end tooth facing a sidewall of a tooth of the other portion to provide a maximum amount of juxtaposed surface area;

a second layer of insulation material disposed between and over the first and second portions;

a second reference plate disposed on the second layer of insulation material and over the first and second portions; and

at least one contact electrically connecting at least one of the first and second reference plates to at least one of the first or second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

31. The integrated circuit memory device of claim **30**, wherein the sidewalls of each tooth has a selected height and length to provide a selected capacitance.

32. The integrated circuit memory device of claim **30**, wherein the interleaved comb-like structures form a substantially serpentine gap of a selected width between the first and second portions to provide a selected capacitance between the first and second portions.

33. The integrated circuit memory device of claim **30**, wherein the multi-resistive memory array includes a magnetic random access memory device.

34. An integrated circuit memory device, comprising:

a multi-resistive memory array;

a means for providing a stable voltage to the multi-resistive memory array, the means for providing a stable voltage being coupled to the multi-resistive memory array and including a capacitor, the capacitor includes:

a substrate;

a layer of conductive material formed on the substrate, the layer of conductive material including at least a first portion and a second portion, wherein the first portion and the second portion are arranged in a predetermined pattern relative to one another to provide a maximum amount of juxtaposed surface area between the first and second portions; and

a layer of insulation material disposed at least between the first and second portions; and

a sensor device connected to the multi-resistive memory array and adapted to read information from the multi-resistive memory array.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,109,545 B2
APPLICATION NO. : 10/318971
DATED : September 19, 2006
INVENTOR(S) : Baker et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 10, line 27, in Claim 7, after “integrated” insert -- circuit --.

In column 10, line 52, in Claim 7, after “a” insert -- third --.

In column 11, line 25, in Claim 11, delete “electronically” and insert -- electrically --, therefor.

In column 11, line 39, in Claim 14, delete “and” and insert -- an --, therefor.

In column 11, line 39, in Claim 14, after “amplifier delete “the” and insert -- that--, therefor.

In column 11, line 53, in Claim 15, delete “line s” and insert -- lines --, therefor.

In column 12, line 9, in Claim 18, delete “sidewalks,” and insert -- sidewalls, --, therefor.

In column 12, line 12, in Claim 18, delete “areas;” and insert -- area; --, therefor.

In column 12, line 43, in Claim 22, delete “rows” and insert -- row --, therefor.

In column 13, line 22, in Claim 27, after “formed” insert -- from --.

Signed and Sealed this

Sixth Day of March, 2007

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office