Determining the Effects of Package Parasitics on SI and EMC Performance

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Abstract

Signal Integrity and EMC problems are significantly affected by integrated circuit package parasitics. Such effects can be especially problematical for cases where devices undergo a die shrink in the same package. A simple method of determining the effects of package parasitics for a broad class of chip packages is described. Once significant noise due to package parasitics is identified, it may not actually result in a problem. A method is presented to determine when the observed noise will actually become a problem. Examples of problems that have occurred and how to avoid them are presented. New insight will also be provided on die to heat sink coupling of high frequency signals.

Keywords: signal integrity, EMC, IC packages, noise, IC evaluation, measurement methods

Overview and History

Determining the effects of package parasitics of an integrated circuit, IC, on circuit operation is very important. This is especially true when the IC undergoes a die shrink. The new chip is usually smaller and faster, both of which cause the package parasitics to become more of a problem.

The main package parasitic this paper will be concerned with is the inductance of the connections in the package. An inductance of these connections of just a few nanohenries can cause significant signal integrity, SI, and EMC issues. Sometimes, the problems caused by package inductance can be difficult to track down.

A basic method of quickly determining the effect of package inductance on chip operation was described in a 1997 paper by the author.[1] In this paper, that method is refined and expanded to include EMC problems as well as SI problems and also to include capacitive coupling to metal in contact with the IC package, such as a heat sink.

The method described in this paper has been used by the author many times to track down system SI and EMC problems where other methods have either failed or took excessive time to find the problem caused by IC package inductance. In one case, such a problem put a "stop ship" on all of a company's products for almost two months! Application of the method described here found the problem in only one morning of work.

Let's start with a discussion of inductively coupled measurement of the effect of package parasitics. The goal will be to measure the inductive voltage drop across leads in the IC package ***and*** determine if the measured voltage will be a problem in circuit operation.

Inductively Coupled Measurements

If a simple square wire loop is positioned on the surface of an IC package as shown in Figure 1, a voltage will be induced into the loop. This voltage is equal to Mdi/dt where the di/dt is of currents flowing in the package's internal connections (and to a small extent in the chip itself) and M is the mutual inductance between the loop and the currents flowing in the package. The voltage drop across an internal connection in the package is Ldi/dt where di/dt is of the current flowing in the connection and L is the inductance of the internal connection.

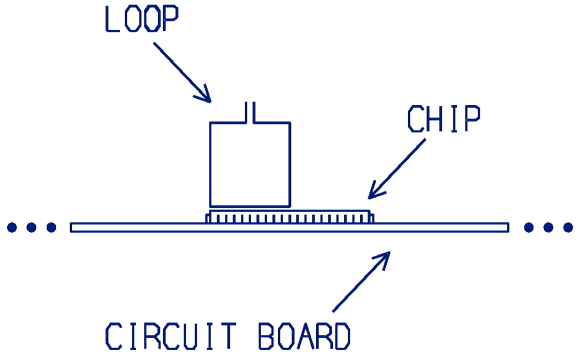

Figure 1. Wire loop positioned over an IC. [2]

M will be less than L so the output of the loop is a lower bound estimate of the voltage drop across the inductance of the internal connections in the IC package. In general, I have found that M is on the order of one quarter of L although it may be higher or lower than that.

Although a shielded loop, such as EMC engineers use to minimize electric field pickup has a slight advantage, the electric field contribution to the output of the loop is generally not significant in this application so a simple wire loop can be used. To check the electric field contribution to the loop output, simply reverse the loop. The output waveform should invert. Any other change in the waveform is due to electric field coupling.

Since the loop output is dependent on the loop capturing the magnetic fields generated by currents flowing in the package, this method will not work if there is metal on the top if the package, such as a heat spreader or heat sink. Access to the bare package is required for the time it takes to do the test. This measurement method works well for flat packs with pins around the perimeter (as shown in Figure 1) and for ball grid arrays.

Since the mutual inductance between the loop and a specific connection in the package falls off quickly with distance and orientation, the output of the loop can be attributed to a small group of pins on a flat pack. The group of pins contributing to the loop output for a ball grid array is much larger so the pin resolution is coarser, but the method described in the next section is still useful.

To prevent unwanted reflections and resonances that will give incorrect readings, the loop should be connected using a high quality 50Ω coax cable to the 50Ω input of an oscilloscope. Without a 50Ω termination, one can get some very interesting but not very useful waveforms on the oscilloscope.

Basic Method for Signal Integrity

The method can be used to find both SI and EMC problems. For SI problems, the method is as follows:

1. Make a square loop whose side is about one half the diameter of the IC package as shown n Figure 1.
2. Slowly rotate the loop with one corner fixed at the center of the IC package. As noise is induced in the loop, maximize it at each orientation of the loop using infinite persistence or by varying the trigger level of the oscilloscope.
3. At each orientation where the loop output exceeds 50 mV, place a pencil mark where the loop was. Those orientations where an output of 50 mV can be observed are important because the inductive drop across the package internal connections under the loop is approximately 4*50mV or about 200 mV. 200 mV is a significant portion of the noise budget.
4. After marking the chip, go back to each pencil mark and fix the loop there. Trigger on the loop output and using a voltage probe appropriate to the signals, measure the chip outputs to see if the noise glitch shows up at an important time.

If there are no locations resulting in a 50 mV output of the loop, step 4 may be eliminated. The voltages across the package inductances are acceptable for most digital applications.

Figure 2 shows an example of positioning the loop on top of a flat pack. The loop used here is a fancy shielded loop in a plastic cover, but a simple wire loop will work as well. A small bent paperclip makes a good loop for this purpose.

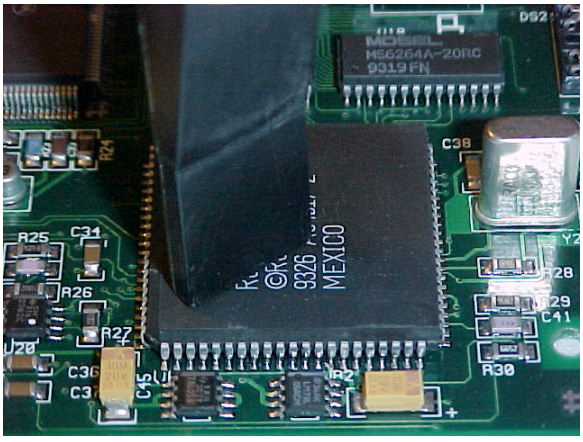

Figure 2. Rotate the loop keeping a corner fixed at the center of the IC package.[2]

Signal Integrity Data

Figure 3 shows waveforms from an actual problem IC. Originally, the chip was in 3.5 micron CMOS and had undergone a die shrink to 1.8 micron CMOS technology. The resulting problem shut down the company's production for almost two months. After taking weeks to find the problem with a logic analyzer, the method of this paper captured the waveform in Figure 3 after only a morning's work.

The lower trace in Figure 3 is the output of the loop. The actual peak of the loop output was 400 mV! That would translate to about 1.6 to 2 Volts drop across the package connection(s) under the loop. There was really no need to go further here, that much drop in an IC package is unacceptable.

The upper trace of Figure 3 is an output of the chip that was routed to an edge triggered input of another chip. Once this scope plot was obtained showing the two-Volt glitch, the problem was obvious.

The time delay in the loop probe cable and scope probe was slightly different. In addition, the glitch in the upper trace could move through a range of five to ten nanoseconds earlier than its position in Figure 3 in response to the operation of system software. Sometimes the glitch was imbedded in the falling edge and barely noticeable, but occasionally it would move out on the base line where it resulted in severe system problems.

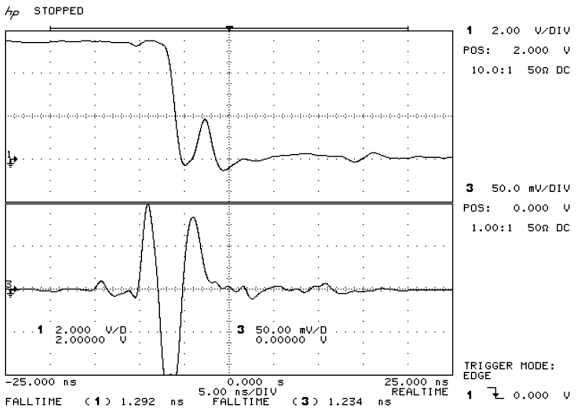

Figure 3. Loop output, lower trace, and IC output pin, upper trace, show the problem.[2]

Signal integrity problems are often bit pattern sensitive, as was the case for the example just cited. In that case, the problem happened when all the bits of a bus were changed from high to low simultaneously. So the result is usually an isolated pulse such as the one shown in Figure 4. The probability of seeing a worst-case pulse like this can be low requiring some waiting time to catch it.

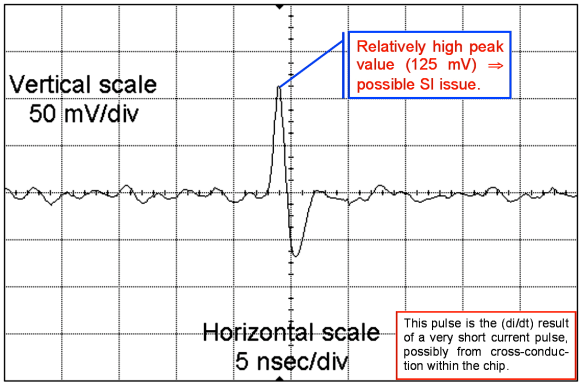

Figure 4. Example of a typical SI problem.[2]

Figure 4 shows a pulse with a peak of ~125 mV, enough to attract attention since this could translate into ~600 mV across a lead in the IC package, most likely a power or ground connection. In fact, looking at Figure 4, the trace is almost certainly due to current in power or ground. Remember, that the loop output is Mdi/dt. To see the actual current flowing, the waveform in Figure 4 must be integrated. The positive going peak is one edge of a current change and the negative going peak is most likely the opposite polarity edge of the same current change. Since most logic families have a stronger pull down than a pull up, the trace seems to show a current that pulls to ground immediately followed by a pull up, with no middle.

Usually a signal will change state and have a "flat" region before changing state again, usually in response to a clock signal or its derivative. The fact that there is no time between the edges in Figure 4 suggest the current is due to conduction through a totem-pole output that can occur during logic transitions. This is sometimes called "shoot-through" or "cross conduction" and can be much larger in amplitude than normal logic currents, but for a short time. The rise and fall times of the (integrated) current in Figure 4 are on the order of a few nanoseconds, commensurate with the age of the IC which was in an older modem.

Since current peaks like that from Figure 4 are usually bit pattern dependent, it may take some time to insure the peak value has been recorded. Sometimes, special versions of the software can be used to increase the likelihood of seeing a worst case event quickly.

Basic Method for EMC

The basic method to find EMC problems due to inductive drop in the package causing ground or power bounce is similar to the procedure for SI except for two points:

1. The signals picked up in the loop can be much smaller and cause EMC problems. A few tens of millivolts is more than enough.
2. The signals picked up by the loop that cause EMC problems are generally continuous signals driven by the clock and are not bit pattern dependent.

A resonant structure, like a 1/2 λ dipole, can radiate enough to cause an emissions problem when driven by as little as a couple of millivolts at a given frequency. A loop output of 10 mV implies the chip die is bouncing on the order of four times that, ~40 mV, with respect to the board ground planes, enough to potentially cause EMC problems.

EMC Data

Data taken from a large IC package using about a 2 cm square loop is shown in Figure 5. A peak reading of 13 mV was observed. The frequency of the larger peaks (three shown on the plot) is 125 MHz, the clock frequency, while the smaller peaks are the third harmonic of the clock at 375 MHz.

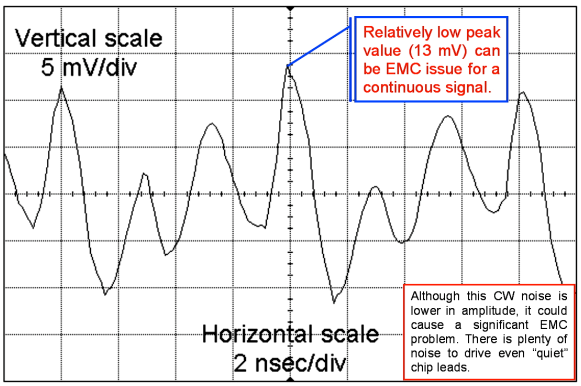

Figure 5. Example of a typical EMC problem.[2]

One output of the chip was used to drive an LED on the faceplate of the board, almost all the way across the length of the board. Since the signal was just "DC" the designers thought it was not necessary to pay attention to routing of this signal. The routing took the LED signal across a few ground plane breaks dividing areas of the board, normally not a good idea, but this was just a DC signal. Right?

It turns out the length of this path was 1/4 λ long at 375 MHz and the board had a severe emissions problem at that frequency. My favorite fix for this kind of problem is what I call "digilog" design, a combination of digital and analog techniques. In this case, the dropping resistor for the LED could be moved as close to the IC as possible and then a 1000 pF capacitor to the ground plane added after the resistor to make the signal truly a "DC" signal. After that, routing of the LED signal would be much less critical.

It is probably safe to assume than any large IC has tens of millivolts of ground bounce and is capable of driving external structures to an emissions problem. All signals from a large IC should be assumed to be EMI hot unless proven otherwise.

Capacitively Coupled Measurements

Up to this point, measurements have been made through mutual inductance between the conductors in the IC package and a square wire loop sized to fit the IC package. One can also make capacitively coupled measurements. They are not as useful for finding problems but do give insight into the circuit operation and give a hint of what may be coupled onto heatsinks.

Figure 6 shows an IC package with copper tape affixed to the top of the package. An Agilent 1158a, 4 GHz active probe was used to measure the voltage between the copper tape and the board ground plane.

What we really have here is a capacitive divider between the chip/lead frame capacitance to the copper tape and the capacitance of the probe input (with the high DC input resistance of the probe in parallel with its input capacitance). The capacitance between the chip and lead frame and the copper tape is probably on the order of a few picofarads whereas the probe input capacitance is on the order of 1/4 of a picofarad, so most of the average voltage across the surface of the chip and lead frame will appear as an input to the probe. If one wanted to measure only the die surface, cut the copper tape to match the die size.

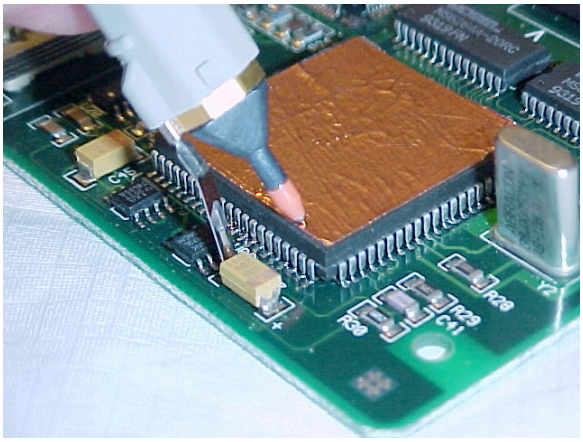

Figure 6. Capacitively couple measurement.[2]

Figure 7 shows the result for an older chip used in a modem. The transitions are occurring at roughly 50 ns intervals, showing the clock speed of this circuit to be about 20 MHz.

Each step in the plot corresponds to part of the chip and lead frame rising or falling in voltage. Starting just to the left of center we see a rise of about 300 mV. 50 ns later more of the chip surface goes high pushing the plot up another 400 mV to a peak of about 700 mV. 50 ns later, the trace falls a little and 50 ns after that, it falls ~ 600 mV to a value a bit below zero. Since the measurement is AC coupled, the average voltage must be zero over time and the area under the trace above and below the zero voltage line, the center of the screen, must be equal over time as well.

The peak voltage of 700 mV is a significant fraction of the five Volt supply. One can see that

significant noise may be coupled onto heat sinks by the underlying chip.

One of my clients had a problem where noise at 4.7 GHz was coupled onto a heat sink. As Murphy's Law would have it, the tines on the heat sink were resonant right at 4.7 GHz turning the heat sink into a really nice phased array at 4.7 GHz (third harmonic of the chip clock).[3] Needless to say, a rather severe emissions problem resulted

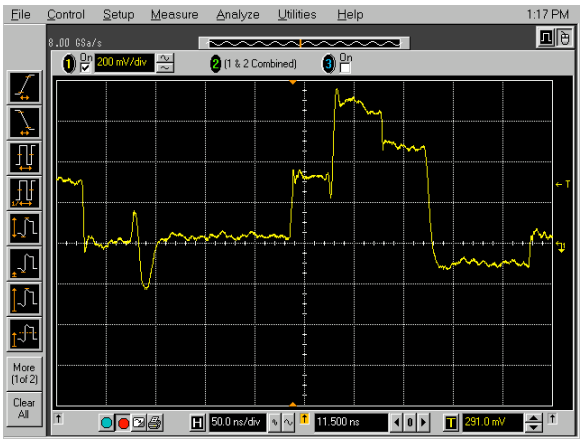

Figure 7. Measured voltage on copper foil for modem IC.[2]

Figure 8 shows another plot from the same chip used in Figures 6 and 7 with a few differences. First, the flat portion of the waveform is long enough that one can see "droop" due to the input resistance of the probe charging up the package to copper tape capacitance.

Also shown in the figure is the Fast Fourier Transform, FFT, of the upper trace shown as the lower trace. The amplitude scale is 20 dB/div and the frequency scale is 50 MHz/division. One can see the bandwidth of the signal is around 150 MHz or so.

A risetime in the plot of about 5 ns can be seen. I believe this is the risetime of the voltage change on the surface of the chip, possibly slowed somewhat by the capacitance between the copper foil and its surroundings.

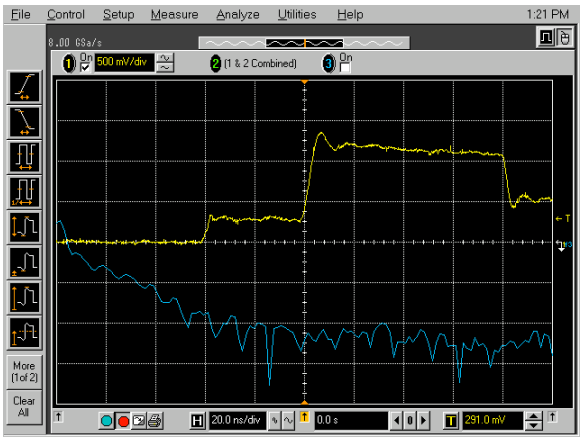

Figure 8. Another plot from modem chip.[2]

Summary and Conclusion

Measurements made through inductive or capacitive coupling from the top of IC packages can be used to find SI and EMC problems and to help understand coupling to heatsinks from ICs.

Simple methods were given to find SI and EMC problems using mutual inductance. Both the amplitude of the loop output and its use as a trigger to measure signals are important to troubleshooting problems in designs.

Capacitively coupled measurements, although not as useful for troubleshooting as inductively coupled measurements, help lead to an understanding of chip operation and coupling to heatsinks.

References

[1] *A Method for Troubleshooting Noise Internal to an IC,* Douglas C. Smith, Proceedings of the 1997 IEEE EMC Symposium, pp. 223-225.

[2] Picture from private seminars on high frequency measurements and troubleshooting of electronic circuits, D. C. Smith, 1988-2007, used with permission.

[3] *Measuring Structural Resonances*, Technical Tidbit - June 2006, High Frequency Measurements Web Page, http://emcesd.com/tt2006/tt060306.htm